

UNIVERSITÉ DE SHERBROOKE
Faculté de génie
Département de génie mécanique

Fiabilité de l'underfill et estimation de la
durée de vie d'assemblages microélectroniques

Underfill Reliability and Life Estimation in Microelectronic
Assemblies

Thèse de doctorat
Specialité: génie mécanique

Ying YANG

Sherbrooke (Québec) Canada

Avril 2022

JURY MEMBERS

Julien Sylvestre

Supervisor

Hélène Frémont

Examiner

Papa Momar Souare

Examiner

Elijah Van Houten

Examiner

RÉSUMÉ

Afin de protéger les interconnexions dans les assemblages, une couche de matériau d'underfill est utilisée pour remplir le volume et fournir un support mécanique entre la puce de silicium et le substrat. En raison de la géométrie du coin de puce et de l'écart du coefficient de dilatation thermique (CTE), l'underfill souffre d'une concentration de contraintes dans les coins lorsque la température est inférieure à la température de cuisson. Cette concentration de contraintes conduit à des défaillances mécaniques dans les encapsulations de flip-chip, telles que la délamination interfaciale puce-underfill et la fissuration d'underfill. Les contraintes et déformations locales sont les paramètres les plus importants pour comprendre le mécanisme des ruptures de l'underfill. En conséquent, l'industrie utilise actuellement la méthode des éléments finis (EF) pour calculer les composantes de la contrainte, qui ne sont pas assez précises par rapport aux contraintes actuelles dans l'underfill. Ces simulations nécessitent un examen minutieux de détails géométriques importants et des propriétés des matériaux.

Cette thèse vise à proposer une approche de modélisation permettant d'estimer avec précision les zones de délamination et les trajectoires des fissures dans l'underfill, avec les trois objectifs suivants. Le premier objectif est de mettre au point une technique expérimentale capable de mesurer la déformation de l'underfill dans la région du coin de puce. Cette technique, combine la microscopie confocale et la méthode de corrélation des images numériques (DIC) pour permettre des mesures tridimensionnelles des déformations à différentes températures, et a été nommée le technique confocale-DIC. Cette technique a d'abord été validée par une analyse théorique en déformation thermique. Dans un échantillon similaire à un flip-chip, la distribution de la déformation obtenues par le modèle EF était en bon accord avec les résultats de la technique confocal-DIC, avec des erreurs relatives inférieures à 20% au coin de puce. Ensuite, le second objectif est de mesurer la déformation autour d'une fissure dans l'underfill. Des fissures artificielles d'une longueur de 160 μm et 640 μm ont été fabriquées dans l'underfill vers la direction diagonale de 45°. Les déformations circonférentielles maximales et principale maximale étaient situées aux pointes des fissures correspondantes. Un modèle de fissure a été développé en utilisant la méthode des éléments finis étendue (XFEM), et la distribution des contraintes dans la simulation a montré la même tendance que les résultats expérimentaux. La distribution des déformations circonférentielles maximales était en bon accord avec les valeurs mesurées lorsque la taille des éléments était plus petite que 22 μm , assez petit pour capturer le grand gradient de déformation près de la pointe de fissure. Le troisième objectif était d'apporter une approche de modélisation de la délamination et de la fissuration de l'underfill avec les effets des variables de fabrication. Un test de cyclage thermique a d'abord été effectué sur 13 cellules pour obtenir les zones délaminées entre la puce et l'underfill, et les profils de fissures dans l'underfill, comme référence. Un réseau neuronal artificiel (ANN) a été formé pour établir une liaison entre les effets des variables de fabrication et le nombre de cycles à la délamination pour chaque cellule. Les nombres de cycles prédits pour les 6 cellules de l'ensemble de test étaient situés dans les intervalles d'observations expérimentaux. La

croissance de la délamination a été réalisée par l'EF en évaluant l'énergie de la déformation au niveau des éléments interfaciaux entre la puce et l'underfill. Pour 5 des 6 cellules de la validation, le modèle de croissance du délaminage était conforme aux observations expérimentales. Les fissures dans l'underfill ont été modélisées par XFEM sans chemins prédéfinis. Les directions des fissures de bord étaient en bon accord avec les observations expérimentales, avec une erreur inférieure à $2,5^\circ$. Cette approche a répondu à la problématique qui consiste à estimer l'initiation des délamination, les zones de délamination et les trajectoires de fissures dans l'underfill pour des flip-chips industriels.

Mots-clés : Underfill, délamination, fissuration, fiabilité, modélisation

ABSTRACT

In order to protect the interconnections in flip-chip packages, an underfill material layer is used to fill the volumes and provide mechanical support between the silicon chip and the substrate. Due to the chip corner geometry and the mismatch of coefficient of thermal expansion (CTE), the underfill suffers from a stress concentration at the chip corners when the temperature is lower than the curing temperature. This stress concentration leads to subsequent mechanical failures in flip-chip packages, such as chip-underfill interfacial delamination and underfill cracking. Local stresses and strains are the most important parameters for understanding the mechanism of underfill failures. As a result, the industry currently relies on the finite element method (FEM) to calculate the stress components, but the FEM may not be accurate enough compared to the actual stresses in underfill. FEM simulations require a careful consideration of important geometrical details and material properties.

This thesis proposes a modeling approach that can accurately estimate the underfill delamination areas and crack trajectories, with the following three objectives. The first objective was to develop an experimental technique capable of measuring underfill deformations around the chip corner region. This technique combined confocal microscopy and the digital image correlation (DIC) method to enable tri-dimensional strain measurements at different temperatures, and was named the confocal-DIC technique. This technique was first validated by a theoretical analysis on thermal strains. In a test component similar to a flip-chip package, the strain distribution obtained by the FEM model was in good agreement with the results measured by the confocal-DIC technique, with relative errors less than 20% at chip corners. Then, the second objective was to measure the strain near a crack in underfills. Artificial cracks with lengths of 160 μm and 640 μm were fabricated from the chip corner along the 45° diagonal direction. The confocal-DIC-measured maximum hoop strains and first principal strains were located at the crack front area for both the 160 μm and 640 μm cracks. A crack model was developed using the extended finite element method (XFEM), and the strain distribution in the simulation had the same trend as the experimental results. The distribution of hoop strains were in good agreement with the measured values, when the model element size was smaller than 22 μm to capture the strong strain gradient near the crack tip. The third objective was to propose a modeling approach for underfill delamination and cracking with the effects of manufacturing variables. A deep thermal cycling test was performed on 13 test cells to obtain the reference chip-underfill delamination areas and crack profiles. An artificial neural network (ANN) was trained to relate the effects of manufacturing variables and the number of cycles to first delamination of each cell. The predicted numbers of cycles for all 6 cells in the test dataset were located in the intervals of experimental observations. The growth of delamination was carried out on FEM by evaluating the strain energy amplitude at the interface elements between the chip and underfill. For 5 out of 6 cells in validation, the delamination growth model was consistent with the experimental observations. The cracks in bulk underfill were modelled by XFEM without predefined paths. The directions

of edge cracks were in good agreement with the experimental observations, with an error of less than 2.5° . This approach met the goal of the thesis of estimating the underfill initial delamination, areas of delamination and crack paths in actual industrial flip-chip assemblies.

Keywords: Underfill, delamination, cracking, reliability, modeling

À mes parents.

ACKNOWLEDGEMENTS

Tout d’abord, je voudrais adresser mes remerciements à mon directeur de recherche Pr. Julien Sylvestre, qui m’a fourni l’opportunité de réaliser ce projet de recherche. J’ai appris de sa merveilleuse expérience dans le domaine de l’encapsulation microélectronique. Il m’a permis de découvrir la domaine de la fiabilité microélectronique et d’améliorer mes compétences de recherche. Je tiens à lui exprimer ma gratitude pour ses conseils, son soutien et son apprentissage pendant mes études. Je remercie également les membres de mon comité de jury Hélène Frémont, Papa Momar Souare et Elijah Van Houten pour leurs évaluations et conseils.

Ensuite, je veux remercier IBM Canada Ltée et le conseil de recherches en sciences naturelles et en génie du Canada (CRSNG) qui a soutenu ce projet financièrement et en mettant toutes les ressources dont j’avais besoin pour mon projet. Egalement le centre de collaboration C2MI, qui m’a aidé de traiter certains essais dans leur laboratoire. Mes remerciements vont spécialement à Éric Duchesne, Papa Momar Souare et Catherine Dufort qui ont participé aux soutiens techniques et réflexions pour ce projet.

Je remercie l’Université de Sherbrooke, la Faculté de Génie et le 3IT, pour leur accueil et encadrement. Mes remerciements vont aux professionnels de recherches et techniciens de laboratoires, pour leur soutien et aide. Je remercie aussi mes collègues Mamadou, Jean-François, Omid, Wei, Liang, Habib, Payam, Abdellah, Assane et Anthony.

Enfin, je souhaite dire un grand merci à mes parents et amis, en particulier DaXiXi, Yi, Estelle et Max, pour leur soutien durant ces années d’étude. Merci à tous ceux qui ont contribué à cette thèse.

TABLE OF CONTENTS

1	INTRODUCTION	1
1.1	Research Background and Motivation	1
1.2	Definition of the Research Project	5
1.3	Roadmap of Underfill Reliability Estimation	7
1.3.1	Perfect Model for Underfill Reliability Estimation	8
1.3.2	Application of the Perfect Model	14
1.3.3	Challenges in Building the Perfect Model	14
1.4	Objectives	18
1.4.1	General Objective	18
1.4.2	Sub-objectives	18
1.5	Outline of the Thesis	20
2	THE STATE OF THE ART	23
2.1	Flip-chip Packages and Underfill Failure	23
2.1.1	Underfill Process in Flip-Chip Packages	23
2.1.2	Material System of Flip-Chip Packages	24
2.1.3	Underfill Failure Modes	25
2.1.4	Influence of Underfill Failure on the Reliability of Assembly	28
2.1.5	Mechanisms of Underfill Failure	29
2.2	Analytical Solutions for Stress Distribution at Corners and Crack Regions	30
2.2.1	Stress Singularity	31
2.2.2	Solutions on a Bimaterial Corner and a Crack	31
2.3	Experimental Approaches on Fracture Properties and Local Strain Evaluation	34
2.3.1	Fracture Properties Test	35
2.3.2	Carbon Nanotube Strain Sensor	36
2.3.3	Digital Image Correlation Method	37
2.3.4	Other Techniques for Underfill Strain Measurements	40
2.4	Numerical Simulations of Underfill Cracking and Delamination	41
2.4.1	Finite Element Method for Underfill Modeling	41
2.4.2	Modeling Underfill Cracks	42
2.4.3	Modeling Interfacial Delamination	44
2.4.4	Fatigue Life Model	47
2.4.5	Crack Modeling for Particle Composites	49
2.4.6	Stochastic Modeling for Fractures	50
2.5	Summary	51
3	Using Confocal-DIC to Measure Local Strains around a Chip Corner and a Crack Front	55
3.1	Avant-propos	55
3.2	Résumé	57

3.3	Abstract	58
3.4	Introduction	59
3.5	Experiments	61
3.5.1	Setup	61
3.5.2	Materials and Samples	63
3.6	Modeling	65
3.7	Results and Discussion	66
3.7.1	Deformation Validation by CTE	66
3.7.2	Comparison of Underfill Corner Strain between Experimental and Numerical Results	68
3.7.3	Comparison of Crack Tip Strain between Experimental and Numerical Results	70
3.8	Conclusions	71
4	Study of Underfill Corner Cracks by the Confocal-DIC and Phantom-Nodes Method	75
4.1	Avant-propos	75
4.2	Résumé	77
4.3	Abstract	78
4.4	Introduction	79
4.5	Experiments	82
4.5.1	Samples	82
4.5.2	Confocal-DIC Method	84
4.6	Modeling	85
4.6.1	XFEM Phantom-Nodes Method	85
4.6.2	Numerical Model	87
4.7	Results and Discussion	89
4.7.1	Experimental Results	89
4.7.2	Comparison and Improvements of Numerical Model from Experimental Results	91
4.7.3	Order of Stress Singularity	96
4.7.4	Discussion on the Current Model Limitations	99
4.8	Conclusions	102
5	Modeling of Flip-Chip Underfill Delamination and Cracking with Five Input Manufacturing Variables	105
5.1	Avant-propos	105
5.2	Résumé	107
5.3	Abstract	108
5.4	Introduction	109
5.5	Reliability Tests	113
5.5.1	Samples and Test Procedure	113
5.5.2	Characterization Methods	115
5.6	Modeling	115
5.6.1	ANN Modeling of Delamination Initiation	115

5.6.2	Finite Element Models	121
5.7	Results and Discussion	127
5.7.1	Initiation of Chip-Underfill Delamination	127
5.7.2	Propagation of Chip-Underfill Delamination	132
5.7.3	Underfill Cracking Angles	136
5.8	Conclusions	140
6	ENGLISH CONCLUSION	143
6.1	General Conclusions	143
6.2	Perspectives for Future Work	147
7	CONCLUSION FRANÇAISE	149
7.1	Conclusions Générales	149
7.2	Perspectives pour les Travaux Futurs	154
	LIST OF REFERENCES	157

LIST OF FIGURES

1.1	Typical flip-chip package. [8]	2
1.2	(a) Conventional, (b) no-flow, (c) molded and (d) wafer-level underfill. [5]	3
1.3	Typical temperature profile for thermal cycle test conditions. [13]	4
1.4	Roadmap of underfill reliability estimation.	8
1.5	Diagram of the perfect model.	10
1.6	Typical survival-functional graph. The N_{10} , N_{50} , and N_{90} points are shown, representing the times when 10%, 50%, and 90% of the samples have failed.	15
1.7	Progression of the three sub-objectives based on the levels of model characteristics in Table 1.6.	20
2.1	Conventional flip-chip process. [24]	23
2.2	Cross-section of underfill area. [7]	24
2.3	Delaminations from the sidewalls in a micrograph of a cross-section leaving a 25 μm underfill film on the sidewall. [34, 37]	26
2.4	(a) C-SAM image of an underfill test vehicle after moisture exposure at 30 $^{\circ}\text{C}$ /60% relative humidity for 192 h, followed by three reflows at 250 $^{\circ}\text{C}$, (b) cross-sectional view of area X at AA'. [38]	26
2.5	Cracks propagation in the underfill toward the substrate. The cross-sectional plane is perpendicular to the chip sidewall. [34, 39]	27
2.6	Underfill crack growth toward the external underfill fillet. [34, 40]	27
2.7	Cracks propagation in the BOEL. [41, 42]	28
2.8	Cracks propagation in the solder joints. [43]	28
2.9	Cross-section of the solder joint zone. [39]	29
2.10	Order of stress singularity λ for rectangular corner $\alpha = 90^{\circ}$. The solid lines represent $\text{Re}\lambda$ for perfect adhesion ($\text{Im}\lambda$ vanishes), dashed and dash-dotted line represents $\text{Re}\lambda$ and $\text{Im}\lambda$ for delaminated interface. (a) $(\kappa_1, \kappa_2) = (1.0, 1.0)$, (b) $(\kappa_1, \kappa_2) = (1.0, 2.2)$, (c) $(\kappa_1, \kappa_2) = (2.2, 1.0)$, (d) $(\kappa_1, \kappa_2) = (2.2, 2.2)$. [64]	32
2.11	Order of singularity for 3D corners. [62]	33
2.12	Three modes of crack propagation. [65]	33
2.13	Order of singularity for wedge-shaped cracks. [62]	34
2.14	Diagram of the double cantilever beam test. P is the force load, h and b are the height and width of the beam. [73]	35
2.15	Typical Raman spectra of MWCNT and Epoxy between 1000-3000 cm^{-1} . [77]	37
2.16	Shift in G' band with compression strain. [55]	38
2.17	(a) Area of interest (AOI) and subsets in a reference image; (b) schematic presentation of a reference subset before deformation and the corresponding target subset after deformation. [86]	38
2.18	Sample mounting configuration in the micro-CT system. [87]	39

2.19	(a) Schematic of uniaxial constrained compression of a spherical inclusion in a matrix with a sliding interface, (b) experimentally measured strain field ϵ_{33} near a spherical inclusion. [91]	40
2.20	Strain contour ϵ_y on the X-section at 100°C. [92]	40
2.21	Finite element flow chart for semiconductor packaging modeling. [95]	42
2.22	Typical subdivision of elements intersected by a crack. [111]	43
2.23	Schematic concept of the Virtual Crack Closure Technique. An interface crack of length a is extended a small amount Δa when the energy released equals the interface toughness G_{Ic} . [123]	45
2.24	Schematic of interface elements. [112]	45
2.25	Typical bilinear cohesive law. [112]	46
2.26	Typical FEM model for the underfill delamination. [127]	46
2.27	Typical relationship between the crack growth rate and stress intensity amplitude. [134]	48
2.28	(a) Circular interface corner delamination between silicon/epoxy interface, (b) finite element mesh, and (c) the advancing circular corner delamination. [132]	48
2.29	Crack-particle interaction in a particulate system showing three possible fracture mechanisms, namely particle fracture, crack deflection and interface debonding. [146]	49
2.30	(a) Central crack configuration, where W , L , B , $2a$ and σ are the width, length, thickness, initial crack length and applied load of the sample, (b) crack length with respect to the number of cycles for the result regions of MCS and SPSEM. [157]	51
3.1	(a) General principle of the laser scanning confocal microscopy; left: incident laser illuminating the sample, right: pinhole accepting the reflection from the focal plane, thus rejecting most out-of-focus light. (b) Typical 3-dimensional stacked image, with particle fillers dispersed in epoxy resin. (c) Diagram of the image processing.	62
3.2	Diagrams of the samples preparation: (a) non-constrained sample, (b) thin-layer sample, (c) chip-corner sample and its cross-section view, (d) 3-point bending sample with a prefabricated crack.	64
3.3	Finite element models of the (a) thin-layer sample, (b) chip-corner sample, (c) 3-point bending sample, with a round and a triangular crack front geometry.	66
3.4	(a) Strain components x (dashed line), y (dotted line) and xy (dot-dash line) in the non-constrained sample and the strain calculated from the CTE (solid line), with respect to loading temperatures. Error bars represent one standard deviation. (b) Typical strain images for one layer at 33.6°C, 43.4°C and 54.6°C.	67
3.5	Strain component x of the calculation (solid line) and the measurement (dashed line) with respect to vertical distance from the bi-material interface in the thin-layer sample at (a) 33.6°C, (b) 43.4°C and (c) 54.6 °C. Error bars represent one standard deviation. (d) Typical strain images at 54.6°C.	68

3.6	3-dimensional stacked images of the first principal strain near the chip corner at 60°C.	69
3.7	First principal strain at 60°C as a function of the distance from the chip corner in the diagonal direction, for the calculation with an element size of 24 μm (dashed line) and 40 μm (dotted line), and the measurements (triangle markers) with an exponential fitting curve (solid line). Error bars represent one standard deviation.	70
3.8	3-dimensional stacked images of the (a) strain component x, (b) strain component y, (c) first principal strain in front of the crack area.	71
3.9	Maximum first principal strain at the round crack tip (dashed line) and the triangular crack tip (dotted line) with respect to the element size.	72
3.10	First principal strain along the crack front direction in the calculation with a round crack front (dashed line) and a triangular crack front (dotted line), and the measurements (diamond markers) with an exponential fitting curve (solid line). Error bars represent one standard deviation.	73
4.1	(a) Sample diagram, (b) sample photo and (c) nominal dimensions of each component.	83
4.2	<i>In-situ</i> cooling observation setup.	84
4.3	General principle of the confocal-DIC technique: (a) incident laser illuminating the sample, (b) pinhole accepting the reflection from the focal plane and rejecting out-of-focus light, (c) calculating the strain tensor from captured images (the die corner is shown in gray), (d) photo of the LSCM. . .	86
4.4	Principle of XFEM based phantom-nodes method: (a) global mesh, (b) a superposition of sub-elements, $f(X)$ is the signed distance measured from the crack (dashed line).	87
4.5	XFEM model definition with an underfill crack: (a) quarter-symmetrical model, (b) sub-model of the selected region, (c) crack defined along the diagonal direction, shown by a red line.	88
4.6	XFEM sub-model definition of crack propagation: (a) sub-model of the underfill region, (b) initial crack at the chip corner, shown by a red line. . .	90
4.7	(a) and (b) 2-dimensional and (c) 3-dimensional images of the naturally initiated corner crack.	91
4.8	Strain component ϵ_θ and first principal strain ϵ_1 in the sample with a crack length of 160 μm . White lines represent the position of the etched crack. The die corner is shown in gray.	92
4.9	Strain component ϵ_θ and first principal strain ϵ_1 in the sample with a crack length of 640 μm . White lines represent the position of the etched crack. The die corner is shown in gray.	93
4.10	Hoop strain computed by XFEM for (a) the 160 μm crack and (b) the 640 μm crack, with an element size of 22 μm . Scale bar lengths of 100 μm . The white area in the lower left corner represents the die.	94

4.11	Strain component ϵ_θ as a function of the distance away from the crack tip along the diagonal direction, for the 160 μm crack, for the XFEM model with an element size of 30 μm (square markers), 22 μm (round markers), 16 μm (triangle markers), together with the confocal-DIC measurements (diamond markers). Error bars represent two-sided 90% confidence intervals.	95
4.12	Strain component ϵ_θ as a function of the distance away from the crack tip along the diagonal direction, for the 640 μm crack, for the XFEM model with an element size of 30 μm (square markers), 22 μm (round markers), 16 μm (triangle markers), together with the confocal-DIC measurements (diamond markers). Error bars represent two-sided 90% confidence intervals.	96
4.13	Strain component ϵ_θ as a function of the distance away from the crack tip, in the direction perpendicular to the diagonal direction, for (a) the 160 μm crack and (b) the 640 μm crack. The triangle markers represent the XFEM model results with an element size of 16 μm . The round markers represent the confocal-DIC measurements. Error bars represent two-sided 90% confidence intervals.	97
4.14	First principal strain ϵ_1 at (a) the 160 μm crack tip and (b) the 640 μm crack tip; on top layers by simulation (square markers), bottom layers by simulation (round markers), top layers by experiment (triangle markers) and bottom layers by experiment (diamond markers). Error bars represent two-sided 90% confidence intervals.	98
4.15	Hoop stress σ_θ at the crack tip with respect to the distance away from the crack tip for the model of the 160 μm crack, with an element size of 50 μm (round markers), 30 μm (triangle markers), 22 μm (diamond markers), and 16 μm (star markers).	99
4.16	Hoop stress σ_θ at the crack tip with respect to the distance away from the crack tip for the model of the 640 μm crack, with an element size of 50 μm (round markers), 30 μm (triangle markers), 22 μm (diamond markers), and 16 μm (star markers).	100
4.17	Diagram of the whole crack height.	101
4.18	Crack path starting from the chip corner: (a) initiating element, (b) growing on z direction, (c) propagating along the diagonal direction, (d) end stage.	102
5.1	Illustration of underfill failure modes: 1) delaminations from the sidewalls, 2) delaminations from the kerf areas, 3) crack propagation in the underfill toward the substrate, 4) crack propagation toward the external underfill fillet, 5) crack propagation in the chip circuitry.	110
5.2	Typical samples with (a) C-shape sealband and (b) 4 lines-shape sealband, obtained by scanning acoustic microscopy (C-SAM). Scale bar lengths of 5 mm.	114
5.3	Cross-sectional images perpendicular to the chip edges and along the first row of solder connections on (a) cell 1 without laser grooving at the chip edges and without laser outriggers and (b) cell 3 with laser grooving at the chip edges and with laser outriggers. Scale bar lengths of 20 μm	114

5.4	Location of cutting planes illustrated on the active side of a bare unpackaged die, for cross-sectioning.	115
5.5	One hidden layer ANN architecture.	117
5.6	Macro-model, (a) global quarter-symmetric view, (b) symmetry plane boundary condition at the planes of symmetry, (c) cross-section view in the xz-plane.	123
5.7	Submodel configuration, (a) global view, (b) cross-sectional view on the xz-plane at the chip corner area, (c) profile of the underfill fillet obtained by experiment (square markers) and the fitting curve by a power-law function (solid line).	124
5.8	Geometry of an interface element. [112]	125
5.9	Setup of (a) the diagonal initial crack with a cross-sectional view on the xy-plane and (b) the edge initial crack with a cross-sectional view on the xz-plane.	127
5.10	Z displacement of the chip-underfill interface from the chip center to the chip corner in the macro model.	128
5.11	Underfill hoop strain with respect to the distance from the chip corner in the xy-plane with a 45° angle from the x-axis in the submodel.	129
5.12	C-SAM images on cell 4 at (a) 250 cycles, (b) 500 cycles, (c) 1000 cycles and (d) 1000 cycles with a crack on the die. Scale bar lengths of 4 mm.	131
5.13	Typical convergence curve of the ANN model in 10,000 iterations.	132
5.14	Distribution of predicted initial moment of delamination on the test dataset, (a) cell 2, (b) cell 6, (c) cell 7, (d) cell 9, (e) cell 11, (f) cell 13. The black curves represent fitted Gaussian distributions.	133
5.15	Infrared microscopy images at each corner of the sample with die cracks in cell 6. Scale bar lengths of 100 μm.	134
5.16	Propagation of a delamination from one die corner, located at the top right, (a) 108 DTC cycles, (b) 216 DTC cycles, (c) 324 DTC cycles, (d) 432 DTC cycles after the initiation of delamination. The gray areas represent delaminated zones. Scale bar lengths of 1 mm.	135
5.17	Typical shapes of the chip-underfill delamination areas: (a) convex shape and (b) concave shape.	136
5.18	Delaminated areas at the chip-underfill interface as functions of thermal cycles obtained by the FEM model (lines) and the corresponding C-SAM results (round markers). Shaded areas represent ±1 standard deviation from the ANN prediction average in each cell. Error bars represent two-sided 90% confidence intervals.	137
5.19	Underfill cracks observed at the die corner by cross-sectioning in the samples of cell 4, (a) in front of the die corner, (b) at the die corner, (c) at the beginning of crack-stop line, (d) at the line of crack-stop. Scale bar lengths of 100 μm.	138
5.20	Diagram of the right edge cracks observed in the cross-sectioning test planes (AB and DC). The underfill fillet is not displayed in the diagram.	139

- 5.21 Cracked elements starting from the chip corner: (a) initial cracked elements, (b) cracks growing in the z direction, (c) cracks growing on both edges and diagonal direction, (d) final state of the three cracks. Wire-frames represent the outline of the underfill in the submodel. 140
- 5.22 YZ cross-sectional images of the edge crack at the final state of the simulation with x-direction distances of (a) 20 μm , (b) 50 μm and (c) 100 μm from the chip corners. Scale bar lengths of 20 μm 141
-

LIST OF TABLES

1.1	Temperature cycling test conditions. [13]	5
1.2	Input parameters for the perfect model for thermal cycling	9
1.3	Output parameters for the perfect model	10
1.4	Kolmogorov–Smirnov test parameter $c(\alpha)$ with respect to α . [16]	13
1.5	Variability of input parameters and possible solutions	16
1.6	Complexity of underfill reliability modeling at the chip corner	17
2.1	Summary of the analysis techniques for flip-chip failure analysis. [35, 36]	25
3.1	Material properties in models.	66
4.1	Dimensions of components	83
4.2	Material properties in models	88
4.3	Order of singularity at crack tips	98
5.1	Input variables encoded as binary values in the set $\{0,1\}$ for each test cell and the dataset partitioning of the cells	119
5.2	Material properties and dimensions in models	122
5.3	Summary of delamination area at chip-underfill interface	130
5.4	Leave-one-out cross validation results	130

LIST OF ACRONYMS

Acronyme	Définition
ANN	Artificial Neural Network
APDL	Ansys Parametric Design Language
ATC	Accelerated Temperature Cycle
BEOL	Back End of Line
C-SAM	C-Mode Scanning Acoustic Microscopy
C4	Controlled Collapse Chip Connection
CNT	Carbon Nanotube
CTE	Coefficient of Thermal Expansion
CZM	Cohesive Zone Model
DCB	Double Cantilever Beam
DIC	Digital Image Correlation
DVC	Digital Volume Correlation
DTC	Deep Thermal Cycling
FEM	Finite Element Method
IC	Integrated Circuit
IR	Infrared
I/O	Input and Output
JEDEC	Joint Electron Device Engineering Council
LSCM	Laser Scanning Confocal Microscopy
MCM	Multi-Chip Module
Micro-CT	X-ray Micro-Computed Tomography
PCB	Printed Circuit Board
SEM	Scanning Electron Microscope
SFEM	Stochastic Finite Element Method
UdeS	Université de Sherbrooke
VCCT	Virtual Crack Closure Technique
WLCSP	Wafer-Level Chip Scale Packaging
XFEM	Extended Finite Element Method

CHAPTER 1

INTRODUCTION

1.1 Research Background and Motivation

Integrated circuits (IC), also known as microelectronic chips, are devices connecting and integrating on a small scale different types of electronic components, for example transistors, diodes, resistors and capacitors. In 1947, the first transistor was invented and manufactured by William Shockley, John Bardeen and Walter Brattain at the Bell Laboratory. The transistor is a fundamental component of electronic devices and this invention marks the beginning of the development of microelectronics. In 1958, the first modern integrated circuit was invented by Jack Kilby. Prototype transistors were interconnected in the same block, which allowed the creation of memories, as well as of logical and arithmetic units. This concept became the basis of modern computer technology. Today, microelectronic devices are everywhere in our lives. The chip is a key component of these devices. As the silicon chip is very thin and fragile, packages protect the chip from mechanical and thermal loads to guarantee its long-term reliability [1].

Microelectronic packaging is a key technology to achieve the desired functionality of the electronic devices. It provides communication between the chip and external components, and also maintains the reliability of the device. Microelectronic packaging could be divided into three levels [2]:

- Level 1: Components. The chip is interconnected to a substrate or other components, which provide a means for connecting it to the external environment, via balls or pins.
- Level 2: Printed circuit board (PCB). The assemblies from level 1 are integrated on a PCB.
- Level 3: System. In this level, one or more PCBs are interconnected into an electronic system to provide complex functionalities.

In this thesis, we focus on level 1 packages.

Many types of packages have been developed according to different uses and needs. Wire-bonding and flip-chip are two popular packaging types. In the wire-bonding package, interconnections between the chip and other electrical components are realised by metal wires, leading to limited interconnection density [3]. The flip-chip packaging technology

was first developed by IBM in 1964 [4]. In this type of module, the chip is inverted and interconnected with the substrate by a matrix of C4 interconnections (Controlled Collapse Chip Connection). Figure 1.1 provides a diagram of a flip-chip package. Unlike wired-bonding techniques using metal wires to connect the chip to the substrate, flip-chip packages allow for more inputs and outputs (I/O) and reduce communication time because of short interconnects. A better heat dissipation performance is also achieved due to the direct connection on the backside of the chip. The exceptional advantages of flip-chip packaging have made it one of the most popular technologies in modern packaging, especially for multi-chip modules (MCM), high frequency communication devices, high performance computers and portable devices [5].

To protect the electrical components in the assembly, an underfill is used between the chip and the substrate. The underfill mechanically supports the chip and the C4 matrix. Modern underfills consist mostly of epoxy resins reinforced with silica particles (SiO_2). Polymer-based underfill materials can fill all areas between the chip and the substrate by capillarity¹, even if the geometry of the cavity is irregular. The main role of the silica particles is to improve the mechanical properties of the underfill, in particular to increase rigidity and reduce the thermal expansion of the underfill [7].

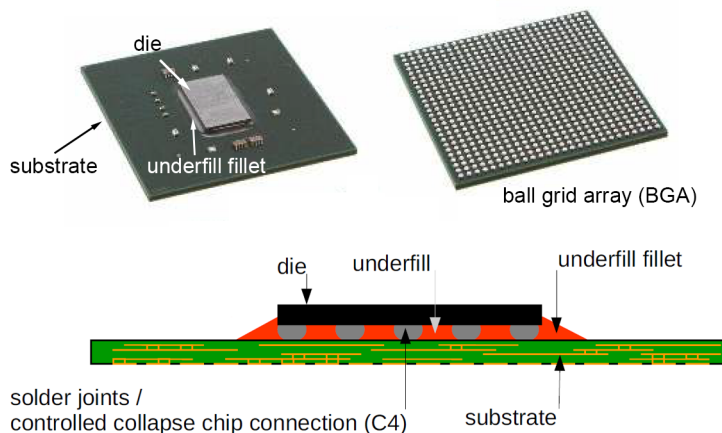


Figure 1.1 Typical flip-chip package. [8]

Today, several types of underfill processes have been developed, such as (a) conventional underfill with capillary flow, (b) no-flow underfill, (c) molded underfill, and (d) wafer-level underfill (as shown in Figure 1.2). For conventional underfills, the C4s are first interconnected and then the underfill is dispensed between the chip and the substrate for

1. As the distance between the chip and the substrate is small (around $50\text{ }\mu\text{m}$), the combination of surface tension of the underfill and the adhesive forces between the underfill and the surface of chip and substrate act to propel the underfill to fulfil the area between the chip and the substrate [6].

curing. The no-flow underfill changes this process by dispensing the liquid resin before interconnects are formed [9]. The limitation of the no-flow underfill is that it is not available for a resin with high filler density. Then, the molded underfill has an inlet and an outlet to control the injection of underfill, which is effective, but the injection pressure can cause cracks in C4 solders [10]. The wafer-level underfill process is very different from previous processes. It works directly on the wafer and cures the underfill between the wafer and the substrate. The wafers are then cut into small assembled chips. Low costs of production can be achieved with this process. It is possible to build a multi-layer underfill on a wafer, but this type of underfill also poses challenges. As the wafer is much larger than a single chip, the uniformity of the underfill and the quality of the interconnections are more difficult to control [11].

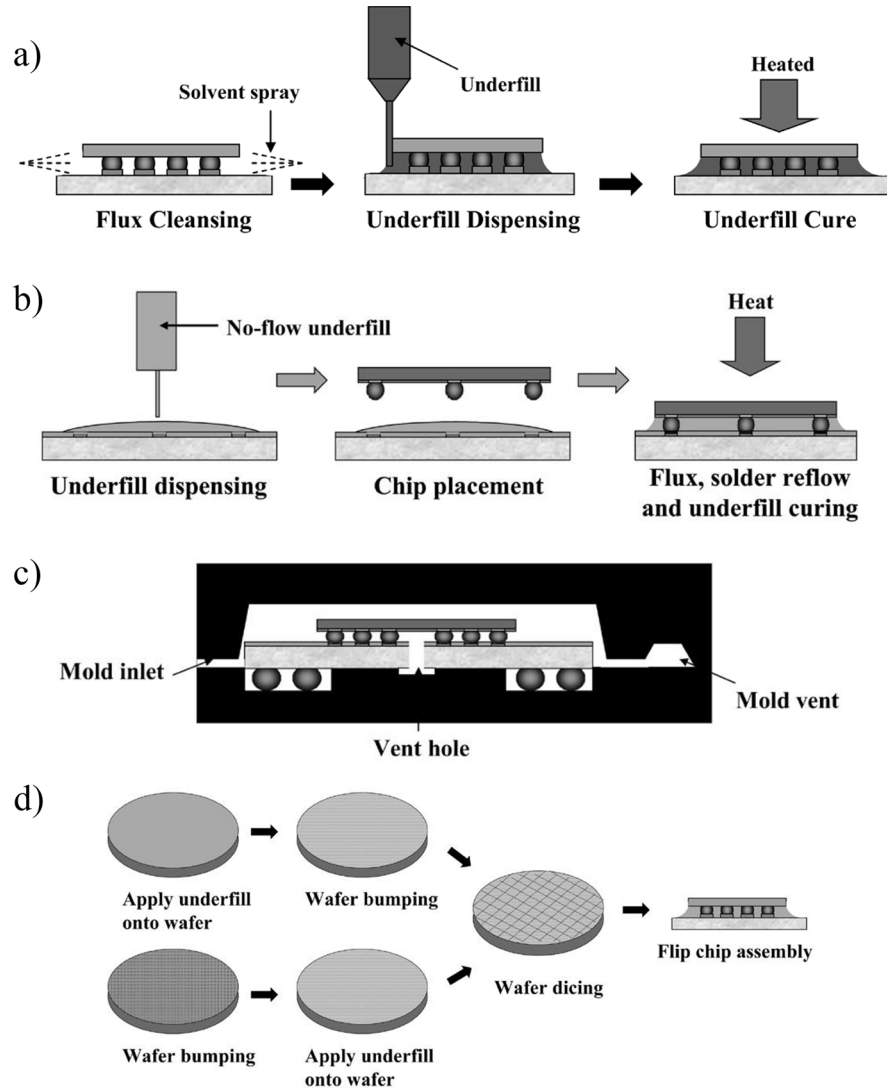


Figure 1.2 (a) Conventional, (b) no-flow, (c) molded and (d) wafer-level underfill. [5]

Regardless of the underfill process used for flip-chip packages, the underfill reliability is always one of the key properties of the assembly. During the operation of microelectronic devices, high and low temperature cycles can cause cyclic thermal expansion of each component. The mismatch of the coefficients of thermal expansion (CTE) between the different materials leads to shear stresses at the chip-underfill interface and the underfill-substrate interface [12]. The geometry of the chip corners leads to stress concentrations in the underfill when the environmental temperature is lower than the curing temperature (around 150 °C). These stress concentration areas accumulate damage faster than low stress regions, and this has a direct impact on the initiation of delamination and cracks in the underfill. Damage initiated in the underfill can lead to subsequent assembly failures, such as cracking of C4s and a laminated substrates. To test the package reliability performance under cyclic loading conditions, accelerated temperature cycling (ATC) and deep thermal cycling (DTC) are commonly used according to the JEDEC standard JESD22-A104 [13]. Figure 1.3 shows a typical temperature profile for the thermal cyclic test. Table 1.1 shows the temperature ranges for different test conditions. The soak time could range from 1 to 15 minutes and the typical cycling rate are in the range of 1 to 3 cycles per hour [13]. There is no specific requirement for the number of cycles. These standards provide test protocols for evaluating the package reliability. Further characterizations of the mechanical and electrical failures of the packages can be carried out after the cyclic test.

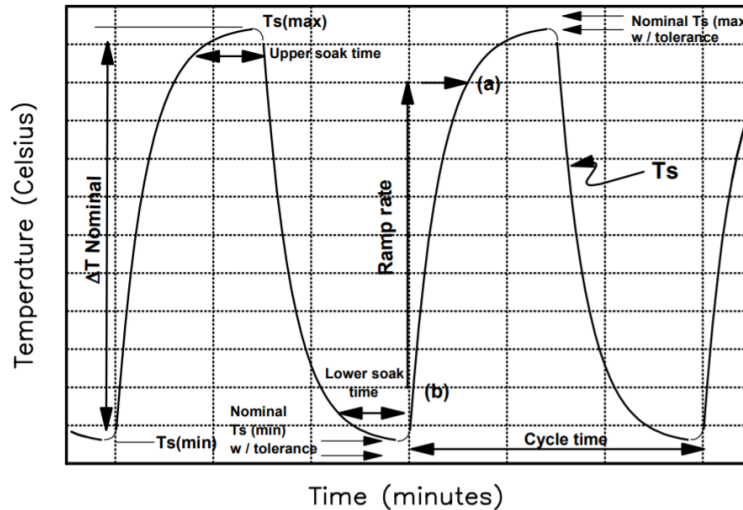


Figure 1.3 Typical temperature profile for thermal cycle test conditions. [13]

Although the underfill failures, such as the chip-underfill delamination and the underfill cracks, may be observed in the experimental characterizations, the microelectronics industry has not yet fully understood the mechanism of underfill failure. This makes it difficult to identify the package structural weaknesses and improve the packaging design.

Table 1.1 Temperature cycling test conditions. [13]

Test Condition	Nominal $T_s(\text{min})(\text{degC})$ with tolerances	Nominal $T_s(\text{max})(\text{degC})$ with tolerances
A	-55(+0,-10)	+85(+10,-0)
B	-55(+0,-10)	+125(+15,-0)
C	-65(+0,-10)	+150(+15,-0)
G	-40(+0,-10)	+125(+15,-0)
H	-55(+0,-10)	+150(+15,-0)
I	-40(+0,-10)	+115(+15,-0)
J	-0(+0,-10)	+100(+15,-0)
K	-0(+0,-10)	+125(+15,-0)
L	-55(+0,-10)	+110(+15,-0)
M	-40(+0,-10)	+150(+15,-0)

Knowing the distribution of stresses or strains around the chip corner area is essential to determine the initiation of underfill failures. The main motivation for this project is to understand how the underfill damage evolves during temperature cycling and to obtain an appropriate model to describe the chip-underfill delamination and underfill cracking. This project will allow the industry to have a more accurate and realistic model that can estimate the initial moment of delamination, the growth of delaminated areas and the crack profiles of the underfill in actual industrial flip-chip assemblies. This project is the result of a collaboration between the IBM Corporation and the Université de Sherbrooke.

1.2 Definition of the Research Project

Numerical studies of fracture problems, such as delamination and cracking, have been developed for many years. However, the application of the numerical tools to underfill still faces many challenges, since it is difficult to prove the accuracy of the numerical results with the existing experimental characterization methods. The characterizations are usually performed before or after the reliability test. Pre-test characterization aims at determining the input parameters to the model, such as material properties, geometries of components, etc. Post-test characterization aims to reveal the end state of the sample, such as the electrical failures, chip-underfill delamination areas and underfill crack paths. It is difficult to experimentally obtain a direct relationship between the underfill failure and the number of cycles during the reliability test, e.g. the distributions of stresses or strains in the underfill and their evolution with respect to the loading conditions by experimental characterizations. Although the finite element method can provide numerical estimates for stresses and strains in underfills, their accuracy is difficult to validate by existing experimental methods. FEM simulations require careful consideration of a plethora of important geometrical and material details.

In order to construct an appropriate numerical model to estimate the underfill reliability, the area of interest should be located near the chip corners. When calculating the stresses and strains at the bimaterial corners by FEM, the stress/strain will tend to infinity when the element size is reduced to near zero, which is the singularity effect. The singularity effect and the corner shape may greatly affect the accuracy of the stress/strain values at the corners. The question is therefore whether the stresses and strains calculated by FEM are in good agreement with their actual values. Some advanced characterization techniques, such as the X-ray tomography (micro-CT), Raman spectroscopy and confocal microscopy, have been developed in the literature to measure local deformations within a material. Their advantages and disadvantages will be discussed in section 2.3. Herein, the first question in this thesis is:

How to perform in-situ strain measurements in the underfill corner area, in order to obtain the strains at the underfill corner?

To answer this question, an *in-situ* strain measurement technique was developed by combining laser scanning confocal microscopy (LSCM) and digital image correlation (DIC) method, and was named the confocal-DIC technique. The confocal-DIC technique provides a strain distribution in a tri-dimensional view. In addition, the deformation around the crack from the underfill corner can be measured. The confocal-DIC-measured strains can provide a reference strain distribution for further simulation to validate the underfill cracking.

Experimental characterizations, especially when performed repeatably during the thermal cycling, can be costly and time-consuming. It would be desirable to develop a good numerical model that could simulate the underfill damage for the whole thermal cycling process. The underfill damage model includes two steps: damage initiation and propagation. For the underfill damage initiation, the stresses and strains in the underfill are the key metrics calculated from the FEM models. Several manufacturing variables could influence the underfill stresses and strains. For example, the type of dicing could cause different chip corner geometries and affect the maximum stress and strain at the chip corner when the temperature is below the curing temperature. With the help of the confocal-DIC-measured strains, the FEM model could be improved by reducing the differences between the calculated and measured strains. For the underfill damage propagation, the areas of chip-underfill delamination and the crack trajectories are the key metrics. The chip-underfill delamination is usually observed by C-SAM and the crack trajectories are usually observed by cross-sectioning. However, how the mechanical damage grows in the

underfill is unknown. Herein, the fracture models for the underfill delamination growth and crack paths could help estimate the evolution of damage without repeated characterization in the thermal cycling. Several 2D and 3D fracture models have been studied in the literature and their pros and cons will be discussed in section 2.4.

When building a numerical model to predict the underfill damage initiation and propagation, many input variables need to be used carefully, such as the geometry of the package components and the material properties. However, addressing all of these geometrical and material details in a single FEM model can be challenging and time-consuming, as the exact data on the chip corner radius, underfill filler distribution, chip-underfill interface adhesion strength, underfill fracture toughness, etc., can only be obtained by the experimental characterization of actual parts. Thus, an efficient model should directly link the input variables to the underfill damage initiation. After obtaining the underfill damage initiation, the model should further estimate the underfill delamination areas and crack paths under the cyclic thermal loading. This leads to the second research question in the thesis:

How to construct a numerical model that relates the input manufacturing variables to the initial moment of underfill delamination, the delaminated areas and the underfill crack paths?

1.3 Roadmap of Underfill Reliability Estimation

According to the research questions presented in section 1.2, we know that practitioners do not have an appropriate model to accurately estimate the underfill reliability in thermal cycling. However, it is expensive and time-consuming to perform experimental reliability tests for different package designs, processes and materials. It would be valuable to have an accurate model that could numerically estimate the time to electrical failure. Practitioners could then select the suitable configurations, processes and materials for a package without having to wait for the results of the experimental reliability tests. In order to achieve the estimation of underfill reliability in thermal cycling, a roadmap to obtain a numerical model (named 'perfect model') can be first defined. Figure 1.4 shows this roadmap, which includes six general steps:

1. Goals definition. This step is to define the demands and goals of underfill reliability estimation, in particular the demands from practitioners. Appropriate metrics for each goal should be defined for model evaluation.

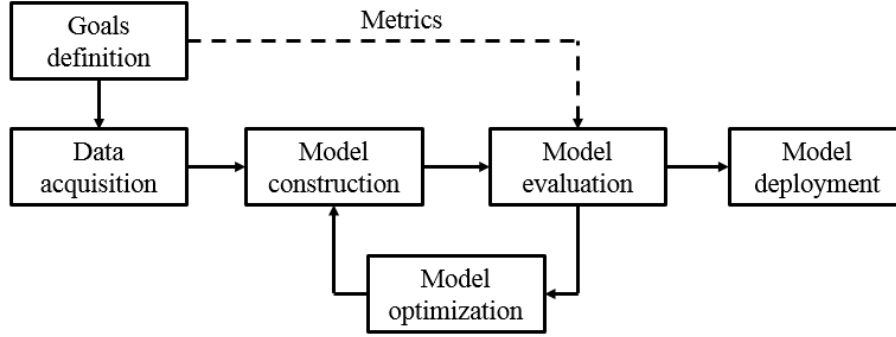


Figure 1.4 Roadmap of underfill reliability estimation.

2. Data acquisition. This step aims to acquire all necessary raw data for building the model for estimating the underfill reliability.
3. Model construction. This step is to build a numerical model for underfill reliability estimation. This model is an ideal solution that could handle all underfill failure modes and give accurate time to failure predictions.
4. Model evaluation. This step is to evaluate the accuracy of model outputs based on the predefined metrics and confirm the model applicability.
5. Model optimization. This step is to improve the model performance by reducing the difference between the model-obtained and experimentally obtained results. The iteration of model optimization aims to obtain the perfect model for underfill reliability estimation.
6. Model deployment. After the model validation, practitioners could apply this model to estimate the underfill reliability based on their input data.

1.3.1 Perfect Model for Underfill Reliability Estimation

This roadmap provides a general development path for underfill reliability estimation and the core aspect of the roadmap is to develop a perfect model. With this perfect model, practitioners could evaluate the effect of flip-chip configurations, materials and processes on the underfill reliability by calculating the distribution of times to the electrical failure of flip-chip packages. This section will introduce the inputs and outputs of this model, the elements of the model, the methods for model evaluation and the challenges in building the model.

Inputs and Outputs for the Perfect Model

The perfect model for underfill damage estimation should have multiple inputs. To be useful for practitioners, the input variables should be easy to obtain, such as the design

and process of the flip-chip packages, and the loading conditions in the reliability test. Furthermore, the design and process of the flip-chip packages affect the configuration of the package and the dimensions of each part in the flip-chip packages. So, the geometry-related inputs must include the thickness, length and width of each part, lid shape, underfill fillet dimensions, and other advanced features (see Table 1.2). The material properties include the elastic modulus, Poisson's ratio, CTE, fracture toughness, interfacial adhesion, and other advanced features. Table 1.2 shows the detailed input parameters for the perfect model. Most input parameters are not single-valued and they are described by a distribution in the population of their values. Section 2.1.3 will review the experimental studies on the effect of underfill elastic modulus, CTE, filler type, filler volume ratio and voids on the underfill reliability, but the numerical modeling of the effect of the advanced features on the underfill reliability has not been thoroughly studied. These unstudied effects still require extensive researches to achieve the perfect model.

Table 1.3 summarizes the output parameters for the perfect model. Practitioners would obtain the time to the underfill failure initiation, delamination areas and crack paths, and time to the electrical failure of flip-chip packages as the outputs. The distribution of times to the underfill failure initiation could be used to evaluate the state of underfill (if the damage occurs or not). The distribution of times to the electrical failure could be used to estimate the lifetime of flip-chip assemblies. Thus, with this perfect model, practitioners could evaluate the effect of each input variables on the time to underfill damage and lifetime of the flip-chip assembly.

Table 1.2 Input parameters for the perfect model for thermal cycling

Category	Parameters
Basic geometries	Thickness, length and width of each part, lid shape, underfill fillet dimensions
Advanced geometrical features	Chip dicing artefacts, chip alignment, underfill voids, C4 and BEOL layout, substrate warpage, laminate copper traces and vias
Basic material properties	Elastic modulus, Poisson's ratio, CTE, fracture toughness interfacial adhesion, glass transition temperature,
Advanced material features	Filler segregation, filler volume ratio, filler type, moisture, material non-uniformity, viscoplasticity, flux residues
Loading conditions	Max. and Min. temperature, ramp rate, soak time, frequency of cycles, number of cycles.

Elements of the Perfect Model

As different underfill failure modes need to be estimated, this perfect model will be very complex. The perfect model could be divided into multiple blocks. Each block aims at one specific function, including 1) basic preprocessing, 2) advanced preprocessing, 3) underfill

Table 1.3 Output parameters for the perfect model

Category	Parameters	Experimental validation
Failure metrics	Distribution of times to initial delamination	None
	Distribution of delamination areas	C-SAM
	Distribution of times to initial cracking	None
	Distribution of cracks plane directions, crack lengths and heights	Cross-sectioning
	Distribution of times to electrical failure	Electrical tests on C4s and circuits

strain calculation, 4) initiation of underfill delamination, 5) growth of underfill delamination, 6) initiation of underfill cracking, 7) growth of underfill cracking, and 8) crack growth in metallic components. The diagram of the perfect model and the functionality of each block is introduced in Figure 1.5:

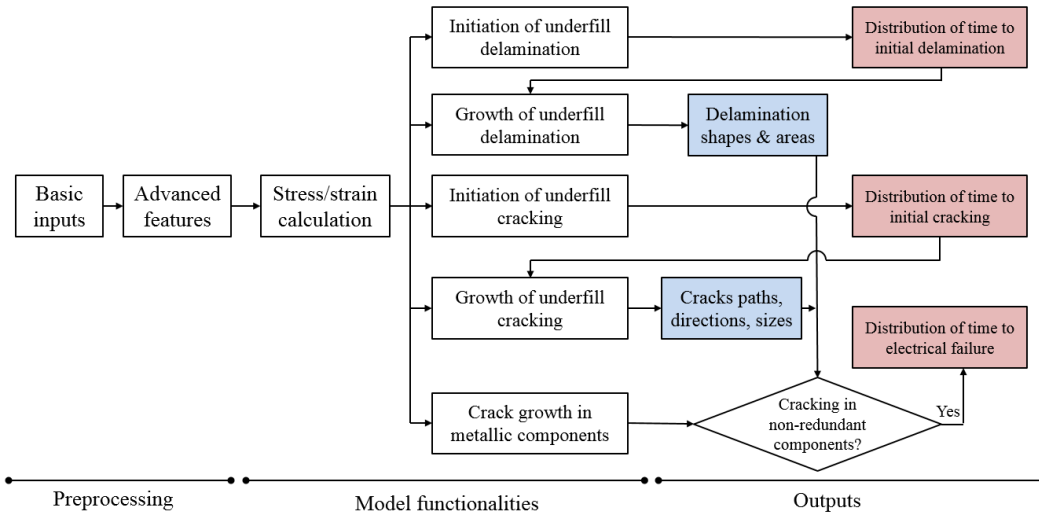


Figure 1.5 Diagram of the perfect model.

1. Basic preprocessing. Entry of the basic geometries and material properties of each part in the flip-chip package, loading conditions and boundary conditions presented in Table 1.2. The basic geometries and material properties are in the form of distributions. Advanced geometrical and material features could be entered in the next block.
2. Advanced preprocessing. This block handles the advanced geometrical and material features in the input parameters. These parameters have an impact on the local geometry and local material properties of the model. The variability of all input parameters will be discussed in section 1.3.3.

3. Underfill strain calculation. This block focuses on calculating the underfill strain distribution as a function of spatial positions and number of cycles, which is essential for the underfill damage modeling. The underfill strain is a random variable that depends on the input parameters. The calculated strain distribution should be compared with the experimentally measured strains by a strain measurement technique, which is one of the challenges in building the perfect model (discussed in 1.3.3). The strain evaluation method will be described later. The advances in the underfill stress and strain calculation by FEM will be discussed in section 2.4.1.
 4. Initiation of underfill delamination. This block focuses on estimating the numbers of cycles to delamination of the underfill. Due to the variability of input parameters, the perfect model will obtain a distribution of number of cycles to delamination for each corner. The evaluation of this distribution will be introduced in section 1.3.1.
 5. Growth of underfill delamination. This block could be performed by FEM on the chip-underfill interface region. The C-SAM observed delamination areas could be used to validate the model-calculated delamination areas. The delamination shapes, distributions of dimensions in each direction and areas with respect to the number of cycles could be obtained experimentally and numerically for validation. The advances in the underfill delamination modeling will be discussed in section 2.4.3 and 2.4.4.
 6. Initiation of underfill cracking. This block focuses on estimating the number of cycles to cracking of the underfill. Due to the variability of input parameters, the perfect model will obtain a distribution of number of cycles to cracking for each corner. The underfill cracking characterization relies on cross-sectioning. Thus, the initial cracking moment could be determined in an interval before the observation of cracks by cross-sectioning near the chip corner. The evaluation of this distribution will be introduced in section 1.3.1.
 7. Growth of underfill cracking. This block could be performed by crack modeling based on the stress distribution in underfill and obtain the crack trajectories with respect to the number of cycles. In addition to the variability of measurable input parameters, some unobserved parameters, such as underfill fillers and voids locations, could also affect the crack directions and sizes. This is one of the challenges in building the perfect model and will be discussed in section 1.3.3. Cross-sectioning could be used to observe the crack position and size experimentally, and validate the model-obtained crack paths by the normal vectors of crack planes and the crack lengths/heights in each cross-sectional images. For a population of samples, the normal vector directions of crack planes, crack lengths and heights are also random
-

variables, which should be described by distributions. The advances in the underfill crack modeling will be discussed in section 2.4.2 and 2.4.4.

8. Crack growth in metallic components. This block is an extension of underfill reliability modeling on delamination and cracks, which estimates the damage growth in the solder joints, BEOL and substrates that could lead to electrical failure. As the solder joints also suffer from fatigue before the cracks reach them from the underfill, a key aspect is to determine how the underfill damage affects the number of cycles that the solder joints could resist before cracking. In addition, not every cracked metal wire or solder joint will cause an electrical failure. Some components have one or more homologous parts with the same function, such as the ground wires in the circuits of BEOL and substrates. If one of these parts is cracked and the package still works properly, it is a redundant part. The time to electrical failure can be determined by the perfect model when a non-redundant part is cracked. Then, the proportion of electrical failures caused by each failure mechanism (cracked solder joints, BEOL or substrate) could be obtained by the perfect model. The time to electrical failure caused by each failure mechanism is also a random variable and should be described by a distribution.

In the perfect model, the elements 4 to 8 are not independent from each other, as the delamination and cracking could exist at the same time. Thus, the perfect model should be able to implement the elements from 4 to 8 in parallel.

Evaluation of the Perfect Model

From the outputs of the perfect model, practitioners could be mostly interested in the distribution of times to initial delamination, initial cracking and electrical failure. Other metrics, such as the delamination areas and crack paths, are of secondary importance for practitioners. As the perfect model includes a large amount of input variables from the geometry and material properties, it is costly and time-consuming to perform experimental reliability tests for every combination of input variables and obtain their time to failure data. Moreover, the time to delamination and cracks is determined by underfill local stress and strain, and the time to electrical failure is determined by the cracks in non-redundant electrical components. It would be wise to first validate the underfill stress or strain distributions and then validate the time to failure data.

The stresses are difficult to obtain experimentally, but some optical techniques could be used to measure the strains inside a material (discussed in section 2.3). After setting all input variables, the perfect model could then provide the means, variances and confidence

intervals of calculated strains as a function of spatial positions. For a population of test samples, the experimentally measured strains are also described by distributions for each spatial position at the selected number of cycles. If the model-obtained strain distribution matches the experimentally obtained strain distribution, we could confirm the accuracy of strain calculation. For the experimentally obtained strain sample set \mathcal{E}_e and model-obtained strain sample set \mathcal{E}_m at a selected position and for a given number of cycles, the two-sample Kolmogorov–Smirnov (KS) test could be used to determine if these two sets were sampled from the same distribution [14]. The KS test is a non-parametric test and the KS statistic is:

$$D_{n,m} = \sup |F_{1,n} - F_{2,m}|, \quad (1.1)$$

where $F_{1,n}$ and $F_{2,m}$ are the cumulative distribution functions (c.d.f.) of the first and second sets of samples, respectively, \sup is the supremum (least upper bound) function, m and n are the sizes of first and second sets of samples. If $D_{n,m} > c(\alpha)\sqrt{(n+m)/(n \cdot m)}$, the two sets of samples are not from the same distribution [15]. The value of $c(\alpha)$ is given in Table 1.4 for the common test significance levels α .

Table 1.4 Kolmogorov–Smirnov test parameter $c(\alpha)$ with respect to α . [16]

α	0.10	0.05	0.025	0.01
$c(\alpha)$	1.224	1.358	1.480	1.628

Then, there are three metrics of times to failure in Table 1.3: 1) distribution of times to initial delamination, 2) distribution of times to initial cracking and 3) distribution of times to electrical failure. They could be evaluated as follows:

1. Distribution of times to initial delamination. A periodical C-SAM inspection could be performed for each test sample to verify if a delamination had occurred at a specific interval, regardless of the location of the delamination. For a population of test samples, the number of delaminated samples with respect to the sequence of intervals could be obtained and composed as a discrete distribution of times to initial delamination $\mathcal{T}_e^{\text{delam}}$. The model-obtained distribution of times to initial delamination $\mathcal{T}_m^{\text{delam}}$ could then be compared with $\mathcal{T}_e^{\text{delam}}$ by the KS test.
2. Distribution of times to initial cracking. The evaluation method of this distribution is the same as that on the time to initial delamination.
3. Distribution of times to electrical failures. The electrical failure could be caused by the cracks in different metallic components. The evaluation of the distribution of times to electrical failure could be performed in two steps when the reliability test of thermal cycling is finished (e.g. 1000 cycles):

- For a population of test samples (N), we should first identify the failure mechanism of each sample by cross-sectioning (cracks in solder joints, BEOL or substrate), and count the number of failed sample n_{sj} , n_{BEOL} and n_{subs} . The occurrence probability of each failure mechanism for the population of samples could then be obtained by n_{sj}/N , n_{BEOL}/N and n_{subs}/N . These experimentally obtained probabilities should first be compared with the model-obtained probabilities of the corresponding failure mechanisms.
- As the electrical readout is only tested periodically, a failure interval could be obtained for each failed sample as well. Thus, for each failure mechanism, we could obtain the corresponding discrete distribution of times to electrical failure $\mathcal{T}_{\text{e,sj}}^{\text{elec}}$, $\mathcal{T}_{\text{e,BEOL}}^{\text{elec}}$ and $\mathcal{T}_{\text{e,subs}}^{\text{elec}}$. For each failure mechanism, the experimentally obtained and model-obtained distribution of times to electrical failure could then be compared by the KS test.

1.3.2 Application of the Perfect Model

From the outputs of the perfect model, practitioners could obtain the distribution of numbers of cycles to electrical failure of the flip-chip packages under thermal cycling. In addition to the mean and variance of the distribution, practitioners could also obtain the survival-function graph, which shows the percentage of samples remaining functional over time, as shown in Figure 1.6. In the survival-functional graph, the $N50$ is defined as the number of cycles where 50% of the samples have failed [17]. When practitioners need to qualify a new package design, they could compare the model-obtain $N50$ of this package and a target number of cycles. If the model-calculated $N50$ is greater than the target number of cycles, the package design can be approved for thermal cycling reliability verification.

1.3.3 Challenges in Building the Perfect Model

The perfect model presented in section 1.3.1 is an ideal solution for the estimation of underfill reliability in thermal cycling. Several challenges exist in building this perfect model. This section will describe the challenges that we would be faced during the model construction.

Variability of Input Parameters

Table 1.5 summarizes several variability situations for the input parameters. The first variability is about the values of certain parameters, including the dimensions of each part, elastic modulus, Poisson's ratio, CTE, fracture toughness, interfacial adhesion strength and underfill T_g . They could be directly measured, but take random values due to the

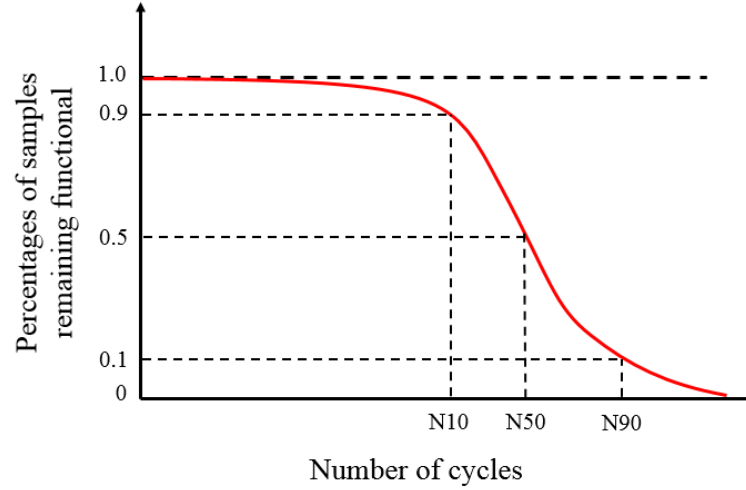


Figure 1.6 Typical survival-functional graph. The N_{10} , N_{50} , and N_{90} points are shown, representing the times when 10%, 50%, and 90% of the samples have failed.

tolerances of fabrication, material purity and quality. We should first determine the distribution of these parameter values, and then perform a random sampling for each parameter. In addition, these material properties may also vary during the aging process, which needs to be considered into the variability of material properties.

The second variability is about the shape of components. For the advanced geometrical features, the chip dicing artefacts could cause different chip corner shapes, which requires to build a detailed geometry for the chip corner. The chip misalignment and substrate warpage could cause different parallelisms between the chip and substrate and the distortion of solder joints [18, 19]. The geometry of solder joints and underfill near the solder joints should be determined carefully, while the geometry of solder joints could be characterized by the X-ray tomography. The BEOL, laminate copper traces and vias require submodeling, as their dimensions are much smaller than that of the die, underfill and solder joints.

The fabrication characteristics and defaults could lead to some unobserved features, which is the third variability of modeling. The filler segregation could cause a resin-rich zone near the chip [7] and the determination of local filler density is critical for the local underfill material properties. The current solution is to build a multi-layered underfill model [20, 21]. In addition, the underfill non-uniformity, voids and flux residues may be in random locations. It is difficult to define the exact position and size of these randomly located defaults in the model. Stochastic modeling might be useful for this situation and will be

discussed in section 2.4.6. Overall, a careful determination of the input parameters is the first challenge in building the perfect model.

Table 1.5 Variability of input parameters and possible solutions

Type	Affected parameters	Reasons	Solutions
Values	Dimensions of each part, elastic modulus, Poisson's ratio, CTE, fracture toughness, interfacial adhesion strength underfill T_g	Fabrication tolerance, material purity, material quality	Obtain the value distribution and random sampling
Shapes	Chip corner, solder joints, BEOL, laminate copper traces and vias, chip substrate parallelism	Dicing artefacts, chip misalignment, substrate warpage	Shape adjustment, submodeling
Unobserved features	Filler segregation, underfill non-uniformity, underfill voids, flux residues	Fabrication defaults, material quality	Multi-layered underfill model, stochastic model

Validation of Model-obtained Strains

The stresses and strains are used throughout the perfect model and are the key parameters for delamination and crack modeling. A verification of model-obtained stresses and strains is required. Stresses could not be directly measured by experiments, but strains can be derived from the gradient of local displacement of material when the local displacement can be measured. However, the chip corners, chip-underfill interfaces and underfill cracks are not located at the exterior surface of the package, which makes the underfill strain measurement difficult in practice.

In order to achieve the underfill strain measurements, we could first try to define different levels of characteristics of the chip corner region and start to validate the chip corner strain from the simplest case. Table 1.6 summarizes the levels of characteristics of chip and underfill for the underfill reliability modeling, while the level 1 is the simplest case and the level 5 is the most complex case (reality). The different situations of delamination and cracking are also summarized in Table 1.6. As we focus on the strains in underfill, appropriate experimental techniques have to be developed based on the different levels of underfill characteristics. Sections 2.3.2 to 2.3.4 will review recent advances on the strain measurement techniques and some of them are useful for validating the chip corner model at certain levels of complexity. The contributions of this thesis will also be positioned based on Table 1.6.

Complicated Failure Mechanisms

The underfill delamination and cracking are not independent from each other. For example, when the underfill delamination occurs, the stress in the underfill is different from the non-delaminated state, which leads to a different moment of initiation and growth rate of underfill cracks. For the metallic components, the mechanical failure may be induced by

Table 1.6 Complexity of underfill reliability modeling at the chip corner

Level	Chip characteristic
1	isotropic, pyramid corner
2	anisotropic (depends on Si crystal planes), pyramid corner
3	anisotropic, corner with user-defined radius
4	anisotropic, arbitrary shaped corner
5	anisotropic, arbitrary shaped corner, BEOL
Level	Underfill material characteristic
1	homogeneous, no fillers
2	homogeneous, low filler density (<1 wt%)
3	homogeneous, regular filler density (~ 60 wt%)
4	regular filler density (~ 60 wt%), filler segregations
5	regular filler density (~ 60 wt%), filler segregations, underfill voids, flux residues
Level	Underfill crack situation
1	no cracks
2	one crack
3	multiple cracks
4	cracks penetrating solder joints, BEOL or circuits
Level	Chip-underfill interface situation
1	no delamination
2	delamination on flat interfaces
3	delamination on sidewall interfaces
4	delamination on flat and sidewall interfaces

1) the metal fatigue during the thermal cycling, 2) the cracks propagating from underfill, and the combination of 1) and 2). The perfect model must be able to estimate the damage of metallic components accumulated from different resources and estimated the number of cycles to electrical failure.

At the micron scale, the location of voids and fillers has a significant impact on the underfill crack growth trajectory when the underfill material characteristic is at level 3 or higher. If the crack grows into a void, the void will slow down the crack propagation, because it eliminates the high stress concentration at the crack tip. If a crack reaches a SiO_2 filler, the crack direction must change due to the obstruction of the filler, which may affect the following crack trajectory. Sections 2.4.5 and 2.4.6 will review the advances in crack modeling for particle reinforced composites and the stochastic modeling method for fracture problems. In addition, cleavage fracture could occur in brittle crystalline materials, such as the silicon dies [22], which is the result of splitting along definite crystallographic structural planes [23]. This should also be considered in crack modeling.

1.4 Objectives

1.4.1 General Objective

The roadmap from section 1.3 provides a development path for building a perfect underfill damage model and this thesis aims to complete parts of the roadmap leading to the perfect model. Our general objective is to contribute a numerical model that could estimate the distribution of initial moment of delamination, deterministic growth of delamination areas, and point estimates of crack directions from the basic inputs. The basic inputs include 1) deterministic dimensions, elastic moduli, CTEs and Poisson's ratios of the die, underfill, substrate, lid and TIM, 2) fracture toughness and T_g of the underfill, and 3) thermal cycling conditions from 150 to -55°C, with no consideration of the effect of ramp rate, soak time and frequency of cycling. Section 1.4.2 will introduce three sub-objectives from the general objective. Also, the contribution of each sub-objective will be identified and positioned in the roadmap.

1.4.2 Sub-objectives

The first sub-objective of this project is to experimentally measure the underfill strain distribution around the chip corner and compare the measured strains with FEM results to validate FEM modeling. Good strain measurements near the underfill corner have not previously been reported in the literature, as will be reviewed in Chapter 2.3. Our contribution to strain measurements could help improve the model accuracy by reducing the errors on calculated strains. This sub-objective is addressed in the first part of the thesis and it can be divided into the following tasks:

1. Develop a 3D *in-situ* strain measurement technique based on laser scanning confocal microscopy and digital image correlation method, named the confocal-DIC technique. This technique is able to measure the deformation of the underfill near the chip corner without mechanically destructing the test component.
2. Build a flip-chip FEM model and calculate the underfill strain distribution around the chip corner. Compare the calculated strain distribution with the confocal-DIC results and evaluate their differences.

Compared with the challenges of the validation of model-obtained strains in section 1.3.3 and Table 1.6, this contribution fits the level 1 of the chip characteristic (isotropic, pyramid corner), level 2 of the underfill characteristic (homogeneous, low filler density), level 1 of the underfill crack situation (no cracks) and level 1 of the chip-underfill interface situation (no delamination). In addition, the first sub-objective addresses the spatial distribution of the underfill strains, but the strains as a function of number of cycles are not studied.

Based on the confocal-DIC technique developed in the first sub-objective, it is possible to validate an underfill crack model by similar strain distributions near the crack tip between experiments and simulations. The second sub-objective is therefore to develop a precise underfill crack model by XFEM. Our main original with that could, for the first time, be directly compared against experimental strain measurements in the underfill. The contribution of this sub-objective is the application of XFEM in the underfill crack modeling, as demonstrated by a validation using the confocal-DIC-measured strains near the crack tip. This sub-objective can be divided into the following tasks:

1. Fabricate a test component similar to a flip-chip package with diagonal cracks in the underfill. Apply the confocal-DIC technique to measure the deformation around the cracks.
2. Construct an underfill crack model with XFEM. Compare the strain values and their distribution between the experimental and numerical results.
3. Optimize the numerical model from the element size, the chip corner geometry and the underfill filler distribution with the reference of experimental results.

Compared with the challenges of the validation of model-obtained strains in section 1.3.3 and Table 1.6, the second sub-objective fits the level 2 of the underfill crack situation (one crack), while the chip characteristic, underfill material characteristic and chip-underfill interface situation are not changed. The relationship between the underfill strain and number of cycles is still not studied.

After experimentally validating the FEM for calculating the strains in the underfill and the XFEM for calculating the crack tip strains, the FEM and XFEM could be used for calculating the underfill stresses and strains in various flip-chip packages. The third sub-objective is to develop a modeling approach that can estimate the initial moment of delamination, the growth of chip-underfill delamination areas and the underfill cracking profiles in various flip-chip packages. To achieve this objective, five tasks are presented as follows:

1. Perform DTC tests on the samples of flip-chip packages. Inspect their chip-underfill delamination areas by C-SAM and underfill crack profiles by cross-sectioning.
 2. Train an artificial neural network (ANN) model to predict the initial moment of delamination for test cells.
 3. Construct a FEM model to estimate the interfacial delamination areas growth with respect to the number of DTC cycles.
 4. Use the XFEM to model the underfill crack profiles starting from the chip corner.
-

5. Evaluate the performance of the numerical model, by comparing the predicted initial moment of delamination with C-SAM inspection intervals, the chip-underfill delamination areas calculated by FEM with the areas measured by C-SAM, and the crack plane directions calculated by XFEM with the results of cross-sectioning images.

Our main contribution with this sub-objective is to estimate the number of cycles to delamination by a machine learning method, and to use FEM and XFEM that have been experimentally validated to estimate delamination areas and crack paths. Both the use of machine learning and of FEM that have been validated by direct experimental measurements of strain are original contributions to the flip chip reliability literature.

Compared with the challenges of variability of input parameters in section 1.3.3, the third sub-objective contributes to the effect of chip corner shapes on the initial moment of delamination. Then, based on Table 1.6, the chip and underfill material characteristics are not changed. The delamination growth model meets the level 2 of the chip-underfill interface situation (delamination on flat interfaces). The cracking model meets the level 3 of the underfill crack situation (multiple cracks), but the crack growth with respect to the number of cycles are not studied. The delamination growth and crack trajectory modeling do not consider the variability of input parameters, and the dependency of these two models is not studied either. The progression of the three sub-objectives is visualized in Figure 1.7.

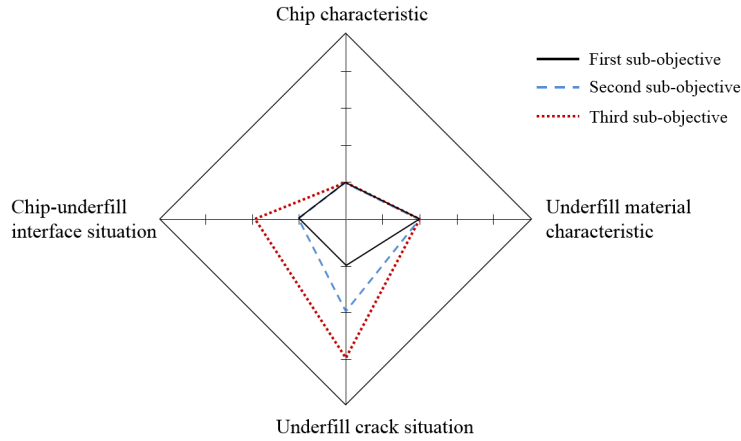


Figure 1.7 Progression of the three sub-objectives based on the levels of model characteristics in Table 1.6.

1.5 Outline of the Thesis

This thesis contains 6 chapters, with chapters 3 to 5 presented in the form of articles. Chapter 2 reviews the research literature in the field related to the topic, including failures of flip-chip packages, experimental approaches on evaluating fracture properties and local

deformation, and numerical methods for cracking and delamination modeling. Chapter 3 corresponds to the first sub-objective and is a first article which presents the confocal-DIC technique with validation tests. The deformation around a chip corner and a crack front in a three-point flexure sample were measured by the confocal-DIC technique. A FEM model of a flip-chip was developed to calculate the underfill strain distribution around the corners. The evaluation of the corner strain distribution was performed between the experimental and numerical results.

Then, revealing the strain distribution around the crack in the underfill is the main contribution of the article in Chapter 4, corresponding to the second sub-objective. This chapter presents the deformation around the corner crack inside the underfill, obtained by the confocal-DIC method, with a test component similar to a real flip-chip package. XFEM was used to model the underfill cracks and the strains around the crack tip were slightly lower than that of the confocal-DIC results. To optimize the model, the effects of element size, shape of chip corner and filler density were also analysed to reduce the difference between the numerical and experimental measured strains at the chip corner. With such experimental insight as an essential element, our model could become more realistic and accurate in practice than classical finite element models.

Chapter 5 corresponds to the third sub-objective and presents DTC reliability tests up to 1000 cycles on actual flip-chip assemblies and the modeling of the initial delamination, the delamination areas growth and the underfill crack trajectories. Five manufacturing variables were included which were the kerf width, dicing type, laser outrigger presence, sealband material and sealband shape. The results of C-SAM and cross-sectioning showed the chip-underfill delamination areas and underfill crack paths. The modeling approaches of ANN, FEM and XFEM were used to estimate the initial moment of delamination, the growth of delaminated areas and the underfill cracking paths for actual industrial flip-chip assemblies. The modeling approaches presented in this chapter could eventually be used to predict the initiation of delamination, growth of delamination and underfill crack trajectories in actual flip-chip packages, when multiple input manufacturing variables need to be considered.

The final chapter gives the general conclusions of this project and answers the research questions. The conclusions summarize the results and contributions in the development of the confocal-DIC technique (Chapter 3), the modeling of underfill cracks (Chapter 4) and the modeling approaches for chip-underfill delamination and underfill cracking (Chapter 5). Perspectives for future work are proposed as well.

CHAPTER 2

THE STATE OF THE ART

In this chapter, the literature is reviewed for previous work in the area of underfill reliability, including the following four parts: section 2.1 introduces the underfill process, flip-chip package materials, failure modes and their influence on the reliability of the assembly; section 2.2 presents the analytical solutions for the stress distribution at chip corners and underfill crack regions; section 2.3 summarizes the current experimental methods on the evaluation of materials properties for the underfill and discusses the possibilities of directly measuring the underfill strain; section 2.4 shows the advances in numerical modeling on fracture mechanics and the application of numerical simulations on underfill failure.

2.1 Flip-chip Packages and Underfill Failure

2.1.1 Underfill Process in Flip-Chip Packages

The underfill process is one of the steps in flip-chip packaging. Figure 2.1 shows the conventional flip-chip process. This process involves the following steps: 1) dip or dispense the flux¹; 2) align the chip solders to the pad on the substrate; 3) reflow the solder bumps to build the interconnections; 4) clean the flux; 5) dispense the underfill material between the die and the substrate; 6) cure the underfill to form a solid composite. The steps 5 and 6 are the capillary underfill process. In the step 5, the capillary flow allows the underfill to fill the space between the die, substrate and interconnections.

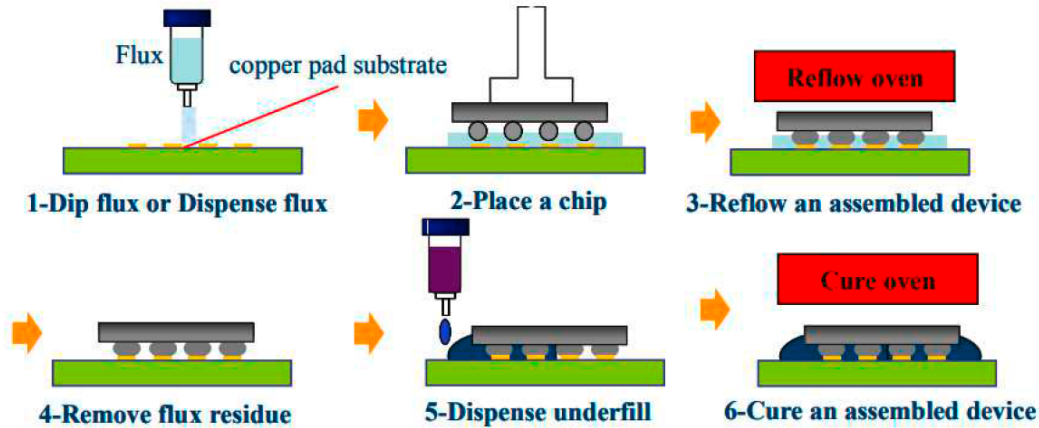


Figure 2.1 Conventional flip-chip process. [24]

1. chemical substance used to limit the formation of the oxide on the surface

2.1.2 Material System of Flip-Chip Packages

In flip-chip packages, most underfill materials are polymers reinforced with rigid particle fillers (see Figure 2.2), as they can flow and fill irregular cavities in the liquid state, then be cured in a solid form with good thermal, chemical and mechanical properties [25]. Epoxy is one of the most commonly used polymers as the resin matrix of underfill. Epoxy is a type of thermosetting resin with epoxide functional groups, which has a hardening temperature around 150-200°C. The fillers are spherical SiO_2 particles of micron scale. The main role of fillers is to improve the elastic modulus and reduce the CTE of the underfill [7].

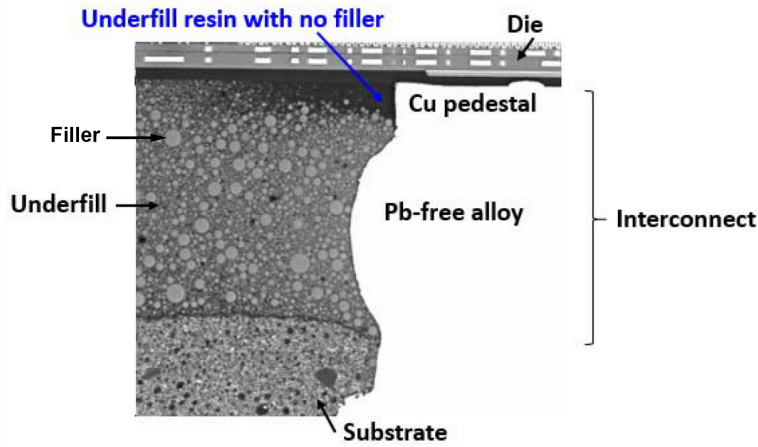


Figure 2.2 Cross-section of underfill area. [7]

Apart from the underfill, the chip and substrate are the other two components in the flip-chip package. The chip is commonly made of silicon, which has a high elastic modulus (around 120 GPa) and low CTE (around 2.5 ppm/°C). The quality of chip dicing can be essential to the initiation of underfill delamination and cracking, since the local strain in the underfill is sensitive to the chip corner angles [26]. There are established dicing techniques, such as laser grooving, blade dicing, etc. [27]. At the micrometer scale, laser grooving can remelt the chip surface and produce a rounded surface at the chip edge, which is less sharp than the 90° corner from blade dicing [28]. The blade dicing process also applies mechanical stresses to the die and may cause chipping and cracking on sidewalls, affecting the interfacial adhesion by having a different surface roughness [28]. Blade dicing might also cause an imperfectly flat surface and an imperfectly square corner [29].

Then, the substrate has a multi-layered structure with copper layers and dielectric layers, and it provides the connectivity to the chip via solder joints. The elastic modulus and CTE of the substrate are the most often considered parameters in evaluating the underfill reliability [7, 30, 31]. The elastic modulus of the substrate has less impact than the CTE

on the warpage of the flip-chip package [32]. Substrates with lower CTE help reduce the warpage of the flip-chip package during the temperature loading [33].

The CTE mismatch between different materials in the flip-chip assembly leads to shear stresses at the chip-underfill interfaces and underfill-substrate interfaces [30]. The geometry of the chip corners leads to stress concentrations in the underfill when the temperature is below the underfill curing temperature [30]. These stress concentration areas accumulate damage faster than low stress regions, and thus have a direct impact on the initiation of delamination and cracking.

2.1.3 Underfill Failure Modes

The failure modes of the underfill are divided into: 1) delaminations from the chip sidewalls, 2) delaminations from the chip kerf areas, which is between the die passivation and the underfill, 3) crack propagation in the underfill toward the substrate, 4) crack propagation toward the external underfill fillet, 5) crack propagation in the chip circuitry [34]. These failure modes usually progress as the number of cycles increases in reliability tests. After the reliability tests, which may include accelerated temperature cycling (ATC) and deep thermal cycling (DTC), several experimental approaches have been used to characterize the underfill damage. Table 2.1 summarizes the characterization techniques and compares their advantages and disadvantages.

Table 2.1 Summary of the analysis techniques for flip-chip failure analysis. [35, 36]

Technique	Advantages	Disadvantages
Scanning acoustic microscopy (C-SAM)	<ul style="list-style-type: none"> - Non-destructive. - Detects delamination, large voids, non-uniform underfill and crack. 	<ul style="list-style-type: none"> - Lower resolution (10μm). - Poor quality at edges. - Poor sensitivity to cracks.
3D X-ray tomography (CT)	<ul style="list-style-type: none"> - Useful for 3D packaging. - High spatial resolution. - Can image through metallisation. 	<ul style="list-style-type: none"> - Insensitive to cracks in underfill. - Long processing time. - Destructive.
Infrared (IR) microscopy	<ul style="list-style-type: none"> - Non-destructive. - Detects voids and cracks in solder bumps. 	<ul style="list-style-type: none"> - Suitable only for μm defect range; - Cannot penetrate through metal or thick underfill.
Cross sectioning optical microscopy/ scanning electron microscopy (SEM)	<ul style="list-style-type: none"> - Very high spatial resolution. 	<ul style="list-style-type: none"> - Destructive. - Time consuming.

Many experimental characterizations have observed the five underfill failure modes. In some highly stressed assemblies (such as those using large chips and high CTE underfills), the delamination is commonly observed from the sidewalls and from the chip kerf areas, starting from the chip corner, corresponding to the first and second underfill failure modes. Figure 2.3 shows the delaminations from the sidewalls [34, 37]. Figure 2.4 shows delaminations from the kerf area [38].

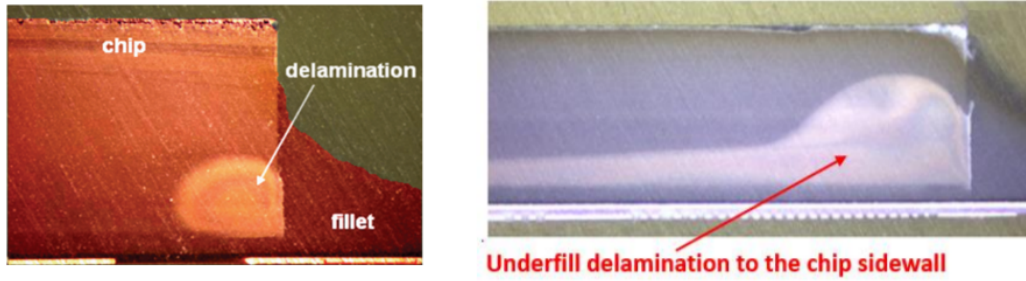


Figure 2.3 Delaminations from the sidewalls in a micrograph of a cross-section leaving a 25 μm underfill film on the sidewall. [34,37]

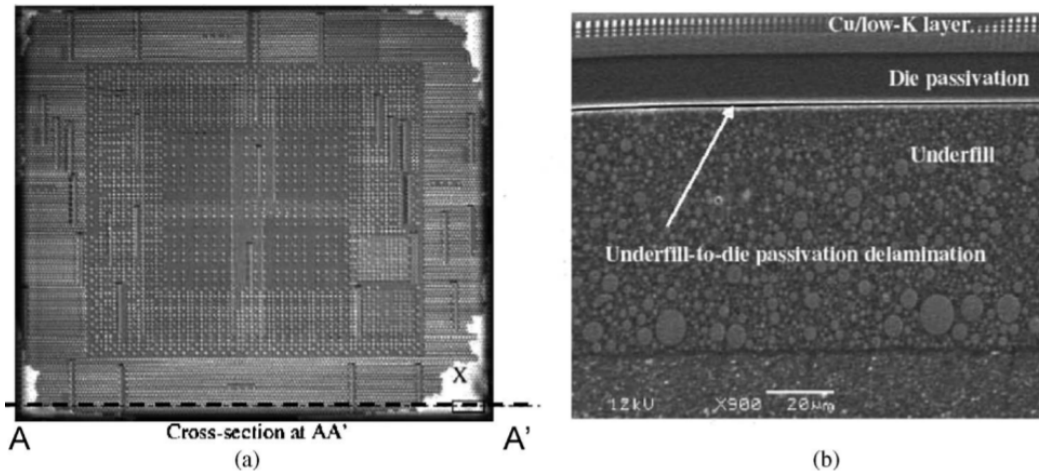


Figure 2.4 (a) C-SAM image of an underfill test vehicle after moisture exposure at 30 $^{\circ}\text{C}$ /60% relative humidity for 192 h, followed by three reflows at 250 $^{\circ}\text{C}$, (b) cross-sectional view of area X at AA'. [38]

Cracks propagation toward the substrate and the external underfill fillet are commonly observed as well [34,39], corresponding to the third and fourth underfill failure modes. Due to the stress concentration at the chip corner, the crack usually begins from the corner, as shown in Figure 2.5 and 2.6. The corner crack might also propagate to the substrate layers. The direction of the crack path depends on the local stress distribution, which is determined by the material properties of each component and the loading conditions. The stress distribution near a crack tip will be introduced in section 2.2.

Cracks in the chip circuitry correspond to the fifth underfill failure mode and are observed in the BEOL and the solder joints, as shown in Figures 2.7 and 2.8. The cracks in the BEOL and the solder joints may cause electrical failure of the entire device.

In order to obtain the best mechanical performance and reliability of the underfill, the choice of filler is important. Li et al. [44] developed a type of mesoporous SiO_2 nanoparticles with a low CTE, in order to achieve the same CTE for the underfill but fewer fillers.

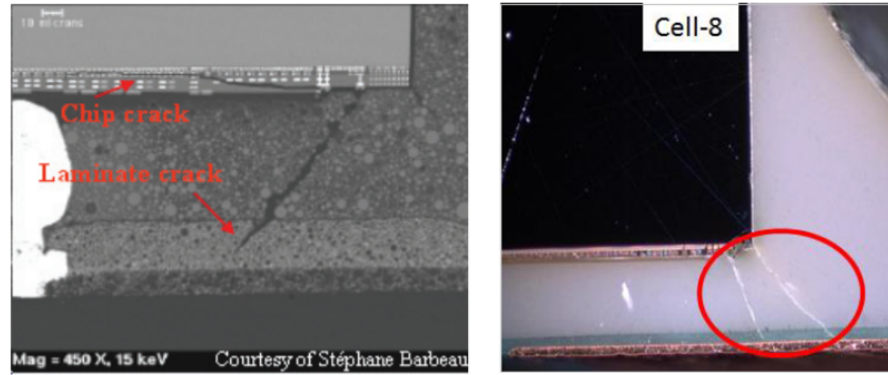


Figure 2.5 Cracks propagation in the underfill toward the substrate. The cross-sectional plane is perpendicular to the chip sidewall. [34, 39]

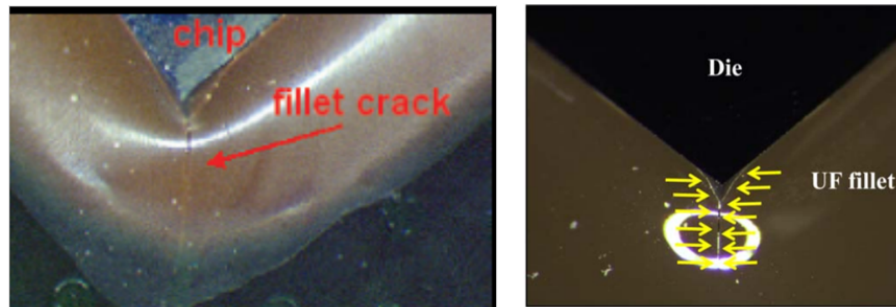


Figure 2.6 Underfill crack growth toward the external underfill fillet. [34, 40]

Compared with traditional non-porous SiO_2 composites, the new underfill can have a higher glass transition temperature and higher adhesion strength with silicon chips. Chen et al. [31] analyzed the influence of the filler volume ratio (20-68%), CTE (25-48 ppm/ $^{\circ}\text{C}$) and elastic modulus (3.8-12 GPa) of the underfill on the strength of adhesion at chip-underfill interfaces. Their results showed that an underfill with a higher filler volume ratio and a higher modulus can produce better adhesion at chip-underfill interfaces.

In addition to the filler volume ratio, the filler distribution may also affect the underfill reliability performance in some local areas. Due to the migration of electrostatic charge, the filler density is much smaller around the copper pillar than the other regions in the underfill (see Figure 2.2) [7]. Some mechanisms were found to understand the separation of filler in the resin, for example the gravity, capillary flow and surface modification of the filler. Such filler settling phenomena produce a pure resin zone near the chip-underfill interface, in which the stress/strain distribution can be different than that of an underfill with uniformly distributed fillers.

Apart from the material of the underfill itself, some other factors may still affect the underfill reliability, such as the chip corner shape, contamination on the chip surface, flux

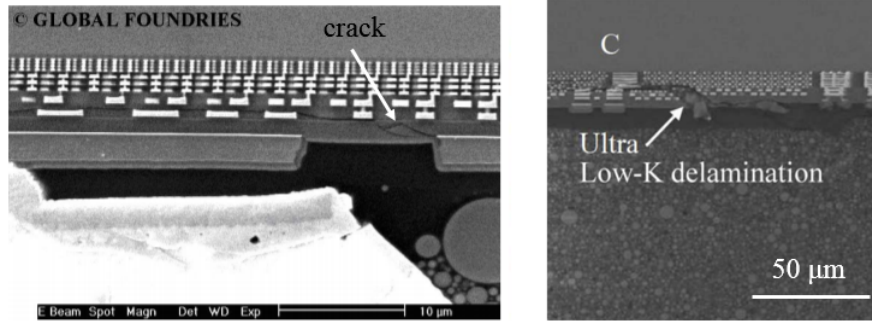


Figure 2.7 Cracks propagation in the BOEL. [41,42]

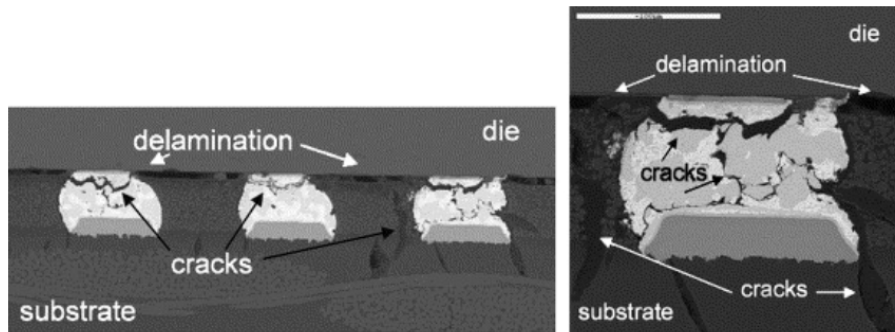


Figure 2.8 Cracks propagation in the solder joints. [43]

residues and moisture absorption. The chip-underfill interface strength can be influenced by the chip surface contamination and the flux residues. The presence of process-related contaminants on the chip surface might reduce the interface adhesion [45]. Flux residues can create underfill flow voids and weaken the adhesion to the die [46], whereas plasma cleaning of the die and substrate can reduce such voids [47,48]. Moisture absorption should be avoided as well, as it reduces the adhesion strength of the chip/underfill interface [49,50].

2.1.4 Influence of Underfill Failure on the Reliability of Assembly

The underfill failure can affect the reliability of other components, especially the electrical components. According to the five underfill failure modes presented in section 2.1.3, the crack propagation in the underfill towards the substrate and the crack propagation in the chip circuitry have a direct impact on the electrical reliability of the device. Figure 2.9 shows the cross-sectional view of a solder zone. When the chip-underfill interfacial delamination are present, the solder joints are subjected to higher stresses, since the delamination changes the continuity of the chip-underfill interface and induces stress concentrations in certain regions near the solder joints [51]. And then, if a crack is generated across the solder joint, an open circuit may cause an electrical failure of the entire device. The BEOL is another electrical component that is sensitive to cracks. The BEOL process consists

of fabricating stage contacts, interconnect wires, vias and dielectric structures. Cracks in the BEOL may lead to the electrical breakdown of the entire device. As the BEOL layer is located at the bottom of the chip, a delamination at the chip-underfill interface can directly influence the stress distribution in the BEOL and further induce cracking [52]. Thus, it is meaningful to first predict the underfill delamination and cracks from the chip corner, because these are the triggers of electrical failure.

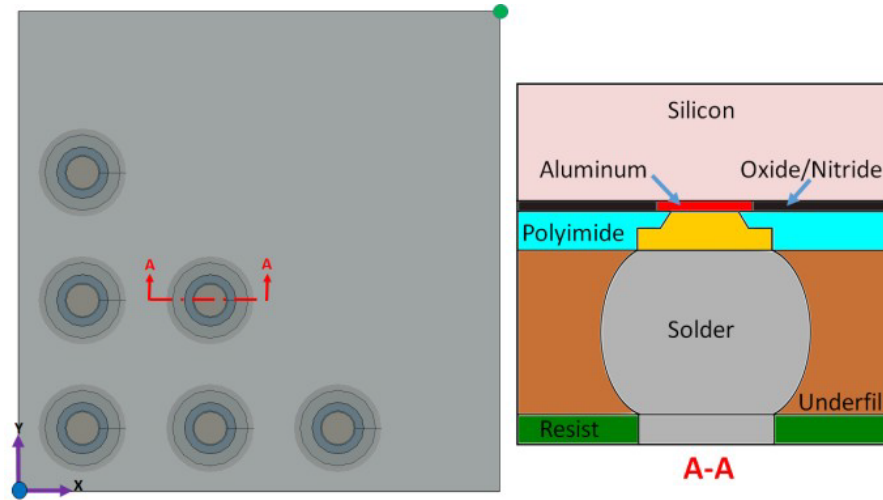


Figure 2.9 Cross-section of the solder joint zone. [39]

2.1.5 Mechanisms of Underfill Failure

After observing the five underfill failure modes, the mechanisms of each failure mode are summarized in this section. First, the delamination from the sidewalls is the result of the interfacial stress at the chip-underfill interface and the poor adhesion of the underfill to the chip sidewalls [34]. As the underfill has a higher CTE than the chip, the sidewalls suffer from shear stress during the temperature cycling. The maximum shear stresses at the chip-underfill sidewall near the chip corner increases with an increase in the underfill CTE, elastic modulus and T_g [34,37]. This mismatch leads to the high stress concentration at the sidewalls near the chip corner.

Second, the mechanism of the delamination from the kerf area is similar to that of the sidewalls, and is caused by the interfacial stress. During the thermal cycling test, the delaminations grow faster along the chip edges than toward the center of the chip [53]. The shear stress at the chip corners is a suitable metric for determining the delaminations initiation and growth [53]. Zhai et al. [54] found that the shear stress at the chip corner does not necessarily increase with the die size. The maximum shear stress at the chip corner occurs when the die side length is approximately 0.6 of the lid cavity side length (for square die and lid).

Third, the crack propagation in the underfill toward the substrate is determined by the stress distribution in the underfill and the fracture toughness of the underfill [26]. This crack originates from the chip corner, indicating that the chip corner stress is still the key metric for the cracking [34]. After the initiation of a crack, many crack directions have been observed [34, 39] (as shown in Figure 2.5).

Fourth, the crack propagation toward the external underfill fillet is also determined by the stress distribution in the underfill and the fracture toughness of the underfill. This crack can also be observed from the exterior surface of the underfill fillet, and is usually planar and along the diagonal direction [34, 40]. This indicates that this crack grows both in the vertical and diagonal directions after the crack initiation at the chip corner.

Lastly, the crack propagation in the chip circuitry is observed in the BEOL [41]. It is determined by the stress distribution in the BEOL and the fracture toughness of each component in the BEOL. As cracks may traverse multiple materials, such as the metal wires and dielectric materials, the crack direction could change frequently at each bimaterial interface [41, 42]. The complexity of the BEOL makes the crack trajectories difficult to predict [41, 42].

Overall, all the five failure mechanisms have been experimentally observed. Stress in the underfill at the chip corner is the key metric for all the five failure mechanisms [34]. The filler distribution, chip corner shape, underfill material properties and chip size could affect the shear stress at the chip corners [34, 37]. The flux residue and moisture absorption could reduce the chip-underfill interfacial adhesion [47, 48]. However, how exactly the stresses or strains distribute in the underfill is unknown from the observations of the five failure mechanisms. The damage evolution is not easily monitored to explain how the underfill damage grows with respect to the number of cycles. So, a measurement of stresses or strains with the underfill failure is desired and the measured values could be important to validate the results obtained from the underfill reliability models [55].

2.2 Analytical Solutions for Stress Distribution at Corners and Crack Regions

The stress distribution in the underfill is a key parameter to evaluate the underfill reliability. This section reviews the analytical solutions for the stress field on a bimaterial corner and a crack model, which are similar to the configuration of a chip corner and an underfill crack.

2.2.1 Stress Singularity

In a bimaterial model, the values of materials properties, such as the elastic moduli and Poisson's ratios, are discontinuous at the bimaterial interface. This discontinuity causes a stress discontinuity at the bimaterial interface, and may lead to an unbounded stress value at a sharp corner (the stress singularity) [56]. However, there is no stress singularity in a real structure, because the sharp corner is an artificial concept introduced by the model simplifications. So, it is necessary to understand how the stress distributes near the singularity points and the metric to evaluate the order of singularity. For 2D plane-strain, the singular stress field is generally expressed as [57–59]

$$\sigma_i \propto \frac{1}{r^{1-\lambda}}, \quad (2.1)$$

where σ_i is a stress component, r is the distance to the singular point and λ is the order of singularity. λ is a complex number with its imaginary part related to the oscillatory behaviour of the stress in the vicinity of the singular point [57, 58]. The oscillation implies unrealistic relative displacements of the material very near the singular point, which is the impossible physical overlap of crack faces [60]. Within the framework of linear elastic material response, there is no apparent way to eliminate the oscillation associated with the complex singularity [61]. If $0 < \text{Re}\lambda < 1$, the stress field is singular with $\sigma_i \rightarrow \infty$ as $r \rightarrow 0$. λ depends on both the material properties in the bimaterial system and the geometry of the corner. For 3D models, the singular stress field cannot be expressed explicitly, but the order of singularity for a 3D corner can still be obtained by numerical methods [62, 63].

2.2.2 Solutions on a Bimaterial Corner and a Crack

As the order of singularity λ depends on the geometry and material properties, this section presents the values of λ for different material properties, in plane-strain and 3D configurations. Figure 2.10 summarizes the relations between the λ and the ratio of the shear modulus of two materials Γ for a corner of 90° . $\Gamma = \mu_2/\mu_1$, where μ is the shear modulus (the subscript 1 and 2 represent the material in the regions of 90° and 270° , respectively). For plane-strain, $\kappa = 3 - 4\nu$ and ν is Poisson's ratio.

Several conclusions can be drawn from Figure 2.10 about the effects of the adhesion and delamination on the order of singularity. When two materials have the same shear moduli, the stress singularity at the corner vanishes ($\lambda = 1$). When $10^{-2} < \Gamma < 10^{-1}$ and $(\kappa_1, \kappa_2) = (2.2, 2.2)$ (Figure 2.10d), the situation is similar to the chip corner enclosed in the underfill and the order of singularity ranges from 0.6 to 0.8. The plane-strain configuration is effective when the out-of-plane stress can be neglected by symmetry, such

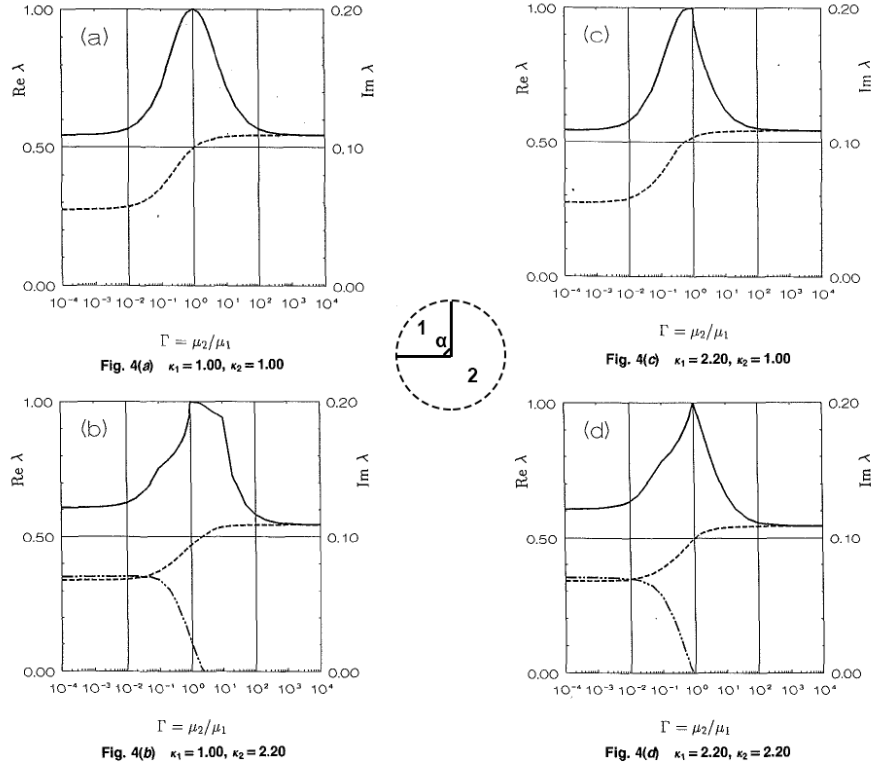


Figure 2.10 Order of stress singularity λ for rectangular corner $\alpha = 90^\circ$. The solid lines represent $\text{Re}\lambda$ for perfect adhesion ($\text{Im}\lambda$ vanishes), dashed and dash-dotted line represents $\text{Re}\lambda$ and $\text{Im}\lambda$ for delaminated interface. (a) $(\kappa_1, \kappa_2) = (1.0, 1.0)$, (b) $(\kappa_1, \kappa_2) = (1.0, 2.2)$, (c) $(\kappa_1, \kappa_2) = (2.2, 1.0)$, (d) $(\kappa_1, \kappa_2) = (2.2, 2.2)$. [64]

as at the chip edge midpoint. However, the order of singularity for the 3D configuration is more realistic for the chip corner.

The 3D corner is a solid concave corner between three non-parallel planes [62]. Figure 2.11 shows the order of singularity at the 3D corner in an homogeneous material with arbitrary elastic modulus and CTE. α is the angle between two vertical planes. $\lambda = 0.78$ when $\alpha = 90^\circ$ in the symmetrical mode (with symmetrical boundary conditions at the x-z plane), and this is similar to the situation of underfill surrounding the chip corner.

In addition to the chip corner configuration, the order of singularity at the crack tip is also an important parameter. The cracking can be regarded as a superposition of three independent modes (see Figure 2.12). These crack propagation modes are defined as follows [65]:

- Mode I: Opening mode (a tensile stress acting normal to the plane of the crack),
- Mode II: Sliding mode (a shear stress acting parallel to the plane of the crack and perpendicular to the crack front),

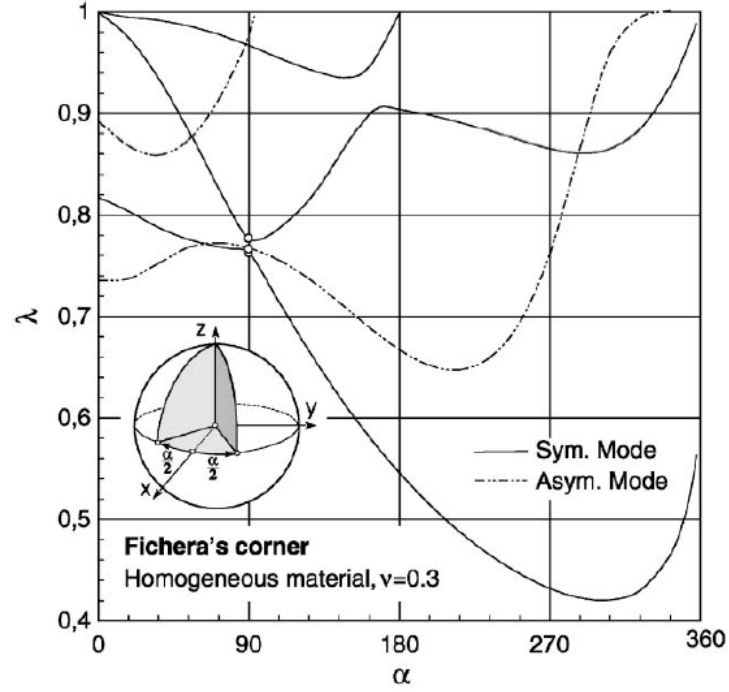


Figure 2.11 Order of singularity for 3D corners. [62]

- Mode III: Tearing mode (a shear stress acting parallel to the plane of the crack and parallel to the crack front).

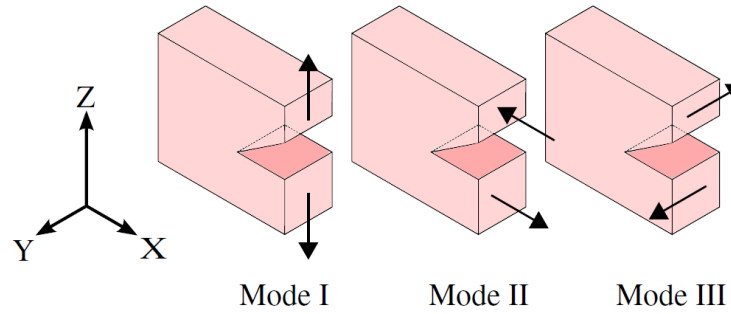


Figure 2.12 Three modes of crack propagation. [65]

The analytical solution for λ for a plane-strain crack is $\lambda = 0.5$ [66]. The stress component for a plane-strain crack is expressed in the form:

$$\sigma_i = \frac{K}{\sqrt{2\pi r}} f_i(\theta), \quad (2.2)$$

where σ_i is a stress component, K is the stress intensity factor, f_i is the dimensionless quantity that varies with the crack mode, (r, θ) are the polar coordinates with origin at the crack tip [66, 67].

For a crack in a 3D configuration, Figure 2.13 shows the order of singularity for wedge-shaped cracks, where α is the angle between two wedge edges [62]. When $\alpha = 180^\circ$, λ for all three crack modes is equal to 0.5, which is in agreement with the plane-strain configuration.

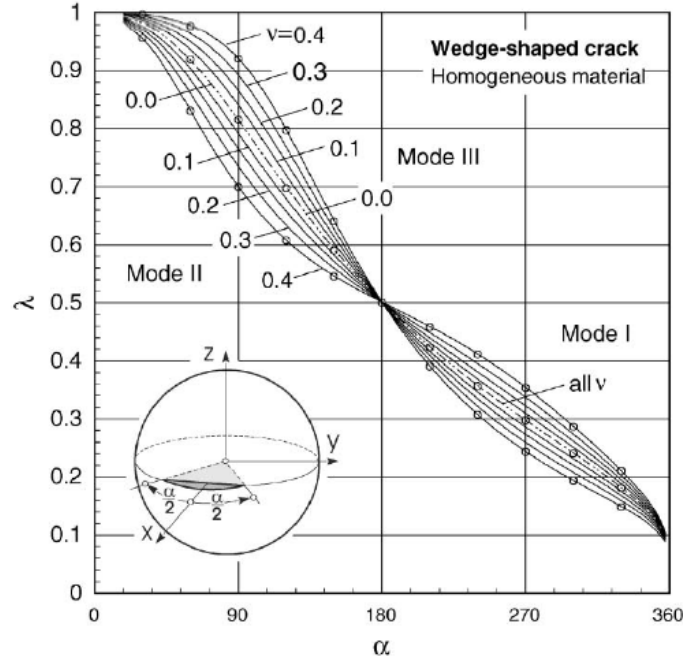


Figure 2.13 Order of singularity for wedge-shaped cracks. [62]

Overall, the order of singularity is a key parameter to describe the stress field near a singular point. This section shows two areas of interest for the underfill reliability, the chip corner and the crack tip, with analytical solutions on the order of singularity. For both 2D plane-strain and 3D configurations, the order of singularity has been sufficiently studied for rectangular corners and cracks. These reference results could be used to validate some of the underfill stress or strain fields obtained in the experiments and simulations.

2.3 Experimental Approaches on Fracture Properties and Local Strain Evaluation

The materials properties, especially the fracture toughness, are one of the most critical input parameters in the modeling of underfill failure. The fracture properties are intrinsic to the materials, and have to be measured experimentally. The fracture toughness test is used to evaluate the bulk material cracking and the cantilever beam test is often applied to evaluate the bimaterial interface adhesion strength. Moreover, several approaches of local deformation measurement will be introduced and discussed in this section.

2.3.1 Fracture Properties Test

The fracture toughness is a critical parameter for fracture mechanics in bulk materials. When an appropriate force is applied, the crack propagates from the crack front. In order to measure the fracture toughness in mode I (K_{Ic}), the standard ASTM E1820 [68] gives a procedure with a recommend specimen, such as the single-edge bending (SEB), compact (CT) and disk-shaped compact (DCT) specimen. The end notched flexure (ENF) sample [69] and the edge crack torsion (ECT) sample [70] are widely used to measure K_{IIc} (mode II fracture toughness) and K_{IIIc} (mode III fracture toughness), respectively. For various loadings, if the stress intensity factor K at the chip corner is larger than the fracture toughness, crack initiation is assumed to occur [58]. Underfills with higher fracture toughness have less cracks in reliability tests [71]. An underfill bulk fracture toughness of at least $2.0 \text{ MPa}\cdot\text{m}^{0.5}$ is essential to prevent fillet cracking [37].

In addition to the fracture toughness in bulk materials, the chip-underfill interfacial fracture properties are also required for the underfill reliability. The cantilever beam (CLB) test, in particular the double cantilever beam (DCB) test, is commonly used to measure the Mode I inter-laminar fracture toughness [72]. The specimen contains an initial crack at one end of the bimaterial interface, which grows as the two beams of the specimen are pulled apart. A typical setup of DCB test is illustrated in Figure 2.14.

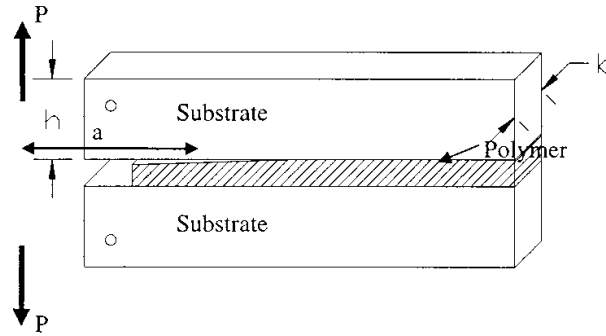


Figure 2.14 Diagram of the double cantilever beam test. P is the force load, h and b are the height and width of the beam. [73]

The interfacial energy release rate G for the bimaterial system between the beams is expressed as [73]:

$$G = \frac{6P^2a^2}{b^2h^3} \left(\frac{1}{E_1} + \frac{1}{E_2} \right), \quad (2.3)$$

where b and h are the width and thickness of the beam, a is the length of the crack, P is the force load, E_1 and E_2 are the elastic moduli of material I and II in the bimaterial system. From the DCB apparatus, several similar methods were also developed. For example, the simple cantilever beam (SCB) [74, 75] was used for simplifying the loading condition.

The DCB at the assembly scale [76] can measure the chip-underfill interface adhesion in an assembled package. A wedge delamination method (WDM) [65] was also developed by driving a sharp wedge between the bimaterial interface. The interfacial energy release rate can be derived from the maximum insertion force of the wedge and the geometry of each component. WDM is more appropriate in measuring the interfacial fracture toughness for brittle materials compared to the cantilever beam methods [65].

A good correlation between the underfill reliability data and CLB data was observed in the literature. Paquet et al. [34] found that with an optimized filler treatment, higher interfacial fracture toughness between the chip and the underfill was obtained, and the no electrical fail parts were observed in the 700-cycle DTC test (-55 to 125°C). With a modified resin type (stiffer molecular structure) that lead to higher interfacial toughness, no underfill delamination was reported in the 1500-cycle DTC test (-55 to 125°C) [37].

However, both the bulk fracture toughness and the interfacial fracture toughness of the underfill are measured *ex-situ*, with some clear limitations: 1) there is no stress concentration in the CLB configuration similar to what occurs at the chip corner; 2) between the fracture toughness test sample and the underfill in a real flip-chip package, their filler distribution might be different and cause variations in the values of fracture toughness; 3) the microscale surface characteristics of the chip might be critical to the fracture properties [34]. Thus, an *in-situ* experimental technique is desired to measure the fracture properties in the underfill.

2.3.2 Carbon Nanotube Strain Sensor

In addition to the fracture toughness of bulk materials and the interfacial adhesion at bimaterial interfaces, *in-situ* measurements of the underfill strain are valuable to accelerate the development and validation of numerical models. The strains in the underfill are generated from the thermal loading and are challenging to measure directly because of the small dimensions of the chip corner region ($< 1 \text{ mm}^3$). The chip corner is also totally hidden inside the underfill and is not directly accessible. The finite element method can calculate the stresses and strains numerically, but it cannot always provide a correct result because of the limitations of mechanical theory, in particular in a singular and non-continuous system (e.g. cracks and delamination). In order to carry out a direct characterization on the underfill deformation at the micron scale, several optical and non-destructive techniques have been developed so far. Carbon nanotubes (CNTs) can be good strain sensors, because they are small enough to disperse in the underfill and their Raman shift responds linearly to the imposed strains [77]. Three characteristic peaks are normally observed by Raman spectroscopy: the D band, G band and G' band at 1350

cm^{-1} , 1580 cm^{-1} and 2700 cm^{-1} respectively, as shown in Figure 2.15. Although the D and G bands might be overlapped by the epoxy bands, the G' band can still be clearly observed with good sensitivity to the applied traction and compression. Figure 2.16 shows a typical linear response of the Raman shift on the compression strain. In fact, Raman spectroscopy is a mature technique in the semiconductor industry, since semiconductor materials often have good Raman optical activities [78].

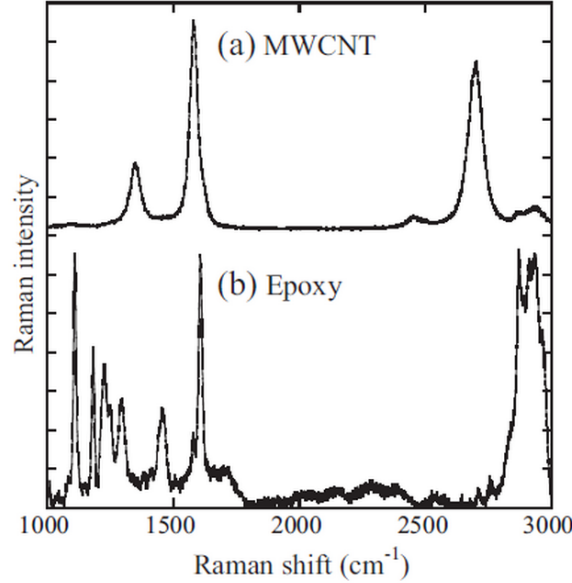


Figure 2.15 Typical Raman spectra of MWCNT and Epoxy between $1000\text{-}3000 \text{ cm}^{-1}$. [77]

Preliminary research on the direct measurement of local strains in the underfill was carried by the IBM T.J. Watson Research Center, by dispersing single-wall CNTs in the underfill as Raman strain sensors [55, 79]. This approach provided the two-dimensional strain components x , y and xy by selecting individual nanotubes oriented along the appropriate direction, a somewhat time-consuming process. However, the position of the measured maximum strain appeared to be quite random and not located at the chip corner, thus raising questions about the validity of the method [55].

2.3.3 Digital Image Correlation Method

The digital image correlation method is a full-field non-contact optical method to measure the surface deformation of materials under various loading conditions [80]. Developed by Sutton et al. in 1983 [81], this method has been widely applied in many fields of science and engineering [82]. Compared to conventional strain gauges, the measurement of the microscale and nanoscale deformations is easier by DIC combined with high-resolution microscopes [83, 84]. In order to perform DIC, an area of interest needs to be chosen

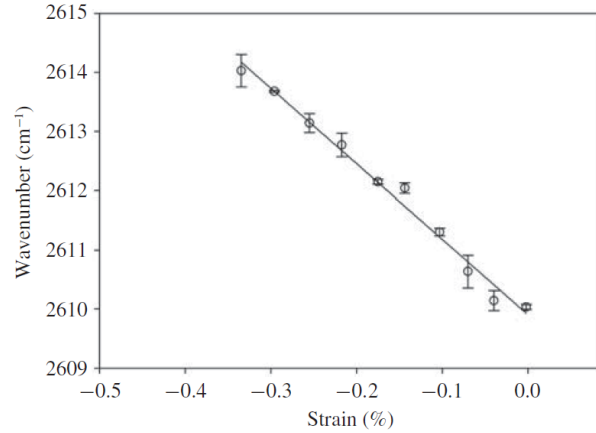


Figure 2.16 Shift in G' band with compression strain. [55]

and divided into a grid, as shown in Figure 2.17(a). Figure 2.17(b) shows the tracking of movement of the center point $P(x, y)$ (undeformed image) to $P'(x', y')$ (deformed image) by finding the maximum correlated subsets in the deformed and undeformed images. The full-field deformation is obtained by calculating the difference of displacements between adjacent subsets. In addition, the digital volume correlation (DVC), also called volumetric-DIC, was developed in 1999 [85]. The DVC extends the 2D DIC method to 3D, and provides the internal deformation of solid objects by tracking the movement of volume units (voxels).

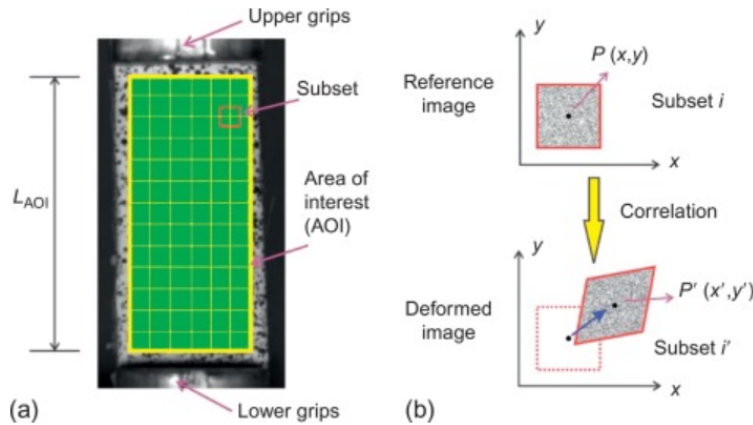


Figure 2.17 (a) Area of interest (AOI) and subsets in a reference image; (b) schematic presentation of a reference subset before deformation and the corresponding target subset after deformation. [86]

Acquiring high quality images is the key challenge for both the DIC and DVC method. For the surface deformation measurement by 2D DIC, most optical microscopes are able to capture clear images with speckles or position markers. However, if trying to measure the internal deformation inside a solid object, the X-ray micro-computed tomography

(micro-CT) or the confocal microscopy is required. The micro-CT uses X-rays to create a series of cross-sections over a solid object by rotational scanning, as shown in Figure 2.18. Lall et al. [87–89] applied the micro-CT and DVC for 3-dimensional reconstruction and strain evaluation on bonding wires and solder joints. However, due to the rotational scanning configuration, the spatial resolution is limited by the total size of the assembly. The contrast of the underfill and other polymer components is not great in X-ray images. Metallic particle fillers might be used to improve the contrast, but can affect the mechanical properties of the underfill as well. In addition, applying a thermal load in a tomography machine can be difficult. Thus, the micro-CT is not the best way to obtain the underfill images near the chip corner.

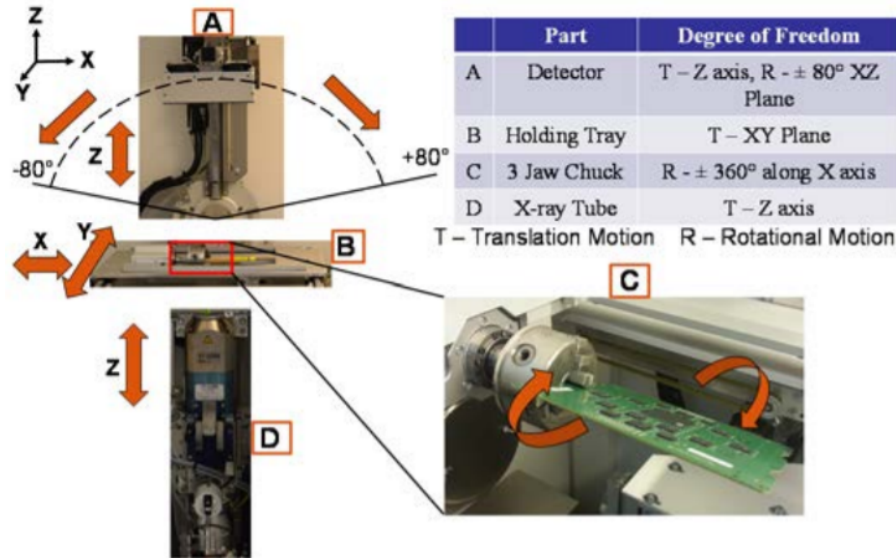


Figure 2.18 Sample mounting configuration in the micro-CT system. [87]

The laser scanning confocal microscopy (LSCM) avoids some of the shortcomings of the micro-CT and can be a useful tool for capturing the 3D images in the underfill if the substrate and underfill are quasi-transparent to the laser [90]. As the LSCM scans the sample from one side by controlling the position of the focal plane, it can provide a series of high resolution images with a simple configuration. Franck et al. [91] combined the LSCM with the DVC and measured the strain field near a spherical inclusion in agarose gel under uniaxial compression. A high strain concentration of ϵ_{33} on the compression direction of up to 25% was captured near the spherical inclusion, as shown in Figure 2.19. In this thesis, the LSCM and DIC are extensively used to measure the underfill local deformation near the chip corner and cracks, in a new technique named the confocal-DIC technique. The detailed description of the LSCM will be presented in Chapter 3.

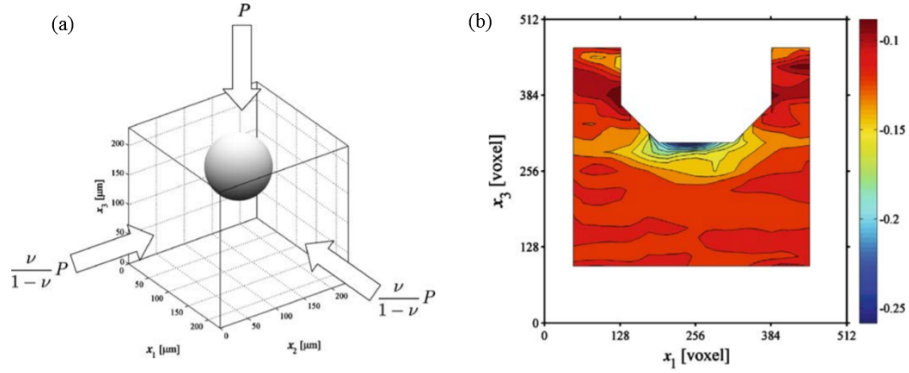


Figure 2.19 (a) Schematic of uniaxial constrained compression of a spherical inclusion in a matrix with a sliding interface, (b) experimentally measured strain field ϵ_{33} near a spherical inclusion. [91]

2.3.4 Other Techniques for Underfill Strain Measurements

In addition to the direct strain measurements at the chip corner, some indirect methods were developed to measure the strains on a cross-sectional plane in flip-chip packages. Wang et al. [92] used the 2D DIC on the cross-section of a flip-chip package to calculate the strain component ϵ_y at 100°C, with a reference temperature of 23°C, as shown in Figure 2.20. The maximum ϵ_y is located near the chip corner. The average ϵ_y for the $30 \times 50 \mu\text{m}^2$ area at the chip corner also increased as the temperature increased from 23 to 100°C. Moiré interferometry is another optical method and has been used to measure the residual thermal strains in the underfill after cross-sectioning, based on the phase difference between two images [93]. For the underfill on the cross-sectional plane, the measured residual strain distributions were the similar to the FEM simulations [93].

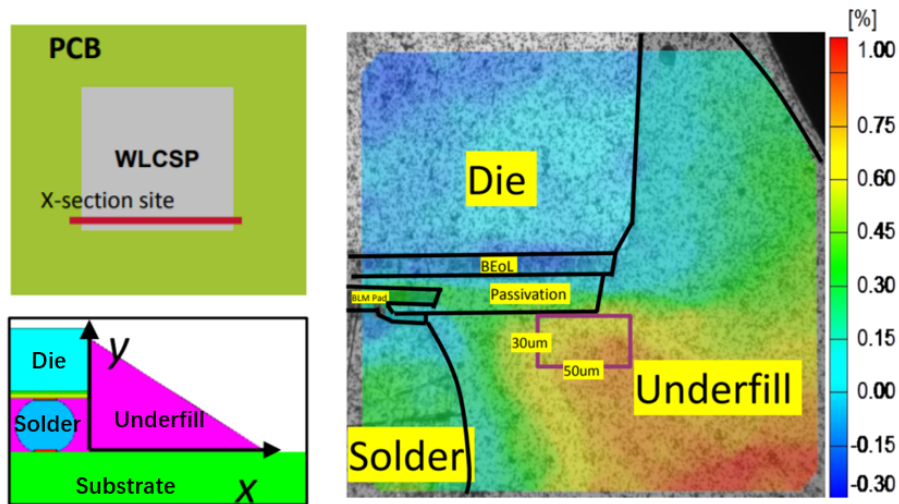


Figure 2.20 Strain contour ϵ_y on the X-section at 100°C. [92]

Due to the high-resolution and *in-situ* requirements for the underfill strain measurements, the applicable methods are very limited. Compared with the strain measurements inside the underfill, the measurements on the cross-sectional plane are easier to implement with high-resolution SEM (nanometre resolution) [92]. This method is able to measure areas of interest on a much smaller scale than optical microscopy. However, the limitations of the cross-sectional strain measurements are clear: 1) it is a destructive method; 2) it can only provide strain results for one single plane; 3) the boundary conditions of the cross-sectional surface becomes a free surface, different from its original state in the package [94]. Thus, the cross-sectional strain measurements could help understand the chip corner strain distribution, but are not the best way to obtain the underfill strains for this project.

2.4 Numerical Simulations of Underfill Cracking and Delamination

2.4.1 Finite Element Method for Underfill Modeling

The finite element method (FEM) is widely used to solve engineering problems, such as structural analysis, heat transfer, fluid flow and electromagnetic potential [95]. In the FEM model, a discretization is applied on the volumes to smaller and simpler parts, called finite elements. The FEM formulation of a boundary value problem results in a system of algebraic equations. For structural analysis, the field of displacements is finally solved, and is used to calculate the fields of strain and stress. Figure 2.21 shows a typical flow chart of the solution process of the FEM in semiconductor packaging. In general, the pre-processing and post-processing are the most time-consuming steps during the whole process of the finite element analysis.

In the field of reliability for microelectronic packaging, 2D plane-strain models were first used to evaluate the stress and strain in each components [96]. The simplification to 2D plane-strain was effective when the out-of-plane stress could be neglected by symmetry, such as at the chip edge midpoint planes and the chip diagonal planes. In addition, the 2D results can be easily compared with analytical solutions. However, the 2D plane-strain configuration may seriously underestimate the magnitude of crack driving forces [97]. In some critical regions, such as the chip corner and solder joints, a full 3D model is required, since the plane-strain approximation is no longer applicable in such complex regions [98]. The stress distribution around the chip corner has been modelled for both 2D plane-strain [57,75,99,100] and 3D configurations [98,101,102]. These studies used classical linear elastic FEM models to calculate the stress at chip corners. In the existing 3D models, the chip corners were considered as perfectly sharp with orthogonal planes, and the effect

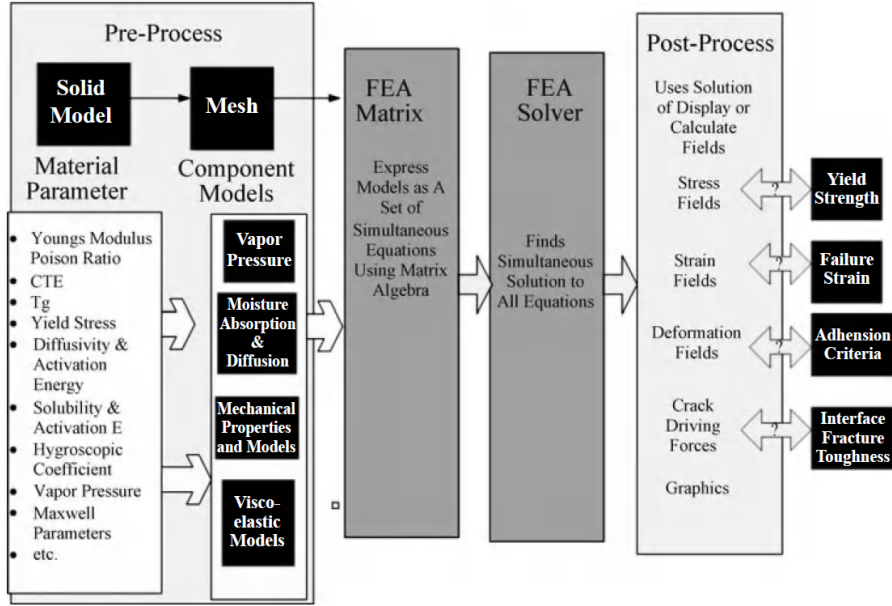


Figure 2.21 Finite element flow chart for semiconductor packaging modeling. [95]

of corner radius and angles between the sidewalls and bottom surface of the die were not included. The effect of the corner shape on the chip corner stress was only analyzed in a 2D model, but the corresponding underfill stress was not studied [103]. The filler settling effect on the stresses in solders was modelled by a bilayered underfill model, but the corresponding underfill reliability was not quantified [20, 104]. Thus, the numerical study on the effect of detailed geometrical and material properties on the underfill reliability is still not sufficient in the literature.

2.4.2 Modeling Underfill Cracks

The studies on the stress distribution near the underfill cracks and the modeling on the crack propagation are limited in the literature. Mahalingam [105] constructed a 3D assembly model with cracks of different sizes in the underfill fillet and studied the relationship among the underfill modulus, size of cracks and the energy release rate to guide the design of the underfill. The results showed that the energy release rate increases linearly with respect to the elastic modulus of the underfill, and increases non-linearly with respect to the CTE of the underfill. Kacker et al. [30] demonstrated that the geometry of the underfill fillet can directly influence the delamination around the chip corner, which is induced by the shear stress. The distribution of normal stresses and shear stresses between the chip and the underfill was also studied. The shear and normal stresses remained low in most regions from the centre of the chip and increases rapidly closer to the chip corner [106]. This phenomenon is consistent with the singularity theory in section 2.2.

Ayhan et al. [107] found that the stress distribution near the underfill crack between the results in the 2D plane-strain and 3D models could be significant different, because the out-of-plane thermal strain has a significant effect on the solution.

Although the conventional FEM has been widely used in structural and thermal analysis, it is still difficult to generate an appropriate underfill model with cracks by the FEM, since the accuracy of local stress estimates is highly dependent on the size and quality of the mesh [108]. The FEM requires an extremely refined mesh in the area of the crack tip and an update after each increment of crack growth. The extended finite element method (XFEM) was first developed by Ted Belytschko et al. in 1999 [109], and alleviates some of the shortcomings of the FEM in modeling cracks. The XFEM uses enriched nodes in the crack-related area with additional displacement functions. This improvement avoids refining and updating the mesh in the vicinity of the crack tip, which makes XFEM a good engineering approach for modeling both stationary cracks and crack-growth problems [110]. Figure 2.22 shows a typical subdivision of elements intersected by a crack [111].

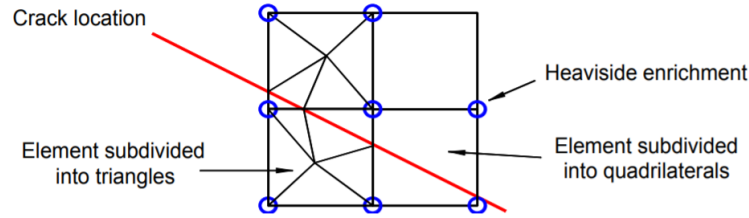


Figure 2.22 Typical subdivision of elements intersected by a crack. [111]

The XFEM offers the following features [112]:

1. extends the FEM to account for cracks based on the concept of partition of unity;
2. offers a way to model the cracks without explicitly meshing the crack surface;
3. allows for arbitrary crack growth within the existing mesh;
4. accessible for most commercial solvers, such as ANSYS, ABAQUS, LS-DYNA, NAS-TRAN and COMSOL.

Previous researchers have applied XFEM in various other fields such as concrete, composite materials and metal sheets [113–115]. In the packaging area, the XFEM has been applied in estimating the cracks in solder joints and the model predictions correlated well with the observed failure modes [116–118]. Cracks initiated from the copper-TSV were also simulated by the XFEM to help clarify the crack propagation paths in silicon [119, 120]. However, XFEM has not been applied to the underfill cracking problem so far, and has a good potential to estimate the crack trajectories in the underfill.

2.4.3 Modeling Interfacial Delamination

The delamination problem at a bimaterial interface is somewhat simpler than the crack problem in bulk materials, because the delamination is always along a predefined path, specifically the bimaterial interface. Several fracture mechanics methods are available to simulate an interface delamination, such as the virtual crack closure technique (VCCT) and the cohesive zone model (CZM).

The VCCT approach is based on linear elastic fracture mechanics and relies on calculating the strain energy release rate at the crack tip [121]. This is an energy-based technique and an initial crack is required to start the calculation process. As shown in Figure 2.23, when the crack propagates by an increment Δa , the released strain energy G^* is the same as the energy to close the same distance of the crack surfaces. So, the crack propagates when the following relationship is fulfilled:

$$f(G_{Ic}, G_{IIc}, G_{IIIc}, G_I, G_{II}, G_{III}) \geq 1, \quad (2.4)$$

where $G_{Ic}, G_{IIc}, G_{IIIc}$ are the critical energy release rates of mode I, II and III cracks, and G_I, G_{II}, G_{III} are the current energy release rates at the crack tip. The fracture criterion f can be expressed in several forms, such as the critical energy release rate criterion for 2D and 3D simulations:

$$f = \frac{G_T}{G_{Tc}} = \frac{G_I + G_{II} + G_{III}}{G_{Ic} + G_{IIc} + G_{IIIc}}, \quad (2.5)$$

where G_T is the total energy release rate and G_{Tc} is the critical total energy release rate. The linear fracture criterion for 3D mixed-mode fracture can be expressed as

$$f = \frac{G_I}{G_{Ic}} + \frac{G_{II}}{G_{IIc}} + \frac{G_{III}}{G_{IIIc}}, \quad (2.6)$$

and the B-K fracture criterion for composite interfacial fracture can be expressed as [122]

$$f = \frac{G_T}{G_{Ic} + (G_{IIc} - G_{Ic}) \left(\frac{G_{IIc} + G_{IIIc}}{G_T} \right)^\eta}, \quad (2.7)$$

where η is a material constant.

Alternatively, the cohesive zone model can be used to simulate the delamination at a bimaterial interface as well [124]. The interface elements are applied between two components and a cohesive zone is defined on the interface elements, as shown in Figure 2.24. The node pairs along the thickness direction (L, I) and (K, J) are initially coincident. The interface separation between the chip and underfill is represented by an increasing displacement

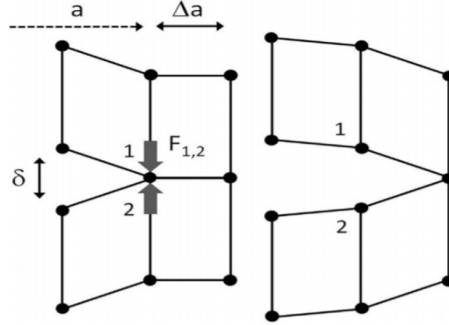


Figure 2.23 Schematic concept of the Virtual Crack Closure Technique. An interface crack of length a is extended a small amount Δa when the energy released equals the interface toughness G_{Ic} . [123]

between node pairs within the interface element itself. A bilinear law is commonly used as the mixed-mode fracture criterion,

$$f = \sqrt{\left(\frac{\delta_n}{\delta_n^c}\right)^2 + \beta^2 \left(\frac{\delta_t}{\delta_t^c}\right)^2}, \quad (2.8)$$

where δ_n and δ_t are the normal and tangential displacement jumps in the interface elements, δ_n^c and δ_t^c are the normal and tangential displacement jumps at the completion of debonding, β is the weight to the tangential and normal displacement jumps. Figure 2.25 shows a typical bilinear cohesive law. The interface has an initial linear elastic response and begins to be damaged when the displacement jump arrives at δ^* . Then, a linear softening occurs and the internal stress reduces to zero, which indicates the final separation. The area under the curve in Figure 2.25 represents the strain energy released at the interface elements. Compared to the VCCT, CZM does not need to define an initial crack in the model. More studies on the traction-separation relationships on different materials have been included in reference [125, 126].

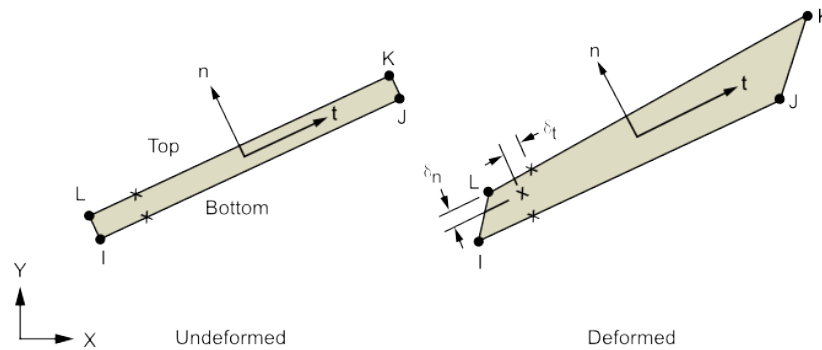


Figure 2.24 Schematic of interface elements. [112]

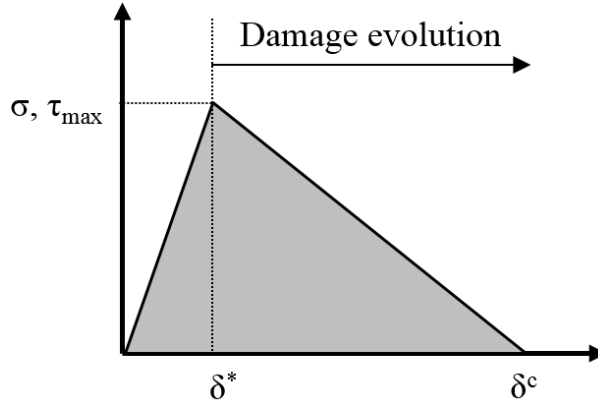


Figure 2.25 Typical bilinear cohesive law. [112]

In the packaging field, both the VCCT and CZM methods have been applied to the problem of delamination [121, 127, 128]. Figure 2.26 shows a typical FEM model for underfill delamination. For the chip-underfill delamination at chip corners, the strain energy release rate G increased with increasing underfill elastic modulus and CTE [52, 97]. For the chip-underfill delamination near solder joints, G increased with decreasing underfill modulus and increasing underfill CTE [52]. With the growth of the chip-underfill interfacial delamination, the solder fatigue life was greatly reduced [129]. In addition to the chip-underfill interface, the delamination was also modelled for the BEOL layer in references [130, 131]. A delamination at the top metal level in the BEOL was found to be the most critical region, which had the largest strain energy release rate [130]. So far, the modeling of the chip-underfill delamination was focused on the strain energy release rate with respect to the underfill materials properties and the delamination size [52, 121, 127]. How the delamination grows at the chip-underfill interface during thermal cycling and the delamination growth rate have not been fully studied [132]. Section 2.4.4 will continue to discuss the modeling methods for the cracking and delamination under cycling loading conditions and the advances in underfill cracking and delamination during thermal cycling.

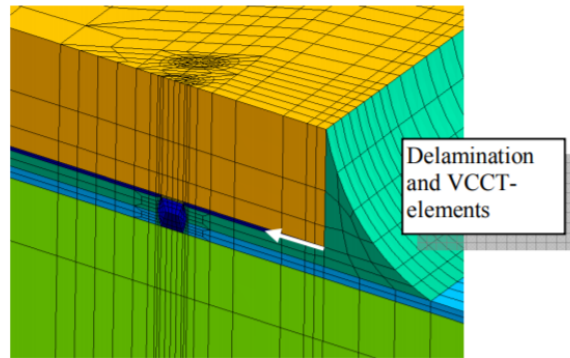


Figure 2.26 Typical FEM model for the underfill delamination. [127]

2.4.4 Fatigue Life Model

As microelectronic devices usually work under thermal cycles, the cyclic fatigue damage is an important aspect of the life of devices. The Coffin-Manson equation is an empirical model that is widely used to describe the fatigue behavior by [133]

$$\Delta\epsilon = C_1 N_f^b, \quad (2.9)$$

where $\Delta\epsilon$ is the strain amplitude during cyclic loading and is equal to the difference between the maximum and minimum strain ($\epsilon_{\max} - \epsilon_{\min}$), N_f is the number of cycles to failure, and C_1 and b are constants. These two constants are usually obtained by fitting the equation to experimental results of the number of cycles and strain amplitude.

The Coffin-Manson model is empirical and does not provide any detail about the damage process, such as the change in crack length during the applied loading cycles. When simulating the fatigue crack growth with respect to the number of cycles, the stress value near the crack tip is necessary. The crack growth rate can be expressed as [134]

$$\frac{da}{dN} = g(\Delta K, R), \quad (2.10)$$

where da is the crack increment length, dN is the number of applied loading cycles, $\Delta K = K_{\max} - K_{\min}$ is the amplitude of the stress intensity factor at the crack tip, and $R = K_{\min}/K_{\max}$ is the stress ratio. g is a function of ΔK and R . To estimate the growth of a certain delamination or crack, Paris' law is a fundamental model to relate the crack length to the fatigue life, which is visualized as a linear region on a log-log plot of da/dN and ΔK , as the regime B shown in Figure 2.27. Paris' law is expressed as

$$\frac{da}{dN} = C(\Delta K)^m, \quad (2.11)$$

where C and m are constants obtained from experiments by fitting Equation 2.11 to the crack growth rate and stress intensity amplitude.

In the field of underfill reliability, most studies have focused on experimentally obtaining the constants of the Paris' law for the underfill [135–138]. In addition to the constants, Ozkan et al. [132] developed an interfacial delamination growth model according to Paris' law, with a periodical temperature loading from 170 to 25°C. Figure 2.28 shows the new delamination front dimensions for each step of the fatigue delamination simulation, starting from a circular shape and evolving to a triangle shape. The delamination near the edges of the chip grew at a higher rate than the inside of the chip. However, this model did not

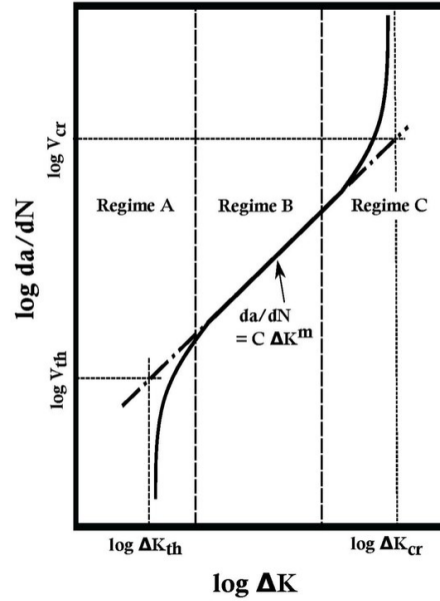


Figure 2.27 Typical relationship between the crack growth rate and stress intensity amplitude. [134]

have underfill fillets, leading to different boundary conditions at the chip corner regions of the model than in a real flip-chip package. Similar studies and results could also be found in [139, 140], but the model-obtained delamination areas were not experimentally validated. No studies were found on the modeling of underfill fatigue crack growth. Thus, in the field of flip-chip packages, the delamination growth and the underfill crack growth with respect to the number of thermal cycles still require further studies.

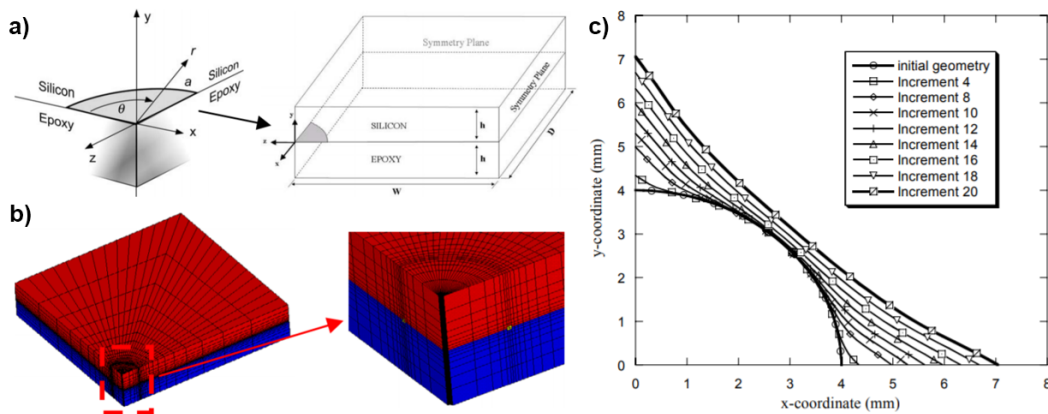


Figure 2.28 (a) Circular interface corner delamination between silicon/epoxy interface, (b) finite element mesh, and (c) the advancing circular corner delamination. [132]

2.4.5 Crack Modeling for Particle Composites

The numerical study of underfill cracking is limited, but the advances in crack modeling of polymer-matrix composite with particle fillers are still very meaningful to this project. FEM [141, 142], boundary element method (BEM) [143, 144] and XFEM [145] have been used for the crack modeling of particle composites. Three possible fracture mechanisms of the crack-particle interaction could be identified, which are the particle fracture, crack deflection and interface debonding (see Figure 2.29). The key aspects affecting the fracture mechanisms include: 1) the mismatch in fracture properties (i.e., mismatch in fracture strength and fracture energy), 2) the effect of interfacial properties (i.e., interfacial strength and toughness), and 3) the flaws inside the particle and at the particle-matrix interface [146–148].

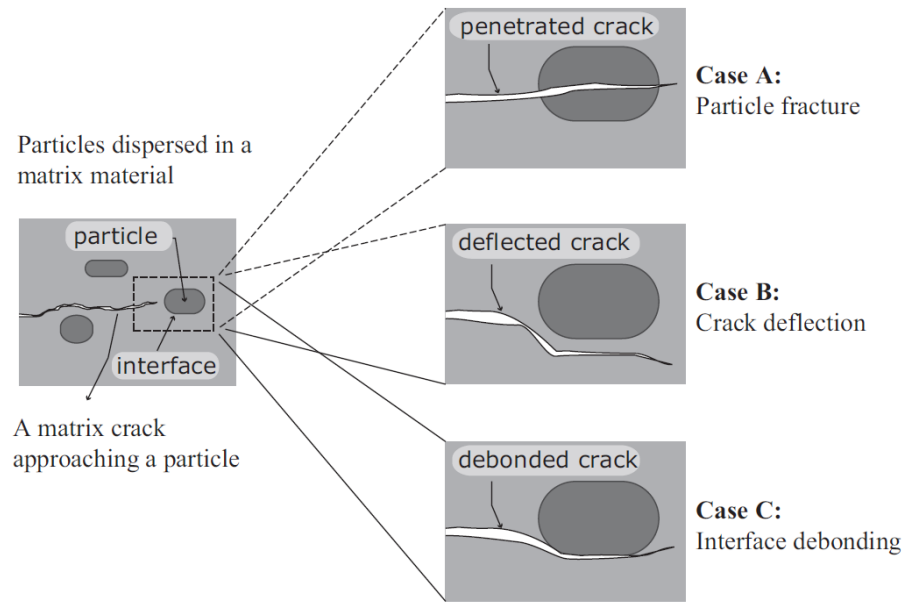


Figure 2.29 Crack-particle interaction in a particulate system showing three possible fracture mechanisms, namely particle fracture, crack deflection and interface debonding. [146]

For high modulus and high strength particle fillers, such as the SiO_2 particle fillers in the underfill, the particle fracture (case A in Figure 2.29) is seldom observed. This phenomenon can also be supported by the result of [146]. The particle-matrix interface debonding will occur if the interface strength is reduced below a certain limit [146, 149]. For completing the perfect model of underfill reliability with a high filler density, these existing methods should be applied to simulate crack growth in the underfill with fillers.

2.4.6 Stochastic Modeling for Fractures

The numerical methods presented in sections 2.4.1 to 2.4.5 are deterministic, and do not take the variability of input parameters into consideration. The variability of input parameters for underfill reliability models has been discussed in section 1.3.3. If one seeks to obtain reliable numerical predictions which are usable in a design process or for decision-making, it is essential to incorporate the uncertainties on model geometries and material properties by a stochastic approach to the model [150].

The stochastic finite element method (SFEM) is a powerful tool in computational stochastic mechanics and is an extension of the classical FEM [151]. There are two main variants of SFEM in the literature: 1) the perturbation approach based on a Taylor series expansion of the response vector (reaction force or displacement) [152] and 2) the spectral stochastic finite element method (SSFEM) where each response quantity is represented by a series of random Hermite polynomials [153]. Monte-Carlo simulation (MCS) is another commonly used method [151]. MCS relies on repeated random sampling of input variables and solves a deterministic problem a large number of times. MCS is often used as a reference method for other approaches due to its robustness and simplicity, and is sometimes combined with the two aforementioned SFEM variants [151, 154]. Similar stochastic strategies are also developed for XFEM [150, 155].

Specifically for the stochastic modeling for fracture problems, Hamdia et al. [156] studied the effect of uncertain input parameters on the fracture in polymer-based particle nanocomposites. The uncertain input parameters included the volume fraction of the nanoparticles, the diameter of the nanoparticle, Young's modulus of the epoxy matrix, the maximum allowable principal stress, the thickness, and Young's modulus of the particle-matrix interface zone. A polynomial chaos expansion model (PCE, one type of SSFEM) was constructed for this fracture problem. The results showed that the maximum allowable principal stress and Young's modulus of the epoxy matrix are the most significant parameters that dominate the variance in the fracture energy at the crack tip.

The fatigue growth modeling with stochastic perturbation series expansion method (SPSEM) [157] and PCE [158] have been studied for a 2D standard central crack configuration. Figure 2.30a illustrates the model configuration. In reference [157], the crack growth model was based on the Paris' law and the coefficient of variance (standard deviation divided by the mean) of two material constants were set to 0.001. Figure 2.30b shows the comparison among crack length history probabilistic regions. The experiment results fall within the six standard deviations ($\pm 6\sigma$) range predicted by the SPSEM, which are also in close agreement with the result of MCS.

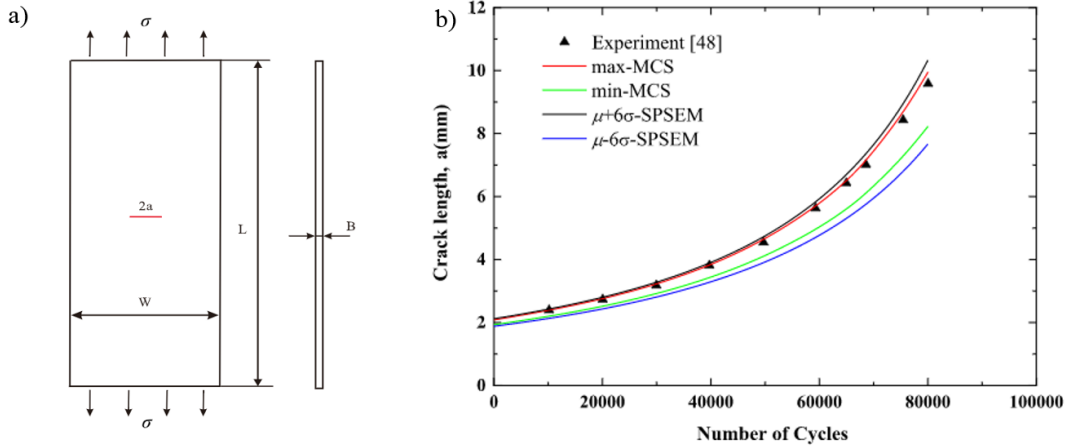


Figure 2.30 (a) Central crack configuration, where W , L , B , $2a$ and σ are the width, length, thickness, initial crack length and applied load of the sample, (b) crack length with respect to the number of cycles for the result regions of MCS and SPSEM. [157]

Existing stochastic modeling methods have shown excellent accuracy in crack modeling for standard samples. For completing the perfect model with the variability of input parameters, these advanced stochastic modeling methods could be applied in the underfill delamination and cracking problems.

2.5 Summary

This chapter presents a literature review on underfill failure in flip-chip assemblies. The flip-chip package, underfill process and material system were first introduced [7, 24]. Five underfill failure modes resulting from reliability tests were identified including 1) delaminations from the sidewalls [34, 37], 2) delaminations from the kerf areas [38], 3) crack propagation in the underfill toward the substrate [34, 39], 4) crack propagation toward the external underfill fillet [34, 40], 5) crack propagation in the chip circuitry [41–43]. After discussing the mechanism of each failure mode, the stress in the underfill, especially at the chip corners and crack tips, was determined as a key metric for all five failure modes [34, 37]. The chip-underfill interfacial adhesion and underfill bulk fracture toughness are other key metrics for delamination and cracks, respectively [26, 47]. Interfacial adhesion can be measured by cantilever beam tests [74–76] and bulk fracture toughness can be measured by bending tests of notched samples [68–70].

Analytically, the stress component near a bimaterial corner follows a power law $\sigma_i \propto \frac{1}{r^{1-\lambda}}$ with respect to the distance to the corner r , and tends to an unbounded value as $r \rightarrow 0$,

which is a stress singularity [56]. λ is the order of singularity valued from 0 to 1 [57], and can be estimated reliably for linear elastic models [62]. A crack tip is a special case of the bimaterial corner when the angle of one material in the bimaterial corner tends to 0 and the elastic modulus of that material is lower than that of the other material. The order of singularity at a crack tip is equal to 0.5 in both the 2D and 3D configurations [62]. The bimaterial corner and crack tip singularity values could be used to validate some of the stress or strain fields near the underfill corner and crack tip obtained in the experiments and simulations. But the real situations are more complex due to the chip corner and underfill material characteristics (as shown in Table 1.6), which were not considered in analytical models.

In addition to the analytical solutions, experimental measurements of underfill strains have attracted the interest of researchers, because accurately measured strains allow researchers to understand the true strain distribution in the underfill and to validate the finite element models. Some techniques, such as CNT strain sensors [55, 79] and cross-sectional DIC [92], have been used to measure the underfill strain distribution. They have limitations in terms of accuracy and boundary conditions, respectively. High-resolution microscopy (LSCM and micro-CT) [87–89, 91] combined with optical strain measurement techniques (DIC and DVC) [81, 83–86] show great potential for *in-situ* underfill strain measurements. In Chapter 3, a confocal-DIC technique will be described to achieve the *in-situ* measurements of the underfill strains at low filler densities.

For numerical simulations, the underfill failure has not been sufficiently studied in the literature because of the complexity of underfill reliability modeling at the chip corner described in Table 1.6. We have reviewed the numerical methods related to the modeling of underfill failure, including the FEM for underfill stress and strain calculations [57, 75, 98–102], the XFEM for crack modeling [113–118], the VCCT and CZM methods for delamination modeling [52, 121, 127, 130, 131], Paris' law for the growth of cracks and delaminations [132, 135–140], fracture mechanisms in particle-matrix systems [146–149] and stochastic modeling methods with uncertainties on the geometrical and material properties [156–158]. One common limitation of all these methods is that the model-obtained underfill stresses, strains, delamination areas and crack trajectories were not fully validated experimentally. Then, in numerical studies, the complexity of underfill reliability models at the chip corner could be determined based on Table 1.6 by the chip characteristics, underfill material characteristics, chip-underfill interface situations and underfill crack

locations. For the chip characteristic, the chip corners were considered as perfectly sharp with orthogonal planes, and the effect of the corner radius and angles between the sidewalls and bottom surface of the die on the underfill strains have not been investigated [98–102]. This corresponds to the level 1 of the chip characteristic (isotropic, pyramid corner). For the underfill material characteristic, the chip-underfill interfacial stresses were studied with the filler settling effect [7, 104], but the underfill was still modelled as homogeneous in the underfill fracture modeling [127–129], corresponding to the level 1 of the underfill material characteristic. For underfill fracture modeling, XFEM has never been used to model cracks in the underfill, but could be a powerful tool because it does not require predefining the crack paths and updating the mesh near crack tips [115]. This corresponds to the level 1 of the underfill crack location (no cracks). The growth of chip-underfill delamination was simulated by the VCCT with Paris’ law [132]. However, the delamination model did not have underfill fillets, leading to different boundary conditions at the chip corner regions compared to a real flip-chip package, and the model-obtained delamination areas were not experimentally validated. This corresponds to the level 2 of the chip-underfill interface situation (delamination on flat interfaces). In addition, fracture mechanisms in particle-matrix systems and stochastic modeling methods may be promising for optimizing the underfill reliability models in terms of the crack paths at the micron scale and the variability of input parameters (for high levels of the chip and underfill material characteristics), but they have not been studied in the literature so far. Herein, in Chapter 4, XFEM will be applied to model the underfill cracks, and the model-obtained strains near the crack tips will be validated by the confocal-DIC-measured results. Chapter 5 will focus on the modeling of the underfill delamination growth and the underfill crack trajectories under thermal cycling, and compare the model-obtained initial moment of delamination, delamination areas and crack paths with C-SAM and cross-sectioning results of the samples after DTC tests.

CHAPTER 3

Using Confocal Microscopy and Digital Image Correlation to Measure Local Strains Around a Chip Corner and a Crack Front

3.1 Avant-propos

Auteurs et affiliation:

Y. Yang: Étudiant au doctorat, Université de Sherbrooke, Faculté de génie, Département de génie mécanique.

P. M. Souare: Professionnel de recherche, Université de Sherbrooke, Faculté de génie, Département de génie mécanique.

J. Sylvestre: Professeur, Université de Sherbrooke, Faculté de génie, Département de génie mécanique.

Date d'acceptation: 13 décembre 2019

État de l'acceptation: version finale publiée

Revue: IEEE Transactions on Device and Materials Reliability

Référence: [Y. Yang, P. M. Souare and J. Sylvestre, "Using Confocal Microscopy and Digital Image Correlation to Measure Local Strains Around a Chip Corner and a Crack Front," in IEEE Transactions on Device and Materials Reliability, vol. 20, no. 1, pp. 97-105, March 2020.]

Titre anglais: Using Confocal Microscopy and Digital Image Correlation to Measure Local Strains Around a Chip Corner and a Crack Front

Titre français: Utilisation de la microscopie confocale et de la corrélation d'images numériques pour mesurer les déformations locales autour d'un coin de puce et d'un front de fissure

Contribution au document: Cet article présente la méthode confocale-DIC pour mesurer la déformation locale dans la résine époxy avec des particules de remplissage Al_2O_3 . Il contribue à la thèse en répondant au premier objectif de ce projet de recherche, à savoir valider la possibilité de mesurer des déformations locales sans détruire le composant. Ce

travail a permis de déterminer les déformations de l'underfill à proximité du coin de la puce. La différence des déformations au coin entre la simulation et l'expérimentation est inférieure à 5%.

Dans cet article, j'ai fabriqué tous les échantillons d'essai, réalisé et validé le protocole expérimental, développé les modèles numériques et analysé les résultats expérimentaux et numériques.

3.2 Résumé

Dans une encapsulation de flip-chip, les régions du coin de puce qui sont intégrées dans le matériau de l'underfill sont souvent critiques pour le déclenchement des dommages, car une concentration de contraintes existe généralement à ces endroits. Un niveau élevé de concentration de contraintes favorise souvent l'initiation des fissures à partir du coin d'une puce. Afin de mieux comprendre la déformation locale autour des coins de puce et des fronts de fissure, une méthode basée sur la microscopie confocale à balayage laser combinée à la corrélation d'images numériques (confocal-DIC) a été développée pour mesurer la déformation locale directement dans des objets transparents et déformés. Une résine époxy transparente avec des charges de particules d'alumine a été utilisée dans quatre types d'échantillons différents, qui ont été fabriqués dans le but de validation. Un échantillon sans contraintes et un échantillon en couche mince ont été utilisés pour vérifier respectivement la dilatation thermique isotrope et les gradients de déformation par rapport à la profondeur. Les résultats des deux échantillons étaient en bon accord avec le calcul à partir du coefficient de dilatation thermique (CTE) et des simulations des éléments finis. En outre, la technique confocale-DIC a été appliquée pour mesurer la distribution de déformation près de la zone du coin de puce d'un troisième échantillon reproduisant la géométrie d'une encapsulation de flip-chip. La déformation principale maximale mesurée était située au coin de la puce, atteignant 0,9% à 60°C, en bon accord avec les résultats de la simulation. La déformation devant le front de fissure a également été évaluée par un essai de flexion en trois points dans un quatrième échantillon. La déformation maximale mesurée était de $5,8 \pm 0,7\%$, ce qui correspond à une erreur relative de seulement environ 5% par rapport aux simulations pour une configuration de pointe de fissure ronde. L'effet de moyenne utilisée dans la DIC abaisse sa résolution spatiale et rend difficile la capture de gradients de déformation plus élevés dans des petites régions. Cependant, l'approche confocale-DIC semble être en mesure de fournir des résultats raisonnables pour évaluer la déformation maximale et la distribution de déformation en plein champ dans des volumes tridimensionnels avec des géométries, des matériaux et des dimensions qui sont très similaires à ceux des encapsulations de flip-chip.

3.3 Abstract

In a flip chip package, the chip corner areas which are embedded in the underfill material are often critical to the damage initiation, since a stress concentration usually exists at these locations. A high level of stress concentration often promotes crack initiation from the chip corner. In order to better understand the local deformation around chip corners and crack tips, a method based on laser scanning confocal microscopy combined with the digital image correlation (confocal-DIC) was developed to measure local strain directly in deformed, transparent objects. A transparent epoxy resin with alumina particle fillers was used in four different types of samples, which were fabricated for the purpose of validation. A non-constrained sample and a thin-layer sample were used to verify the isotropic thermal expansion and the strain gradients with respect to the depth, respectively. Results from both samples were in good agreements with the calculation from the coefficient of thermal expansion (CTE) and FEM simulations. Furthermore, the confocal-DIC technique was applied to measure the strain distribution near the chip corner area of a third sample replicating the geometry of a flip chip package. The measured maximum first principal strain was located at the chip corner, reaching 0.9% at 60°C, in a good agreement with the simulation results. The strain in front of the crack tip was also evaluated by a three-point bending test in a fourth test sample. The measured maximum strain was $5.8 \pm 0.7\%$, corresponding to a relative error of only about 5% compared to simulations for a round crack tip configuration. The averaging used in DIC lowers its spatial resolution and makes it difficult to capture higher strain gradients in small regions. However, the confocal-DIC approach appears to be able to provide reasonable results for evaluating the maximum strain and the full field strain distribution in tri-dimensional volumes with geometries, materials and dimensions which are very similar to those of actual flip chip microelectronic packages.

3.4 Introduction

High performance polymers and polymer-based composites are widely used in microelectronic packaging to enhance the reliability of the devices. An appropriate management of stress and strain in microelectronic packaging is quite important, as the high level of stress often induces mechanical or electrical failures [79]. In flip-chip packages, the large mismatch in the coefficient of thermal expansion (CTE) between the silicon die and the organic substrate induces high stress levels, which are exacerbated by concentrations at interfaces and die corners, from which the underfill damage often originates [34]. Many of the reliability failures in flip-chip packages result from delaminations or cracks in the underfill material, which is applied between the die and the substrate to alleviate the effect of the aforementioned CTE mismatches on the solder joints [5]. Several types of underfill failure modes, such as the interface delamination and cracking, are observed in accelerated temperature cycling tests [37, 39]. The cracks in the underfill may not initially cause an electrical failure, but may propagate over time into the solder joints and the die back end of line (BEOL), thus resulting in device failure [52]. Macroscopic fracture properties, such as the fracture toughness, adhesion strength and the critical energy release rate at the Si/polymer interface, can be experimentally measured, e.g. via the cantilever beam test [26, 40, 75]. Although these fracture properties can be applied as input parameters to models to evaluate the reliability of the package, it is still challenging to predict the lifetime of the devices due to the difficulties involved in estimating correctly the local stress or strain levels at some critical positions, such as the die corner, the solder joints and the BEOL.

Numerical simulations, such as those based on the finite element method, are a popular way to predict the stress levels at critical locations within the package [57, 58, 159]. Reference [64] has studied the singularity of the right angle geometry of the chip corner using two-dimensional fracture mechanics. In the case of quasi-static loading, the order of the singularity is only dependent on the elasticity constants of the two materials. Reference [30] has evaluated the interface shear stress considering the height and width of the underfill fillet, using the finite element method. In the experimental validations, no failures were observed to 3000 cycles (0°C to 100°C, 2 cycles per hour), with fillet heights at the die corner varied from 2% to 70% of the die thickness. The microelectronic packaging community relies on numerical simulations to predict stresses and strains that develop within package structures. However, numerical models do not always provide enough accuracy due to approximations on geometries, materials properties, etc. Considering the chip dicing process, the real die corner is not a perfect cube and its geometry is hard to

model precisely. The dicing might provide a rough surface on the sidewalls, and the chip faces might not form a perfect 90° right angle [29, 160]. In addition, the underfill usually consists of inorganic particle fillers added to a resin to improve its mechanical properties. Due to the variability of filler sizes, contents and curing process, the underfill is not perfectly uniform on a scale of a few tens of micrometers, and may exhibit the separation of fillers and resin [7] and cavities [75]. The finite element method itself also has limitations on calculating the stress at the singularity point, with results that are not convergent when reducing the element size [60]. The above restrictions remain a significant obstacle to obtaining the correct stress and strain value near the chip corner, thus increasing the difficulty of fatigue predictions.

Direct measurements of strain in the underfill would be useful to validate existing physical models or to develop new models to improve the accuracy of numerical simulations. The local deformation of the underfill around the die corner is challenging to measure experimentally, since the relevant area is small ($< 1 \text{ mm}^3$) and the pyramid corner is totally hidden inside the underfill and is not directly accessible. Several experimental techniques have been proposed to measure the strain at small scales in the underfill. Carbon nanotubes (CNTs) can be a good strain sensor, because their Raman shift responds linearly to imposed strains [77, 161, 162]. Reference [55] has dispersed single-wall carbon nanotubes (SWCNTs) in the underfill to measure the internal strains. However, this approach as presented works only in two dimensions, and the position of the measured maximum strain appeared to be quite random and not located at the chip corner, thus raising questions about the validity of the method. Other 2-dimensional methods, such as moiré interferometry and conventional digital image correlation, can only provide deformations on the exterior surface of the underfill [55, 163, 164]. Scanning acoustic microscopy is able to detect the voids and delaminations inside the underfill, but does not have sufficient resolution to provide information about strains [165–167]. In order to obtain the global distribution of strains inside an assembly, displacements in three dimensions must be estimated. Unlike 2-dimensional strain mapping, the 3-dimensional microscale strain field is more difficult to obtain by strain sensors or conventional optical microscopy. An X-ray micro-computed tomography (Micro-CT) has been applied in 3-D reconstruction on metallic components, while the digital volume correlation method (DVC) was used to calculate their volumic deformations [168–170]. However, due to the rotational scanning configuration of the micro-CT, the spatial resolution is limited by the size of the assembly, which makes it difficult to realize high-resolution imaging on a large sample. As an example, the typical voxel sensitivity of micro-CT in reference [168] is $157 \times 157 \times 157 \text{ }\mu\text{m}^3$ for a silicone soft material sample with a dimension of $20 \times 10 \times 3 \text{ mm}^3$. References [87, 171] describe an

optical scanning tomography method to obtain 3D images by using a laser plane, with a spatial resolution reaching $60 \times 60 \times 60 \mu\text{m}^3$ per voxel. Due to their limited spatial resolution, these methods are not appropriate to capture the deformation gradient in the underfill precisely, especially near the chip corner area and in front of the possible cracks.

Laser scanning confocal microscopy (LSCM) avoids some of the drawbacks of other 3D methods, as it scans the sample from one side by controlling the position of the focal plane and can provide high resolution images of volumes. Reference [91] has combined the LSCM and DVC methods to measure large strains (up to 25%) in agarose gels (with typical sample dimensions of 6.4 mm in diameter and 1.4 mm in height). The DVC requires well-structured voxels, while the underfill is a fairly thin layer (tens of micrometers). According to the geometry of voxels used in reference [87, 91, 171], only one or two voxels could be constructed along the layer thickness in an underfill layer, which would translate into a low vertical resolution. Conventional 2-dimensional DIC is simpler to apply on such thin layers, by choosing enough slices when the sample warpage is negligible.

In this paper, we report on the development of an experimental approach to measure the local strain distribution inside a quasi-transparent material for the geometry of a flip-chip corner and a sample with a prefabricated crack. LSCM is combined with digital image correlation (DIC) to produce a method (confocal-DIC) which was used for strain measurements with excellent strain sensitivity (around 0.01%) and spatial resolution ($37 \times 37 \times 3 \mu\text{m}^3$) in a small volume ($1200 \times 1200 \times 60 \mu\text{m}^3$). Section 3.5 presents the procedure for sample preparation and the measurement protocol. Section 3.6 provides the details of finite element models used to confront the experimental results. The results of the comparison to the models and applications of the confocal-DIC method are discussed in section 3.7.

3.5 Experiments

3.5.1 Setup

In order to realize the characterization of local strain inside the materials, laser scanning confocal microscopy was applied in this study. Conventional optical microscopes collect visible light from a large fraction of the sample volume, and cannot separate the image at the focal plane from images at other out-of-focus planes. However, the LSCM uses a pinhole in front of the detector to block the incoming light from the volume outside of a thin focal plane region. Figure 3.1a shows the general principle of the LSCM, including the step of illuminating (left) and light collection (right). During the illuminating step, the laser is reflected by the dichroic mirror and focused on the sample. Then, the reflected

lights goes through the dichroic mirror and is directed toward the detector. Due to the finite focal depth of the objective lens and the angular selection of light rays by the pinhole, only the light from a shallow region around the focal plane can reach the detector. By controlling the vertical position of the sample, a series of sliced images can be produced and stacked vertically. Figure 3.1b displays a typical stacked image obtained by the LSCM (Olympus FV3000, laser at 640 nm wavelength, 10× UPlanSApo objective), with particle fillers dispersed in the epoxy resin as position markers (fabrication details below).

The image processing procedure used to obtain a estimate of planar strain in each slice of the stacked image is shown in Figure 3.1c. After obtaining two stacks of images, before (L0) and after (L1) applying the load, the same layer in each stack is selected and the calculation parameters are initialized. Then, the 2D displacement array is obtained by comparing the images from the two stacks using a digital image correlation algorithm, and the strain values are finally calculated from the displacement array. Herein, this technique, which combines the features of confocal microscopy and digital image correlation method, is called the confocal-DIC method.

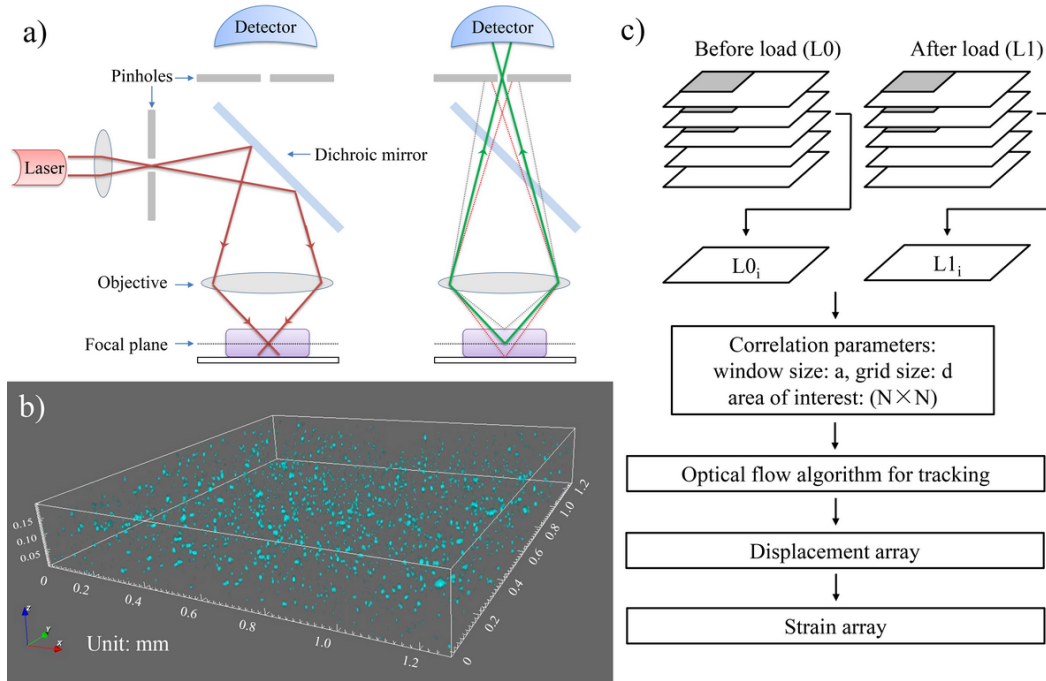


Figure 3.1 (a) General principle of the laser scanning confocal microscopy; left: incident laser illuminating the sample, right: pinhole accepting the reflection from the focal plane, thus rejecting most out-of-focus light. (b) Typical 3-dimensional stacked image, with particle fillers dispersed in epoxy resin. (c) Diagram of the image processing.

3.5.2 Materials and Samples

The underfill material used in this work was composed of the SU-8 2005 epoxy resin, which was loaded with particle fillers consisting of alumina powder ($1\ \mu\text{m}$ in diameter). The SU-8 2005 epoxy is thermally and chemically stable and it has an excellent optical transparency when the light wavelength is above $500\ \text{nm}$ [172]. The nominal Young's modulus and coefficient of thermal expansion of unloaded SU-8 2005 are $2\ \text{GPa}$ and $52 \times 10^{-6}/^\circ\text{C}$, respectively [173]. Before curing the epoxy, about $0.1\ \text{wt}\%$ alumina particle fillers were ultrasonically dispersed in the epoxy to ensure a good distribution of the particles as position markers. The concentration of fillers should be low to avoid the occlusion of fillers by other fillers above, and to avoid modifying the mechanical properties of the epoxy too much. It must however be appropriately high to allow an accurate strain calculation during the image processing.

Four types of specimens were prepared as illustrated in Figure 3.2. The first sample was used to validate the thermal expansion deformation. The mixed resin and fillers were formed on a silicone substrate, so it could be removed from the substrate easily (c.f. Figure 3.2a). It was placed on the microscope stage directly, without any boundary limitations. The second sample was designed to verify the capability of the method to characterize the strain gradient along the thickness of the sample. The epoxy mixture was coated on a transparent glass substrate, with a thickness that was carefully controlled at $0.1\ \text{mm}$ by grinding and polishing (c.f. Figure 3.2b). Both of these two samples were imaged at 24°C , 36°C , 48°C and 60°C , over a $1.2 \times 1.2\ \text{mm}^2$ area of interest. A thermocouple was also used to monitor the temperature on the sample, as the air convection usually caused heat dissipation on the surface.

The third sample in Figure 3.2c was used to measure the deformation near the chip corner area. A rectangular silicon die was encapsulated on a glass substrate by the same epoxy mixture, so that it provided a right angle boundary to the epoxy. The epoxy mixture played a role similar to the underfill in a flip-chip package, with the fillet width chosen to be large (about $3\ \text{mm}$) to avoid the effects of the free surface. The sample was cured at 170°C for 20 minutes and then cooled down slowly on a hotplate. This sample was imaged at 24°C and 60°C to obtain the local deformation near the chip corner (24°C was used as the reference temperature).

The fourth sample in Figure 3.2d was used to characterize the deformation near a crack tip, which had a greater strain concentration than the right angle geometry. For the purpose of having a perfect surface on the sample, a high temperature tape was placed inside a rectangular aluminum mould ($20 \times 10 \times 2\ \text{mm}^3$) during the epoxy curing. The

aluminum mould was dissolved in a HCl solution and the tape was easily removed manually. A pre-crack, 2 mm in length, was produced in the centre of the long edge by a sharp blade. Referring to the standard ASTM E1820 [68], the whole sample was loaded in a 3-point bending test fixture, and the displacement of the loading point (about 0.2 mm) was measured by an optical microscope. Although the area near the indenter imposing the displacement at the loading point may present a large stress gradient, the crack position is far away enough from the indenter, the finite element simulations show that its influence on the stress distribution near the crack can be neglected.

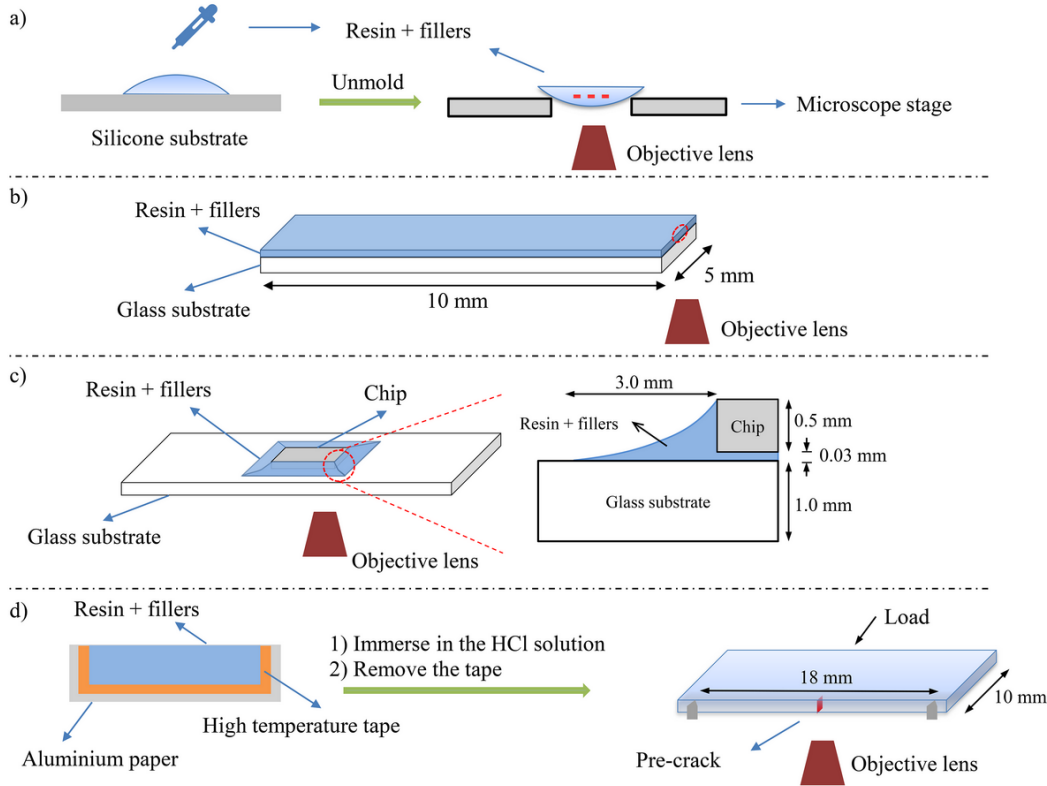


Figure 3.2 Diagrams of the samples preparation: (a) non-constrained sample, (b) thin-layer sample, (c) chip-corner sample and its cross-section view, (d) 3-point bending sample with a prefabricated crack.

As described in Figure 3.1c, we obtained two series of stacked LSCM images from the same region in each sample (before loading and after loading). A global vertical alignment was accomplished by carefully comparing their patterns of speckles in order to choose the photos from the same vertical position. The pixel size in the LSCM images was $2.5 \times 2.5 \mu\text{m}^2$. A Python-based DIC script was used with a correlation window (subtile) of $50 \times 50 \text{ pixel}^2$ and a grid size of $15 \times 15 \text{ pixel}^2$ [174]. The DIC script firstly tracked the displacement of each subtile (in two dimensions) and then calculated the strain component x , y and xy from the central difference of displacements in four grid points. After obtaining

the displacement and strain array of each layer, the strain contours were stacked to form volumetric representations of the strain fields. Currently, we did not apply the DVC to calculate the full 3-dimensional deformation, but might develop it in the future. In this work, for the first three configurations (non-constrained, thin-layer and chip corner samples), we fabricated 3 samples for each configuration and tested 3 times for each sample. For the last 3-point bending configuration, we fabricated 1 sample and performed 3 tests.

3.6 Modeling

Of the four samples, only the deformation in the first non-constrained sample could be easily calculated analytically from the CTE due to the complexity of the geometries. Thus, the finite element method was used to compare the results between the experiments and theoretical expectations, for the last three samples. The finite element models are shown in Figure 3.3, using the same geometry as the samples and material properties as described in Table 3.1. As is common practice in this field, the mechanical properties of silicon were simplified as isotropic, since the Young's modulus of the underfill is significantly lower than the modulus of the silicon, so the anisotropic nature of silicon has only a small influence on the deformation of underfill. As mentioned in the reference [175], the crystal structure of silicon has cubic symmetry, so calculations for devices with orthogonal shapes and loads will be reasonably accurate. Several researchers [106, 176] also chose one single elasticity value for the silicon die. As the loading temperatures did not exceed 60°C, only the material properties of the underfill under the T_g were used. To create the parametric numerical models efficiently, a custom software was used, PACK [177]. PACK is a Python-based high performance numerical software, incorporating advanced pre- and post-processing features for multiple commercial finite element softwares (including Ansys APDL used in this work) [178]. The chip-corner models were generated by PACK (cf. Figure 3.3b), with two sizes of underfill elements (40 μm and 24 μm) used to study how to best capture the corner strain concentration. A quarter simplification was used for the thin-layer model and chip-corner model, while a x-symmetric and y-symmetric boundary condition were applied on the yz and xz plane. A fixed constraint was also applied on the node at (0,0,0) to avoid rigid body motion. In order to correctly calculate the deformation, the reference temperature was set at 24°C, in accordance with the experimental measurements. In the 3-point bending model (cf. Figure 3.3c), two types of crack front (round and triangular) were also used, since the real crack front produced by the blade is possibly between these two ideal geometries.

In Figure 3.3a and 3.3b, we used 8-node solid elements for most components, while the underfill fillet was modeled by prisms and tetrahedral elements due to the complex ge-

Table 3.1 Material properties in models.

	Die	Underfill	Substrate
Young's modulus (GPa)	120	2 (below T_g) 0.5 (above T_g)	82
CTE (ppm/°C)	2.6	52 (below T_g) 298 (above T_g)	7.1
T_g (°C)		120	
Poisson ratio	0.35	0.3	0.2

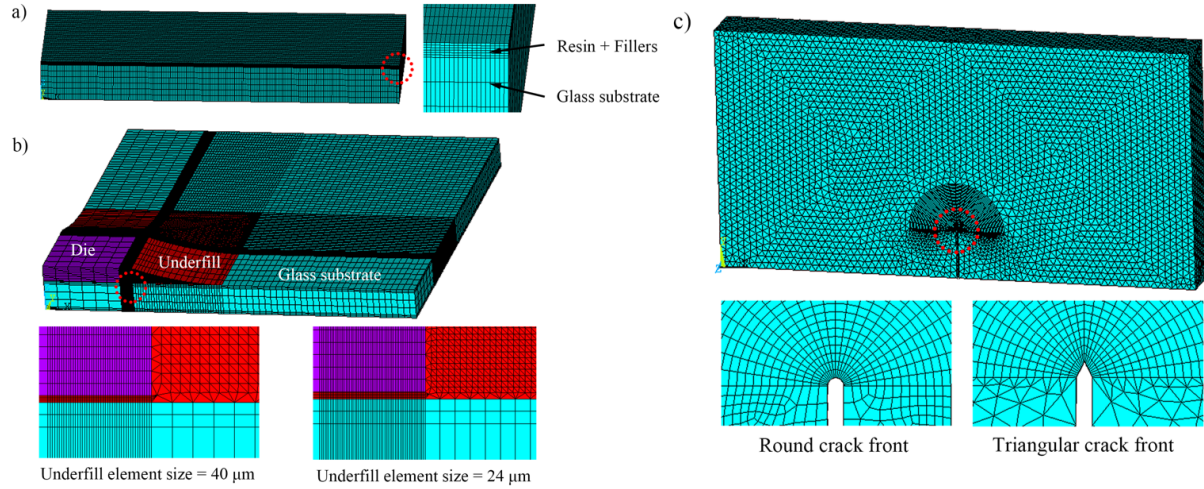


Figure 3.3 Finite element models of the (a) thin-layer sample, (b) chip-corner sample, (c) 3-point bending sample, with a round and a triangular crack front geometry.

ometry. Parabolic 20-node solid elements were used to build the crack models for more accurate strain evaluation near the crack tip. Uniform temperatures were applied on the thin-layer and chip-corner models. A 0.2 mm central displacement load was set on the the 3-point bending sample. All the FEM models were solved by the Ansys Sparse solver. We extracted the deformation on the edge of the thin-layer model, the strains along the diagonal direction from the chip corner and along the vertical direction from the crack tip.

3.7 Results and Discussion

3.7.1 Deformation Validation by CTE

The aim of the non-constrained sample and the thin-layer sample was to validate the feasibility of the confocal-DIC method. The shape of the non-constrained sample was entirely defined by the effect of fluid surface tension. This sample was free of restriction on its boundary, so that the strain ϵ_i at each position was controlled by the CTE α of the

bulk material and is expressed by:

$$\epsilon_i = \alpha \Delta T, \quad (3.1)$$

where ΔT is the temperature difference between the two load conditions, and $i_{x,y,xy}$ indicates the components of strain. As described in Figure 3.4a, both the strain components x and y were evaluated by the confocal-DIC method. Each measured point in Figure 3.4a represents the average value and standard deviation calculated over the strain components in a 9-slice stacked image. The measured deformation for components x and y showed a quasi-linear relationship with respect to the temperature of the sample, with a slope comparable to the CTE of the epoxy. The average strains of both the x and y components were in good agreement with the calculations from the CTE at each test temperature, with the maximum relative error reaching 13.5% for the strain component y at 54.6°C. The averaged strain values obtained by a linear fit gave a CTE of $(47.2 \pm 4.5) \times 10^{-6}/^\circ\text{C}$, slightly lower but consistent with the SU-8 2005 expected value of $52.0 \times 10^{-6}/^\circ\text{C}$. Figure 3.4b shows typical images of ϵ_x , ϵ_y and ϵ_{xy} for one layer. ϵ_x and ϵ_y increased with temperature, while ϵ_{xy} was small and independent of temperature.

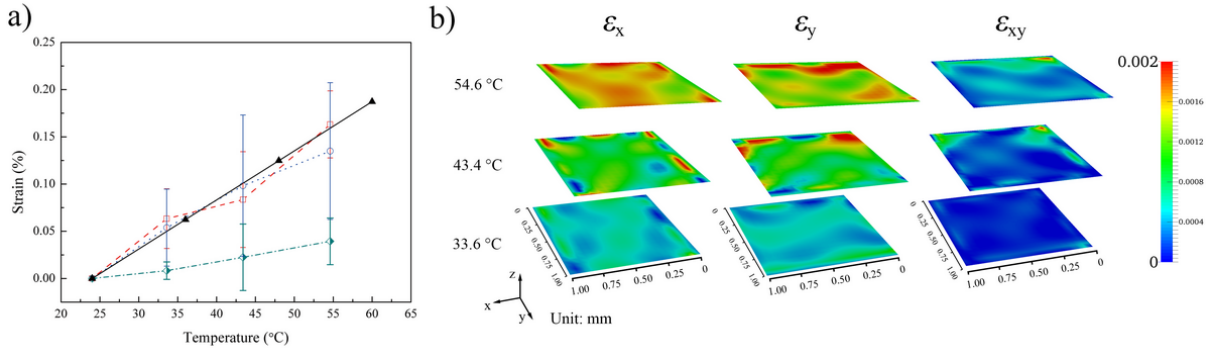


Figure 3.4 (a) Strain components x (dashed line), y (dotted line) and xy (dot-dash line) in the non-constrained sample and the strain calculated from the CTE (solid line), with respect to loading temperatures. Error bars represent one standard deviation. (b) Typical strain images for one layer at 33.6°C, 43.4°C and 54.6°C.

The thin-layer sample was used to verify the measurement of strain gradients with respect to the depth inside the material. Since the glass substrate had a low CTE and a high Young's modulus, the deformation of the epoxy mixture near the bi-material interface was strongly controlled by the glass substrate. Thus, an increase of deformation is expected along a path from the interface to the free edge. Figure 3.5 summarizes the results for strain component x. With increasing temperatures, the strain gradients became more significant in both simulations and experiments. Due to image noises compared to the

small deformation, some data fluctuations are clearly visible, especially near the interface area. However, the global trends of these strain values were in a good agreement with the simulation results. The maximum strain on the component x reached 2.8×10^{-4} , 5.7×10^{-4} and 7.3×10^{-4} at the three measurement temperatures, which shows a good sensitivity for small deformation measurements. Figure 3.5d presents typical strain images of ϵ_x , ϵ_y and ϵ_{xy} at 54.6°C . Although some noise is clearly present, an ϵ_x can still be observed to be increasing along the z direction, while ϵ_y and ϵ_{xy} keep a relatively low level.

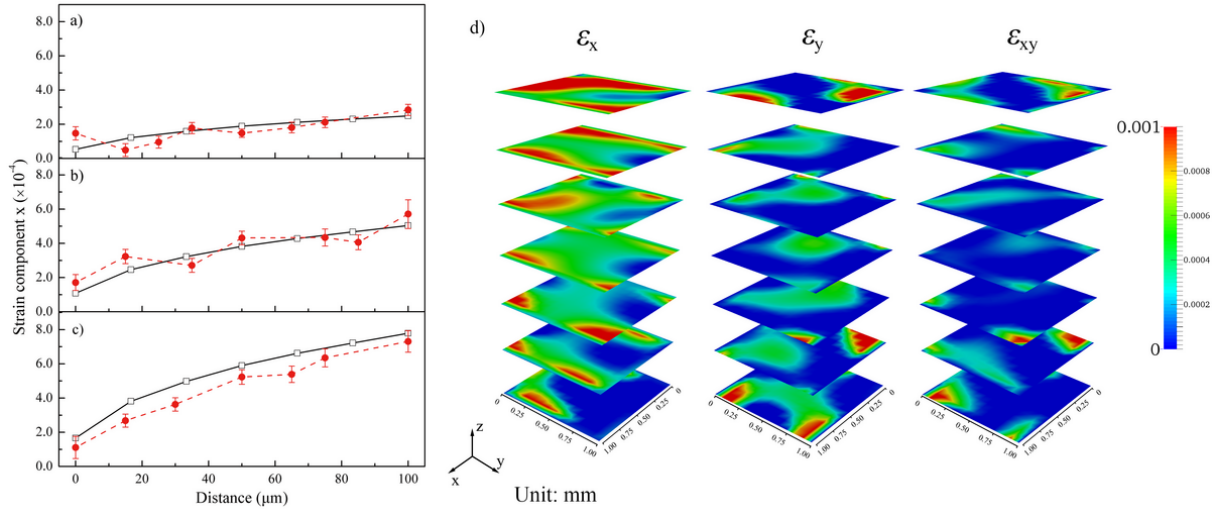


Figure 3.5 Strain component x of the calculation (solid line) and the measurement (dashed line) with respect to vertical distance from the bi-material interface in the thin-layer sample at (a) 33.6°C , (b) 43.4°C and (c) 54.6°C . Error bars represent one standard deviation. (d) Typical strain images at 54.6°C .

3.7.2 Comparison of Underfill Corner Strain between Experimental and Numerical Results

The above two preliminary validation tests show that the confocal-DIC method is capable to measure local deformations at the micrometer scale and to produce reasonable strain estimates. We next apply this method to evaluate the underfill deformation near the chip corner area, as described in Figure 3.2c. Figure 3.6 shows the measured first principal strain in the underfill, with the chip area shown in grey (without considering its deformation). The vertical step (gap between two slices in the image stack) for all the four samples was set as $3 \mu\text{m}$ in order to collect enough information and avoid missing possibly large strain gradients. The 1st to 4th layers from the top represent the area above the chip corner and the 6th to 9th layers were the underfill between the chip and the substrate. The 5th layer from the top was exactly the layer at the corner point. The maximum value of the first principal strain appears at the chip corner area in the 5th layer and reaches

0.9%. On the edge of the sidewall, the maximum value reaches about 0.5%. Although the first principal strains on the 1st to 4th layer were generally lower than on the 5th layer, the in-plane maximum value was still located near the chip corner and the interface regions. From 6th to 9th layers, a broad area reaches 0.5% deformation as a result of the differences of CTE between the silicon die and glass substrate.

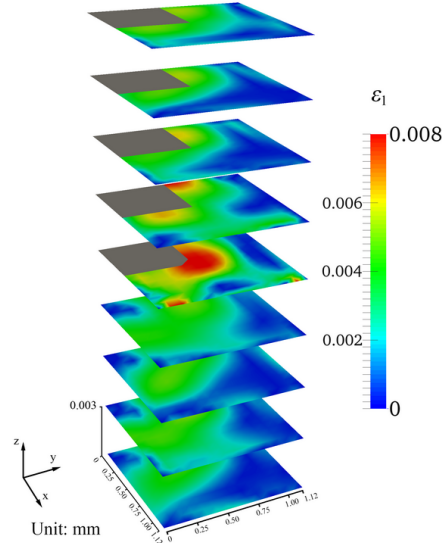


Figure 3.6 3-dimensional stacked images of the first principal strain near the chip corner at 60°C.

In order to further compare the effect of strain concentration between the simulations and experiments, Figure 3.7 shows the first principal strain along the diagonal direction from the chip corner. Considering the singularity effect on the right angle area, the strain concentration was steeper in simulation results than in experiments. Smaller elements were also better able to capture the local strain gradient. The maximum strain in the model with 24 μm and 40 μm elements sizes reached 1.16% and 1.10% respectively, while the measured maximum strain was 0.92%. The measured value was about 20% lower than the simulation, since the real chip corner was not a perfect pyramid (e.g. due to imperfect dicing of the die). When the position is 50 μm away from the strain concentration area, all the three values remain at a similar, low strain level (0.1-0.2%). When the element size is refined, we observed higher principal strains at the chip corner. This is due to the singularity effect at the corner of the chip. For the confocal-CID results, the high deformation gradient near the chip corner (from 0 to 25 μm) could be further improved by an investigation of the DIC algorithms. At this point, the strain values obtained by the model for the small feature size (dashed line) matched the confocal-DCI measurements better than those of the large feature size (dotted line) of 25 to 100 μm .

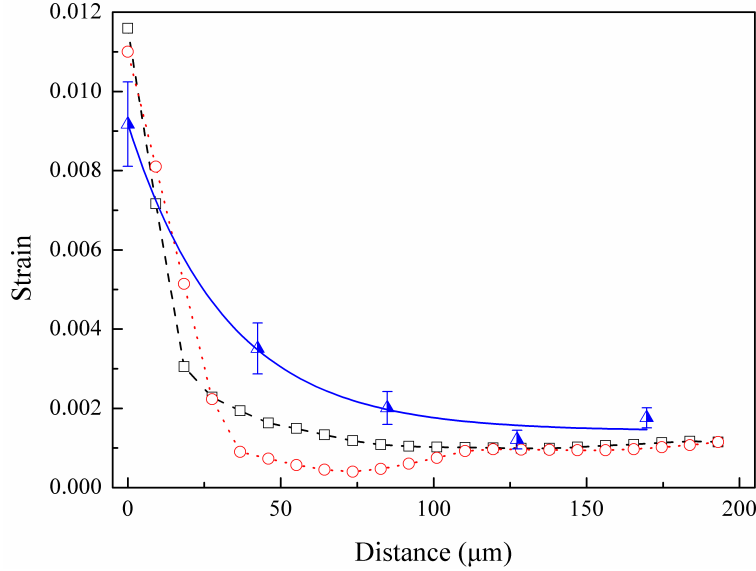


Figure 3.7 First principal strain at 60°C as a function of the distance from the chip corner in the diagonal direction, for the calculation with an element size of 24 μm (dashed line) and 40 μm (dotted line), and the measurements (triangle markers) with an exponential fitting curve (solid line). Error bars represent one standard deviation.

3.7.3 Comparison of Crack Tip Strain between Experimental and Numerical Results

As the chip corner is often subjected to high strain levels, many reliability tests have found that cracks might initiate from the chip corner and then propagate into the underfill and the back end of line (BEOL). Thus, we have also tried to characterize the strain distribution in front of a single crack by the 3-point bending test, as described in Figure 3.2d. The central displacement load was 0.2 mm, measured by an optical microscope. Figure 3.8 shows the measured strain contours near the crack front area on the component x, y and the first principal strain. Since the central load was along the y direction, the mode I crack was dominant, which means that the tensile stress was normal to the crack plane yz. The strain component x (Figure 3.8a) showed a significant concentration near the crack front area (the right edge of images), while the strain component y (Figure 3.8b) was generally low, indicating the same situation of mode I crack. Here we still use the first principal strain to evaluate the global strain level in the crack front area (Figure 3.8c). A high level of strain concentration can be observed from the right edge of the images.

In order to compare the results between the experiments and simulations, Figure 3.9 summarizes the relationship between the maximum first principal strain and the element size for round and triangular crack tip configuration in the FEM simulation. Since the

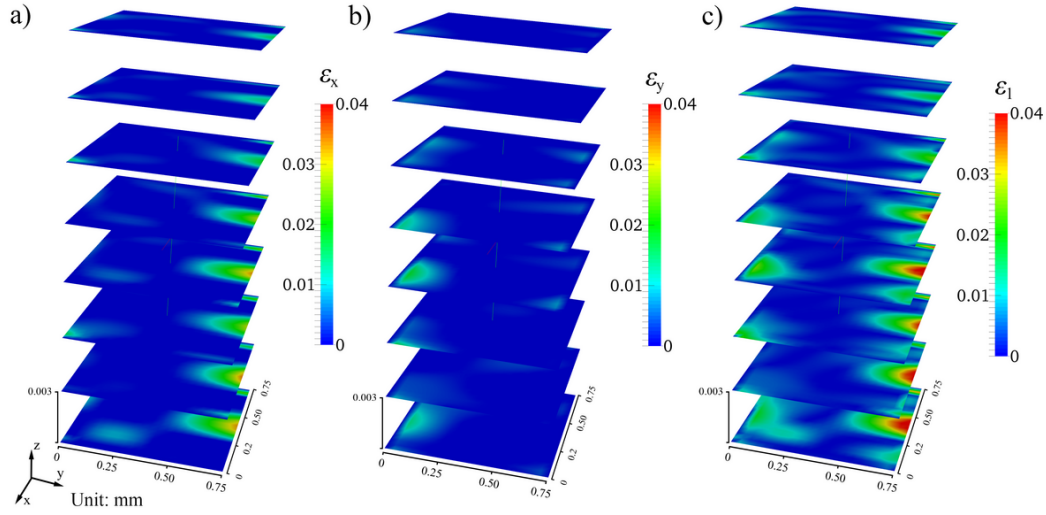


Figure 3.8 3-dimensional stacked images of the (a) strain component x , (b) strain component y , (c) first principal strain in front of the crack area.

real crack tip is not a sharp angle but has a small radius, these two configurations were analyzed, representing two types of ideal geometry of the crack tip. Due to the singularity effect, the strain at the triangular crack tip increased rapidly and became non-convergent when the element size was less than $40\text{ }\mu\text{m}$. However, the strain at the round crack tip was generally stable. Here we chose the results of the element size at $35\text{ }\mu\text{m}$ for further comparison with the experiments, to have a similar resolution as in the DIC calculation ($37 \times 37\text{ }\mu\text{m}$). Figure 3.10 shows the first principal strains along the y direction from the crack front. The triangular tip model had the highest strain level near the crack, reaching 9.2%, while the maximum strain for the round tip model was 6.1%. The experimental data were quite close to the round tip configuration at $5.8 \pm 0.7\%$, only about 5% lower than that in the round tip model. Since the DIC calculates a single strain value for each correlation window, strong deformation gradients near the crack tip are averaged, which is equivalent to a spatial low-pass filter in the data processing. This results in a smoothing of the strain distribution and reduces the slope in high strain gradient areas. Although it is difficult to capture high strain gradients by our method, it is still useful to evaluate the maximum strain level and the general distribution of full strain fields.

3.8 Conclusions

In this work, we have developed a methodology for measuring the local strain inside the underfill material directly. This technique combines the advantages of the laser scanning confocal microscopy and digital image correlation methods, and is able to provide a 3-dimensional stacked strain contours.

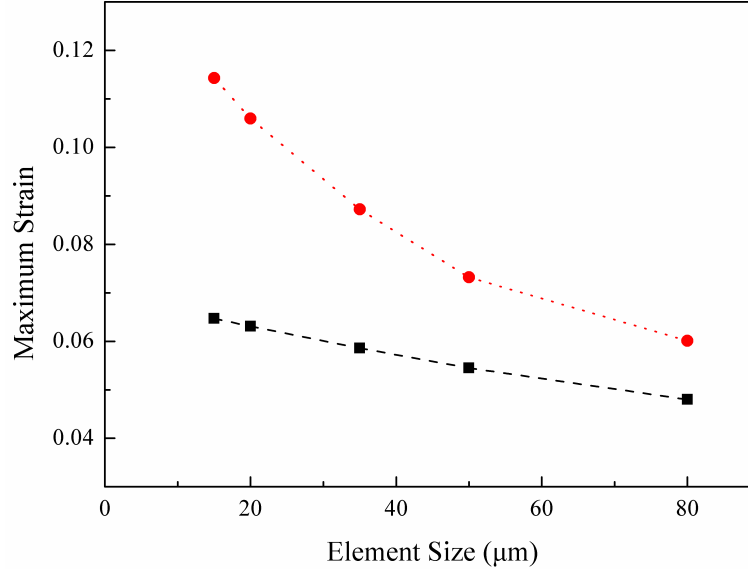


Figure 3.9 Maximum first principal strain at the round crack tip (dashed line) and the triangular crack tip (dotted line) with respect to the element size.

Four types of samples were fabricated for the purpose of validation. A preliminary validation was performed by a non-constrained sample and a thin-layer sample, for the thermal expansion deformation and the strain gradient with respect to the depth in the material. Both the strain components x and y in the non-constrained sample were in a good agreement with the coefficient of thermal expansion (CTE) of the bulk resin. The strain gradients obtained in the thin-layer sample were consistent with the simulation results, as a function of the depth from the resin/glass interface. This demonstrates the usefulness of the confocal-DIC approach in obtaining the internal strain of quasi-transparent materials at the micrometer scale. We applied this approach to measure the strain in the underfill around a chip corner. The first principal strain reached 0.9% at the corner area, which is close to the simulation results. In the 3-point bending test, a higher strain concentration was found in front of the crack tip, while the measured maximum strain was $5.8 \pm 0.7\%$, only about 5% lower than the simulations of the round crack tip configuration.

The confocal-DIC approach seems to have some difficulties to capture very high strain gradients, because of the limitations on resolution and the averaging effect in each correlation window resulting from the DIC calculation. It can nevertheless provide very reasonable results for evaluating the maximum strain and the full field strain distribution in a 3-dimensional stacked view. It is expected that this technique will provide more opportunities to understand the real microscale mechanical behaviour inside materials, thus leading to better reliability estimates for microelectronic devices.

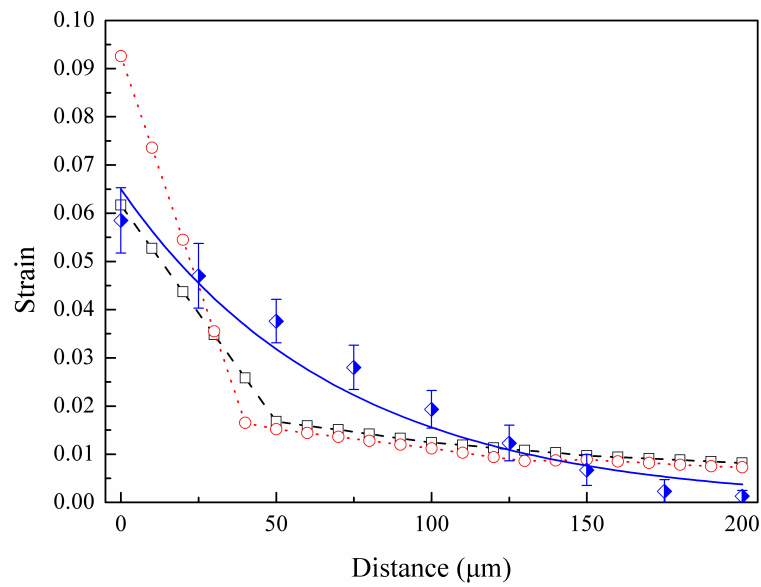


Figure 3.10 First principal strain along the crack front direction in the calculation with a round crack front (dashed line) and a triangular crack front (dotted line), and the measurements (diamond markers) with an exponential fitting curve (solid line). Error bars represent one standard deviation.

CHAPTER 4

Study of Underfill Corner Cracks by the Confocal-DIC and Phantom-Nodes Method

4.1 Avant-propos

Auteurs et affiliation:

Y. Yang: Étudiant au doctorat, Université de Sherbrooke, Faculté de génie, Département de génie mécanique.

M. K. Toure: Professionnel de recherche, Université de Sherbrooke, Faculté de génie, Département de génie mécanique.

P. M. Souare: Ingénieur, IBM Bromont.

E. Duchesne: Ingénieur, IBM Bromont.

J. Sylvestre: Professeur, Université de Sherbrooke, Faculté de génie, Département de génie mécanique.

Date d'acceptation: 12 novembre 2021

État de l'acceptation: version finale publiée

Revue: Microelectronics Reliability

Référence: [Y. Yang, M. K. Toure, P. M. Souare, E. Duchesne and J. Sylvestre, "Study of Underfill Corner Cracks by the Confocal-DIC and Phantom-Nodes Method," in Microelectronics Reliability, vol. 128, pp. 114431, 2021.]

Titre anglais: Study of Underfill Corner Cracks by the Confocal-DIC and Phantom-Nodes Method

Titre français: Étude sur la fissure du coin de l'underfill par la méthode de confocal-DIC et les nœuds fantômes

Contribution au document: Cet article présente l'application de la méthode confocale-DIC dans la mesure de la déformation près des fissures de l'underfill et la modélisation de la fissuration de l'underfill par XFEM. Il contribue à la thèse en répondant au deuxième objectif de ce projet de recherche, à savoir le développement du modèle de fissuration des underfills. Ce travail a permis d'améliorer la sélection des paramètres du modèle (taille des

éléments, distribution de la charge de particule et angle de la paroi latérale), en fonction de la déformation mesurée au front de la fissure comme référence.

Dans cet article, j'ai fabriqué tous les échantillons d'essai, effectué les mesures expérimentales, développé les modèles numériques et analysé les résultats expérimentaux et numériques.

4.2 Résumé

Dans une encapsulation de flip-chip, en raison de la géométrie du coin de puce carré pointu et de l'incohérence dans les coefficients de dilatation thermique entre les matériaux de l'assemblage, une concentration de contrainte dans la zone du coin de la puce a souvent un impact important sur la fiabilité en chargement de température cyclique. Les fissures proviennent souvent de cette concentration de contraintes, et peuvent conduire à la défaillance de l'appareil lors de sa propagation dans la puce ou les interconnexions électriques. Afin de mieux comprendre le mécanisme de la fissuration de l'underfill et de prédire le chemin de la fissure, une méthode basée sur la microscopie confocale à balayage laser et la corrélation d'images numériques (confocal-DIC) a été utilisée pour mesurer la déformation locale autour d'une fissure à partir d'un coin de puce. Un échantillon a été fabriqué en collant une puce de silicium ($6 \times 6 \times 0.55 \text{ mm}^3$) à un substrat de quartz ($20 \times 12 \times 0.4 \text{ mm}^3$), dans une configuration similaire à une encapsulation de flip-chip. La résine époxy SU8-2005 mélangée avec une fraction massique de 0,1% en poids de charges de particules d'alumine a été utilisée comme matériau de l'underfill aux fins des mesures. Des fissures initiées naturellement ont été observées vers la direction diagonale lorsque l'échantillon a été soumis à des cycles thermiques de $-18/25^\circ\text{C}$. Des fissures artificielles d'une longueur de $160 \text{ }\mu\text{m}$ and $640 \text{ }\mu\text{m}$ ont été fabriquées à partir du coin de la puce par un laser, vers la direction diagonale de 45° , de la même manière que les fissures initiées naturellement. L'échantillon fissuré artificiellement a été imagé à 25°C et 5°C par un microscope confocal et la distribution des contraintes autour de la fissure a été estimée par un traitement d'image. La déformation maximale circonférentielle et la déformation principale se situaient au front de fissure pour les fissures de $160 \text{ }\mu\text{m}$ and $640 \text{ }\mu\text{m}$. Un modèle numérique a été construit en utilisant la méthode des éléments finis étendus (XFEM) avec l'approche des nœuds fantômes. Lorsque la taille des mailles a été réduite à $16 \text{ }\mu\text{m}$, la déformation circulaire obtenue par simulation à la pointe de la fissure était inférieure de 22.0% et de 9.5% à celle mesurée par confocal-DIC, pour la fissure de $160 \text{ }\mu\text{m}$ et la fissure de $640 \text{ }\mu\text{m}$, respectivement. Cette différence a diminué à 8,2% et 6,3%, respectivement, lorsque la distance était de 50 à $175 \text{ }\mu\text{m}$ de la pointe de la fissure dans la direction diagonale. La distribution de déformation circonférentielle était généralement en accord avec les valeurs mesurées, mais une différence des gradients de déformation a été observée. Un modèle de propagation a été réalisé par la méthode des nœuds fantômes. La fissure partait du coin de la puce et a évolué vers une fissure planaire dans le sens diagonal, ce qui est en bon accord avec les observations expérimentales. Nous concluons que la technique confocale-DIC peut mesurer la distribution des déformations autour de la zone de fissure, et que l'approche du XFEM nœud fantôme peut simuler correctement la croissance de fissures dans l'underfill.

4.3 Abstract

In a flip chip package, due to the sharp square chip corner geometry and the loading from mismatches in the coefficients of thermal expansion between materials in the assembly, a stress concentration in the chip corner area is often thought to greatly impact reliability in thermal cyclic loading. Cracks often originate from this stress concentration, and may lead to the failure of the device when propagating into the chip or electrical connections. In order to better understand the mechanism of underfill cracking and predict the crack path, a method based on laser scanning confocal microscopy and digital image correlation (confocal-DIC) was used to measure the local deformation around a crack from a chip corner. A sample was fabricated by bonding a $6 \times 6 \times 0.55$ mm³ silicon chip to a $20 \times 12 \times 0.4$ mm³ quartz substrate, in a configuration that is similar to a flip-chip package. The SU8-2005 epoxy resin mixed with a mass fraction of 0.1 wt% alumina particle fillers was used as the underfill material for the purpose of measurements. Naturally initiated cracks were observed along the diagonal direction when the sample was subjected to $-18/25^\circ\text{C}$ thermal cycles. Artificial cracks with lengths of 160 μm and 640 μm were fabricated from the chip corner by a laser, along the 45° diagonal direction, similarly to the naturally initiated cracks. The artificially cracked sample was imaged at 25°C and 5°C by a confocal microscope and the strain distribution around the crack was estimated by DIC. The maximum hoop strain and first principal strain were located at the crack front area for both the 160 μm and 640 μm cracks. These data were used to build a numerical model using the extended finite element method (XFEM) with the phantom-nodes approach. When the mesh size was decreased to 16 μm , the hoop strain obtained by simulation at the crack tip was 22.0% and 9.5% lower than that measured by confocal-DIC, for the 160 μm crack and the 640 μm crack, respectively. This difference decreased to 8.2% and 6.3%, respectively, when the distance was from 50 to 175 μm away from the crack tip along the diagonal direction. The distribution of hoop strain was in good agreement with the measured values, when the element size was small enough to capture the strong strain gradient near the crack tip. A propagation model was realized based on the phantom-nodes method. The crack started from the chip corner and evolved into a planar crack along the diagonal direction, which is in good agreement with the experimental observations.

4.4 Introduction

Flip-chip is a popular packaging technique for high-end devices because of its small volume and high input/output capacity [179]. High performance polymers mixed with SiO₂ particle fillers are commonly used as the underfill in flip-chip packages to protect the interconnections and improve the reliability performance. Due to the mismatch in the coefficient of thermal expansion (CTE) between the silicon chip, polymer-based underfill and substrate, a high level of stress often occurs at interfaces, as well as significant warpage of the whole package. The geometry, with chip corners and multiple bi-material interfaces, leads to stress concentrations where the underfill damage often initiates [34]. Based on the JEDEC reliability test standard such as JESD22-A104D [13] for accelerated temperature cycling (ATC) and deep thermal cycling (DTC), several reliability experiments have observed multiple underfill failure modes, including underfill cracking and interface delamination [39, 40]. In spite of its broad industrial relevance, underfill-related failures are still a major issue limiting the reliability of large, high-end flip-chip packages [7, 180]. While the general mechanical loads leading to underfill damage are well understood and easily modelled [39, 181], it is still considered to be extremely challenging to predict by numerical simulations the underfill failure dynamics with a level of precision that is sufficient for industrial applications, as such simulations require the careful consideration of a plethora of important geometrical and material details, that often can only be obtained via the experimental characterization of actual parts [92, 99, 182].

As an example, the exact stress distribution and the underfill cracks trajectory induced by stress concentrations from the chip corner have not yet been fully understood, and it is therefore still challenging to construct from reliability experiments a direct relationship between the early-stage mechanical failure and the late-stage electrical failure. In the published research work on reliability experiments for typical populations of flip chip modules, the delaminations from the sidewalls and from the chip active face appear first, and are generally followed by bulk fractures that continue in the underfill fillet [34, 37, 52, 75]. Some conventional experimental methods are available to characterize the interface adhesion strength and underfill material toughness, such as the cantilever beam (CLB) test [26]. These fracture properties are often used as input parameters in numerical models to estimate the reliability of flip-chip packages, with some clear limitations: in the CLB configuration, there is no stress concentration comparable to what occurs at the chip corner. Due to variations in the filler distribution [7], the interface strength measured by the CLB test might further be different than in a real flip-chip. The presence of the

process-related contaminants and microscale surface characteristics might also be critical to the fracture properties measured from an *ex-situ* configuration [34].

In-situ experimental investigations on the underfill cracks would be valuable to accelerate the development and validation of numerical models that can effectively estimate the reliability of flip-chip packages in thermal cycling. At the small dimensions of the chip corner region ($< 1 \text{ mm}^3$), the measurement of the fracture behavior is challenging for conventional experimental techniques. The lower square corner is fully enclosed in the underfill and cannot be directly accessed. Carbon nanotubes can be good strain sensors, because they are small enough to disperse in the underfill and their Raman shift responds linearly to the imposed strains [77]. In reference [55], single-wall carbon nanotubes were dispersed in the underfill to estimate the internal strains. This approach provided the 2-dimensional strain components in the plane of the chip, by selecting individual nanotubes oriented along the appropriate directions, a somewhat time-consuming process. In another work [87], X-ray micro-computed tomography (micro-CT) was used for 3-dimensional reconstruction of bonding wires and solder joints. The digital volume correlation technique was applied to evaluate their volumetric deformation. However, the contrast of underfill and other polymer components is not great in x-ray images. Metallic particle fillers might be used to improve the contrast, but could affect the mechanical properties of the underfill as well. In addition, it might also be difficult to apply thermal loading in a tomography machine. We have found that laser scanning confocal microscopy (LSCM) avoids some of the above drawbacks and can be a useful tool for observing the chip corner area if the substrate and underfill are quasi-transparent to the laser. From a series of images captured by the confocal microscope, we applied the digital image correlation (DIC) method to estimate the local deformation by inspecting the position of underfill filler particles before and after thermal loading. In our previous work [90, 183, 184], we have validated this approach, which is called the confocal-DIC technique herein. Although the DIC is more often used as a full field method, several studies have successfully applied DIC in crack areas with large strain gradients, to determine the strain distribution [185], stress intensity factors [186] and fracture toughness [164, 187] with good precision. This indicates that DIC could be useful for measuring the underfill crack behaviour.

Numerical simulations are widely used for the stress/strain assessments of flip-chip packages but, as mentioned above, they have not yet reached a sufficient level of sophistication to be useful to predict the reliability of high-end flip chip packages in an industrial context. In many simulations, the calculated maximum stress is generally the key parameter for estimating the reliability before doing costly experimental validations. The finite element

method (FEM) is an effective numerical tool for accurately calculating the critical stress level for most simple structures. Although conventional FEM is widely used in structural and thermal analysis, proper underfill models with fracture can be complicated to generate and mesh by classical FEM, since the accuracy of local stress and strain estimates is highly dependent on the mesh quality [108] and the errors on stress calculations cumulatively influence the direction of the crack growth [188]. As the FEM requires a highly refined mesh near the crack tip area and an update of the mesh after each crack growth increment, it can be time-consuming to apply on parametric models with complicated and varied geometries. The extended finite element method (XFEM) alleviates some of the shortcomings of the FEM in modeling discontinuities [109], such as cracks and delaminations. By adding enriched nodes in the crack-related zone, the XFEM avoids the refinements and updates of the mesh in the vicinity of the crack zone. These advantages of XFEM simplify the model construction and improve the precision of calculation near the crack tip. The XFEM was used to study the cracking problem in the solder joints and interlayer dielectric structures [117, 189], but has not been reported for the modeling of underfill cracks.

In an actual flip-chip package, the underfill usually contains inorganic particle fillers to improve the mechanical properties, so that the underfill is not homogeneous on a scale of a few tens of micrometers, and may have a separation of fillers and resin [7] as well as cavities [75]. Due to the blade dicing process, the shape of chip corners is not perfectly square and the surface is not perfectly flat [29]. The laser grooves can further remelt the chip surface, while the different surface roughness might change the interface strength [28]. The presence of process-related contaminants on the chip surface might reduce the interface adhesion as well [45]. Most current numerical models ignore the above manufacturing effects, while they are often considered to be essential to correctly anticipate the reliability of actual packages [190, 191]. Thus, we posit that an experimental technique that can perform an in-situ strain measurement in the underfill of a flip-chip package could be the basis for developing more complete models of the aforementioned effects, to improve the state-of-the-art for the reliability estimates.

In this paper, we applied the confocal-DIC technique to experimentally measure the local deformation around the crack initiating from the chip corner and use the resulting mechanistic insights to build a numerical model for the underfill crack propagation. As it is difficult to fabricate controlled cracks and perform in-situ strain measurements directly in real flip-chip packages, this work used a test component with a quartz substrate and a transparent underfill with a low density of fillers. This test component had the same

geometry as a real flip-chip package, thus allowing a more complete understanding of the strain distribution around the corner crack. A modeling method for underfill cracking is proposed with XFEM and could be applied to real flip-chip packages by practitioners. Section 4.5 presents the procedure for preparing samples with a specific underfill material and the measurement protocol of the confocal-DIC technique. Section 4.6 presents a numerical model of the same geometry built by XFEM with phantom-nodes. Section 4.7 discusses the comparison of the confocal-DIC and numerical results, as well as the crack growth path.

4.5 Experiments

4.5.1 Samples

In order to reproduce a strain distribution similar to a real flip-chip package, Figure 4.1a and 4.1b show a sample that was fabricated by bonding a square silicon chip (diced by a Disco DAD320 dicing saw) to a rectangular quartz substrate. The dimensions of all components are provided in Table 4.1, and were measured by a vernier caliper with an accuracy of 0.01 mm. The thickness of the underfill was evaluated by subtracting the thickness of the chip and of the substrate from the total thickness of the sample. Alignment marks were drawn in the centre of the chip and of the substrate to estimate the relative position of the two structures. The distance between the centres is estimated to be 0.35 mm at most. According to the variation in the underfill thickness and the distance between the chip edge and the substrate edge, the lack of parallelism between the chip and substrate along any of the three possible rotation axes was estimated to be 1° at most. The SU-8 2005 epoxy was chosen as the resin for the underfill because of its excellent optical transparency at the 640 nm wavelength [172], which was the wavelength of the laser used for imaging. 0.1 wt% of Al_2O_3 particles (1 μm in average diameter) were dispersed in the resin as position markers, with a nominal increase of 0.2% on the mechanical properties of the resin mixture, according to estimates using the rule of mixture with the nominal Young's modulus of Al_2O_3 at 380 GPa. Under an appropriate load, the tiny displacements of these markers were captured and used to calculate the local strain of the underfill. The Young's modulus of cured SU-8 is 2 GPa and its coefficient of thermal expansion is 52 PPM/°C [173]. The sample was cured at 170°C for 20 minutes and then cooled down slowly on a hotplate. The bonding process consists of the following steps: 1) mixing fillers and resins to form the underfill material, 2) dispensing the underfill on the quartz substrate, 3) placing the silicon chip on the underfill and aligning the chip manually, and 4) curing the sample. Figure 4.1c describes the nominal dimensions of each component on a cross-

section view. The nominal width of the underfill fillet was relatively large at 2.0 mm, to avoid the possible influence of its boundary on the deformation at the chip corner.

Table 4.1 Dimensions of components

	Length (mm)	Width (mm)	Thickness (mm)
Chip	6.01 ± 0.003	5.99 ± 0.003	0.55 ± 0.003
Underfill			0.06 ± 0.006
Substrate	20.25 ± 0.003	12.08 ± 0.015	0.40 ± 0.003

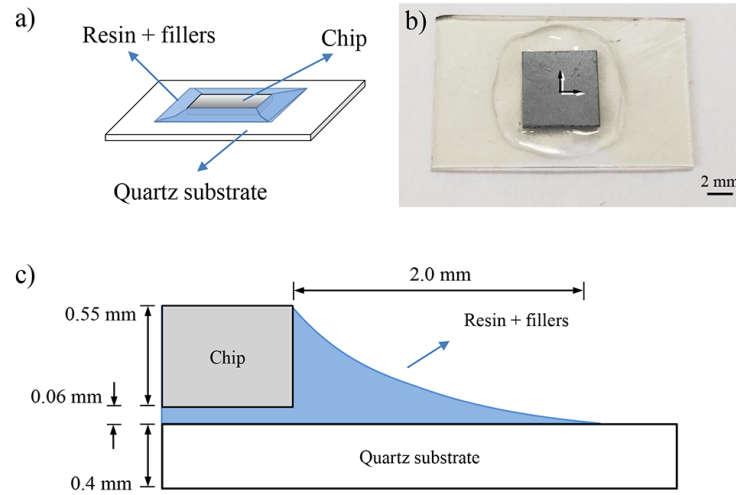


Figure 4.1 (a) Sample diagram, (b) sample photo and (c) nominal dimensions of each component.

An artificial planar crack was fabricated near the chip corner along the 45° diagonal direction of the chip, by using a laser with a 355 nm wavelength in the LPKF Protolaser U3 laser etching system. The diameter of the focused beam was $15 \mu\text{m}$ and the power was set at 1.2 W. At this intensity, the laser can pass through the quartz without causing any mechanical and thermal damage; only the underfill was etched. The position of this artificial crack could be controlled with a tolerance of $\pm 10 \mu\text{m}$, which facilitated the construction of a corresponding numerical model. The crack height was estimated from the width of etching multiplying a typical height-to-width ratio. The width of etching was $15 \mu\text{m}$, identical to the diameter of the focused beam. In reference [192], a typical height-to-width ratio of a single pass laser etching with a 355 nm wavelength was 11.6 ± 2.2 . Thus, the nominal crack height above the plane of the substrate was estimated at $174 \pm 33 \mu\text{m}$.

A cooling temperature profile was chosen as the loading condition to generate strain in the sample. Due to the limited space on the microscope stage, an ice pack was placed on an aluminum plate as a cooling source. A 3D printed frame made of polylactic acid served as a chamber for the sample and supported the aforementioned cooling source. The

temperature in the chamber was cooled down from 25°C to 5°C ($\Delta T = -20^\circ\text{C}$), while the sample was observed by a confocal microscope. The configuration is shown schematically in Figure 4.2. The first measurement was on a sample with a crack length of 160 μm . The crack was later extended by the laser to 640 μm in the same direction for the second measurement. Another sample without artificial crack was loaded for 10 cycles between -18°C and 25°C. This sample was used to observe the direction of naturally initiated cracks, which was consistent with the direction of the artificial cracks formed by laser etching.

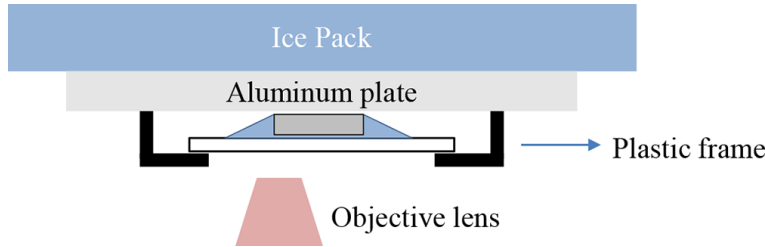


Figure 4.2 *In-situ* cooling observation setup.

4.5.2 Confocal-DIC Method

To perform the measurement of the local deformation around the crack area, LSCM was used to capture the images inside the underfill fillet. The sample was firstly illuminated by a 640 nm incident red laser reflected of a dichroic mirror, in an Olympus FV3000 confocal microscope with a 10 \times objective. Figure 4.3 shows the general principle of the confocal-DIC technique and the setup of the experiments. The sample was located above the objective lens and illuminated by the incident laser, which was reflected by the dichroic mirror (Figure 4.3a). Then, the light reflected from the sample passed through the dichroic mirror and arrived in front of a pinhole before the detector. Only the reflected light originating from the focal plane could pass through the pinhole and be imaged, whereas the out-of-focus light was rejected (Figure 4.3b). By controlling the vertical position of the focal plane, series of sliced images were captured along the vertical direction. The confocal-DIC technique was applied to the chip corner area to obtain two sets of sliced images of the underfill fillers at 25°C and 5°C, respectively. The light reflected of the sample passed through the dichroic mirror and arrived in front of a pinhole located before the detector. Only the reflected light rays originating from very close to the focal plane could be selected by the pinhole and imaged, whereas the out-of-focus light was rejected. By controlling the vertical position of the focal plane, a series of sliced images was captured along the vertical direction. This technique was applied to the chip corner area to obtain two sets of sliced images of the underfill fillers, at 25°C and 5°C. Then, a Python-based digital image correlation (DIC) script [174] was applied to calculate the strain components

by evaluating the displacement between each pair of images at the same vertical position, as shown in Figure 4.3c. Each layer produced a contour image of strain distribution. These images were gathered to construct a stacked strain distribution in a 3-dimensional view. In this work, the pixel resolution of LSCM images was $2.5 \times 2.5 \mu\text{m}^2$. For the DIC, we used a correlation window of $50 \times 50 \text{ pixel}^2$ and a grid size of $20 \times 20 \text{ pixel}^2$. Since the image was sampled in a rectangle grid by DIC, the strain components in Cartesian coordinate were firstly calculated from the DIC displacements by:

$$\begin{aligned}\epsilon_x^{i,j} &= \frac{\partial u}{\partial x} = \frac{u^{i+1,j} - u^{i-1,j}}{2d_x} \\ \epsilon_y^{i,j} &= \frac{\partial v}{\partial y} = \frac{v^{i,j+1} - v^{i,j-1}}{2d_y} \\ \epsilon_{xy}^{i,j} &= \frac{1}{2} \left(\frac{\partial u}{\partial y} + \frac{\partial v}{\partial x} \right) = \frac{1}{2} \left(\frac{u^{i+1,j} - u^{i-1,j}}{2d_y} + \frac{v^{i,j+1} - v^{i,j-1}}{2d_x} \right),\end{aligned}\tag{4.1}$$

where $\epsilon_x^{i,j}$, $\epsilon_y^{i,j}$ and $\epsilon_{xy}^{i,j}$ are the strain components x, y and xy at the correlation subset (i, j) . u and v represent the displacement in the x and y directions. dx and dy are the grid size in the x and y directions. The thermal strains were excluded from the total strains to obtain the mechanical strain components. The strain at the edge of the image was set to 0. Then, the strain components were transformed into the cylindrical coordinates. Figure 4.3d shows a photograph of the LSCM equipment. Additional details and experimental validations of this confocal-DIC technique for the local strain measurements can be found in [90].

4.6 Modeling

4.6.1 XFEM Phantom-Nodes Method

Based on the displacement function of the conventional finite element method, XFEM with phantom nodes [110, 193] introduces additional enrichment functions, which consider jumps in displacement across the crack surfaces. By introducing phantom nodes, the displacement function can be rewritten in terms of a superposition of two sub-elements to describe the cracked element. Each sub-element has real nodes and phantom nodes on both sides of the crack. Figure 4.4a shows how the cracked elements are described by sub-elements. For the example of the two sub-elements in Figure 4.4b, the displacement function becomes [193]:

$$\mathbf{u}(\mathbf{X}) = \sum_{I \in S_1} \mathbf{u}_I^1 N_I(\mathbf{X}) H[-f(\mathbf{X})] + \sum_{I \in S_2} \mathbf{u}_I^2 N_I(\mathbf{X}) H[f(\mathbf{X})],\tag{4.2}$$

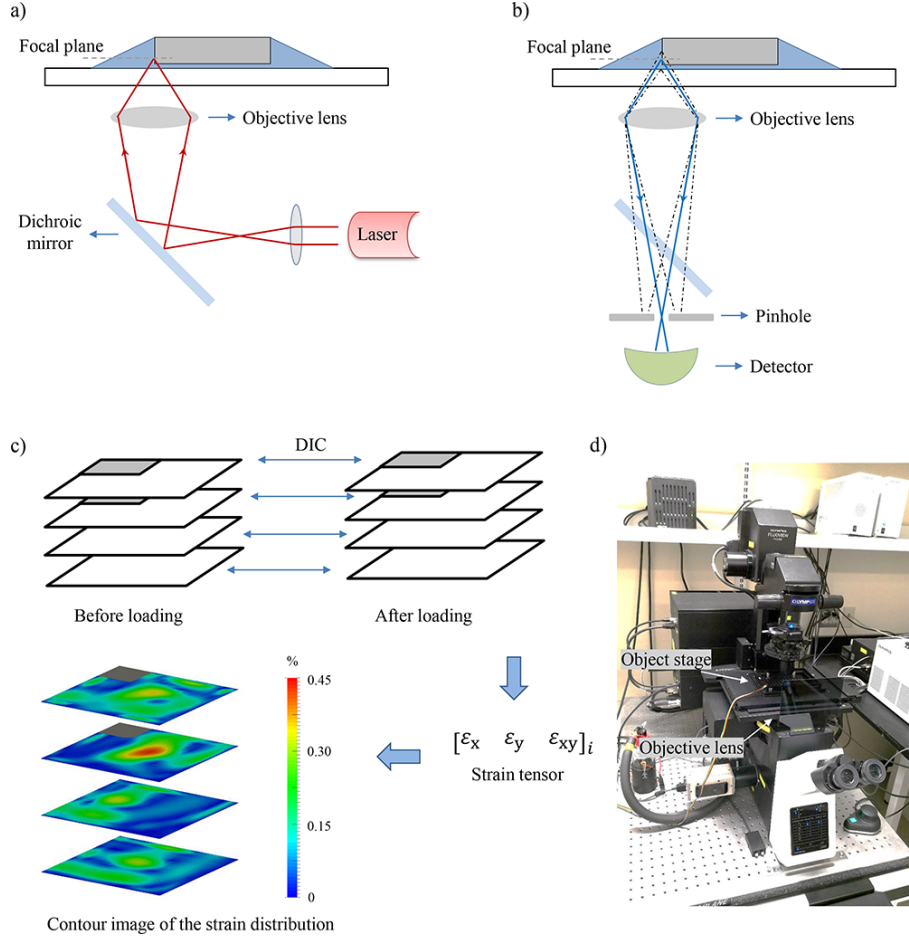


Figure 4.3 General principle of the confocal-DIC technique: (a) incident laser illuminating the sample, (b) pinhole accepting the reflection from the focal plane and rejecting out-of-focus light, (c) calculating the strain tensor from captured images (the die corner is shown in gray), (d) photo of the LSCM.

where \mathbf{u} is the displacement vector. S_1 and S_2 represent the index sets of the nodes in the superposed sub-elements 1 and 2. \mathbf{u}_I^1 and \mathbf{u}_I^2 are the nodal displacement vectors in the sub-elements 1 and 2. N_I is the conventional nodal shape functions. $f(\mathbf{X})$ is the signed distance perpendicular from the crack surface and \mathbf{X} is the coordinate vector of the position where the displacement is evaluated, as shown in Figure 4.4b. The crack surface is defined by $f(\mathbf{X}) = 0$. In a 3D configuration, the crack surface is discretized with each cut element and approximated into a series of flat planes. H is the Heaviside step function which equals 0 or 1. This method is available in ANSYS with few modifications from the conventional finite element model. The original mesh does not have to be changed if the model has been already meshed. In this method, the crack has to end on the edge of an element. This feature greatly simplifies the modeling and the mesh with cracks. Compared to a conventional FEM model with a highly refined mesh in the crack area,

the phantom-nodes method reduces the total number of elements, which saves computing resources.

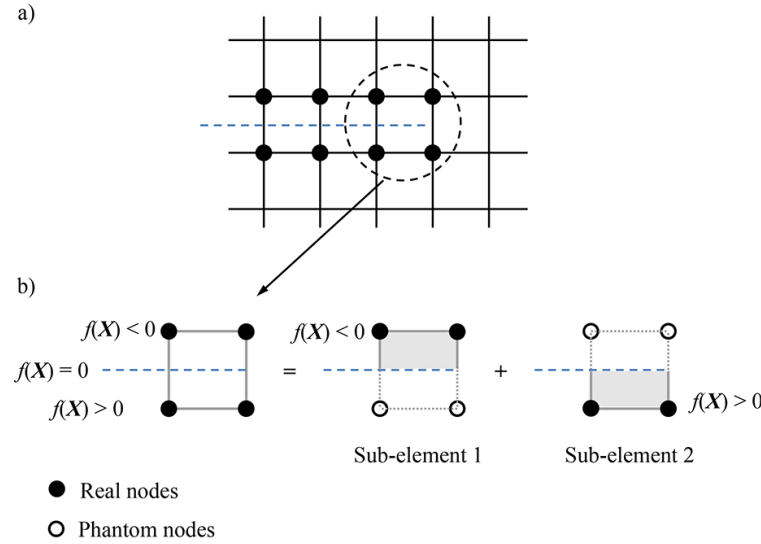


Figure 4.4 Principle of XFEM based phantom-nodes method: (a) global mesh, (b) a superposition of sub-elements, $f(X)$ is the signed distance measured from the crack (dashed line).

4.6.2 Numerical Model

A quarter-symmetry flip-chip model (global model) with the same geometry as the experimental sample was built by an efficient custom software named PACK [177], as shown in Figure 4.5a. PACK is a Python-based high performance numerical software, incorporating advanced pre- and post-processing features for multiple commercial finite element platform (including ANSYS used in this work) [178, 194]. The elements for the chip, the substrate and the underfill were hexahedral in shape, while the elements for the underfill fillets were wedge-shaped or tetrahedral-shaped. The maximum and minimum element sizes in the model were $430 \times 430 \times 55 \mu\text{m}^3$ and $35 \times 35 \times 20 \mu\text{m}^3$, respectively. In order to achieve a detailed and structured mesh for the cracking simulation, a sub-model ($1.4 \times 1.4 \times 0.3 \text{ mm}^3$) around the chip corner was built (Figure 4.5b). The cut-boundary displacements from the global model were transferred to the sub-model as an input condition, to considerably save on time and memory consumption in the calculation. The element length in the sub-model was varied from $50 \mu\text{m}$ to $16 \mu\text{m}$ in order to test independence to the mesh dimensions. For the sub-model with an element size of $16 \mu\text{m}$, the maximum and minimum elements sizes were $16 \times 16 \times 16 \mu\text{m}^3$ and $16 \times 16 \times 10 \mu\text{m}^3$. All elements in the sub-model were hexahedral in shape. Figure 4.5c shows the top view of the crack setup at the corner. The crack surface (red line) was defined by level sets, which were the shortest distances from the crack plane to the nodes of the cracked elements (e.g. from d_1 to d_4

in Figure 4.5c). The crack was positioned 1/4 length of the element away from the node 2, since $d_1 = 0$ was invalid when defining the initial crack. The crack was planar and vertically extended about 250 μm from the bottom of the underfill. The length of the crack was set at 160 μm and 640 μm , while the model was subjected to cooling from 25°C to 5°C, as in the experiments. The model reference temperature (with zero thermal strain) was set at 25°C, since this temperature was considered as the initial state for DIC calculations in the experiments. The deformation around the static crack in the experiments and simulations were compared for the same temperature difference ($\Delta T = -20^\circ\text{C}$). The materials properties are summarized in Table 4.2.

Table 4.2 Material properties in models

	Die	Underfill	Substrate
Young's modulus (GPa)	120	2	82
CTE ($\times 10^{-6}/^\circ\text{C}$)	2.6	52	7.1
Poisson ratio	0.35	0.3	0.2
Critical energy release rate (J/m^2) [195]	N/A	106.6	N/A
Maximum hoop stress (MPa)	N/A	15	N/A

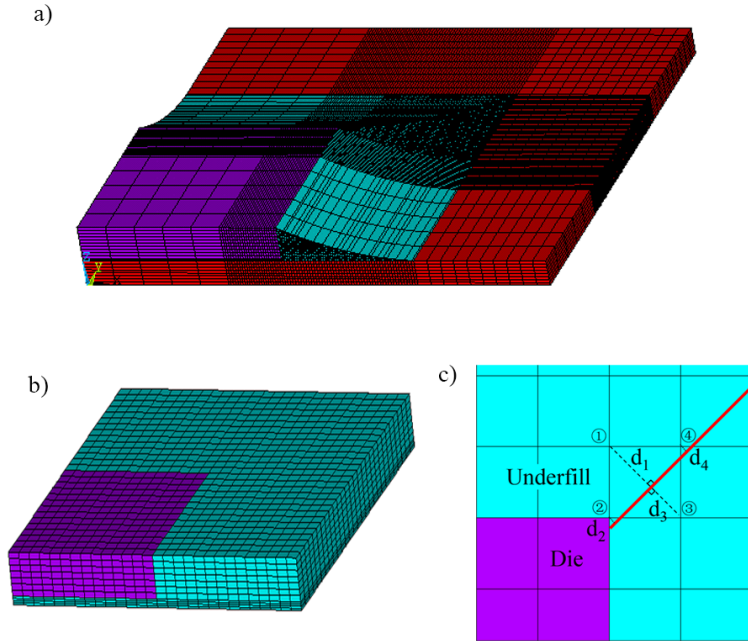


Figure 4.5 XFEM model definition with an underfill crack: (a) quarter-symmetrical model, (b) sub-model of the selected region, (c) crack defined along the diagonal direction, shown by a red line.

In addition to the static crack model, a failure criterion was implemented into the model to propagate the crack, in order to compare with the trajectories of naturally initiated cracks in the experiments. Unlike the static crack configurations with long planar cracks,

the initial crack was only placed at the chip corner, within one single element (Figure 4.6a and 4.6b). This setup could properly describe the evolution of cracks emanating from the chip corner. The model of crack propagation was subjected to cooling from 170°C to −18°C, with a stress-free temperature of 170°C corresponding to the curing temperature of the underfill. The mode I critical energy release rate of SU-8 epoxy (G_{Ic}) was set to 106.6 J/m², as reported in reference [195]. The criterion of maximum circumferential stress was used as the failure criterion [112]. The maximum circumferential stress criterion is based on evaluating the maximum value of the circumferential stress σ_θ , also called hoop stress, when sweeping around the crack tip at a radius of twice the element length. The hoop stress is perpendicular to the radial line to the crack tip. In each sub-step, when the maximum value of the hoop stress reaches a threshold value σ_{th} , the crack propagates along the direction of maximum value of the hoop stress. The value of σ_{th} is obtained from:

$$\sigma_{th} = \frac{K_{Ic}}{\sqrt{2\pi r}} = \sqrt{\frac{G_{Ic}E}{2\pi r}}, \quad (4.3)$$

where K_{Ic} is the fracture toughness, G_{Ic} is the critical energy release rate, r is twice the average element length, and E is the elastic modulus of the underfill. Although the thermal strains in the crack propagation model resulted from a single cooling pass instead of the −18/25°C cyclic loading conditions, the cracks experimentally observed propagated rapidly in the first cycles. This indicated a propagation that is consistent with single pass cracking instead of cyclic fatigue cracking. Thus, in the model the crack growth was controlled by the maximum hoop stress rather than by the fatigue damage accumulation. As it will be shown below, the comparison for static cracks of strain estimated by the confocal-DIC measurements and XFEM simulations supports the use of XFEM as a valid method to estimate the trajectory of propagating cracks.

4.7 Results and Discussion

4.7.1 Experimental Results

Figure 4.7a and 4.7b show images of the crack path for the sample without laser-etched cracks that was cycled 10 times between −18°C and 25°C, captured by a conventional optical microscope. The 3-dimensional image Figure 4.7c was obtained by the confocal microscope from the same position as Figure 4.6a. The crack started from the chip corner and propagated along the diagonal direction into the fillet area. The crack path was mainly along a straight line and no sidewall delamination was found in this situation. Thus, in the following experimental and numerical study, it was reasonable to place the artificial planar crack at the corner of the chip and along the diagonal direction.

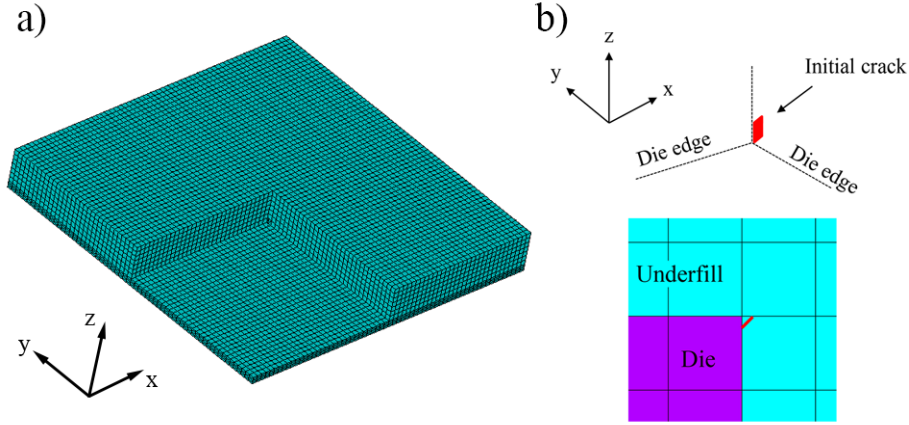


Figure 4.6 XFEM sub-model definition of crack propagation: (a) sub-model of the underfill region, (b) initial crack at the chip corner, shown by a red line.

Figure 4.8 displays the confocal-DIC strain distribution of the sample with a 160 μm crack, for a loading from 25°C to 5°C. From the top to bottom, the first 4 layers are within the chip, which is identified by a gray square. The last 3 layers are between the chip and substrate. The white lines represent the etched crack position. In order to better display the strain distribution near the crack area, the contours were plotted in a cylindrical coordinate system centred at the chip corner. In Figure 4.8 (left), ϵ_θ is the hoop strain, perpendicular to the radial crack direction. This component is most important on the mode I crack opening. The position of the maximum hoop strain was located at the crack front and its value reached around 0.25%. Figure 4.8 (right) shows the first principal strain ϵ_1 . Similar to the hoop strain, the maximum values of ϵ_1 were also located near the crack front and along the diagonal direction, and reached about 0.45%.

Then, the crack was extended to 640 μm in the same direction via laser etching. Figure 4.9 shows the contours of ϵ_θ and ϵ_1 in this situation. Both the maximum values of these two components moved to the 640 μm diagonal position. Figure 4.8 and Figure 4.9 show a clear and precise movement of the maximum strain value compared to the etched crack position. As the confocal-DIC is based on an optical system, the accuracy of strain measurements may be affected by both image acquisition and image processing. In our previous work [90], when the temperature difference before and after loading was 20°C, the absolute error between the strain components measured by confocal-DIC and the thermal strains calculated analytically was estimated to be around 0.05%. This error led to some areas away from the crack regions with strain levels that were above the low background strain level in Figure 4.8 and 4.9. Also, for both 160 μm crack and 640 μm crack, the top four

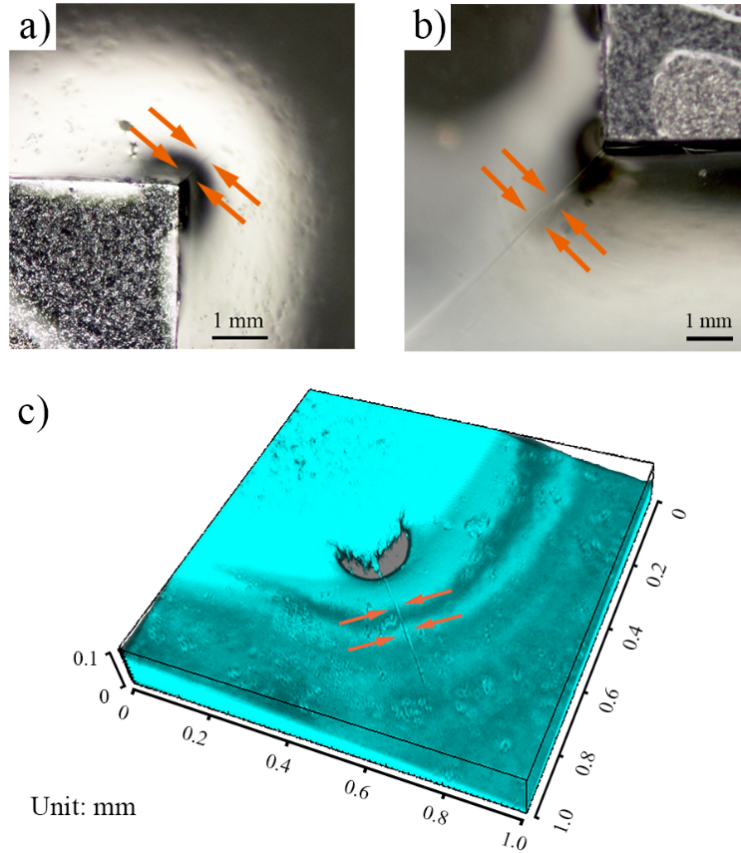


Figure 4.7 (a) and (b) 2-dimensional and (c) 3-dimensional images of the naturally initiated corner crack.

layers had higher levels of principal strain at the crack tip. Apart from the crack front area and noise patches, no other areas of high local strain were observed.

4.7.2 Comparison and Improvements of Numerical Model from Experimental Results

The typical contours of hoop strain computed using XFEM for the 160 μm crack and 640 μm crack are shown in Figure 4.10, in the plane of the chip corner. The XFEM strain contours are similar to the strain patterns obtained experimentally and shown as in Figure 4.8 and 4.9. For both the 160 μm crack and 640 μm crack, large hoop strains were found at the crack tip and the strain distributions were symmetrical about the cracks. The hoop strains in the regions far away from the crack tip were constant and were less than 0.12%.

In order to compare with the numerical results, the strain ϵ_θ was extracted at various distances from the crack tip along the diagonal direction. To obtain a better spatial resolution, the window size of DIC was reduced from $50 \times 50 \text{ pixel}^2$ to $20 \times 20 \text{ pixel}^2$ and the grid size was reduced from $20 \times 20 \text{ pixel}^2$ to $10 \times 10 \text{ pixel}^2$ at the crack tip areas. It is

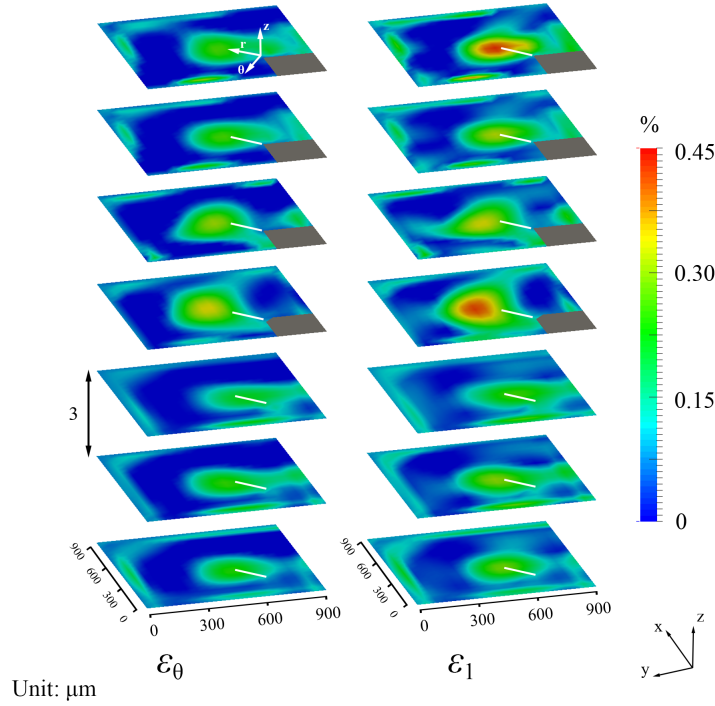


Figure 4.8 Strain component ϵ_θ and first principal strain ϵ_1 in the sample with a crack length of 160 μm . White lines represent the position of the etched crack. The die corner is shown in gray.

important to mention that a smaller window size and grid size can improve the resolution, but may also cause larger random errors depending on the quality of images [196]. Several parametric studies have shown that a window size of no less than $20 \times 20 \text{ pixel}^2$ were appropriate in practice [187, 197, 198]. In this work, the random errors increased rapidly when the window size was smaller than $20 \times 20 \text{ pixel}^2$. Figure 4.11 and 4.12 summarize the distribution of ϵ_θ for the sample with a crack length of 160 μm and 640 μm , respectively. In the top four layers in Figure 4.8 (left) and 4.9 (left), the strain values ϵ_θ of each layer were collected along the diagonal direction, with respect to the distance away from the crack tip. Then, the four values at the same horizontal position were averaged. Two-sided 90% confidence intervals for small sample size were calculated based on the t-distribution [199]. The strain measured by confocal-DIC near the crack tip had a larger confidence interval, because the calculated strain values became more sensitive to the large deformation when the correlation window reached the crack tip. In Figure 4.11, the maximum hoop strain measured by confocal-DIC was 0.32% and decreased to 0.082% at 50 μm . From 50 to 175 μm , the measured strains had a slight fluctuation but were generally stable around 0.1%.

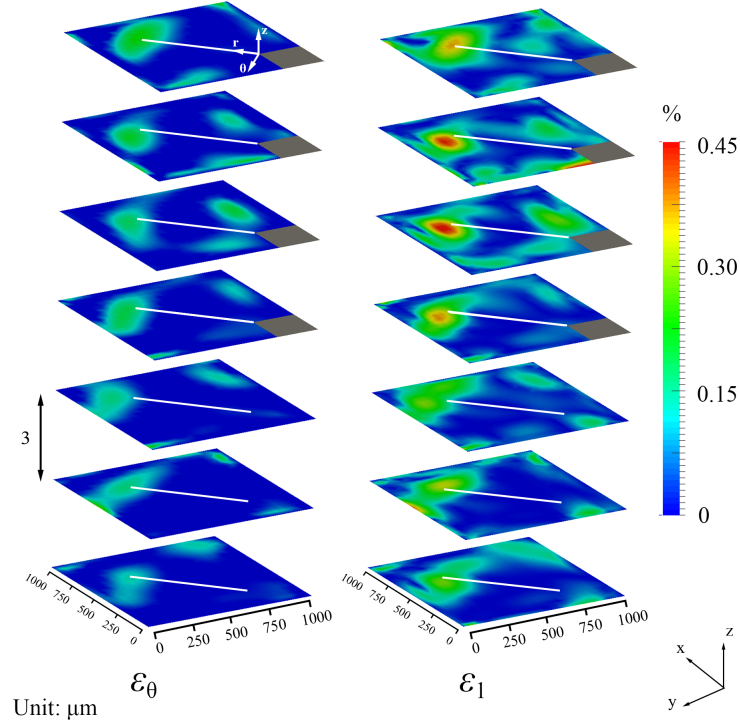


Figure 4.9 Strain component ϵ_θ and first principal strain ϵ_1 in the sample with a crack length of 640 μm . White lines represent the position of the etched crack. The die corner is shown in gray.

Because of the strong strain gradient near the crack tip, it was expected that the element size in the numerical simulations would have to be reduced (at the cost of longer calculation times) to capture the large strain variation observed experimentally near the crack tip. Without any other adjustments to the parameters of the simulation, multiple runs of the simulation were performed by reducing the element size from 30 μm to 16 μm . In all cases, the strain decreased rapidly in the first 50 μm away from the tip and then attained a constant value. With the reduction of the element size, the maximum strain increased up to 0.23% at 16 μm element size, which was close to the experimental results. Figure 4.12 shows similar distributions for a longer crack. For both crack lengths, the calculated strain values were consistent with the confidence intervals for the experimental measurements. In terms of percentage comparison between experiments and simulations, the hoop strain obtained by the simulation at 16 μm element size was 22.0% and 9.5% lower than the average hoop strain measured by experiments, for the 160 μm crack and the 640 μm crack, respectively. When the distance was from 50 to 175 μm away from the crack tip, the average hoop strain over this interval in simulation was only 8.2% and 6.3% higher than that in experiments, for the 160 μm crack and the 640 μm crack, respectively.

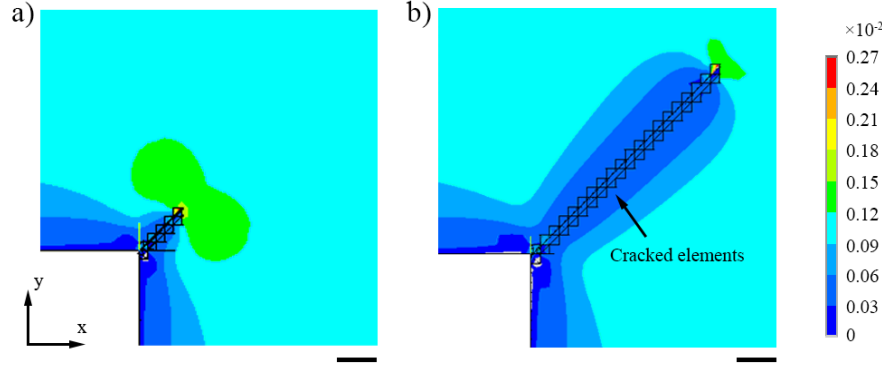


Figure 4.10 Hoop strain computed by XFEM for (a) the 160 μm crack and (b) the 640 μm crack, with an element size of 22 μm . Scale bar lengths of 100 μm . The white area in the lower left corner represents the die.

Then, a comparison of hoop strains in the direction perpendicular to the diagonal direction from the crack tip was performed between the experiments and simulations (16 μm element size). Figure 4.13 shows the distribution of hoop strain ϵ_θ perpendicular to the diagonal direction for the samples with a crack length of 160 μm and 640 μm . The strain gradients from the simulation results near the crack tips were smaller than those shown in Figure 4.12 and 4.14. When the distance was 150 μm away from the crack tip, the XFEM calculated hoop strains remained constant at 0.11% for the 160 μm crack and 0.10% for the 640 μm crack. For both crack lengths, the calculated hoop strains perpendicular to the diagonal direction were all located within the confidence intervals of measured hoop strains.

Although the crack lengths were different in Figure 4.11 and Figure 4.12, the local strain distribution was still strongly controlled by its position relative to the crack tip, instead of the global position in the underfill. For both the experimental and numerical data, the maximum values of ϵ_θ are close together and largely independent of crack length. The values far from the crack tip also matched well between the experimental and numerical data.

In addition to the element size, it may be possible to improve the accuracy of the numerical model by considering the effect of corner shape and filler distribution, among other possible modifications to the model that are motivated by experimental observations. Several runs of our model were performed while changing the angle of the chip sidewall by up to $\pm 14^\circ$, with an increase of only 1% observed in the strain value at the crack tip. The same analysis showed that the influence of the underfill thickness was less than 2% on the crack tip strain when the thickness increased or decreased by up to 20%. Thus, the angle of the chip sidewall and the underfill thickness is not a main factor to improve the agreement to experimental results.

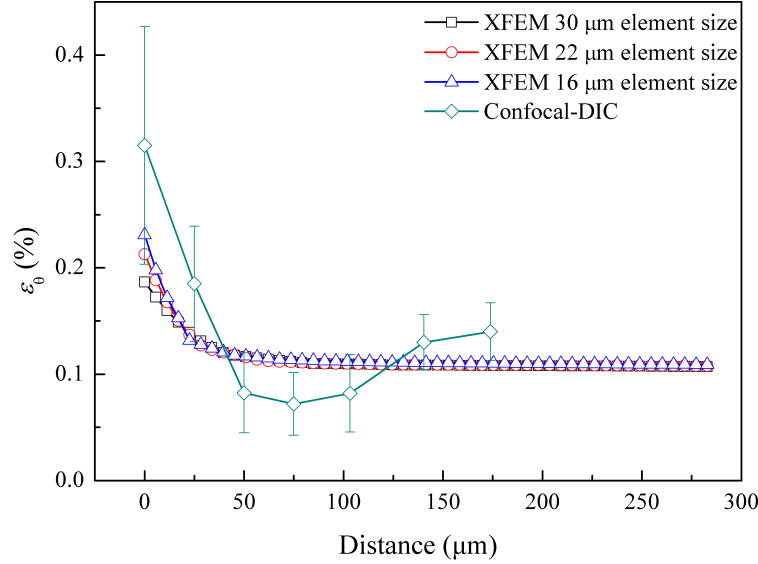


Figure 4.11 Strain component ϵ_θ as a function of the distance away from the crack tip along the diagonal direction, for the 160 μm crack, for the XFEM model with an element size of 30 μm (square markers), 22 μm (round markers), 16 μm (triangle markers), together with the confocal-DIC measurements (diamond markers). Error bars represent two-sided 90% confidence intervals.

Then, the effect of filler distribution was analyzed on the strain value. In Figure 4.8 and 4.9, when considering the planes below the chip, the first principal strain at the crack tip in the bottom three layers was about 20-40% lower than that in the top four layers. Considering the effect of gravity on fillers, more fillers are observed in the bottom than in the top regions, and the CTE in this region might be lower than the other regions in the underfill. The filler density in each layer was evaluated by counting the number of light pixels in the raw images obtained by the confocal microscope. The average filler density was around 0.8% in the bottom layers. The corresponding CTE of the bottom layers was calculated by the model given by Kerner [200]. The calculated CTE was 51.2 PPM/ $^{\circ}\text{C}$ in the bottom layers, which was 1.5% lower than in the top layers. Figure 12 summarizes the relationship between the first principal strain at the crack tip and the variation of filler density in the bottom layers. The principal strain ϵ_1 is used as it showed more evident differences than the hoop strain ϵ_θ in Figure 4.8 and 4.9. In the simulations, for both the model with the 160 μm crack and with the 640 μm crack, the ϵ_1 strain at the crack tip already showed differences between the top layers and bottom layers if the fillers were considered to be uniformly distributed. When the filler density was increased in the bottom layers, the ϵ_1 strain remained almost constant in the top layers but was reduced in the bottom layers. The hoop strain ϵ_θ had a similar behaviour as the principal strain in both experiments and simulations. Incorporating in the model the gravity-driven

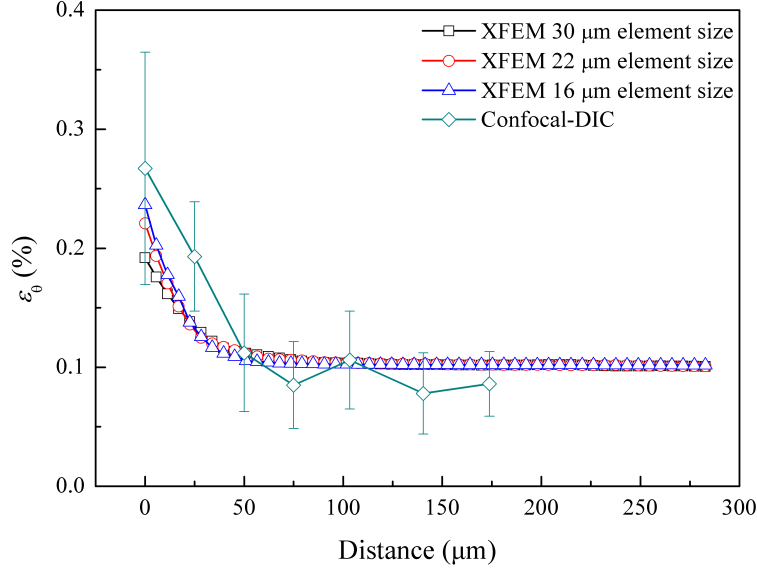


Figure 4.12 Strain component ϵ_θ as a function of the distance away from the crack tip along the diagonal direction, for the 640 μm crack, for the XFEM model with an element size of 30 μm (square markers), 22 μm (round markers), 16 μm (triangle markers), together with the confocal-DIC measurements (diamond markers). Error bars represent two-sided 90% confidence intervals.

concentration of fillers could thus slightly improve the accuracy of the calculated strain in the bottom layers, but the effect is relatively small (around 1.7% relative change per 1% relative change in the filler volume fraction).

4.7.3 Order of Stress Singularity

The order of singularity at the crack tip is another useful parameter. Figure 4.15 and Figure 4.16 summarize the relation between the hoop stress along the diagonal direction and the distance away from the crack tip for the model of the 160 μm crack and the 640 μm crack, in a log-log plot. In the vicinity of the crack tip, the stress can be described as:

$$\sigma_\theta \propto \frac{1}{r^{1-\lambda}}, \quad (4.4)$$

where σ_θ is the hoop stress, r is the distance to the crack tip and λ is the order of singularity. Table 4.3 summarizes the value of λ estimated from the slope of σ_θ , using the data from 10 to 50 μm in Figure 4.15 and Figure 4.16. The order of singularity between the different crack lengths was similar at each element size, and it reaches 0.76 and 0.77 at an element size of 16 μm .

The theoretical order of singularity is 0.5 for a crack tip, as reported in the literature [57]. The cracks fabricated in our experiment had a less pronounced singular effect, as the

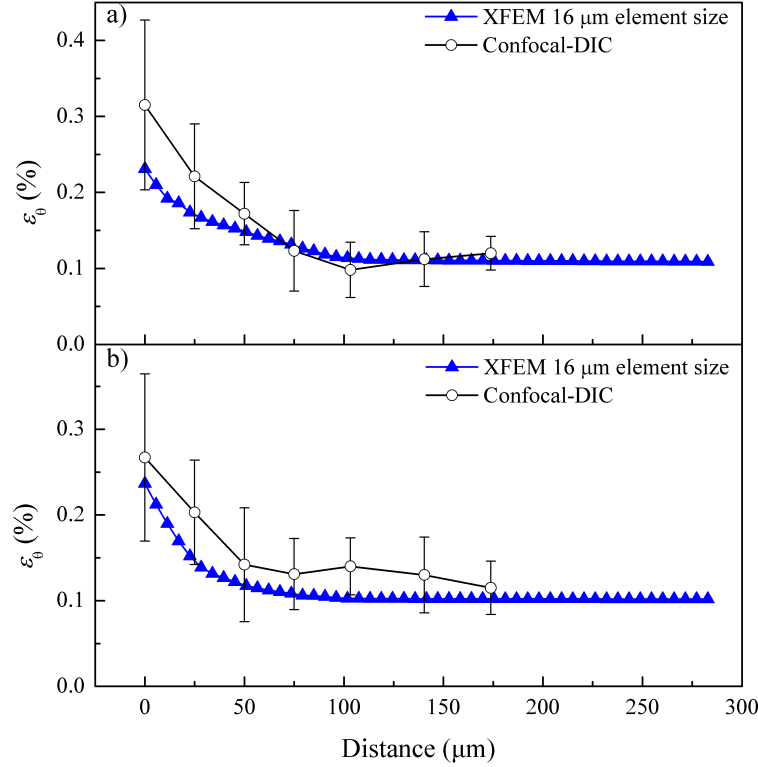


Figure 4.13 Strain component ϵ_θ as a function of the distance away from the crack tip, in the direction perpendicular to the diagonal direction, for (a) the 160 μm crack and (b) the 640 μm crack. The triangle markers represent the XFEM model results with an element size of 16 μm . The round markers represent the confocal-DIC measurements. Error bars represent two-sided 90% confidence intervals.

crack tip had a finite radius of around 10 μm . In addition, while the crack profile was planar along the diagonal direction, its upper and lower boundaries were located in the underfill and on the substrate, as shown schematically in Figure 4.17. The crack geometry was symmetrical at the half-height point, where the order of singularity should be higher than 0.5, since this value represents the strongest singularity effect in theory, which is the ultimate value for the actual situation. The singularity effect has also been found to be weakened when the Poisson's ratio of the material was greater than zero [201]. The lower and upper boundary vertices can be considered as a special form of the Fichera corner with a small angle. The Fichera corner was a solid concave corner between three non-parallel planes [62]. As the angle between the two planes decreased to zero, the Fichera corner converged to the same shape as the crack in our model. In reference [62], the order of singularity at the vertex of Fichera corner was about 0.82. In our analysis, the order of singularity could thus theoretically be expected to be between that of the half-height point

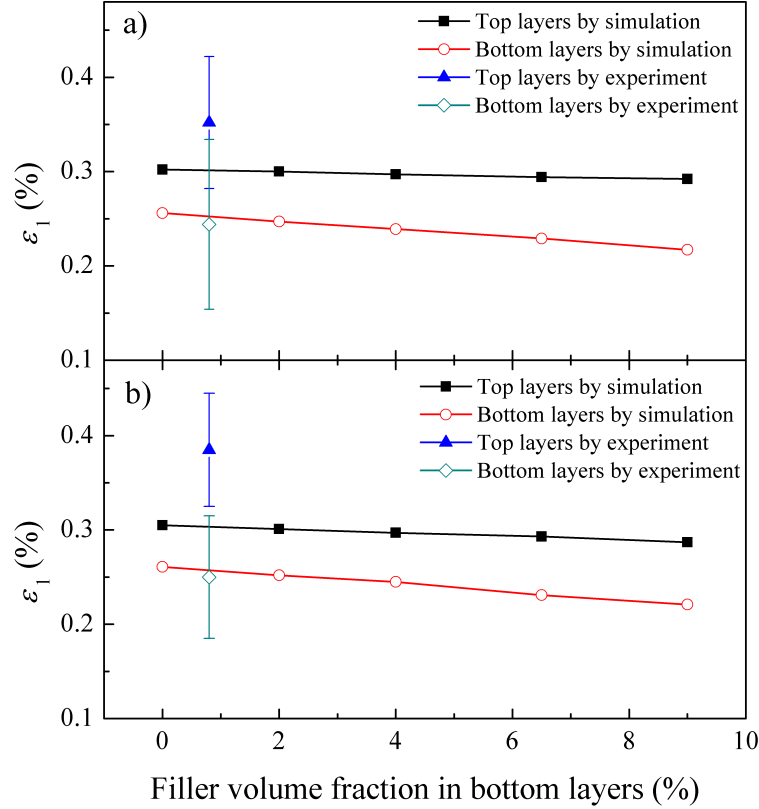


Figure 4.14 First principal strain ϵ_1 at (a) the 160 μm crack tip and (b) the 640 μm crack tip; on top layers by simulation (square markers), bottom layers by simulation (round markers), top layers by experiment (triangle markers) and bottom layers by experiment (diamond markers). Error bars represent two-sided 90% confidence intervals.

and of the small angle Fichera corner, at the position of the measurement height (Figure 4.17).

Table 4.3 Order of singularity at crack tips

Element size (μm)	50	30	22	16
Crack at 160 μm	0.92	0.86	0.81	0.76
Crack at 640 μm	0.92	0.85	0.81	0.77

The model with 16 μm elements provides strain values that are similar to those from the model with 22 μm elements, except in the first few elements near the chip corner, but it consumes twice the amount of computing resources. The element size of 22 μm was chosen in the following models of crack propagation to achieve a reasonable balance between accuracy and computing time. In the modeling of crack propagation, the model simulated a single crack emanating from the chip corner. Figure 4.18 shows the evolution of the crack profile. At first, the crack started from the corner element. It firstly propagated

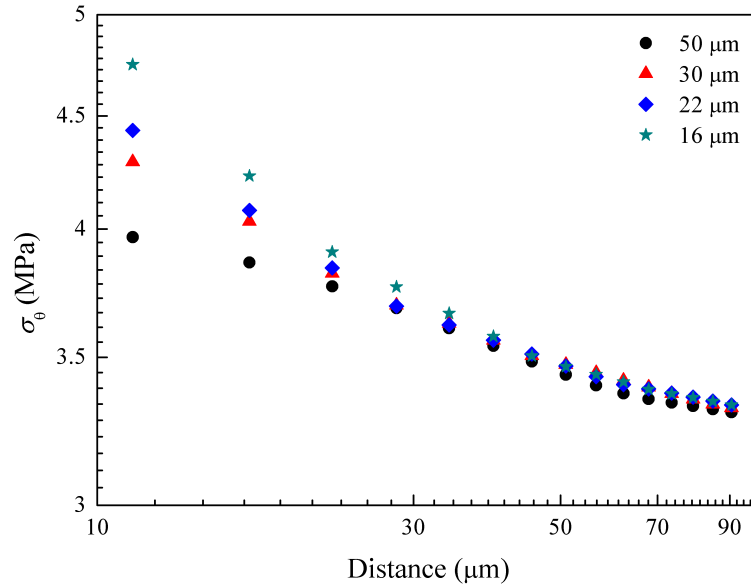


Figure 4.15 Hoop stress σ_θ at the crack tip with respect to the distance away from the crack tip for the model of the 160 μm crack, with an element size of 50 μm (round markers), 30 μm (triangle markers), 22 μm (diamond markers), and 16 μm (star markers).

vertically along the chip edge and then grew along the diagonal direction away from the chip corner, as a planar crack at a 45° angle. The direction of this crack profile was in good agreement with the experimental observations shown in Figure 4.7. In the model, the crack ended at a length of 495 μm , shorter than the cracks observed in the experiments, which were observed to propagate to 1090 μm . This was an artificial effect resulting from the geometry of the sub-model that restricted the crack path.

4.7.4 Discussion on the Current Model Limitations

In addition to the above improvements in the static cracking model, this section discusses the limitations of this work and provides an outlook for building a better underfill reliability model. The confocal-DIC technique in this work focused on the in-plane strain components in the underfill. As the observed crack was in the diagonal direction from the chip corner and were likely the result of mode I crack opening, the measurements of in-plane strains for different slices were appropriate. The confocal-DIC technique, as used herein, was not able to provide the strain components in the out-of-chip-plane direction, which would be necessary to evaluate the rate of growth of the cracks in the underfill in the out-of-chip plane direction. To obtain full 3D strain measurements, a DIC method based on voxel tracking could be used in the future.

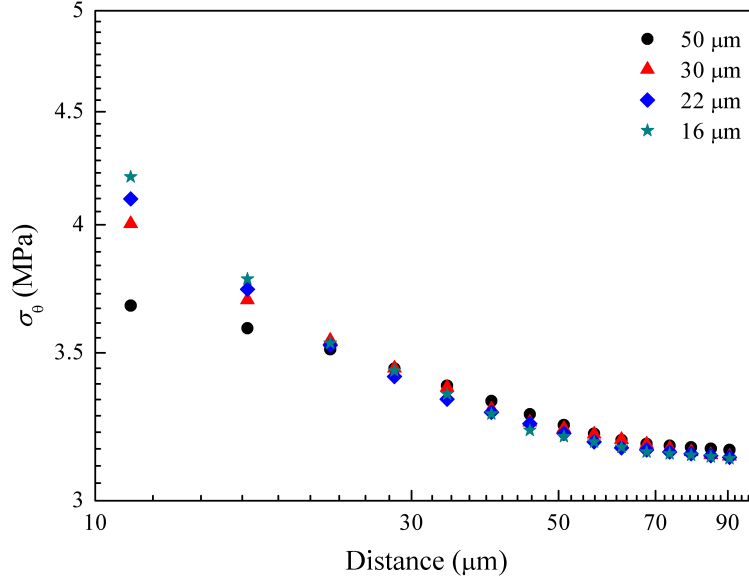


Figure 4.16 Hoop stress σ_θ at the crack tip with respect to the distance away from the crack tip for the model of the 640 μm crack, with an element size of 50 μm (round markers), 30 μm (triangle markers), 22 μm (diamond markers), and 16 μm (star markers).

A model of fatigue crack growth could be further developed, which would be able to estimate the underfill damage with respect to the number of cycles. In our crack propagation model, the crack was generated during a single load cycle, while during experimental thermal cycling fatigue crack growth, the crack was observed after the first few cycles. A 3D fatigue crack model could also be useful when the underfill crack is observed to grow steadily with the number of cycles. More parameters would have to be estimated to build fatigue crack models, such as the fitting coefficients of the Paris law, that empirically describes the relationship between a stress intensity factor and the crack growth rate. The stress intensity factor is a theoretical construct to provide a failure criterion, that can be expressed in the following form:

$$\sigma_i = \frac{K}{2\pi r} f_i(\theta), \quad (4.5)$$

where σ_i is a stress component, K is the stress intensity factor, r is the distance to the crack tip, and f_i is a dimensionless quantity that varies with the crack mode [66]. In such a simplified relationship, the K value may not be constant during the whole process of crack growth, as the stress σ_i would vary with the actual filler density at the crack tip. A more highly refined mesh could also help obtain better accuracy of σ_i . Then, the fatigue crack growth model would have to evaluate the growth rate at each point of the crack front and determine the global crack increment at each time step. An experimental approach to monitor the crack growth rate with the number of cycles would have to be developed to

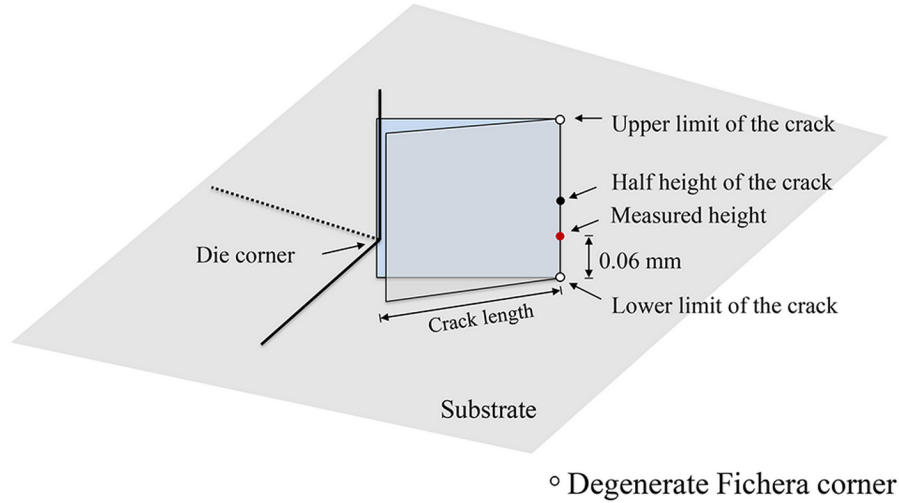


Figure 4.17 Diagram of the whole crack height.

validate such simulations. The fatigue crack growth model would be more useful than the static crack model for reliability predictions, as the cracks are usually observed to grow progressively with respect to the number of cycles [136]. The fatigue crack model could further estimate the reliability of solder joints by evaluating their maximum stress, starting from the underfill crack initiation. However, the errors of estimation would accumulate with each iteration, which may make it challenging to obtain accurate predictions of the crack location after a certain number of cycles [202].

In addition to the fatigue crack model, the moment of crack initiation is another metric for the reliability estimation, that is inversely correlated with the local stress amplitude [203]. The crack initiation moment is difficult to obtain precisely during a cyclic test, as the crack usually requires destructive cross-sectioning to observe. But it can be roughly estimated by setting up several inspection intervals. Then, an empirical fit between the crack initiation moment and the local stress amplitude could be performed and applied to the crack initiation estimation.

Other failure modes, such as delamination on passivation interface, should also be considered in the future model. The model of delamination aims at estimating the delaminated area at the passivation-underfill interface with respect to the number of cycles. Due to the CTE mismatch between the silicon die and underfill, the passivation-underfill interface is subjected to shear stresses and its delamination was often observed in practice [34, 42, 53, 204]. As the delamination occurs when the shear stress reaches the interfacial shear strength, a measurement of stresses or strains in the interface region could be used to construct an accurate model. As the shear strain varies with the vertical distance to

the interface, it is necessary to obtain high resolution strain measurements perpendicular to the interface. 3D X-ray tomography may provide higher resolution than the confocal microscopy for DIC strain measurements, since the X-ray can better penetrate the test component and obtain vertical cross-sectional images. As the underfill strains in modeling are strongly affected by the local filler distribution, geometry and element size, with careful strain measurements in the region near interfaces, practitioners could better select the element size, underfill local CTE and geometry of each component to approximate the strain level near the interface. Thus, starting from the static crack model, the underfill reliability model can further include fatigue cracking, crack initiation and interface delamination, whose strain fields can be validated experimentally.

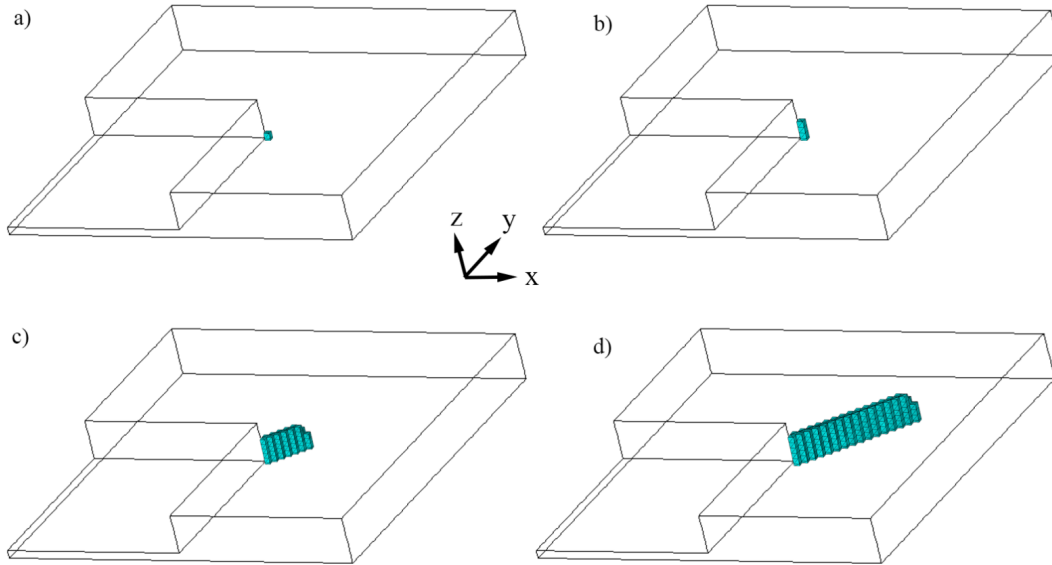


Figure 4.18 Crack path starting from the chip corner: (a) initiating element, (b) growing on z direction, (c) propagating along the diagonal direction, (d) end stage.

4.8 Conclusions

In this work, we have applied the confocal-DIC technique to directly measure the local deformation of the underfill material around cracks in an assembly which was similar to a flip-chip package. The position of the maximum measured strain was in good agreement with the position of artificial cracks. After cyclic temperature loading, naturally initiated cracks were observed from the chip corner and propagated along the diagonal direction.

Based on the guidelines provided by the confocal-DIC results, a numerical model was built by introducing the extended finite element method with phantom nodes in a crack sub-model. In a first, relatively coarse model that did not include much of the complications

of an actual flip chip package, the distributions of the hoop strain in the experiments and simulations were in good agreement, with rapidly dropping values away from the crack tip, that reached a constant value far from the tip. The local strain distribution was controlled by its position relative to the crack tip, independently on the crack length. Furthermore, a propagation model was built based on the XFEM phantom-nodes method. The crack paths were in good agreement with experimental observations, along the diagonal direction. The crack ended at a length of 495 μm , shorter than the experimental observations, because of the geometry limitations of the sub-model. The XFEM phantom-nodes approach could thus obtain a similar strain distribution and a correct crack path, compared to the experimental data.

Then, more detailed features were introduced in the model and analyzed, in an attempt to improve the accuracy of the model. The angle of the chip sidewalls and the underfill thickness had a negligible influence on the crack tip strain, so they did not appear to be critical features in underfill crack modeling. When reducing the element size to 16 μm in the numerical model, the hoop strain ϵ_θ at the crack tip was within the confidence intervals for the measured strains. The use of smaller elements resulted in a better agreement between the numerical and experimental data. The hoop strain obtained by simulation at 16 μm element size was 22.0% and 9.5% lower than the average hoop strain measured by experiments for the 160 μm crack and 640 μm crack respectively. This difference decreased to 8.2% and 6.3%, respectively, when the distance was from 50 to 175 μm away from the crack tip along the diagonal direction. A reduction in the CTE in the regions below the chip, resulting from the gravity-driven concentration of filler particles, could also slightly improve the agreement with the measurements of the principal strain and hoop strain at the crack tip between the chip and the substrate. The analysis showed how the element size, model geometry and local CTE affected the calculated strain at underfill crack tips.

In addition to the precision improvements in underfill static crack modeling, fatigue crack growth and passivation-underfill interface delamination should become part of future models. A fatigue crack growth model would be able to estimate the crack location with respect to the number of cycles. Local stresses and strains at the crack tip or near the interface are the key parameters in constructing reliability models that incorporate all relevant failure modes. As the stress and strain have stress singularities in both bulk cracks and interface crack regions, the actual strain values near the crack tip must be studied experimentally to improve the accuracy of strain calculations. Compared to theoretical formulas and standardized cantilever beam tests, *in-situ* strain measurements can reflect the influence of process-related effects on the strain, such as filler density and corner geometry. Thus,

in-situ strain measurements are the most direct way to obtain the actual strain field and provide reference metrics for modeling. We have presented in this paper strain measurements that were applied to corner cracks and that could eventually be used to validate the underfill cracking model.

CHAPTER 5

Modeling of Flip-Chip Underfill Delamination and Cracking with Five Input Manufacturing Variables

5.1 Avant-propos

Auteurs et affiliation:

Y. Yang: Étudiant au doctorat, Université de Sherbrooke, Faculté de génie, Département de génie mécanique.

M. K. Toure: Professionnel de recherche, Université de Sherbrooke, Faculté de génie, Département de génie mécanique.

P. M. Souare: Ingénieur, IBM Bromont.

E. Duchesne: Ingénieur, IBM Bromont.

J. Sylvestre: Professeur, Université de Sherbrooke, Faculté de génie, Département de génie mécanique.

Date d'acceptation: 25 mars 2022

Revue: Microelectronics Reliability

Titre anglais: Modeling of Flip-Chip Underfill Delamination and Cracking with Five Input Manufacturing Variables

Titre français: Modélisation de la délamination et de la fissuration de l'underfill des puces retournées avec l'effet de cinq variables de fabrication en entrée.

Contribution au document: Cet article présente une approche de modélisation pour estimer le moment initial de délamination à l'interface de puce/underfill, les régions de délamination et les trajectoires de fissures dans l'underfill de flip-chip. Il contribue à la thèse en répondant au troisième objectif de ce projet de recherche. Sous l'influence de cinq variables de fabrication en entrée, ce travail a permis de fournir une prédiction sur le nombre de DTC cycles à délamination, les zones de délamination et les directions des fissures, qui sont cohérentes avec les caractérisations expérimentales.

Dans cet article, j'ai développé tous les modèles numériques pour la délamination initiale, la croissance de la délamination et les profils de fissures. Et j'ai analysé les résultats numériques avec les données de caractérisation expérimentales fournies par IBM.

Note: La version publiée et la version de la thèse peuvent différer en raison des commentaires des réviseurs reçus après le dépôt initial.

5.2 Résumé

La géométrie du coin de la puce et l'inadéquation du coefficient de dilatation thermique provoquent une concentration de contraintes dans l'underfill près de la zone du coin de la puce. La délamination à l'interface puce-underfill et les fissures dans l'underfill proviennent souvent du coin de la puce et peuvent se développer dans tout l'assemblage. Cet article présente une approche de modélisation qui permet d'estimer le moment initial de la délamination, la croissance de délamination et les profils de fissuration dans les encapsulations de puces retournées. Le modèle de fiabilité utilisé dans ce travail comprend cinq variables d'entrée: la largeur de l'entaille, le type de découpe, la présence d'un stabilisateur par laser, le matériau de la bande d'étanchéité et la forme de la bande d'étanchéité. Treize cellules d'échantillons expérimentaux de puces retournées ont d'abord été préparées en fonction de ces variables d'entrée et ont été soumises à un test de cycle thermique profond (DTC). La microscopie acoustique à balayage en mode C (C-SAM), la microscopie infrarouge (IR) et la coupe transversale ont été utilisées pour estimer les moments initiaux de délamination dans l'underfill, les zones de délamination et les profils de fissure comme référence pour la modélisation numérique ultérieure. Un modèle de réseau neuronal artificiel (ANN) a été formé pour estimer le nombre de cycles jusqu'à la délamination pour les cellules dans l'ensemble de test. Les nombres de cycles prédits pour les 6 cellules de l'ensemble de test étaient conformes aux observations expérimentales. Un modèle d'éléments finis a été construit pour décrire la croissance de la délamination. Lorsque le modèle a atteint la même zone de délamination que celle mesurée par C-SAM, la différence entre le nombre de cycles prédit et le moment de l'inspection C-SAM était inférieure à l'intervalle d'inspection (250 cycles) pour 5 des 6 cellules en validation; le modèle de croissance de la délamination était donc cohérent avec les observations expérimentales. La méthode des éléments finis étendus (XFEM) a été utilisée pour modéliser les fissures de l'underfill sans chemins prédéfinis. L'une des fissures s'est propagée dans la direction de la diagonale, et les deux autres se sont produites sur les bords de la puce. Les directions des fissures de bord étaient en bon accord avec les observations expérimentales, avec une erreur de moins de $2,5^\circ$ pour les fissures de bord. Dans l'ensemble, avec cinq variables de fabrication en entrée, cette approche de modélisation est capable de fournir des prédictions raisonnables du nombre de cycles avant l'initiation de la délamination de l'underfill, de la zone de délamination et des chemins de fissures de l'underfill dans les encapsulations de puces retournées.

5.3 Abstract

The chip corner geometry and the mismatch of the coefficient of thermal expansion cause a local stress concentration in the underfill near the chip corner area. Delamination at the chip-underfill interface and cracks in the underfill often originate from the chip corner and might develop throughout the assembly. This paper presents a modeling approach that allows the estimation of the initial moment of delamination, the growth of delamination and the cracking profiles in flip-chip packages. The reliability model in this work includes five input variables: kerf width, dicing type, laser outrigger presence, sealband material and sealband shape. Thirteen test cells of flip-chip experimental samples were first prepared according to these input variables and were subjected to deep thermal cycling (DTC). C-mode scanning acoustic microscopy (C-SAM), infrared microscopy (IR) and cross-sectioning were used to estimate the underfill failure moments, delamination areas and crack profiles as a reference for subsequent numerical modeling. An artificial neural network (ANN) model was trained to estimate the number of cycles to delamination for cells in the test dataset. The predicted numbers of cycles for all 6 cells in the test dataset were consistent with experimental observations. A finite element model was built to describe the growth of delamination. When the model reached the same delamination area as measured by C-SAM, the difference between the predicted number of cycles and the C-SAM inspection moment were smaller than the inspection interval (250 cycles) for 5 out of 6 cells in validation; the delamination growth model was thus consistent with the experimental observations. The extended finite element method (XFEM) was used to model the underfill cracks without predefined paths. One of the cracks propagated along the diagonal direction, and the other two cracks were along the edges of the die. The directions of edge cracks were in good agreement with the experimental observations, with an error of less than 2.5° for the edge cracks. Overall, with five input manufacturing variables, this modeling approach is able to provide reasonable predictions of the number of cycles to chip-underfill delamination initiation, area of delamination and underfill crack paths in flip-chip packages.

5.4 Introduction

In a flip-chip package, an 'underfill' material layer is used to fill the volume between the silicon die and the substrate to protect the interconnections and circuits by providing mechanical support. Modern underfills consist mostly of high performance epoxies reinforced with SiO_2 particle fillers. They have a low coefficient of thermal expansion (CTE) and a high mechanical strength [205]. The interfacial adhesion can be improved by a coupling agent such as silanes [206]. Mechanical failure modes of the underfill include sidewall delaminations, delaminations from the chip active surface and cracks in the bulk of the underfill. These failure modes can adversely impact the package reliability by inducing cracks in solder joints or in the chip back end of line structures [34, 207].

The CTE mismatch between different materials leads to shear stresses at the chip-underfill interfaces and the underfill-substrate interfaces [30]. The geometry of the chip corners leads to stress concentrations in the underfill when the temperature is below the underfill curing temperature [30]. These stress concentration areas accumulate damage faster than low stress regions, and such stress concentrations have a direct impact on the initiation of delamination and cracking. The stress-related failure phenomena are aggravated in larger dies as the stress at the corner increases proportionally to its distance to the centre of the chip [40]. As a result, the topic of underfill delamination and cracking from the die corner area continues to receive attention in the literature [37, 92, 93, 97]. Accurate failure predictions for the underfill could better reflect structural weaknesses in the assembly and help understand the relationship between the mechanical and electrical failures [65]. A useful numerical model should be able to estimate the initial moment of delaminations or cracks, the growth of delaminations and the trajectories of cracks [37].

Prior to modeling, it is essential to perform experimental characterizations on real flip-chip components to identify their failure modes, as each failure mode requires an appropriate damage model to be described [34]. Accelerated temperature cycling (ATC) and deep thermal cycling (DTC) are commonly used as reliability tests [13]. In ATC and DTC, underfill cracking and delamination at the chip-underfill interfaces are frequently observed [208–210]. In reference [34], the failure modes of the underfill were divided into: 1) delaminations from the sidewalls, 2) delaminations from the kerf areas, 3) crack propagation in the underfill toward the substrate, 4) crack propagation toward the external underfill fillet, 5) crack propagation in the chip circuitry. Figure 5.1 illustrates these five underfill failure modes. These failure modes usually progress as the number of cycles increases. The delamination of the chip-underfill interface (failure modes 1 and 2 above) is affected by the interface strength. The chip-underfill interface strength can be influ-

enced by factors such as moisture absorption in the underfill, which reduces the adhesion strength of the interface [49, 50]. Flux residues can create underfill flow voids and weaken the adhesion to the die [46], whereas plasma cleaning of the die and substrate can reduce such voids [47, 48]. For crack-related failure modes (3-5 above), the chip dicing process has an impact on the curvature radius of the die corners and a sharper die corner can result in a higher stress concentration in the underfill. To alleviate this effect, laser grooves can be used to remelt the chip edge and produce a rounded surface at the chip edge, which is less sharp than the 90° corner from blade dicing [28]. The blade dicing process also applies mechanical stresses to the die and may cause chipping and cracking on sidewalls [28], affecting the interfacial adhesion through different surface roughness. In addition, gravity- and flow-driven filler segregation has been observed in reference [7] and may also result in a different stress distribution in the underfill, compared to the underfill with uniformly distributed fillers. All these features are important for developing models for the underfill reliability but are difficult to predict from first principles. Thus, numerical models should be informed by certain experimental characterizations to obtain the underfill strain distribution and the trajectories of delaminations and cracks.

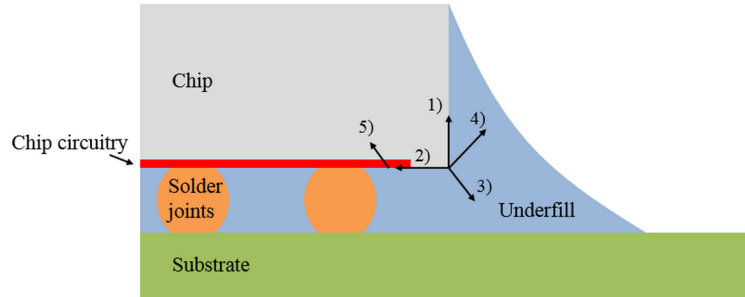


Figure 5.1 Illustration of underfill failure modes: 1) delaminations from the sidewalls, 2) delaminations from the kerf areas, 3) crack propagation in the underfill toward the substrate, 4) crack propagation toward the external underfill fillet, 5) crack propagation in the chip circuitry.

Direct measurement approaches, such as the confocal-DIC method introduced in [90], can obtain the underfill strain distribution at chip corners for an underfill with a low density of fillers [90, 184]. Apart from the confocal-DIC method, carbon nanotubes added to the underfill can also be good strain sensors, as their Raman shift responds linearly to the imposed strains [77]. However, this measurement process requires the selection of individual nanotubes oriented along the appropriate directions, which is a time-consuming process [55]. In addition, the moment of initiation and trajectories of delaminations can be obtained by C-mode scanning acoustic microscope (C-SAM) and the crack paths can be obtained by cross-sectioning periodically during DTC tests.

Experimental characterization, especially when performed repeatably in thermal cycling, can be costly and time-consuming. It would therefore be highly desirable to have a good numerical model that could simulate the whole thermal cycling process, including the initiation and evolution of underfill damage. Considering the mostly flat geometry of flip-chip packages, most studies have simplified the model to a 2D plane-strain configuration to assess the elastic stress distribution at the chip corners under static thermal loading [211] and mechanical loading [212]. The simplification to 2D plane-strain was effective when the out-of-plane stress could be neglected by symmetry, such as the chip edge midpoint cross-sections and the chip diagonal cross-sections. However, the 2D plane-strain configuration may seriously underestimate the magnitude of the crack driving forces [97], which cannot exactly reflect the stress in underfill and estimate the area of chip-underfill delamination.

In addition to the above limitations from 2D models, several 3D models have been used to study the stress distribution in the underfill [7, 90, 101]. These studies used classical linear elastic FEM models to calculate the stress at chip corners. The chip corners were considered as perfectly sharp with orthogonal planes, and the effect of corner radius and angles between the sidewalls and bottom surface of the die have not been included in these studies. For underfill delamination and cracks, the fracture mechanics-based 3D modeling of underfill damage is quite limited [204]. In reference [97], the energy release rate of underfill delamination was calculated for different delamination sizes at the chip-underfill interface, but the delamination was static with no modeling of delamination growth.

To improve the accuracy of underfill reliability models, some attempts have been made on local chip corner shape and underfill filler distribution. In reference [103], the effect of the corner shape on the chip corner stress was analyzed in a 2D model, but the corresponding underfill stress was not studied. The effect of filler settling was studied numerically [20]. Compared to the homogeneous filler assumption, a bilayered underfill model and gradual filler settling model could both cause a higher interfacial peeling stress at the corner and also a slightly reduced peeling stress in the die/solder interface where solders reside [20], but the effect of filler settling on underfill reliability was not quantified. Thus, the development of underfill reliability model with detailed geometrical and material properties is still limited in the literature.

In general, studies are focused on one specific manufacturing defect, but actual flip-chip packages may include multiple input variables together. The separate studies found in the literature do not address superimposition effects on the underfill reliability that might be caused by several defects. However, addressing all of these geometrical and material details in a single FEM model can be challenging and time-consuming, as the exact chip corner

radius, underfill filler distribution, chip-underfill interface adhesion strength and underfill fracture toughness, etc. can only be obtained by the experimental characterization of actual parts. Thus, an efficient model should directly link the input variables to the underfill damage initiation. After obtaining the underfill damage initiation, the model should be further both efficient and accurate in estimating the underfill delamination areas and crack paths under cyclic thermal loading.

In this work, the combined effects are reported of five input variables on the number of cycles to the initiation of underfill delamination during DTC, on the area of chip-underfill interface delamination, and on the underfill crack paths. An experimental characterization was first performed on the delamination and cracking trajectories in the underfill of a state-of-the-art flip-chip package under cyclic thermal loading. Three variables were process-related: the kerf width, dicing type and laser outrigger presence. The remaining two variables were the material and shape of the sealband, which is used for bonding the lid to the laminated substrate. Detailed descriptions of these variables will be presented in section 5.5. Thirteen test cells were prepared for combinations of these five input variables and performed a DTC test. The observations of underfill delamination and cracks were performed at certain time periods. These observations gave the initiation moment, the growth rate and the trajectories of delamination and cracks with respect to the number of cycles.

Then, our modeling was divided into two steps. The first step was to link the five variables to the initial moment of delamination. The five variables were encoded numerically and implemented in an artificial neural network (ANN). An ANN was chosen in this study because of its excellent performance in fitting non-linear functions. The output of the ANN model was the number of cycles to initial chip-underfill delamination. The second modeling step was to model the growth of delamination areas and cracks. The delamination model used FEM to evaluate the strain energy at the chip-underfill interface in each calculation and determine whether any interface element had failed. The calculated areas of delamination were compared with the true delaminated areas obtained by C-SAM on the whole area of die. The underfill cracking was modelled by the extended finite element method (XFEM), which is sufficiently accurate for estimating the crack tip stress and crack trajectory in a flip-chip test component according to a previous study [184]. The crack trajectories were compared with cross-sectioning images obtained near the chip corner. Our three-stage modeling approach allowed the estimation of the initial moment of delamination, the growth of delaminated areas and the 3D trajectories of underfill cracks, as functions of the five aforementioned variables.

Section 5.5 presents the detailed information about the flip-chip samples, test protocols and characterization methods. Section 5.6 presents the ANN model to estimate the initiation time of delamination under cyclic loading, the FEM for the propagation of the delamination on a flat interface and the XFEM model for multi-cracks in the bulk of the underfill. Section 5.7 presents the experimental and modeling results, including the underfill failure modes, initial moment of delamination, the area of delamination and the trajectory of underfill cracks. The comparison between the numerical results and experimental observations is discussed in section 5.7 and revealed that our model predictions were in good agreement with the experimental results.

5.5 Reliability Tests

5.5.1 Samples and Test Procedure

The reliability tests were performed with industrial high-end flip-chip packages. These packages were provided and assembled by the IBM Corporation, and comprised a large silicon die ($25 \times 25 \text{ mm}^2$), an underfill with a mass fraction of 60% SiO_2 fillers, a multi-layer laminated substrate ($55 \times 55 \text{ mm}^2$) and a copper lid. The thicknesses of the top, core and lower laminate layers were 0.33 mm, 0.40 mm and 0.33 mm. The nominal width and thickness of the sealband bonding the copper lid to the laminated substrate was 2.0 mm and 0.15 mm, respectively. The nominal thickness of the thermal interface material (TIM) between the die and the copper lid was 0.1 mm. The lid dimension was $41.5 \times 41.5 \text{ mm}^2$ (smaller than the substrate) with a thickness of 1.0 mm. The edges of the lid (3.5 mm in width) were stepped 0.7 mm down to bond to the laminated substrate. A smaller lid was chosen in an attempt to experimentally modify to corner stress distribution. The underfill was cured at 150°C for 2 hours. Figure 5.2 shows typical samples with a C-shape sealband and with a 4 lines-shape sealband. The 4 lines-shape sealband was a complete square frame, while the C-shape sealband left an opening, 7.5 mm in length.

Table 5.1 presents the thirteen test cells generated from the five input variables. Each cell contained 15 samples that were used in reliability tests. Each variable had two possible values. The kerf width is the spacing of a wafer between the crackstop of a chip to the crackstop of an adjacent chip [210]. The remaining kerf width on the die was 117 μm and 24 μm for the wide kerf (300 μm) and narrow kerf (100 μm), respectively (see Figure 5.3). The dicing type compared the blade dicing only and a combination of blade dicing with laser grooving. The laser grooving produced a rounded, irregular surface and a corner that was less sharp than the corner produced by blade dicing (see Figure 5.3). The laser outrigger is a grooved structure parallel to the die edges to increase the contact

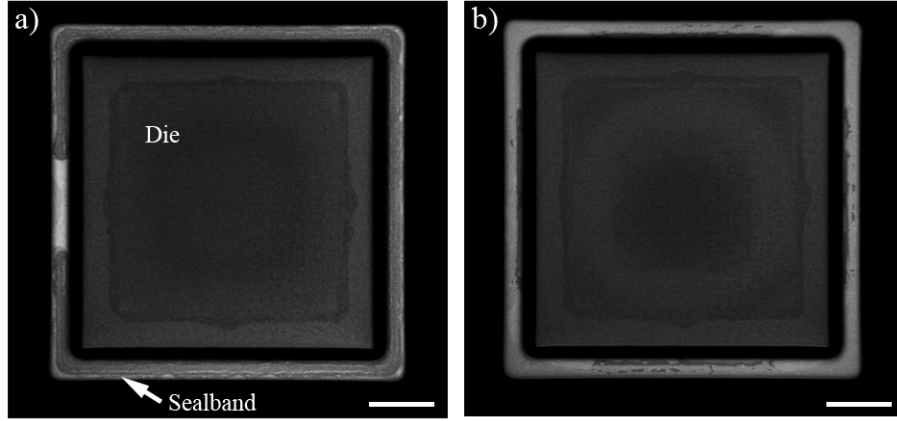


Figure 5.2 Typical samples with (a) C-shape sealband and (b) 4 lines-shape sealband, obtained by scanning acoustic microscopy (C-SAM). Scale bar lengths of 5 mm.

area between the die edge and the underfill, that were fabricated by laser etching. The width and depth of each outrigger groove was $10\text{ }\mu\text{m}$ and $15\text{ }\mu\text{m}$, respectively (see Figure 5.3). The length of each outrigger groove was identical to the length of the die. The elastic modulus and the shape of the sealbands were the last two variables. The sealband material could have a high elastic modulus (4.8 GPa) or a low elastic modulus (3.9 MPa).

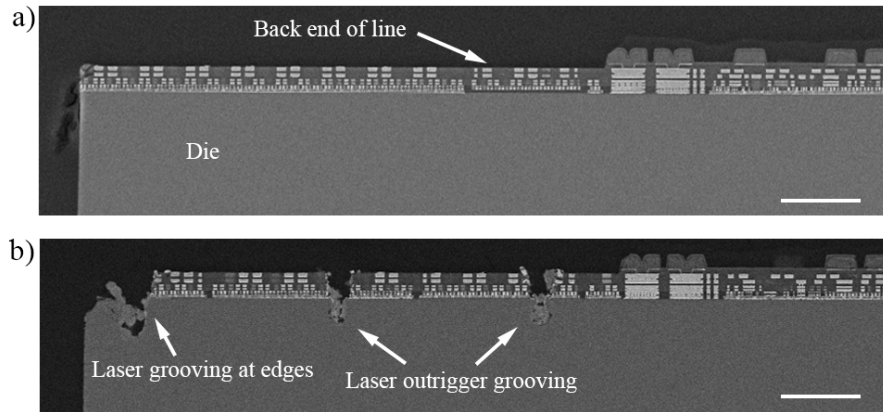


Figure 5.3 Cross-sectional images perpendicular to the chip edges and along the first row of solder connections on (a) cell 1 without laser grooving at the chip edges and without laser outriggers and (b) cell 3 with laser grooving at the chip edges and with laser outriggers. Scale bar lengths of $20\text{ }\mu\text{m}$.

Before performing the reliability tests, the samples were submitted to a JEDEC preconditioning level 3 [213], which is 30°C and 60% relative humidity for 192 hours. Then, the samples were subjected to a deep thermal cycling (DTC) test [13], with a temperature cycles ranging from -55°C to 125°C for 1000 cycles. The ramp rate was $15^{\circ}\text{C}/\text{minute}$, and the

soak time was 5 minutes at the maximum and minimum temperature. One or two samples were withdrawn every 250 cycles from each cell for detailed destructive characterization.

5.5.2 Characterization Methods

In order to detect the underfill delamination and cracks, several characterization methods were used. For a large delamination on the flat interface, scanning acoustic microscopy (C-SAM) was applied to scan the whole die area. The frequency of the C-SAM transducer was 100 MHz. As the acoustic waves scattered at the chip edges, infrared (IR) microscopy was also applied to observe the chip corner areas at higher resolution,. After 500 DTC cycles, one sample from cell 4 was cut in cross-sections to observe the crack trajectories in the bulk of the underfill. The cutting planes were perpendicular to the die diagonal, from the underfill fillet to the die crack-stop line, as shown in Figure 5.4. Scanning electron microscopy (SEM) was used to capture the cross-sectional images, using secondary electrons and with a voltage of 15.0 kV. The first cross-sectional position was captured by optical microscopy with a resolution of 1.5 $\mu\text{m}/\text{pixel}$.

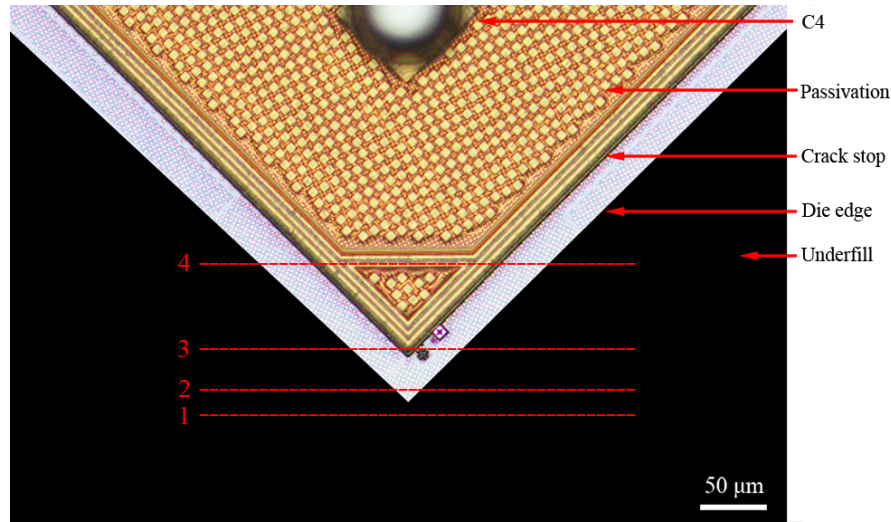


Figure 5.4 Location of cutting planes illustrated on the active side of a bare unpackaged die, for cross-sectioning.

5.6 Modeling

5.6.1 ANN Modeling of Delamination Initiation

The underfill delamination process was divided into an initiation step and a propagation step. The objective of the ANN model is to predict the numbers of cycles to delamination according to the five input variables. An artificial neural network (ANN) was used for the initiation step to link the input variables to the number of cycles to delamination. This method avoided the comparison between the calculated stress and a threshold stress

value to calculate the number of cycles to delamination, since such a threshold value is difficult to calculate from first principles. ANNs are a powerful tool to build input-output models of complex systems. In an ANN, a large number of hyper-parameters provide enough degrees of freedom to produce a generative function that can be used to predict the output. Thus, ANN can be used to fit and predict certain metrics in a complex system, such as the initial moment of delamination in the flip-chip package. A common ANN structure for non-linear prediction is a multi-layer perceptron architecture trained with error back propagation [214]. During the training procedure, the back-propagation (BP) algorithm is used to update the ANN weights based on the gradient descent learning rule in order to minimize the training errors calculated by a loss function [215]. The mean square error (MSE) loss function was used in this work, with a regularization term given by the L2-norm (sum of squares) of the weights to avoid over-fitting. Due to the smallness of the dataset, the model could be more prone to overfitting than with a larger dataset. The coefficient of the regularization term is usually set from 0 to 0.1 in practice [216] and a larger coefficient could help better avoid the overfitting issue. Thus, this coefficient was set to 0.1 in this work. The training goal was to provide an accurate number of cycles to delamination output with multiple input variables. We used an ANN with one hidden layer, as shown in Figure 5.5. In the input layer, the five variables were considered as the input elements. These variables were encoded as binary values in the set $\{0,1\}$ (see Table 5.1). One hundred neurons were used in the hidden layer. The number of neurons was much larger than the number of input variables to provide sufficient model redundancy, while the L2-norm regularization term would help control over-fitting. The output was the estimated number of cycles to the first observation of delamination. The rectified linear unit (ReLU) was used as the activation function in the hidden layer.

The ANN model used the data in the training dataset to calculate an output value, and then updated the weights of each neuron by gradient descent to reduce the value of the loss function. When the value of loss function had decreased to a low enough threshold value (set to 10^{-2}), the model was considered to have completed its training. In this work, as the C-SAM inspection was performed every 250 cycles, the actual number of cycles to delamination (target value) for each cell was censored to an interval of 250 cycles. An algorithm named random-ANN is proposed to use the censored data in the ANN modeling, as Algorithm 1.

In this algorithm, each value of the number of cycles to first delamination in the target vector from the training dataset is randomly sampled from a uniform distribution from $N_i^{DTC} - 250$ to N_i^{DTC} cycles, where N_i^{DTC} is the first detectable moment of chip-underfill

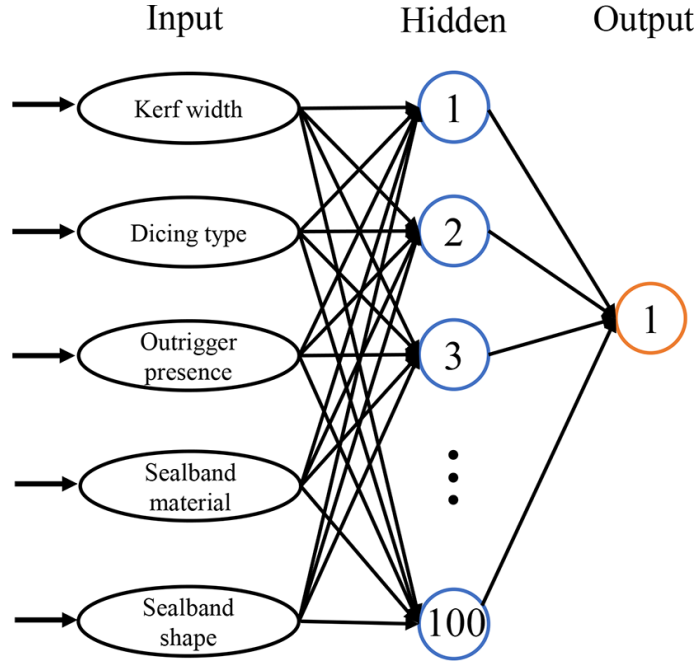
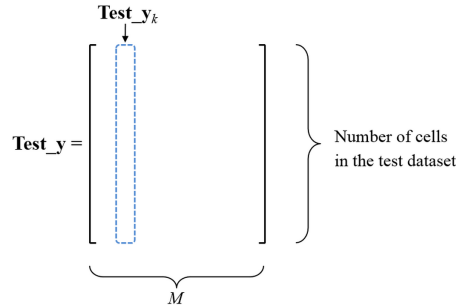


Figure 5.5 One hidden layer ANN architecture.

delamination for the i th cell by C-SAM, to account for the inspection censoring. M is the number of random samples and should be large enough to obtain stable histogram plots for statistical analysis. For k from 1 to M , multiple ANN models f_k are fitted to randomly sample the distribution of prediction values in the test dataset, relative to the uncertainty introduced by the inspection censoring. M affects the uncertainty of the predicted mean. A larger M helps to reduce the confidence interval of the predicted mean, but consumes more computing resources (the confidence interval scales like $1/\sqrt{M}$). When M is set to 100 and the standard deviation of the predicted distribution is less than 100 cycles (as shown later in Table IV), the 90% two-sided confidence interval for the predicted mean is less than 16 cycles based on the t-distribution. The whole ANN model was built and trained under the Pytorch framework [217].

A leave-one-out cross validation (LOOCV) analysis was also performed on 8 cells (number 1, 2, 3, 4, 6, 8, 10 and 12) to select the cells in the training dataset. This analysis was called the 'train-test partitioning analysis' and this dataset of 8 cells was called the 'LOOCV dataset'. The cells with large LOOCV errors were assigned to the training dataset in the complete analysis, since their features cannot be learned from the other cells. The other cells (number 5, 7, 9, 11 and 13) were not considered in the LOOCV due to unexpected failure modes. In the LOOCV dataset, one cell was chosen as the test dataset and the remaining cells were in the training dataset. The LOOCV results will be presented in section 5.7.1. The partitioning of the training and test datasets for the complete analysis,

Inputs:	
N_i^{DTC}	Number of cycles at which the first delamination was detected by C-SAM for the i th cell.
Train_x , Test_x	Input matrix of the training and test datasets. The i th row corresponds to the i th cell, with its j th entry being a binary value for the corresponding input variable.
n	Number of cells in the training dataset.
M	Number of random samples (set to 100).
α	Constant coefficient in the loss function (set to 0.1).
Algorithm 1:	
1:	Split the dataset into the training and test datasets.
2:	$k = 1$
3:	While $k \leq M$:
	Sample each item in the target vector Train_y _{k} from a uniform distribution $U(N_i^{DTC} - 250, N_i^{DTC})$.
	Fit an ANN model f_k on $\{\mathbf{Train_x}, \mathbf{Train_y}_k\}$, by minimizing the loss function:
	Loss = $\frac{1}{n} \ \mathbf{Train_y}_k - f_k(\mathbf{Train_x})\ _2^2 + \alpha \ \mathbf{w}\ _2^2$
	where \mathbf{w} is the weight vector of the ANN model and $\ \cdot\ _2$ is the L2 norm.
	Predict the vector $\mathbf{Train_y}_k = f_k(\mathbf{Train_x})$.
	$k = k + 1$
	End While
4:	Concatenate the Train_y _{k} vectors to obtain a matrix Train_y . The rows correspond to the different cells and the columns to the different random samples for the censored number of cycles to first delamination.



obtained from the LOOCV, is shown in Table 5.1. The training dataset contained cells number 1, 3, 4, 5, 8, 10 and 12, while the test dataset contained cells number 2, 6, 7, 9, 11 and 13.

A common approach to partition the dataset between a training dataset and a test dataset is to randomly assign 80% of the samples to the training dataset and 20% to the test dataset, without any common items shared by both datasets. However, in our analysis the cells 2 and 6 are used in the LOOCV to partition the complete dataset into the training and test datasets, and in the complete analysis using these two datasets. Thus, the cells 2 and 6 in the test dataset are not statistically independent from the other cells in the training dataset. This lack of independence is the result of the train-test partitioning

Table 5.1 Input variables encoded as binary values in the set $\{0,1\}$ for each test cell and the dataset partitioning of the cells

Cell	Kerf width (0) Large - 300 μm (1) Small - 100 μm	Dicing type (0) Blade dicing (1) Laser grooving + blade dicing	Laser presence (0) No Outrigger (1) Laser outrigger	Sealband material (0) high modulus (1) Low modulus	Sealband shape (0) C-Shape (1) 4 lines-shape	LOOCV dataset	Training dataset	Test dataset
1	0	0	0	1	0	✓	✓	
2	0	1	0	1	0	✓		✓
3	0	1	1	1	0	✓	✓	
4	1	0	0	0	0	✓	✓	
5	1	0	0	0	1	✓	✓	
6	1	1	0	0	0	✓		✓
7	1	1	0	0	1			✓
8	0	0	0	0	0	✓	✓	
9	0	0	0	0	1			✓
10	0	1	1	0	0	✓	✓	
11	0	1	1	0	1			✓
12	0	1	0	0	0	✓	✓	
13	0	1	0	0	1			✓

analysis and is different from the training sample leakage (items repetition between the training and test datasets), because no cell was directly duplicated between the training and test datasets. However, the prediction errors for the outputs of cells 2 and 6, that is, the proportions of model outputs falling outside the intervals of experimental observations, might still be underestimated, because the selected training dataset already contains the features of cells 2 and 6 according to the train-test partitioning analysis, which by design produces a trained model that always produces a lower error output for cells 2 and 6.

The LOOCV dataset was used instead of the test dataset in the validation of the delamination growth model (presented in section 5.6.2), because the cells in the test dataset could not all be used to validate the delamination growth model. In the test dataset, cells 7, 9, 11 and 13 were not inspected by C-SAM after 250 cycles due to unexpected failure modes and were not available for the validation of the delamination growth model. The occurrences of delamination for cells 2 and 6 were both in the interval from 750 to 1000 cycles. The delamination growth model also had to be validated according to cells with initial delamination before 750 cycles. In the LOOCV dataset, cells 8 and 12 were observed to have delamination before 750 cycles, and their areas of delamination were also measured by C-SAM. So, the predicted numbers of cycles to delamination for cells in the LOOCV dataset were used as the initial moments in the delamination growth model.

The predictions for cells in the LOOCV dataset were not statistically independent from each other and this lack of independence might affect the prediction accuracy on the number of cycles to delamination for some cells. A method was therefore required to evaluate the prediction accuracy for each cell in the LOOCV dataset. This is because for two different left-out cells, their models were trained with 7 cells, where 6 out of these 7 cells were the same. The effect of this lack of independence on the prediction accuracy will be quantitatively evaluated as follows. As the experimental number of cycles to delamination was censored to an interval, the difference between the experimental and predicted numbers of cycles to delamination could not be obtained directly. The random-ANN was applied to predict the number of cycles to delamination for each cell in the LOOCV dataset. The random-ANN output for each cell was a distribution of the number of cycles to delamination for that cell. The proportion of number of cycles from this distribution located in the experimental censored intervals was thus used as a metric to evaluate the prediction accuracy. This metric was named the 'overlap fraction'. If the overlap fraction was over 0.5, the predicted distribution could be considered a good match with the experimental censored interval. Table 5.4 summarizes the averages and standard deviations of the number of cycles to delamination predicted by the random-

ANN, the number of cycles to initial delamination determined by experiments, and the overlap fractions, for cells in the LOOCV dataset.

5.6.2 Finite Element Models

Meshing and Boundary Conditions

The objective of this section is to calculate the delamination areas as a function of DTC cycles, and to validate the result using C-SAM observations. After estimating the initial moment of delamination by an ANN, an efficient Python-based custom software named PACK [177] was used to construct the flip-chip model. The model was quarter-symmetric for the 4 lines-shape sealband configuration, with the same geometry as the experimental sample (macro-model), as shown in Figure 5.6. The symmetry plane boundary condition shown in Figure 5.6b implies that the displacements normal to the plane of symmetry and rotations about axes in the plane of symmetry are zero. The C-shape sealband configuration could not be simplified to a quarter-symmetric model, so it was analyzed in a full model. The material properties and the dimensions of each component are summarized in Table 5.2. As the die corner is usually the position with the highest level of stress, it is necessary to use a submodeling technique focusing on the chip corner area with a detailed mesh to achieve accurate results. Figure 5.7 shows the configuration of the submodel at the chip corner. The exterior profile of the underfill fillet was approximated by a power-law function, which closely matched the true fillet geometry (see Figure 5.7c). The chip corner was enclosed in the underfill and the fillet. The cut-boundary displacements from the macro-model were transferred to the submodel as an input condition. The reference temperature (with zero thermal strain) was set at 150°C for both the macro model and the submodel, as the underfill was cured at this temperature. The model actual temperature was set at -55°C, which was the lowest temperature during the DTC test. When the temperature was below the stress-free temperature, thermal strains were induced in the underfill. All of the elements were linear, with the total number of elements of 172264 for the macro-model, and 57624 for the submodel. For the macro model, the minimum and maximum element sizes were $75 \times 75 \times 20 \mu\text{m}^3$ and $200 \times 200 \times 220 \mu\text{m}^3$. For the submodel, the minimum and maximum element sizes were $10 \times 10 \times 10 \mu\text{m}^3$ and $40 \times 40 \times 50 \mu\text{m}^3$. All of the elements in the submodel were hexahedral elements, while the macro model had tetrahedral and wedge elements in the underfill fillet. The simulations were performed by the ANSYS software [112].

Underfill Delamination Model

The simulation of delamination at the chip-underfill interface was carried out with 8-node linear interface elements between the chip and the underfill, as shown in Figure 5.8. The

Table 5.2 Material properties and dimensions in models

Component	Die [90]	Underfill	Substrate laminates	Substrate core layer	TIM	Lid [39]	Sealband (Low modulus)	Sealband (High modulus)
Young's Modulus (GPa)	120	10/0.15	9	27	0.01	117	3.9×10^{-3}	4.8
CTE (ppm/°C)	2.6	25/92	20	11	14	16	275	50
Poisson ratio	0.35	0.3	0.27	0.35	0.35	0.33	0.35	0.35
T_g (°C)	N/A	100	176	205	N/A	N/A	N/A	N/A
K_{Ic} (MPa·m ^{0.5})	N/A	2.3	N/A	N/A	N/A	N/A	N/A	N/A
Thickness (mm)	0.75	0.06	0.33	0.4	0.1	1.0	0.15	0.15
Length (mm)	25	N/A	55	55	25	41.5	41.5	41.5
Width (mm)	25	1.5	55	55	25	51.4	3.0	3.0

node pairs along the thickness direction (I, M), (J, N), (K, O) and (L, P) were initially coincident. The interface separation between the chip and the underfill was represented by an increased displacement between node pairs within the interface element [112]. The strain energy at the interface elements was used as the metric to estimate the interfacial damage.

To perform the simulation of interfacial delamination during thermal cycling, the rules for interfacial delamination need to be determined first. As the endurance limit (minimum stress to drive fatigue cracks) of engineering polymers and composites is observed to be around 30% of their ultimate stress [218], a threshold value $u_{m}athrm{mc}$ on the strain energy amplitude could be determined from the endurance limit and further implemented into the model. In this work, the ultimate stress σ_s for the underfill was first estimated by

$$\sigma_s = \frac{K_{Ic}}{\sqrt{2\pi l_e}}, \quad (5.1)$$

where K_{Ic} is the mode I fracture toughness of the underfill (see Table 5.2) and l_e is the characteristic length (125 μm) for the interface elements. Then, the threshold value u_c was determined by

$$u_c = \frac{\sigma_c^2}{E} l_e, \quad (5.2)$$

where u_c is 30% of σ_s and E is the elastic modulus of the underfill. l_e is determined by the average length and width of the interface elements and is equal to 125 μm . The threshold value u_c was thus 8×10^{-3} MPa·mm. As the chip-underfill delamination was a cohesive fracture (discussed later with Figure 5.15), the delamination fluctuated between the interface and the bulk of the underfill. This phenomenon suggests that the interfacial adhesion was good [34] and the delamination path was mainly in the bulk underfill near the interface rather than at the interface. The strain energy in the underfill near the interface should therefore be used as the criterion for the growth of delamination. In this

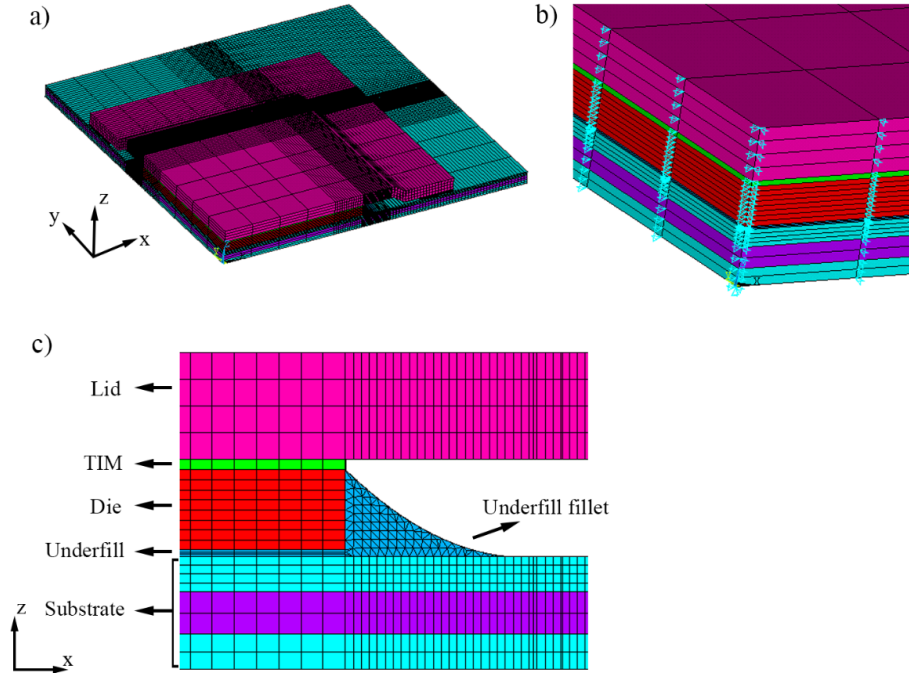


Figure 5.6 Macro-model, (a) global quarter-symmetric view, (b) symmetry plane boundary condition at the planes of symmetry, (c) cross-section view in the xz -plane.

case, it is thus appropriate to use the underfill bulk material properties to calculate the interfacial strain energy [65].

To realize the modeling of chip-underfill interface delamination, the strain energy amplitude for each interfacial element of interfacial area l_e^2 were evaluated by an iterative finite element method. In each iteration, the temperature was set to -55°C and the strain free temperature was 150°C . The calculated strain energy amplitude of each interface element was compared with u_c . If the strain energy amplitude of any interface element was above u_c , the interface element was set to have zero elastic modulus (disabled) for all following iterations, indicating delamination in this area. Otherwise, the interface element was not modified. The delamination areas as a function of the number of finite element model iterations could thus be obtained.

In order to relate the number of finite element model iterations and the number of DTC cycles, an adjustable parameter N^c was defined as the equivalent number of DTC cycles per model iteration. N^c was fitted to the experimentally observed delamination areas in cell 8, because: 1) the delamination areas were large enough in that cell (larger than the delamination area of a single iteration of the model) to fit N^c ; 2) the delamination areas of cell 8 were obtained experimentally at both 250 cycles and 500 cycles, while other cells

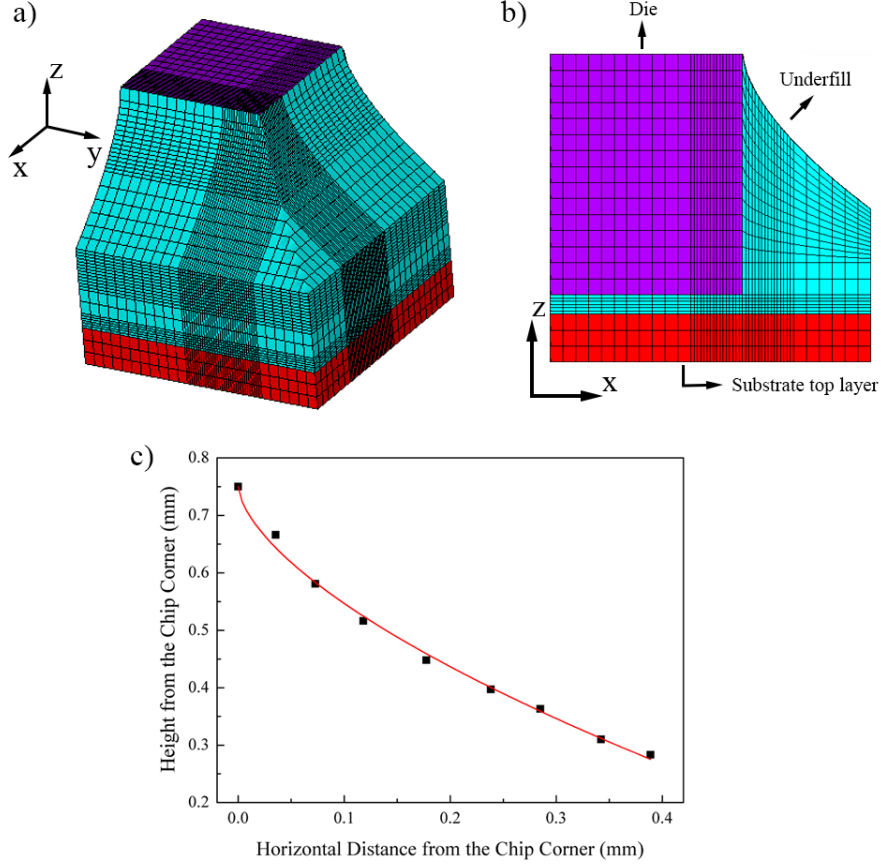


Figure 5.7 Submodel configuration, (a) global view, (b) cross-sectional view on the xz-plane at the chip corner area, (c) profile of the underfill fillet obtained by experiment (square markers) and the fitting curve by a power-law function (solid line).

had available delamination areas only at one moment (either 500 cycles or 1000 cycles) of C-SAM inspection. These two conditions made cell 8 more suitable to fit N^c than other cells. As the delamination growth model only accounts for the period after the initial delamination, N^c is defined by

$$N^{\text{delam}} - N_0^{\text{delam}} = N^c \cdot n^{\text{iter}}, \quad (5.3)$$

where for a delamination area A measured by C-SAM after N^{delam} DTC cycles, N_0^{delam} is the initial moment of delamination that was unobserved but lies within the 250-cycle interval before first observation of delamination by C-SAM (for cell 8, N_0^{delam} is between 0 and 250 cycles), and n^{iter} is the number of finite element model iterations when the calculated delamination area reaches A . n^{iter} is obtained by a linear interpolation between the delamination areas and the number of model iterations. As N_0^{delam} was not observed,

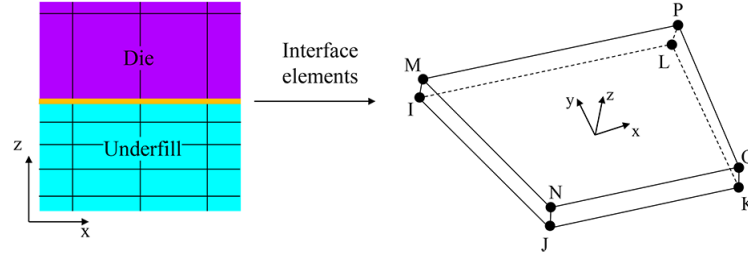


Figure 5.8 Geometry of an interface element. [112]

it was assumed to have a uniform distribution from 0 to 250 cycles. N_0^{delam} was assigned to 125 cycles, because this value is the median of the uniform distribution from 0 to 250 cycles. At $N^{\text{delam}} = 125$, 250 and 500 cycles, n^{iter} was equal to 0, 6.6 and 12.8 model iterations, respectively. N^c was fitted linearly by the least squares method from these three points. Following Equation 5.3, the fit was forced to go through $n^{\text{iter}} = 0$ iterations and $N^{\text{delam}} = 125$ cycles. A value of $N^c = 27$ DTC cycles per finite element model iteration was finally obtained.

Then, the delamination area as a function of DTC cycles could be obtained by multiplying the number of finite element model iterations with N^c , and adding the number of cycles to first delamination estimated by the random-ANN model. The area of delamination for up to 432 cycles from the initiation was estimated by the FEM model with 16 calculation iterations described above. Cells in the LOOCV dataset (number 1, 2, 3, 4, 6, 8, 10 and 12) were then used to evaluate the growth curves of the delamination areas. The other cells (number 5, 7, 9, 11 and 13) were not used for the prediction of the delamination areas due to unexpected failure modes (sealband cracking and delamination) after 250 cycles. The comparison between the measured and predicted delamination areas will be presented in section 5.7.2 as well.

Underfill Cracking Model

The objective of underfill crack modeling is to obtain the correct crack trajectories, as validated by the cross-sectional images. The crack propagation simulation was carried out by the extended finite element method (XFEM) with phantom nodes. The principle and advantages of this method have been introduced in our previous work [184]. In particular, local mesh refinement and updates are not required during the calculation. Figure 5.9 shows the initial crack setup for the diagonal crack and one edge crack. The diagonal crack was perpendicular to the xy-plane with a 45° angle from the x-axis. One edge crack was perpendicular to the xz-plane with a 45° angle from the x-axis, while the other edge crack was in a symmetric position with respect to the 45° diagonal plane. As the initial cracks position were limited by the software to not be across the nodes, the diagonal crack

and edge cracks were positioned 1/4 length and 1/4 height of the element away from the corner node, respectively. As each element can only be cracked once in the modeling, the two edge cracks were also placed one element away from the corner. Then, the model was subjected to cooling from 150°C (stress free temperature) to -55°C (actual temperature). The criterion of maximum hoop stress was used as the crack propagation criterion [112], by evaluating the maximum value of the hoop stress σ_θ around the crack tip at a radius of 40 μm . The crack was propagated along the direction of maximum value of σ_θ when it reached a threshold value σ_{th} . To determine the σ_{th} , the ultimate value of hoop stress is first obtained from

$$\sigma_{\text{max}} = \frac{K_{\text{Ic}}}{\sqrt{2\pi r}}, \quad (5.4)$$

where K_{Ic} is the mode I fracture toughness of the underfill, and r is the distance ahead of the crack tip (40 μm , the maximum side length of the underfill elements). σ_{max} represents the highest hoop stress that the underfill can support around the crack tip at a radius of r . The threshold value σ_{th} was then set at 30% of σ_{max} to obtain crack propagation in a static cooling process instead of a cyclic thermal loading, for the same reason as in the delamination model. Thus, this threshold value could be applied to estimate the directions of cracks propagated in the underfill. The stress intensity factor and the energy release rate were not used as the fracture criterion because they could not be used to determine the crack directions. As the cross-sectional characterization was only performed on cell 4 at 500 cycles, the initiation moment and the growth rate of the underfill cracks could not be quantified from our experiments. Thus, the purpose of crack modeling in this work was to determine the direction of each crack rather than their lengths with respect to the number of cycles. The modeling of fatigue crack growth (crack length vs. number of cycles) would be possible in future work if the crack locations could be monitored periodically.

Mesh Size Sensitivity Tests

The accuracy of finite element results can be affected by the element size [219–221]. In order to analyze the sensitivity of the model to the element size presented in section 5.6.2, the overall element size of the model was modified to 0.75 \times and 1.5 \times the original sizes. Figure 5.10 shows the z displacement at the chip-underfill interface along the diagonal direction from the chip center to the chip corner, when the actual temperature was -55°C (stress free temperature at 150°C). Compared with the original element sizes (ratio 1), the maximum z displacements at the chip corner of the models with 0.75 \times and 1.5 \times original element sizes were very close, with a relative error of less than 0.5%. In a cylindrical coordinate system centred at the chip corner, Figure 5.10 shows the hoop strains ϵ_θ in the underfill along the diagonal direction in the submodel, which is from the chip corner in

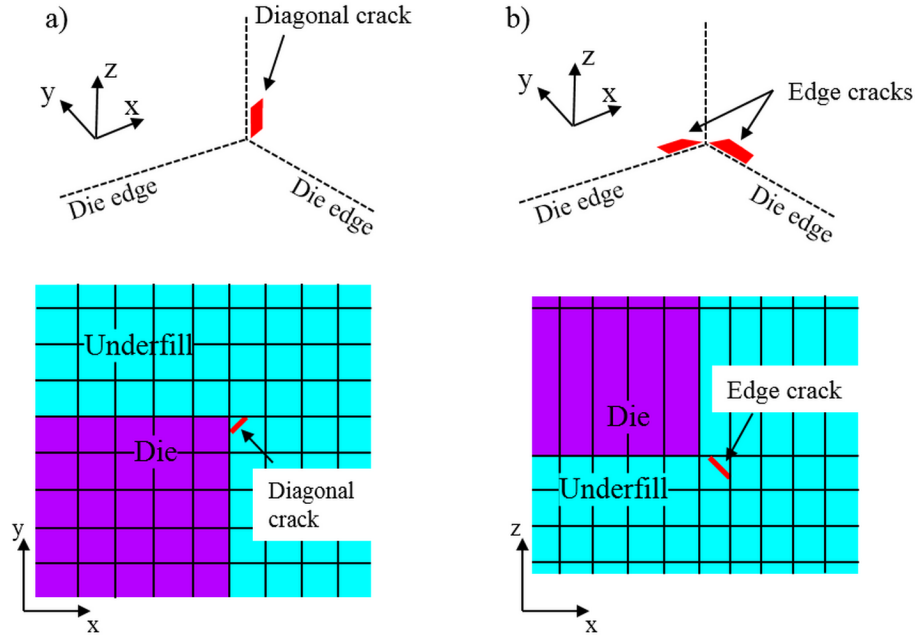


Figure 5.9 Setup of (a) the diagonal initial crack with a cross-sectional view on the xy-plane and (b) the edge initial crack with a cross-sectional view on the xz-plane.

the xy-plane with a 45° angle from the x-axis. The relative errors for the maximum hoop strains were only 2.2% and 8.2% for the models with $0.75\times$ and $1.5\times$ original element sizes, respectively. Therefore, models with the original element sizes could achieve robust results for the present simulation.

5.7 Results and Discussion

5.7.1 Initiation of Chip-Underfill Delamination

The chip-underfill delamination area is one of the important metrics for evaluating the underfill reliability. Table 5.3 summarizes the average delamination areas for all cells inspected by C-SAM, where N/A indicates that no C-SAM inspections were performed. Because cracked electrodes were found under the sealband in cells 7, 9, 11 and 13 (unexpected failure mode and not in the scope of this work), the inspections on chip-underfill delamination at or after 500 cycles were not performed in these cells. Measurable chip-underfill delamination areas were first observed in cell 8 after only 250 cycles. Cells 1, 2, 4 and 10 had detectable chip-underfill delamination areas at 1000 cycles as well. Figure 5.12 shows a typical C-SAM observation for cell 4 at 250, 500 and 1000 cycles. The delaminated areas were all located near the corner of the die, in all cells. In addition, a large crack on

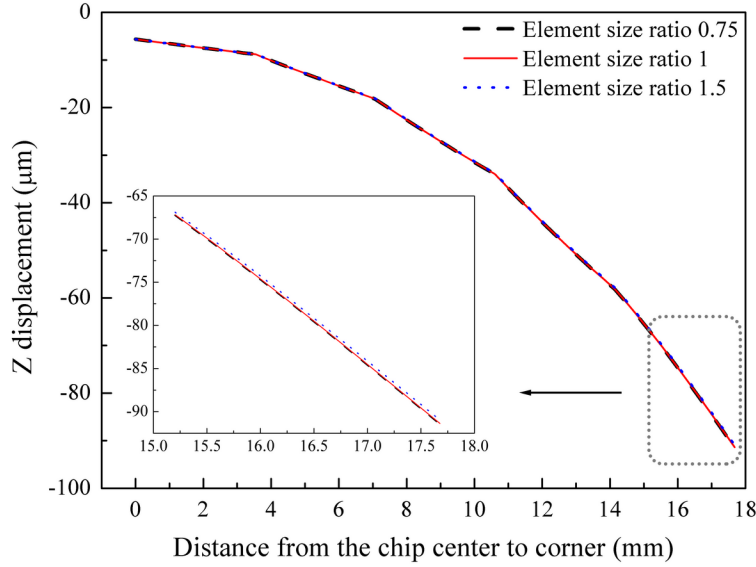


Figure 5.10 Z displacement of the chip-underfill interface from the chip center to the chip corner in the macro model.

the die was observed in Figure 5.12d; similar cracks were also observed after chip-underfill delamination in cells 6, 8 and 12.

Using the C-SAM delamination data, the random-ANN model was first applied to estimate the number of cycles to first delamination. Figure 5.13 shows a typical convergence curve of the MSE loss function during the training of the ANN. The MSE decreased steadily and reached a threshold of 10^{-2} at 10,000 iterations, when training was stopped. The convergent nature of the MSE means that the fitting inaccuracy was kept at a low level. However, the initial weights of each neuron (sampled from a uniform distribution from -0.17 to 0.17 by Kaiming initialization [222]) might have had an impact on the generation of the final model. Before performing the random-ANN modeling, the effect of initial weights was examined with a fixed target value ($N_i^{DTC} - 125$) for each cell, which is the mean of the uniform distribution from $N_i^{DTC} - 250$ cycles to $N_i^{DTC} - 125$ cycles. This resulted in a standard deviation over different choices of the initial weights for each prediction in the LOOCV dataset that was less than 25 cycles. Thus, the ANN model used in this work was reasonably insensitive to the initial weights.

Then, using Algorithm 1, the LOOCV was first performed on the LOOCV dataset to select the cells with the necessary features for the training dataset of the complete analysis. Table 5.4 shows the average and standard deviation of the predictions by the LOOCV. To quantitatively evaluate the performance of the model in LOOCV, an overlap fraction was calculated as the proportion of ANN predictions located in the intervals of experimental

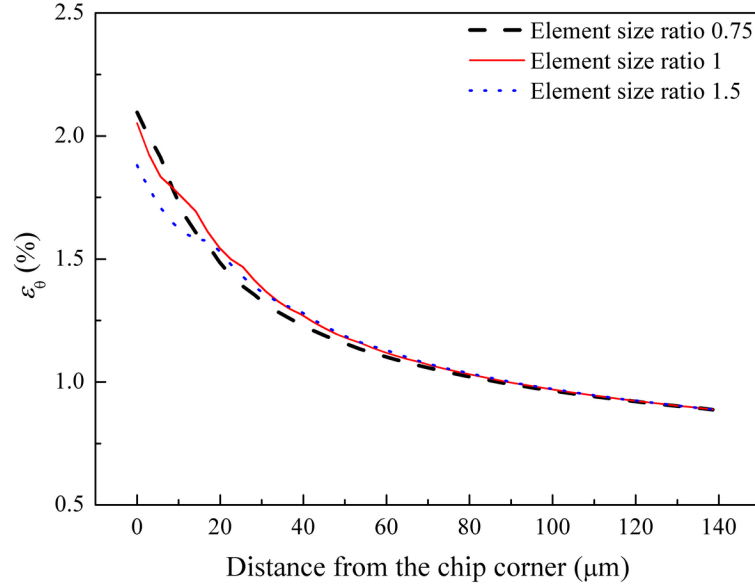


Figure 5.11 Underfill hoop strain with respect to the distance from the chip corner in the xy-plane with a 45° angle from the x-axis in the submodel.

observations. The predictions for cells 2, 3, 6 and 12 were mainly located in the interval of experiments, with overlap fractions over 0.7. The predicted average numbers of cycles to delamination for cells 1, 4 and 10 were within 150 cycles from the left boundary of their experimental intervals of initial delamination, with small overlap fractions less than 0.15, indicating relatively low accuracy. The prediction for cell 8 was the only one that not in agreement with the experimental data, with the random-ANN failing to predict the experimentally observed early failures. This shows that, in such a small dataset, cells 1, 4, 8 and 10 were necessary in the training dataset, because they have features that could not be learned from other cells.

After the LOOCV, cells 1, 3, 4, 5, 8, 10 and 12 were assigned to the training dataset and cells 2, 6, 7, 9, 11 and 13 were assigned to the test dataset for the complete analysis (see Table 5.1). Using Algorithm 1, the prediction distributions for the test dataset were statistically analyzed to show the effect of random sampling on the number of cycles to first delamination. Figure 5.14 shows the distribution of the number of cycles to delamination estimated on the test dataset, where the density is estimated by the number of samples in each bar divided by the product of the total number of samples and the bar width. All these distributions were approximately Gaussian, without significant skews or separated peaks. The average number of cycles to delamination for cell 2 and cell 6 were 842 cycles and 918 cycles. The corresponding C-SAM results in Table 5.3 for cell 2 show a first delamination at 1000 cycles, consistent with the prediction of 842 cycles for that cell. In

Table 5.3 Summary of delamination area at chip-underfill interface

Cell	Averages and 90% two-sided confidence intervals of delamination areas over each inspected component and each corner (mm ²)			
	DTC 250	DTC 500	DTC 750	DTC 1000
1	0	0	N/A	8.7
2	0	0	N/A	5.6
3	0	0	N/A	0
4	0	0	N/A	12.7 and die crack
5	0	N/A	N/A	0
6	0	0	N/A	Die crack
7	0	N/A	N/A	N/A
8	10.3	14.5	N/A	Die crack
9	0	N/A	N/A	N/A
10	0	0	N/A	0.8
11	0	N/A	N/A	N/A
12	0	10.2	N/A	Die crack
13	0	N/A	N/A	N/A

Table 5.4 Leave-one-out cross validation results

Cell	Number of cycles to delamination			
	ANN		Experiments	Overlap fraction
	Average	St. dev.		
1	611	73	(750,1000]	0.06
2	866	79	(750,1000]	0.86
3	1298	90	> 1000	1
4	651	86	(750,1000]	0.14
6	926	97	(750,1000]	0.74
8	527	73	(0,250]	0
10	621	63	(750,1000]	0.06
12	474	66	(250,500]	0.71

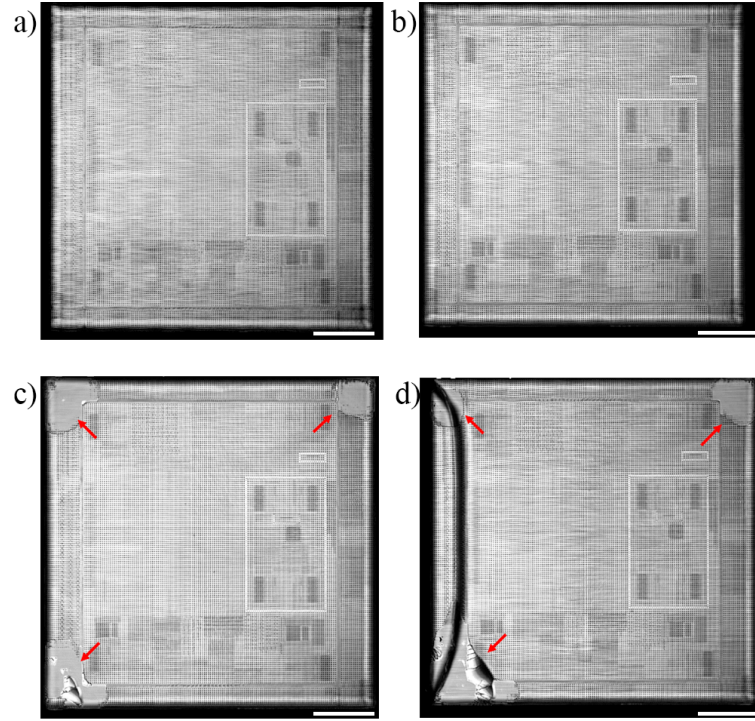


Figure 5.12 C-SAM images on cell 4 at (a) 250 cycles, (b) 500 cycles, (c) 1000 cycles and (d) 1000 cycles with a crack on the die. Scale bar lengths of 4 mm.

cell 6, a die crack was observed at 1000 cycles. Unlike cells 4, 8 and 12 exhibiting die cracks after initial delamination, the C-SAM did not reveal any delamination in cell 6. Because of possible scattering of acoustic waves at the edges, detailed images were further obtained by IR microscopy at each corner of the sample with a die crack in cell 6, as shown in Figure 5.15. At the northwest and southwest corner, two small delaminated regions of less than 0.01 mm^2 were observed. This demonstrates that the initial moment of delamination on cell 6 occurred just before 1000 cycles, consistent with the ANN prediction. The different brightness in the delaminated areas also indicates that the chip-underfill delamination did not remain at the same depth, but rather fluctuated between the interface and the bulk of the underfill. The delamination located in the bulk of the underfill near the interface is known as a cohesive fracture and was also observed in references [34, 75]. The predicted average number of cycles to delamination for cells 7, 9, 11, 13 were 877, 310, 722 and 356 cycles, respectively. As no delamination were observed in C-SAM at 250 cycles, the predictions of the random-ANN model were consistent for cell 7, 9, 11 and 13. As delamination data were not available after 250 cycles for these cells, the predictions of the random-ANN could not be further verified.

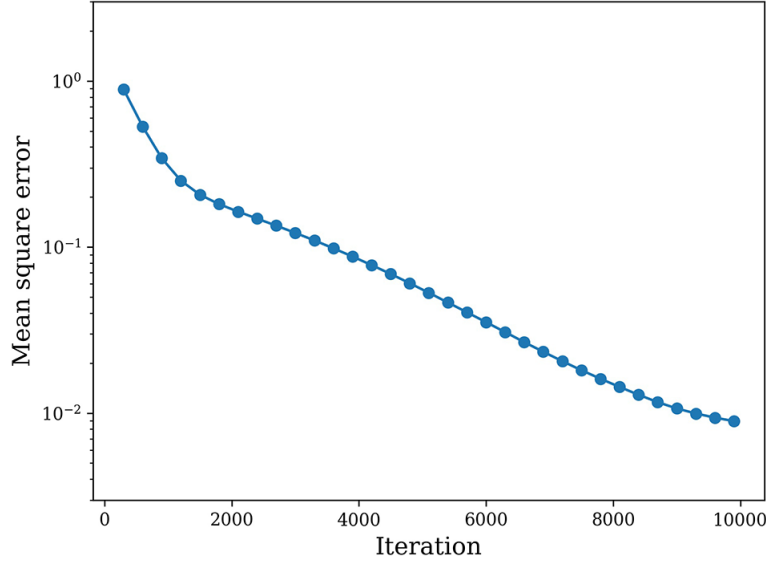


Figure 5.13 Typical convergence curve of the ANN model in 10,000 iterations.

To further improve the accuracy of ANN modeling for the number of cycles to first delamination, the volume of the dataset should be expanded. For example, a shorter period between C-SAM inspections could better capture the initial moment of delamination. In the current work, the predicted number of cycles to first delamination were in general agreement with the experimental results, but only after a careful partitioning of the training dataset and the test dataset. While this shows a good potential for the estimation of the number of cycles to first delamination, it is possible that this is the result of over-fitting the ANN model to the training dataset. Experiments with a larger quantity of data will be required to definitely resolve this issue.

5.7.2 Propagation of Chip-Underfill Delamination

After the estimation of the number of cycles to first delamination, the propagation of delamination at the chip-underfill interface was modelled. According to the method proposed in section 5.6.2, the value of N^c was 27 cycles for the value of u_c given in section 5.6.2. The progress of the delamination at the chip-underfill interface of the cell 4 is shown in Figure 5.16, which represents a total of 432 DTC cycles after the initiation of delamination. The delamination started at the die corner and quickly grew to the two adjacent edges, because the corner area had the highest stress and strain concentrations caused by the corner geometry and CTE mismatch between the underfill and die, while the stress and strain at the two adjacent edges had the second largest values [101]. Then, from Figure 5.16b to 5.16c, the delaminated areas in the corner region continued to grow towards the centre of the chip. Finally, the growth rate slowed down, since the strain energy had been mostly released. When focusing on the shapes of delamination, two typical shapes were

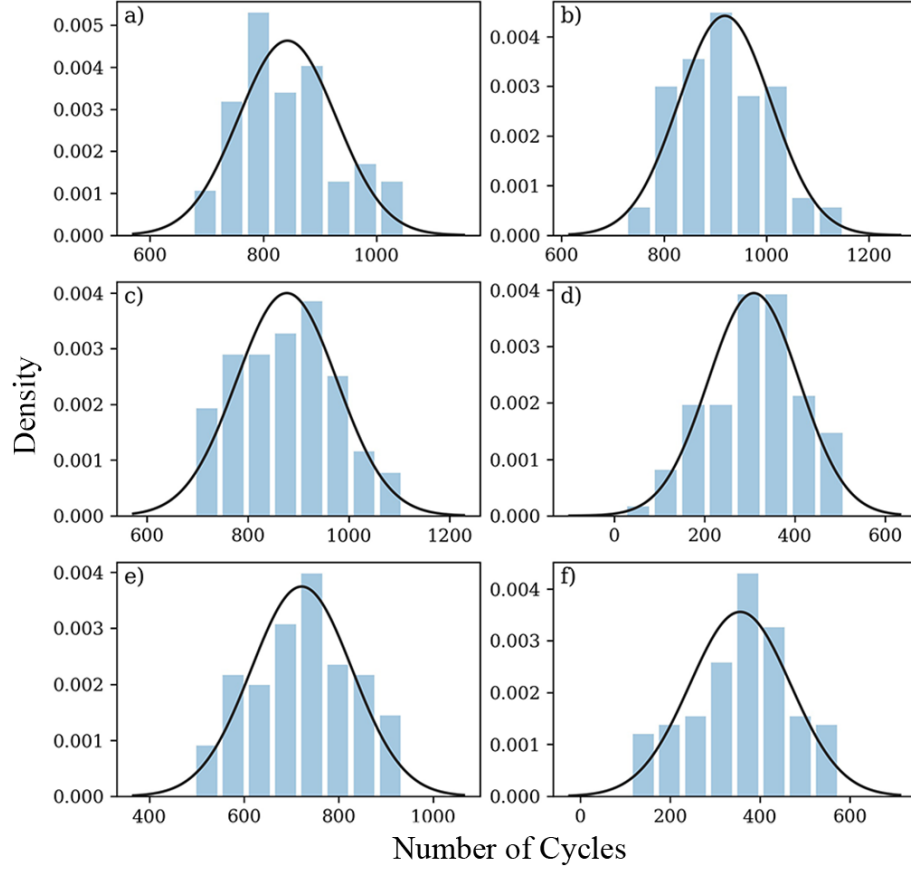


Figure 5.14 Distribution of predicted initial moment of delamination on the test dataset, (a) cell 2, (b) cell 6, (c) cell 7, (d) cell 9, (e) cell 11, (f) cell 13. The black curves represent fitted Gaussian distributions.

obtained in C-SAM observations, which were convex and concave (see Figure 5.17). In the convex delamination, the front of the delamination is almost circular, as observed in the northeast corner in Figure 5.12c and 5.12d. On the other hand, the concave delamination has a larger proportion of the delaminated area at the edge regions than the convex delamination, which as observed in the southwest corner in Figure 5.12c and 5.12d. In Figure 5.16, the simulation generated a concave delamination. In addition, the concave shape of delamination was also observed in references [38, 53, 223]. In general, the shape of chip-underfill delamination areas obtained in our model appears to be qualitatively consistent with observations and the literature. No significant correlation was found between the input values and the delamination shapes. In the C-SAM observations of the delaminated samples from cells 1, 2, 4, 8, 10 and 12, the convex delamination shapes appeared when the delamination areas were less than 4 mm^2 . With the increase of delamination areas, the delamination at the chip edge grew faster than in the chip central region and the delamination shape converted to concave. The mechanism of these two delamination

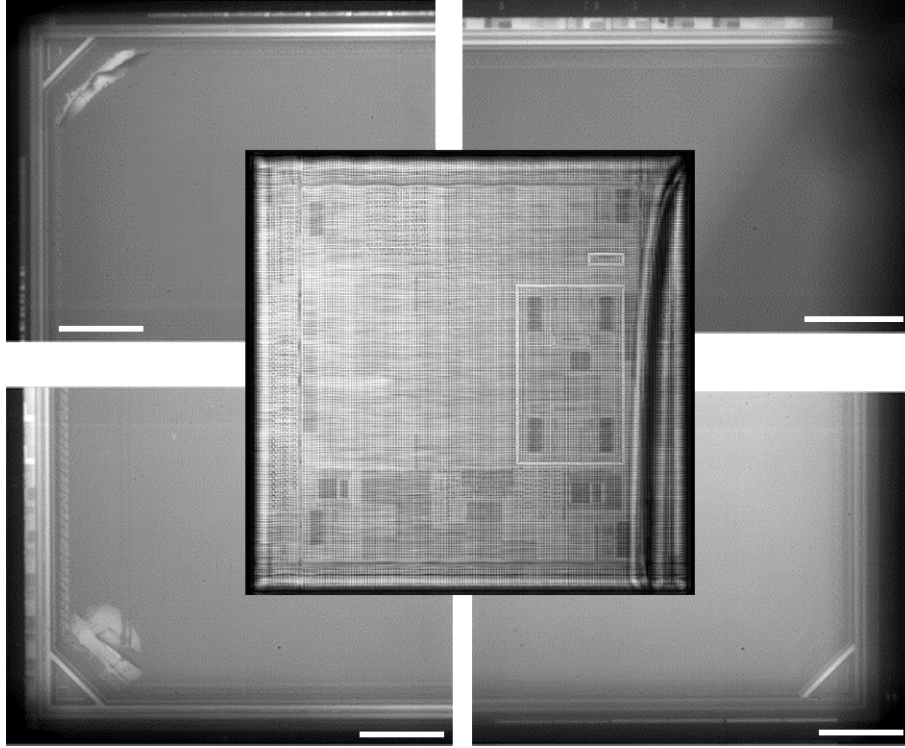


Figure 5.15 Infrared microscopy images at each corner of the sample with die cracks in cell 6. Scale bar lengths of 100 μm .

shapes may require further studies on the interfacial fracture properties near the chip edge and the chip central region. As a result, the total area of the delaminated regions was next considered as the primary metric in the following comparison between the experimental and numerical results.

To do so, the growth of delamination areas were determined by combining the number of cycles to first delamination obtained from the random-ANN predictions for the LOOCV dataset, and the propagation of delamination from FEM modeling. The reported areas of delamination were evaluated at the sum of the number of cycles to first delamination predicted by the random-ANN and the number of cycles used in FEM. Figure 5.18 shows the average delaminated areas per corner of the part of each cell extracted for the C-SAM inspections. The delamination area of each corner in the same specimen was used to calculate the two-sided 90% confidence interval based on the t-distribution. The curves are the predictions of the 1/4-symmetry FEM submodel, for the cells in the LOOCV dataset except for cells 3 and 8. Cell 3 could not be used for the comparison between experiments and simulations, because the initial delamination in both experiments and simulations did not occur until after 1000 cycles. No data on the areas of delamination could be used for the delamination growth model. As the cell 8 was used to estimate the value of N^c

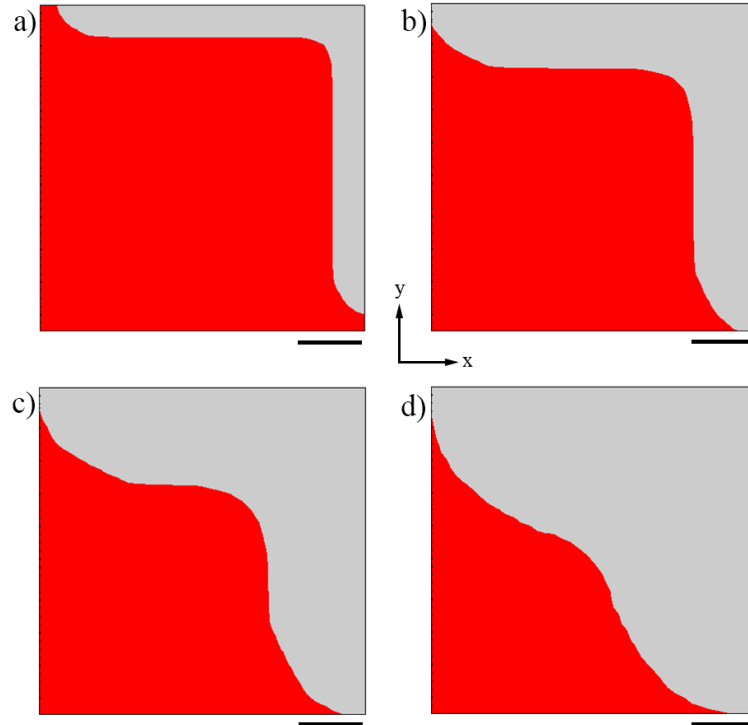


Figure 5.16 Propagation of a delamination from one die corner, located at the top right, (a) 108 DTC cycles, (b) 216 DTC cycles, (c) 324 DTC cycles, (d) 432 DTC cycles after the initiation of delamination. The gray areas represent delaminated zones. Scale bar lengths of 1 mm.

(equals to 27 cycles per iteration), it was not used to evaluate the prediction accuracy relative to experimental results. Cells 5, 7, 9, 11 and 13 were not in the LOOCV dataset and were not included in the comparison due to unexpected failure modes. The beginning of the delamination area growth for cells 1, 2, 4, 6, 10 and 12 were the average number of cycles to first delamination obtained by the LOOCV and the shaded areas in Figure 5.18 represent a variation of ± 1 standard deviation from the prediction average in each cell (see Table 5.4).

According to the prediction curves in Figure 5.18, the growth rate for each cell was generally fast in the first 200 cycles from the initiation of delamination and gradually slowed down in the later stages, which was reasonable due to the release of interfacial strain energy. When reaching the same delamination areas as measured by C-SAM, the difference between the predicted number of cycles and the C-SAM inspection moment was defined as the model error. The model errors were less than ± 100 cycles for cells 2 and 6, and less than ± 200 cycles for cells 4 and 12. For cells 1 and 10, the average predicted number of cycles were 220 and 350 cycles earlier than their C-SAM inspection moments, respectively. Due to the uncertainties introduced by the inspection censoring (250 cycles) in estimating

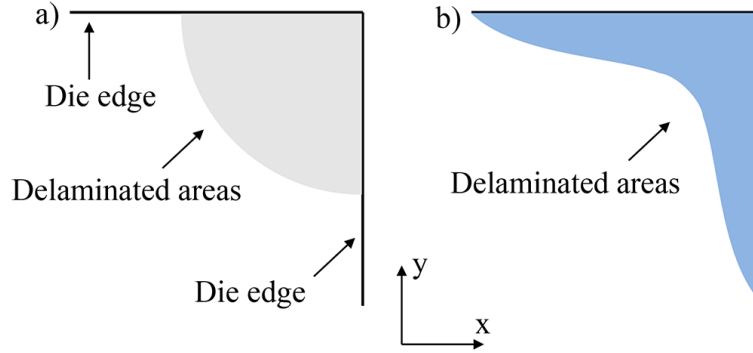


Figure 5.17 Typical shapes of the chip-underfill delamination areas: (a) convex shape and (b) concave shape.

the initial delamination, the model with an error of less than 250 cycles was still consistent with the experimental observations. Thus, by comparing the experimental and numerical results in all 6 cells, 5 out of 6 predictions are in good agreement with the experimental data, demonstrating a relatively good fit of the model to the data. Only the error in cell 10 was larger than the width of the censoring interval (250 cycles). These errors were mainly attributed to the underestimation of the number of cycles to first delamination (as seen in Table 5.4), indicating that the features of cells with large errors, such as the cell 10, cannot be learned from other cells. As described in section 5.6.2, the prediction curves in Figure 5.18 were obtained with a value of N^c equal to 27 cycles per iteration, as obtained for cell 8. If the value of N^c had instead been estimated using cells 1, 2, 4 or 12, similar conclusions as above would still have been obtained.

5.7.3 Underfill Cracking Angles

In addition to the chip-underfill interface delamination, the cracks in the bulk underfill were observed by successive cross-sectioning from the corner of the package. As the cracks in the underfill may grow to reach electrical components (solder joints, back-end of line and circuits in the substrate), leading to electrical failures, the accurate estimation of crack angle is the first step for modeling the crack growing from underfill to electrical components. Figure 5.19 shows four cross-sectional positions of a sample from cell 4 after 500 thermal cycles, corresponding to the dashed lines in Figure 5.4. A planar crack appeared from the die corner in Figure 5.19a, along a diagonal direction of 45° from the chip sidewall extensions (135° from the chip sidewall) and perpendicular to the plane of the laminated substrate. Then, Figure 5.19b to 5.19d reveal two cracks on both sides of the die. These two cracks are oriented towards the laminated substrate. In these cross-sectional images, the angle between the cracks and the chip sidewalls is 125° . Figure 5.20 presents a diagram of the right edge cracks observed in the cross-sectioning test planes (Figure

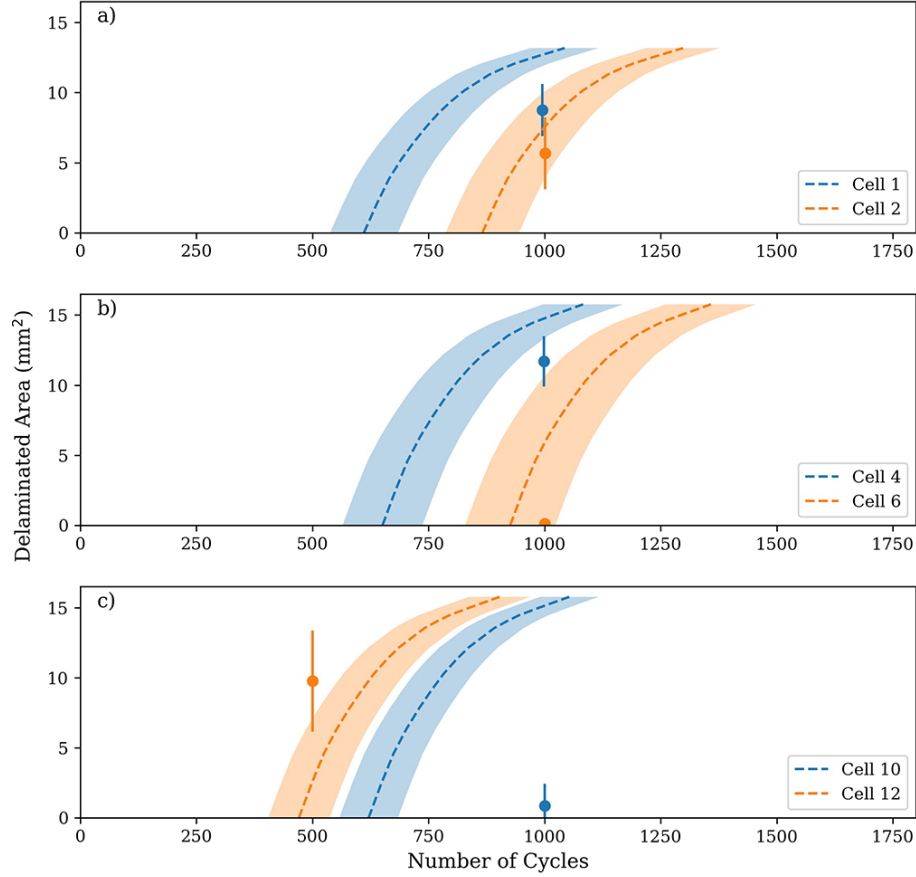


Figure 5.18 Delaminated areas at the chip-underfill interface as functions of thermal cycles obtained by the FEM model (lines) and the corresponding C-SAM results (round markers). Shaded areas represent ± 1 standard deviation from the ANN prediction average in each cell. Error bars represent two-sided 90% confidence intervals.

5.19). In order to quantitatively estimate the direction of the edge crack plane (ABCD), the normal vectors to the ABC, ABD, BCD and ACD planes were first obtained from the right edge crack locations in Figure 5.19c and 5.19d. Then, the average angles between the normal vectors and the x, y, z axes were estimated to be $(90.1 \pm 2.2)^\circ$, $(46.4 \pm 1.5)^\circ$ and $(43.6 \pm 1.6)^\circ$, respectively, where the uncertainties represent the two-sided 90% confidence intervals based on the t-distribution for the four planes. This demonstrates that the edge crack (ABCD) is approximately planar, mostly perpendicular to the yz plane and at $(135.0 \pm 2.9)^\circ$ to the chip sidewall. The direction for the left edge crack was similar. Similar cracks have not been reported in previous works. This may be the result of traditional cross-sectional characterizations that are usually oriented radially from the chip center and perpendicular to our cutting direction. Thus, a single radial cut may miss such edge cracks. The observed edge cracks did not reach the substrate and were 60 to 100 μm deep.

According to images on these four cutting positions, the paths of the diagonal and edge cracks were essentially planar, with no apparent change in direction.

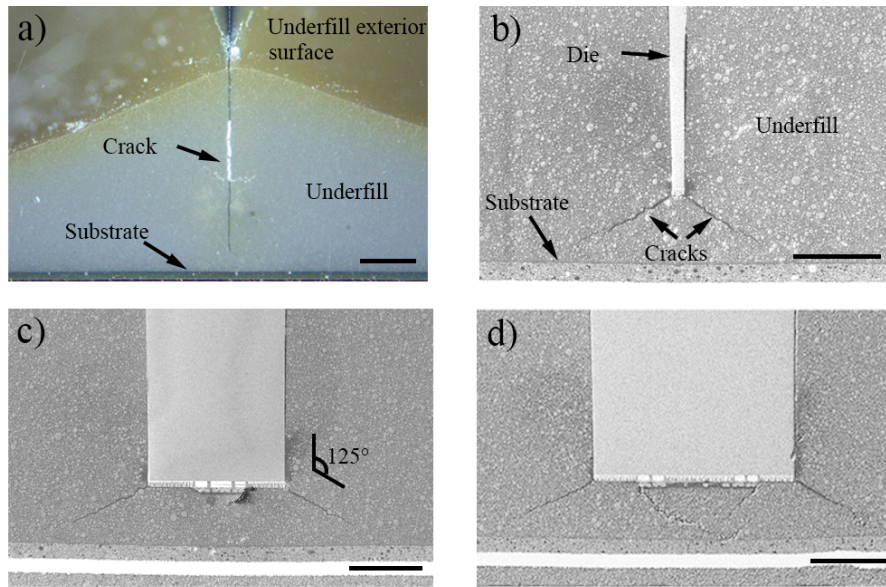


Figure 5.19 Underfill cracks observed at the die corner by cross-sectioning in the samples of cell 4, (a) in front of the die corner, (b) at the die corner, (c) at the beginning of crack-stop line, (d) at the line of crack-stop. Scale bar lengths of 100 μm .

The underfill crack modeling was realized by the XFEM phantom-nodes method described in section 5.6.2. In the current model, the underfill was considered to be homogeneous, as no significant resin-rich zones were observed. Figure 5.21 shows the evolution of the cracked elements for the cell 4 based on the submodel proposed in Figure 5.9. As shown in Figure 5.21b, the diagonal crack started to propagate first along the vertical edges of die, before the edge cracks. The diagonal crack then grew both vertically and radially along a 45° angle. Then, the two edge cracks were also found to propagate along the horizontal edges (Figure 5.21c).

In the final state shown in Figure 5.21d, the diagonal crack reached a length of 150 μm and a height of 600 μm . The edge cracks reached a length of 190 μm from the chip corner. Figure 5.22 summarizes the yz cross-sectional images of the edge crack at three distances along the chip edge in the x-direction. The maximum length (distance between the two endpoints of the crack in each cross-sectional image) of the edge crack reached 28 μm . The edge crack length is smaller than the experimental observations in Figure 5.19, because the experimental observed cracks were produced from 500 cycles instead of a monotonous static cooling process in simulation. To evaluate the directions of the edge crack plane (EFGH) in Figure 5.22, the normal vectors to the EFG, EFH, EGH and

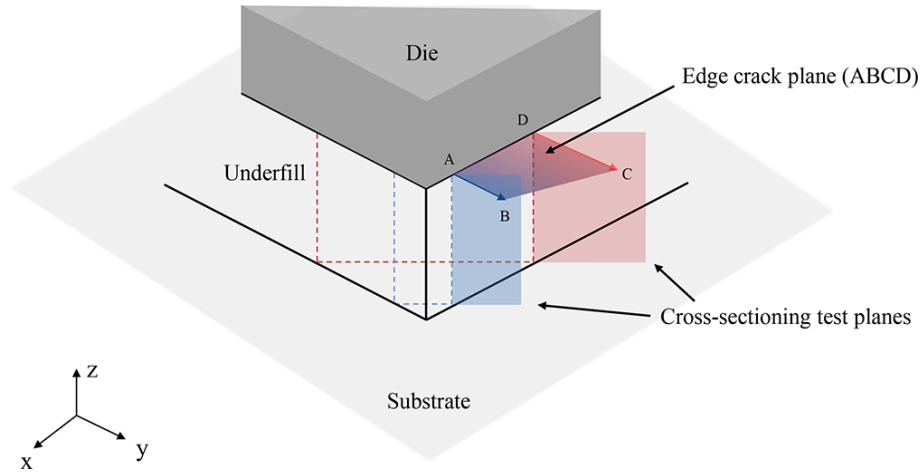


Figure 5.20 Diagram of the right edge cracks observed in the cross-sectioning test planes (AB and DC). The underfill fillet is not displayed in the diagram.

FGH planes were obtained from the crack locations. Then, the average angles between the normal vectors and the x, y, z axes were estimated to be $(89.8 \pm 2.6)^\circ$, $(44.0 \pm 4.9)^\circ$ and $(46.1 \pm 4.9)^\circ$, respectively, where the uncertainties represent the two-sided 90% confidence intervals based on the t-distribution for the four planes. These results are consistent with the experimental observations of the edge crack directions.

This approach does not require updating the mesh near the crack tip during the calculations and is suitable for already meshed underfill models. This model also has the limitation that as an element can only support one crack at a time, the intersection of the three cracks near the chip corner cannot be precisely simulated.

As the crack model implemented in this work was in a monotonous static cooling process instead of a cyclic loading process (fatigue crack growth), the length and height of the cracks obtained in the model were not the key metrics to be compared with experiments. To realize an effective fatigue crack growth modeling, it will be necessary to experimentally obtain the crack initiation moment and the crack locations in the underfill with respect to the number of cycles. However, these two parameters are more difficult to obtain than the initiation moment and the areas of chip-underfill delamination, since the cross-sectioning characterization is costly and time-consuming. The cross-sectioning is also a destructive characterization method that may aggravate the cracks in the underfill. Thus, a non-destructive method will be preferred in the future to realize the crack path monitoring, which would be essential to validate the model of underfill fatigue crack growth. The crack locations with respect to the number of cycles will be an effective parameter for estimating the electrical failure of the package.

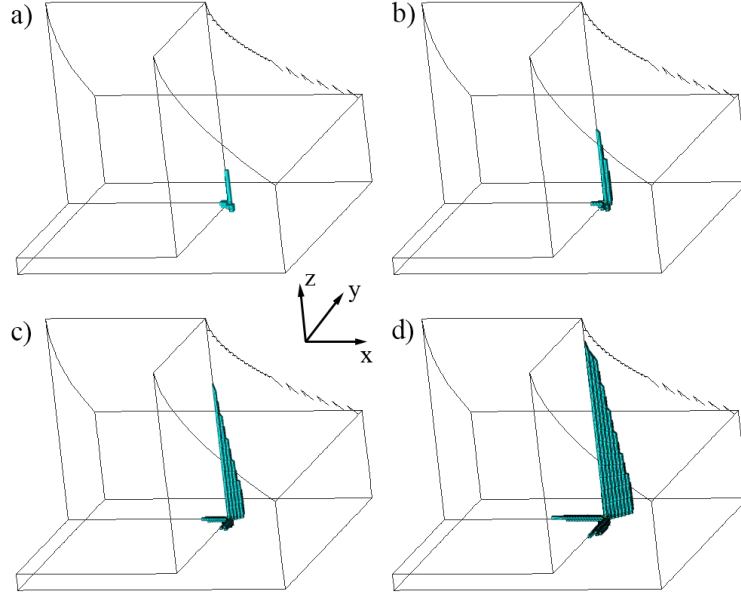


Figure 5.21 Cracked elements starting from the chip corner: (a) initial cracked elements, (b) cracks growing in the z direction, (c) cracks growing on both edges and diagonal direction, (d) final state of the three cracks. Wire-frames represent the outline of the underfill in the submodel.

5.8 Conclusions

In this work, three modeling approaches were proposed that estimate the initial moment of chip-underfill delamination, the growth of delaminated areas and the underfill cracking trajectories in the flip-chip packages. To study the effects of input manufacturing variables on the underfill reliability, five variables were considered, which are the kerf width, dicing type, laser outrigger presence, sealband material and sealband shape. A DTC test was first performed on thirteen cells of flip-chip test components with these input variables, and multiple characterizations were applied on the underfill to help construct the underfill reliability model. C-SAM, IR and cross-sectioning were performed to obtain the chip-underfill delamination and underfill cracks.

In order to estimate the number of cycles to delamination from the above input variables, these variables were encoded as binary values and implemented in a random-ANN model. Three overlapping datasets were used as shown in Table I, which were the LOOCV dataset (with cells number 1, 2, 3, 4, 6, 8, 10 and 12), the training dataset (with cells number 1, 3, 4, 5, 8, 10 and 12) and the test dataset (with cells number 2, 6, 7, 9, 11 and 13). A leave-one-out cross validation (LOOCV) was performed on the LOOCV dataset. The results indicated that the LOOCV should be used to partition the complete dataset, as a simpler random partitioning was not effective for such a small datasets. Cells 1, 4, 8,

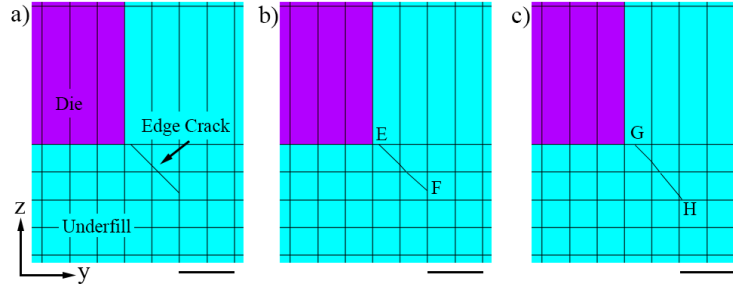


Figure 5.22 YZ cross-sectional images of the edge crack at the final state of the simulation with x-direction distances of (a) 20 μm , (b) 50 μm and (c) 100 μm from the chip corners. Scale bar lengths of 20 μm .

10 had features that could not be learned correctly from the other cells in the LOOCV dataset, and so they had to be included in the training dataset for the full analysis. Only the predicted distribution of the number of cycles to delamination for the cell 8 in the LOOCV dataset did not overlap with the experimental interval.

When the random-ANN model was next trained on the training dataset in the full analysis and then used to predict the number of cycles to delamination for cells in the test dataset, the predicted average number of cycles to delamination for cells 2 and 6 were 842 cycles and 918 cycles, inside the censored intervals of the experimental observations. For cells 7, 9, 11, 13, the predicted average numbers of cycles to delamination were 877, 310, 722 and 356 cycles, respectively, consistent with the experimental observation that no delaminations were found at 250 cycles. These predicted numbers of cycles were mostly independent of the randomized initial weights of the random-ANN model. Overall, the initial delamination were correctly predicted by the random-ANN model for all 6 cells in the test dataset.

Then, the propagation of delamination at the chip-underfill interface was modelled by the FEM. In this model, the delamination areas on the chip-underfill interface started at the die corners and grew to the die edges and interior regions. The growth rate of the delaminated areas decreased rapidly after the first 200 cycles after initial delamination due to the release of interfacial strain energy. When reaching the same delamination areas as measured by C-SAM, the difference between the average predicted number of cycles and the C-SAM inspection moment was defined as the model error. The LOOCV dataset was used for comparison between the experiments and simulations. For cells 2 and 6, the model errors were less than ± 100 cycles. The model errors for cells 4 and 12 were less than ± 200 cycles. The model error for cells 1 and 10 were 220 and 350 cycles (earlier than their C-SAM inspection moments at 1000 cycles). Of the 6 cells used for validation, the

model errors for 5 cells were less than the width of the censoring interval, consistent to the experimental observations.

In addition to the chip-underfill delamination, underfill cracks were observed along the diagonal direction and also along the die edge directions by successive cross-sectioning at the chip corner area. XFEM was used to model the crack trajectories. The directions of diagonal and edge cracks were in good agreement with the experiments, with an error of less than 2.5° for the edge cracks. The modeling of fatigue crack growth could be further developed with a similar technique if the crack locations could be monitored with respect to the number of cycles.

In this paper, an ANN was applied to estimate the number of cycles to delamination for different input manufacturing variables for the first time. Although the performance of the ANN was sensitive to the partitioning of the small dataset, the predicted numbers of cycles to delamination in the LOOCV dataset and in the test dataset were consistent with the experimental observations. The accuracy of the ANN model could be improved by including more cells and reducing the C-SAM inspection intervals. The predicted initial delamination would then be more accurate when used as the initial moment of delamination for the delamination growth model. The chip-underfill interface adhesion quality may affect the interfacial strength [49, 50], while the filler density [224] and filler distribution [7] may affect the maximum stress in the underfill. These factors could also be relevant in estimating the initiation and growth of delamination, and could be considered in future models. In addition, the stresses and strains calculated from the FEM and XFEM could be further used as input parameters for the ANN model as well. For the underfill crack modeling, XFEM has shown good accuracy in predicting the underfill crack trajectories. To better model the crack growth in the underfill, a non-destructive technique could be required to monitor the crack path with respect to the number of DTC cycles for validation of a fatigue crack model. The modeling approaches presented in this paper could eventually be used to predict the initiation of delamination, growth of delamination and underfill crack trajectories in actual flip-chip packages, when multiple input manufacturing variables need to be considered.

CHAPTER 6

ENGLISH CONCLUSION

The research project presented in this thesis focused on the damage and reliability issue of the underfill in flip-chip packages. A study on the chip-underfill interfacial delamination and underfill cracking was performed by both experimental and numerical methods. This chapter presents a summary of results and the main contributions achieved in this thesis. Perspectives for future work are also suggested in order to improve the knowledge of reliability in microelectronics.

6.1 General Conclusions

A roadmap for building the underfill reliability model in thermal cycling was first described in section 1.3. In this roadmap, a perfect model was defined with input and output variables. A total of 8 elements should be included in this model. The general objective of this project was to contribute to a numerical model that could estimate the initiation and growth of delamination and crack paths from the basic inputs. This thesis contributes to parts of the roadmap leading the perfect model, which is the 3rd (underfill strain calculation), 4th (initiation of underfill delamination), 5th (growth of underfill delamination) and 7th (growth of underfill cracking) elements. The detailed results are presented for our three sub-objectives below:

Underfill strain distribution near the chip corner

The first sub-objective of the project was to experimentally obtain the underfill strain distribution and to confirm the accuracy of the FEM-calculated strains at chip corners. An approach for measuring the local strain inside the underfill was developed and named the confocal-DIC technique. This technique combined the advantages of laser scanning confocal microscopy and digital image correlation method to provide 3-dimensional stacked strain contours. This technique was validated with a free thermally expanded sample and its deformations could be calculated analytically. Then, the confocal-DIC technique was applied to measure the underfill strain around a chip corner, which had a thermal loading from the ambient temperature (24°C) to 60°C. The confocal-DIC-measured first principal strain reached 0.9% at the corner area, consistent with the results of FEM. In the simulation of a notched 3-point bending sample, the maximum strains in front of the notch were only about 5% lower than the simulations results. The confocal-DIC method shows

excellent capability in measuring the strain distribution in a 3-dimensional stacked view. These results respond to the first research question, which aimed to develop an *in-situ* strain measurement technique for obtaining the strains in the underfill. Our contribution is the development of the confocal-DIC technique for strain measurements in the underfill and the validation of underfill corner strains.

Compared with the level of complexity of underfill reliability modeling at the chip corner (see Table 1.6), this contribution fits the level 1 of the chip characteristic (isotropic, pyramid corner), level 2 of the underfill characteristic (homogeneous, low filler density), level 1 of the underfill crack situation (no cracks) and level 1 of the chip-underfill interface situation (no delamination). Higher levels of complexity for chip and underfill material were not investigated in this part.

Underfill strain distribution near the cracks

The second sub-objective was to construct a precise numerical model to describe the cracking behaviour that has been often observed in the underfill after the thermal cycling tests. A test component that is similar to a flip-chip package was fabricated. Artificial cracks were also fabricated along the diagonal direction from the chip corner and the local deformations near the crack areas were measured by the confocal-DIC technique at 0°C, with a reference temperature of 25°C. A crack model was built by XFEM. The distributions of the hoop strain in the experiments and simulations were in good agreement, with rapidly dropping values away from the crack tip and reaching a constant value far from the tip. When reducing the element size to 16 μm in the numerical model, the hoop strain at the crack tip was within the confidence intervals for the confocal-DIC-measured strains. The hoop strain obtained by simulations at 16 μm element size was 22.0% and 9.5% lower than the average hoop strain measured by experiments for the 160 μm crack and 640 μm crack respectively. These differences decreased to 8.2% and 6.3%, when the distance was from 50 to 175 μm away from the crack tip. The angle of the chip sidewalls and the underfill thickness had a negligible effects on the crack tip strains, so they are not the critical features for modeling. A reduction in CTE in the regions below the chip from the gravity-driven concentration of filler particles could slightly improve the agreement with the measurements of the principal strains and hoop strains at the crack tip in bottom layers.

Furthermore, a propagation model was realized based on the XFEM with phantom nodes. The crack path was along the diagonal direction, in good agreement with the experimental observations. The XFEM phantom-node approach is able to provide a correct crack

path and a reasonable strain distribution around the crack zone. As a result, the strain measurements applied to the corner cracks could eventually be used to validate the underfill crack model. Our contribution is the demonstration of the applicability of XFEM for underfill crack modeling by confocal-DIC-measured strains.

According to Table 1.6, this contribution fits the level 2 of the underfill crack situation (one crack). The chip characteristic, underfill material characteristic and chip-underfill interface situation are not changed. In addition to the lack of complexity for the chip and underfill characteristics, several extra limitations still exist in this part: 1) the cracks at the chip edges and cracks towards the substrate were not studied, but are more likely to grow into electrical components; 2) we did not achieve the strain measurements in the underfill during the growth of delamination and cracking, for validating the strain variation with respect to the number of cycles; 3) the effect of input variability on the underfill strain spatial distributions was not investigated.

Modeling of chip-underfill delamination and underfill cracking for actual flip-chip packages

The third sub-objective was to build a generalized model that could describe delamination and cracking of the underfill with the effect of five input manufacturing variables. 13 test cells were prepared with the five manufacturing variables, including kerf width, dicing type, laser outrigger presence, sealband material and sealband shape. Before modeling, the deep thermal cycling (DTC) tests were performed on 13 test cells of samples. The characterization of C-SAM, IR microscopy and cross-sectioning were accomplished to reveal the number of cycles to delamination, the chip-underfill interface delamination areas and the underfill crack trajectories.

A random-ANN model was applied to estimate the initial moment of delamination in order to use the censored data in the ANN modeling. To estimate the number of cycles to delamination from the five input variables, these variables were encoded as binary values and implemented in a random-ANN model. Three overlapping datasets were used, which were the LOOCV dataset (with cells number 1, 2, 3, 4, 6, 8, 10 and 12), the training dataset (with cells number 1, 3, 4, 5, 8, 10 and 12) and the test dataset (with cells number 2, 6, 7, 9, 11 and 13). A leave-one-out cross validation (LOOCV) was performed on the LOOCV dataset. The results indicated that the LOOCV should be used to partition the complete dataset, as a simpler random partitioning was not effective for such a small datasets. From the 8 cells in the LOOCV dataset, cells with low prediction accuracy on the number of cycles to delamination had to be included in the training dataset, since their

features could not be learned correctly from the other cells in the LOOCV dataset. When the random-ANN model was next trained on the training dataset, the predicted numbers of cycles for all 6 cells in the test dataset were consistent with experimental observations.

Then, the delamination growth model was built by FEM with a layer of interface elements between the chip and the underfill. When reaching the same delamination areas as measured by C-SAM, the difference between the predicted number of cycles and the C-SAM inspection moment was defined as the model error. The LOOCV dataset was used for comparison between the experiments and simulations. Of the 6 cells used for validation, the model errors for 5 cells were less than the width of the censoring interval (250 cycles), consistent to the experimental observations.

In the cross-sectional images from the corner of the test components, multiple cracks were observed near the die corner along the diagonal and edge direction. With the help of XFEM, the crack directions were in good agreement with the experiments, with an error of less than 2.5° for the edge cracks.

Overall, these modeling approaches could eventually be used to predict the initiation of delamination, growth of delamination and underfill crack trajectories in actual flip-chip packages, when multiple input manufacturing variables need to be considered. These results respond to the second research question, which aimed to develop a numerical model for underfill delamination and cracking. The careful validation of delamination occurrence, delamination areas and crack paths demonstrates the good performance of the numerical model developed in this work.

Referring to the challenges of variability of input parameters in section 1.3.3, this part contributed to the effect of chip corner shapes on the initial moment of delamination. The model complexity of chip (isotropic, pyramid corner) and underfill material (homogeneous, low filler density) characteristic remained unchanged. The delamination growth model fits the level 2 of the chip-underfill interface situation (delamination on flat interfaces). The cracking model fits the level 3 of the underfill crack situation (multiple cracks). In addition, the limitations still include: 1) the initial moment of underfill cracking was not investigated; 2) the crack growth with respect to the number of cycles was not studied; 3) the dependency of delamination and cracking models was not studied; 4) the effect of input variability on the delamination and crack modeling was not considered.

6.2 Perspectives for Future Work

The work of this thesis can be considered as a first step in modeling the underfill reliability in thermal cycling. According to the modeling roadmap defined in section 1.3, several points are still unaddressed. For the element of advanced preprocessing in the perfect model, we did not give a solution on the effect of advanced geometrical and material features on the time to underfill failure, but they are critical to the underfill reliability. As most input parameters should be described by a distribution in the population, a stochastic process for modeling the time to failure will be required in the future.

For the element of underfill strain calculation in the perfect model, the confocal-DIC technique was developed to validate the model-obtained strains. The confocal-DIC technique has shown excellent performance in strain measurements on some quasi-transparent materials, but it still has some limitations on non-transparent materials. The next step is to increase the filler density from 0.1 wt% to 60 wt% and realise the underfill imaging in real flip-chip packages. This requires a technique to penetrate the epoxy, silicon and metal at the same time, and the micro-CT may be able to meet this requirement. In the field of DIC, as the current DIC algorithm was less capable of capturing very high gradients of deformation, it is suggested to improve the algorithm on a small scale, for example by adding a local power function to fit the strain distribution at the crack tip region.

For the elements of underfill delamination initiation and growth, the C-SAM inspection interval was 250 cycles and could be shortened to 100 cycles, in order to obtain the initial moment of delamination and the growth of delamination areas more precisely. The material constants of the Paris' law at the chip-underfill interface could be experimentally measured as well to calculate the delamination increment per iteration in the model. In addition, the modeling of delamination should be applied to the chip sidewall as well, and a non-destructive technique for measuring the sidewall delamination areas will be required in the future. After the implementation of these improvements, the variability of the input parameters will have to be considered in the model. Based on the discussion in section 2.4.6, the stochastic finite element methods, including the perturbation approach represented by a Taylor series, polynomial chaos expansion represented by Hermite polynomials and Monte-Carlo simulation [151–153], could be used to incorporate the input uncertainties. Moreover, the chip and underfill material complexity will be set to level 5 (see Table 1.6), closest to the real material properties. The model will obtain the distribution of number of cycles to delamination and the growth of delamination areas per cycle. The experimentally and numerically obtained strain distributions at selected spatial positions and numbers of cycles could then be compared.

For the elements of underfill crack initiation and growth, the initial moment of underfill crack has not been studied in the literature, as the underfill crack initiation is more difficult to observe than the delamination initiation. So, the determination of the number of cycles to cracking is difficult. In addition, the crack model implemented in this project was in a monotonous static cooling process instead of a cyclic loading process (fatigue crack growth). To validate the fatigue crack growth model, the crack initiation moment and the crack locations with respect to the number of cycles must be experimentally obtained. Thus, a non-destructive method needs to be developed in the future to realize the crack path monitoring. Then, similar to the modeling of delamination, the stochastic modeling combined with the input variability will be added to the modeling of underfill cracks as well.

For the element of cracks in metallic components, the underfill delamination and crack could affect the stress distribution in solder joints and BEOL. As the metallic components also suffer from the fatigue damage from the beginning of thermal cycling, the predictions on the time to failure is influenced by both the metal fatigue and underfill damage, which makes the modeling on time to electrical failure more complicated. Future work could focus on the variation of elastic modulus, strength and fracture toughness in the metallic components with respect to the number of cycles. In order to validate the model-obtained strains in the BEOL, it will be desirable to develop a technique to experimentally measure the strain at sub-micron resolution (probably the micro-CT). In addition, the cracks need to be carefully identified in redundant or non-redundant electrical components, as the electrical failure only occurs when a non-redundant component is cracked.

Practitioners, before this thesis, could only use the non-validated underfill corner stress and strain as metrics to compare with the threshold values, which are empirically defined by a percentage of the ultimate strength and strain of the underfill. After this thesis, the model-obtained strain distributions have been experimentally validated on the underfill with low filler density. Practitioners could be more confident for the model-calculated stresses and strains in the underfill. The stresses and strains are then used to calculate the underfill delamination areas and crack paths with good accuracy. When the perfect model is finished, practitioners will be able to predict the time to electrical failure (e.g. the survival-functional graph and the $N50$) based on the basic inputs, advanced geometrical and material features. They will also understand which cracked components caused the electrical failure. These results will help them select the most suitable package configuration, process and materials for best reliability performance.

CHAPTER 7

CONCLUSION FRANÇAISE

Le projet de recherche présenté dans cette thèse s'est concentré sur la question des dommages et de la fiabilité de l'underfill dans les encapsulations de puces retournées. Une étude approfondie a été menée par des méthodes expérimentales et numériques. Ce chapitre présente un résumé des résultats et des principales contributions qui ont été apportées à cette thèse. Des perspectives de travaux futurs sont également suggérées afin de compléter les connaissances sur la fiabilité microélectronique.

7.1 Conclusions Générales

Un plan d'action pour la construction du modèle de fiabilité de l'underfill en cyclage thermique a d'abord été décrit à la section 1.3. Dans ce plan de route, un modèle parfait a été défini avec des variables d'entrée et de sortie. Au total, 8 éléments doivent être inclus dans ce modèle. L'objectif général de ce projet était de contribuer à un modèle numérique capable d'estimer l'initiation et la croissance de la délamination et des chemins de fissures à partir d'entrées de base. Cette thèse contribue à certaines parties du plan de route menant au modèle parfait, à savoir les 3e (calcul de la déformation de l'underfill), 4e (initiation de la délamination de l'underfill), 5e (croissance de la délamination de l'underfill) et 7e (croissance de la fissuration de l'underfill) éléments. Les résultats détaillés sont présentés ci-dessous pour nos trois sous-objectifs :

Distribution de déformation près du coin de puce dans l'underfill

Le premier sous-objectif du projet est d'obtenir la distribution de la déformation dans l'underfill expérimentalement et confirmer la précision des déformations calculées par éléments finis aux coins des puces. Une approche pour mesurer la déformation locale à l'intérieur de l'underfill a été développée et est connue sous le nom de technique confocale-DIC. Cette technique combine les avantages de la microscopie confocale à balayage laser et des méthodes de corrélation d'images numériques, et elle peut fournir des contours de déformation empilés en 3 dimensions. Cette technique a été validée par un échantillon de dilatation thermique libre dont la déformation a été calculée analytiquement. Ensuite, la technique confocale-DIC a été appliquée pour mesurer la contrainte de l'underfill autour d'un coin de puce, qui avait une charge thermique de la température ambiante (24°C) à 60°C. La déformation principale a atteint 0,9% au coin, en cohérence avec les résultats de

la simulation numérique par la méthode des éléments finis. Dans un échantillon encoché de flexion à 3 points, les déformations maximales devant l'entaille n'étaient inférieures que d'environ 5% aux résultats des simulations. La méthode confocale-DIC montre une excellente capacité à mesurer la distribution des déformations dans une vue tridimensionnelle. Ces résultats répondent à la première question de recherche, qui visait à développer une technique de mesure des déformations *in-situ* pour obtenir les déformations dans l'underfill. Notre contribution est le développement de la technique confocale-DIC pour les mesures de déformation dans l'underfill et la validation des déformations des coins de l'underfill.

Par rapport au niveau de complexité de la modélisation de la fiabilité de l'underfill au coin de la puce (voir Tableau 1.6), cette contribution correspond au niveau 1 de la caractéristique de la puce (isotrope, coin pyramidal), au niveau 2 de la caractéristique de l'underfill (homogène, faible densité de remplissage), au niveau 1 de la situation de fissure de l'underfill (aucune fissure) et au niveau 1 de la situation de l'interface de puce-underfill (aucune délamination). Les niveaux de complexité plus élevés pour les puces et les matériaux de l'underfill n'ont pas été étudiés dans cette partie.

Distribution de déformation près des fissures dans l'underfill

Le deuxième sous-objectif est de construire un modèle numérique pour décrire le comportement de fissuration souvent observé en underfill après des tests de cyclages thermiques. Un composant de test similaire à un boîtier de puce retournée a été fabriqué. Des fissures artificielles ont également été fabriquées dans le sens de la diagonale à partir du coin de la puce et les déformations locales près des zones de fissures ont été mesurées par la technique confocale-DIC à 0°C, avec une température de référence de 25°C. Un modèle de fissuration a été construit par XFEM. Les distributions de déformations circonférentielle dans les mesures et les simulations étaient en accord général, les valeurs chutant rapidement loin du fond de fissure et atteignant une valeur constante loin de la pointe. En réduisant la taille des éléments à 16 μm dans le modèle numérique, la déformation circulaire au front de la fissure se situait dans les intervalles de confiance des déformations mesurées. La déformation circonférentielle obtenue par simulation à une taille d'élément de 16 μm était de 22,0% et 9,5% inférieure à la déformation circonférentielle moyenne mesurée expérimentalement pour la fissure de 160 μm et de 640 μm respectivement. Ces différences ont diminué à 8,2% et 6,3%, respectivement, lorsque la distance était de 50 à 175 μm du fond de fissure. L'angle des parois latérales du sidewall et l'épaisseur de l'underfill ont eu une influence négligeable sur la déformation de la pointe de la fissure, ce n'étaient donc pas les caractéristiques essentielles de la modélisation. Une réduction du CTE dans les

régions situées sous la puce pourrait mieux correspondre à la différence de déformation principale à la pointe de la fissure dans les couches inférieures.

De plus, un modèle de propagation a été réalisé basé sur le XFEM avec des nœuds fantômes. La trajectoire de la fissure était vers la direction diagonale, en bon accord avec les observations expérimentales. L'approche du XFEM nœud fantôme est capable de fournir un chemin de fissure correct et une distribution de contrainte raisonnable autour de la zone de fissure. En conséquence, les mesures de déformation appliquées aux fissures du coin pourraient éventuellement être utilisées pour valider le modèle de fissure de l'underfill. Notre contribution est la démonstration de l'applicabilité de XFEM pour la modélisation des fissures d'underfill par des déformations mesurées par la technique confocale-DIC. Par rapport à l'élément de calcul de la déformation de l'underfill dans le modèle parfait, nous avons validé la distribution de la déformation de l'underfill en fonction des positions spatiales avec des fissures diagonales. Cependant, plusieurs limitations existent encore dans cette partie. Nous avons mesuré la distribution de la déformation de l'underfill pour les fissures diagonales vers le filet, mais les fissures aux bords de la puce et les fissures vers le substrat n'ont pas été étudiées. Ces situations non étudiées sont importantes, car ces fissures sont plus susceptibles de se développer dans les composants électriques et de provoquer des défaillances électriques. De plus, nous n'avons pas réalisé les mesures de déformation dans l'underfill pendant la croissance du délaminage et de la fissuration, pour valider la variation de la déformation à chaque position spatiale par rapport au nombre de cycles.

Selon le tableau 1.6, cette contribution correspond au niveau 2 de la situation de fissure de l'underfill (une fissure). La caractéristique de la puce, la caractéristique du matériau de l'underfill et la situation de l'interface de puce-underfill ne sont pas modifiées. En plus du manque de complexité pour les caractéristiques du puce et de l'underfill, plusieurs limitations supplémentaires existent encore dans cette partie : 1) les fissures aux bords de la puce et les fissures vers le substrat n'ont pas été étudiées, mais elles sont plus susceptibles de se développer en composants électriques ; 2) nous n'avons pas réalisé les mesures de déformation dans l'underfill pendant la croissance de la délamination et de la fissuration, pour valider la variation de la déformation par rapport au nombre de cycles ; 3) l'effet de la variabilité d'entrée sur les distributions spatiales de la déformation de l'underfill n'a pas été étudié.

Modélisation de la délamination et de la fissuration pour des encapsulations puces retournées réelles

Le troisième sous-objectif est de construire un modèle général qui pourrait décrire ensemble la délamination et la fissuration de l'underfill avec l'effet de cinq variables de fabrication d'entrée. 13 cellules d'essai ont été préparées avec les cinq variables de fabrication, y compris la longueur de l'incision Si₃N₄, le type de découpe, la présence d'un outrigger, le matériau de la bande d'étanchéité et la forme de couverture. Avant la modélisation, les tests de cyclage thermique profond (DTC) ont été effectués sur 13 cellules. La caractérisation du C-SAM et des coupes transversales a été réalisée pour révéler le moment initial et la superficie de la délamination de l'interface et les trajectoires des fissuration de l'underfill.

Un réseau de neurones artificiels aléatoire (random-ANN) a été appliqué pour estimer le moment initial de délamination pour utiliser les données censurées pendant la modélisation de ANN. Afin d'estimer le nombre de cycles jusqu'à la délamination à partir les cinq variables d'entrée, ces variables ont été codées comme des valeurs binaires et mises en œuvre dans un modèle random-ANN. Trois ensembles de données se chevauchant ont été utilisés, qui étaient l'ensemble LOOCV (avec les cellules 1, 2, 3, 4, 6, 8, 10 et 12), l'ensemble d'apprentissage (avec les cellules 1, 3, 4, 5, 8, 10 et 12) et l'ensemble de test (avec les cellules 2, 6, 7, 9, 11 et 13). Une validation croisée leave-one-out (LOOCV) a été effectuée sur l'ensemble LOOCV. Les résultats indiquent que la LOOCV devrait être utilisée pour partitionner l'ensemble complet, car un partitionnement aléatoire simple n'était pas efficace pour un ensemble aussi petit. Parmi les 8 cellules de l'ensemble LOOCV, les cellules ayant une faible précision de prédiction du nombre de cycles jusqu'à la délamination doivent être incluses dans l'ensemble de données d'entraînement, car leurs caractéristiques n'ont pas pu être apprises correctement à partir des autres cellules de l'ensemble LOOCV. Lorsque le modèle random-ANN a ensuite été entraîné sur l'ensemble d'entraînement, les nombres de cycles prédits pour toutes les 6 cellules de l'ensemble de test étaient conformes aux observations expérimentales.

Ensuite, le modèle de croissance du délaminage a été construit par FEM avec une couche d'éléments d'interface entre la puce et l'underfill. En atteignant les mêmes zones de délamination que celles mesurées par C-SAM, la différence entre le nombre de cycles prédits et le moment de l'inspection C-SAM a été définie comme l'erreur du modèle. L'ensemble LOOCV a été utilisé pour comparer les résultats entre les expériences et les simulations. Sur les 6 cellules utilisées pour la validation, les erreurs du modèle pour 5 cellules étaient

inférieures à la largeur de l'intervalle de censure (250 cycles), en accord avec les observations expérimentales.

Dans les images en coupe transversale du coin des composants testés, de multiples fissures ont été observées près du coin de la puce, dans la direction de la diagonale et du bord. Les directions des fissures diagonales et de bord étaient en bon accord avec les expériences, avec une erreur de moins de $2,5^\circ$ pour les fissures de bord.

En général, les approches de modélisation présentées dans ce chapitre pourraient éventuellement être utilisées pour prédire l'initiation de la délamination, la croissance de la délamination et les trajectoires des fissures de l'underfill dans des encapsulations de puces retournées réels, lorsque de multiples variables de fabrication doivent être prises en compte. Ces résultats répondent à la deuxième question de recherche, qui visait à développer un modèle numérique pour la délamination et la fissuration dans l'underfill. La validation minutieuse de l'apparition de la délamination, des zones de délamination et des chemins de fissures démontre la bonne performance du modèle numérique développé dans ce travail. Par rapport aux éléments d'initiation et de croissance du délaminage dans l'underfill du modèle parfait, cette contribution a obtenu la distribution du nombre de cycles jusqu'au délaminage, mais n'a pas tenu compte de la variation des propriétés géométriques et matérielles avancées sur cette distribution. Les dimensions des zones de délamination dans chaque direction n'ont pas encore été étudiées. Pour les éléments d'initiation et de croissance de la fissuration d'underfill, le moment initial de la fissuration n'a pas été étudié. Le modèle de croissance des fissures de l'underfill a été simplifié à un processus de refroidissement statique monotone au lieu d'un processus de chargement cyclique. Ainsi, les hauteurs et longueurs des fissures en fonction du nombre de cycles n'ont pas été obtenues.

En se référant aux défis de la variabilité des paramètres d'entrée dans la section 1.3.3, cette partie a contribué à l'effet des formes de coin de la puce sur le moment initial de délamination. La complexité du modèle de la caractéristique de la puce (isotrope, coin pyramidal) et du matériau de l'underfill (homogène, faible densité de remplissage) est restée inchangée. Le modèle de croissance du délaminage correspond au niveau 2 de la situation de l'interface de puce-underfill (délaminage sur des interfaces plates). Le modèle de fissuration correspond au niveau 3 de la situation de fissuration d'underfill (fissures multiples). En outre, les limitations incluent toujours : 1) le moment initial de la fissuration d'underfill n'a pas été étudié ; 2) la croissance de la fissure par rapport au nombre de cycles n'a pas été étudiée ; 3) la dépendance des modèles de délamination et de fissuration n'a pas été étudiée ; 4) l'effet de la variabilité des entrées sur la modélisation de la délamination et de la fissuration n'a pas été pris en compte.

7.2 Perspectives pour les Travaux Futurs

Le travail de cette thèse peut être considéré comme une première étape dans la modélisation de la fiabilité de l'underfill en cyclage thermique. Selon le plan de route de la modélisation défini dans la section 1.3, plusieurs points ne sont toujours pas résolus à ce jour. Pour l'élément de prétraitement avancé dans le modèle parfait, nous n'avons pas donné de solution sur l'effet des caractéristiques géométriques et matérielles avancées sur le temps de défaillance de l'underfill, mais ils sont essentiels pour la fiabilité de l'underfill. Comme la plupart des paramètres d'entrée doivent être décrits par une distribution dans la population, un processus stochastique pour la modélisation du temps avant défaillance sera nécessaire à l'avenir.

Pour l'élément de calcul de la déformation de l'underfill dans le modèle parfait, la technique confocale-DIC a été développée pour valider les déformations obtenues par le modèle. La technique confocale-DIC a montré d'excellentes performances pour les mesures de déformation dans certains matériaux quasi-transparents, mais a quelques limitations sur les matériaux non transparents. L'étape suivante consiste à augmenter la densité d'underfill de 0,1% en poids à 60% en poids et à réaliser l'imagerie de l'underfill dans des boîtiers de puces retournées réels. Cela nécessite une technique permettant de pénétrer à la fois dans l'époxy, le silicium et le métal, et le micro-CT peut être en mesure de répondre à cette exigence. Dans le domaine de la DIC, l'algorithme DIC actuel étant moins capable de capturer de très hauts gradients de déformation, il est suggéré d'améliorer l'algorithme à petite échelle, par exemple en ajoutant une fonction de puissance locale pour régler la distribution de la déformation dans la région de la pointe de la fissure.

Pour les éléments d'initiation et de croissance du délaminage de l'underfill, l'intervalle d'inspection C-SAM était 250 cycles et pourrait être réduit à 100 cycles, afin d'obtenir le moment initial du délaminage et la croissance des zones de délaminage avec plus de précision. Les constantes matérielles de la loi de Paris à l'interface puce-underfill peuvent également être mesurées expérimentalement pour calculer l'augmentation du délaminage par itération dans le modèle. En outre, la modélisation de la délamination devrait être appliquée à la paroi latérale de la puce également, et une technique non destructive pour mesurer les zones de délamination de la paroi latérale sera nécessaire à l'avenir. Après la mise en œuvre de ces améliorations, la variabilité des paramètres d'entrée devra être prise en compte dans le modèle. Sur la base de la discussion dans la section 2.4.6, les méthodes stochastiques d'éléments finis, y compris l'approche de perturbation représentée par une série de Taylor, l'expansion polynomiale du chaos représentée par des polynômes d'Hermite et la simulation de Monte-Carlo [151–153], pourraient être utilisées pour incorporer les

incertitudes d'entrée. De plus, la complexité des matériaux de la puce et de l'underfill sera placée au niveau 5 (voir Tableau 1.6), le plus proche des propriétés réelles des matériaux. Le modèle obtiendra la distribution du nombre de cycles jusqu'à la délamination et la croissance des zones de délamination par cycle. Les distributions de déformation obtenues expérimentalement et numériquement à des positions spatiales et des nombres de cycles sélectionnés peuvent ensuite être comparées.

Pour les éléments de l'initiation et la croissance des fissures d'underfill, le moment initial des fissures d'underfill n'a pas été étudié dans la littérature, car l'initiation des fissures d'underfill est plus difficile à observer que l'initiation du délaminage. La détermination du nombre de cycles jusqu'à la fissuration est donc difficile. De plus, le modèle de fissure mis en œuvre dans ce projet se situait dans un processus de refroidissement statique monotone au lieu d'un processus de chargement cyclique (croissance des fissures par fatigue). Pour valider le modèle de croissance des fissures par fatigue, le moment d'initiation des fissures et les emplacements des fissures en fonction du nombre de cycles doivent être obtenus expérimentalement. Ainsi, une méthode non-destructive doit être développée à l'avenir pour réaliser la surveillance de la trajectoire des fissures. Ensuite, comme pour la modélisation du délaminage, la modélisation stochastique combinée à la variabilité des entrées sera également ajoutée à la modélisation des fissures de l'underfill.

Pour l'élément des fissures dans les composants métalliques, la délamination et la fissure de l'underfill pourraient affecter la distribution des contraintes dans les soudures et le BEOL. Comme les composants métalliques souffrent également de dommages de fatigue dès le début du cyclage thermique, les prédictions sur le temps jusqu'à la défaillance sont influencées à la fois par la fatigue du métal et les dommages de l'underfill, ce qui rend plus compliquée la modélisation du temps jusqu'à la panne électrique. Les travaux futurs pourraient porter sur la variation du module élastique, de la résistance et de la ténacité à la rupture des composants métalliques en fonction du nombre de cycles. Afin de valider les déformations obtenues par le modèle dans le BEOL, il sera désirable de développer une technique pour mesurer expérimentalement la déformation à une résolution sous-micron (probablement le micro-CT). En outre, les fissures doivent être soigneusement identifiées dans les composants électriques redondants ou non redondants, car la défaillance électrique ne se produit que lorsqu'un composant non redondant est fissuré.

Avant cette thèse, les praticiens ne pouvaient utiliser que les contraintes et les déformations non validées dans les coins de l'underfill comme paramètres de comparaison avec les valeurs seuils, qui sont définies empiriquement par un pourcentage de la résistance et de la déformation ultimes de l'underfill. Après cette thèse, les distributions des déformations

obtenues par le modèle dans l'underfill ont été partiellement validées expérimentalement. Les praticiens peuvent être plus confiants pour les contraintes et les déformations calculées par le modèle dans l'underfill. Les contraintes et les déformations sont ensuite utilisées pour calculer les zones de délamination et les chemins de fissures avec une bonne précision. Lorsque le modèle parfait sera terminé, les praticiens seront en mesure de prédire le temps jusqu'à la défaillance électrique (par exemple, le graphique survie-fonction et le $N50$) à partir des entrées de base, et des caractéristiques géométriques et matérielles avancées. Ils comprendront également quels composants fissurés ont causé la défaillance électrique. Ces résultats les aideront à sélectionner la configuration du boîtier, le processus et les matériaux les plus appropriés pour obtenir les meilleures performances en matière de fiabilité.

LIST OF REFERENCES

- [1] C.P. Wong. Thermal-mechanical enhanced high-performance silicone gels and elastomeric encapsulants in microelectronic packaging. *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part A*, 18(2):270–273, 1995.
- [2] M. Pecht, R. Agarwal, and P. et al. McCluskey. *Electronic packaging: materials and their properties*. CRC press, 2017.
- [3] B. Milton, O. Kwon, C. Huynh, I. Qin, and B. Chylak. Wire bonding looping solutions for high density system-in-package (sip). In *International Symposium on Microelectronics*, volume 2017, pages 000426–000431. International Microelectronics Assembly and Packaging Society, 2017.
- [4] M. Ranjan, L. Gopalakrishnan, K. Srihari, and C. Woychik. Die cracking in flip chip assemblies. In *1998 Proceedings. 48th Electronic Components and Technology Conference (Cat. No. 98CH36206)*, pages 729–733. IEEE, 1998.
- [5] Z. Zhang and C.P. Wong. Recent advances in flip-chip underfill: materials, process, and reliability. *IEEE Transactions on Advanced Packaging*, 27(3):515–524, 2004.
- [6] J. Wan. *Analysis and modeling of underfill flow driven by capillary action in flip-chip packaging*. PhD thesis, 2005.
- [7] M. Paquet, D. Danovitch, P.M. Souare, and J. Sylvestre. Study of capillary underfill filler separation in advanced flip chip packages. In *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, pages 1361–1368. IEEE, 2017.
- [8] W. Greig. *Integrated circuit packaging, assembly and interconnections*. Springer Science & Business Media, 2007.
- [9] C.P. Wong and D. Baldwin. No-flow underfill for flip-chip packages. 1996.
- [10] P.O. Weber. Chip package with molded underfill, March 14 2000. US Patent 6,038,136.
- [11] S.H. Shi, T. Yamashita, and C.P. Wong. Development of the wafer level compressive-flow underfill process and its required materials. In *1999 Proceedings. 49th Electronic Components and Technology Conference (Cat. No. 99CH36299)*, pages 961–966. IEEE, 1999.
- [12] J. Pellerin. *Estimation de la Vie en Fatigue D’un Assemblage Microélectronique Par la Méthode Des Éléments Finis*. PhD thesis, Université de Sherbrooke, 2016.
- [13] JESD22-A104D. Standard for temperature cycling. *JEDEC Solid State Technology Association*, 1:85–103, 2009.
- [14] J. Massey and J. Frank. The kolmogorov-smirnov test for goodness of fit. *Journal of the American statistical Association*, 46(253):68–78, 1951.
- [15] A. Lall. Data streaming algorithms for the kolmogorov-smirnov test. In *2015 IEEE International Conference on Big Data (Big Data)*, pages 95–104. IEEE, 2015.
- [16] L. Baringhaus and N. Henze. Tests of fit for exponentiality based on a characterization via the mean residual life function. *Statistical Papers*, 41(2):225–236, 2000.

-
- [17] F.C. Classe and S.K. Sitaraman. Asymmetric accelerated thermal cycles: An alternative approach to accelerated reliability assessment of microelectronic packages. In *Proceedings of the 5th Electronics Packaging Technology Conference (EPTC 2003)*, pages 81–89. IEEE, 2003.
 - [18] M. Fendler, F. Marion, D.S. Patrice, V. Mandrillon, F. Berger, and H. Ribot. Technological and electrical performances of ultrafine-pitch flip-chip assembly based on room-temperature vertical interconnection. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 1(3):291–298, 2011.
 - [19] J. Sylvestre, M. Samson, D. Langlois-Demers, and E. Duchesne. Modeling the flip-chip wetting process. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 4(12):2004–2017, 2014.
 - [20] C. Chen and N. Thammadi. Modeling and simulations of the underfill filler settling effect on the interfacial stresses of flip chip packaging. In *2006 11th International Symposium on Advanced Packaging Materials: Processes, Properties and Interface*, pages 51–56. IEEE, 2006.
 - [21] C. Chen. Effect of underfill filler settling on thermo-mechanical fatigue analysis of flip-chip eutectic solders. *Microelectronics Reliability*, 48(7):1040–1051, 2008.
 - [22] B. Cotterell, Z. Chen, J. Han, and N. Tan. The strength of the silicon die in flip-chip assemblies. *J. Electron. Packag.*, 125(1):114–119, 2003.
 - [23] J. Chen and R. Cao. *Micromechanism of cleavage fracture of metals: a comprehensive microphysical model for cleavage cracking in metals*. Butterworth-Heinemann, 2014.
 - [24] S. Lee, M. Yim, R. Master, C. Wong, and D. Baldwin. Void formation study of flip chip in package using no-flow underfill. *IEEE Transactions on electronics packaging manufacturing*, 31(4):297–305, 2008.
 - [25] V. Mylläri, T. Ruoko, J. Vuorinen, and H. Lemmetyinen. Characterization of thermally aged polyetheretherketone fibres—mechanical, thermal, rheological and chemical property changes. *Polymer Degradation and Stability*, 120:419–426, 2015.
 - [26] X. Fan, J. Zhou, and A. Chandra. Package structural integrity analysis considering moisture. In *2008 58th Electronic Components and Technology Conference*, pages 1054–1066. IEEE, 2008.
 - [27] C. Belgardt. Thermal laser separation with deep scribe for silicon wafer dicing. In *2019 International Wafer Level Packaging Conference (IWLPC)*, pages 1–6. IEEE, 2019.
 - [28] A. Hooper, J. Ehorn, M. Brand, and C. Bassett. Review of wafer dicing techniques for via-middle process 3di/tsv ultrathin silicon device wafers. In *2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*, pages 1436–1446. IEEE, 2015.
 - [29] Y. Fan, A. Arevalo, H. Li, and I. Foulds. Low-cost silicon wafer dicing using a craft cutter. *Microsystem Technologies*, 21(7):1411–1414, 2015.
 - [30] K. Kacker, S. Sidharth, A. Dubey, C.J. Zhai, and R.C. Blish. Impact of underfill fillet geometry on interfacial delamination in organic flip chip packages. In *56th*
-

- Electronic Components and Technology Conference 2006*, pages 1604–1610. IEEE, 2006.
- [31] K.M. Chen, D.S. Jiang, N.H. Kao, and J.Y. Lai. Effects of underfill materials on the reliability of low-k flip-chip packaging. *Microelectronics Reliability*, 46(1):155–163, 2006.
- [32] M.Y. Tsai, H.Y. Chang, and M. Pecht. Warpage analysis of flip-chip pbga packages subject to thermal loading. *IEEE Transactions on Device and Materials Reliability*, 9(3):419–424, 2009.
- [33] Y. Morita, K. Arakawa, M. Todo, and M. Kaneto. Experimental study on the thermo-mechanical effects of underfill and low-cte substrate in a flip-chip device. *Microelectronics Reliability*, 46(5-6):923–929, 2006.
- [34] M. Paquet, J. Sylvestre, E. Gros, and N. Boyer. Underfill delamination to chip sidewall in advanced flip chip packages. In *2009 59th Electronic Components and Technology Conference*, pages 960–965. IEEE, 2009.
- [35] A. Trigg. Applications of infrared microscopy to ic and mems packaging. *IEEE Transactions on Electronics Packaging Manufacturing*, 26(3):232–238, 2003.
- [36] P. Aryan, S. Sampath, and H. Sohn. An overview of non-destructive testing methods for integrated circuit packaging inspection. *Sensors*, 18(7):1981, 2018.
- [37] M.C. Paquet, C. Dufort, T.E. Lombardi, and et al. Effect of underfill formulation on large-die, flip-chip organic package reliability: A systematic study on compositional and assembly process variations. In *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, pages 729–736. IEEE, 2016.
- [38] Y. Y. Ong, S. W. Ho, V. N. Sekhar, et al. Underfill selection, characterization, and reliability study for fine-pitch, large die cu/low-k flip chip package. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 1(3):279–290, 2011.
- [39] T. Sinha, T.J. Davis, T.E. Lombardi, and J.T. Coffin. A systematic exploration of the failure mechanisms in underfilled flip-chip packages. In *2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*, pages 1509–1517. IEEE, 2015.
- [40] M. Diop, M. Paquet, D. Danovitch, and D. Drouin. Void-free underfill process with variable frequency microwave for higher throughput in large flip chip package application. *IEEE Transactions on Device and Materials Reliability*, 15(2):250–257, 2015.
- [41] J. Auersperg, D. Vogel, M. Lehr, M. Grillberger, and B. Michel. Crack and damage evaluation in low-k beol structures under cpi aspects. In *2009 11th Electronics Packaging Technology Conference*, pages 596–599. IEEE, 2009.
- [42] K. Chen, Y. Guu, and T. Lin. Lead-free flip-chip packaging affects on ultralow-k chip delamination. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2(12):1985–1991, 2012.
- [43] T. Braun, K. Becker, M. Koch, V. Bader, R. Aschenbrenner, and H. Reichl. High-temperature reliability of flip chip assemblies. *Microelectronics Reliability*, 46(1):144–154, 2006.
-

-
- [44] G. Li, P. Zhu, T. Zhao, R. Sun, D. Lu, G. Zhang, X. Zeng, and C. Wong. Mesoporous silica nanoparticles: a potential inorganic filler to prepare polymer composites with low cte and low modulus for electronic packaging applications. In *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, pages 2134–2139. IEEE, 2016.
 - [45] M.A. Uddin, M.O. Alam, Y.C. Chan, and H.P. Chan. Plasma cleaning of the flex substrate for flip-chip bonding with anisotropic conductive adhesive film. *Journal of Electronic Materials*, 32(10):1117–1124, 2003.
 - [46] J. Wang. The effect of flux residue and substrate wettability on underfill flow process in flip chip packages. In *56th Electronic Components and Technology Conference 2006*, pages 7–pp. IEEE, 2006.
 - [47] P.S. Ho, Z.P. Xiong, and K.H. Chua. Study on factors affecting underfill flow and underfill voids in a large-die flip chip ball grid array (fcbga) package. In *2007 9th Electronics Packaging Technology Conference*, pages 640–645. IEEE, 2007.
 - [48] S.P. Lim, M.Z. Ding, and M. Kawano. Chip-to-wafer (c2w) flip chip bonding for 2.5 d high density interconnection on tsv free interposer. In *2017 IEEE 19th Electronics Packaging Technology Conference (EPTC)*, pages 1–7. IEEE, 2017.
 - [49] S. Luo and C.P. Wong. Influence of temperature and humidity on adhesion of underfills for flip chip packaging. *IEEE Transactions on Components and Packaging Technologies*, 28(1):88–94, 2005.
 - [50] J.J. Licari and D.W. Swanson. *Adhesives technology for electronic applications: materials, processing, reliability*.
 - [51] S. Rzepka, M.A. Korhonen, E. Meusel, and C. Li. The effect of underfill and underfill delamination on the thermal stress in flip-chip solder joints. 1998.
 - [52] C.J. Zhai, U. Ozkan, A. Dubey, R.C. Blish, R.N. Master, et al. Investigation of cu/low-k film delamination in flip chip packages. In *56th Electronic Components and Technology Conference 2006*, pages 709–717. IEEE, 2006.
 - [53] M. Rahim, J. Suhling, R. Jaeger, and P. Lall. Fundamentals of delamination initiation and growth in flip chip assemblies. In *Proceedings Electronic Components and Technology, 2005. ECTC’05.*, pages 1172–1186. IEEE, 2005.
 - [54] C.J. Zhai, S.S. Too, and R.N. Master. Reliability modeling of lidded flip chip packages. In *2007 Proceedings 57th Electronic Components and Technology Conference*, pages 1091–1096. IEEE, 2007.
 - [55] I. Nnebe, S. Park, and C. Feger. Using single-wall carbon nanotubes and raman spectroscopy to measure local stresses in first-level flip-chip organic packages. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 1(10):1601–1607, 2011.
 - [56] J.P. Dempsey. Power-logarithmic stress singularities at bi-material corners and interface cracks. *Journal of Adhesion Science and Technology*, 9(2):253–265, 1995.
 - [57] X. Fan, H. Wang, and T. Lim. Investigation of the underfill delamination and cracking in flip-chip modules under temperature cyclic loading. *IEEE Transactions on Components and Packaging Technologies*, 24(1):84–91, 2001.
-

-
- [58] A.Q. Xu and H.F. Nied. Finite element analysis of stress singularities in attached flip chip packages. *Journal of Electronic Packaging*, 122(4):301–305, 2000.
- [59] H.L. Groth. Stress singularities and fracture at interface corners in bonded joints. *International Journal of Adhesion and Adhesives*, 8(2):107–113, 1988.
- [60] S.S. Pageau and S.B. Biggers Jr. Finite element evaluation of free-edge singular stress fields in anisotropic materials. *International Journal for Numerical Methods in Engineering*, 38(13):2225–2239, 1995.
- [61] J. Lee and H. Gao. A generalized comninou contact model for interface cracks in anisotropic elastic solids. *International journal of fracture*, 67(1):53–68, 1994.
- [62] A. Dimitrov, H. Andra, and E. Schnack. Efficient computation of order and mode of corner singularities in 3d-elasticity. *International Journal for Numerical Methods in Engineering*, 52(8):805–827, 2001.
- [63] E. Glushkov, N. Glushkova, and O. Lapina. 3-d elastic stress singularity at polyhedral corner points. *International Journal of Solids and Structures*, 36(8):1105–1128, 1999.
- [64] J. Van Vroonhoven. Effects of adhesion and delamination on stress singularities in plastic-packaged integrated circuits. *Journal of Electronic Packaging*, 115:28–33, 1993.
- [65] S. Swaminathan, K.K. Sikka, R.F. Indyk, and T. Sinha. Measurement of underfill interfacial and bulk fracture toughness in flip-chip packages. *Microelectronics Reliability*, 66:161–172, 2016.
- [66] H. Tada, P. Paris, and G. Irwin. The analysis of cracks handbook. *New York: ASME Press*, 2:Part 2, 2000.
- [67] G.C. Sih and B. Macdonald. Fracture mechanics applied to engineering problems-strain energy density fracture criterion. *Engineering Fracture Mechanics*, 6(2):361–386, 1974.
- [68] ASTM. Standard test method for measurement of fracture toughness. *ASTM, E1820-01*, pages 1–46, 2001.
- [69] M. Arai, Y. Noro, K. Sugimoto, and M. Endo. Mode i and mode ii interlaminar fracture toughness of cfrp laminates toughened by carbon nanofiber interlayer. *Composites Science and Technology*, 68(2):516–525, 2008.
- [70] A.B. De Moraes, A.B. Pereira, M. De Moura, and A.G. Magalhães. Mode iii interlaminar fracture of carbon/epoxy laminates using the edge crack torsion (ect) test. *Composites Science and Technology*, 69(5):670–676, 2009.
- [71] H. Lavoie, M.C. Paquet, J. Sylvestre, S. Ouimet, E. Duchesne, S. Barbeau, M. Gauvin, and V. Oberson. From leaded to lead free assembly and new packaging technology challenges. In *2007 Proceedings 57th Electronic Components and Technology Conference*, pages 1333–1339. IEEE, 2007.
- [72] S. Park, Z. Tang, and S. Chung. Temperature effect of interfacial fracture toughness on underfill for pb-free flip chip packages. In *2007 Proceedings 57th Electronic Components and Technology Conference*, pages 105–109. IEEE, 2007.
-

-
- [73] X. Dai, M. Brillhart, and P. Ho. Adhesion measurement for electronic packaging applications using double cantilever beam method. *IEEE Transactions on Components and Packaging Technologies*, 23(1):101–116, 2000.
 - [74] D. Shin, J. Lee, C. Yoon, G. Lee, J. Hong, and N. Kim. Development of single cantilever beam method to measure the adhesion of thin film adhesive on silicon chip. *Engineering Fracture Mechanics*, 133:179–190, 2015.
 - [75] M. Paquet, M. Gaynes, E. Duchesne, D. Questad, L. Bélanger, and J. Sylvestre. Underfill selection strategy for pb-free, low-k and fine pitch organic flip chip applications. In *56th Electronic Components and Technology Conference 2006*, pages 1595–1603. IEEE, 2006.
 - [76] S. Akbari, A. Nourani, and J.K. Spelt. Effect of adhesive fillet geometry on bond strength between microelectronic components and composite circuit boards. *Composites Part A: Applied Science and Manufacturing*, 87:228–236, 2016.
 - [77] S. Yashiro, Y. Sakaida, Y. Shimamura, and Y. Inoue. Evaluation of interfacial shear stress between multi-walled carbon nanotubes and epoxy based on strain distribution measurement using raman spectroscopy. *Composites Part A: Applied Science and Manufacturing*, 85:192–198, 2016.
 - [78] W. Qiu, C. Cheng, R. Liang, C. Zhao, Z. Lei, Y. Zhao, L. Ma, J. Xu, H. Fang, and Y. Kang. Measurement of residual stress in a multi-layer semiconductor heterostructure by micro-raman spectroscopy. *Acta Mechanica Sinica*, 32(5):805–812, 2016.
 - [79] I. Nnebe, S. Park, and C. Feger. Direct measurement of local stress in first-level flip-chip organic packages. In *2010 Proceedings 60th Electronic Components and Technology Conference (ECTC)*, pages 1266–1272. IEEE, 2010.
 - [80] B. Pan, K. Qian, H. Xie, and A. Asundi. Two-dimensional digital image correlation for in-plane displacement and strain measurement: a review. *Measurement Science and Technology*, 20(6):062001, 2009.
 - [81] M.A. Sutton, W.J. Wolters, W.H. Peters, W.F. Ranson, and S.R. McNeill. Determination of displacements using an improved digital correlation method. *Image and Vision Computing*, 1(3):133–139, 1983.
 - [82] B. Pan. Recent progress in digital image correlation. *Experimental Mechanics*, 51(7):1223–1235, 2011.
 - [83] A.D. Kammers and S. Daly. Digital image correlation under scanning electron microscopy: methodology and validation. *Experimental Mechanics*, 53(9):1743–1761, 2013.
 - [84] K. Hamdi, G. Moreau, and Z. Aboura. Digital image correlation, acoustic emission and in-situ microscopy in order to understand composite compression damage behavior. *Composite Structures*, 258:113424, 2021.
 - [85] B.K. Bay, T.S. Smith, D.P. Fyhrie, and M. Saad. Digital volume correlation: three-dimensional strain mapping using x-ray tomography. *Experimental Mechanics*, 39(3):217–226, 1999.
-

-
- [86] B. Mobasher. Textile fiber composites: Testing and mechanical behavior. In *Textile Fibre Composites in Civil Engineering*, pages 101–150. Elsevier, 2016.
 - [87] P. Lall and J. Wei. X-ray micro-ct and digital-volume correlation based three-dimensional measurements of deformation and strain in operational electronics. In *2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*, pages 406–416. IEEE, 2015.
 - [88] P. Lall, S. Deshpande, J. Wei, and J. Suhling. Non-destructive crack and defect detection in sac solder interconnects using cross-sectioning and x-ray micro-ct. In *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, pages 1449–1456. IEEE, 2014.
 - [89] P. Lall, S. Deshpande, L. Nguyen, and M. Murtuza. Microstructural indicators for prognostication of copper–aluminum wire bond reliability under high-temperature storage and temperature humidity. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 6(4):569–585, 2016.
 - [90] Y. Yang, P.M. Square, and J. Sylvestre. Using confocal microscopy and digital image correlation to measure local strains around a chip corner and a crack front. *IEEE Transactions on Device and Materials Reliability*, 20(1):97–105, 2019.
 - [91] C. Franck, S. Hong, S.A. Maskarinec, D.A. Tirrell, and G. Ravichandran. Three-dimensional full-field measurements of large deformations in soft materials using confocal microscopy and digital volume correlation. *Experimental Mechanics*, 47(3):427–438, 2007.
 - [92] H. Wang, S. Shao, and V. et al. Pham. Quantification of underfill influence to chip packaging interactions of wlscsp. In *International Electronic Packaging Technical Conference and Exhibition*, volume 51920, page V001T01A004. American Society of Mechanical Engineers, 2018.
 - [93] Q. Wang, S. Ri, and T. Enomoto. Residual thermal strain distribution measurement of underfills in flip chip electronic packages by an inverse approach based on the sampling moiré method. *Experimental Mechanics*, pages 1–16, 2020.
 - [94] Z. Zhong, S.C. Lim, A.K. Asundi, and T.C. Chai. Micro-moire for thermal deformation investigation in electronics packaging. In *Advanced Photonic Sensors and Applications II*, volume 4596, pages 256–260. International Society for Optics and Photonics, 2001.
 - [95] S. Liu and Y. Liu. *Modeling and simulation for microelectronic packaging assembly: manufacturing, reliability and testing*. John Wiley & Sons, 2011.
 - [96] B. Xu, X. Cai, W. Huang, and Z. Cheng. Research of underfill delamination in flip chip by the j-integral method. *Journal of Electronic Packaging*, 126(1):94–99, 2004.
 - [97] Z. Zhang, C. Zhai, and R. Master. 3d fracture mechanics analysis of underfill delamination for flip chip packages. In *2008 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, pages 751–755. IEEE, 2008.
 - [98] Z. Kornain, A. Jalar, and R. Rasid. The investigation of die back edge cracking in flip chip ceramic ball grid array package (fc-cbga). *Journal of Science and Technology*, 2(1), 2010.
-

-
- [99] Q. Zhao, Y. Zhang, J. Wu, Y. Ma, and X. Feng. Failure mechanism of underfill fillet cracks in flexible wearable electronics. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 8(11):1881–1887, 2018.
 - [100] M. Yeh and C. Tsai. Reliability analysis in flip chip package under thermal cycling. In *Key Engineering Materials*, volume 261, pages 489–494. Trans Tech Publ, 2004.
 - [101] Q. Qi. Improving the component level reliability of a flip-chip ball-grid-array (fcbga) package using numerical modeling method. In *2007 8th International Conference on Electronic Packaging Technology*, pages 1–5. IEEE, 2007.
 - [102] Z. Kornain, A. Jalar, N. Amin, R. Rasid, and C. Foong. Comparative study of different underfill material on flip chip ceramic ball grid array based on accelerated thermal cycling. *American Journal of Engineering and Applied Sciences*, 3(1), 2010.
 - [103] S.W. Yoon, S.M.L. Thew, S. Lim, et al. 150-um pitch cu/low-k flip chip packaging with polymer encapsulated dicing line (pedl) and cu column interconnects. *IEEE transactions on advanced packaging*, 31(1):58–65, 2008.
 - [104] C. Chen and P.C. Karulkar. Underfill filler settling effect on the die backside interfacial stresses of flip chip packages. *Journal of Electronic Packaging*, 130:031005, 2008.
 - [105] S. Mahalingam. *Study of interfacial crack propagation in flip chip assemblies with nano-filled underfill materials*. PhD thesis, Georgia Institute of Technology, 2005.
 - [106] L. Chen, Q. Zhang, G. Wang, X. Xie, and Z. Cheng. The effects of underfill and its material models on thermomechanical behaviors of a flip chip package. *IEEE Transactions on Advanced Packaging*, 24(1):17–24, 2001.
 - [107] A. Ayhan and H. Nied. Finite element analysis of interface cracking in semiconductor packages. *IEEE Transactions on Components and Packaging Technologies*, 22(4):503–511, 1999.
 - [108] A. Needleman and V. Tvergaard. Mesh effects in the analysis of dynamic ductile crack growth. *Engineering fracture mechanics*, 47(1):75–91, 1994.
 - [109] N. Moës, J. Dolbow, and T. Belytschko. A finite element method for crack growth without remeshing. *International Journal for Numerical Methods in Engineering*, 46(1):131–150, 1999.
 - [110] J. Song, P. Areias, and T. Belytschko. A method for dynamic crack and shear band propagation with phantom nodes. *International Journal for Numerical Methods in Engineering*, 67(6):868–893, 2006.
 - [111] E. Giner, N. Sukumar, J.E. Tarancón, and F.J. Fuenmayor. An abaqus implementation of the extended finite element method. *Engineering Fracture Mechanics*, 76(3):347–368, 2009.
 - [112] Ansys Release. 18.0 mechanical user’s guide. *Ansys Inc*, 2017.
 - [113] S. Roth, P. Leger, and A. Soulaomani. A combined xfem–damage mechanics approach for concrete crack propagation. *Computer Methods in Applied Mechanics and Engineering*, 283:923–955, 2015.
 - [114] S. Mohammadi. *XFEM fracture analysis of composites*. Wiley Online Library, 2012.
-

-
- [115] F. Xue, F. Li, and J. et al. Li. Numerical modeling crack propagation of sheet metal forming based on stress state parameters using xfem method. *Computational materials science*, 69:311–326, 2013.
 - [116] J. Auersperg, S. Rzepka, and B. Michel. Aspects of chip/package interaction and 3-d integration assessed by the investigation of crack and damage phenomena in low-k beol stacks. In *2011 IEEE International Interconnect Technology Conference*, pages 1–3. IEEE, 2011.
 - [117] P. Lall, M. Kulkarni, A. Angral, D. Panchagade, and J. Suhling. Digital-image correlation and xfem based shock-reliability models for leadfree and advanced interconnects. In *2010 Proceedings 60th Electronic Components and Technology Conference (ECTC)*, pages 91–105. IEEE, 2010.
 - [118] P. Lall, M. Kulkarni, S. Shantaram, and J. Suhling. Sif evaluation using xfem and line spring models under high strain rate environment for leadfree alloys. In *International Electronic Packaging Technical Conference and Exhibition*, volume 44618, pages 281–297, 2011.
 - [119] J. Auersperg, R. Dudek, and R. et al. Jordan. On the crack and delamination risk optimization of a si-interposer for led packaging. *Microelectronics Reliability*, 54(6-7):1223–1227, 2014.
 - [120] D. Sonawane and P. Kumar. New insights into fracture of si in cu-filled through silicon via during and after thermal annealing. *Engineering Fracture Mechanics*, 238:107281, 2020.
 - [121] W. Krieger, S. Raghavan, A. Kwatra, and S. Sitaraman. Cohesive zone experiments for copper/mold compound delamination. In *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, pages 983–989. IEEE, 2014.
 - [122] M. Benzeggagh and M. Kenane. Measurement of mixed-mode delamination fracture toughness of unidirectional glass/epoxy composites with mixed-mode bending apparatus. *Composites science and technology*, 56(4):439–449, 1996.
 - [123] F.A. Gilabert, K. Van Tittelboom, E. Tsangouri, D. Van Hemelrijck, N. De Belie, and W. Van Paepegem. Determination of strength and debonding energy of a glass-concrete interface for encapsulation-based self-healing concrete. *Cement and Concrete Composites*, 79:76–93, 2017.
 - [124] D. Samet, A. Kwatra, and S. Sitaraman. Cohesive zone parameters for a cyclically loaded copper-epoxy molding compound interface. In *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, pages 1011–1018. IEEE, 2016.
 - [125] K. Park and G.H. Paulino. Cohesive zone models: a critical review of traction-separation relationships across fracture surfaces. *Applied Mechanics Reviews*, 64(6), 2011.
 - [126] M. Elices, G.V. Guinea, J. Gomez, and J. Planas. The cohesive zone model: advantages, limitations and challenges. *Engineering Fracture Mechanics*, 69(2):137–163, 2002.
 - [127] T. Chiu, H. Lin, and H. Yang. Analysis of flip-chip corner delamination using 3-d virtual crack closure technique. In *2008 International Conference on Electronic Materials and Packaging*, pages 157–160. IEEE, 2008.
-

-
- [128] V. Srinivasan, M. Miller, and S. et al. Gurrum. Delamination prediction in lead frame packages using adhesion measurements and interfacial fracture modeling. In *2011 IEEE 61st Electronic Components and Technology Conference (ECTC)*, pages 1269–1275. IEEE, 2011.
- [129] X. Gao, F. Wang, and S. Liu. Interfacial delamination analysis at chip/underfill interface and investigation of its effect on flip-chip’s reliability. In *2013 14th International Conference on Electronic Packaging Technology*, pages 954–958. IEEE, 2013.
- [130] T. Xu, Z. Wu, and H. et al. Zhang. Die edge crack propagation modeling for risk assessment of advanced technology nodes. In *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, pages 2260–2266. IEEE, 2018.
- [131] B. Debecker, K. Vanstreels, M. Gonzalez, and B. Vandeveld. Delamination in beol: analysis of interface failure by combined experimental & modeling approaches. In *2013 IEEE International Reliability Physics Symposium (IRPS)*, pages 5C–2. IEEE, 2013.
- [132] U. Ozkan and H. Nied. Finite element based three dimensional crack propagation simulation on interfaces in electronic packages. In *2008 58th Electronic Components and Technology Conference*, pages 1606–1613. IEEE, 2008.
- [133] E. Wong, Van D., A. Dasgupta, and M. Pecht. Creep fatigue models of solder joints: A critical review. *Microelectronics Reliability*, 59:1–12, 2016.
- [134] P.C. Paris. A rational analytic theory of fatigue. *The Trend in Engineering*, 13:9, 1961.
- [135] J. Zhang. Fatigue crack propagation behavior of underfill materials in microelectronic packaging. *Materials Science and Engineering: A*, 314(1-2):194–200, 2001.
- [136] S. Park, C. Feger, and I. Nnebe. Underfill acceleration factor based on thermal fatigue crack growth rate. In *2010 Proceedings 60th Electronic Components and Technology Conference (ECTC)*, pages 490–495. IEEE, 2010.
- [137] C. Gurumurthy, L. Norris, C. Hui, and E. Kramer. Characterization of underfill/passivation interfacial adhesion for direct chip attach assemblies using fracture toughness and hydro-thermal fatigue measurements. In *1998 Proceedings. 48th Electronic Components and Technology Conference (Cat. No. 98CH36206)*, pages 721–728. IEEE, 1998.
- [138] J. Cremaldi, M. Gaynes, P. Brofman, N. Pesika, and E. Lewandowski. Time, temperature, and mechanical fatigue dependence on underfill adhesion. In *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, pages 255–262. IEEE, 2014.
- [139] T. Chiu and C. Chen. A numerical procedure for simulating delamination growth on interfaces of interconnect structures. *Microelectronics Reliability*, 52(7):1464–1474, 2012.
- [140] Y. Lai, C. Chen, and T. Chiu. Analysis of fatigue delamination growth in flip-chip package. *Acta Mechanica*, 225(10):2761–2773, 2014.
-

-
- [141] A. Ayyar and N. Chawla. Microstructure-based modeling of crack growth in particle reinforced composites. *Composites Science and technology*, 66(13):1980–1994, 2006.
- [142] A. Ayyar and N. Chawla. Microstructure-based modeling of the influence of particle spatial distribution and fracture on crack growth in particle-reinforced composites. *Acta Materialia*, 55(18):6064–6073, 2007.
- [143] R.C. Williams, A.V. Phan, H.V. Tippur, T. Kaplan, and L.J. Gray. Sgbem analysis of crack–particle (s) interactions due to elastic constants mismatch. *Engineering fracture mechanics*, 74(3):314–331, 2007.
- [144] M.G. Knight, L.C. Wrobel, J.L. Henshall, and L.A. De Lacerda. A study of the interaction between a propagating crack and an uncoated/coated elastic inclusion using the be technique. *International Journal of Fracture*, 114(1):47–61, 2002.
- [145] S. Natarajan, P. Kerfriden, D. Mahapatra, and S. Bordas. Numerical analysis of the inclusion-crack interaction by the extended finite element method. *International Journal for Computational Methods in Engineering Science and Mechanics*, 15(1):26–32, 2014.
- [146] S.A. Ponnusami, S. Turteltaub, and V. Sybrand. Cohesive-zone modelling of crack nucleation and propagation in particulate composites. *Engineering Fracture Mechanics*, 149:170–190, 2015.
- [147] F. Erdogan, G.D. Gupta, and M. Ratwani. Interaction between a circular inclusion and an arbitrarily oriented crack. *Journal of Applied Mechanics*, 41:1007–1013, 1974.
- [148] Z. Li and Q. Chen. Crack-inclusion interaction for mode i crack analyzed by eshelby equivalent inclusion method. *International journal of fracture*, 118(1):29–40, 2002.
- [149] W. Wang, K. Sadeghipour, and G. Baran. Finite element analysis of the effect of an interphase on toughening of a particle-reinforced polymer composite. *Composites Part A: Applied Science and Manufacturing*, 39(6):956–964, 2008.
- [150] A. Nouy, A. Clement, F. Schoefs, and N. Moes. An extended stochastic finite element method for solving stochastic partial differential equations on random domains. *Computer Methods in Applied Mechanics and Engineering*, 197(51-52):4663–4682, 2008.
- [151] G. Stefanou. The stochastic finite element method: past, present and future. *Computer methods in applied mechanics and engineering*, 198(9-12):1031–1051, 2009.
- [152] W. Liu, T. Belytschko, and A. Mani. Probabilistic finite elements for nonlinear structural dynamics. *Computer Methods in Applied Mechanics and Engineering*, 56(1):61–81, 1986.
- [153] R. Ghanem and P. Spanos. *Stochastic finite elements: a spectral approach*. Courier Corporation, 2003.
- [154] H. Riahi, P. Bressolette, and A. Chateaneuf. Random fatigue crack growth in mixed mode by stochastic collocation method. *Engineering Fracture Mechanics*, 77(16):3292–3309, 2010.
- [155] E. Martinez, S. Chakraborty, and S. Tesfamariam. Machine learning assisted stochastic-xfem for stochastic crack propagation and reliability analysis. *Theoretical and Applied Fracture Mechanics*, 112:102882, 2021.
-

-
- [156] K.M. Hamdia, M. Silani, X. Zhuang, P. He, and T. Rabczuk. Stochastic analysis of the fracture toughness of polymeric nanoparticle composites using polynomial chaos expansions. *International Journal of Fracture*, 206(2):215–227, 2017.
- [157] Z. Qiu and Y. Zheng. Fatigue crack growth modeling and prediction with uncertainties via stochastic perturbation series expansion method. *International Journal of Mechanical Sciences*, 134:284–290, 2017.
- [158] Z. Qiu and Z. Zhang. Fatigue crack propagation analysis in structures with random parameters based on polynomial chaos expansion method. *Theoretical and Applied Fracture Mechanics*, 105:102404, 2020.
- [159] C.J. Zhai, R.C. Blish, R.N. Master, et al. Investigation and minimization of underfill delamination in flip chip packages. *IEEE Transactions on Device and Materials Reliability*, 4(1):86–91, 2004.
- [160] M. Kumagai, N. Uchiyama, E. Ohmura, R. Sugiura, K. Atsumi, and K. Fukumitsu. Advanced dicing technology for semiconductor wafer—stealth dicing. *IEEE Transactions on Semiconductor Manufacturing*, 20(3):259–265, 2007.
- [161] C.A. Cooper, R.J. Young, and M. Halsall. Investigation into the deformation of carbon nanotubes and their composites through the use of raman spectroscopy. *Composites Part A: Applied Science and Manufacturing*, 32(3-4):401–411, 2001.
- [162] P. Dharap, Z. Li, S. Nagarajaiah, and E.V. Barrera. Nanotube film based on single-wall carbon nanotubes for strain sensing. *Nanotechnology*, 15(3):379, 2004.
- [163] Y. Sun and J. Pang. Digital image correlation for solder joint fatigue reliability in microelectronics packages. *Microelectronics Reliability*, 48(2):310–318, 2008.
- [164] X.Q. Shi, Y.L. Zhang, and W. Zhou. Determination of fracture toughness of under-fill/chip interface with digital image speckle correlation technique. *IEEE Transactions on Components and Packaging Technologies*, 30(1):101–109, 2007.
- [165] D. Vogel, E. Auerswald, J. Auersperg, et al. Stress analyses of high spatial resolution on tsv and beol structures. *Microelectronics Reliability*, 54(9-10):1963–1968, 2014.
- [166] S. Brand, P. Czurratis, P. Hoffrogge, and M. Petzold. Automated inspection and classification of flip-chip-contacts using scanning acoustic microscopy. *Microelectronics Reliability*, 50(9-11):1469–1473, 2010.
- [167] G. Zhang, D.M. Harvey, and D.R. Braden. Microelectronic package characterisation using scanning acoustic microscopy. *NDT & E International*, 40(8):609–617, 2007.
- [168] K. Wolter, M. Speck, and Ro. Heinze. Reliability analysis in microelectronic packaging by acoustic microscopy. In *28th International Spring Seminar on Electronics Technology: Meeting the Challenges of Electronics Technology Progress, 2005.*, pages 436–443. IEEE, 2005.
- [169] P. Lall and J. Wei. X-ray micro-ct and dvc based analysis of strains in metallization of flexible electronics. In *2017 16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, pages 1253–1261. IEEE, 2017.
-

-
- [170] K. Cinar and I. Guven. Micro-computed tomography as a tool to investigate the deformation behavior of particulate-filled composite materials. *Journal of Engineering Materials and Technology*, 140(2), 2018.
- [171] A. Germaneau, P. Doumalin, and J. Dupré. Comparison between x-ray micro-computed tomography and optical scanning tomography for full 3d strain measurement by digital volume correlation. *Ndt & E International*, 41(6):407–415, 2008.
- [172] A. Del Campo and C. Greiner. Su-8: a photoresist for high-aspect-ratio and 3d sub-micron lithography. *Journal of Micromechanics and Microengineering*, 17(6):R81, 2007.
- [173] Y. Pan, N. Khan, M. Lu, and J. Jeon. Organic microelectromechanical relays for ultralow-power flexible transparent large-area electronics. *IEEE Transactions on Electron Devices*, 63(2):832–840, 2015.
- [174] D. Andre. <https://gitlab.com/damien.andre/pydic/>. Technical report.
- [175] M.A. Hopcroft, W.D. Nix, and T.W. Kenny. What is the young’s modulus of silicon? *Journal of Microelectromechanical Systems*, 19(2):229–238, 2010.
- [176] M. Tsai, C. Hsu, and C. Wang. Investigation of thermomechanical behaviors of flip chip bga packages during manufacturing process and thermal cycling. *IEEE Transactions on Components and Packaging Technologies*, 27(3):568–576, 2004.
- [177] J. Sylvestre. Integrated modeling of c4 interconnects. In *2007 Proceedings 57th Electronic Components and Technology Conference*, pages 1084–1090. IEEE, 2007.
- [178] M.K. Toure, P.M. Souare, S. Allard, B. Foisy, E. Duchesne, and J. Sylvestre. Cfd-based iterative methodology for modeling natural convection in microelectronic packages. In *2018 19th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, pages 1–8. IEEE, 2018.
- [179] X. Jiang, P. Lin, Y. Song, Y. Huang, B. Lian, and Q. Yao. Effect of temperature cycling on reliability of flip chip solder joint. In *2014 15th International Conference on Electronic Packaging Technology*, pages 989–991. IEEE, 2014.
- [180] P. Lall, P. Choudhury, J. Suhling, and J. Williamson. Effect of thermal aging on the interface fracture toughness of the pcb-uf interface. In *2020 19th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, pages 1395–1399. IEEE, 2020.
- [181] S. Mallampati, Z. Baig, S. Pozder, and E.C. Chua. A comparison of environmental stressing data and simulation at the corner of a test chip in a fc-bga package. In *2019 IEEE International Reliability Physics Symposium (IRPS)*, pages 1–4. IEEE, 2019.
- [182] F.X. Che, X.R. Zhang, and L. Ji. Thermal aging induced underfill degradation and its effect on reliability of advanced packaging. In *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, pages 1525–1532. IEEE, 2020.
- [183] Y. Yang, P.M. Souare, and J. Sylvestre. Direct measurements of underfill local strain using confocal microscopy and digital image correlation. In *2019 20th International*
-

- Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, pages 1–5. IEEE, 2019.
- [184] Y. Yang, F. Habib, P.M. Souare, E. Duchesne, and J. Sylvestre. A mechanistic study of underfill cracks by the confocal-dic method. In *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, pages 1087–1093. IEEE, 2020.
 - [185] Y. Chen, S.e Sun, and C. Ji. Analysis of aluminum sheets with multiple sites damage based on fatigue tests and dic technique. *International Journal of Fatigue*, 109:37–48, 2018.
 - [186] T.M. Jobin, S.N. Khaderi, and M. Ramji. Experimental evaluation of the strain intensity factor at the rigid line inclusion tip embedded in an epoxy matrix using digital image correlation. *Theoretical and Applied Fracture Mechanics*, 106:102425, 2020.
 - [187] M. Mokhtarishirazabad, P. Lopez-Crespo, B. Moreno, A. Lopez-Moreno, and M. Zanganeh. Evaluation of crack-tip fields from dic data: a parametric study. *International Journal of Fatigue*, 89:11–19, 2016.
 - [188] D. Bellett and D. Taylor. The effect of crack shape on the fatigue limit of three-dimensional stress concentrations. *International Journal of Fatigue*, 28(2):114–123, 2006.
 - [189] M. Stolarska and D.L. Chopp. Modeling thermal fatigue cracking in integrated circuits by level sets and the extended finite element method. *International Journal of Engineering Science*, 41(20):2381–2410, 2003.
 - [190] H.H. Jiun, I. Ahmad, A. Jalar, and G. Omar. Effect of laminated wafer toward dicing process and alternative double pass sawing method to reduce chipping. *IEEE Transactions on Electronics Packaging Manufacturing*, 29(1):17–24, 2006.
 - [191] R. Chaware and L. Hoang. Reliability improvement of 90nm large flip chip low-k die via dicing and assembly process optimization. In *2006 8th Electronics Packaging Technology Conference*, pages 622–626. IEEE, 2006.
 - [192] F. Dupont, S. Stoukatch, P. Laurent, S. Dricot, and M. Kraft. 355 nm uv laser patterning and post-processing of fr4 pcb for fine pitch components integration. *Optics and Lasers in Engineering*, 100:186–194, 2018.
 - [193] T. Belytschko, R. Gracie, and G. Ventura. A review of extended/generalized finite element methods for material modeling. *Modelling and Simulation in Materials Science and Engineering*, 17(4):043001, 2009.
 - [194] M.K. Toure, P.M. Souare, B. Foisy, E. Duchesne, and J. Sylvestre. Accurate modeling of forced convection cooling for microelectronic packages: Numerical and experimental thermal studies. In *2019 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, pages 525–530. IEEE, 2019.
 - [195] A. Das, A. Sinha, V.R. Rao, and K.N. Jonnalagadda. Fracture in microscale su-8 polymer thin films. *Experimental Mechanics*, 57(5):687–701, 2017.
 - [196] Y. Sun and J.H.L. Pang. Study of optimal subset size in digital image correlation of speckle pattern images. *Optics and lasers in engineering*, 45(9):967–974, 2007.
-

-
- [197] B. Pan, H. Xie, Z. Wang, K. Qian, and Z. Wang. Study on subset size selection in digital image correlation for speckle patterns. *Optics express*, 16(10):7037–7048, 2008.
- [198] R. Jiang, F. Pierron, S. Octaviani, and P.A.S. Reed. Characterisation of strain localisation processes during fatigue crack initiation and early crack propagation by sem-dic in an advanced disc alloy. *Materials Science and Engineering: A*, 699:128–144, 2017.
- [199] K.L. Lange, R.J.A. Little, and J.M.G. Taylor. Robust statistical modeling using the t distribution. *Journal of the American Statistical Association*, 84(408):881–896, 1989.
- [200] E.H. Kerner. The elastic and thermo-elastic properties of composite media. *Proceedings of the physical society. Section B*, 69(8):808, 1956.
- [201] P. Hutar and L. Nahlik. Fatigue crack shape prediction based on vertex singularity. *Applied and Computational Mechanics*, pages 44–52, 2008.
- [202] F. Mazaheri and H. Hosseini-Toudeshky. Low-cycle fatigue delamination initiation and propagation in fibre metal laminates. *Fatigue & Fracture of Engineering Materials & Structures*, 38(6):641–660, 2015.
- [203] M. Boeff, H. Ul Hassan, and A. Hartmaier. Micromechanical modeling of fatigue crack initiation in polycrystals. *Journal of Materials Research*, 32(23):4375, 2017.
- [204] J. Auersperg, D. Vogel, M.U. Lehr, M. Grillberger, and B. Michel. Crack and damage in low-k beol stacks under assembly and cpi aspects. In *2010 11th International Thermal, Mechanical & Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems (EuroSimE)*, pages 1–6. IEEE, 2010.
- [205] Q. Guo, P. Zhu, G. Li, D. Lu, R. Sun, and C. Wong. Effects of surface-modified alkyl chain length of silica fillers on the rheological and thermal mechanical properties of underfill. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 6(12):1796–1803, 2016.
- [206] L. Sun, M. Zhou, T. Sun, and X. Zhang. Effects of underfill thickness on mechanical properties and fracture behavior of si/underfill/si adhesion structures. In *2020 21st International Conference on Electronic Packaging Technology (ICEPT)*, pages 1–4. IEEE, 2020.
- [207] S. Raghavan, I. Schmadlak, and S.K. Sitaraman. Interlayer dielectric cracking in back end of line (beol) stack. In *2012 IEEE 62nd Electronic Components and Technology Conference*, pages 1467–1474. IEEE, 2012.
- [208] A. Bansal, T. Kang, and Y. Li. Reliability of high-end flip-chip package with large 45nm ultra low-k die. In *2008 58th Electronic Components and Technology Conference*, pages 1357–1361. IEEE, 2008.
- [209] K. Nguyen, E. Opiniano, and R. Mah. Backside die-edge and underfill fillet cracks induced by additional tensile stress from increasing die-to-package ratio in bare-die fcbga. In *2020 IEEE International Reliability Physics Symposium (IRPS)*, pages 1–4. IEEE, 2020.
-

-
- [210] Z. Wu, M. Nayini, C. Carey, S. Donovan, D. Questad, and E. Blackshear. Cpi reliability challenges of large flip chip packages and effects of kerf size and substrate. In *2019 IEEE International Reliability Physics Symposium (IRPS)*, pages 1–7. IEEE, 2019.
- [211] J.H. Lau, S.W.R. Lee, C. Chang, and C. Ouyang. Effects of underfill material properties on the reliability of solder bumped flip chip on board with imperfect underfill encapsulants. In *1999 Proceedings. 49th Electronic Components and Technology Conference (Cat. No. 99CH36299)*, pages 571–582. IEEE, 1999.
- [212] T. Sinha, K.K. Sikka, D.N. Yannitty, and P.F. Bodenweber. Measurements of interfacial strengths in underfilled flip-chip electronic packages using wedge delamination method (wdm). In *Fourteenth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, pages 346–354. IEEE, 2014.
- [213] JESD22-A113F. Standard for preconditioning of nonhermetic surface mount devices prior to reliability testing. *JEDEC Solid State Technology Association*, 2009.
- [214] S. Hung, C. Lee, and Y. Lin. Data science for delamination prognosis and online batch learning in semiconductor assembly process. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 10(2):314–324, 2019.
- [215] X. Yao. Evolving artificial neural networks. *Proceedings of the IEEE*, 87(9):1423–1447, 1999.
- [216] Y. Jin, Z. Yin, W. Zhou, J. Yin, and J. Shao. A single-objective epr based model for creep index of soft clays considering l2 regularization. *Engineering Geology*, 248:242–255, 2019.
- [217] A. Paszke, S. Gross, F. Massa, et al. Pytorch: An imperative style, high-performance deep learning library. *Advances in neural information processing systems*, 32:8026–8037, 2019.
- [218] L. Yao, R.C. Alderliesten, M. Zhao, and R. Benedictus. Discussion on the use of the strain energy release rate for fatigue delamination characterization. *Composites Part A: Applied Science and Manufacturing*, 66:65–72, 2014.
- [219] H. El-Emam, H. Salim, and H. Sallam. Composite patch configuration and prestraining effect on crack tip deformation and plastic zone for inclined cracks. *Journal of Composites for Construction*, 20(4):04016002, 2016.
- [220] H. El-Emam, H. Salim, and H. Sallam. Composite patch configuration and prestress effect on sifs for inclined cracks in steel plates. *Journal of Structural Engineering*, 143(5):04016229, 2017.
- [221] M. Atta, A. Abd-Elhady, A. Abu-Sinna, and H. Sallam. Prediction of failure stages for double lap joints using finite element analysis and artificial neural networks. *Engineering Failure Analysis*, 97:242–257, 2019.
- [222] K. He, X. Zhang, S. Ren, and J. Sun. Delving deep into rectifiers: Surpassing human-level performance on imagenet classification. In *Proceedings of the IEEE international conference on computer vision*, pages 1026–1034, 2015.
- [223] M. Schulz, H. Walter, R. Mroßko, et al. In situ monitoring of interface delamination by the 3ω -method. In *20th International Workshop on Thermal Investigations of ICs and Systems*, pages 1–8. IEEE, 2014.
-

-
- [224] H.T. Vo, M. Todd, F.G. Shi, et al. Towards model-based engineering of underfill materials: Cte modeling. *Microelectronics Journal*, 32(4):331–338, 2001.
-

