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Conception et Fabrication de FinFET GaN Verticaux de Puissance Normalement Bloqués

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Design and Fabrication of Normally-off Vertical GaN Power FinFET

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"To accomplish great things, we must not only act, but also dream, not only plan, but also believe."
« Anatole France »

Résumé en français

Les énormes demandes de systèmes à hautes performances motivées par des contraintes économiques ont forcé l'industrie des semi-conducteurs à réduire considérablement les dimensions des dispositifs pour compenser les propriétés physiques relativement modestes du silicium. Ces limitations ouvrent la voie aux semi-conducteurs III-V, qui sont d'excellentes alternatives au silicium et peuvent être déclinés dans de nombreuses compositions. Par exemple, le nitrure de gallium (GaN) a été considéré comme un concurrent fabuleux pour faciliter l'horizon de l'industrie des semi-conducteurs au-delà des limitations de performances du silicium en raison de sa grande mobilité, de sa large bande interdite et de ses propriétés de conductivité thermique élevées pour T>300K (Bulk GaN). Il promet de réduire les pertes dans les circuits de conversion de puissance et de réduire de 10 % la consommation d'énergie.

À l'heure actuelle, les structures latérales et verticales ont été considérées pour les dispositifs de puissance en GaN. L'immense potentiel du dispositif HEMT AlGaN/GaN provient du gaz d'électrons à haute densité et à haute mobilité formé au niveau de son hétérojonction. Le dispositif est vulnérable aux problèmes de fiabilité résultant de l'exposition fréquente à des conditions d'effondrement de champ électrique, de température et de contrainte élevés, limitant ainsi ses performances et sa fiabilité. En revanche, les dispositifs de puissance verticaux en GaN ont attiré beaucoup d'attention en raison de leur capacité à atteindre des niveaux de tension et de courant élevés sans augmenter la taille de la puce. De plus, ces dispositifs verticaux présentent des performances thermiques supérieures à leurs homologues latéraux.

Par ailleurs, les dispositifs GaN verticaux sont confrontés aux défis d'un courant de fuite élevée et de claquage se produisant aux coins du canal. Un autre défi associé aux dispositifs normalement bloqués est l'absence d'une méthode optimisée pour éliminer la diffusion de magnésium de la couche p-GaN.

Cette thèse a deux objectifs stratégiques ; premièrement, un dispositif de puissance FinFET GaN normalement bloqué a été conçu et optimisé pour surmonter les défis du FinFET vertical en GaN. Cela a été fait en optimisant les paramètres de performance tels que la tension de seuil V_{TH}, la tension de claquage V_{BR} et la résistance

spécifique à l'état passant R_{ON}. En conséquence, l'impact des paramètres structurels et physiques doit être incorporé pour avoir un processus d'optimisation précis. Par la suite, l'identification et l'optimisation d'un processus de fabrication à faible coût et de haute qualité pour la structure proposée à souligner cette thèse comme deuxième objectif.

Mots clés:

Nitrure de gallium (GaN), Simulation, TCAD Sentaurus, Normalement Bloqués, Tension de claquage (V_{BR}), Résistance à l'état passant (R_{ON}), GaN FinFET vertical, Plans cristallographiques GaN, Hydroxyde de tétraméthylammonium (TMAH), Nanofabrication, source d'abord approcher.

Abstract (in English)

The tremendous demands for high-performance systems driven by economic constraints forced the semiconductor industry to considerably scale the device's dimensions to compensate for the relatively modest Silicon physical properties. Those limitations pave the way for III-V semiconductors, which are excellent alternatives to Silicon and can be declined in many compositions. For example, Gallium Nitride (GaN) has been considered a fabulous competitor to facilitate the semiconductor industry's horizon beyond the performance limitations of Silicon due to its high mobility, wide bandgap, and high thermal conductivity properties for T>300K (Bulk GaN). It promises to trim the losses in power conversion circuits and drive a 10 % reduction in power consumption.

Both lateral and vertical structures have been considered for GaN power devices. The AlGaN/GaN HEMT device's immense potential comes from the high density, high mobility electron gas formed at its heterojunction. The device is vulnerable to reliability issues resulting from the frequent exposure to high electric field collapse, temperature, and stress conditions, thus limiting its performance and reliability. Contrariwise, the vertical GaN power devices have attracted much attention because of the potential to reach high voltage and current levels without enlarging the chip's size. Furthermore, such vertical devices show superior thermal performance to their lateral counterparts.

Meanwhile, Vertical GaN devices have the challenges of high leakage current and the breakdown occurring at the corners of the channel. Another challenge associated with Normally off devices is the lack of an optimized method for eliminating the magnesium diffusion from the p-GaN layer.

This thesis has two strategic objectives; Firstly, a Normally-OFF GaN Power FinFET has been designed and optimized to overcome the vertical GaN FinFET challenges. It was done by optimizing the performance parameters such as threshold voltage V_{TH}, high breakdown V_{BR}, and the specific ON-state-resistance R_{ON}. Accordingly, the impact of both structural and physical parameters should be incorporated to have an exact optimization process. Afterward, the identification and optimization of a low-cost and high-quality fabrication process for the proposed

structure underlined this thesis as the second objective.

Keywords:

Gallium Nitride (GaN), Simulation, TCAD *Sentaurus,* Normally-OFF , Breakdown Voltage (V_{BR}), On-state resistance (R_{ON}), Vertical GaN FinFET, GaN crystallographic planes, Tetramethylammonium hydroxide (TMAH), Nanofabrication, source first approach.

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List of Abbreviations and Acronyms

AlGaN	Aluminum Gallium Nitride
AlN	Aluminum Nitride
InAlN	Indium Aluminum Nitride
GaN	Gallium Nitride
GaAs	Gallium Arsenide
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon Germanium
InP	Indium Phosphide
FET	Field-effect transistor
HEMT	High Electron Mobility Transistor
RF	Radio Frequency
LDMOS	Laterally diffused metal oxide semiconductor
MESFET	Metal–Semiconductor Field-Effect Transistor
MOSHEMT	Metal-Oxide-Semiconductor High Electron Mobility Transistor
CAVET	Current aperture Vertical Electron Transistor
VHFET	Vertical Heterojunction Field-Effect Transistor.
MOSFET	Metal Oxide Semiconductor vertical field effect Transistor
UID gallium	Unintentionally doped GaN
CBLs	Current blocking layers
HBL	Hybrid blocking layers
2DEG	Two-dimensional electron gas
MOCVD	Metal-organic chemical vapor deposition
MBE	Molecular Beam epitaxy
FOM	Figure of merit
JFM	Johnson's face merit of merit
KFM	Keye's figure of merit
BFM	Baliga's Figure of Merit
TMAH	Tetramethylammonium hydroxide
EBL	Electron Beam Lithography
V_{TH}	Threshold voltage
R_{ON}	Specific on-state-resistance
V_{BR}	Breakdown voltage
L_{GTG}	Gate to Gate Length
EBR	Edge Bead Removal
AFM	Atomic Force Microscopy
SEM	Scanning Electron Microscopy
RTA	Rapid Thermal Annealing
OD	Orientation Determination
AOE	Advanced Oxide Etching
ICP-RIE	Inductively Coupled Plasma Reactive-Ion Etching

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General Introduction

For more than five decades, Silicon has been the backbone of the semiconductors industry. However, Silicon technology reaches maximum theoretical limits on how much it can be improved. Gallium Nitride (GaN) has been mostly steadfast in its superior material properties; extensive and diverse research is being targeted at the viability of GaN-based systems for commercial or industrial requirements and consumer-specific demands. GaN is exceptionally robust, with high tolerance to temperatures and voltages, and highly relevant in high power and frequency domains. GaN-based systems are predicted to occupy a significant share of the semiconductor market over the next decade and promise huge economic advantages with continued development [1].

AlGaN/GaN HEMT has outstanding possibilities in several applications referring to its AlGaN/GaN heterostructure, which empowers extreme mobility and density channel. Both piezoelectric and spontaneous polarization charges at the interfaces create the two-dimensional electron gas, which can deliver high current densities without the requirement of an external bias or doping. However, those outstanding capabilities of GaN HEMT are criticized by several degradation mechanisms that limit performance and worsen the reliability and lifetime[2]. Also, the distinctive physical features that allow the advantages of these devices are complicating reliability investigations of GaN HEMTs[3]. Currently, an intensive focus of GaN research is carried out toward a comprehensive understanding of physics behind the challenges and trends that oversteer GaN devices to enrich the technological development in this paradigm[4].

Large-scale investments, e.g., by Google and BMW, GaN systems, IEPC, SAMSUNG, etc. have been undertaken into optimizing GaN-based technologies for implementation into varied circuit architectures and packaging solutions that could set qualification criteria for the next phase of research and fabrication chain roadmap towards higher performance systems[5]. However, the significant correspondent of several obtrusive and reliability issues is the GaN crystal quality within the device epi-structure. This contributor plays a principal role in channel density restriction and the aggravation of the device performance[6]. Despite trap-induced limitations, academic and industrial corporations have made advances in GaN HEMT reliability improvement to sustain the acceleration

in GaN markets. However, there is a need to build transistors capable of capitalizing on the true potential of III-N materials[7]. To date, the GaN-based technologies are used in power electronics with horizontal transistors field-effect, such as an insulated gate on a specific heterostructure (MOS) HEMTs. However, by its side operation, this architecture has two major challenges. The first is a strong device self-heating, and the second consists of a strong electric field close to the device surface [8].

A new structure of vertical GaN transistor has been proposed in the literature to overcome the mentioned challenges. The more uniform distribution of the current and the electric field across the device is a good solution for HEMT challenges due to its valuable improvement for heat dissipation resulting from self-heating generated.

The current in vertical devices flows through the device bulk, so the heat dissipation is much more uniform than lateral devices. Meanwhile, the vertical GaN device features many advantages; high breakdown voltage, the ultra-low leakage current, better reliability due to shifting of the electric field from the surface, reduced dynamic on-state resistance and current collapse, flexibility for Normally-OFF controllability, and the ability to design a drift region to obtain higher breakdown voltage are advantages of vertical structure transistors.

There are several types of Vertical GaN transistors; the main ones are the VHFET (Vertical heterojunction field-effect transistor)[9], the MOSFET (Metal-oxide-semiconductor vertical field-effect-transistor)[10], and CAVETs (Current aperture vertical electron transistor)[11]. In terms of threshold voltage, on-state resistance, and breakdown voltage, studies on these devices have an active research domain even with the condition that this technology is still under development and optimization.

A vertical transistor based on n-type GaN MOSFET (also known as Vertical GaN FinFET) structure has been designed in this thesis with a fully optimized fabrication process. The device has an operative threshold voltage around 0.71V, voltage breakdown greater than 1500 V, and resistance less than $1m\Omega.cm^2$. First, the design simulation and optimization of the normally-off vertical GaN power FinFET fabrication process has been carried out using TCAD *sentaurus*. Explicit, the starting structure is built based on the one reported by the Sun *et al*. group[12]. The physical models used for the simulation and optimization are then calibrated based on such structure.

The optimization process incorporates various physical and structural parameters and investigates their impact on the device's overall performance. Consequently, the final fabrication process has been identified. Four critical processing modules are adhered to in the optimization process, the orientation determination (OD), the source deposition (OH), the GaN etching (GaN), and the gate metallization (GM).

Overall, these fruitful efforts led to a fully optimized process to fabricate the vertical GaN FinFET transistor with low-cost and novel processing modules. This work will expand by fabricating the vertical GaN FinFET device. In addition, the capability to compare the electrical performance of a-GaN and m-GaN crystal-oriented devices will provide important information about how to optimize new versions from the device being fabricated with capable of operating within its theoretical limits concerning R_{ON} and V_{BR}.

CHAPTER ONE: GAN POWER TECHNOLOGY STATUS AND CHALLENGES

1.1 The Growth of GaN's industry

The superior performance advances of GaN-based devices are reported across market-driven fields such as high-frequency communications, photonics, RF power devices, high power conversion, and control, which aids corporations and commences in sustaining the rapidly evolving demands metrics. The inherent robustness capably addresses modern markets for compact, rugged, and highly reliable automotive, defense, and space applications. GaN engineering is promising in meeting key performance needs and the potential for sustained economic rewards on maturity.

1.1.1 Device Power Market

The core necessities for a successful power semiconductor technology are efficiency, reliability, and cost-efficiency. In 2009, EPC released the first mode enhancement GaN (EGAN) field-effect transistor (FET) to replace power MOSFETs[13]. The market for GaN has grown considerably since that time. The current distribution and projection of the energy market are shown in Figure 1.

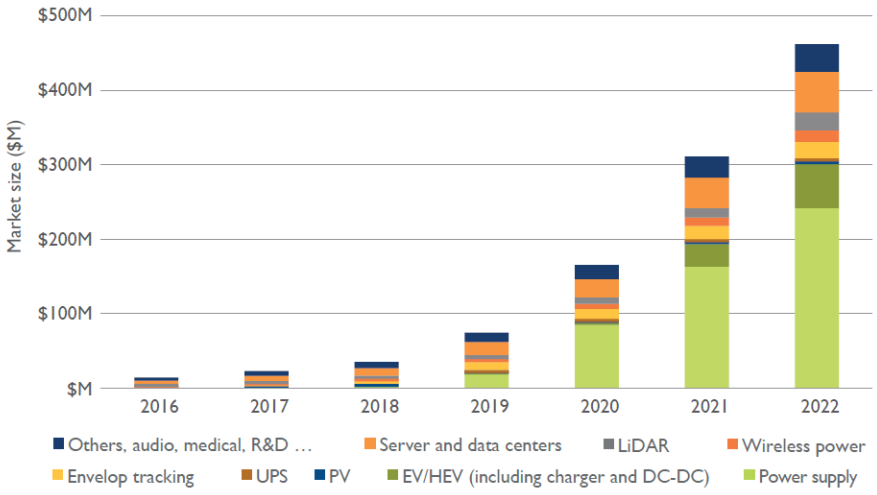

Figure 1:Predictive distribution of the energy market GaN[13] compiled in 2017 for supporting applications, including food, energy, wireless, electric/hybrid electric vehicles (EV / HEV), sources of uninterruptible power supply (UPS), Photovoltaics

The main organizations led the first generation of energy production reliable GaN on innovative territories Transphorm, Infineon, EPC, Navitas, Dialog, and GaN Systems[4][3][5][8]. They have reported impressive improvements for GaN-based devices concerning the current ranges, switching frequency, and breakdown voltages while having different milestones on fabrications and design. The power supply has been expected to remain a major player in the market growth in 2022. LIDAR (Light Detection and Ranging) and wireless power and monitoring of the envelope are good additions to the low voltage segment/average since GaN is particularly well suited to managing their specific needs. Velodyne LIDAR accelerates 3D sensors for load, and wireless solutions are available from companies like EPC, Apple, and Starbucks. As power converters for the general automobile, the GaN electric vehicle and hybrid electric (EV / HEV) market could be very useful soon due to the raised demand for high-speed switching efficiency GaN. GaN performance advantages offer the original investment and profits running, looking into the next phase prioritizes devices fabricated as shown in Figure 2.

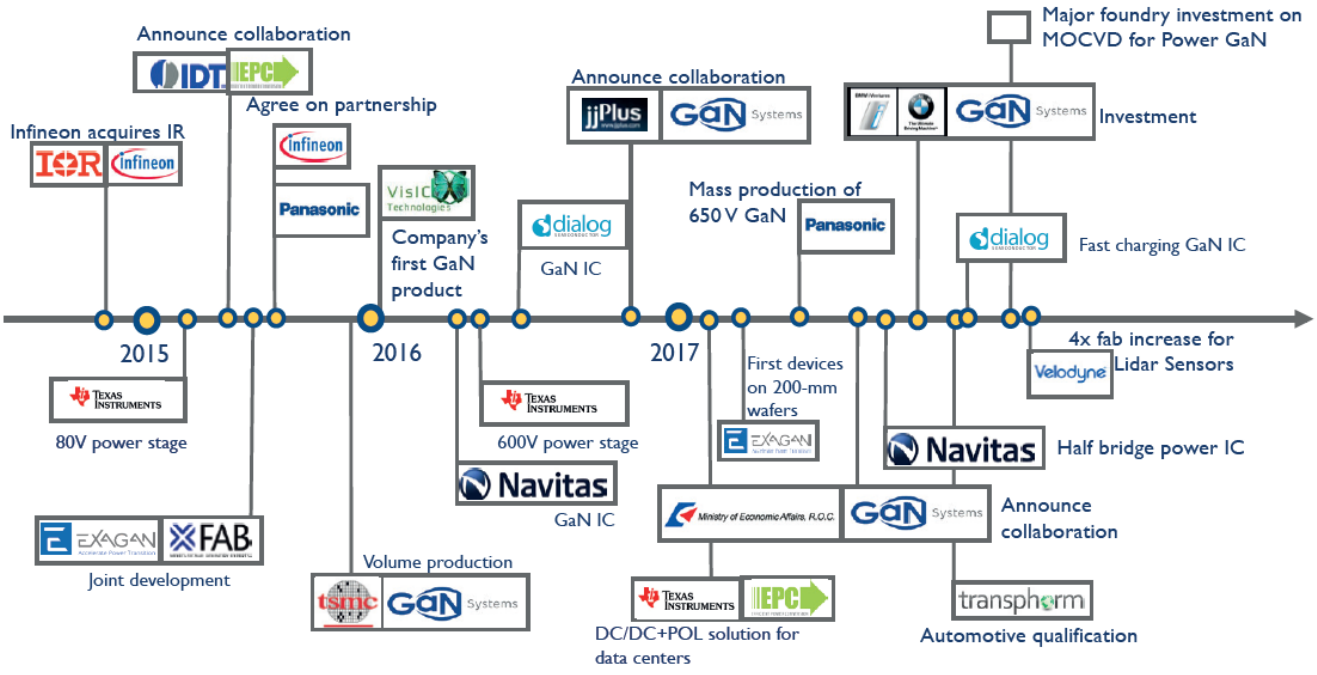

Figure 2:Business investment GaN by companies established in 2017 [14]

Commercially viable large-area substrates are very close to being launched for power conversion applications. Foundries continue optimistically to mass production of GaN devices undertake huge investments in handling

capacity and fabrication, such as the recent partnership with Navitas TSMC and Amkor. Panasonic announced the mass production of its 650 V devices while several other companies are in the final phase of R & D, which should soon be ready for the start. Working with GaN Systems, which recently received an investment from BMWi Ventures, the Taiwan Ministry of Economic Affairs encourages applications for GaN green energy.

1.1.2 GaN RF Market

The RF market focuses on the initial interest and research in GaN development and continues to expand with new industry solutions. Both established and upcoming companies involved in the production, such as Sumitomo Electric, Infineon, Wolfspeed, Qorvo, NXP Semiconductors, Mitsubishi Electric, GaN Systems, United Monolithic Semiconductors (UMS), M A / COM, Ampleon, RFHIC, Northrop Grumman, and Anadigics. There are different structures to have normally-off GaN HEMTs for high-frequency applications, e.g., the "cascade HEMT," the "p-GaN gate," and the "recessed gate."Accordingly, the hybrid MISHEMT has already been commercialized despite the difficulty of having optimized p-GaN layers [15]. Telecommunications and the military are the key markets for GaN RF technology, as presented in Figure 3.

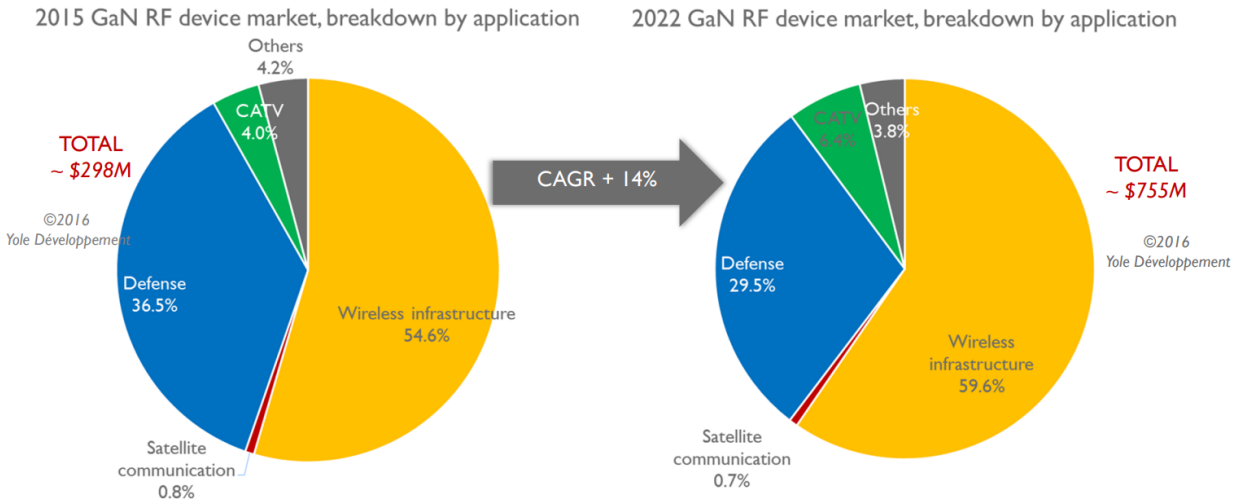

Figure 3:GaN RF market breakdown by an application between 2015-2022, including major telecommunications and military contributions predicting an annual growth rate of 23% to an estimated $ 1.3 billion of 2023[16].

Because GaN can exhibit a higher-power efficiency level than laterally diffused semiconductor metal oxide semiconductor (LD MOS) and GaAs, It is considered an important advantage for high-frequency

telecommunications networks[16]. Different sectors of RF energy are wireless infrastructure, wired broadband, satellite communications, coaxial cable and fiber, military, and aerospace.

1.2 Introduction to GaN Physics

1.2.1 GaN crystallographic structure

Gallium nitride crystallizes in two different forms: the hexagonal form, called Wurtzite, or the cubic form, called Zinc Blende. The crystal structure, commonly obtained, of GaN is hexagonal (the Wurtzite phase), it consists of two hexagonal networks, one with gallium atoms (Ga), the other with nitrogen atoms (N), interpenetrated and shifted along the c axis by 5 /8th of the elementary cell [17]. Its mesh parameters are a= 3.189Å and c = 5.186Å. The other metastable crystalline form of GaN is the cubic form (called Zinc Blende), with a lattice parameter a= 4.52Å. The layers of GaN in the cubic phase are generally grown on a silicon substrate. Due to the differences in lattice parameters and thermal expansion coefficients between Si ($\Delta a = 3.17\times10^{-6}K^{-1}$) and GaN ($\Delta a = 3.17\times10^{-6}K^{-1}$ and $\Delta c = 3.17\times10^{-6}K^{-1}$), the epitaxial GaN layers in the Zincblende phase have a very high defect density, which therefore limits their use.

Figure 4 illustrates the crystal structure of GaN (a) in its hexagonal structure (b) highlights the common polar, semipolar, and non-polar GaN crystallographic planes [18][19].

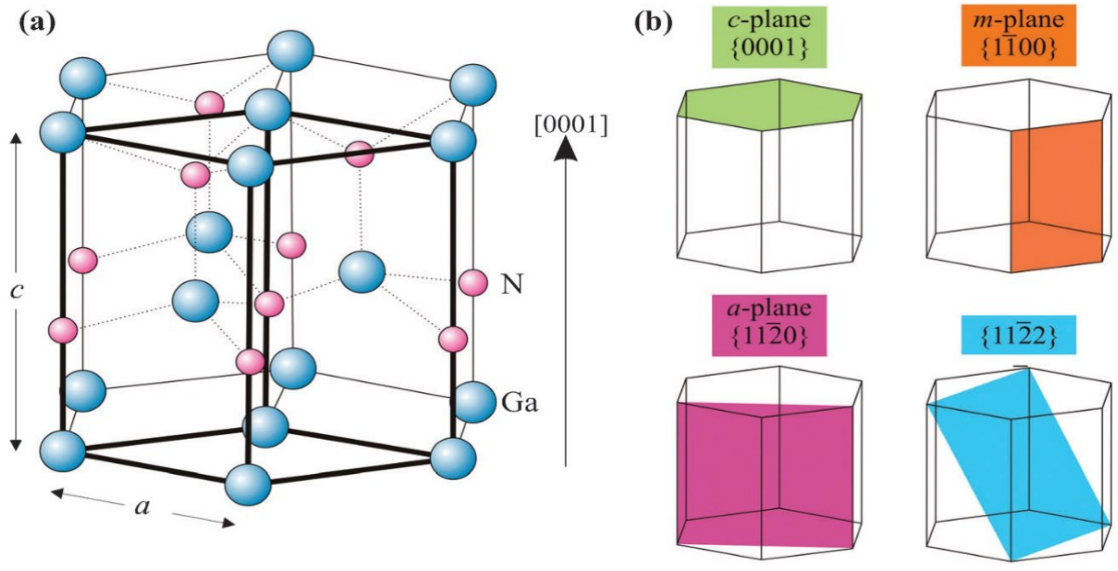

Figure 4:Crystal structure of GaN (a)Wurtzite Phase, (b) highlights the polar c-plane, the nonpolar a-, and m-planes, and the semi-polar plane [18][19].

The map of different III-V materials with their corresponding crystal structures is shown in Figure 5

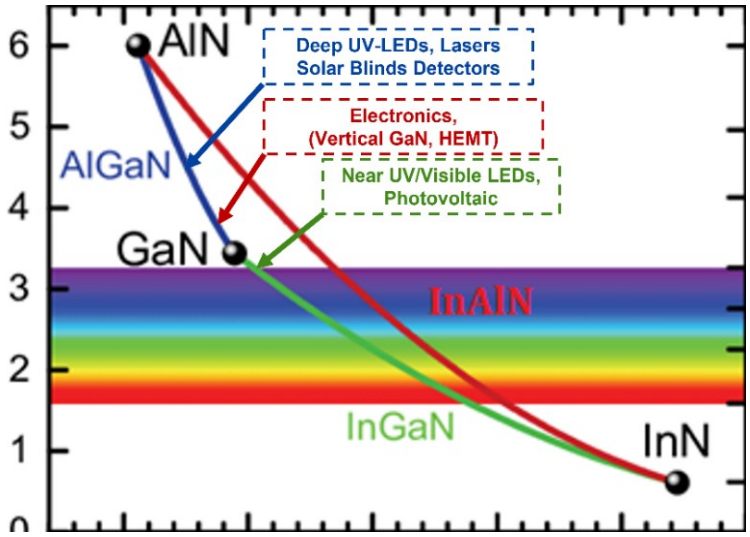

Figure 5:Map of distribution of III-V materials and their alloys according to their mesh sizes and their forbidden bands [24]

1.2.2 The electrical properties Of Gallium Nitride

The III-Nitride group semiconductors exhibit fascinating properties, giving AlN and GaN huge advantages for high power and high-frequency applications. Table 1 presents the inherent properties of the end of the III-N semiconductor. Because of the wide E_g (GaN = 3.4 eV, AlN = 6.2eV), these materials have minimal intrinsic doping concentrations for temperature up to 1000°C. It will make them rugged and thermally stable for high voltage applications. Associated systems and thus can withstand high temperatures junction current breakdown voltage V_{BR} beyond 1 kV. Besides, their wurtzite lattice structures include strong ties, promoting high and long-term stability. It promotes several automotive and aircraft applications such as high voltage and rectifier or high voltage converters. There is a critical trade-off between breakdown voltage V_{BR} of the transistor and its cut-off frequency f_T bring specific advantages.

Derivation of those balances described their *E*c as the critical electric field, and the path l of the electron is represented as follows[19];

$$V_{BR}(Volt) = E_C(\frac{Volt}{m}) \times l(m) \tag{1.1}$$

$$f_T(Hz) = \frac{1}{2\pi\tau(second)} = \frac{v_{sat}(\frac{m}{second})}{2\pi l(m)} \tag{1.2}$$

$$JFM(V/s) = V_{BR}f_T(Volt.Hz) = \frac{E_C v_{sat}}{2\pi} \tag{1.3}$$

Therefore, the product is constant, known as the character of Johnson's talent (JFM). The electron-hole pairs created by impact ionization require hot carriers with an energy equivalent to E_G. GaN wide bandgap and thus, like SiC, allows very high Ec. Besides, the saturation velocity v_{SAT} is also significantly higher for GaN because of the great energy separation between the conduction band valleys, limiting other Valley transitions under high electric fields[19]. Therefore, it gives excellent JFM values for GaN compared to Si and GaAs.

Table 1:Properties and advantages of III-Nitride semiconductors in comparison to other semiconductor candidates at room temperature [25–27]

Property	Si	GaAs	SiC	GaN
Bandgap Eg (eV)	1.12	1.42	3.25	3.4
Intrinsic Carrier Density ni (cm^{-3})	1.45×10^{10}	1.79×10^{6}	1.16×10^{-8}	1.67×10^{-10}
Breakdown Field EBR (MV cm^{-1})	0.3	0.4	3.5	4.0
Johnson's figure of merit (~ Si)	1.0	2.7	20	27.5
Baliga's figure of merit (@ E= 500 kV/cm)	1.0	9.6	3.1	24.6
Saturated Drift Velocity vd (10^7 cm s^{-1})	1.0	2.0	2.0	3.0
Electron Mobility μ ($cm2V^{-1}s^{-1}$)	1350	6000	650	1000-2000
Thermal conductivity κ (W cm^{-1} K)	1.5	0.5	4.9	1.7

The figure of merit of Baliga (BFOM) identifies material parameters that minimize conduction losses in low-frequency unipolar transistors. It can be represented as $BFOM = \mu e E_C^3$ where GaN is again mastering other technologies[20]. Unlike SiC, which suffers from low electron mobility [5]. Thus, GaN devices can dominate the power electronics market because of their ability to operate at high frequencies and high power [4, 29]. The material power density itself is ten times that of GaAs devices [22]. The associated high power per unit. Width translates into easier fabrication and smaller devices with high impedance, making them easier to match into the system. In comparison, a matching ratio ten times higher might be necessary for a GaAs transistor. In addition, the need for voltage and power conversion is also obviated. The high thermal conductivity helps with reducing the need for expensive and complex cooling systems. It is especially significant because the cost and weight of cooling systems

constitute an important portion of the building costs of a high-power microwave transmitter. The overall compactness of weight, volume, and cost is also crucial for space-targeted devices. Also, this makes GaN strategically competent to counteract global warming through utilization in major production systems. The high E_c in conjunction with the ability to create a heterostructure and conduct two-dimensional electron gas (2DEG) channel on V_G= 0V due to the positive polarity provides simultaneous high current and high voltage operation and low Ron (<50 mΩ @ 30 A)[23]. As a result, you can build highly efficient (> 99%) and small, cost-effective systems with high breakdown voltages that guarantee high working voltage conditions off. The high RF and microwave performances of III-N materials are related to their high electron velocity v_{sat} and excellent cut-off frequencies. GaN-based systems also have low noise figures of merit, minimal power dissipation, and low R_{ON} value[24]. Due to excellent R_{ON} vs. V_{BR} ratios under identical on-resistance conditions, the superior switching capability of GaN will yield significantly lower losses than the Si device[13]. Thus, the driving needs of RF power applications such as the ever-expanding wireless communication field are well achieved. This domain is also strategic for military, civil and space applications such as C band satellite communications, Ku-K small aperture terminal, and digital radio and radar systems[25].

1.3 GaN Substrates options

In addition to the bulk GaN substrate, there are three conventional substrate options in which the GaN epitaxy process is performed, which are; Sapphire (Al_2O_3), Silicon carbide (SiC), and silicon (Si) substrates. Each has advantages and disadvantages to consider. Figure 6 represents the salient advantages and disadvantages of each. The gallium nitride substrate is the ideal option for the growth of a homo-epitaxial device fabrication device since it would automatically absorb issues related to heteroepitaxy[26]. However, GaN still needs significant optimization that can be replaced before the other substrates. The Garden synthesis bulk process is complicated because of the very high melting point of GaN ° C ~ 2800 [27]. At high temperatures, the equilibrium vapor pressure of nitrogen is very high, and high pressures are required (Bar 2000) to combine N and finally grow GaN. The technique is to grow very thick (> 100 micrometers) by Hydride Vapor layers Phase Epitaxy (HVPE) and to use unto them as

"quasi" substrates [28]. While other techniques are employed for producing bulk GaN crystals, only high-pressure growth from solutions such as HVPE has produced large area crystals.

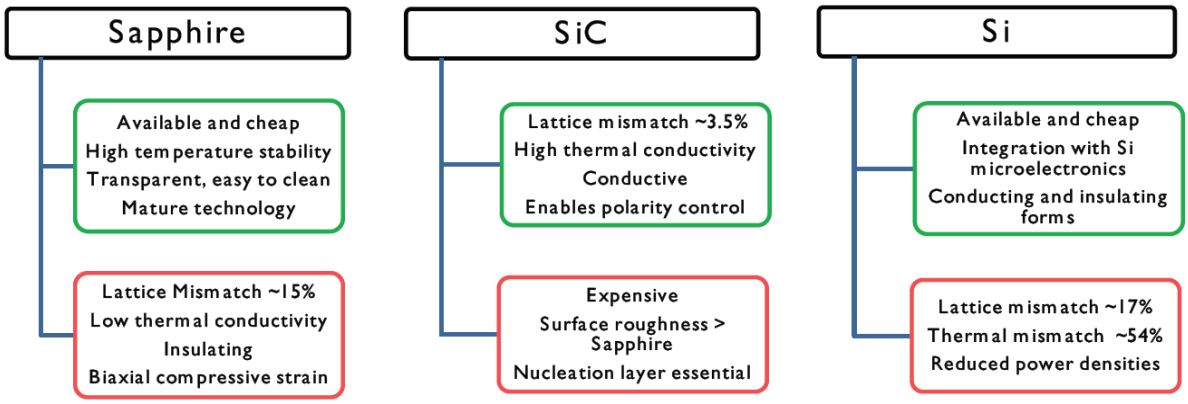

Figure 6: Advantages and drawbacks of substrates options for GaN epitaxy

However, the ammonia-thermal method proves to be a good contender to HVPE [29]. Despite the low quality and defect densities that would eliminate other technologies, the power and reliability metrics make GaN still promising for the future pending further research.

1.4 Lateral GaN HEMTs Transistors

The AlGaN ternary alloy, whose energy band gap and the lattice parameter may vary depending on the aluminum concentration in the material, of heterostructures such as HEMTs (high electron mobility transistor) shown in Figure 7, can be fabricated.

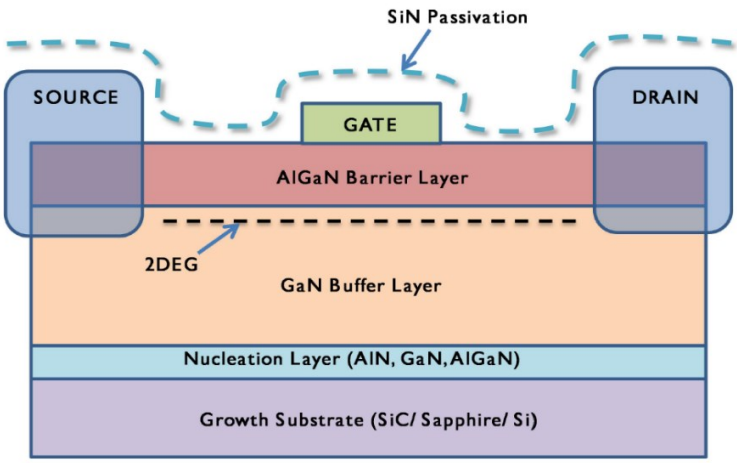

Figure 7: Structure of an AlGaN / GaN HEMT [39].

Unlike conventional HEMTs made of modulation-doped semiconductor heterostructures, no intentional doping is required to generate two-dimensional electron gas (2DEG) at the AlGaN/GaN interface., the heterojunction AlGaN / GaN enables the formation of a free-electron gas (2DEG) in a high surface density (~ 1×10^{13} cm^{-2}) whose mobility is two times that GaN by volume[30]. Explicit, in the 2DEG channel, the electrons are moving in two dimensions but tightly confined in the third. Since electron confinement generates quantized energy levels for their movements in the third direction, it appears as a 2D sheet embedded in a 3D environment[31].

1.4.1 Enhanced HEMTs Transistors

To date, the threshold voltage (MOS) HEMTs corresponding to the gate voltage required to implement the normally-off operation since the electron channel is formed without using gate voltage through the heterojunction AlGaN / GaN. However, it is recommended to have positive threshold voltages for safety reasons in power electronics.

Several approaches have been proposed in the Literature to obtain enhanced HEMTs structures. For example, the decrease in the carrier density in the 2DEG can be accomplished by decreasing the aluminum levels in the AlGaN layer. Nevertheless, this non-localized depletion significantly increases specific resistance R_{ON}, which is undesired. A second approach has been proposed to deplete the channel only under the gate by reducing the thickness of the AlGaN under the plasma etching gate electrode. However, this approach requires high precision control, and damage from plasma can cause an increase in leakage current by the gate and non-uniformity of the threshold voltage [38].

A third approach has been considered with a dielectric layer, such as SiO_2, placed between the gate and the heterostructure AlGaN / GaN to form an MIS-HEMT (Metal / Insulator / Semiconductor). However, the dielectric impact of the channel mobility and stability of threshold voltage [39]. Thus, to enhance HEMT, a promising and very recently studied alternative is to deposit a layer of p-GaN between the gate and the heterostructure. In this case, the p-GaN layer is used to deplete the 2DEG under the gate. Although this process strongly attracts the attention of researchers and industry [32].

1.4.2 Challenges of GaN HEMTs devices

Having horizontal conduction generates two major drawbacks in the (MOS) HEMTs. First, the current flows through the 2DEG: a very narrow electron sink near the surface. This conductive channel has a thickness of about fifty nanometers [40]. As a result, very non-uniform heat generation and dissipation there, causing degradation of transport properties and activation of deep trap levels already present in the structure, all resulting in a degradation in device performance. Therefore, vertical conduction must be required to allow current to pass through the bulk semiconductor to dissipate the heat more uniformly. The second challenge of the (MOS) HEMTs because the conducting channel is very close to the surface. A strong electric field is generated in the drain side gate by applying high drain voltages, which causes electrical stress. Having traps and dangling bonds on the surface of AlGaN, electrons from the gate can jump from a surface state to the other (electron hopping) to generate a leakage current between the surface gate and drain. It will also cause a collapse of the drain-source current and premature breakdown. Thus, vertical conduction is required to distribute and confine the electric field in the material by volume. Moreover, having a high breakdown voltage requires increasing the device dimensions (and cost).

1.5 Vertical GaN Power Devices:

Vertical devices can play a significant role in overcoming the challenges in lateral GaN HEMTs devices. It can be considered an alternative solution for device operation beneath the theoretical limits of GaN, even if their device operation principle does not rely on 2DEG conductivity. Similarly, the operation voltage drops across a well-designed epitaxial layer at an off state for many Si-based power devices. At one stage, the current directly flows through the device from the top (source contact) to the bottom (drain electrode). After that, the current flow is controlled by a gate electrode on the wafer top. The free-standing GaN substrates are a prerequisite for the efficient realization of vertical device concepts due to the capability to have a low ohmic contact resistance. As the technology of these substrates has matured in the last few years, true GaN vertical transistors are becoming feasible now[9].

Vertical GaN-based devices are better than lateral devices, especially if the high voltage and low on-resistance are targeted. First, the whole chip can operate in high voltage potential separation; thus, destructive

surface arcing is avoided. Second, vertical device dimensions (and cost) are slightly independent of breakdown voltage so that the device can have high breakdown voltage in a small chip area. Third, vertical GaN structure has a uniform heat generation and dissipation; thus, a significant reduction in dynamic on-state resistance and current collapse could be achieved with current extraction greater than 100A. Fourth, the rare flexibility for normally-off device technology using vertical structure without the P-GaN is another advantage with ultra-low leakage current. Finally, but not the end, the drift region's good design might lead to the optimum critical field [33].

Several approaches for vertical GaN-based transistors have been reported, for example, current aperture vertical electron transistors (CAVETs)[34], vertical heterojunction field-effect transistors (VHFETs)[9], and gate trench MOSFETs[35] approaches during the past few years. However, in most of the vertical GaN field-effect transistor (FET) concepts, the breakdown voltage is mainly determined by the thickness of the n−-drift region and the quality of the material. Therefore, it is obvious that significant performance improvement will only be possible if the breakdown voltage versus on-state resistance trade-off can be handled. For this thesis, we are investigating the vertical GaN FinFET device.

1.5.1 Challenges of vertical GaN devices:

The literature review revealed different configurations of vertical transistors based on GaN (VHFET, FinFET, and CAVET) as reported in[9],[10], and [36], respectively. The summary table and figures of merit were beneficial to identify the superior structure concerning device performance. Thus, the Normally-Off vertical GaN FinFET and CAVET are the shortlisted structures for the best reliability. It is also worth mentioning that it was possible to highlight the various challenges, proposals, advantages, and disadvantages through both structures' State of the art [34].

Generally, it can be concluded from the CAVETs fabrication history that it is still not yet optimized even if they are improving over the years. Indeed, according to studies, the major challenge for CAVETs is utilizing the P-GaN layer, which is, up to this moment, not fully optimized for GaN-based power devices. Explicit, although magnesium (Mg) is the only shallow acceptor for GaN, two major reasons account for the difficulty of achieving high free hole concentrations. First, it is difficult to achieve a high free hole concentration owing to two major

limitations. The second drawback is the high Mg doping required to reduce the ionization energy. The free hole concentration will be significantly reduced due to the Mg segregation in the polarity inversion domains (PIDs)[37-38]. Therefore, developing a fabrication process to eliminate the diffusion of magnesium from the p-GaN layer to the AlGaN / GaN. Second, it was noted that the fabrication of CAVETs on the GaN substrate offers more impressive performance due to a reduction of dislocations and defects compared to fabrication on other substrates (SiC, sapphire, Si). However, it remains to improve growth methods to minimize the density of defects in the materials. Third, even after several studies and improvements, the leakage current problem in transistors has not been resolved. Finally, adding a p+ GaN layer under the gate to have a positive threshold voltage has been proposed, but still little studied[39].

According to state of the art, development of high-performance Normally-Off vertical GaN FinFET attracts the attention of the researchers; these appear to be the most promising devices to date in terms of fabrication process since they are composed exclusively of a thick GaN layer doped N-type made without having a p-GaN which can overcome some major challenges observed in CAVETs [40]. For these reasons, the development of the structure Normally-Off Vertical GaN FinFET has been considered to optimize the structural design and fabrication process.

1.5.1.1 The structural Challenges:

The structural challenges are related to the lack of optimum design for Vertical GaN FinFET. Some of these challenges refer to the physical parameters in a different device region, such as the extrinsic GaN doping concentration and the quality of the oxide layer deposited under the gate. Others are related to the structural parameters such as the channel width and the Gate channel interface shape. The optimizing of those and other parameters will lead to better performance devices.

1.5.1.2 Break down mechanisms.

The physics behind breakdown mechanisms in different regions is still inapprehensible and much lower than the theoretical limits in Vertical GaN FinFET devices. This is mainly related to the electric field concentration in some parts of the device, such as the Fin corners under the gate. Different structural and processing parameters have a hand in device early breakdown phenomena. The detailed study for the impact of those parameters on device breakdown is an urgent issue for device reliability optimization[41].

1.5.1.3 The lack of gate controllability:

In vertical GaN FinFET, the current is controlled through fin-shaped n-GaN channels surrounded by gate dielectrics and metal electrodes. At zero bias, the electrons in the Fin channels are depleted due to the GaN surface depletion region. By shrinking the fin width below 500 nm, the more the V_{TH} tends towards the positive values achieved. This behavior is explained by merging the natural depletion region generated by two gate sides [40]. However, decreasing the Fin channel width will increase the on-state resistance leading to lower conduction current and breakdown related to the high electric field in the channel, as depicted in Figure 8

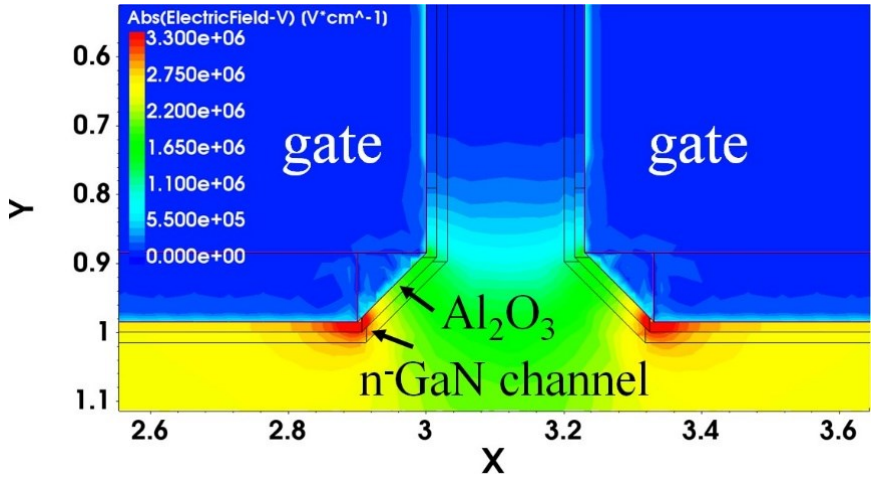

Figure 8: Cross-section of a simulated MOSVFET showing the electrical field distribution (VGS=0V, VBR=697V).

1.5.1.4 Device saturation problem:

The breakdown voltage in vertical GaN devices can be increased by increasing the thickness of the drift region. The lower doping concentration in the drift region will also scavenge better breakdown voltage. The R_{ON} will degrade by increasing the required V_{GD} to pinch the channel toward fast device saturation. Explicitly, the transition between the linear region and saturation region in $I_{DS}(V_{DS})$ is more gradual when the doping of the drift region is reduced. This is due to the voltage drop along the drift region. Indeed, to pinch off the bottom part of the channel between the two side-by-side gates in front of the drain, a higher drain voltage must be applied. Thus, the drain current will saturate at higher V_{DS} for lower drift region doping. The extra voltage applied to the drain current saturation vs. V_{DS} is called “voltage waste.” Thus, the optimum design of the drift region in Fin FET to decrease the voltage waste is a must[24][42].

1.5.1.5 Material and GaN epitaxial challenges:

A complete understanding of current leakage mechanisms and their correlation dislocation/defect densities are also incomplete or nonexistent in GaN FinFET. Some open questions remain on selecting carrier concentration for different parts in vertical GaN transistors to improve the forward device characteristics. Moreover, the optimum channel design shall have a normally-off structure with high carrier mobility and without epitaxial re-growth in bulk Fin channel [43].

Accordingly, the marketing of vertical GaN power devices has been frustrated by the high cost of bulk GaN substrates. The mainstream GaN substrates are 2-inch, while 4- and 6-inch GaN substrates are recently available. The wafer cost (per area) for 2-inch GaN-on-GaN is \$60–\$100/cm^2, still much higher than the cost for 4-inch SiC (~\$8/cm^2) and 8-inch GaN-on-Si (~\$1/ cm^2). The fundamental challenge here is how to obtain high-quality material associated with free-standing GaN substrates while allowing the devices to be transferred to alternate substrates and have the GaN substrates re-used to reduce cost. The Photoelectrochemical (PEC) etching can be used to remove a few epitaxial layers from bulk or free-standing GaN substrates without damaging the substrate. It can effectively serve to make GaN epitaxial substrates reusable[44].

Likewise, the fabrication process of FinFET also has several challenges and concerns that should be brought under control, such as the GaN Fin channel formation, the rounding of channel corners, the smoothing of channel sides, the GaN/dielectric interface, etc. These fabrication steps shall be optimized to obtain an operational FinFET with characteristics close to simulation results. So, the research questions could be formed as follows:

How is the design and fabrication process of normally-off GaN-based vertical Fin FET being optimized toward high electrical performance without using P-type GaN?

1.6 Main Objectives and methodology

The main objective of this thesis is the design and realization of Normally-Off vertical GaN power FinFET on the bulk substrate without the utilization of the p-GaN layer. The minor related objectives could be summarized as follows:

A. Design and optimization of vertical GaN power FinFET device structure (dimensions, doping, and topology) to meet the following performance specifications:

- Realization normally-off device with a positive threshold voltage larger than 0.6V.
- High breakdown voltage enhanced to be greater than 1500 V.
- Improving the device on-state specific resistance R_{ON} with a value less than 1mΩ·cm^2.
- Decrease the leakage current value by having I_{ON}/I_{OFF} Higher than 10^5.

B. To identify the fabrication process modules to realize the optimized device.

C. Optimizing the critical modules toward high quality and effective cost fabrication process.

To achieve such objectives, the device structure shall firstly be built on *sentaurus* TCAD. The appropriate meshing and physical models are then calibrated based on the reported structure in the literature. Consequently, different simulation scenarios are being applied to optimize the device structure. The first fabrication process proposition is then identified, several optimization tests are then applied to optimize and test the proposed process. The final fabrication process is underlined using the "source first" approach.

1.7 Thesis Outline

This thesis consists of seven chapters; the first chapter introduces the necessary information about GaN technology and its challenges. The second chapter illustrates the state of the art in detail to link the current contribution to what has already been done in the Literature. The third chapter underlines the design and optimization procedures for vertical GaN power FinFET devices using *sentaurus* TCAD software. Many semiconductor companies rely on TCAD to explore process variations and design choices to maximize productivity and performance metrics through intensive and accurate modeling instead of lengthy and abstract tests. Thus, it is a highly efficient and inexpensive method to set parameter standards and development targets. In addition, simulations that provide an in-depth look at the internal physics of modeled devices under varying constraints are highly useful in recognizing factors that might exacerbate device weaknesses. Subsequently, chapter four introduces the proposed fabrication process modules toward developing vertical GaN Power FinFET. The testing modules will be detailed, followed by the final fabrication process steps. The optimization and validation procedures of the fabrication modules will be discussed in detail in Chapter five. The article titled "Characterization of m-GaN and a-GaN Crystallographic Planes

after Being Chemically Etched in TMAH Solution" will be discussed in detail in Chapter six. Finally, Chapter seven concludes the thesis contribution and the potential extension of this work.

CHAPTER TWO: STATE -OF- THE ART OF VERTICAL GAN-BASED TECHNOLOGY

2.1 Introduction

New vertical architectures have been proposed in the Literature to avoid the drawbacks of (MOS) HEMTs. This literature review summarizes the three types of vertical transistors based on GaN's most common Literature, either VHFET, MOSFET, or CAVET. Of these, some variations occur, such as MOSFET reversing or Normally-Off and the like with or without CAVETs inclined channel.

2.2 Vertical Heterojunction Field-Effect Transistor (VHFET)

The VHFET transistor (Vertical Heterojunction Field-Effect Transistor), whose structure is shown in Figure 9 [9], enjoys the mobility of electrons in the 2DEG due to the presence of a heterojunction AlGaN / GaN. The layer of p-GaN makes it possible to deplete the electron channel at the junction AlGaN / p-GaN to block the current when the gate voltage is less than the device's threshold voltage. In addition, the presence of the PN junction between p-GaN and n-GaN of the drift region is reverse biased by the drain to prevent the electrons from passing through the layer p-GaN. As a result, the channel opens at the AlGaN / GaN interface by applying sufficiently high gate voltages to allow current flow from the source to the drain.

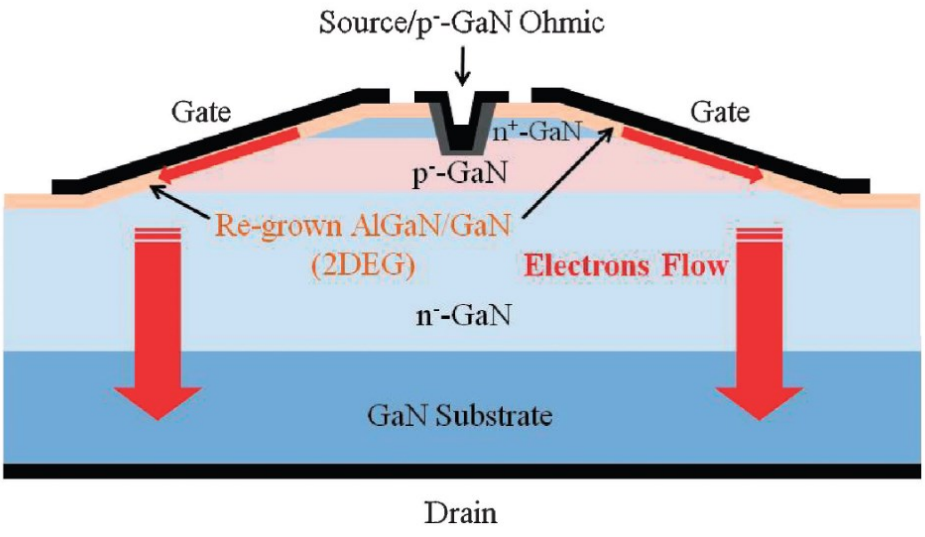

Figure 9:Structure a vertical transistor and a heterojunction field-effect transistor (VHFET)[9]

The main advantage of this type of vertical transistor is that it can withstand high voltages in blocked mode by the PN junction between p-GaN and the n-GaN reverse-biased drift region. In 2010, the Team of Okada et al. [9]Obtained a threshold voltage of -1.1 V, a specific mode resistance of 7.6 $m\Omega \cdot cm^2$, and the breakdown voltage of 672 V. Regarding the fabrication of the transistor, the slope of 16 degrees gates has been etched by ICP-RIE (inductively coupled plasma reactive ion etching), followed by regrowth of GaN and AlGaN for an MOVPE 2DEG. Finally, by varying the thickness of the AlGaN of 35 nm to 10 nm, the charge density in the 2DEG is decreased, achieving an enhancement transistor with a threshold voltage of 0.3V.

2.3 Transistor Vertical MOS field-effect transistor (MOSFET)

2.3.1 Inversion GaN MOSFET (GaN Trench MOSFET)

The starting structure for vertical MOS field-effect transistor (MOSFET) inversion is implemented by the association of VHFET n-GaN / p-GaN / n-GaN. However, as shown in Figure 10(a), the absence of a heterojunction AlGaN / GaN indicates that the electron channel is not formed by a 2DEG but using the MOS capacitor (metal/oxide/ semiconductor). Indeed, the application of a gate voltage is used to attract or repel electrons to generate or close the channel to the p-GaN / SiO_2 interface. Therefore, creating an electron channel in this interface represents the capacity MOS inversion regime.

In 2015, team T. Oka et al. [10]Fabricated a MOSFET inversion having a voltage threshold of 3.5 V, a 1.2 kV breakdown voltage, and specific resistance in passing fashion 1.8 $m\Omega \cdot cm^2$. Since the current must pass vertically in the n-GaN drift region, a small resistance of this layer has been reached by reducing its thickness and increasing its doping. Also, the hexagonal shape of the transistors illustrated in Figure 10 (b) increases the depth of the gate per unit area and thus reduces the specific resistance in passing mode. Finally, an extension of the gate (field plate) was set up to decrease the PN junction's potential. In the future, the team would like to reduce the area occupied by the transistor to be closer to the surface occupied by the SiC power transistors and, thereby, lower the resistivity-passing mode.

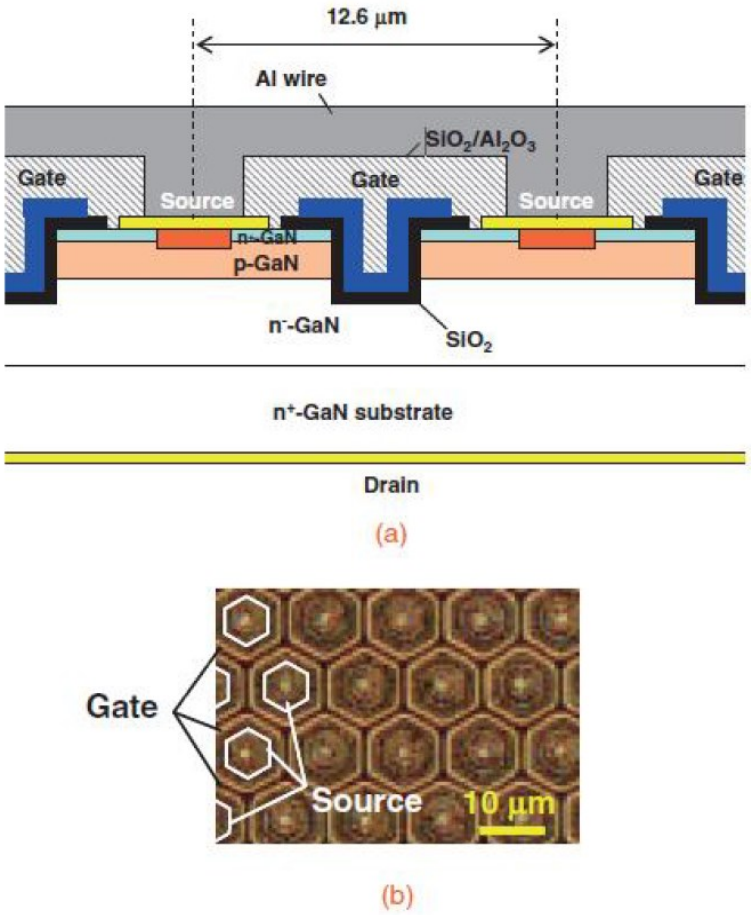

Figure 10: Structure of vertical GaN field-effect transistor MOSVFET[10].

2.3.2 Accumulation MOSFET (or Fin power FET)

The main disadvantage of the MOSFET inverted structure is the presence of the p-GaN layer. Indeed, the activation of magnesium atoms to the p-type GaN doping is relatively difficult and considerably increases the complexity of the fabrication process[45]. The significant mobility degradation due to dislocation is also another challenge for FinFET. Obviously, the trapped electrons due to epi defects will be de trapped by the electric field for higher electric field values, causing mobility degradation through Coulomb scattering. The high activated charge density will dominate the scattering mechanisms resulting in a drastic reduction in the device's performance.

Different architectures were simulated and published by the W. Li et al. team in 2016[46] to overcome those challenges. It is also called MOSFET (vertical MOS-gate transistor accumulation or End Power FET) made of GaN doped n. As shown in Figure 11(a), this simulated structure is to have a low gate-to-gate distance L_{gtg} to

take advantage of the depletion layer created by the gate when it is negatively biased to block current. The simulation was conducted using the TCAD Silvaco software is using the drift-diffusion transport 2D model (drift-diffusion). With 0.8 µm between two gates and depth of 2.0µ Gate, simulations have resulted in a threshold voltage of 0.25V, a 1.2 kV breakdown voltage, and specific resistance mode from $m\Omega \cdot cm^2$ [12]. The simulated design is described in Figure 11(b)

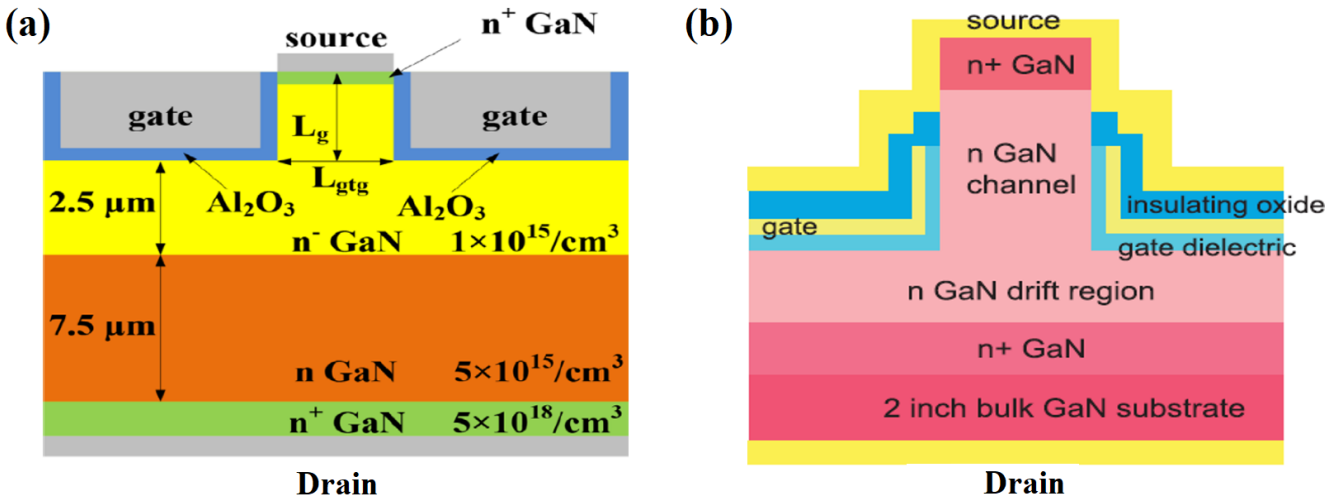

Figure 11: Schematic of MOSVFET device (a) simulated structure of a Normally Off MOSVFET [46]. (b) Structure of fabricated MOSVFET to accumulation (FinFET)[47].

The study analyzed the impact of the gate-to-gate length L_{gtg} on the threshold voltage and leakage current. The depletion zones on either side of the gates pinch the channel by decreasing that dimension simulation, thereby increasing the threshold voltage. As for the etching depth for the gates, the latter controls the power off mode. Ideally, a etching depth for more than 2 µm gates to reduce this leakage current.

In 2017, the Team of Mr. Sun et al.[12] Fabricating the MOSFET to build the structure as shown in Figure 11(a). Not containing p-GaN layers, this type of transistor fabrication has low costs epitaxy while providing excellent performance. The team fabricated transistors with a breakdown voltage of 800 V, a resistance mode from 0.36 $m\Omega \cdot cm^2$, and a threshold voltage of 1V. In addition, a gate-to-gate length (L_{gtg}) of 180 nm was defined by using electron beam lithography.

In 2019, another GaN FinFET structure was reported by Riyaz Abdul Khader. In such design, a fully vertical power MOSFET on 6.6-µm-thick GaN grown on a 6-inch Si substrate by metalorganic chemical vapor deposition (MOCVD). The specific on-resistance (R_{ON}) of 5 mΩ.cm^2 and the breakdown voltage (V_{BR}) of 520 V. Consequently, Huang et al. have reported a new structure for vertical FET; according to their paper, a trenched-gate scheme is employed to realize the normally-off VFET. Meanwhile, an additional back current blocking layer (BCBL) is proposed and inserted into the GaN normally off VFET to improve the device performance. However, the idea to deposit a BCBL is not realized until today and technically can't be fabricated due to the structure of GaN epitaxy growth. The simulation results for the reported structure exhibit a threshold voltage of 3.5 V and a breakdown voltage around 1800 V[47].

2.4 Current Aperture Vertical Electron Transistor (CAVET)

2.4.1 Non-trench Gate CAVET:

As shown in Figure 12, the GaN-based CAVET (Vertical Aperture Current Electron Transistor) is a vertical transistor with a structure like a HEMT except that the drain is found in the backside of the device. Indeed, this structure also has a gas 2DEG interface AlGaN / GaN, allowing the highly mobile electrons to pass. However, by placing the drain under the device, the 2DEG acts as a source. Through this, the current controlled by the gate can be run vertically in the solid material through a small trench to distribute and confine the electric field in the GaN by volume to increase the device's breakdown field. The CBLs (current blocking layer) acts as an insulating layer consisting of p-GaN to ensure that the electrons do not cross the device without going through the control gate. The first CAVET device was implemented by S. Chowdhury *et al.* in 2008 [43].

Meanwhile, to ensure the current flow in CAVET, it is necessary to have a greater conductivity in the 2DEG. Thus, the parameters playing a critical role are the length of the gate, the doping concentration in the channel, and the thickness of GaN UID. Furthermore, R_{ON} must optimize the channel structure to have a low specific resistance [11]. In 2015, team Nie et al. fabricated a CAVET with a voltage threshold of 0.5 V, a 1.5 kV breakdown voltage, and a specific resistance of 2.2 mΩ·cm^2. The positive threshold voltage was obtained with the p-GaN layer under the gate [48].

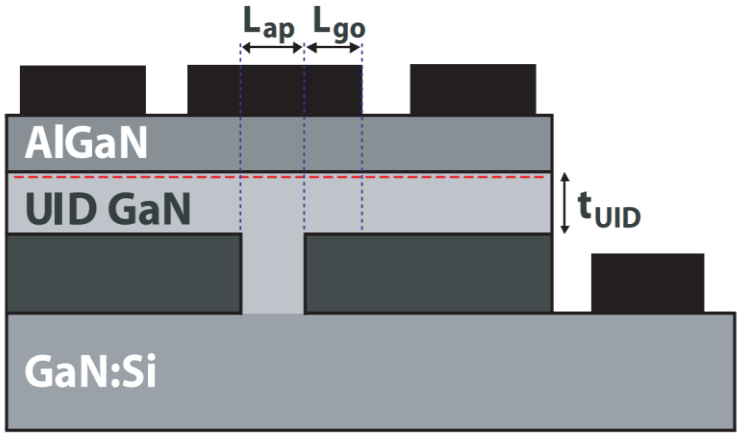

Figure 12:Structure an AlGaN / GaN CAVET[36].

Another type of CAVET transistor has been proposed in the Literature whose particularity is the inclination of the channel[53]. As shown in Figure 13(a), triple layers p-GaN / AlGaN / GaN were grown epitaxially shaped angle V. This configuration uses a semi-polarized face to reduce the carrier concentration in the channel AlGaN / GaN interface to obtain enhancement transistor, as shown in Figure 13(b).

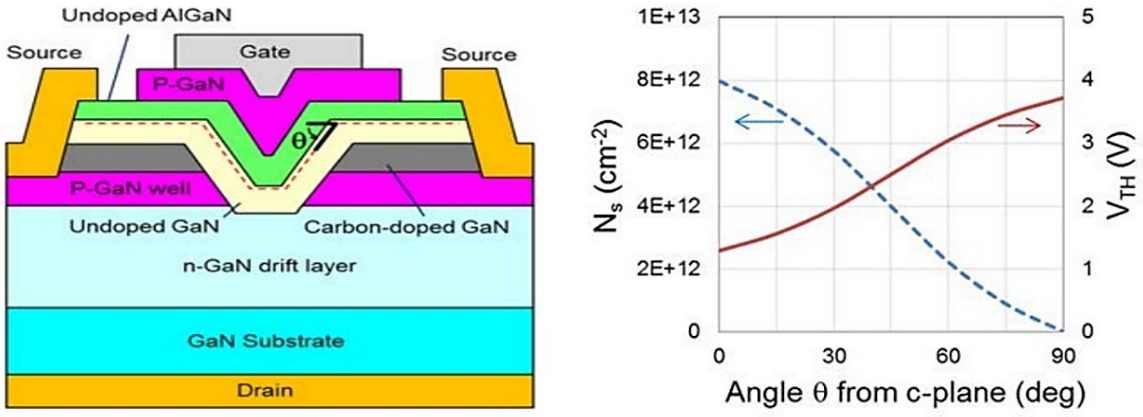

Figure 13:Trench CAVET. (a)Structure of an AlGaN / GaN CAVET inclined channel [11]. (b) carrier density ns and tension threshold Vth calculated in the channel p-GaN / AlGaN / GaN depending on the angle of inclination θ concerning the c-plane (0001)

As the angle is pronounced, carriers require less bias to form the channel. Another aspect added to the structure is a semi-insulating GaN layer doped carbon above the insulating layers of p-GaN (CBLS). This role is to prevent the passage of leakage current through the CBLS p-doped GaN magnesium. It should be noted that the junction GaN: C / p-GaN is called a hybrid insulating layer (HBLS).

2.5 Comparison of different vertical architectures

This literature review has revealed the different types of transistors verticals GaN-based most frequently in the Literature, either VHFET, MOSFET, or CAVET[9], [24], and [45], respectively. For such structures, some variants were analyzed, including MOSFET, its inversion and accumulation, or as CAVETs with and without slanting channel. Table 2 summarizes the results of each of the architectures in terms of breakdown voltage, specific on-state resistance R_{ON}, and threshold voltage. The figure of merit FOM for different research teams using power devices V^2 / R_{ON} FOM are represented in Table 2. It is possible to notice that CAVETs and Power FETs obtained the most impressive performance to date because of their higher FOM. However, it should be noted that this figure of merit does not judge the performance and quality of the technology itself. Indeed, this stage of research is not yet optimized. Therefore, weaker results in the Literature do not mean that technology is not promising. For visualization purposes, Figure 14 illustrates the on-state resistance depending on the breakdown voltage, which summarizes the performance of the state-of-the-art different architectures vertical transistors based on GaN.

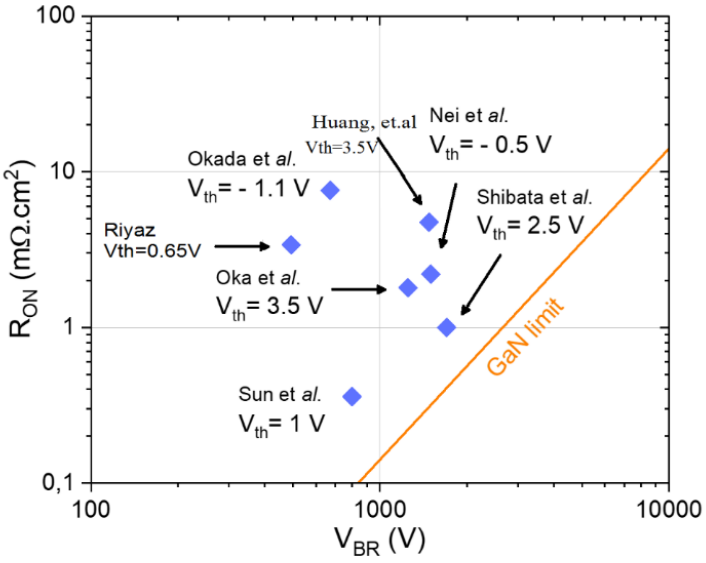

Figure 14: Resistance in the conducting state RON depending on the voltage Vbr breakdown different architectures of vertical transistors

It is noticeable that the inclined CAVET Shibata et al.[50] and the MOSFET Sun et al.[12] have the closest characteristics to the theoretical limit of GaN while having positive threshold voltages.

Table 2: Comparison of different types of vertical transistors GaN-based in terms of breakdown voltage V_{BR}, specific resistance R_{ON} and threshold voltage V_{TH}

Year	Group of research	Type	Title	Results			
				V_{BR} [V]	R_{ON} [mΩ · cm^2]	V_{TH} [V]	FOM [V ^{2}Ω-1cm^{-2}]
2010	M.Okada / Sumitomo Electric	VHFET	Novel Vertical Heterojunction Field Effect Transistors with-Re-grown AlGaN / GaN Two- Dimensional Electron Gas Channels are GaN Substrates [9]	672	7.6	-1.1	6
2015	Oka / Toyoda Gosei Co.	MOSVFET to inversion (Trench MOSFET)	1.8 mΩ · cm^2 GaN-based vertical trench metal-oxide-semiconductor field-effect transistors were free-standing GaN substrate for 1.2-kV-class operation [10].	1250	1.8	3.5	87
2017	Mr. Sun / IEEE	MOSVFET to accumulation (Power Fin FET)	High Performance GaN Vertical Fin Power Transistors on Bulk GaN Substrates [12]	800	0.36	1	178
2014	Nei / Ivory	CAVET	1.5 kV and 2.2 mΩ·cm^2 vertical GaN transistors are bulk GaN substrates[48]	1500	2.2	0.5	102
2016	Shibata / Sumitomo Electric	CAVET trench	1.7 kV / 1.0 mΩ.cm^2 normally- off vertical GaN transistor is regrown GaN substrate with p-GaN / AlGaN / GaN semi-polar gate structure [50]	1700	1	2.5	289
2019	Riyaz Abdul Khadar/ WBG Electronic	Trench MOSVFET	Fully Vertical GaN-on-Si power MOSFETs[47]	520	5	0.65	123
2019	Huang, Huolin.et.al	FinFET	Gallium Nitride Normally-Off Vertical Field-Effect Transistor Featuring an Additional Back Current Blocking Layer Structure[45]	1800	3.14	3.5	56.7

2.6 History and progress in the fabrication of the most promising transistors

Among the various vertical transistors discussed in the literature review, two structures, either CAVETs or MOSFETs, are outstanding performance in breakdown voltage, specific on-state resistance (R_{ON}) resistance, and threshold voltage (V_{TH}). Therefore, it is preferable to go through state of the art and the progress made over the years to achieve such performance to explore the advantages and challenges of each structure.

2.6.1 CAVET

The first AlGaN / GaN CAVET on the sapphire substrate was reported between 2000-2004 by Ben-Yaakov et al., and it was then made and characterized[49]. The research team studied in detail three types of losses in the device. As shown in Figure 15, the first type of leakage current occurs when the electrons from the source pass directly through the insulating layers CBLS (current blocking layers) GaN: Mg to reach the drain. The second occurs when electrons from the source move in the 2DEG, so the gate can't control that. Finally, the third type of leakage occurs when electrons move from the gate to the drain. To remedy these problems, the team proposes a specific fabrication process in the growth of materials to reduce losses through CBLS significantly. They have proposed a non-intentionally ultra-thin doped GaN layer (UID-GaN) to minimize losses in the 2DEG and add an insulator under the gate. As another part of their studies[51], Three different CBL insulating layers (p-GaN) were studied; GaN: Fe, GaN: Mg, and GaN implanted aluminum ions. The results show that the parasitic leakage current for GaN device implanted ions is significantly smaller than that of GaN: Fe and GaN: Mg. It could be explained by the fact that the iron or magnesium is incorporated in the layers during the regrowth, which increases the channel resistance and decreases the current in the device. As for the ion implantation method, it allows defining the insulation regions. However, in this study, the leakage could not be eliminated and is found mainly in the gate, generating relatively low breakdown voltages [51].

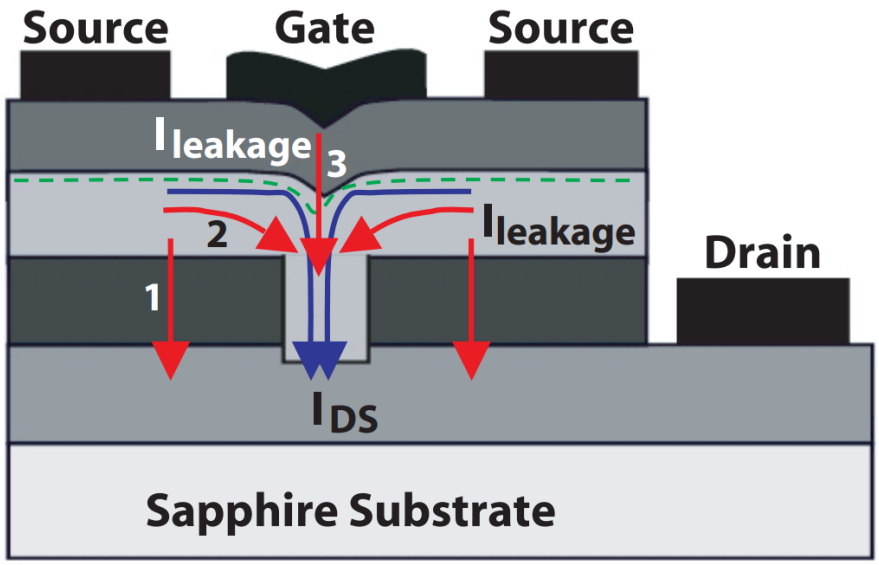

Figure 15:Schematic leakage current resources in CAVET represented by arrows pale gray color [14].

In 2008, the fabrication process was reviewed by Chowdhury et al. [11]. For fabrication, the first CAVET enhancement-mode (E-mode) by CF4 plasma has a threshold voltage of 0.6 V. As those of Ben-Yaakov et al.[49], The transistors of Chowdhury et al. were fabricated on sapphire substrate, and the insulating layers of CBLS were carried out by ion implantation of magnesium. In addition, layers of AlGaN / GaN were deposited by the MOCVD method (metalorganic chemical vapor deposition). The special feature of this study lies in the exposure of certain samples to a CF4 plasma. The results show that this exhibition will slightly vary the threshold voltage of the transistors to positive values. However, in 2012, team Chowdhury et al.[11] Reported that their previous 2008 study[51] Exposed to CF4 plasma was unreliable. They explain this by the uncontrollable variation in threshold voltage due to the diffusion of magnesium CBLS in layers of AlGaN / GaN during growth by MOCVD. Therefore, another study was carried out to solve this issue by growing AlGaN / GaN Plasma-MBE (molecular beam epitaxy) layers to the GaN substrate to have a low growth temperature. The results show that by performing the growth of AlGaN / GaN MBE low-temperature layers, diffusion of magnesium ions has been avoided. This improvement makes fabrication a more easily reproducible device, which is advantageous for future high-power applications.

Furthermore, an insulating layer of 30 nm of SiN was deposited by MOCVD directly under the gate (between the gate and the AlGaN) to minimize the gate leakage. Finally, to have low resistance in the aperture between CBLS, constant doping in the trench $2\times10^{16}cm^{-3}$ was selected to assess the impact of the length of the trench on the specific RON. They vary this distance from 1 to 15 µm. The results show that over the trench length increases, the specific resistance decreases until saturation. By characterizing devices, a breakdown voltage of around 250 V and a specific resistance R_{ON} of 2.2 $m\Omega\cdot cm^2$ were observed on a device with a GaN drift thickness (Drift Region) of 3µ m.

In 2014, Team Nie et al.[48] CAVETs Tennant gains greater capabilities in the perfecting of fabrication techniques. The growth of GaN was made by homoepitaxy of GaN substrate, allowing low defect densities in the material, and CBLS were carried out by in-situ growth of p-GaN doped with magnesium. A p-GaN layer was also filed under the gate, whose thickness and doping was selected to have a positive threshold voltage. The results show a threshold voltage of 0.5 V, a 1.5 kV breakdown voltage, and a specific resistance of 2.2 $m\Omega\cdot cm^2$.

In 2016, Shibata et al.[50] proposed a new design, CAVET, on GaN substrate whose upper part of the p-GaN structure / AlGaN / GaN has a V-shape under the gate. The advantage of this form is that depending on the angle of the V shape. The band diagram has been modified by shifting up the 2DEG channel above the conduction band. Therefore, the transistor is being normally-off as no polarization has been applied. In conclusion, a positive threshold voltage of 2.5V can be achieved. Finally, the specific resistance of 1 $m\Omega \cdot cm^2$ and a breakdown voltage of 1.7 kV was measured.

2.6.2 Normally Off GaN (FinFET)

Since GaN FinFET are such a recently developed structure, and only a few publications have addressed it [48-44], we have covered the entire history of this device in the state-of-the-art section. The advantage of this architecture over the CAVET is that it does not require any p-GaN layers to develop a normally-off operating device.

CHAPTER THREE: DESIGN AND OPTIMIZATION OF NORMALLY-OFF VERTICAL GAN FINFET USING TCAD TOOL

3.1 Introduction:

Using *Sentaurus* TCAD simulation tools, this chapter explores the origins of breakdown processes in a vertical GaN power FinFET. The 2D drift-diffusion model was used for simulations. Furthermore, we studied the impact of several design approaches to optimize the device architecture and improve the V_{BR} and R_{ON}. Among incorporated parameters are the gate shape, gate oxide thickness, Drift Layer doping concentration and thickness, and n-GaN/n+GaN channel. Indeed, a part of the vertical GaN FinFET design chapter had been investigated by Marie-Clara Pépin, a group GaN team member who was doing her master thesis on "Design of a Vertical MOSVFET Transistor Based Gallium Nitride" [42]. Therefore, the objectives of this chapter could be summarized as follows:

- ✓ Understanding the physics behind the results obtained by Marie-Clara Pépin for the first version of vertical GaN FinFETwith *Sentaurus* TCAD. Regenerating the obtained curves has been done as well.
- ✓ Investigating the unexplained observations obtained in the first version of the device.
- ✓ After ordering the GaN epitaxial wafers, we have recognized that some optimized parts can't be realized based on the discussion with the manufacturer. Indeed, the design of the optimized device shall be updated to be aligned with the GaN epitaxial growth without degrading the device's electric performance. The new design corresponds to the real GaN epitaxial wafers that have been simulated and compared to the first optimized structure.

3.1.1 Introduction to TCAD *Sentaurus* tool:

The simulations were carried out utilizing *Sentaurus* TCAD (version G2018.06), provided by Synopsis. It is a useful computer-aided tool to design semiconductor devices toward reproducing the measured results, predict device performance, and understand the physics behind the device's electrical behavior [53]. This chapter firstly

presents the optimization procedures of vertical GaN FinFET using *Sentaurus* TCAD. Explicitly, the starting structure has been built in *Sentaurus* TCAD software based on the characterized device reported by Sun. *et al.* [12] group. The physical models and parameters implemented in the software have been calibrated to reveal approximately the results published in the reference design. Consequently, the design and material parameters are optimized to improve the device's performance to levels close to the theoretical limits of GaN material.

Generally, the process of meshing represents a continuous region by discretizing it into its constituent nodes. The electrical characteristics are carried out by solving numerical equations in each node one at a time. Figure 16 illustrates the steps involved in creating a simulation. The simulation begins with defining materials, adding doping, adding contacts, and meshing the device. Applying appropriate meshing is the most important step toward achieving better convergence. Afterward, corresponding material parameters (such as carrier mobility and bandgap energy) and physical models (such as carrier transport mechanisms) are assigned to each region. Next, the test conditions (such as the ramping voltage across contacts) are planned, followed by the solution of the transport equations. The final step involves extracting the current-voltage (I-V) results and constructing the device profile.

3.2 The incorporated parameters and models incorporated in the Simulations

Sentaurus Workbench software can extract many basic physical and electrical data to characterize device performance. Among others, it brings out the output characteristics (I_{DS}-V_{DS}) and transfer (I_{DS}- V_{GS}), where I_{DS} is the output current (drain-source), and V_{DS} and V_{GS} are respectively the drain and gate voltages concerning the source. From these curves, it is then possible to determine the specific resistance (R_{ON}) of the transistor, the transconductance (G_M), the threshold voltage (V_{TH}), and the breakdown voltage (V_{BR}). Since there are several physical models and calculation methods, the software is realistic. It can accurately describe most of the physical operations when the transistor is operational. The flow chart of TCAD simulation procedures is shown in Figure 16.

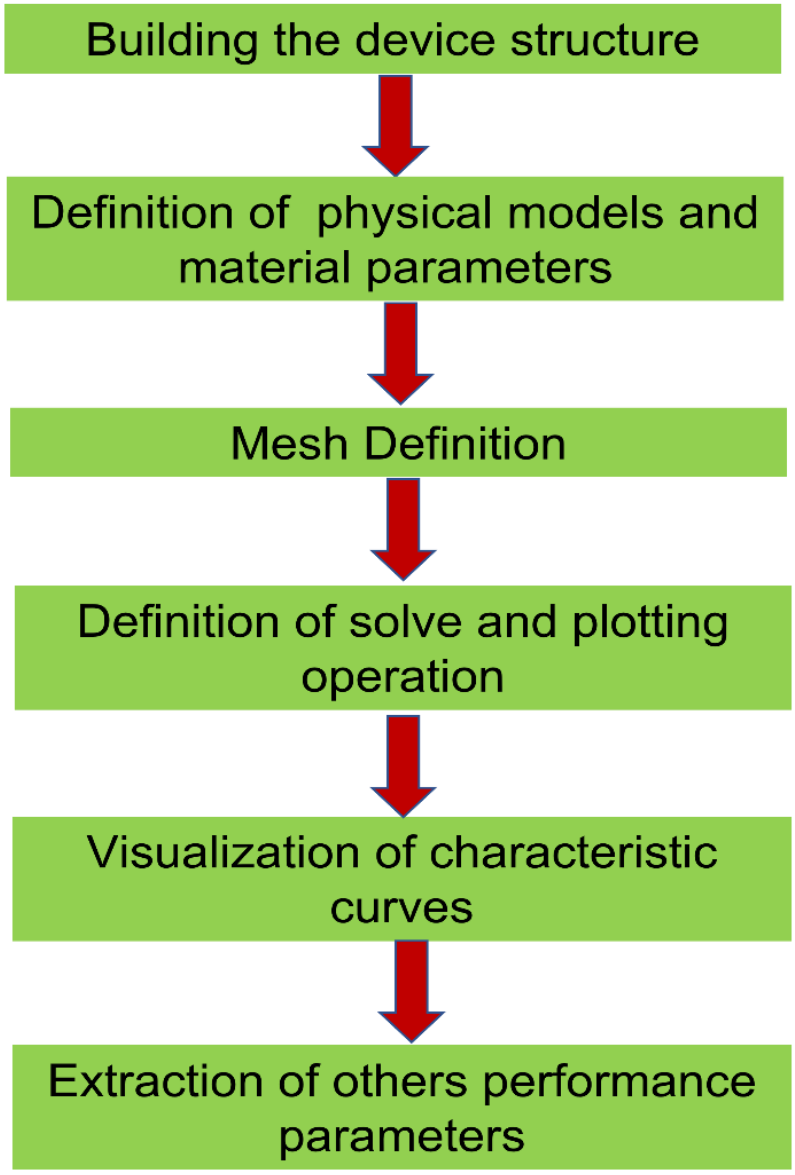

Figure 16: The flow of TCAD simulation procedures.

3.3 Introducing the Vertical GaN FinFET starting structure

The starting structure used to build the vertical GaN FinFET is related to the one reported by Mr. Sun et al. [12], illustrated in Figure 17(a). It was fabricated after it was designed using *Sentaurus* Structure Editor (SDE). Our first objective is to align our simulation results with the article results to validate the software calibration. The diagram of the simulated epi-structure is shown in Figure. The starting structure is built in TCAD with specifications detailed in Figure 17(c).

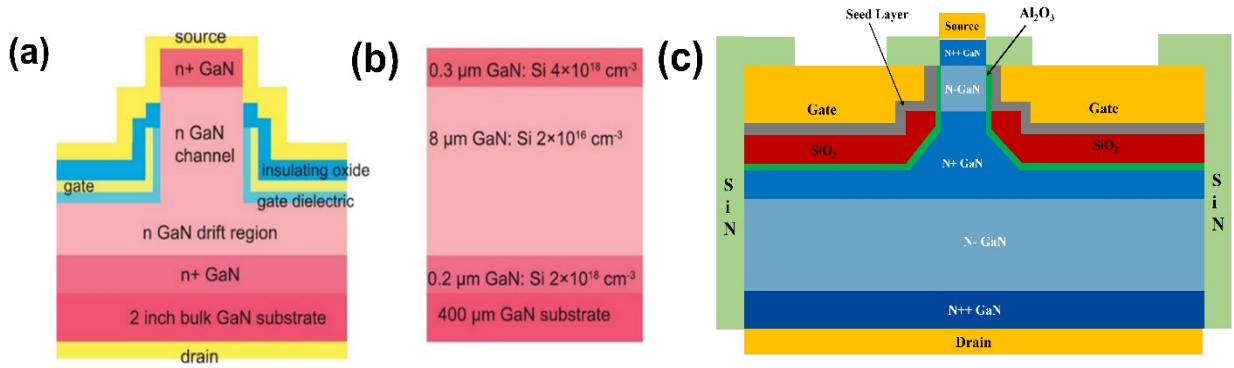

Figure 17: a)Schematic of the calibration structure of vertical GaN FinFET. b). c) schematic of the simulated structure in TCAD Sentaurus.

The role of each of the layers and regions is defined as follows;

-**The n-GaN channel layer** has the function to control the channel, thus the opening and closing of the transistor. The doping of this layer is critical to the threshold voltage Vth. Indeed, in this type of device, the channel's closing is caused by the superposition of the depletion regions created by the surface potential of the MOS structure on either side of the channel. Thus, low doping and a short gate-to-gate distance L_{gtg} are required for obtaining positive threshold voltage.

-**The n-GaN drift layer (Drift Layer)** distributes the electric field in the bulk material. Its thickness and doping lie particularly influence the resistance in the on-state R_{ON}. According to the article by W. Li [46], More than 90% of the total resistance of the device comes from this layer.

-**The layers n^+-GaN** adjacent to the source and drain contacts allow an ohmic contact between the metal and the semiconductor.

-**The layers of SiN** on the sides of devices are present only to delimit the boundary conditions.

Comparing the dimensions and doping of the calibration structure with that simulated in software TCAD Sentaurus is presented in *Table 3*

Table 3: Comparison of dimensions and doping levels of the calibration structure and the first optimized version with Sentaurus TCAD software.

Dimensions and doping	The value used in [12]	The value used in simulation[42]
THE WIDTHS		
Total device-width [µm]	-	**6.23**
Width grids L_g [µm]	-	**3**
Gate width-to-gate L_{gtg} [µm]	0.18	**0.2**
Width of the gate oxide L_{ox} [nm]	15	**15**
THE THICKNESSES		
The thickness of layer n+GaN source side [µm]	0.3	**0.1**
The thickness of the channel layer n-GaN [µm]	8	**0.8**
The thickness of the drift region n-GaN [µm]		**5**
The thickness of the top of drift region nGaN [µm]	-	**0.7**
The thickness of layer n+GaN drain side [µm]	0.2	**0.1**
The total thickness of the device [µm]	8.5	**6.7**
DOPING CONCENTRATION		
Doping of the n-layer+GaN source side [cm^{-3}]	4×10^{18}	$\mathbf{4 \times 10^{18}}$
Doping of the channel layer n-GaN [cm^{-3}]	2×10^{16}	$\mathbf{1.1 \times 10^{16}}$
The thickness of the top of drift region nGaN [cm^{-3}]	-	$\mathbf{5 \times 10^{16}}$
The thickness of the drift region nGaN [µm]	-	$\mathbf{1 \times 10^{16}}$
Doping of the n-layer GaN drain side [cm^{-3}]	$\mathbf{2 \times 10^{18}}$	$\mathbf{4 \times 10^{18}}$

3.3.1 The meshing

Once the structure is generated in Sentaurus Structure Editor by defining the finite element mesh is done using the SNMESH interface. The mesh size corresponds to a set of points the Poisson equation is solved. The different characteristics outputs are calculated (band diagrams, concentrations of the holders, electric field, current, potential, etc.) Viewed that time and calculation precision depend on the number of nodes to calculate the mesh must be chosen wisely. Thus, a compromise must be reached between the computation time and accuracy. As shown in Figure 18, a dense mesh is generated in critical areas (such as the interfaces of different materials and in the conductor channel). In contrast, a looser mesh is selected from materials massive.

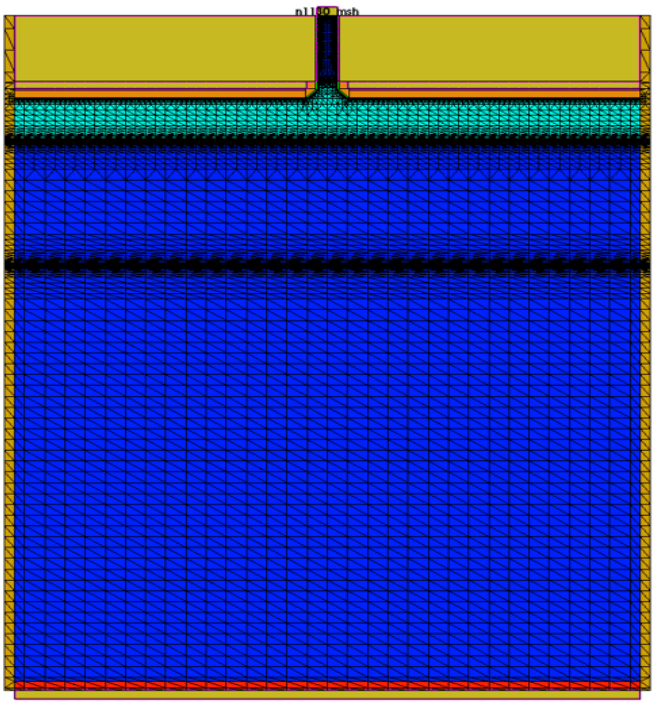

Figure 18: Schematic of the generated mesh using SNMESH

3.3.2 Contacts definition

The next step following the generation of the structure and the mesh is the one concerning the definition of the contacts (source, drain and gate). To do this, a file is created in SDEVICE whose electrodes syntax is as follows:

```
Electrode {
{Name = "gate" Voltage = 0 Schottky Workfunction = 5.1}
{Name = "source" Voltage = 0 DistResist = @ DistResist @}
{Name = "drain" Voltage = 0 DistResist = @ DistResist @}
}
```

3.3.3 Voltage

By specifically defining the electrode bias voltage as zero volt, the voltage command enables users to calculate different characteristics of outputs (band diagrams, concentrations of holders, electric fields, currents, etc.) at zero volt.

3.3.4 Ohmic / Schottky

According to the Sentaurus Device Guide[54], the contact is considered Ohmic by default if the work function is not specified. Otherwise, the contact is considered Schottky; therefore, no work function has been specified for

the source and drain as they must be Ohmic to facilitate the flow of current between them. As for the grid is of the Schottky type, and a work function of 5.1 eV has been specified to it, corresponding to gold metal.

3.3.5 Contact resistance

Even though the sources and drains are considered ohmic, there will always be metal-to-semiconductor resistance when fabricating the devices. For this reason, in the simulation, we applied the DistResist syntax and imposed a distributed resistance with the value @ DistResist @ = 1×10^{-6} Ω.cm^2 (value from the Workbench).

3.4 Extraction of performance parameters

Because the extraction of current characteristics can be done in different ways (depending on the publication or convention), it is important to define the definition employed in this work. The on-state resistance (R_{ON}) is calculated at V_{GS}= 5V and V_{DS} = 0.15V and equal to the inversed slope of the I_{DS}-V_{DS} curve in linear mode.

- The threshold voltage (V_{TH}) represents the gate voltage at which the ratio of the current drain I_{ON} / I_{OFF} =10^5.
- The breakdown voltage (V_{BR}) is calculated at V_{GS} = 0V and is defined by one or the other of these two conditions:

1) Critical Electric Field.

If the electric field reaches the critical value of 3.3MV/cm in GaN or 7MV/cm in oxide, the simulation indicates that breakdown is reached at this drain voltage.

2) Leakage current.

If the I_{DS} current reaches a value greater than 10^{-5} A / cm^2, the simulation indicates the associated drain voltage.

3.4.1 Comparison of simulation results with Literature

The simulated transfer characteristic curves are shown in Figure 19(a) compared to experimental curves of the article by M. Sun et al.[12] shown Figure 19(b). Explicitly, Figure 19 illustrates IDS -IGS's characteristics curves at V_{DS}=5V in logarithmic and linear scales. Note that the pace is very similar on a logarithmic scale between simulation and experimental. The current saturation tends towards currents of the order of 10^4 A/cm^2. The threshold voltage extracted for an I_{ON} / I_{OFF} ratio = 10^5 is 0.67 V for the simulation compared to 1.0 V for the experimental one. On these points, the simulation roughly agrees with the publication. However, we notice that the maximum drain current is not the same on the two graphs of Figure 19. Since the simulation models have been calibrated with experimental

curves, the difference could be related to different explanations (e.g., the real values of channel width, doping, thickness, gate's dielectric thickness are not accurate like the simulated ones. However, this difference is acceptable. since the current saturation occurs at the same voltages below V_{Dsat} are relatively similar, making it possible to validate the simulation code.

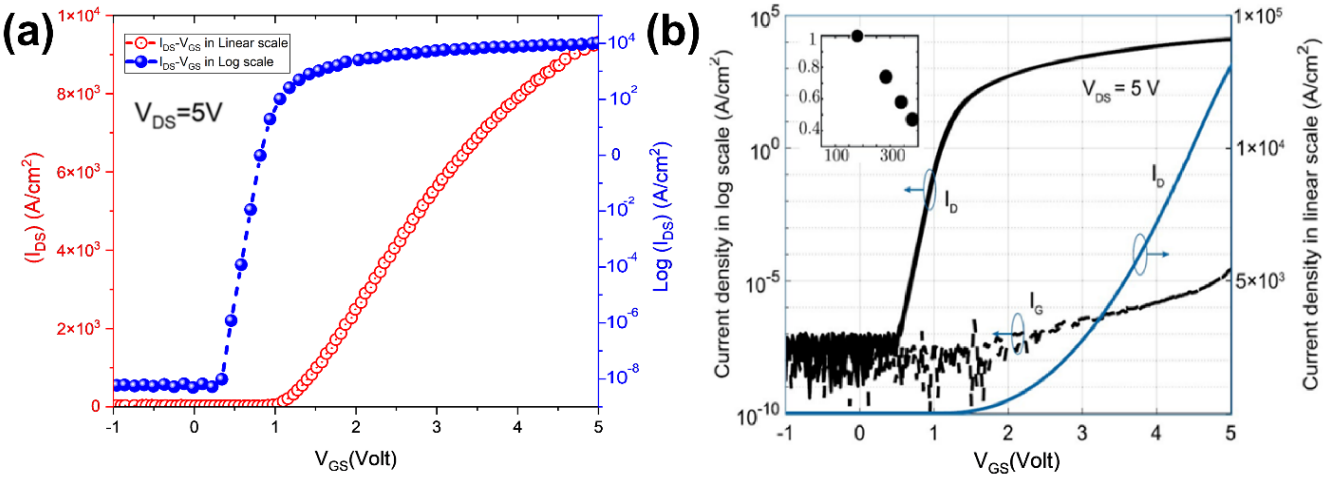

Figure 19: Comparison between the transfer characteristics of simulated vertical GaN FinFETand and reference article, (a)Transfer characteristics of the simulated transistor. Lgtg is 200 nm[42]*, (b) Reference material transfer characteristics[37], Lgtg is 180 nm.*

Up to this moment, the simulation code was calibrated and validated by implementing different physical models and then comparing its results with experimental results. By incorporating the effects of different structural and physical parameters on the device characteristics curves, the remaining sections explain how our starting device structure is optimized, resulting in a high-performance version of the normally-off vertical GaN power FinFET device.

3.5 Summary of the optimization process of vertical GaN power FinFET starting design using TCAD *Sentaurus* tool

Previously in section 3.6, the simulation models have been validated by comparing them to the fabricated structure reported in [12]. Therefore, this section's remaining parts summarize our team's previous investigation to optimize different parameters (dimensions, dopings, and topology) on the overall device's performance[42]. The Schematic of the startup structure of vertical GaN power FinFET is shown in Figure 20.

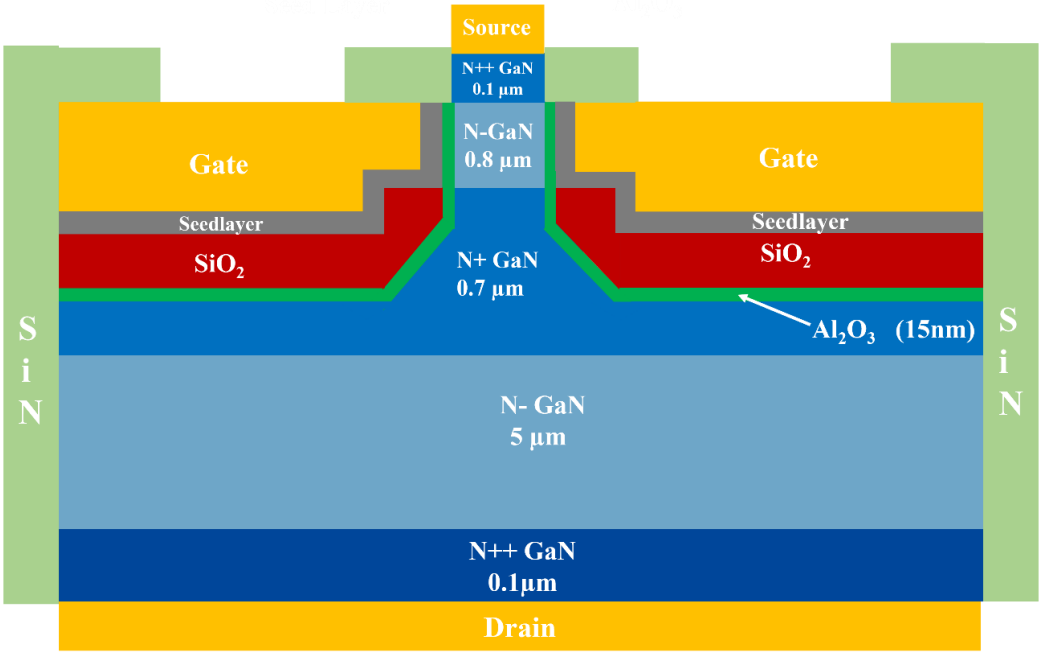

Figure 20: Schematic cross-section of a simulated normally-off GaN Fin Power FET.

Figure 20 illustrates the epitaxial structure of n-type GaN (source to drain). The device consists of channel and drift regions, each doped to $1x10^{16}$ cm^{-3} and $5x10^{16}$ cm^{-3}, respectively. Additionally, it has a dielectric gate layer of Al_2O_3 with15 nm thick. Likewise, a 0.1µm thick $4x10^{18}cm^{-3}$ n+GaN doped layer was used to improve the contact resistance. Accordingly, as part of this thesis, the incorporated parameters in the optimization process can be summarized by region as follows:

The Fin Channel region parameters

–The Gate-to-Gate length L_{gtg};

–The shape of the Gate corners on the drain side (square, triangular and circular corners);

–The addition of a composite oxide SiO_2 / Al_2O_3;

The drift layer region parameters

–Doping and thickness of the drift region.

–Adding an n-channel layer-GaN / n+GaN at the top of the drift layer region.

– n+GaN/N-GaN blocks for the whole drift region.

The remaining part of this chapter will explain the optimization procedure for both regions toward high breakdown V_{BR} voltage and lower on state-specific resistant R_{ON}.

3.5.1 Optimization of GaN Fin channel region parameters

As previously mentioned, three different parameters were incorporated to optimize the channel regions toward having a positive threshold larger than 0.6V, improve the specific R_{ON} state resistance for a value less than $1m\Omega \cdot cm^2$, and obtain a higher Ion/Ioff ratio than 10^5; the Gate-to-Gate length L_{gtg}, the shape of the Gate corners on the drain side (square, triangular and circular corners), and the addition of a composite oxide SiO_2 / Al_2O_3 layer under the gate toward channel corners.

3.5.1.1 Optimization of the Gate-to-Gate length (L_{gtg})

The first parameter studied is the gate-to-gate length L_{gtg} since this distance is critical concerning the threshold voltage and the leakage currents of the device. Figure 21 illustrates the impact of L_{gtg} on the device's threshold voltage and the breakdown voltage.

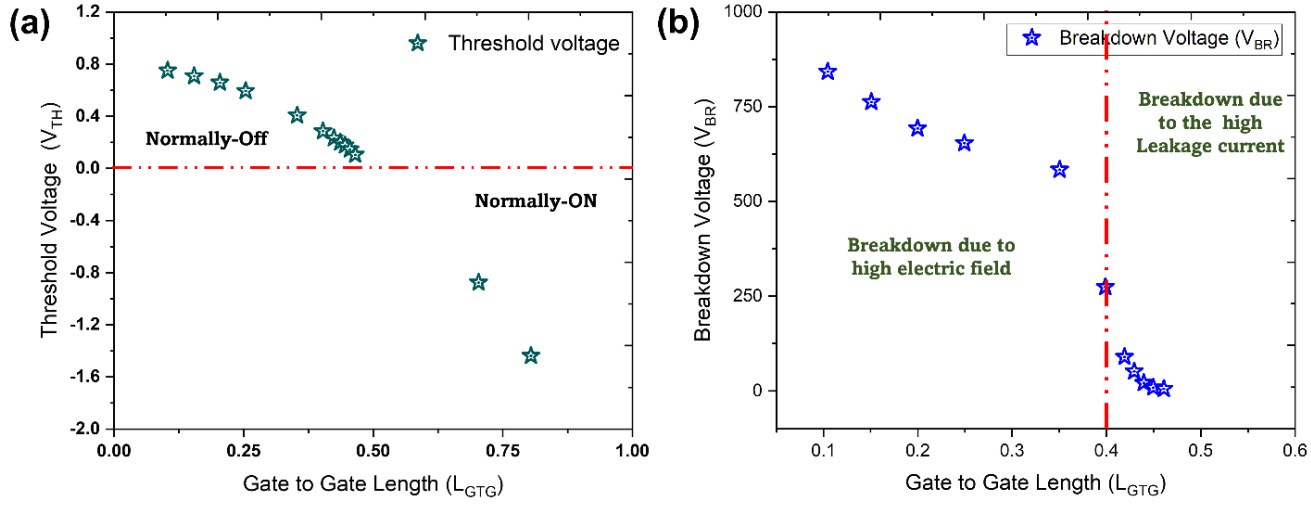

Figure 21: The gate-to-gate length (Lgtg) impacts a) the threshold voltage(Vth) and b) the breakdown voltage (V_{BR}) at V_{GS}=0V.

According to Figure 21(a), the lower the L_{gtg} value, the Vth value is more positive. An explanation for this behavior lies along the channel where the natural depletion region of both sides gates are merged [46]. Generally, if the drain leakage current is equal to $10^{-5}A/cm^2$, or when the critical electric field within the device is reached (3.3 MV/cm in GaN, or 7 MV/cm in Al_2O_3), the V_{BR} value is numerically determined. In Figure 21(b), when L_{gtg} is less than 0.5µm, the breakdown of the device is caused by a high electric field. However, when L_{gtg} is greater than 0.4

µm, the breakdown is caused by very low voltage (V_{th}) due to significant leakage current. The device will be normally ON as the channel width increases [46]. When we apply a negative V_{DS}, the V_{BR} will be improved, accordingly, since the drain potential will be stronger, making it a bit easier to access the gate end area to pinch off the channel. Indeed, the objectives of the thesis include having a normally-off transistor with positive Vth, which can't be achieved by using -ve Vds (Normally-ON).

3.5.1.2 Impact of the gate shapes

It was found that the breakdown of the device happened on the tip of the oxide because the squared corners of the gates concentrated the field. It has been found that the breakdown voltage increases from 687 V to 800 V when the electric field is homogeneously distributed. The gate shape has been optimally rounded to ensure this possibility. However, the rounded shape doesn't correspond to the real devices, as they have slopes like the most common GaN inclined planes (triangle shapes). Accordingly, triangle shapes were studied by changing their sizes and angles. Indeed, optimizing the triangular shape dimensions led to a maximum V_{BR} of 760 V. However, the breakdown voltage versus the gate corner parameters remains relatively constant since the high electric field stays concentrated at the bottom gate corner (Figure 22).

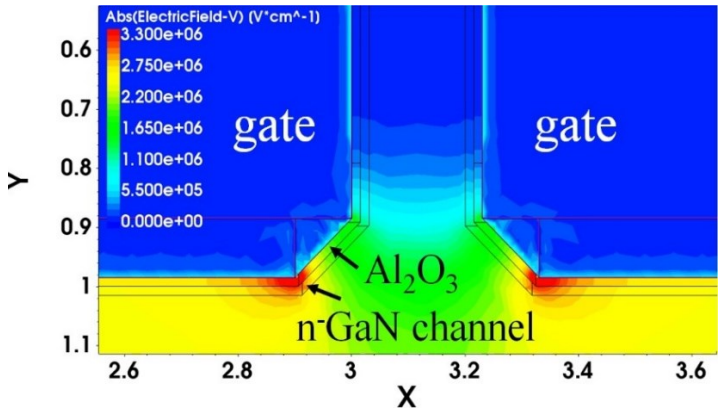

Figure 22: Cross-section shows the electric field distribution for the simulated vertical GaN FinFET (VGS=0V, VBR=697V).

3.5.1.3 Impact of gate oxide SiO_2/Al_2O_3 combination

To improve the breakdown voltage at the channel region, As depicted in Figure 23(a), an oxide layer (SiO_2) is deposited on top of the gate oxide (Al_2O_3). Interestingly, during the manufacturing process, only the bottom part of the gate is layered with SiO_2. The low electrical permittivity of SiO_2 leads to the peak of the electric field concentrating towards the thick SiO_2 (assuming that the SiO_2 critical electric field is 7 MV/cm), resulting in a higher

breakdown voltage. To match the gate shape observed experimentally, it is noteworthy that a triangular gate shape (Xgate=Ygate=100 nm) was used in the simulations [55].

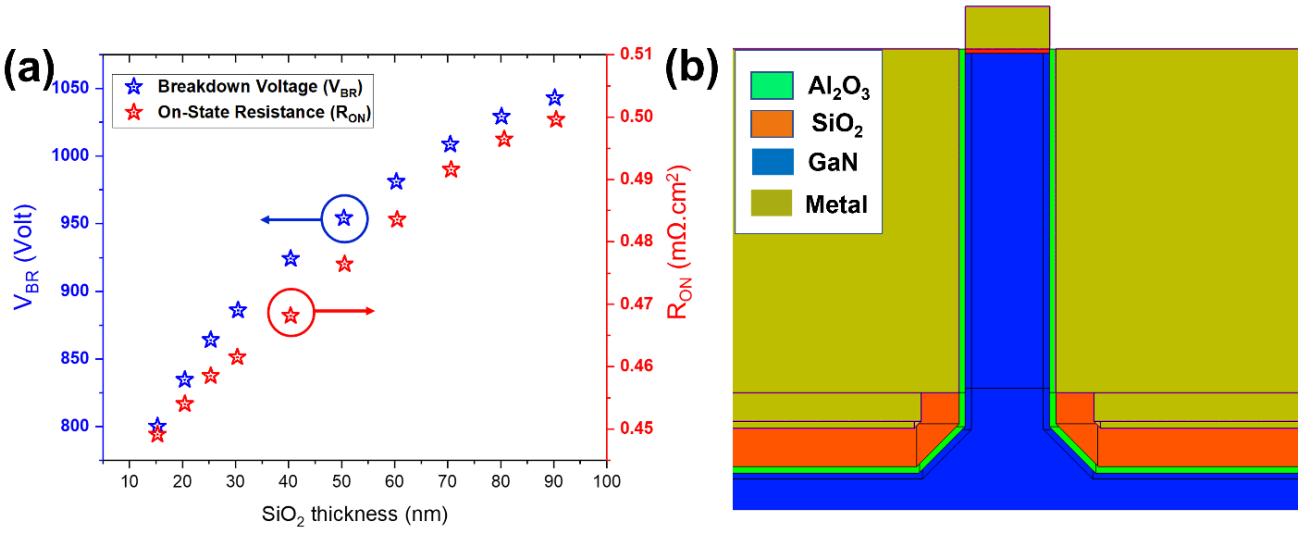

Figure 23: a) The influence of SiO_2 thickness on the V_{BR} and R_{ON}. b).Schematic of simulated vertical GaN FinFET with the SiO_2/Al_2O_3 composite as gate oxide

The effect of such gate oxide combination thickness on V_{BR} and R_{ON} has been investigated, as shown in Figure 23(b). Indeed, for a SiO_2 thickness of 90 nm, we improve the breakdown voltage from 1048V to 1802 V while the R_{ON} increases from 0.5 $m\Omega \cdot cm^2$ to 0.69 $m\Omega \cdot cm^2$. Concerning the I-V curves, It is found that a thicker SiO2 layer leads to a greater breakdown voltage since the electric field peak in the channel is reduced. However, it results in lower transconductance at high V_{GS} due to channel bottom part controllability between the two gates.

3.5.2 Optimization of GaN drift region parameters

As previously mentioned, three important parameters have been incorporated in optimizing the vertical GaN FinFET device: the doping concentration of the drift layer, the thickness of the drift region, and the addition of the n-GaN/n+GaN channel layer at the top of the drift layer region. The impacts of these parameters on device performance have been studied and detailed in the next sections.

3.5.2.1 Impact of the Drift Layer doping concentration

The impact of drift layer doping concentration on V_{BR} and R_{ON} has been investigated by sweeping the doping concentration from $1x10^{16}$ cm^{-3} to $5x10^{16}$ cm^{-3}. It is found that decreasing the drift layer doping concentration from $5x10^{16}$ cm^{-3} to $1x10^{16}$ cm^{-3} also improves the breakdown voltage depicted in Figure 24. Nevertheless, reducing the

drift layer doping concentration will reduce the transconductance of the new epi structure. The transistor operates at high V_{GS} in the linear region of characteristics curves since I_{DS}-V_{GS} was taken at 5V.

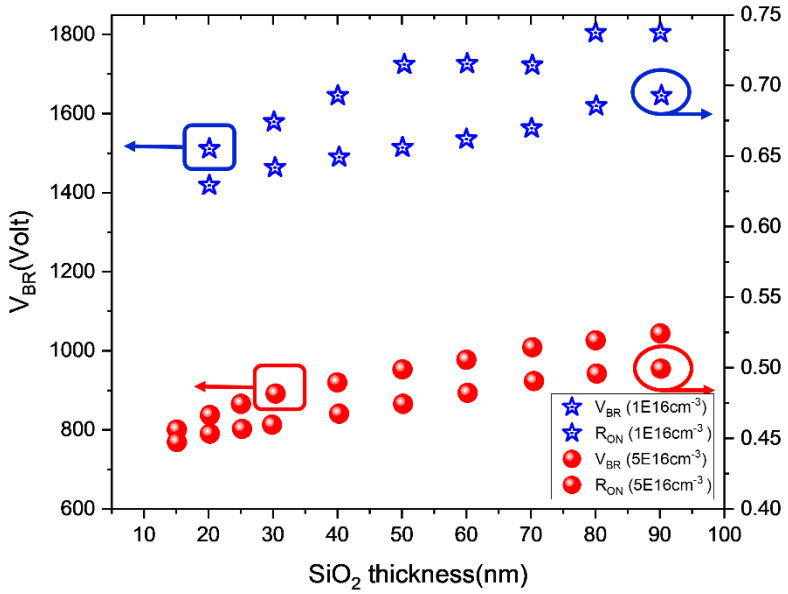

Figure 24:Impact the SiO_2 thickness on the V_{BR} and the R_{ON} for two different Drift Layer doping concentrations ($5x10^{16}$ cm^{-3}: Red and $1x10^{16}$ cm^{-3}: blue).

The I_{DS}-V_{DS} curves correspond to two drift layer doping concentrations (Figure 25). It has been seen that when doping is reduced in the drift region, the transition between the linear and saturation regions is more gradual. This is due to the voltage drop along the drift region. Indeed, a higher drain voltage is needed to pinch off the bottom part of a channel between two gates side by side in front of a drain.

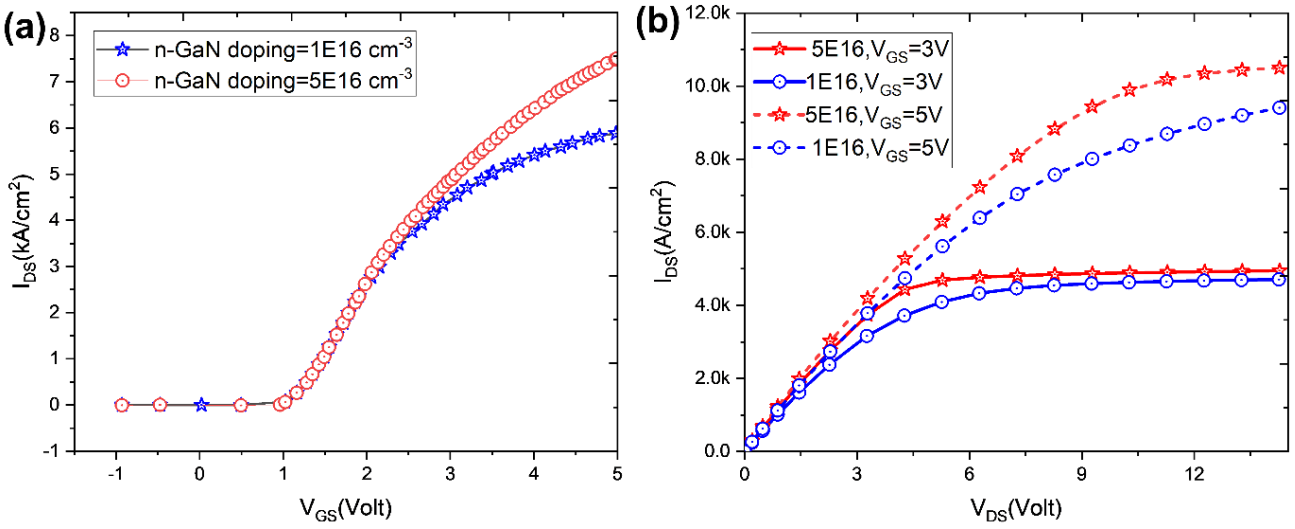

Figure 25: Current characteristics for two different drift layer doping concentration ($5x10^{16}$ $cm^{-3}$and $1x10^{16}$ cm^{-3}),t_{SiO2}=90nm.

Therefore, the drain current saturates with a greater V_{DS} value due to the lower doping in the drift region. The additional voltage consumed to pinch off the channel toward device saturation is called "the voltage waste."

3.5.2.2 Impact of the n-GaN/n+GaN channel layer

An approach to reducing voltage waste in the drift region of a device involves replacing the n-GaN drift region with a composite n-GaN/n+GaN channel layer. The underlined approach was validated by steeping the doping concentration of n+GaN and then analyzing I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristic curves to determine the performance parameters (e.g ., V_{BR} and $R_{ON,}$ etc.). It is observable from the obtained results that as the doping concentration is higher, the related voltage waste will be decreased. To the best of our knowledge, this can be explained as follows; Firstly, since the channel layer n+GaN is less resistive, drain potential can reach the gate end easily. Secondly, by increasing the doping of the top layer of the drift region, it becomes more equipotential, which allows the gate-drain voltage to be stronger, allowing the channels to pinch off at a lower voltage. The impact of n+GaN doping concentration on the V_{BR} and R_{ON} parameters is shown in Figure 26.

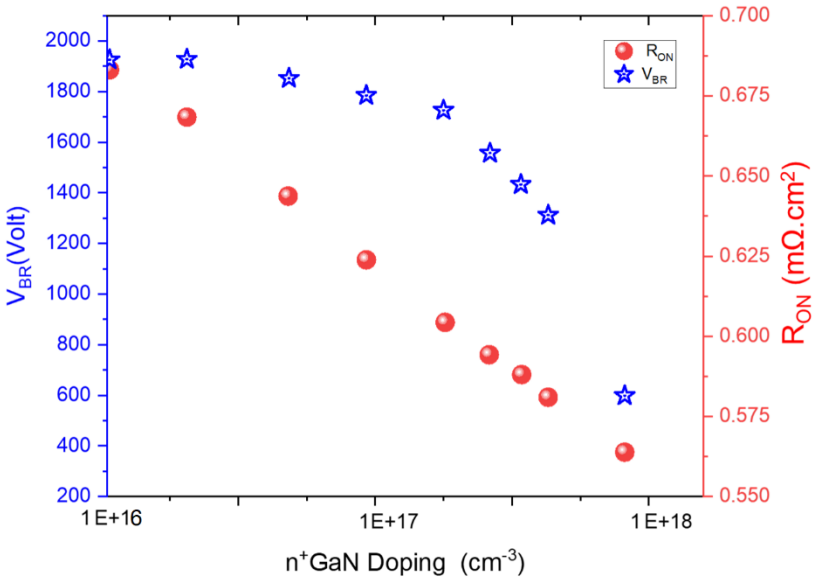

Figure 26:Impact of the n+GaN doping concentration on the V_{BR} and R_{ON}. at 0.3µm N+GaN thickness.

It was observable from Figure 26 that a higher doping concentration leads to a lower breakdown voltage. This phenomenon can be explained as at high V_{DS} (for V_{GS}=0V), the drift region should be depleted. As the doping level in the top part of the layer increases, the depletion at high V_{DS} becomes more and more difficult, leading to an increase in the electrical field. It could explain why the V_{BR} drops when the doping level of the top part of the drift

region increases. A doping concentration of $5x10^{16}cm^{-3}$ was chosen for the simulations to optimize the potential waste and breakdown voltage.

3.5.2.2.1 Impact of the n+GaN layer thickness

The impact of the n^+GaN layer thickness has also been investigated by varying its value between 0.3 µm and 4.2 µm, starting from the gate to downward. According to the same reasons as the section on n+GaN doping concentration, device behavior could be elucidated in response to n+GaN layer thickness variation. As a result, simulations have shown that the thicker the n+GaN channel layer is, the lower the voltage waste at the expense of breakdown voltage. It was determined that 0.7µm was the optimal thickness, giving the best agreement with breakdown and voltage waste.

3.5.2.2.2 Impact of the Drift Layer thickness

To optimize the drift region thickness, it is necessary first to investigate the impact of the thickness parameter on both V_{BR} and R_{ON} values. Accordingly, the drift layer thickness has been simulated, starting from 5µm to 27µm. The V_{BR} and R_{ON} parameters are extracted as previously explained in this chapter. Figure 27 illustrates the obtained results from the simulation. It is noteworthy that, as the low doping part of the drift region is thicker, the R_{ON} significantly increases since this layer is relatively highly resistive.

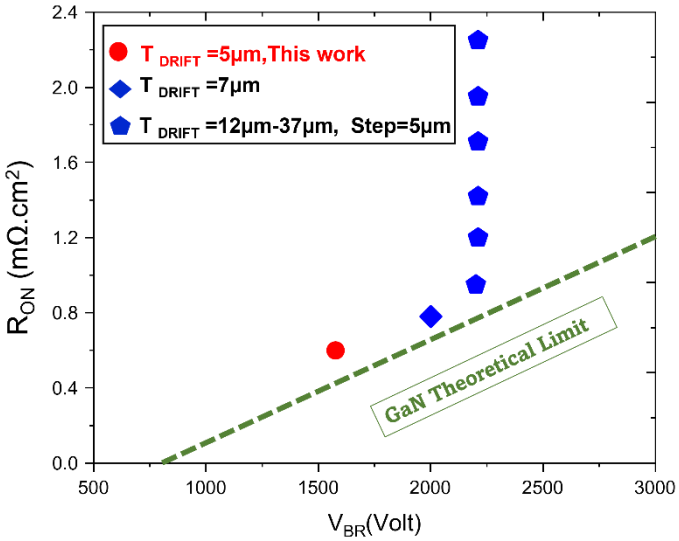

Figure 27:Impact of the Drift Layer thickness on the V_{BR} and the R_{ON}.

Meanwhile, the V_{BR} increases with region thickness and reaches saturation at about 2.2 kV for drift regions over 12µm. Regardless of drift region thickness, the breakdown occurs at almost the same voltage at the gate corner.

This limitation is because the drain to gate voltage will no longer have access to the additional drift region thickness region to deplete it. This limitation needs to be deeply studied and overcome to improve the V_{BR} for Normally-OFF Vertical GaN FinFET.

The first optimized version of vertical GaN FinFET has been chosen to have 90 nm-thick SiO_2 gate oxide and 0.7 µm-thick of n^+GaN channel doped $5x10^{16}$ cm^{-3}. It has a breakdown voltage equal to 1576 V and the R_{ON} to 0.61 $m\Omega \cdot cm^2$ with a 5µm drift region thick.

3.5.2.3 Validation of n-GaN/n+GaN (zebra model) utilization for drift Layer optimization

This section investigates the capability to enhance the V_{BR} and R_{ON} values by dividing the drift region into n-GaN/n+GaN blocks, as illustrated in Figure 28(a). This drift layer design is called the "Zebra model." The optimization starts by adding the n+GaN layer with 0.7µm thick and 5×10^{16} cm^{-3} doping concentration (Figure 28(b)). The Simulation targets changing one of the doping values for all n+GaN blocks while the thickness was constant. Accordingly, both doping and thickness for the n-GaN will also be constant. Subsequently, the other parameters will be swept separately to find the optimum value of both doping and thicknesses for each n^- GaN/n^+GaN block.

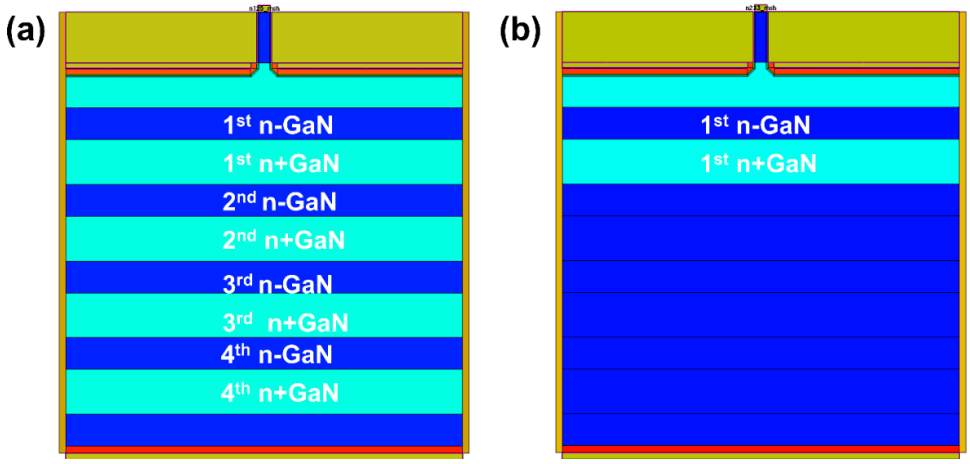

Figure 28: Schematic of n-GaN/n+GaN blocks in Drift Layer (zebra model) a)for all residual n-GaN drift region b)only one n-GaN/n+GaN blocks

After careful analysis of the simulation results, we found that any enhancement in R_{ON} will be at the expense of the V_{BR} value. For instance, increasing the doping concentration of one block will improve the R_{ON} value. However, the V_{BR} value will also be decreased due to the increase in the electric field value in that region. Due to

the performance degradation resulting from the addition of n+GaN, the thickness of the n+GaN addition needs to be reduced to its minimal value making the zebra model unsuitable for device performance optimization. The extracted values for R_{ON} and V_{BR} vs. n+doping concentration is shown in Figure 29

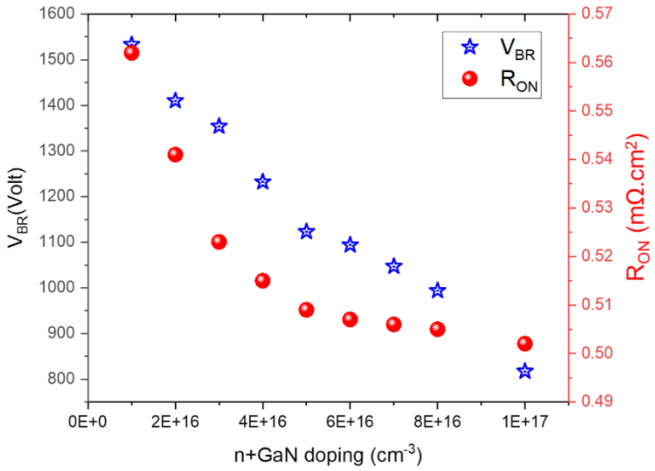

Figure 29:Impact of the doping concentration of added n+GaN on VBR and RON values

3.5.3 Comparison between the first optimized version and the real epitaxial-GaN wafers

As mentioned in this chapter, we discussed the first optimized version with the CPiGaN-ANR project partners in France (CRHEA-CNRS). We observed that some optimized parts couldn't be realized. Indeed, the optimized device specifications need to be replaced with ones aligned with the GaN epitaxial growth without degrading the device's electric performance. The epitaxial Schematic of the wafer after grown is shown in Figure 30.

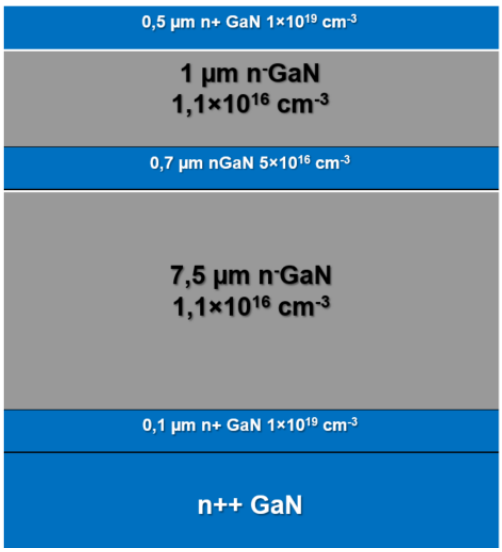

Figure 30: Schematic of real GaN epitaxial wafer ready for the fabrication process

The new design corresponds to the real GaN epitaxial wafers that have been simulated and compared to the first optimized structure. Both structures related to optimized and real epitaxial wafers have then been simulated and compared. We found that our optimized structure has V_{TH}, R_{ON}, and V_{BR} values of 0.67V,0.61 mΩ.cm^2, and 1576 V, respectively. While the structure based on real epitaxial layers has V_{TH}, R_{ON}, and V_{BR} values of 0.67V, 0.8 mΩ.cm^2, and 2154V, respectively. Figure 31shows the simulated I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristic curves for both structures using *Sentaurus* TCAD.

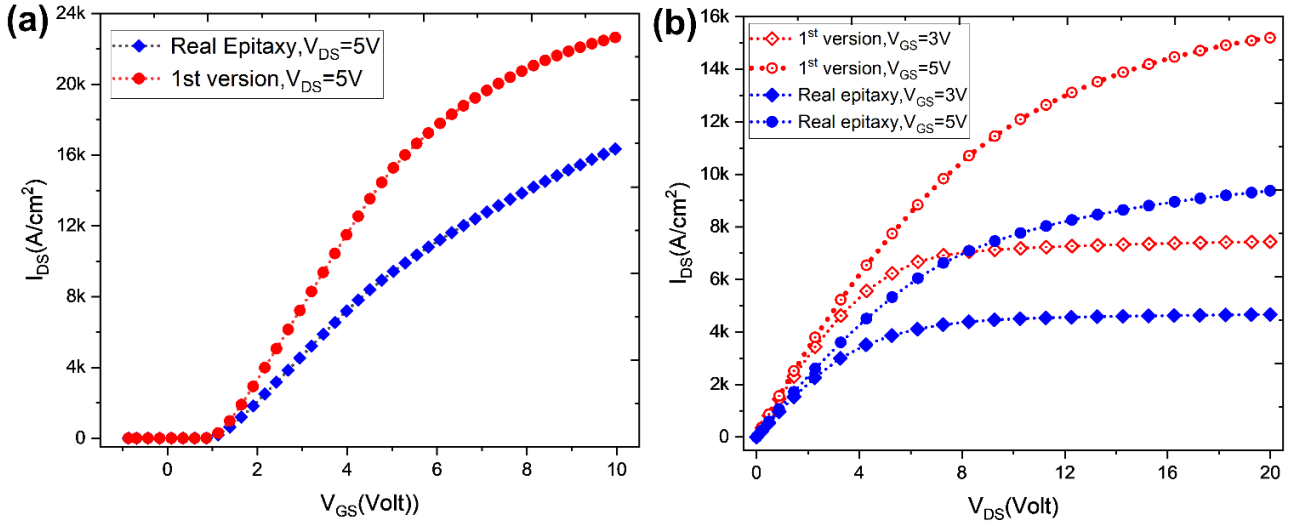

Figure 31: I_{DS}-V_{DS} and I_{DS}-V_{GS} of the 1st optimized version and the one based on the real epitaxial structure, a) I_{DS}-V_{GS} and b) I_{DS}-V_{DS}

It is observable from Figure 31 that the saturation current and the R_{ON} of the optimized structure are better than those for the one based on the real epitaxy. This can be explained by the increase of the R_{ON} resistance of the later structure due to the increase in the drift layer and channel thicknesses. On the other hand, the structure based on the real epitaxy has around 578V enhancement for the V_{BR} resulting from such drift region thickness enlargement. Furthermore, the comparison between the optimized structure and the real wafer ready for the fabrication process has been described in Table 4.

Table 4: Comparison of dimensions and doping levels of the real wafer structure and the optimized one using Sentaurus TCAD software

Dimensions and doping	The real GaN epitaxial /GaN (device structure)	The value used in 1st version of simulations[42]
THE WIDTHS		
Total device Width [µm]	6.23	**6.23**
Gate width grids Lg [µm]	3	**3**
Gate width-to-gate L_{gtg} [µm]	0.2	**0.2**
Width of the gate oxide L_{ox} [nm]	15	**15**
THE THICKNESSES		
The thickness of layer n+GaN source side [µm]	0.5	**0.1**
The thickness of the channel layer n-GaN [µm]	1	**0.8**
The thickness of the top of drift region nGaN [µm]	0.7	**0.7**
The thickness of the drift region nGaN [µm]	7.5	**5**
The thickness of layer n+GaN drain side [µm]	0.1	**0.1**
The total thickness of the device [µm]	9.8	**6.7**
DOPING CONCENTRATION		
Doping of the n-layer+GaN source side [cm^{-3}]	1×10^{19}	$\mathbf{4\times 10^{18}}$
Doping of the channel layer n-GaN [cm^{-3}]	1.1×10^{16}	$\mathbf{1\times 10^{16}}$
The thickness of the top of drift region nGaN [cm^{-3}]	5×10^{16}	$\mathbf{5\times 10^{16}}$
The thickness of the drift region nGaN [µm]	1.1×10^{16}	$\mathbf{1\times 10^{16}}$
Doping of the n-layer GaN drain side [cm^{-3}]	$\mathbf{1\times 10^{19}}$	$\mathbf{4\times 10^{18}}$

3.6 Parameter's sensitivity in the design of Vertical GaN power FinFET

The sensitivity of the parameters incorporated in the optimization process has been determined. The main goal is to quantify the impact of each parameter on the device's performance. The sensitivity calculation starts by sweeping one parameter while keeping others constant and then extracting R_{ON} and V_{BR} from I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristic curves. The sensitivity of such parameters could be calculated based on the following equation.

$$S(\%) = \left|\frac{P_F - P_I}{P_I}\right| \times 100\% \quad (3.1)$$

Where P_F is the value of R_{ON} or V_{BR} for the final value of the parameter, P_I is the value of R_{ON} or V_{BR} for the parameter's initial value. The impact of variation in sensitivity percentage for the breakdown voltage and the on-state resistance R_{ON} will be an outstanding reference in any upcoming optimization scenario suggested enhancing

device performance. Figure 32 and Figure 33 illustrate the sensitivity in R_{ON} and V_{BR} values for the incorporated design parameters, respectively.

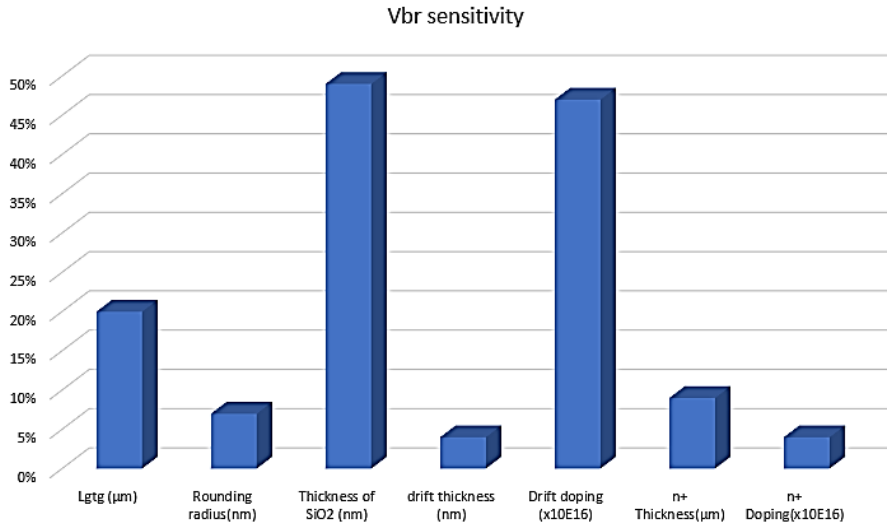

Figure 32: The sensitivity of parameters to VBR

It is worth mentioning that the thickness of SiO_2, drift layer doping, and gate to gate lengths have the highest impact on the breakdown voltage of vertical GaN FinFET devices.

As shown in Figure 33, it is observable that most of the optimization parameters have a significant impact on the R_{ON} value, except the doping of the n^+GaN region at the top of the drift region.

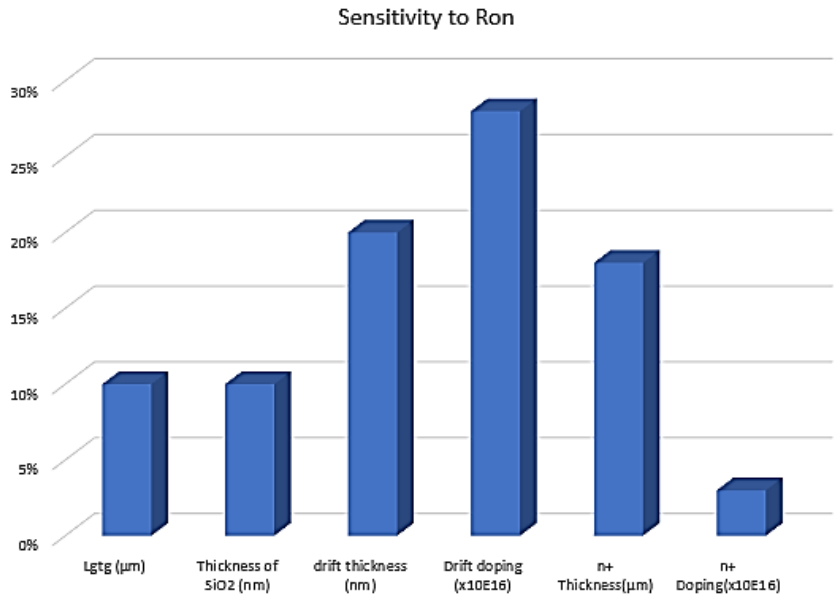

Figure 33: The sensitivity of parameters on R_{ON}

3.7 Conclusion

This study indicates that the breakdown voltage at the corner of the GaN channel primarily limits the performance of the vertical device. A thicker gate oxide composite SiO_2/Al_2O_3 was added to increase the breakdown voltage. With a 90 nm SiO_2-thickness, the breakdown voltage was improved from 697 V to 1043V, and then, When the drift layer doping concentrations are decreased from $5x10^{16}$ cm^{-3} to $1x10^{16}$ cm^{-3}, the breakdown voltage can be improved to 1802 V. However, the higher breakdown voltage of 1802 V may be achieved at higher R_{ON} of 0.69 $m\Omega \cdot cm^2$. It is worth mentioning that the additional SiO_2 will have no impact on the V_{TH} value since it is not located in the channel area (It is in the n+GaN layer under the channel).

The n-GaN/n+GaN configuration has been added during the design process to reduce the voltage waste with 1576 V and 0.61 $m\Omega.cm^2$ for breakdown voltage and R_{ON}, respectively. The optimized structure has been updated to align with the realistic GaN epitaxial wafers.

CHAPTER FOUR: INTRODUCTION TO VERTICAL GAN FINFET FABRICATION PROCESS

4.1 Introduction

Following the optimization of the design of vertical power GaN FETs using TCAD simulation, the focus now turns to the processing modules to manufacture them. In this regard, this chapter details the concepts for optimizing the fabrication process. Accordingly, the epitaxial growth of GaN, design of the mask, and description of each process step will be described. There have been two stages of the processing carried out; first, a testing process is proposed to optimize the fabrication steps by using UV-lithography and dielectric as a mask. At this stage, gate metallization (GM) and GaN etching (GAN) were especially important processing modules we spent the most time testing and optimizing. Thus, the second stage highlighted the final processing modules using the "self-aligned device technique" and electron beam lithography (EBL) for source contact patterning. Also, in this chapter, we will discuss the objectives, challenges, and details of the two stages. Lastly, the next chapter will discuss each fabrication stage's optimization process.

4.2 GaN epitaxial growth

Here, the epitaxial layer structure layer by layer has been investigated, from bottom to top. Firstly, we will mention the highly doped N++ GaN, and sapphire substrate have been chosen to grow two different wafers with the same epitaxial layers. The sapphire substrate type will be used to optimize the final fabrication process modules, while the GaN epitaxial on the GaN wafer will be used to fabricate the final device. A schematic representation of the MOCVD process may be found in Figure 34.

The GaN epi-layer wafer grown by Metal-Organic Chemical Vapor Deposition (MOCVD). Also is known as Metalorganic vapor-phase epitaxy (MOVPE), organometallic vapor-phase epitaxy (OMVPE), or metalorganic chemical vapor deposition (MOCVD)[56]. It is a chemical vapor deposition method in which crystal growth occurs through a chemical reaction, where reactants form metal-organic, and hydride precursors in the gas phase are deposited. MOCVD grows new layers with the same crystal structure (such as lattice structure and crystal orientation) as the substrate below it, which allows for the growth of sequential epitaxial layers of varying material

composition.

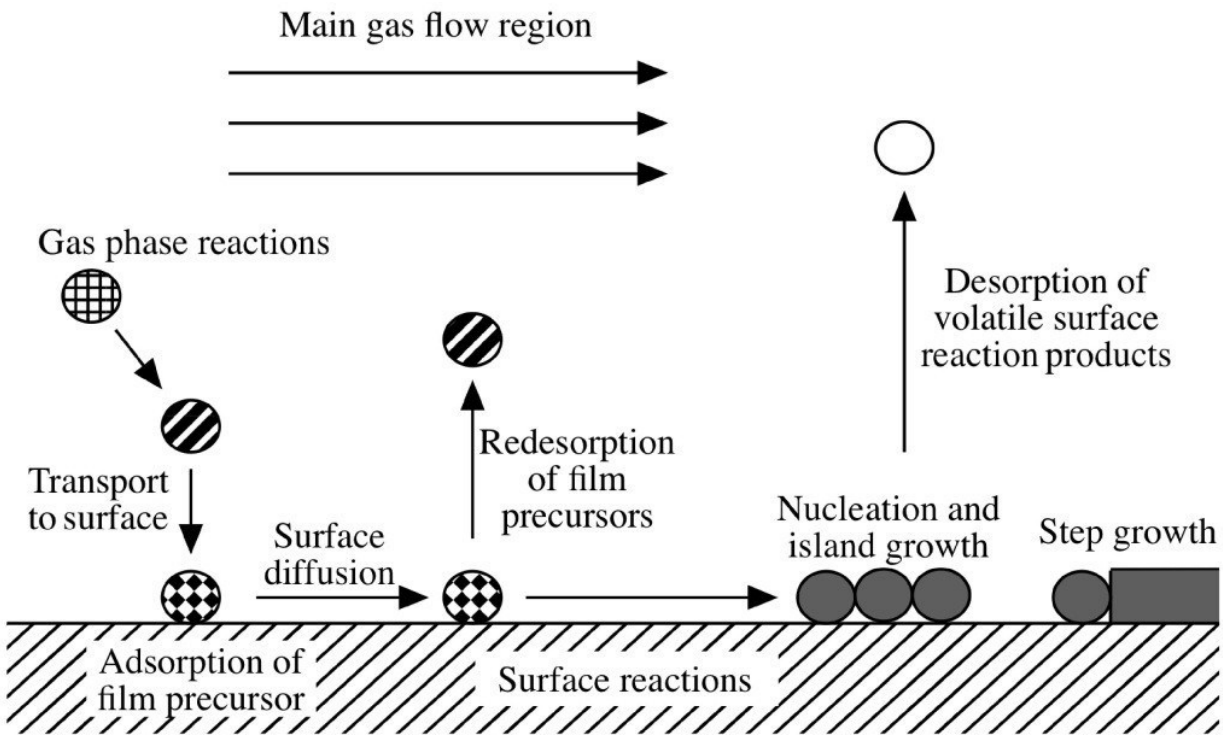

Figure 34:Schematic representation of the fundamental transport and reaction steps underlying MOCVD [50]

This operation allows the growth of a wide variety of materials, unlike other CVD techniques, and is thus a very versatile method. The MOCVD procedure may be divided into the following steps, as described by Dapkus et al. [57]:

1. Mass transport of the reactants/precursors in the reaction chamber to the substrate surface by a carrier gas

2. Surface reactions involving thermal decomposition of the reactants, such as separation of a compound into its elements via thermal energy, followed by adsorption/desorption, surface diffusion, and nucleation

3. New layer growth, one two-dimensional monolayer at a time

4. By-product removal from the reaction chamber.

Accordingly, the first step involving the transport of the group III element, such as Ga to the substrate surface, is the growth-limiting step [57][58]. Group V elements are more likely to desorb from the surface than group III

elements, and thus, an excess of group V elements is required. It is also possible to include dopants in the carrier gas and incorporate them into the grown layer. The ability to select the reactants entering the reaction chamber with the carrier permits abrupt heterojunctions by varying the gas composition. High flow rates are required to produce the required abruptness [58].

For the wafers used in the optimization and fabrication process, a highly doped n+GaN starts the GaN epitaxial with 1×10^{19} cm^{-3} with 0.1 µm thick to ensure the ohmic contact with the drain. The drift layer is grown with 7.5 µm thick and n-GaN doped layer with 1.1×10^{16} cm^{-3} concentration. The drift region's top layer is grown with 0.7 µm thick and nGaN doped layer with 5×10^{16} cm^{-3} concentration. Subsequently, the channel layer will be grown with a 1µm thick and nGaN doped layer with a 1.1×10^{16} cm^{-3} concentration. The last layer to be grown is the n+ GaN epitaxial layer with 1×10^{19} cm^{-3} and 0.5 µm thick to ensure the ohmic contact with the drain and increase the gap between the gate and the source to minimize the C_{GS} value. The epitaxial layers of the wafers are described in Figure 35.

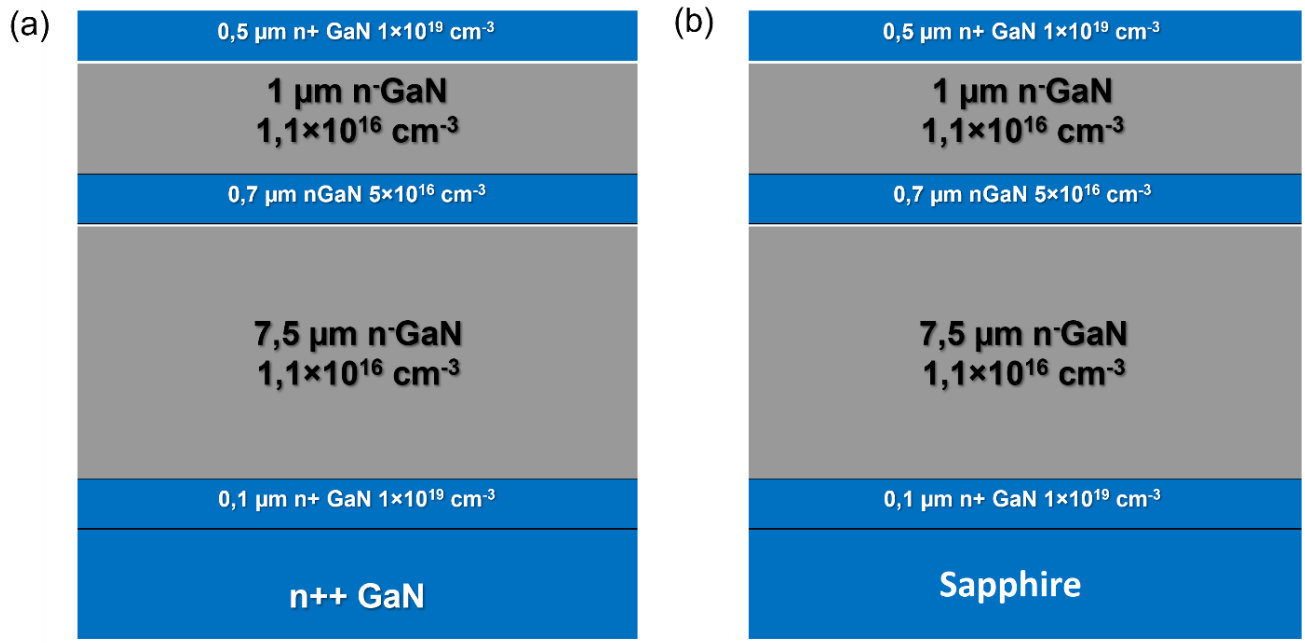

Figure 35:The schematic of real GaN epitaxial wafers on GaN and sapphire substrates;(a) GaN wafer and (b)Sapphire wafer

4.3 Introduction to vertical GaN FinFET fabrication process

This section will describe the processing module to fabricate the vertical GaN FinFET device. In light of this,

there are two main approaches for fabrication: the top-down approach and the bottom-up approach. Due to its implementation simplicity. The top-down approach has been used for our fabrication process.

The illustration of the main processing modules used in the final Vertical GaN FinFET fabrication process is shown in Figure 36. Some modules have been optimized using Si wafers with testing masks since they are inexpensive. Other modules such as the orientation determination and GaN wet etching are optimized using GaN/sapphire and GaN/Si wafers. Finally, the process will be implemented on the Epi- GaN/GaN wafer to fabricate the final device.

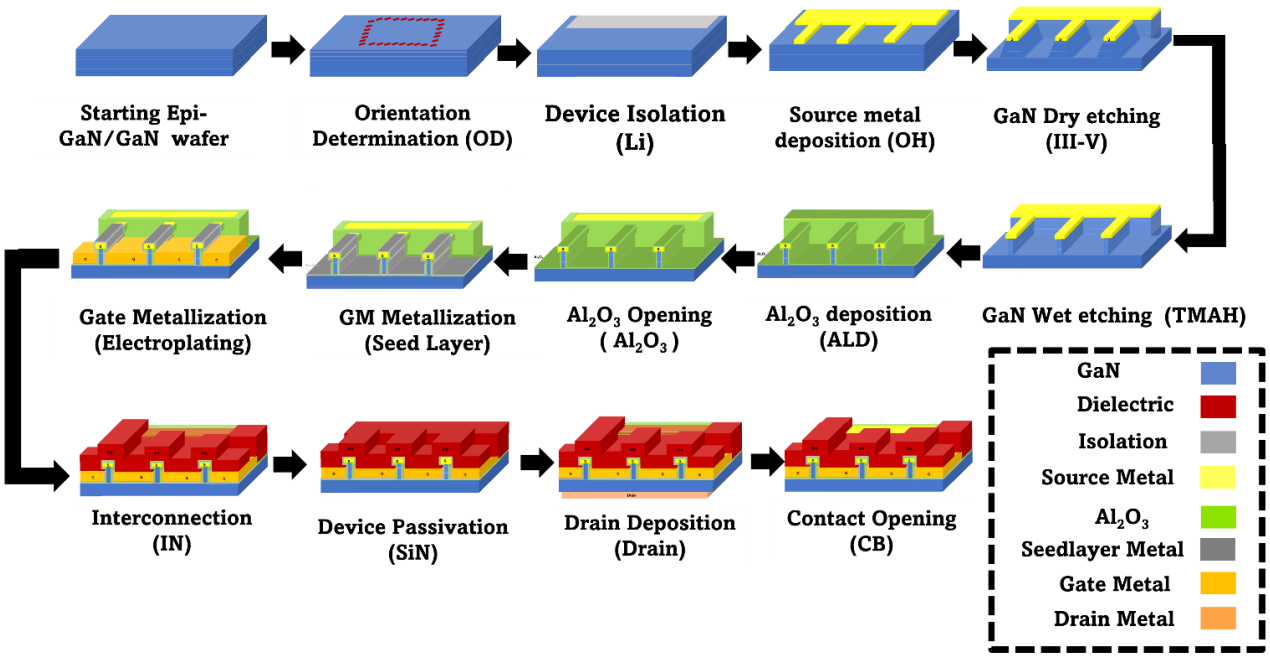

Figure 36:Sequence of final vertical GaN FET processing modules

4.4 A detailed description of vertical GaN FinFET processing modules

The remaining part of this section will review each fabrication step, including the objectives, challenges, and processing steps.

4.4.1 Wafers dicing

Following a wafer of semiconductor material processing, coupon samples are separated from the wafer by dicing. All dicing methods are automated to ensure precision and accuracy, whether scribing and breaking, mechanical sawing (usually with a dicing saw), or laser cutting[59].

The wafer is attached with dicing tape placed on both sides regarding the dicing process. A thin layer of protection resin is spun before dicing to protect the wafer from scratching during the dicing process. After the dicing process. The laser dicing machine is used in our process to have 1cm×1cm dimension coupons from the 2-inch GaN wafer. The flat zone direction shall be marked on the backside of the dies (coupons) to be a reference for the orientation of the lithography process. We are also using the diamond pen to dice the silicon wafers where the shape of the sample is not important since they will be used only for process optimization purposes. After the marking has been done, the coupons will be detached from the tape and prepared for the cleaning process.

4.4.2 Samples Cleaning process

The cleaning steps are essential in microfabrication. Indeed, these steps can constitute nearly 30% of all the process steps. Even if the microfabrication takes place in cleanrooms where the number of particles is strictly regulated, these different cleaning steps must still be carried out to ensure no contaminant on the wafer. Moreover, particles are not the only class of contaminants. We can also think of metals, organic materials, and native oxides. When we want to clean our wafer, several means are available depending on the contaminant to be eliminated. Indeed, the most common way is the use of chemical solution baths. However, in several stages, it is essential to have a sample with minimum contamination and mechanical faults on the surface to ensure good performance at the end of the process. Obviously, the quality of the sample surface has a drastic influence on the operation of the final device. It should not be forgotten that since there are several steps before arriving at the final product, the number of contaminants that can change the device structure is very large. Therefore, these steps should not be taken lightly, and that there must be a multitude of cleaning steps in a process.

We can divide the cleaning steps we performed during the fabrication process into four main parts:

- An initial cleaning with solvents to reduce the number of organic contaminants with the following sequence: sample immersion in remover for 1hour, acetone for 5 min, then 5 min in isopropanol (IPA), a rinse with deionized water, and drying with the nitrogen jet. Finally, the Plasma O_2 removes the residual organic component on the sample surface.

- Masks cleaning with piranha solution (mixture of H_2SO_4: H_2O_2 (2:1)): the immersion of the mask for 15 min in this sauce makes it possible to eliminate the organic residues remaining after cleaning with the solvent.

- Deoxidation of the surface of the GaN wafers with diluted hydrochloric acid (HCL: H_2O (1:10)): immersion for 1min makes it possible to remove the native oxide layer formed during the treatment with the piranha solution. In silicon samples, the (HF: H_2O (1:10)): immersion for 15 sec is used to remove the native oxide layer formed during the treatment with the piranha solution.

Table 5 summarizes the cleaning procedure used in this process after dicing the samples.

Table 5:Cleaning process for the samples after dicing process

Step	Details			comments
02.01	**Cleaning**			**To clean the protection resin on the top of the wafers**
	02.01.01	Remover 1165	1 hour/70°C	
	02.01.02	Acetone	5min	Blow Acetone after transferring the sample to IPA beaker.
	02.01.03	IPA	5min	Blow IPA before rinsing
	02.01.04	Drying	The 30s	Drying with N_2
	02.01.05	Plasma O_2	150W / 300mT / 10min	

4.4.3 Orientation determination process (OD)

One of the critical steps to fabricate the vertical GaN FinFET is wet etching. Explicit, the wet etching will be used after the channel definition step using the Plasma etching (ICP-RIE) to engineer the shape of the channel in which it will be straightened and cleaned from ICP-RIE damages. Since that, the wet etching process will be carried out with Tetramethylammonium hydroxide (TMAH) solution, in which the etching will be crystallographic. To precisely reveal them-GaN and a-GaN channel sidewalls, The device should be precisely oriented to the m or a-plane.

The orientation determination procedure is a novel pre-alignment step for the GaN-on-GaN wafers. We usually work on a coupon, not the whole wafers in which the flat zone is not precisely presented. To avoid any confusion regarding the orientation of the Fins, the orientation determination (OD) procedure is a simple approach

that can be used during the fabrication of the device on a coupon made by dicing a 2" wafer to recognize the orientation and the type of crystal plane with one-degree resolution.

To implement the orientation determination procedure, 180 fingers with 15×2 μm^2 dimensions oriented from 0° to 180° from the coupon flat zone are fabricated as described in Figure 37. The fabrication process starts with depositing a 1µm thick SiO_2 (PECVD) layer on the wafer to act as a mask. An e-beam lithography is performed with PMMA 9% resist for finger definition. The SiO_2 is etched using dry etching to transfer the pattern from the resist to the SiO_2 mask. This step is followed by the ICP-RIE etching of 2 µm of GaN to form the FINs, and finally, the GaN wet etching is performed using the TMAH solution. The incorporated recipe mainly consists of TMAH 25% heated in glassware for (80 C°-85 C°) temperature range with UV-assisted source. The Fins will be investigated using SEM to determine the best orientation for the flat zone to precisely align the upcoming fabrication steps.

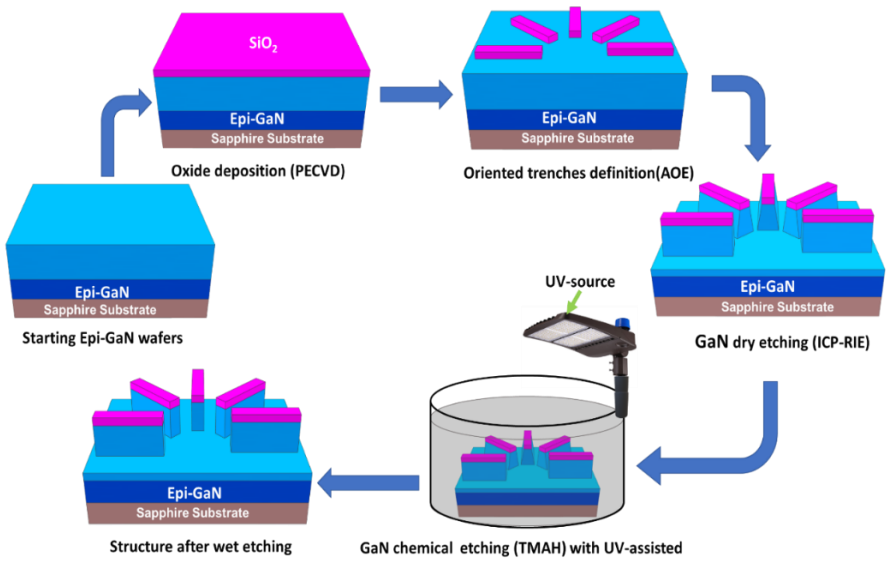

Figure 37:Fabrication process for GaN fingers sidewalls engineering

4.4.4 Device Isolation(Li)

After determining the exact orientation of GaN crystallographic planes, it is time to isolate the inactive parts of the wafer where it might be a source of leakage current when the device is in its off state. The source pads, the device surrounding, and the end of the fingers are the targeted areas to be isolated. The isolation creates a high-resistivity region resulting from the induced lattice damage. Ion implantation is a well-proven technique for the selective creation of such regions in compound semiconductors. The process is known as implant isolation. It is

widely used to obtain inter-device electrical isolation with the significant advantage over selective wet or dry etching of maintaining the planarity of the wafer surface[60][61][62].

The Lithography of the isolation step has been done using UV-Lithography and the Li mask. For the Li mask cleaning, an acetone cleaning, IPA rinsing, and N_2 drying shall be done, followed by a piranha with (H_2O_2:H_2SO_4) with (1:3) dilution for 15min (the mask must be dry to avoid reaction between organic compounds and the acid). Now, the wafers and the mask are ready for the isolation process. The detailed steps to perform the Li process is depicted in Table 6.

Table 6:wafer Isolation process (Li) description using UV-Lithography and Ion implantation

Step	Details		
03.01	**Lithography**		
	03.01.01	Dehydration	150°C / 5min
	03.01.02	MCC Primer	4000rpm / 60s
	03.01.03	LOR3A	4000rpm / 60s
	03.01.04	Soft bake	165°C / 5min
	03.01.05	AZ9245	4000 rpm / 60s
	03.01.06	Soft bake	110°C / 2min
	03.01.07	Photolithography UV AOI 806	200mJ.cm-2 / N2 hard contact (20mA) / LI layer
	02.01.08	Developing AZ400K (1:4)	1min30s+1min30s
	03.01.09	DI Water / Drying	30s / N2
	03.01.10	Plasma O2	50W / 300mT / 3min
	03.01.11	Characterization	Optical microscope / Profilometer
03.02	**Nitrogen implantation**		
	03.02.01	Ion implantation	
	03.02.02	Characterization	Optical microscope / Profilometer
03.03	**Cleaning**		
	03.03.01	Plasma O_2	150W / 300mT / 10min
	03.03.02	Remover 1165	1 hour/70°C
	03.03.03	Acetone	30min
	03.03.04	IPA	10min
	03.03.05	Plasma O2	(150W / 300mT / 10min)x3
	03.03.06	Characterization	Optical microscope

After the isolation process has been done, the wafer becomes ready for the source deposition step (OH). The detailed process set up for the source metallization will be introduced in section 4.4.5. as detailed in Table 6, a preliminary dehydration step shall be performed before spreading the resists using the spinning coater.

4.4.5 Source deposition process (OH)

The metallization will be performed through the lift-off process for the source deposition step, and the e-beam evaporator will deposit the metallization stack. Since the channel width in our design will not exceed 200nm and due to the limitation of UV-Lithography resolution of up to 0.7µm, the electron beam lithography (EBL) has been used for the source deposition. Furthermore, the source metal will be used as a mask to create a self-aligned FIN channel. Considering this, two major optimization scenarios shall be carried out; Firstly, the EBL process shall be optimized to successfully create the lift-off profile with finger width between 200 and 250nm. Secondly, the source metallization stack should be compatible with all further processing steps. Explicit, the 1st proposition for the source metallization stack was by using a Ti/Au/Ni stack with (20nm,300nm,50nm) thicknesses, respectively. However, after GaN dry etching, we realized that the Ni is being etched by the recipe used for ICP-RIE for GaN etching. Likewise, for FIN channel treatment after GaN dry etching, with TMAH etchant, the Ti and Ni will be chemically etched in TMAH, causing metal adhesion problems. Therefore, It is necessary to optimize the metallization stack composite of the source as detailed in the next chapter.

4.4.5.1 The lift-off process

For the source metallization by a lift-off process, it is worth mentioning that the lift-Off term refers to creating patterns on the wafer surface through an additive process. The Lift-Off process involves the exposure of a pattern into photoresist (or some other material), the deposit of a thin film (such as a metal) over the entire area, and finally, the removal of the photoresist (or other material) to leave only the patterned area[63]. In our process, the lift-off; lithography is done using (Bi-layer method). Two different resist types have been spun to prepare the sample for EBL, the top layer is the PMMA9% HMW, and t the bottom resist is the ELL11%. The metal film after evaporation and after the lift-off process has been shown in Figure 38.

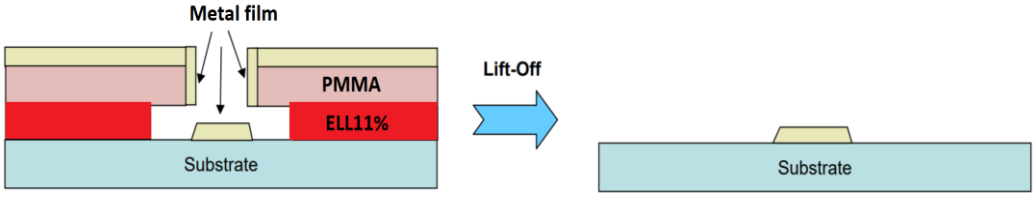

Figure 38:The metal deposition by the lift-off process

4.4.5.2 The e-beam lithography (EBL)

Electron beam lithography (EBL) is a technique that scans electron microscopes (SEMs) to create images using electron beams on electron-sensitive materials. When the resist is exposed to the electron beam, a small pattern is created that either remains on the substrate or is washed away by the developing solution. Depending on the solubility of the material in the developer, the chemical composition of the resist is altered based on the sensitivity of the material when it is exposed to electron energy, leaving a pattern behind. EBL is commonly used to create integrated circuity or larger patterns called masks used for other types of lithography. [64].

Polymers with the same physical properties as photoresists are the EBL resist. However, the EBL resist is sensitive to e-beam energy, which induces chemical or physical changes. This change leads to an easy patterning of resist. Similar to photoresists, electron resists also have positive and negative effects. In a positive electron resist, the electrochemical interaction of the polymer with the electron breaks chemical bonds, forming molecules with shorter lengths. It can be dissolved in a developer solution that attacks low-molecular-weight materials by reducing the molecular weight. Positive electron resists can achieve resolutions as high as 0.1µm. As for negative resists become harder through interaction with the irradiation, and these polymer chains remain after the development process. For both types of resists, a special developer is used to dissolve this material.

Figure 39(a) illustrates the components of the EBL machine. An electron gun produces a beam of electrons with an appropriate density of electrons. Electrons can be generated by heating materials such as tungsten or applying high electric fields to the top of the electron gun. Electron beams are then focused using electromagnetic condenser lenses, producing spots of several nanometers in diameter, which are then switched on and off by beam-blanking plates. It is then possible to create the pattern you desire by manipulating the electron beam's path. Figure 39(b) illustrates the RAITH150Two EBL machine available in LN2-3iT.

There are two techniques for scanning the wafer, the raster method and the vector method. Compared to the raster method, which scans all positions on the wafer and switches on and off when needed, the vector method focuses only on the requested pattern features and jumps from feature to feature instead of scanning the entire chip as in the raster method, thereby saving time.

In both types of scanning, electrons are deflected by coils, which use magnetic and electric fields. A computer controls these coils and operates at MHz or higher rates to direct the focused electron beam to any location on the wafer.

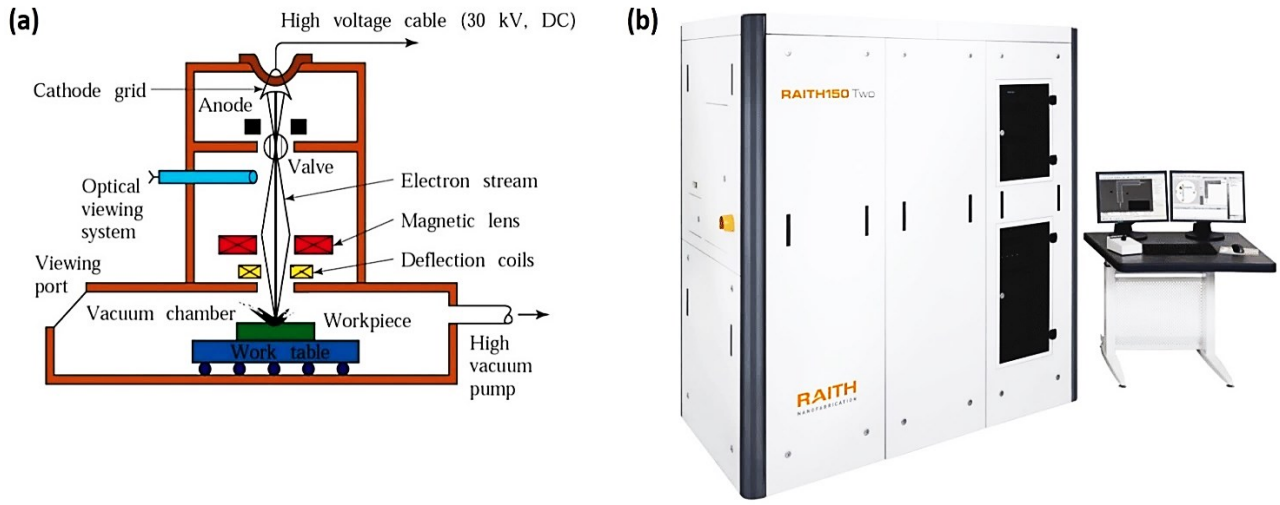

Figure 39:a) Schematic of an electron-beam machine, b) the RAITH150Two EBL machine in LN2-3iT

Thus, EBL enables high-resolution nm-scale patterning of sample surfaces resulting in greater flexibility in design improvement since no mask is necessary. In addition, the exposure process is serial. It has very low throughput and a high risk of damaging samples. EBL has a limited resolution caused by proximity effects created by scattered electrons. Also, it is more expensive than optical lithography. After exposure, the samples are developed in Methyl isobutyl ketone developer to create the patterns.

The detailed source deposition process has been described in Table 7. A de-sum step is required before the GaN dry etching, followed by SEM characterization to ensure that the water is completely clean. This will guarantee symmetrical FINs shapes after the GaN etching process with ICP-RIE.

Table 7:Source metallization (OH) process description using EBL and evaporation

Step	Details			comments
04.01	**Lithography**			**Check the resist thickness with a-Si sample**
	04.01.01	Dehydratation	150°C / 5min	
	04.01.02	ELL11%	4000rpm / 60s	4000rpm_60s_500 on Brewer
	04.01.03	Soft bake	200°C / 2min	Check the temperature with the thermocouple 500nm
	04.01.04	PMMA	4000rpm / 60s	4000rpm_60s_500 on Brewer
	04.01.05	Soft bake	200°C / 2min	Check the temperature with the thermocouple 600nm
	04.01.06	EBL RAITH150Two	250µC.cm$^{-2,\ OH}$ mask	Alignment to the exact flat zone rotation defined by the OD process
	04.01.07	Developping MIBK: IPA (1:2)	2min+2min	
	04.01.08	IPA	25s +5s	5s using the IPA bottle
	04.01.9	Rinsing (N_2)	30 s	
	04.01.10	Plasma O_2 #1	Removal of 10 nm of PMMA around 2 min	Calibration for removing 10nm of PMMA
	04.01.11	Characterization	Keyence and SEM	To check if we have the lift-off profile
04.02	**Source metallization by e-beam evaporator**			
	04.01.01	Deoxidation	10% diluted HCL for 1 min	
	03.02.02	Evaporation	Cr/Au/Cr/Niwith (20/250/50/130)nm, respectively	
04.03	**Lift-off**			
	04.03.01	Remover 1165	1 hour/70°C	Wafers shall be vertically positioned with ends lying down
	04.03.02	Acetone	Three h	Blowing to assist in resist to be lifted. Wafers shall be vertically
	04.03.03	Acetone	Three h	Wafers shall be vertically positioned with ends lying down
	04.03.04	Plasma O_2	(150W / 300mT / 10min)x3	Cooling period of 10 min after each time
	04.03.06	Characterization	SEM	Concentrating on both sides of the fingers ensures no residual PMMA.

4.4.6 GaN etching process (GaN)

The GaN etching process is critical to fabricate the vertical GaN FinFET. It consists of two major parts; Firstly, the channel is defined using the GaN dry etching as the source metal acts as a mask. This process has been carried out using the Inductively Coupled Plasma - Reactive Ion Etching (ICP-RIE). The FINs shapes created by GaN dry etching take trapezoidal shapes with significant damage from the ICP-RIE machine's physical etching.

Thus, the second part of etching will be used by chemically etching the unwanted parts on GaN's FINs sidewalls. Specifically, the TMAH solution will first straighten the FIN shape and then smooth its sidewalls. The challenges to be investigated in this important can be listed as follows:

- Descum recipe to remove the residual PMMA resist after lift-off process, especially on fingers sides.
- Finding the best recipe for GaN dry etching without affecting the source stack.
- Finding the best etchant and recipe for GaN wet etching to engineer the FIN channel.
- Investigating the GaN crystallographic mechanisms to estimate the time required for the FIN channel engineering process.

4.4.6.1 GaN dry etching process with ICP-RIE :

Plasma etching is an essential component for semiconductor fabrication. Low-pressure plasmas can generate high-density ion fluxes for anisotropic etching of a wide array of materials. Plasma etching has two basic requirements: generating ions and then imparting them with momentum to direct them at their target. Once the ions reach their target, they can mechanically or chemically remove atoms from the substrate.

With the ICP process, the excitation uses a time-varying RF source delivered inductively via a coil wrapped around the RIE plasma discharge region, resulting in a changing magnetic field. Through the Maxwell- Faraday equation, this changing magnetic field induces an electric field that circulates the plasma in the plane parallel to the capacitively coupled plasmas (CCP) plates. Collisions of the rapidly moving electrons with the slowly moving ions cause further ionization. Arrangement of the ICP with the RIE creates a very powerful combination. It makes it possible to modify ion density and other plasma parameters using the ICP without significantly altering the CCP-controlled incident energy of ions. In general, as these combined sources are being employed, the ICP controls the number of ions reaching the substrate to produce etching chemically.

In contrast, the CCP controls the ions' momentum to produce etching mechanically. The schematic of the ICP-RIE system is shown in Figure 40. the general schematic of the ICP-RIE system has been described in Figure 40(a). The ICP-RIE etching machine available in LN2 for the III-V etching process has been shown in Figure 40(b)

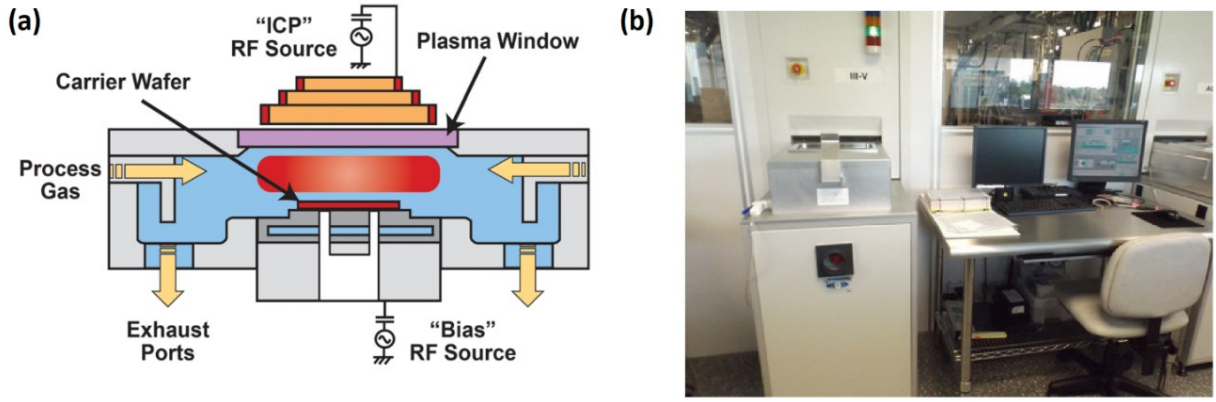

Figure 40: a) Schematic representation of ICP-RIE system. b) STS - Multiplex Inductively Coupled Plasma (ICP) SR III-V (LN2)

For our process, the descaling process will first be done using the O_2 clean recipe in the ICP-RIE machine for 5min. The sample is then characterized using SEM to check if the residual PMMA resist has been removed. If yes, the GaN dry etching will be managed. Otherwise, the step of descum followed by SEM characterization will be repeated. The dry etching process starts with GaN etching rate calibration in the ICP-RIE machine. Two GaN epitaxial pieces with dielectric patterns are used for such calibration. The 1st piece is etched for 2 minutes in the ICP-RIE machine using the same GaN etching recipe (GaN LED). The dielectric mask is then chemically etched using a BOE solution. The profilometer machine is then used to measure the GaN depth etched, and then the etching rate will be calculated. After that, the time to achieve the targeted depth will be calculated based on the measured value of the GaN etching rate from 1st piece.

The second piece is then etched using the targeting depth. The same procedure is then utilized to estimate the etched depth. Once the targeted depth has been achieved using the 2nd GaN piece. The real wafer will then be etched after being stuck on the base disk using the crystal bonding polymer. The GaN LED recipe parameters have been described in Table 8.

Table 8:GaN LED recipe parameters used for GaN etching in ICP-RIE machine

Parameter	value
Coil inductive power (Pc)	400W
RF power (Pp)	200W
Temperature	20°C
Pressure	5mT
Cl_2	15sccm
Ar	5sccm

4.4.6.2 GaN wet etching process:

After the GaN wafer is being etched with the ICP-RIE machine, the next challenge is to engineer the defined FIN channel using the chemical etching. It is very important to optimize a smoothing process to remove the channel's sidewalls imperfections after dry etching. Consequently, it improves the electron mobility at the interface GaN/dielectric of the device. It is also mentioned that the wet etching is used to maintain an undercut at both sides of the FINs with 50nm-80nm width. Such profile will then be used for the gate deposition by the electroplating process. Explicit, to avoid contact between the Gate and the source, the undercut will create a shadow area when the Seedlayer is deposited by evaporation with angle and rotation options. The functionality of the undercut regions can be realized as in Figure 41.

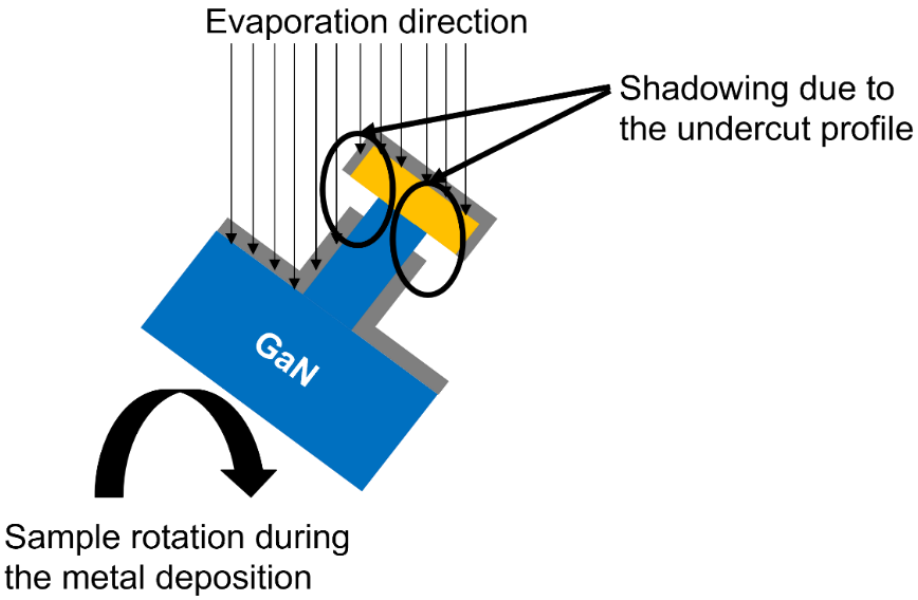

Figure 41:Undercut profile created by GaN wet etching operating as a mask to have the shadowing region during the evaporation

For vertical GaN FinFET devices, a Fin channel structure with non-polar plane side walls is favorable for Normally-Off operation. Non-polar planes at the FinFET channel's sidewall are suitable for fabricating the Normally-Off device because, depending on the channel width, a low charge quantity can be present at $V_{GS} = 0V$ [22-23]. The m-GaN and a-GaN channel sidewalls revealing process require a specific lithography orientation of the Fin channel structure [67].

The chemical etching process has also been demonstrated in the literature for post dry etching treatment of GaN [25–28]. For that purpose, Tetramethylammonium hydroxide (TMAH) is widely used [29-30]. Furthermore, UV light-based TMAH etching is an efficient technique to enhance the GaN sidewalls etching rate [74]. It also improves the etching selectivity when a dielectric material is used as a mask [32-33].

4.4.6.2.1 The theoretical concept of GaN's wet etching with Alkaline solution

TMAH etching results in geometric shapes bounded by perfectly defined crystallographic planes[77]. It is essential to study the evolution of both a and m-GaN crystallographic plan in the presence of TMAH solution to comprehend the concept of wet etching of GaN layers fully. For both m-GaN and a-GaN, the chemical etching mechanism mainly consists of three main steps: OH^- attack of unprotected Ga atoms by the mask and ones on the c-plane affected by dry etching. The second step is forming and dissolving the formation of Gallium oxide (GaO_x) in the TMAH alkaline solution. Finally, at the edge of the mask, the surface will be terminated by N atoms with a significant number of dangling bonds capable of repulsing the OH- ions. Thus, the etching rate will be very low compared to the starting of etching [78]. Despite the etching mechanism similarity of both m and a-GaN, the atomic structure on each plane surface and the etching rate in the TMAH solution is different [79]. Thus, each plane has a different GaN etching rate depending on the etching resistivity of the planes. The etching resistivity of the plane is represented by the etching barrier index (EBI), which could be estimated by multiplying the planar atom density by the surface dangling bonds, as proposed by Yung et al. [80]. Therefore, it is important to model the m-GaN and a-GaN surface evolution during the wet etching to understand both planes' etching profiles. The appropriate plane selection with lower surface roughness will be made based on the proposed atomic models.

The atomic model of m-GaN morphology evolution in TMAH solution has been reported in detail by Junlei He *et* al. [81]. As depicted in Figure 42, two main structures are considered to represent the morphology of m-GaN sidewalls based on the number of the dangling bonds connected to the N atoms on the surface; structure 1 consists of the N atoms with one dangling bond (represented by the dark spheres) while structure 2 represents the N atoms connected to two dangling bonds on the surface (represented by the blue spheres). The starting 2D- crystal reference schematics for a-GaN and m-GaN used for the proposed models, are reported by Jesús Zúñiga-Pérez *et al.* [82] and Junlei He *et* al. [81], respectively.

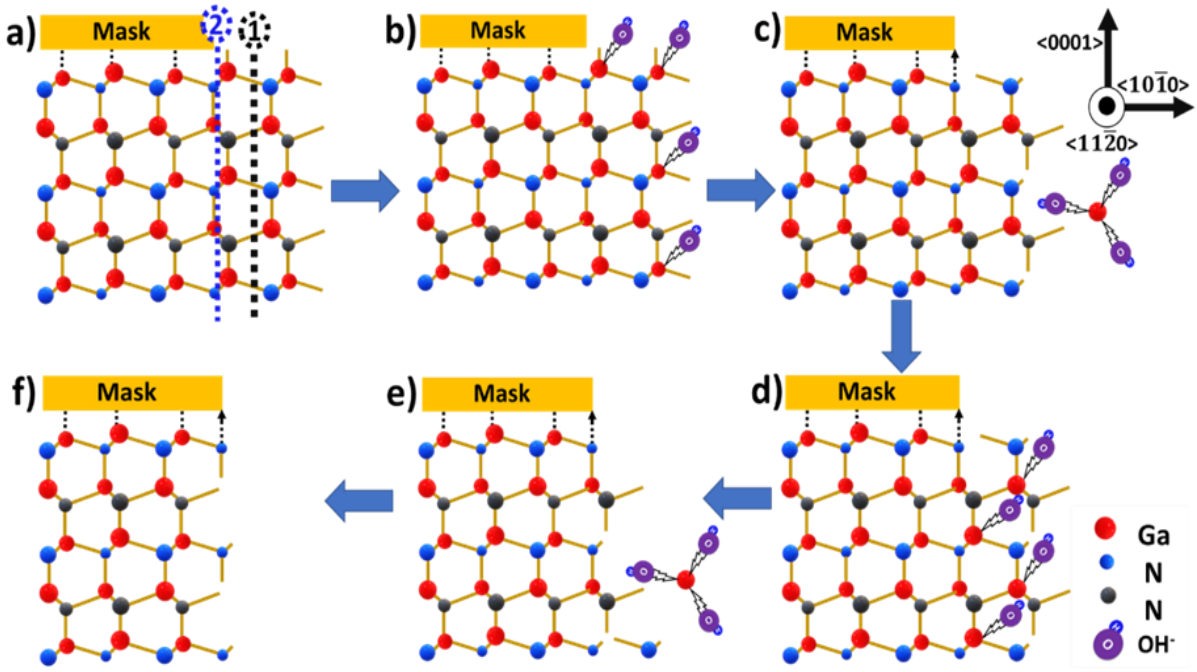

Figure 42: Atomic model for m -plane morphology evolution during chemical etching in TMAH; a) m-GaN surface structures after dry etching, b) OH- attacks the nonprotected parts by the mask on m-GaN and c-GaN, c) the resultant GaOx dissolving in TMAH solution) OH- attacks the Ga atoms away from the mask and structure 1. e) the resultant GaOx dissolves in TMAH solution, f) N atoms at mask edges repelling most OH- attacks to access the lower Ga atoms[26]

The two models will be discussed in detail in the following sections. G.Nowak et al. proposed a mechanism involving OH- ions to oxidize and dissolve GaN in an alkaline solution, respective as follows [83];

$$2\ GaN + 6\ OH^- + 6h^+ \longrightarrow Ga_2O_3 + 3H_2O + N_2 \tag{4.1}$$

and:

$$Ga_2O_3 + 6OH^- \longrightarrow\ 2GaO_3^{-3} + 3H_2O \tag{4.2}$$

The reaction relies on the water in the solution. The TMAH solution used in this thesis also contains water since it was initially mixed with water by 25%. Therefore, the use of water is presented as a vital factor in the reaction. By providing sufficient redox energy, it enables the band to bend, and thus accumulating holes. We believe that the combination of H_2O and holes creates a conducive environment that allows gallium and nitrogen to be separated. We can infer that the last reaction captures the chemical reactions resulting in gallium oxide with an oxidation state of +3 formed in saline-alkaline solution.[84]. Upon dehydration, the H_2O will stop the 2nd part of the reaction, and therefore the Ga_2O_3 will contaminate the GaN's sidewalls. The deoxidation process is required to remove the gallium oxide contamination. In our case, the hydrochloric acid (HCL) diluted in the water with 1:10 percentage is used. The deoxidation reaction in the presence of HCL solution could be described as owed by R.Timm et al. [85]:

$$Ga_2O_3 + 6HCL \rightarrow 2Ga\,Cl_3 + 3H_2O \tag{4.3}$$

The deoxidation step shall be done before any wet etching step during the design of experiments for GaN wet etching optimization.

4.4.6.2.2 Impact of UV- light source on GaN wet etching process

The chemistry of UV- light in etching has been extensively studied.[86][87][88]. For wavelengths shorter than ~365nm, the GaN and TMAH will be photoexcited by photons absorption, in which electron-hole pairs will be produced. The reaction between the GaN and TMAH and the UV-light is respectively described as in the following equations[89];

$$GaN + photons \;\rightarrow\; GaN + e^- + h^+ \tag{4.4}$$

And

$$C_4H_{13}NO + photons \rightarrow 4(CH_3)N^{+\cdot} + OH^{\cdot} \tag{4.5}$$

Depending on the pH of the TMAH alkaline solution, the radicals either recombine, or result in the production of the hydroxide radical (OH^-), or production of the ozonide (O_3^-). For GaN, the Ga^{+3} is also produced, followed by deoxidation and dissolution. The chemical reactions for all previous hypotheses are summarized as follows[90];

$$4(CH_3)N^{+\cdot} + OH^{\cdot} \rightarrow C_4H_{13}NO \quad (4.6)$$

$$GaN + 3h^{+} \rightarrow Ga^{+3} + \frac{1}{2}N_2 \quad (4.7)$$

$$OH^{\cdot} + e \rightarrow OH^{-} \quad (4.8)$$

$$OH^{\cdot} + O_2 \rightarrow O_3^{-} + H^{+} \quad (4.9)$$

4.4.6.2.3 Modeling of morphology evolution of <10$\bar{1}$0> m-GaN sidewalls during TMAH wet etching

As previously mentioned, the atomic model of m-GaN morphology evolution in TMAH solution has been reported by Junlei He *et* al. [81]. According to the reported model, the reaction starts immediately when GaN's wafer is dived in the TMAH solution. The targeted areas by the hydroxide ions (OH^-) consist of the unprotected areas by the mask, the channel sidewalls, and the part on c-GaN damaged by the dry etching (the grooves at the base of channel sides). The reaction of Ga atoms with the hydroxide ions (OH^-) in those areas will lead to the Gallium Oxide (GaO_x) production; The resultant GaO_x is then dissolved in the TMAH solution [78]. The reaction will continue to be repeated until the edge of the mask. The N atoms at the edge of the mask will create a type of bonds with the mask, which will make it higher resistive to be etched by the OH^-. Finally, the surface is smoothed on the edge of the mask because most OH^- is being repelled by N atoms; therefore, the etching rate will be very low compared to the starting stage of etching. The reported model has been simplified, as depicted in Figure 42.

After several design experiments have been conducted, using TMAH 25%, at 85˚C, with UV-assisted source is the optimal recipe for our process. The Process to reveal the GaN crystallographic planes has been optimized using several III-N commonly used etchants such as Potassium Hydroxide (KOH), AZ400K developer, Sodium Hydroxide (NaOH), and TMAH. The detailed design of the experiment for all chemical etchant candidates will be detailed in the optimization chapter. Moreover, the etching selectivity for different masks used for channel definition step in TMAH such as SiO_2, SiN, SiN/SiO_2 sandwich, and the source metal has also been investigated. The overall GaN etching process details can be summarized as in Table 9.

Table 9:GaN etching process description using dry (ICP-RIE) and wet (TMAH) etching

Step	Details			comments
05.01	**GaN dry etching with ICP-RIE**			
	05.01.01	O_2 clean	5min	Descum removal
	05.01.02	Characterization	SEM	Check if the residual PMMA has been removed (repeat if needed)
	05.01.03	GaN etching using GaN LED recipe	2min	1st calibration sample
	05.01.04	BOE	5min	Dielectric mask removal
	05.01.05	profilometer	DEKTAK15O	Measure the GaN etched depth.
	05.01.06	GaN etching using GaN LED recipe	4min:25 sec	2nd calibration sample.The required time to etch 2.2µm depth
	05.01.07	BOE	5min	Dielectric mask removal (SiO2 etching rate is 200nm/Min
	05.01.08	profilometer	DEKTAK15O	Measure the GaN etched depth (last calibration)
	05.01.09	GaN etching using GaN LED recipe	4min:25 sec	Real GaN wafer
	05.01.10	Detaching the sample from the plate	Methanol followed by rinsing for 30 sec	Calibration for removing 10nm of PMMA
	05.01.11	Characterization after Dry etching	Keyence and SEM	To check if we have the lift-off profile
05.02	**Annealing**			
	05.02.01	Annealing using Contact recipe	RTA, 420°C,10min	To relax the source metal and to ensure the ohmic contact
	05.02.02	Characterization	SEM	
05.03	**GaN wet etching**			
	05.03.01	Solution stabilization on the hot plate	80-85°C	Checking the temperature of the water until having 80-85°C
	05.03.02	TMAH 25%	60-80ml on a pyrex beaker to be added to the dish of hot water	Wait for 10 min for temperature stabilization of TMAH solution
	05.03.03	Sample deoxidation	Diluted HCL10%, 1min then distilled water for 15s	The wafer should be on a holder to transfer it directly to the TMAH
	05.03.04	GaN wet etching	5 min step	The etching step is 5 Min
	05.03.05	Characterization	SEM	Characterizing an exact device chosen after dry-etching
	05.03.06	Sample deoxidation	Diluted HCL10%, 1min then distilled water for 15s	The wafer should be on a holder to transfer it directly to the TMAH
	05.03.07	GaN wet etching	5 min step	The etching step is 5 Min
	05.03.08	Characterization	SEM	Characterizing an exact device chosen after dry-etching.
	05.03.06	Sample deoxidation	Diluted HCL10%, 1min then distilled water for 15s	The wafer should be on a holder to transfer it directly to the TMAH
	05.03.07	GaN wet etching	Time varies	The etching step depends on the SEM characterization step
	05.03.08	Characterization	SEM	Characterizing an exact device chosen after dry-etching. Still repeated until having straight, smoothed fingers with undercut profile.

It is worth mentioning that, after the 2nd etching step (after 10 min of wet etching), the time required to finalize the smoothing and undercut profile creation process will be adopted according to the residual damage parts. The deoxidation step is also necessary before each wet etching step. Explicit, GaO_x product resulting from the TMAH reaction with GaN will prevent further etching by covering the etching area. The GaN material will be explored again in the TMAH solution after removing such passivation layer. TMAH solution requires agitation for 10 min at room temperature to ensure that all TMAH is dissolved in the water. This step will maintain the same concentration for all etching steps since the etching rate is directly proportional to the TMAH solution. Since the GaN wet etching with TMAH etchant is crystallographic, the importance of the Orientation determination step appears here where the m-GaN and a-GaN sidewalls can be revealed easily without having adjacent prisms on FIN sidewalls. Up to this moment, the fabrication process could be described as in Figure 43

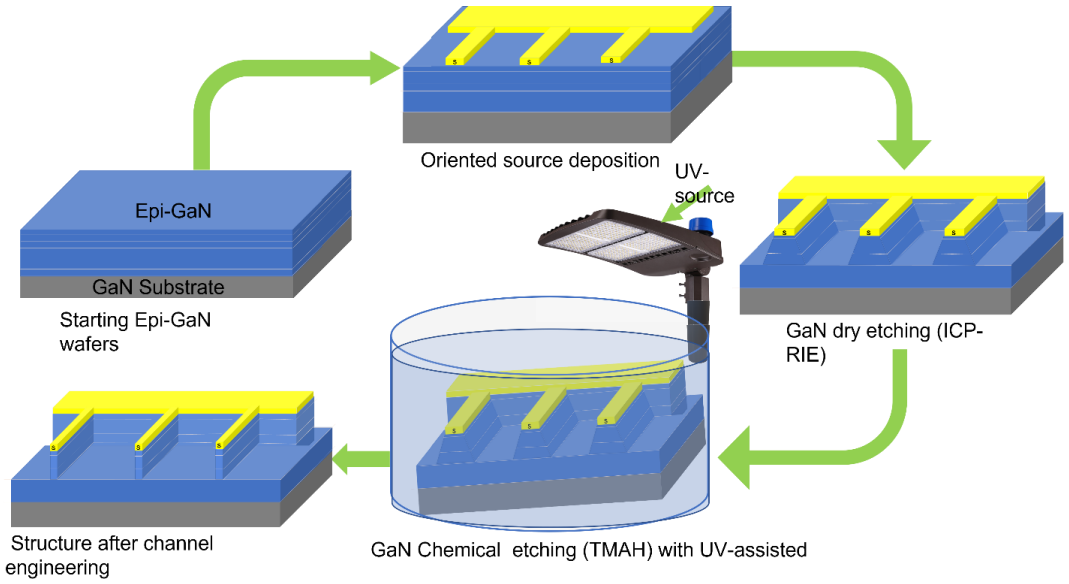

Figure 43: Vertical GaN FinFET processing models before oxide deposition

4.4.7 Gate Oxide Deposition (Al_2O_3):

Once the GaN etching process has been carried out, the wafer is ready to deposit the gate oxide material. For high-conformality deposition, the atomic layer deposition process has been chosen to deposit up to 30 nm of Al_2O_3 thin film everywhere on the wafer's surface to isolate the Gate from the source and the FIN channel. Atomic layer deposition (ALD) is a low-temperature atomic chemical vapor deposition technique, produces thin films from different materials. ALD offers outstanding conformality on high aspect ratio structures, thickness controllability

on the Angstrom scale, and tunable film composition through sequential, self-limiting reactions[91].

The ALD process begins when two reactions are exposed sequentially to a substrate, A and B, without overlap. Contrary to other techniques, such as chemical vapor deposition (CVD), where thin-film growth proceeds steadily, ALD involves reactants reacting with the surface in a self-limited manner: the reaction molecules can interact with a finite number of sites on the surface. After the sites in the reactor have been consumed, the growth stops. The remaining reactant molecules must be flushed out, and only then can reactant B be added[85]. They are exposed alternately to A and B until a thin film of C is formed.

Accordingly, when describing an ALD process, both the dose times (the time a surface is exposed to a precursor) and the purge times (the time it takes between doses for the precursor to evacuate the chamber) should be considered. The dose-purge-dose-purge sequence constitutes an ALD cycle as part of a binary ALD process. Furthermore, this process is described by its growth per cycle [92]. The ALD process to deposit Al_2O_3 films has been illustrated in Figure 44.

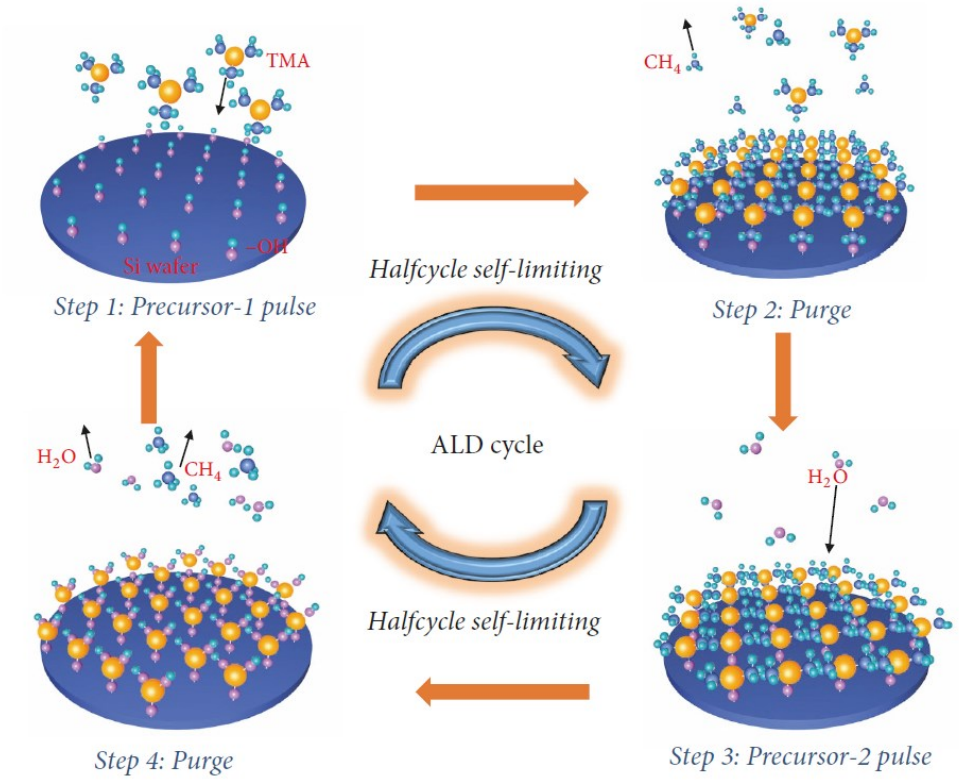

Figure 44: Vertical GaN FinFET processing models before oxide deposition

The schematic of the ALD machine and the Picosun - R-200 Advanced ALD available in LN2-3iT are shown in Figure 45(a) and 45(b), respectively.

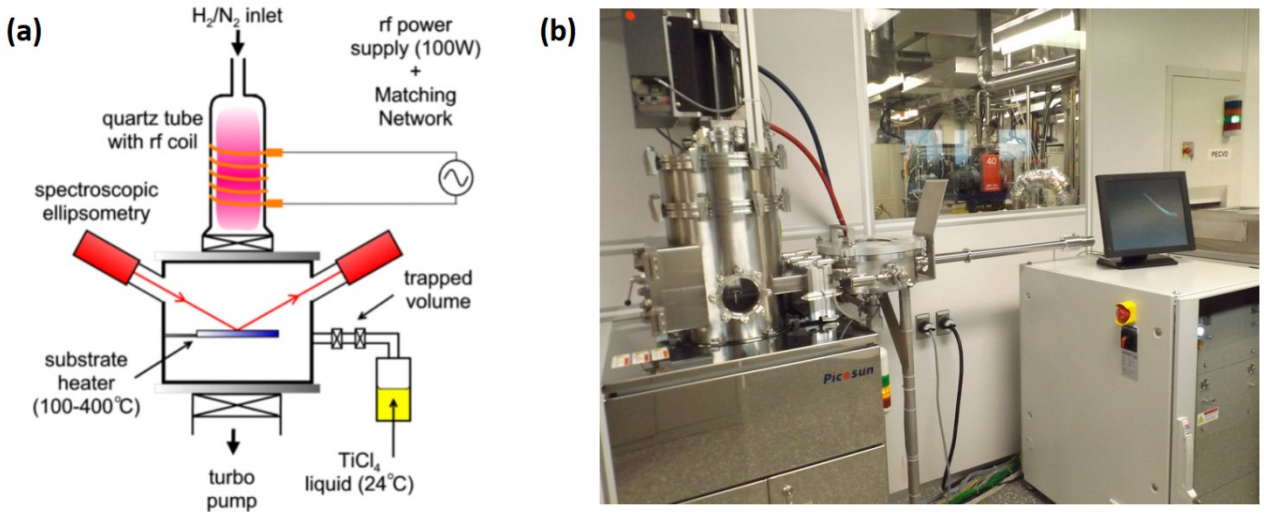

Figure 45: a) ALD system schematic [89] .b) Picosun - R-200 Advanced ALD available in LN2-3iT.

For the ALD process step, a service demand shall be de arranged, and the staff in the cleanroom will carry it out.

4.4.8 Al_2O_3 opening process

Since the Al_2O_3 layer will be deposited everywhere on the wafer surface, we will no longer have access to the source pads for probe connection at the characterization stage. Therefore, an Al_2O_3 opening mask has been designed to etch the $Al_2O_{3\ deposited}$ on the source pad. The process starts with photolithography to protect the Al_2O_3 layer on the whole sample except on the source pads. The wafer will then be developed to remove the exposed positive resist. Finally, the wafer is stuck on the plate using the crystal bonding polymer, and then the ICP-RIE will etch the exposed Al_2O_3 places. Once the Al_2O_3 etching is finished, the ordinary cleaning procedure will be performed, including inserting the wafer into the O_2 plasma line for 10 min at 150W power and 300mTorr pressure. This step will etch the burned resist surface by plasma during the Al_2O_3 etching. After that, the wafer is immersed into the remover for 1hour, Acetone for 5minutes, IPA for 5minutes, rinsing for 30 sec, and O_2 plasma line for 10 min at 150W power and 300mTorr pressure. Finally, the wafer shall be characterized using the optical microscope and SEM to ensure that the Al_2O_3 is removed from the surface of the source pads. The detailed process for such a step has been tabulated in Table 10.

Table 10:Al_2O_3 opening process steps description

Step	Details			comments
07.01	**Lithography**			**Check the resist thickness**
	07.01.01	Dehydratation	150°C / 5min	
	07.01.02	MCC Primer	4000rpm / 60s	4000rpm_60s_500 on Brewer
	07.01.03	AZ9245	4000 rpm / 60s	4000rpm_60s_500 on Brewer
	07.01.04	Soft bake	110°C / 2min	Check the temperature with the thermocouple
	07.01.05	Photolithography UV AOI 806	200mJ.cm-2 / N2 hard contact (20mA) / Al_2O_3 layer	Check the power of the lamp
	07.01.06	Developping AZ400K (1:4)	1min30s+1min30s	
	07.01.07	DI Water / Drying	30s / N2	
	07.01.08	Characterization	Optical microscope / Profilometer	Take a photo of alignment marks on the middle of the sample and at the corner
07.02	**Al_2O_3 etching in III-V**			
	07.02.01	Etching using BCl_3 recipe	2min	Calibration sample with Al_2O_3 patterns on Si
	07.02.02	profilometer	Dektak 150	Measuring the Al_2O_3 etched depth
	07.02.02	Etching using BCl_3 recipe	The time required to etch 30nm of Al_2O_3	shall be calibrated
07.03	**Cleaning**			
	07.03.01	Plasma O_2	150W / 300mT / 10min	Calibration for removing 500nm of AZ9245
	07.03.02	Remover 1165	1 hour/70°C	
	07.03.03	Acetone	30min	
	07.03.04	IPA	10min	
	07.03.05	Plasma O2	(150W / 300mT / 10min) x3	
	07.03.06	Characterization	Optical microscope/SEM	

4.4.9 Gate Metallization process

For the gate metallization step, two depositions scenarios have been optimized for such purpose; Firstly, the Gate metal could be metalized using the electroplating deposition. The Gate deposition by evaporation will be the second choice. Electroplating deposition is Electroplating is coating a conducting surface with metal. During the process, the surface that is to be coated acts as the cathode, and the metal that is to cover it serves as the anode in an electrolytic cell; A salt solution of the metal to be coated is used as the electrolyte, while the anode (positive electrode) is usually either a block of that metal or some other kind of inert material. An external power supply provides the current[93]. The schematic of the electroplating process is shown in Figure 46

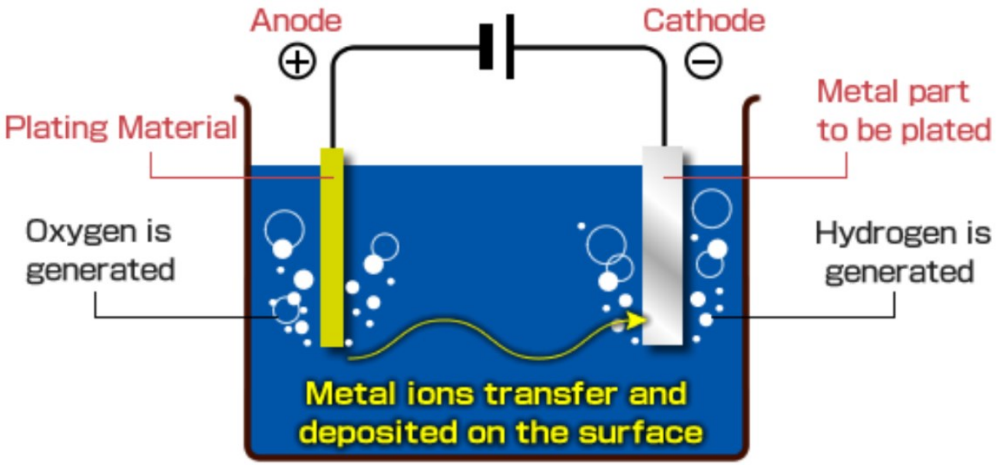

Figure 46:a) ALD system schematic [89] .b) Picosun - R-200 Advanced ALD available in LN2-3iT

The seed layer will be metalized by evaporation with rotation and angle to create the shadowing region using the undercut profile. Accordingly, a new mask has been designed to open the areas where the gate metals will be deposited. The UV-lithography will be used for the gate patterning process. Before the electroplating, the wafer should be deoxidated again using the HCL: H_2O with 1:10 dilution to remove any oxidated part from the surface of the seed layer. The seed layer stack composite has chosen Ti/Au/Ni with (20nm/200nm/20nm) thicknesses, respectively. Since the desired gate metal will be gold, The ELEVATE GOLD 7990 ST2 solution will be used in our process. The challenges related to this processing step is to find the best setup for the wafer to avoid deviation in deposited metal thickness. Explicit, when the wafer is attached to the cathode side from only one edge, the resistance of the Seed layer increases for the areas far away from the tweezer side, a deviation in current density attracting the Au ions will be resulted and leading to deviation in the deposited film thickness. The second challenge to optimize the electroplating process is to investigate the optimum current density value leading to the best deposition profile. Finally, the small area of the wafer (1cmx1cm) concerning the anode area will make it difficult for the electric field to be uniform for all parts of the wafer. All those challenges have been treated in the optimization chapter following this chapter.

On the other hand, since we are performing DC characterization for the device, the value of C_{GS} will be negligible. This motivates us to choose the 2nd scenario for the gate metallization by evaporation process directly after the Al_2O_3 opening with rotation and angle options. The two scenarios have been optimized for the real device

fabrication process. The detailed description of the sample preparation for the electroplating process has been tabulated in Table 11.

Table 11:Sample preparation for the electroplating process

Step	Details			Comments
08.01	**Oxide deposition**			
	08.01.02	Oxide deposition	PECVD	Deposition of 1µm of SiO2 film
08.02	**Lithography for SiO_2 etching**			**Check the resist thickness**
	08.01.01	Dehydratation	150°C / 5min	
	08.02.02	MCC Primer	4000rpm / 60s	4000rpm_60s_500 on Brewer
	08.02.03	AZ1518	4000 rpm / 60s	4000rpm_60s_500 on Brewer
	08.02.04	Soft bake	117°C / 1min	Check the temperature with the thermocouple
	08.02.05	Photolithography UV AOI 806	130mJ.cm^{-2} / N_2 hard contact (20mA) / GM layer	Check the power of the lamp
	08.02.06	Developping AZ400K (1:4)	1min30s+1min30s	
	08.02.07	DI Water / Drying	30s / N2	
	08.02.08	Characterization	Optical microscope / Profilometer	
08.03	**SiO_2 etching (Advance Oxide Etching)**			
	08.03.01	SiO_2 etching	for 2 min	Calibration sample with SiO_2film on Si
	08.03.02	ellipsometer	Alpha-SE	Measuring the SiO2 etching rate
	08.03.03	SiO_2 etching	Required time to etch the SiO2 from the gate areas	
08.04	**Cleaning**			
	08.04.01	Plasma O_2	150W / 300mT / 10min	removing 500nm of AZ1518
	08.04.02	Remover 1165	1 hour/70°C	
	08.04.03	Acetone	30min	
	08.04.04	IPA	10min	
	08.04.05	Plasma O2	(150W / 300mT / 10min)x3	
	08.05.06	Characterization	Optical microscope/SEM	
08.05	**Electroplating**			
	08.05.01	Deoxidation using HCL: H_2O (1:10)	1min	
	08.05.02	Electroplating	3.8mA/Cm^2, 55°C, 2 min	The etching rate is 380nm/Min
	08.05.03	Characterization	Optical microscope and SEM	

4.4.10 The interconnection step (IN)

This step involves increasing the metal thickness on the opening contact areas to make it easier to connect with the probes during device characterization. The metal used for interconnection shall meet the following properties:

✓ Low Resistance: Since the metal circuit needs to pass current, its metal should have low resistance.

✓Thermochemical stability: The metal material properties must remain unchanged during the metal interconnection process.

✓High Reliability: With the development of integrated circuit technology, even a small amount of metal interconnect materials must have sufficient durability.

✓ Manufacturing Cost: Even if the three conditions above have been met, high cost is not suitable for mass production.

The IN mask will be used with lift-off lithography (UV and DUV) to deposit the metal by evaporation. The process involves spinning 2PMMA layers followed by AZ1505 Photoresist; The UV lithography will then be done to pattern the AZ1505 using Aligner OAI 806 (70mJ/cm^2). After developing the exposed AZ1505 using MF-319 (30S:30S: H_2O) followed by N_2 Drying. The DUV will then be performed to pattern the lower PMMA layers using (2500mJ/ cm^2) dose. Chlorobenzene developer is then used for (1Min, followed by rinsing in H_2O and N_2 drying. Plasma line 3Min,50W is then performed to remove 150nm of PMMA (calibration with PMMA/ SI sample). The deoxidation is then done as usually with HCL: H_2O with 1:10 dilution. Finally, the metal will be deposited by evaporation. The procedure of the source lift-off is then followed to remove the PMMA.

4.4.11 Device Passivation (SiN)

The passivation step is used for two main reasons. The first is to isolate the Gate from the source to avoid current leakage generation between contacts. The second reason is to protect the device from damage, especially when further steps after the passivation. For our process, the SiN dielectric is used for the passivation process, and it will be deposited using the Plasma Enhanced Chemical Vapor Deposition (PECVD) machine. For such fabrication step, a service demand is usually made, and the cleanroom staff does the service.

4.4.12 Drain deposition (Drain)

The drain deposition is the last step in our fabrication process. The drain will be deposited on the backside of the wafer by evaporation deposition. The device is then will be ready for characterization tests.

4.4.13 contact opening (CO)

This step involves the etching of the SiN dielectric above our device contacts. A specific mask has been designed for that purpose, and the process will be done by UV-Lithography followed by oxide etching in ICP-RIE machine (AOE). The steps for contact opening are the same as the oxide etching process before electroplating (Table 11, step 08.02 to 08.04) with SiO_2 replacement by SiN and the CO mask instead of the GM mask for the patterning.

4.5 conclusion

The fabrication process modules have been described in detail in this chapter; each module's objective, challenges, and detailed processing steps have been explained before the optimization is started. The next chapter will detail all optimization tests and design of experiments for the critical processing modules such as the source deposition, GaN etching process, Gate metallization by electroplating, and the orientation determination procedure.

CHAPTER FIVE: CHARACTERIZATION OF M-GAN AND A-GAN CRYSTALLOGRAPHIC PLANES AFTER BEING CHEMICALLY ETCHED IN TMAH SOLUTION

5.1 Document descriptions

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Paper contribution: this paper investigates the revealing of m-GaN and a-GaN crystallographic planes when chemically etched with TMAH solution. It is also illustrated a novel procedure to identify the exact flat zone of a coupon sample diced from a GaN wafer with 1˚degree resolution. The new procedure is necessary to engineer the GaN sidewalls engineering after it is etched with (ICP-RIE).

5.2 Abstract:

This paper proposes a new technique to engineer the Fin channel in vertical GaN FinFET toward a straight and smooth channel sidewall. Consequently, the GaN wet etching in the TMAH solution is detailed; we found that the m-GaN plane has lower surface roughness than crystallographic planes with other orientations, including the a-GaN plane. The grooves and slope (Cuboids) at the channel base are also investigated. The agitation does not assist in Cuboid removal or crystallographic planes etching rate enhancement. Finally, the impact of UV light on m and a-GaN crystal plane etching rates in TMAH has been studied with and without UV light. Accordingly, it is found that the m-GaN plane etching rate is enhanced from 0.69 to 1.09 nm/min with UV light; in the case of a-GaN plane etching, UV light enhances the etching rate from 2.94 to 4.69 nm/min.

5.3 Introduction

As a wide-bandgap transistor technology, GaN provides a compelling opportunity to achieve unprecedented performance and efficiency in power electronics systems, owing to its large breakdown electric field and high Baliga's Figure of merit [1–4]. It guarantees a 10% reduction of losses in power conversion circuits [2]. Further, it also offers faster, cooler, and smaller power devices than its silicon counterparts [6,7].

Thus far, both lateral and vertical structures have been considered to be incorporated in the GaN power devices [99]. The GaN-based high electron mobility transistor (HEMT) device's immense potential comes from the high density, the high electron mobility in the 2-dimensional electron gas (2DEG) formed at its heterostructure [100]. However, with the high electric field close to the device surface, the high current density along the 2D channel generates significant heat, increasing the device access resistance and incidences of current collapse due to traps [10,11]. Contrariwise, the vertical GaN power devices, especially the GaN FinFET, have garnered considerable attention because of their potential to reach high voltage and high output current density [12,13]. Furthermore, they exhibit superior thermal performance compared to lateral devices [40]. The first design and fabrication of a Normally-Off GaN vertical fin power FET (or MOSVFET) have been reported by W. Li et al. [46]. They first used a TCAD tool to investigate the impact of the main critical parameters on the device performance, such as the bulk GaN mobility, the gate-to-gate distance, and the gate length. They achieved an ON-state resistance (R_{ON}) of 2.8

$m\Omega \cdot cm^2$ and a breakdown voltage (V_{BR}) of 1.2 kV. Several prototype versions of GaN FinFET devices fabricated on GaN or a foreign substrate have been published in the literature [16–18].

The vertical GaN FinFET fabrication process begins with the anisotropic GaN etching, executed by dry Induced Coupled Plasma-Reactive Ion Etching (ICP-RIE) [104]. However, the main drawback of such technology is the GaN sidewall surface's damage with difficulty in obtaining straight etched sidewalls [105]. Engineering the Fin channel sidewalls plays a crucial role in the electrical performance of vertical GaN FinFET devices [106]. Therefore, it is vital to optimize a smoothing process after dry etching to remove the channel sidewalls imperfections and the GaN/dielectric interface of the device is therefore improved.

For vertical GaN FinFET devices, a Fin channel structure with non-polar plane side walls is favorable for Normally-Off operation. Non-polar planes at the FinFET channel's sidewall are suitable for fabricating the Normally-Off device. Depending on the channel width, a low quantity of charge can be present in the channel at V_{GS} = 0 V [22,23]. The m-GaN and a-GaN channel sidewalls revealing process require a specific lithography orientation of the Fin channel structure [67]. The chemical etching process has also been demonstrated in the literature for post dry etching treatment of GaN [25–28].To achieve this, Tetramethylammonium hydroxide (TMAH) is widely used [29,30]. Furthermore, UV light-based TMAH etching is also effective technique to enhance the GaN sidewall's etching rate [74]. It also improves the etching selectivity when a dielectric material is used as a mask [32,33].Since GaN chemical etching is a crystallographic-dependent process, the Fins sidewalls should be precisely aligned to the crystal plane that we would like to reveal after etching. Therefore, for GaN coupons processing, developing a sensitive orientation determination procedure is an essential step.

The purpose of this paper is to investigate one of the most critical steps in the fabrication process of vertical GaN FinFET transistors, which is the etching of the channel sidewalls. An Orientation Determination (OD) technique has also been demonstrated for GaN Fin channel sidewall. Finally, this work presents a procedure to improve the GaN transistor fabrication process and therefore the performance of the device.

5.4 Experiment Technique

This study intends to determine the exact orientation of the a-GaN and m-GaN planes on the coupon samples, followed by investigating the GaN crystallographic etching with TMAH solution. The GaN channel fingers are firstly fabricated using the top-down process. The wet etching has been used to reveal the crystallographic planes on the channel sidewalls. The fabrication process is depicted in Figure 47. A 7 µm thick GaN epi-layer wafer (Sample1) grown by Metal-Organic Chemical Vapor Deposition (MOCVD) on Sapphire substrate is used for this experiment. The size of this square sample is 1 cm × 1 cm. For this purpose, 180 fingers with 15 × 2 μm^2 dimensions oriented from 0° to 180° with a step of 1° are fabricated (Figure 47 and Figure 48).

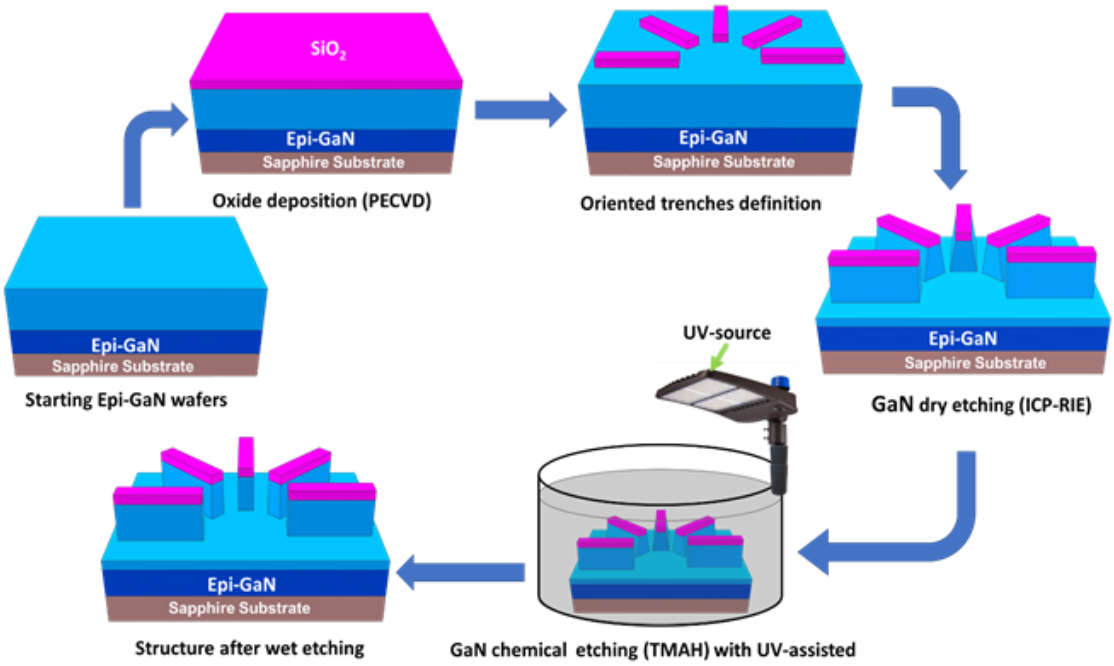

Figure 47:The fabrication process of GaN's fingers for sidewalls engineering.

The fabrication process starts with depositing a 1 µm thick SiO_2 (PECVD) layer on the wafer to act as a mask. An e-beam lithography is then performed with PMMA 9% resist for finger definition. The SiO_2 is etched using dry etching with CF4/He gas mixture to transfer the pattern from the resist to the SiO2 mask. This step is followed by the ICP-RIE using Cl2/Ar gas mixture for etching a 2 µm of GaN for the Fins formation and, finally, the GaN wet etching is performed using TMAH solution. For this last point, the recipe mainly consists of TMAH 25% heated in glassware for (80–85 °C) temperature range with UV-assisted source. It is worth mentioning that GaN wafers de-

oxidation using (1:10) diluted HCl solution before any TMAH wet etching step is very important because it will prepare the GaN surface for the etching process [107].The Scanning Electron Microscope (SEM) characterization for the m-GaN oriented finger is shown in Figure 48.

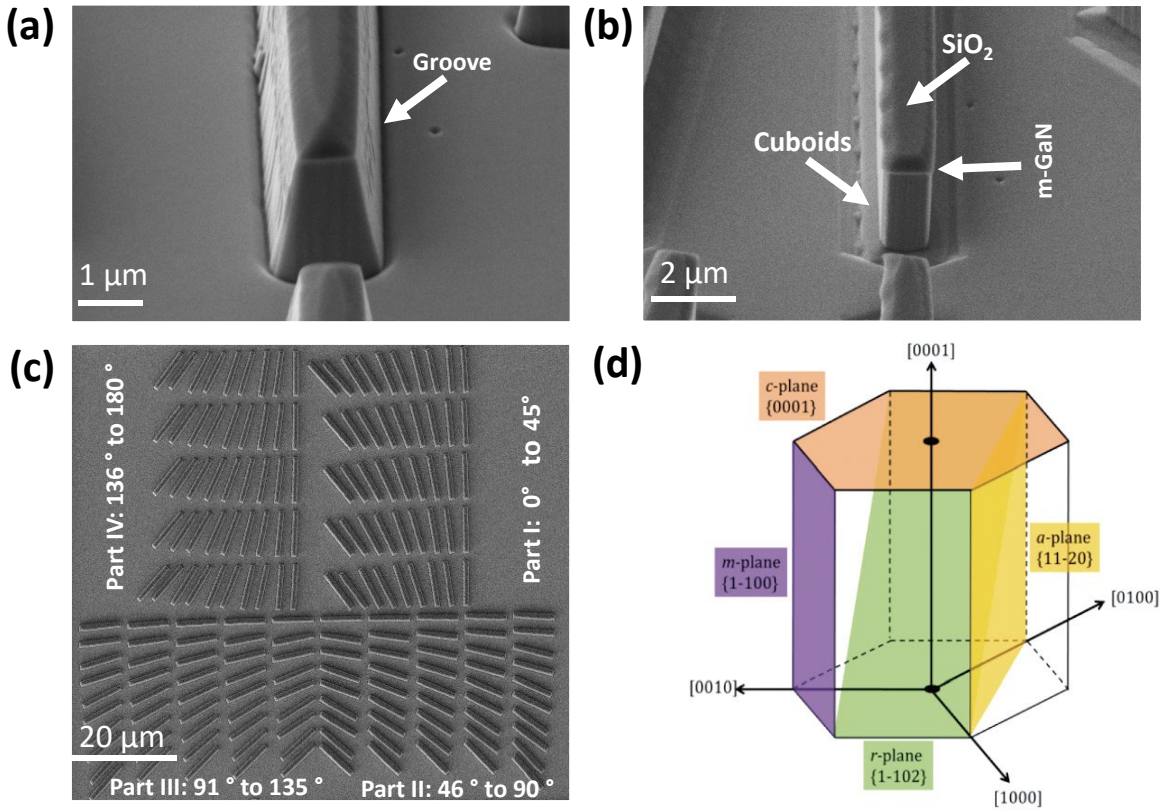

Figure 48:SEM images of fingers after GaN etching;(a) bird eye view of finger after dry etching; (b) bird eye view of finger after wet etching with TMAH solution; (c) top view of an ensemble of fingers for orientation between 0° and 180°; (d) GaN crystallographic planes [76].

The finger shape after ICP-RIE dry etching is shown in Figure 48(a), while the shape of the same finger after chemical etching is presented in Figure 48(b). Figure 48(c) presents an ensemble of fingers after ICP-RIE. The GaN crystallographic planes are shown in Figure 48(d).

Following the previous experiments, another sample (Sample2) grown on GaN substrate was also processed. Indeed, a coupon having the same epitaxial layers as Sample1 has been processed. In this coupon, the SiO_2 mask for the GaN etching is replaced by the Ti/Au/Ni metal stack with 20 nm/350 nm/30 nm thicknesses, respectively, deposited by the e-beam evaporation. The studied patterns have a star shape consisting of 24 identical Fins fingers with 250 nm width and 2.3 µm thickness shifted from each other with 15°. The same fabrication process depicted

in Figure 47 has been used to fabricate the Fins fingers, except for the mask, which is metallic here in this second experiment. The vertical fingers of the star pattern were aligned on the m-GaN plane. The m-GaN and a-GaN crystal planes are investigated during the etching with TMAH.

The fabrication procedure shown in Figure 47 has been associated with some challenges and limitations. For instance, optimizing e-beam lithography, initialization of the GaN surface before the TMAH etching, or selecting a source metal stack compatible with all fabrication steps are just a few of them. Indeed, several tests have been performed to determine the metal stack suitable for the device fabrication process. Likewise, the selected metal stack should present no contamination for the PECVD, ALD, and ICP-RIE machines. Finally, Cr/Au/Cr metal stack has been considered most viable for fabricating the real device. This metal stack will be used for the fabrication of GaN vertical devices.

5.5 Results and Discussion

The results and discussion section are divided into three main parts. Firstly, SEM has been used to characterize the fabricated structures after wet etching. In the second part, both Atomic Force Microscopy (AFM) and SEM are then used to investigate the groove's etching profile. Finally, the fabrication of vertical GaN channel fingers using the proposed orientation determination has been characterized and discussed.

5.5.1 GaN Channel Sidewalls Etching Using the Proposed OD Procedure

Sample1 has been dived in TMAH solution for different etching time intervals with a total of 30 min etching time. The channel fingers have been characterized after each etching step to track the sidewall morphology evolution. The six m-GaN's crystal planes and six a-GaN crystal planes (a-GaN planes and m-GaN planes are perpendiculars) are investigated. In the case of GaN on the sapphire wafer, the flat zone is pre-aligned to the a-GaN plane; therefore, m-GaN planes are located approximatively perpendicularly to the flat. In our fabricated structure, the range of investigated angles was between 0° and 180° with a step of 1°. Therefore, we have investigated all m-GaN and a-GaN planes with ±1°degree precision to estimate the exact GaN crystal orientation. The channel fingers oriented on m-GaN and a-GaN planes have been characterized using SEM after 30 min of chemical etching in TMAH solution, as shown in Figure 49

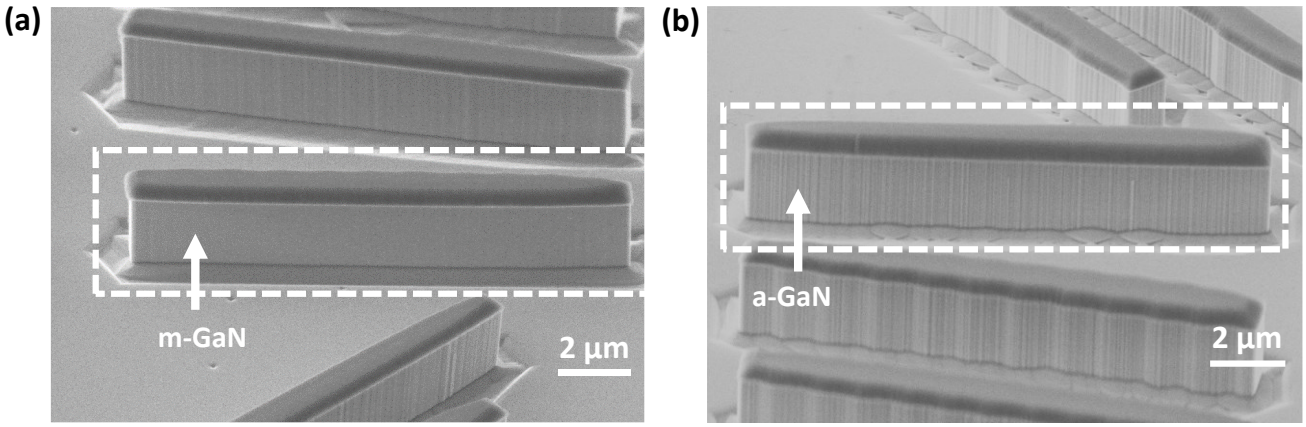

Figure 49:SEM images for m-GaN and a-GaN sidewalls after 30 min in TMAH solution; (a) m-GaN sidewall; (b) a-GaN sidewall.

It can be easily observed from Figure 49(a) that the m-GaN plane surrounded by the dashed rectangle has relatively much lower roughness on its surface compared to the a-GaN plane, which is presented in Figure 49(b) surrounded by the dashed rectangle. After 10 min of wet etching, the a-GaN plane sidewalls are completely vertical. No further smoothening occurs after that. The relatively higher etching rate of the a-GaN plane results from its lower etching resistivity. On the other hand, a 25 min wet etching process is needed to achieve vertical m-GaN fingers, owing to its higher etching resistivity [79]. In light of this, m-GaN orientated Fins is the best choice for fabricating a high-performance vertical FinFET GaN transistor. Noteworthy is the fact that TMAH solution parameters do not solely determine the etching rate of GaN; rather, it is determined by a variety of factors, such as the mask selection [108], the doping level [109], and the crystalline quality resulting from GaN epitaxial growth conditions [71].

5.5.2 Investigation of the Morphology of the Groove Surrounding the Fins after TMAH Etching

It is well known that after the plasma etching, an over-etch appears at the periphery of the patterns (trenching effect) [36]. In our case here, this over-etch creates a groove at the bottom of the Fins. The grooves evolution in both finger sides has been investigated before and after chemical etching. The groove depth was about 94 nm before wet etching. GaN wet etching has been carried out in TMAH for around 120 min in several steps using the same etching recipe. The c-plane is ultimately stable in TMAH solution with only around 2 nm etching depth after 120 min of chemical etching. This 2 nm results from several de-oxidation of GaN surface before TMAH etching between

two etching times. Those results are in good agreement with the one obtained by B. Leung et al. and E. Schubert et al., respectively [35,36].

The Cuboid structure characterized by the slope α as in Figure 50(b) was also investigated. This slope located at the finger base appeared in all our experiments. This structure has also been widely addressed in the literature, as in [37–39]. A clear, convincing explanation of the origin of these Cuboids has not been reported yet. Accordingly, one of the reported explanations declaring that the semipolar r crystal plane <1$\bar{1}$01> could represent the slope an of the Cuboid. The slope angle of the cuboids in our case is 68° after the wet etching. This value is different from the r plane, which is 58°[40].

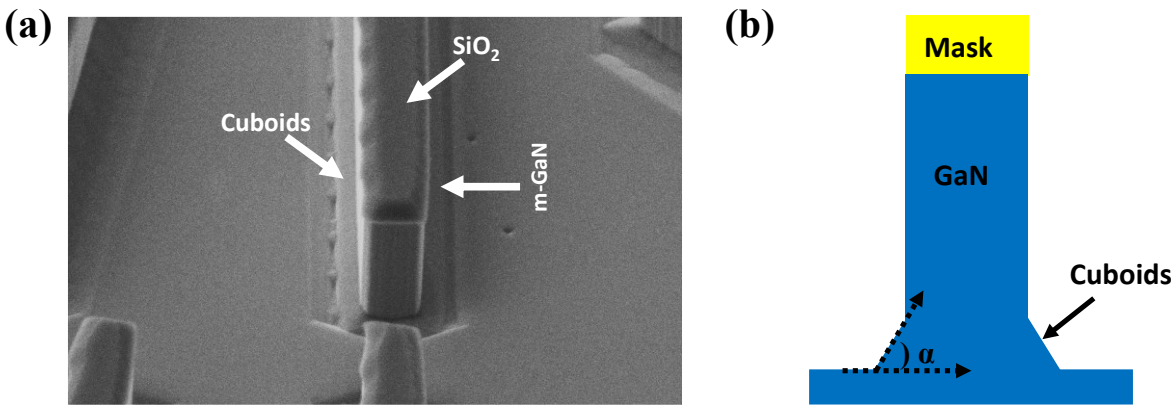

Figure 50:Groove formation due to the GaN etching; (a) This work; (b) description of cuboid formation.

Fatahilah, M.F. et al. have reported another explanation.[73]. According to their observation, the slope is created due to TMAH hydrodynamics flow during the GaN chemical etching. To validate this assumption, we have used two GaN on sapphire substrate samples with dry-etched GaN fingers fabricated using the same process as in Figure 47. Indeed, using the TMAH etching recipe described above, both samples are etched for 25 min, one with agitation and the other without. The TMAH hydrodynamics flow is different for these two samples. After etching, the slopes α observed at the bottom of the fingers are identical on both samples. Furthermore, the Cuboids slope is not depending on the distance between the two neighbor fingers. Thus, the origin of the Cuboids created at the Fins GaN sidewall base after TMAH etching is still not elucidated and needs to be more investigated.

On the other hand, the impact of UV-light on Cuboids etching has also been investigated by diving two GaN on GaN wafers for 30 min in a TMAH solution, one with and one without UV assistance. The Fin patterns from both wafers have been observed before and after etching using the SEM. It is found that the cuboid shape is the same for both samples, which is proof that the UV light is not impacting the cuboid formation.

5.5.3 GaN Non-Polar Planes Wet Etching Rate Estimation in TMAH Solution with and without UV Source Utilization

Using the top-down approach, the proposed OD technique has been used to determine exactly m-GaN oriented vertical GaN channel fingers. The used wafer is a thick GaN grown layer on GaN substrate with 1cm × 1cm dimensions. This sample comes from a 2 inches wafer where the flat zone is aligned to the GaN's m-plane. The processing of this sample started with a pre-alignment step where a pattern comparable to the one presented in Figure 48(c) is placed at the sample's periphery. All these patterns are etched to reveal the exact m-plane. As in our case, where we usually work on coupons, this pre-alignment procedure is very useful for the GaN-on-GaN wafers since the exact in-plane crystal orientation is not well identified. The m-plane is not precisely defined in these coupons since they are diced from a 2-inch wafer. The proposed approach is a simple solution that can be adopted in the device fabrication process to eliminate any miss-alignment of the Fins.

Since the crystal planes can all be identified with a precision of one degree, the sample can now be processed. The e-beam lithography is used to align the Fins finger to the m-plane revealed on the pre-alignment marks. This sample uses the same metal stack previously used to mask the GaN etching to define the Fins. After metal deposition and GaN dry etching, the patterns are ready for the channel sidewall etching step. To determine how UV light will affect the etching rate for both a-GaN and m-GaN planes, A pair of samples was prepared and then chemically etched in TMAH solution at different time intervals: one was etched using the standard process using UV-light, while the other was etched without UV-light. The lateral etching depth was then measured after each time interval. Figure 51 illustrates the plot of m-GaN and a-GaN etching rates with and without UV-light.

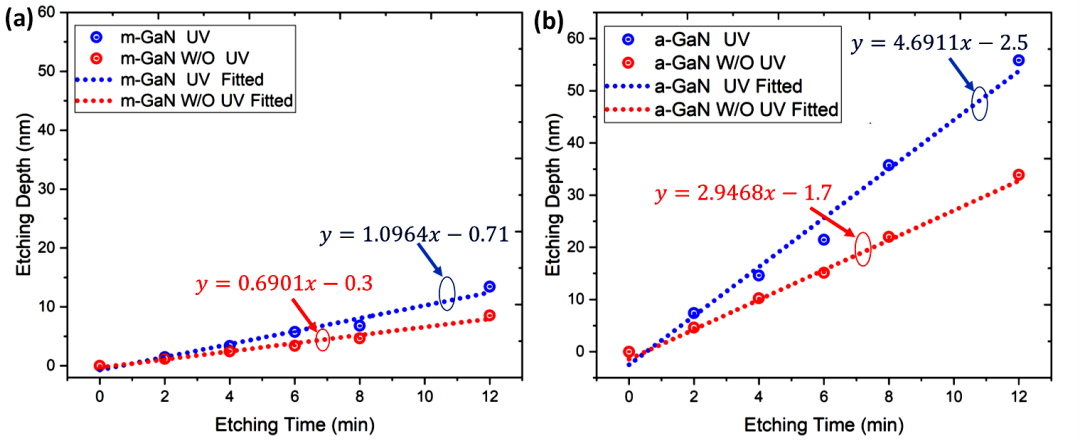

Figure 51:m-GaN and a-GaN wet etching rate in TMAH solution with and without UV-source. (a) for m-GaN plane, (b) for a-GaN plane.

It is observable from Figure 51 that the m-GaN etching rate is enhanced from 0.69 to 1.1 nm/min by using UV light. Moreover, in the case of a-GaN etching rate, UV light enhances the etching rate from 2.95 to 4.69 nm/min. After revealing the GaN crystallographic planes, the etching rate will be affected by the etching resistivity of each plane. We have plotted the etching depth for both a-GaN and m-GaN planes during the wet etching using the SEM measurements for etching durations ranging from 2 to 12 min. In Table 12, we present the obtained results and compare them to those reported in the literature.

Table 12:GaN crystallographic etching rate (β) of m-GaN and a-GaN planes in TMAH for different wet etching setups.

Ref	Authors	Wafer/Substrate	GaN Wet Etching Recipe	UV Light	Etch Time (min)	Mask	β	
							m-GaN (nm/min)	a-GaN (nm/min)
1	This work	GaN/GaN	TMAH, 25%, 85 °C	Yes	14	Ti/Au/Ni	1.09	4.69
2	This work	GaN/GaN	TMAH, 25%, 85 °C	No	14	Ti/Au/Ni	0.69	2.95
3	B. Leung et al. [79]	GaN/GaN	TMAH, 25%, 80 °C	No	52	SiO_2	0.13	0.16
4	F. Horikiri et. al.[41]	GaN/GaN	TMAH, 25%, 85 °C	Yes	30	SiO_2	0.1-2	---

As shown in Figure 52, sample2 has a star-shaped pattern with 24 identical GaN fingers with 250 nm width and 2.3 µm thickness separated by 15° angles. These GaN fingers were characterized after 30 min of wet etching in TMAH solution.

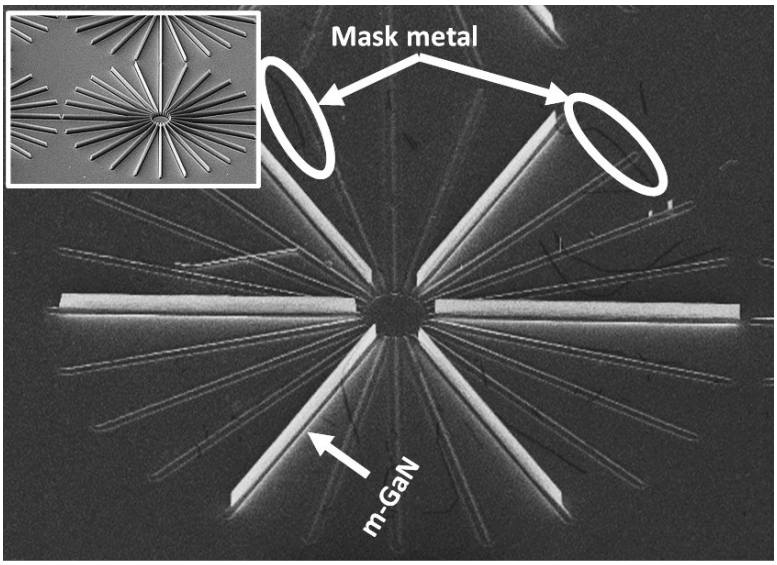

Figure 52. Star shape pattern after 30 min TMAH etching (insert: picture of the same pattern before TMAH etching).

Figure 52 clearly shows that only m-GaN oriented fingers remain after 30 min TMAH etching. Meanwhile, all the other Fins have been etched. This experiment highlights that the GaN m-plane is less etched in TMAH solution than other GaN crystallographic planes [76].

5.6 Conclusions

This work proposes an orientation determination procedure for crystallographic wet etching of a-GaN and m-GaN planes. This pre-alignment procedure is very helpful for the GaN wafers where the exact in-plane crystal orientation is not well identified as for diced coupons. By using the proposed procedure, the m and a-GaN planes are precisely identified. An optimized TMAH 25%, 85 °C, and UV-assisted recipe has been used to engineer both a-and m-GaN oriented Fin channels. The etching of the m-GaN crystal plane reveals smoother and more stable channel sidewalls than those on a-GaN oriented Fins. The Cuboids at the bottom of the GaN fingers are also investigated. Several tests have been performed and still need more investigation to deeply understand the origin of these Cuboids created during the TMAH etching. The impact of UV-light utilization on m and a-GaN planes etching rates in TMAH solution has been investigated. The m-GaN etching rate is enhanced from 0.69 to 1.09 nm/min with UV-light utilization. In the a-GaN plane, the UV-light enhances the etching rate from 2.94 to 4.69 nm/min. Finally, the obtained results in this work are innovative. They will offer more knowledge about a- and m-GaN planes etching mechanisms, a key step in the vertical GaN FinFET fabrication process.

CHAPTER SIX: OPTIMIZATION OF VERTICAL FINFET FABRICATION PROCESS MODULES

6.1 Introduction

The optimization of vertical GaN power FinFET processing modules has been investigated in this chapter. Indeed, The orientation determination (OD), The source metallization (OH), the GaN etching (GAN), and the gate metallization (GM) are the critical steps that were found to be optimized; The remaining part of this chapter can be classified as follows; section II introduces the design and Fabrication of the masks sets for the optimization and final process. Section III details the optimization process for the source metallization step. Consequently, section IV is about optimizing GaN dry and wet etching. Section V details the optimization of Gate metallization by both electroplating and evaporation processes. Finally, section VI will conclude the optimization process. It is worth mentioning that the optimization of the Orientation Determination procedure (OD) is already published and is covered individually in the following chapter (Chapter V).

6.2 Masks Design and Fabrication

After underlying the first proposition of the Vertical GaN FinFET fabrication process, the drawings were completed to prepare the photomasks necessary for the optimization and realization of the optimized structure. In light of that, a completely UV lithography-based mask is firstly designed to optimize the GaN etching and the gate metallization steps. Such a mask contains patterns for both dielectric and source masks to define the FIN channel. A new mask was designed with additional layers such as orientation determination, Al_2O_3 opening, and Interconnection layers for the final device fabrication process. In addition, a hybrid lithography process is used to pattern the layers; obviously, the EBL has been used in orientation determination and source metallization steps, while the UV-lithography will be used for the remaining process steps. The size of the drawing area is chosen to be 1cmx1cm. The Final mask includes all necessary patterns to test the contact resistivity and the coupling capacitance between the source, gate, and drain contacts; Alignment marks, photolithography resolution test patterns, TLM test structures, component identification labels, and other additional GaN components for testing the GaN technology are examples about the added components to the pattern surface.

6.2.1 Optimization-based mask design:

As previously mentioned, the optimization-based mask contains only UV-lithography-based steps toward optimizing the GaN etching, and the gate metallization steps. The final 1cmx1cm mask consists of a 4×4 cell-matrix with a 2.5mm×2.5mm dimension for each. The schematic for one cell has been described in Figure 53

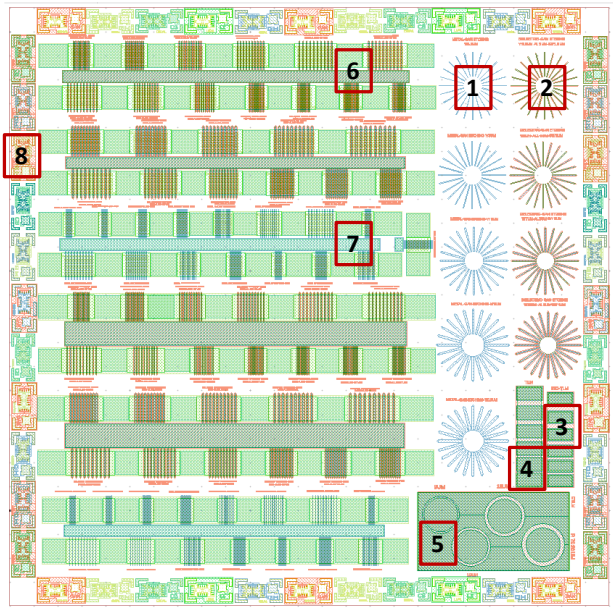

Figure 53:2.5mm×2.5mm cell components for the optimization process

In Figure 53, the descriptions of the numbers from 1 to 8 have been listed in Table 13.

Table 13:2.5mm×2.5mm cell components for the optimization process

Number	Pattern description
1	STAR shape with 24 fingers shifted 15˚from each other with self-aligned structure (metal as a mask)
2	STAR shape with 24 fingers shifted 15˚from each other with a dielectric as a mask.
3	TLM test for the device isolation.
4	TLM test for the source contact resistivity tests.
5	CTLM test for the source contact resistivity tests.
6	The devices with dielectric act as a mask (different numbers and distance between fingers).
7	Self-aligned devices (metal acts as a mask) (different numbers and distance between fingers).
8	Alignment marks to align the layer into each other (Al, LI, OH, GAN, GM, and CB)

After the mask design is finished, the.GDS file has been sent for photomask fabrication on 10cmx10cm transparent glass with a chrome layer. Another four copies from the fabricated mask have been made using UV-

lithography and ICP-RIE. Explicit, the UV-lithography is used to copy the patterns (the chrome-top has been chosen to make it possible to be copied in the LN2-3iT lab). A camera image for the copied mask is shown in Figure 54.

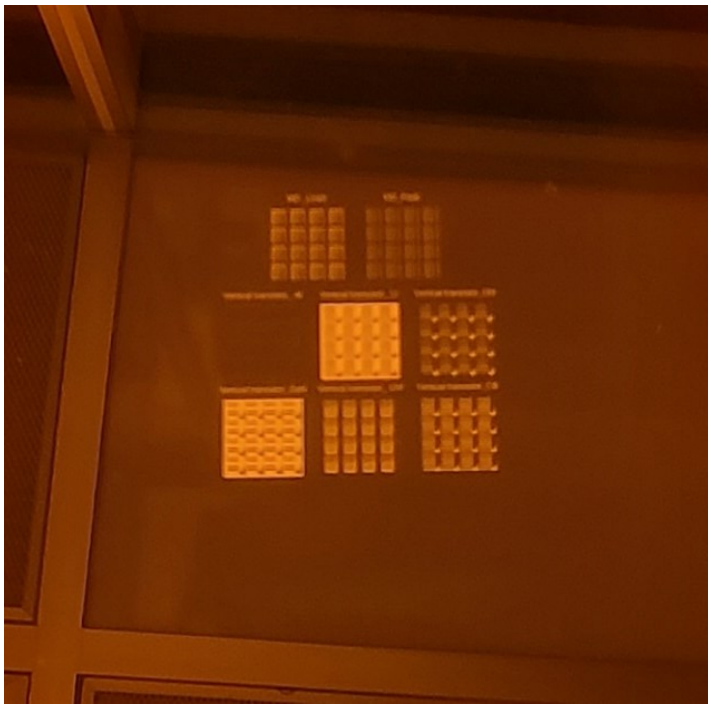

Figure 54: Camera image for the copied mask with all process layers

6.2.2 Final device mask design:

For the final process mask design, the following changes have been made:

- ✓ The orientation determination layer has replaced the Star patterns.
- ✓ The C_{GS}, C_{DS}, C_{GD} capacitances, and Interconnection test patterns have been added.
- ✓ The patterns with a dielectric as a mask have been removed.
- ✓ Two types of oriented devices have been introduced with a-Gan and m-GaN orientation.

The 1cm×1cm designed mask has been depicted in Figure 55. The cells with devices consisting of blue fingers represent the a-GaN oriented devices, while the cells with devices consisting of white fingers represent the m-GaN oriented devices

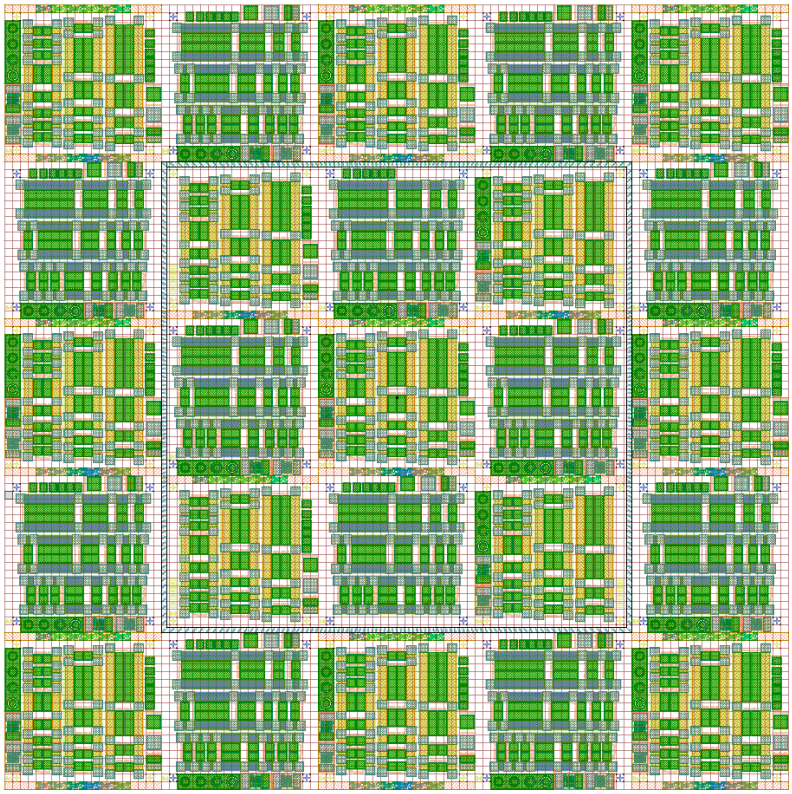

Figure 55:1cm×1cm mask design for Final device fabrication process

As shown in Figure 56, the mask consists of 5×5 cell-matrix with 2mm×2mm dimension for each. The schematic for one m-GaN oriented and One a-GaN oriented cell has been described in Figure 56(a) and 56(b), respectively.

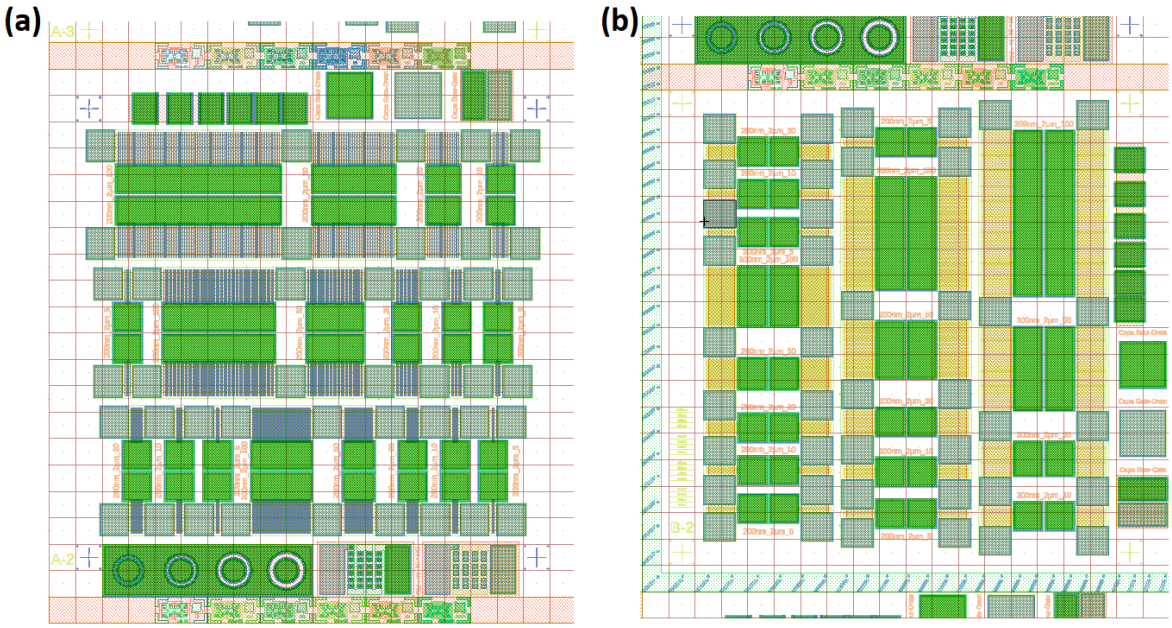

Figure 56:a-GaN and m-GaN oriented cells, a) a-GaN oriented cell,b) m-GaN oriented cell

As previously mentioned, the orientation determination and source deposition layers will be patterned by using the EBL. Other layers of photomasks have been fabricated individually since we use UV- lithography to pattern those layers. A camera image for the copied masks is shown in Figure 57.

Figure 57:Camera image for the copied masks with process layers except for OH and OD.

The testing patterns added to the final mask have been illustrated as in Figure 58

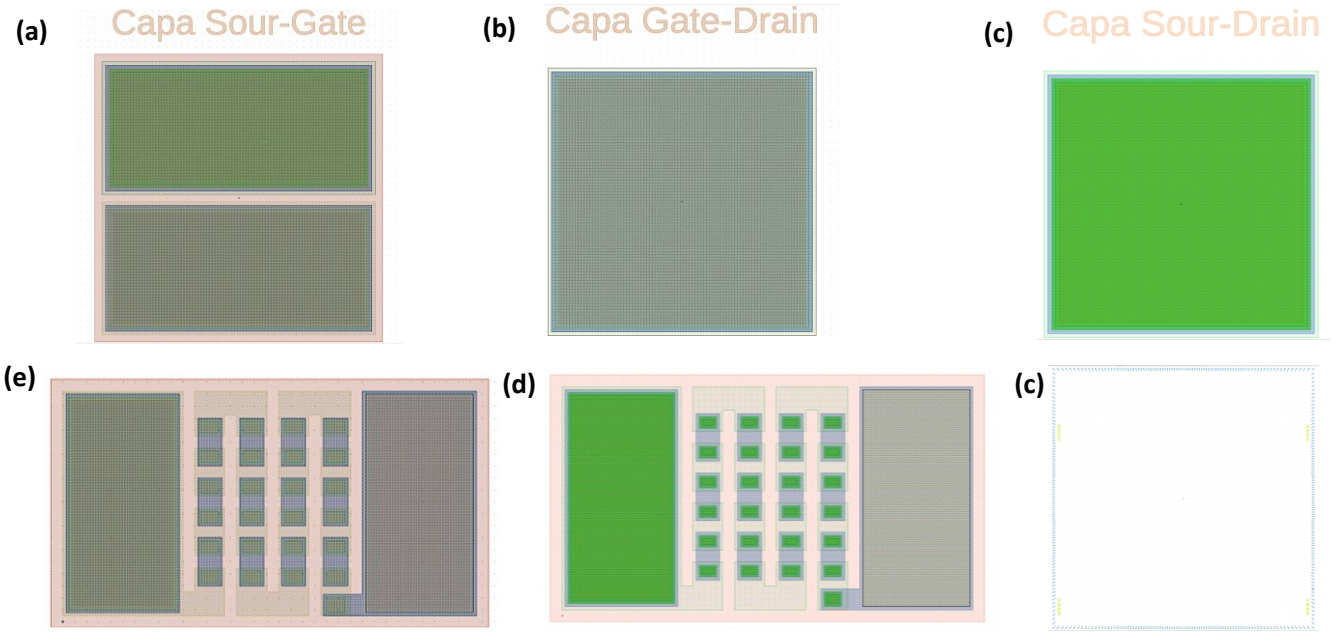

Figure 58:Gate, Source, and drain mutual capacitances test, Interconnection test patterns, and orientation determination (OD) on the final mask; a) CGS test, b)CGD test, c)CSD test, d)Interconnection test (OH), and e) Interconnection test (GM).

The testing patterns for ohmic contact and chosen final device structures are also shown in Figure 59

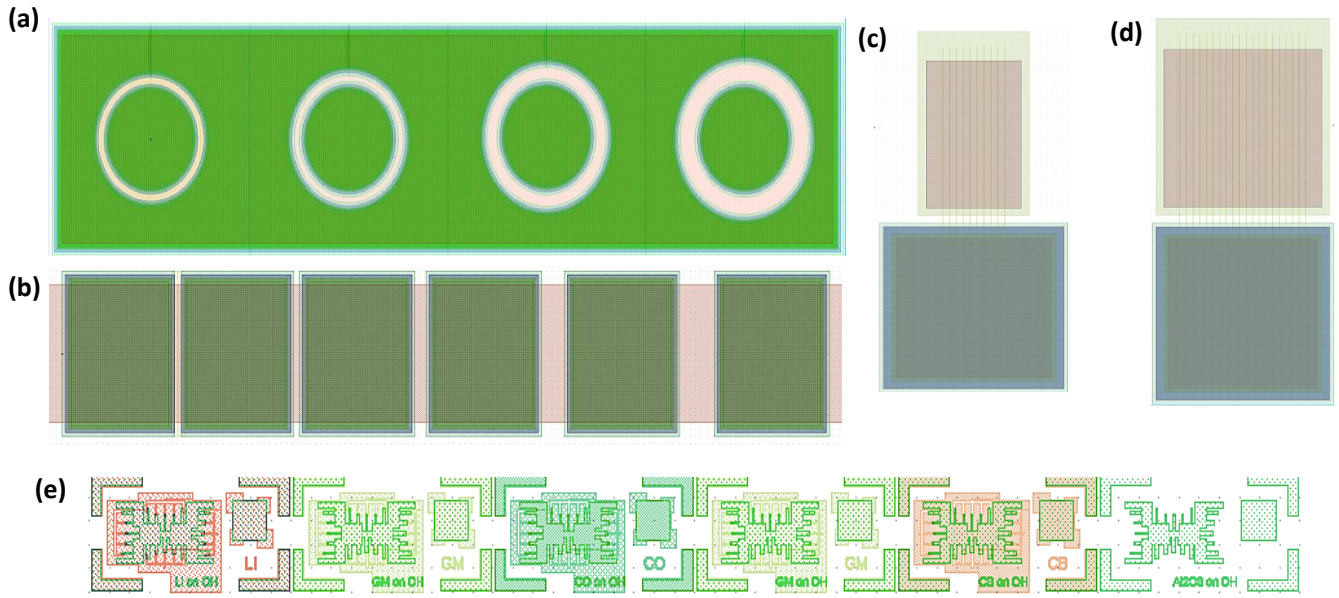

Figure 59:CTLM test, Alignment marks, and selected final device structures; a) CTLM test, b) TLM test, c) final device D=4µm, F=10, d) final device D=4µm, F=20, and e) Alignment marks for all layers.

6.3 Wafers availability for the optimization and final fabrication process

There are different types of wafers assigned for the optimization of processing modules and the final device fabrication. The Si samples are always used for the 1st test before applying the process on the GaN wafers. In addition, GaN/Si wafers are specially used to optimize the GaN wet etching recipe, including selecting mask properties toward FIN channel definition. For the final device masks, the GaN /sapphire wafers having the same final GaN/GaN epitaxial layer are used to apply the optimized steps before moving to GaN epitaxial on GaN. The list of samples assigned for the optimization process and fabricating the final device has been listed in Table 14.

Table 14:Samples availability for the optimization and final device fabrication

No	Wafer type	Description	Mask used	objectives	Sample size (1cmx1cm)	Irregular sample size	Total samples availability
1	Si	4 " wafers	Test-mask	Process optimization	unlimited	NA	unlimited
2	Epi-GaN/GaN	Mechanical	Test-mask	Process optimization	8	5	13
3	GaN substrate	Mechanical	Test-mask	Process optimization	16	5	20
4	GaN/Si	HEMT	Test-mask	Process optimization	0	13	13
5	Epi-GaN/Sapphire	Final wafers	Final mask	Process optimization	10	5	15
6	Epi-GaN/GaN	Final wafers	Final mask	Real device fabrication	10	5	15

6.4 Optimization of source metallization process (OH)

The optimization of the source deposition process has been carried out using the EBL as in the final mask. Since it's preferable to have self-aligned devices, the source metal has chosen to act as a mask for the channel definition step. This approach is called the source first approach, where the source stack composite should be chosen to be compatible with all further processing steps such as the GaN dry etching (ICP-RIE) and GaN wet etching with TMAH solution, ALD, and PECVD machines. The second challenge in the OH module is to optimize the EBL recipe to avoid any problem during the evaporation (e.g., blustering, cracks, discontinuity, etc.). The following subsections underline the design of experiments that we carried out to overcome those two challenges.

6.4.1 Optimization of EBL recipe for lift-off process.

For the EBL recipe optimization, several experimental tests have been carried out with different electron resist. The first trial was by using ELL11% and PMMA4% shown in Table 15.

Table 15:1st trial recipe details for EBL process

Exp	Details			comments
1st	**1st EBL recipe Sample with SSE# P528**			Check the thickness
	01.01	EL11%	4000rpm_60s_500 on Brewer	To have 500nm
	01.02	Soft bake	200°C / 2min	
	01.03	PMMA4%	4000rpm / 60s	To have 150nm
	01.04	Soft bake	200°C / 2min	
	01.05	Ebeam lithography	80, 90, 100, 110, 120, 130, 140, 150, and 160µC.cm^{-2}	Different doses
	01.06	Characterization	Optical microscope	
	01.07	Development	MIBK: IPA (1:2) / 2min	Drying with N_2

After the sample's development had been characterized using the optical microscope, we realized a peeled resist at different places on the sample. In addition, a lot of blustering has been detected due to the secondary electrons in the Raith 150two e-beam machine. The optical microscope images for different writing doses are shown in Figure 60.

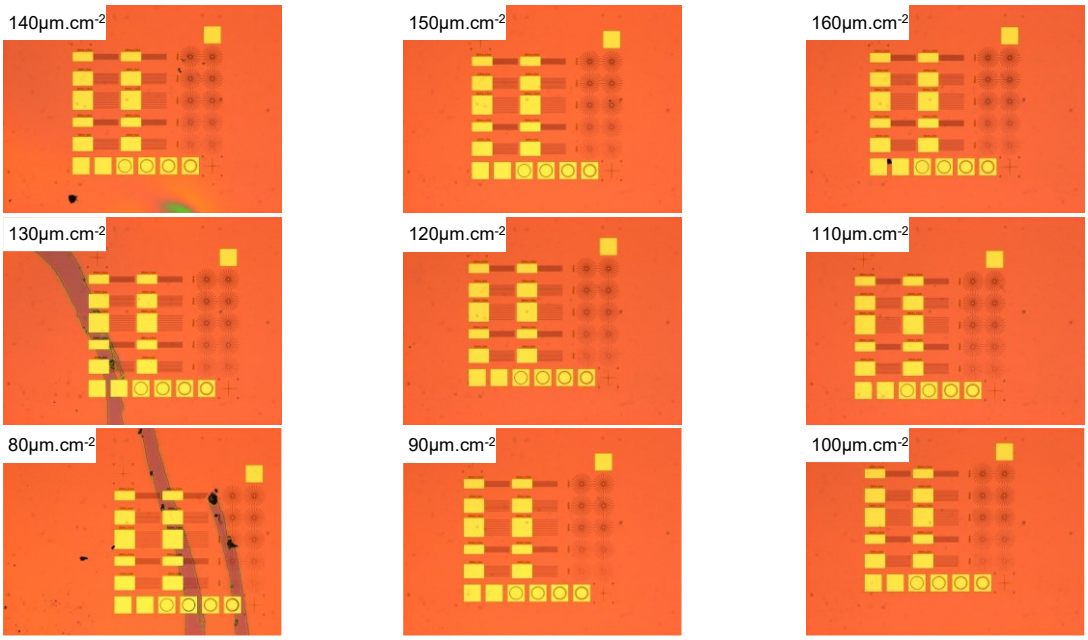

Figure 60: Optical microscope characterization for the 1st EBL recipe with different doses

The source metal stack with Ti/Au/Ni (20nm/350nm/30nm) has been deposited by evaporation to investigate the lift-off process. The SEM images for the metallization process after the lift-off is shown in Figure 61

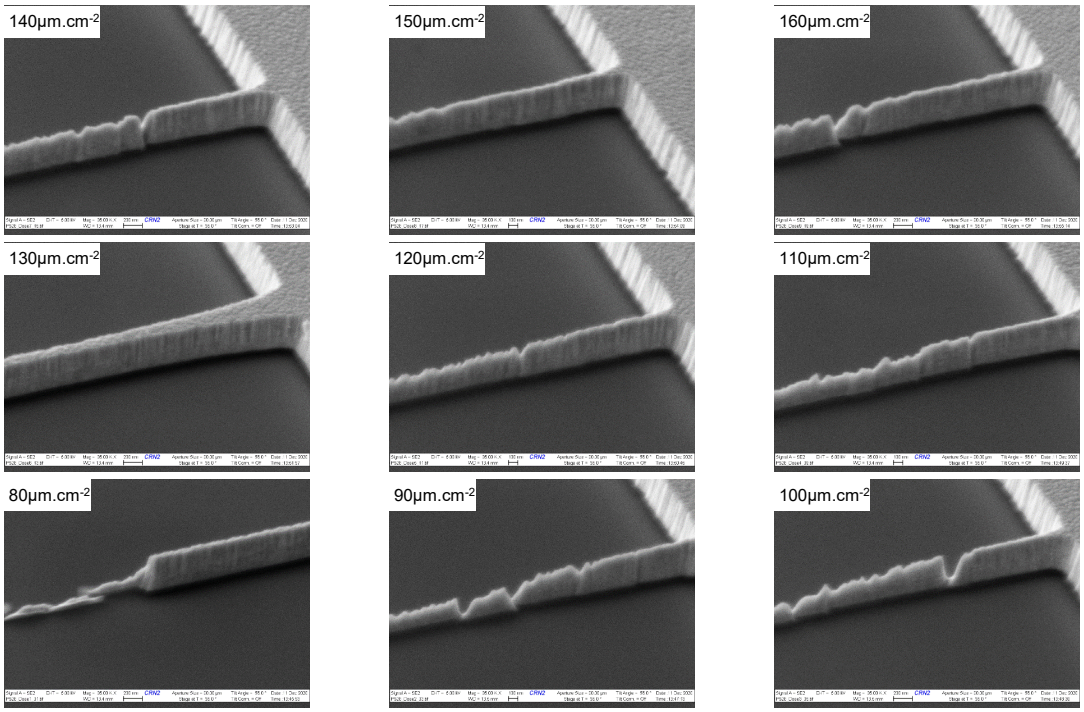

Figure 61: SEM characterization after metallization using the 1st EBL recipe and different doses

After several tests, including changing resist types and combinations, increasing the range of writing doses, development time, and backing temperature. The EBL recipe tabulated in Table 16 is found to be optimal for our process.

Table 16:Optimal recipe description for EBL process

Exp	Details			comments
	Final EBL recipe Sample with SSE# Q456			Check the thickness
	F.01	EL11%	4000rpm_60s_500 on Brewer	To have 450-500 nm
	F.02	Soft bake	200°C / 2min	
	F.03	PMMA9%	4000rpm / 60s	To have 500-600 nm
	F.04	Soft bake	200°C / 2min	
	F.05	Ebeam lithography	250µC.cm^{-2}/ 6nm step size	
	F.06	Characterization	Optical microscope	
	F.07	Development	MIBK: IPA (1:2): IPA/ 2min+2min:30s	Drying with N_2
	F.08	O_2 plasma line #1	Removal of 10nm PMMA≈ 2min	Calibration required

The optical microscope and SEM for the wafer Q456 before metallization are shown in Figure 62 and Figure 63.

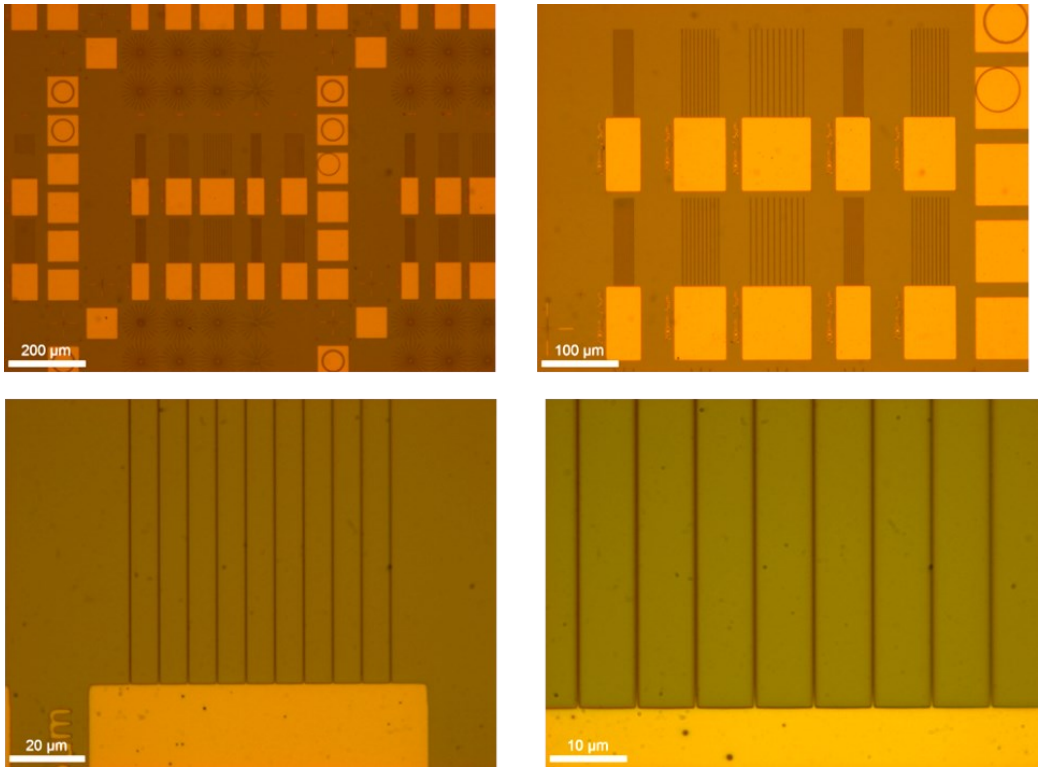

Figure 62:Optical microscope characterization for the optimized EBL recipe with 250µC.cm^{-2} dose

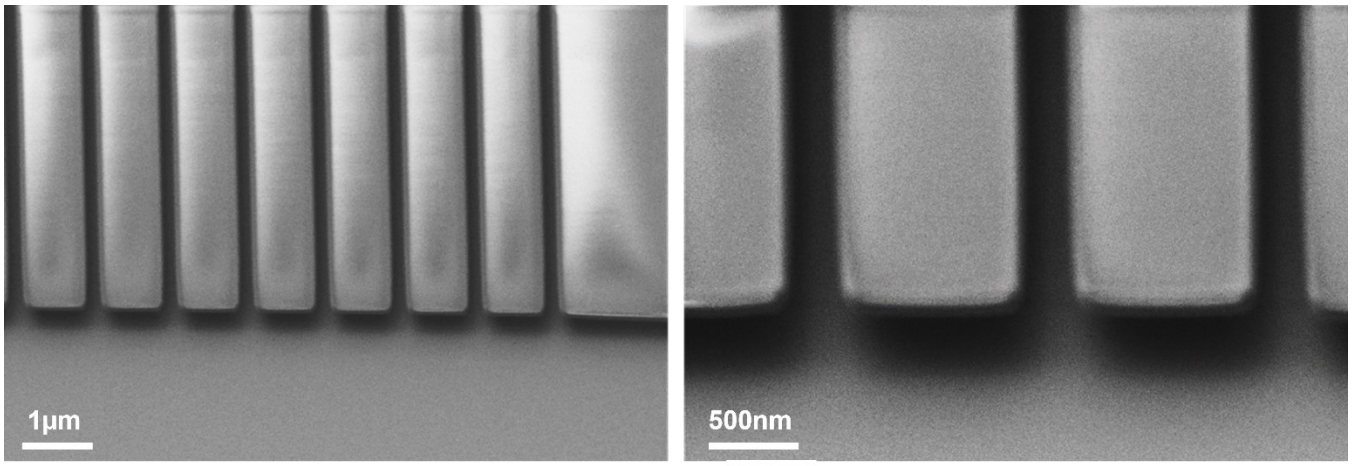

Figure 63: SEM characterization for the optimized EBL recipe with 250µC.cm^{-2} dose

The source metal stack with Ti/Au/Ni (20nm/350nm/30nm) has been deposited by evaporation to investigate the lift-off process. The SEM images for the metallization process after the lift-off is shown in Figure 64.

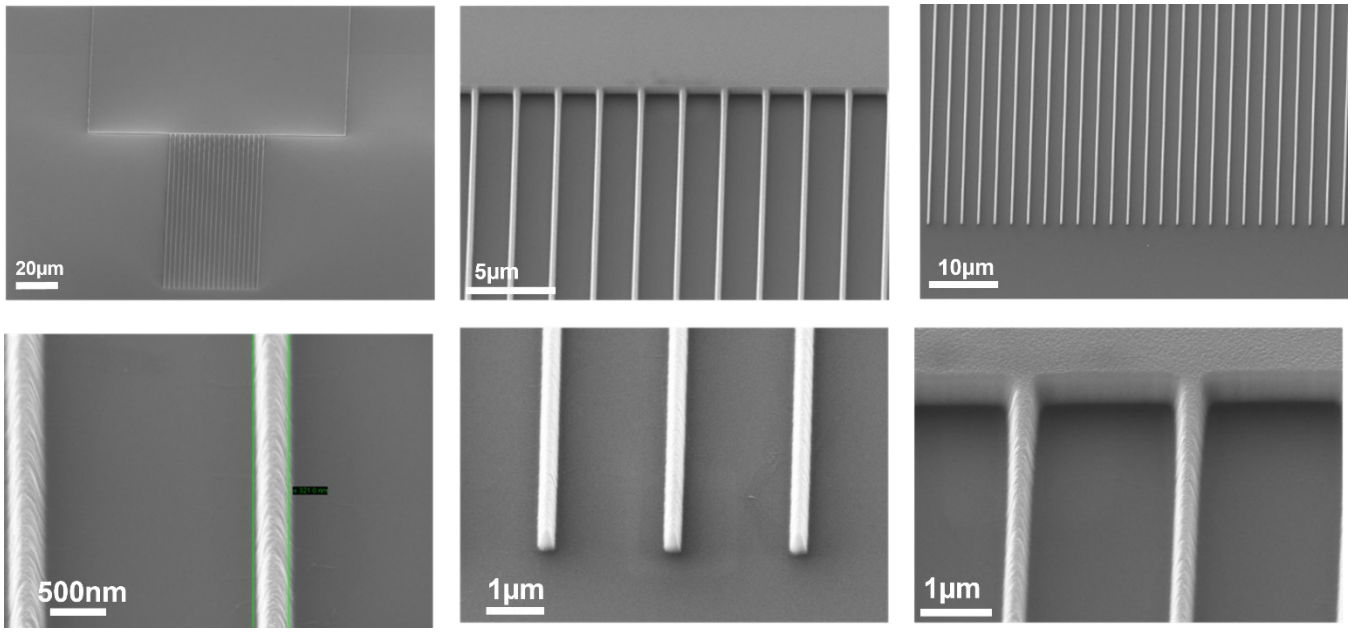

Figure 64: SEM characterization for the optimized EBL recipe after metallization.

It is worth mentioning that the fingers after metallization are regular, with an average width of 320nm. The optimized recipe will then be used for the optimization process of the source metallization stack.

6.4.2 Design of source metallization stack composition.

As previously mentioned in the last section, Ti/Au/Ni (20nm/350nm/30nm) stack has been used to optimize the EBL recipe. The first and the last layer (Ti and Ni) metals shall be compatible with the further processing

modules to proceed with the starting process. Since gold is the best choice for the source contact due to its low resistivity, it should be the thickest metal in the stack. However, the gold metal is incompatible with the STS-PECVD machine used for high-quality SiO_2 deposition. It shall be protected all the time with an upper layer metal or dielectric. Firstly, we investigate the etching rate for both Ti and Ni metals with TMAH solution; Two samples with Ni /Si and Ti /Si with patterns are chemically etched in TMAH solution after the metal thickness has been measured with a profilometer. Aqua Regia solution for 10 min has removed the metal. The profilometer is then done and found that the Ni etching rate is 56nm/Min while the Ti etching rate is very low (less than 1nm/min).

Several compatibility tests have been carried out to find the best source stack composition to protect the gold and to have good adhesion with the GaN surfaces. The starting set of metallization stacks STShas been listed in Table 17.

Table 17:list of samples with proposed source metallization stacks

SSE#	Source metallization stack description	The thickness
Q160A	Ti/Au/Ni	[30nm/320nm/30nm]
Q160B	Ti/Pt/Au/Ni	[30nm/20nm/300nm/30nm]
Q160C	Pt/Au/Ni	[30nm/320nm/30nm]
Q160D	Ni/Au/Ni	[30nm/320nm/30nm]

After the metallization has been done on the four samples, all the lift-off profiles are in good shape except in sample Q160C, where only the pads metal is there without any fingers. The remaining three samples are now ready to pass the test of compatibility with the TMAH solution. The three samples have been immersed in TMAH solution for 1 min followed by SEM characterization, The SEM images for the sample Q160D are shown in Figure 65. It is worth mentioning that, for all stacks composites, we realize that the lower Ni metal has been etched with TMAH solution, while the Ti is still there, which means that Ni is not the right choice for the adhesion layer while Ti is still as an option. However, after GaN etching in ICP-RIE, we realized that the adhesion of Ti would be degraded due to the physical etching part in ICP-RIE. Therefore, both metals shall be changed for further optimization tests.

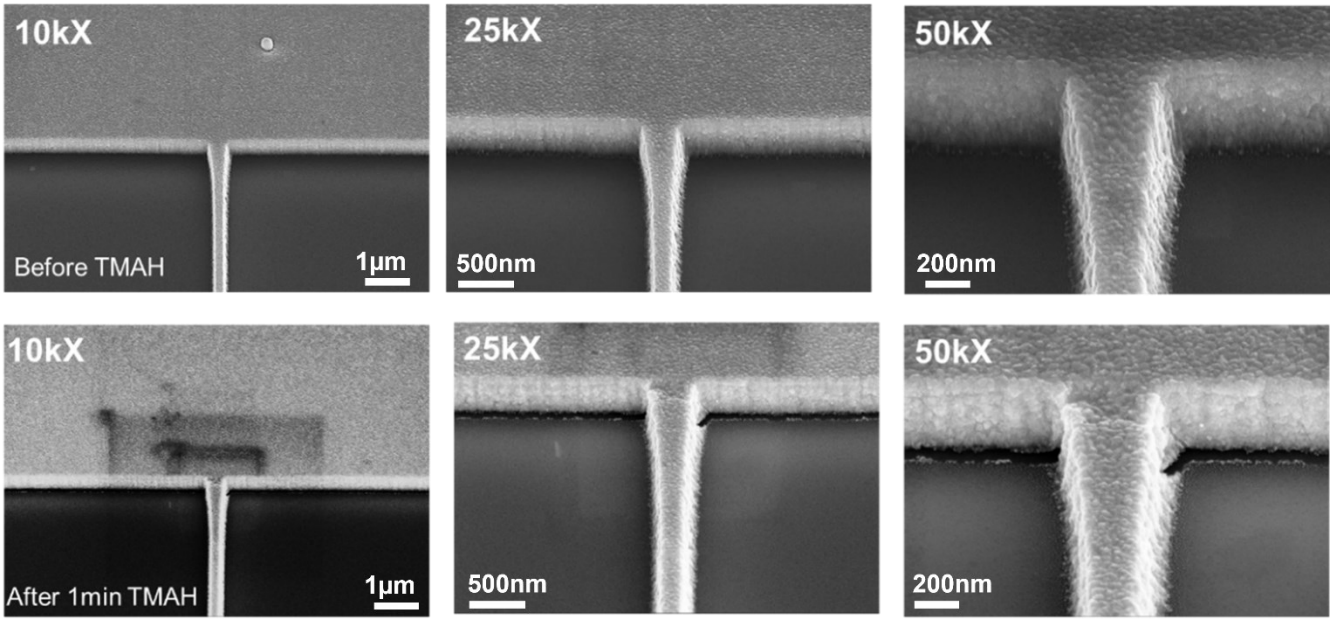

Figure 65:SEM characterization for sample Q160D before and after 1min of etching with TMAH.

The SEM images for sample Q160B with Ti adhesion layer after 1min of wet etching with TMAH have been shown in Figure 66.

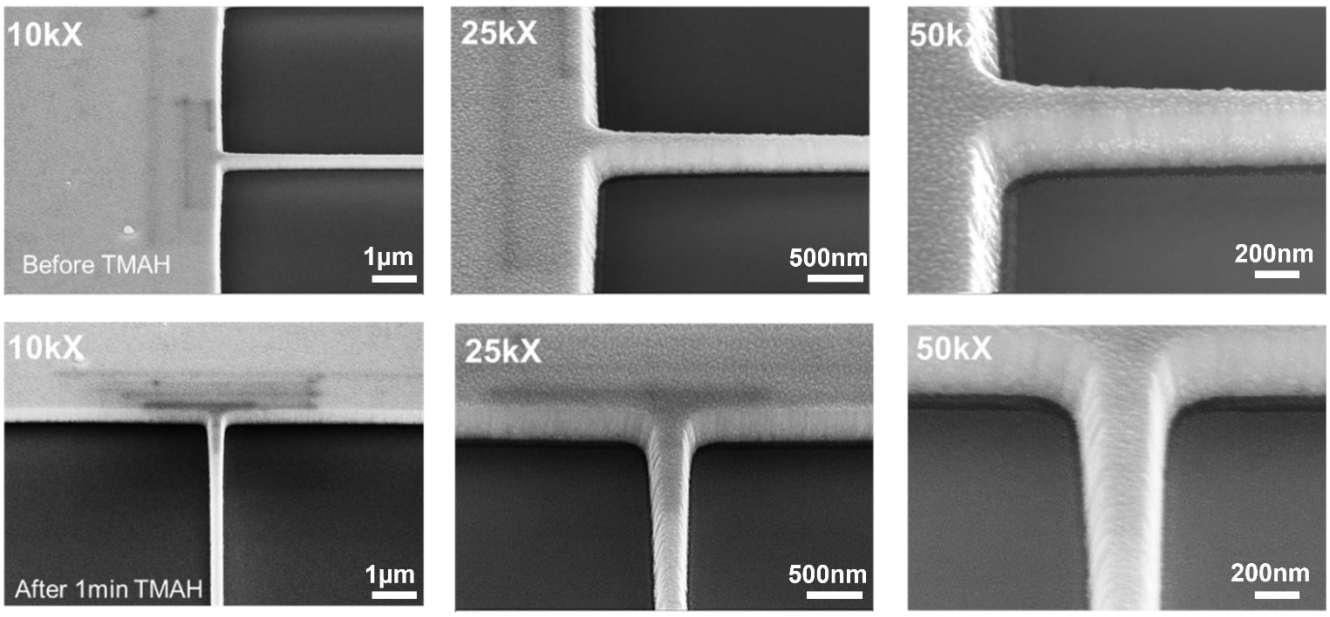

Figure 66:SEM characterization for sample Q160B before and after 1min of etching with TMAH.

As it is known that Cr is a highly reactive metal with superior adhesion properties[116], Thus, an alternative proposition has been underlined by using the Cr metal as an adhesion layer and a protection layer above the gold.

The new source metallization stack composite from Cr/Au/Cr with 20nm/360nm/30nm. The Cr metal is compatible with the PECVD and ALD machines, but its compatibility with ICP-RIE and GaN wet etching recipe (TMAH) shall be investigated. Thus, a Cr/Si sample with Cr patterns was first chemically etched with TMAH solution (optimized recipe). After wet etching, we have realized that the Cr etching rate is very low in TMAH (few angstrom/min). Thus, it is fully compatible with TMAH.

Consequently, the same sample has been etched in ICP-RIE using the" GAN-LED" recipe. Afterward, we realized that the Cr is etched in III-V with an etching rate of 35-40nm/min. Therefore, a new metal layer should be introduced to protect the Cr layer during the GaN etching in ICP-RIE. To investigate the Cr compatibility with the ICP-RIE machine, a GaN epitaxial on GaN sample (SSE# P563) has been metalized using Cr/Au/Cr with 20nm/360nm/30nm source stack; The wafer is then etched in ICP-RIE machine using" GAN-LED" recipe for 4min:30sec period. The SEM characterization for the fingers after III-V is shown in Figure 67 using two different positions.

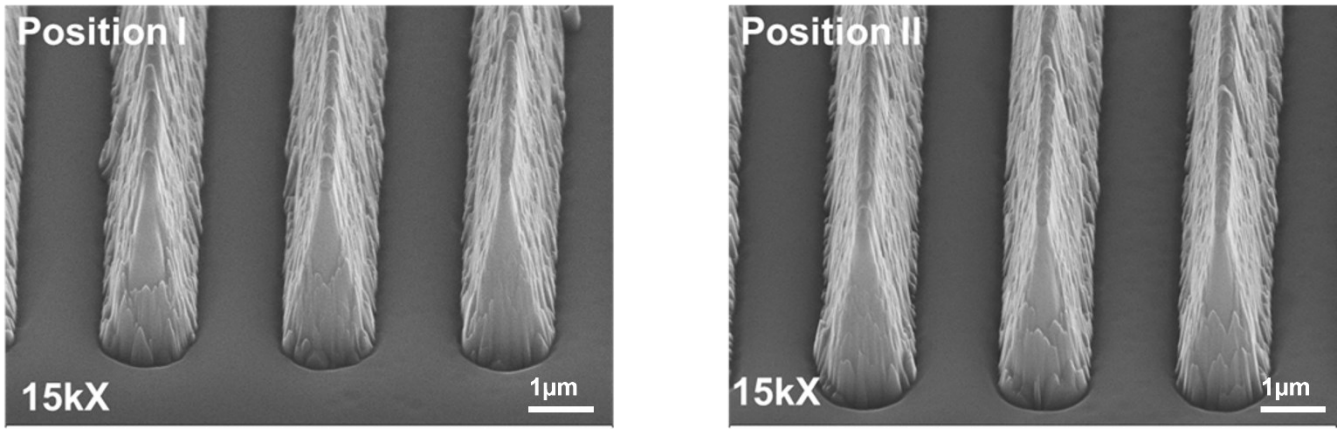

Figure 67: SEM characterization for sample P563 after GaN dry etching in ICP-RIE machine

One can observe from Figure 67 that there is a discontinuity problem for the metal mask. This can be explained as the Cr layer is totally etched, and the Au is then starting to be etched in ICP-RIE. To investigate the impact of TMAH on the FIN channel in the existence of mask discontinuity problem, the same wafer has been chemically etched in TMAH for different periods and then characterized with LEO 1540 XB SEM, as shown in Figure 68. It is easily can be recognized from the figure that metal mask straightness and consistency will protect

the GaN FIN sidewalls from being attacked by the TMAH solution. Explicit, the N^- atoms at the channel edge under the metal mask will create a sort of bond with the mask in which the hydroxide (OH^-) ions can't access the Ga atoms behind the N^- ions[81].

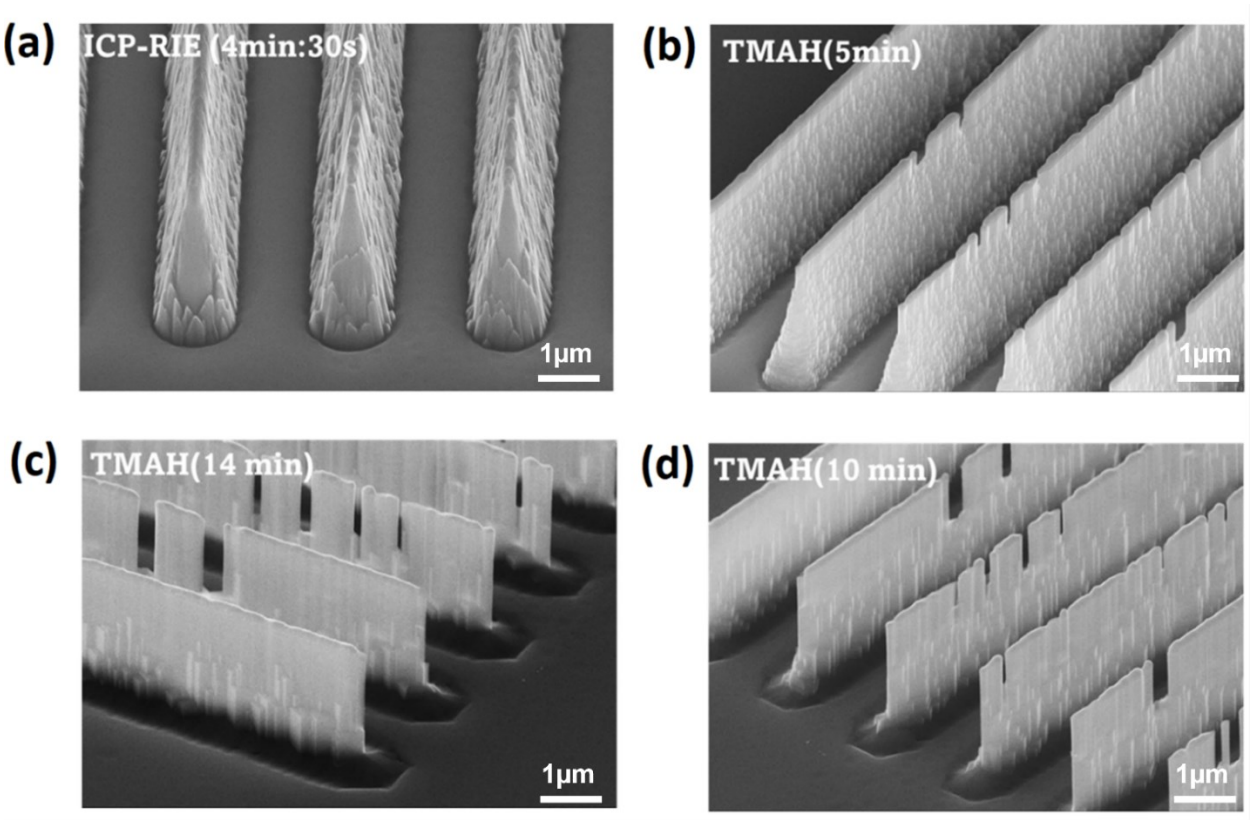

Figure 68: SEM characterization for sample P563 after GaN wet etching with the optimized TMAH recipe. a) after GaN dry etching. b) after 5 min in the TMAH recipe. c) after 10 min TMAH recipe. d)after 14 min TMAH recipe.

Based on the preceding, a new metal should be introduced to the source metallization stack to protect the Cr layer above the gold from being etched in the ICP-RIE system. We have investigated various metals to be compatible with ICP-RIE; Ti and Ni have been selected among those candidates. The Ti and Ni etching rates in III-V have been investigated, and we found that the Ti etching rate is more than 40nm/min. In comparison, the Ni etching rate is 5nm/min. Therefore, we choose to add a Ni layer 100nm thick above the upper Cr layer.

The compatibility test of the new stack with Cr/Au/Cr/Ni with respective (20nm/300nm/50nm/50nm) thicknesses has been carried out using a Si wafer. After the lift-off process, the O_2 cleaning recipe is used in the III-V machine to remove the residual PMMA resist from both sides of the fingers. The GAN-LED recipe has then been

used to etch the wafer for 4min:30sec. After SEM characterization, the discontinuity problem still occurs even with the additional Ni layer, shown in Figure 69.

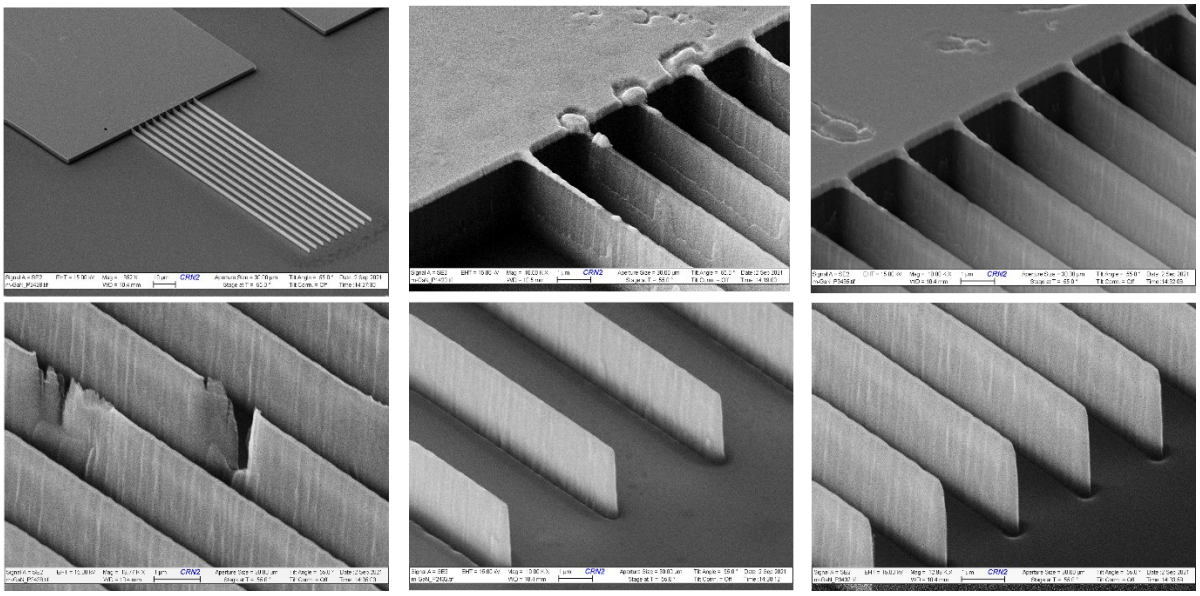

Figure 69:SEM characterization of the Si wafer Q456 after GaN dry etching with ICP-RIE

It is observable from Figure 69 that the origin of the discontinuity problem is not only related to the high etching rate of Ni in the fingers regions but also to some other reasons stressing the metal stack in the III-V machine. Accordingly, two important changes have been added to the process to solve the problem: increasing the Ni layer thickness to 130nm instead of 50nm. The second is to use another recipe to remove the burned PMMA on the sidewalls of the fingers. It is worth mentioning that, with the O_2 clean recipe, the coil power and the O_2 flow rate were 800W and 45sccm, respectively. The relatively high coil power and flow rate are the main reasons for the metal mask's damage. It might be due to the high plasma stressing current (Antenna effect) where the fingers mask acts as an antenna to accumulate and react with a high density of electrons. The high density of electrons resulted from high RF power[117],[118]. Alternatively, a recipe named “DESCUM” is used with the same coil and bias powers of 30W. The O_2 flow rate is reduced to 5sccm with the pressure of 4mTorr. To validate the last propositions, a Si wafer (Q401) has been metalized with a metallization stack consisting of Cr/Au/Cr/Ni with (20nm/250nm/50nm/130nm), respectively, after the lift-off process, the DESCUM recipe has been used for 10min to remove the residual PMMA on both finger’s sides, the GAN-LED recipe has then be used to etch the wafer for

4min:30sec. The SEM images show that the discontinuity problem of source metal disappeared, Moreover, the Cr Cr layer with a residual Ni metal above the Gold is still there after the application of GAN-LED recipe. Conclusionary, the origin of the "Mask discontinuity problem" was due to first recipe used for PMMA cleaning in ICP-RIE machine (O_2 clean). The fingers shape after O_2clean and DESCUM recipes have been illustrated in Figure 70.

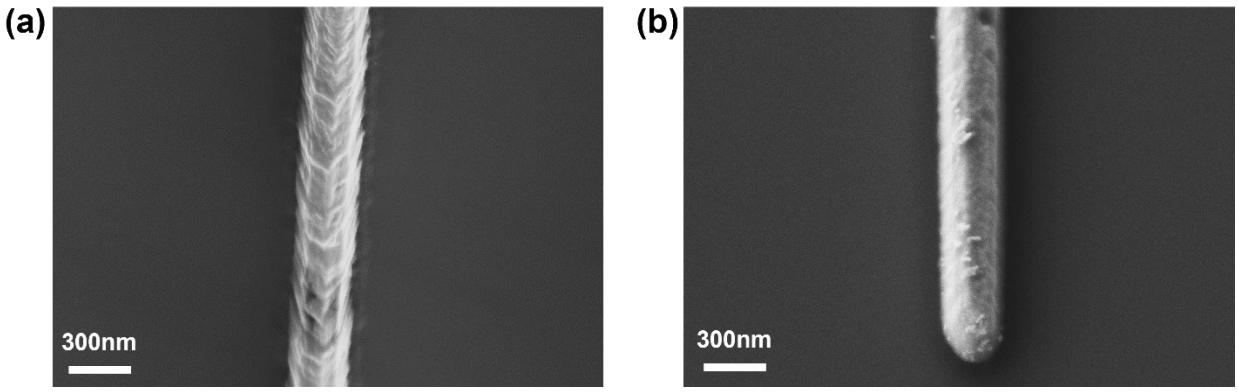

Figure 70: SEM characterization of source stack after 10 min of PMMA cleaning in ICP-RIE; a) using O_2Clean recipe, b)using DESCUM recipe

After the dry etching step in ICP-RIE, the fingers with the final stack were perfectly identified with full protection for the gold layer. The SEM characterization for the wafer Q401 is described in Figure 71.

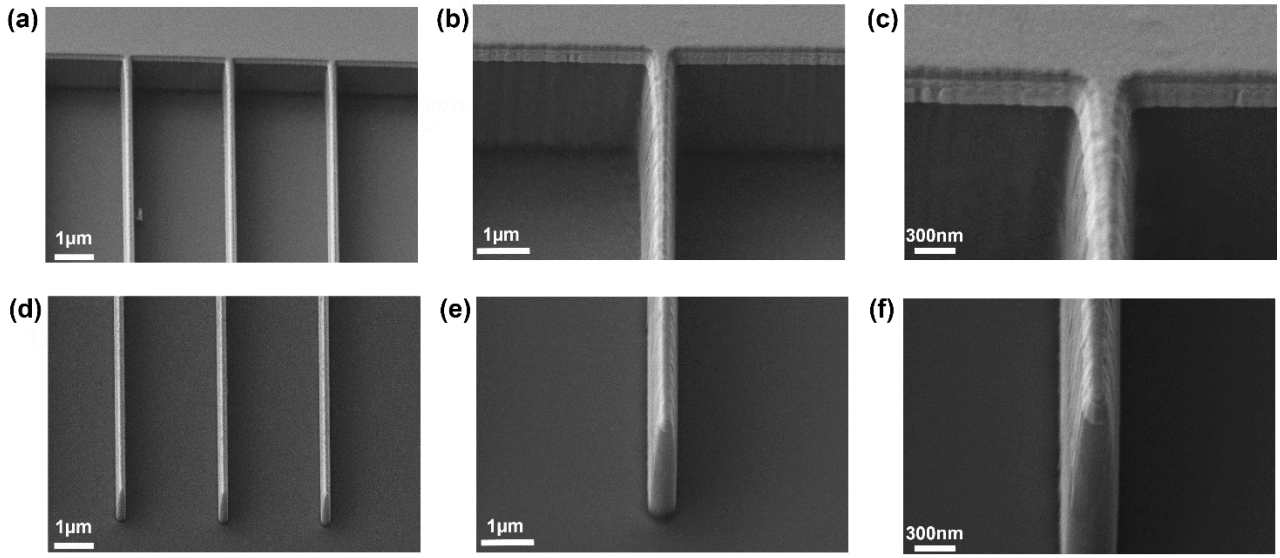

Figure 71:SEM characterization for Q401 wafer with the optimized source stack with different locations; a),b),and c) pads side with 5kX,15kX,and 30kX magnification. d), (e,and f) front view of the finger with 5kX,15kX,and 30kX magnification

6.4.3 Optimization of GaN dry etching process

After the source metallization has been done, the sample is then ready for the channel definition step. This is mainly done by using the ICP-RIE machine called III-V in the LN2-3iT lab. To have channel sidewalls with minimal surface roughness after the wet etching, defining a straight FINs channel is important. Therefore, we will ensure that the finger's sidewalls are clean without residual PMMA from the lift-off process. Explicit, the residual PMMA will act as a mask during the GaN dry etching until it is etched, leading to a denaturized channel shape as shown in Figure 72.

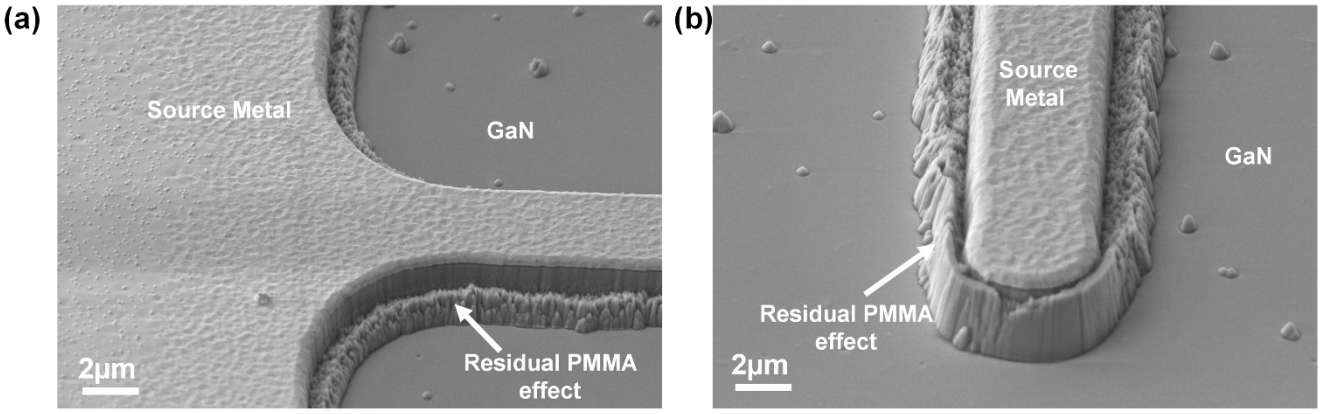

Figure 72: SEM characterization for Impact of residual PMMA on GaN dry etching. a) FIN pad side. b) FIN front side

To prepare the wafer for the plasma etching. The sample should be processed in the III-V machine by using an O_2 clean recipe. This type of recipe is used to remove any organic material (PMMA in our case) from the surface of the wafer. The wafer is then characterized in LEO 1540 XB SEM to check if there is still any resist on the finger's sidewalls. If some residual PMMA is still there, the O_2 clean must be done again for another 5 min slowed by SEM characterization until the whole PMMA is removed.

After the cleaning process is done, the wafer will be etched using the process already detailed in Table 4.5. as this work is a part of Group GaN projects where the GaN dry etching recipes have been already optimized, for our process, we have used the GAN-LED recipe already tabulated in Table 8. After the III-V etching is done, the wafer should be Characterized in LEO 1540 XB SEM to check the dry etching profile. SEM images for the wafer etched in the III-V machine are shown in Figure 73.

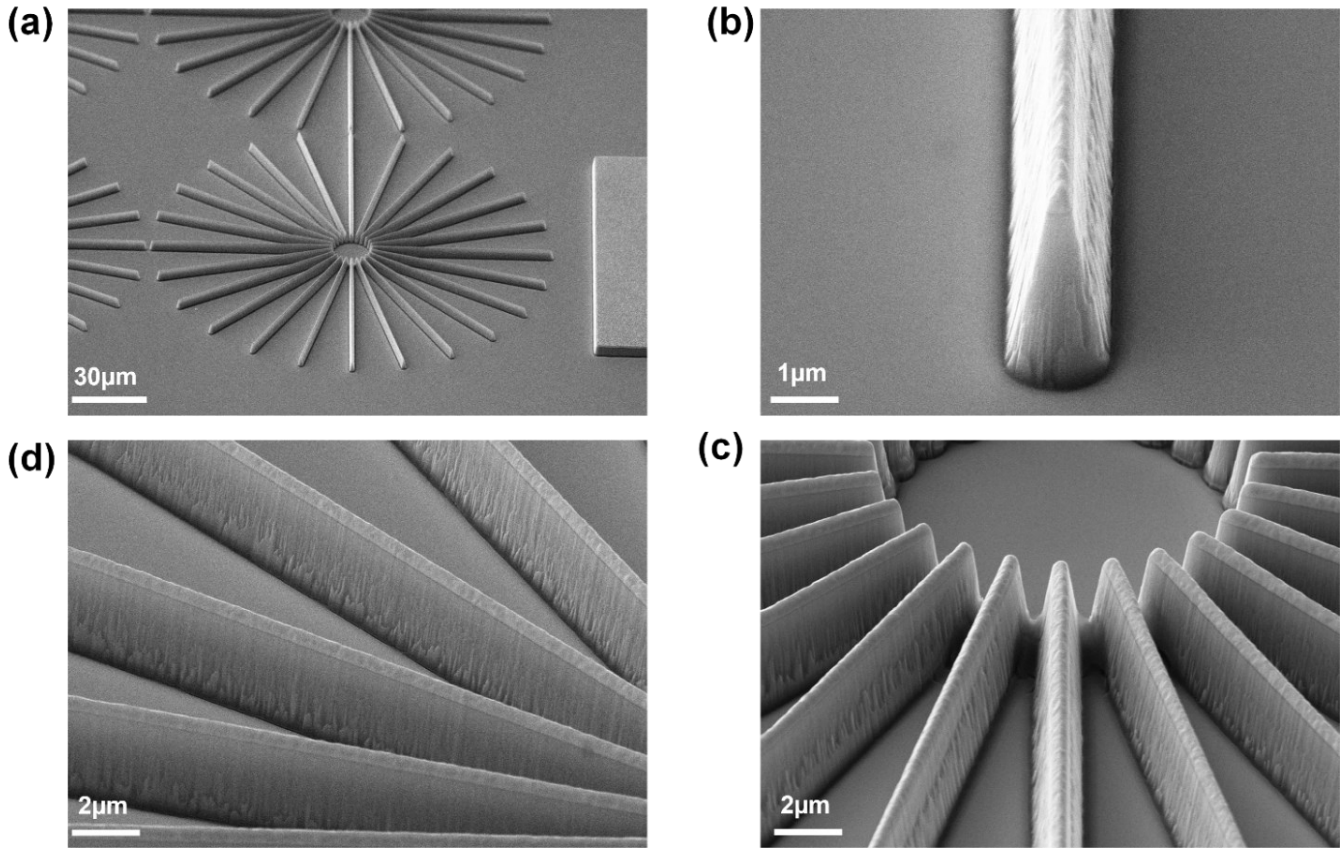

Figure 73:SEM characterization after GaN dry etching using GAN-LED recipe a) STAR patterns b) FIN front view. c) STAR end of the FIN. d) STAR, side view

It can easily be observed from Figure 73 that the GaN dry etching process is associated with a high surface roughness on the FIN channel's sidewalls and a trapezoidal shape.

6.4.4 Optimization of GaN wet etching process

For vertical GaN FinFET devices, a Fin channel structure with non-polar plane side walls is favorable for Normally-Off operation because it offers the desired channel width and low charge density at $V_{GS} = 0V$ [22-23]. The chemical etching process has also been demonstrated in the literature for post dry etching treatment of GaN [25–28]. It is also discussed in detail in the GaN etching process section 4.4.6 in chapter Four.

Etching selectivity, surface roughness rate, and undercut profile creation are the main challenges to be considered when the GaN wet etching process is underlined [67]. The m-GaN and a-GaN channel sidewalls revealing process require a specific lithography orientation of the Fin channel structure. Thus, the optimization process started with the STAR polar diagram patterns shown in Figure 73(a), oriented parallel to the flat zone. Both

dielectric and metal masks have been used for the optimization process with several designs of experiments. The temperature, etchant concentration, etching duration, agitation speed, UV-light assistance, and the finger's orientation with respect to the flat zone have been considered during each experiment design. The list of experiments with the observations has been detailed as in Table 18.

Table 18:Design of experiment results toward GaN wet etching optimization

SSE#	Etchant	Concentration	Temperature	Time	Observations
O984A	AZ400K	100%	80C°	4Hours	Poor (GaN/SiO_2) selectivity, High defect rate, No undercut profile
O984B-1	AZ400K	40%	45 C°	4Hours	Poor (GaN/SiO_2) selectivity, High defect rate, No undercut profile
O984C-1	AZ400K	40%	35 C°	4Hours	Poor (GaN/SiO_2) selectivity, High defect rate, No undercut profile
O984D-1	AZ400K	40%	25 C°	4Hours	Poor (GaN/SiO_2) selectivity, High defect rate, No undercut profile
O984D-3	KOH	45%	80 C°	4Hours	SiO_2 totally removed, High defect rate, No undercut profile
O984B-2	KOH	1%	45 C°	4Hours	Poor (GaN/SiO_2) selectivity, High defect rate, No undercut profile
O984C-2	KOH	1%	35 C°	4Hours	Poor (GaN/SiO_2) selectivity, High defect rate, No undercut profile
O984D-2	KOH	1%	25 C°	4Hours	Poor (GaN/SiO_2) selectivity, High defect rate, No undercut profile
O984E-1	TMAH	10%	80 C°	3Hours /UV	Low (GaN/SiO_2) selectivity, Lower defect rate, Low etching rate, No undercut profile
O984E-1	TMAH	15%	80 C°	3Hours /UV	Higher (GaN/SiO_2) selectivity, Lower defect rate, Low etching rate, No Undercut profile detected
O984F-1	TMAH	20%	80 C°	3Hours /UV	Good (GaN/SiO_2) selectivity, Lower defect rate, etching rate, Start of undercut profile Formation
O984J-1	TMAH	25%	85 C°	2Hours /UV/ Stirring	Very Good (GaN/SiO_2) selectivity, Lowest defect rate, intermediate etching rate, undercut profile detected.
O984J-2	TMAH	25%	80 C°	3Hours /UV	Very Good (GaN/SiO_2) selectivity, Lower defect rate, etching rate, Undercut profile
O984J-3	TMAH	25%	95 C°	4.5Hours /UV/ glycerol	Very Good (GaN/SiO_2) selectivity, High defect rate, high etching rate (compared to other TMAH, undercut profile detected)
P562	TMAH	25%	85 C°	30 min /UV	The metal used as a mask, superior selectivity with Cr Lowest defect rate, intermediate etching rate, undercut profile created.

It is observable from Table 18 that (TMAH 25%,85˚C) is found to be the best proposition for GaN FIN channel engineering using crystallographic etching. Furthermore, UV light-based TMAH etching is an efficient technique to enhance the GaN sidewalls etching rate [74]. It also improves the etching selectivity when a dielectric

material is used as a mask [32-33]. The time of etching was longer than the estimated time for the final process since we have done the optimization using the UV-lithography with wide fingers (>3.5µm) where the difference between the width of the FIN base and the top is much higher in the case of EBL patterns (<320nm).

As a prerequisite for engineering a-GaN and m-GaN oriented channel sidewalls, the FIN channel was fabricated on a GaN epitaxial /GaN wafer (P558-B) with the source metal as a mask. After the dry etching of GaN is completed in the III-V machine, we moved on to the wet etching of a specific a or m-GaN-oriented pattern for 10 minutes with 2 min wet etching steps. Consequently, 4 min and 6 min wet etching steps were performed. The characterization of a-GaN patterns and m-GaN patterns for the total etching period has been characterized as shown in Figure 74 and Figure 75, respectively.

One can observe from Figure 74 and 82 that the wet etching profile follows the theoretical concept of GaN wet etching, which is already discussed in 4.4.6; furthermore, the surface roughness on a-GaN oriented Channel sidewalls is higher than in the case of m-GaN channel sidewalls. The etching rate started with a much higher value when the a-GaN or m-GaN was revealed, and This is due to the repulsing power generating from the N- ions with negatively charged dangling bonds.

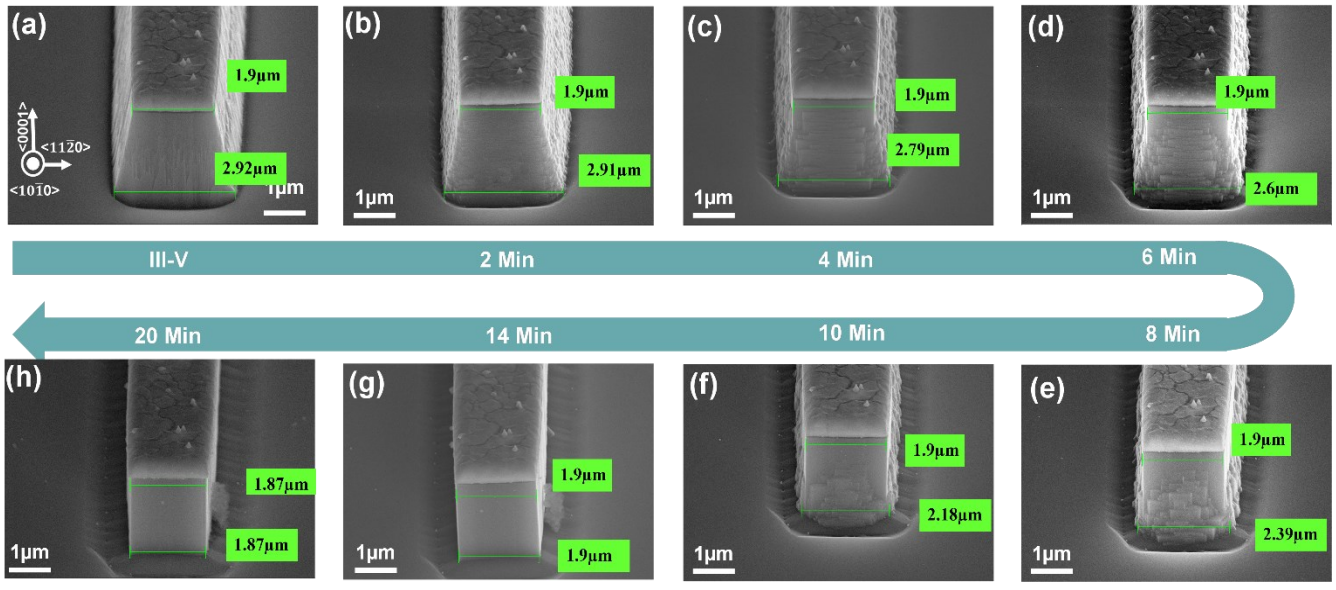

Figure 74:wet etching process for a-GaN oriented FIN channel engineering. (a)to(h); III-V,2min, 4min,6min,8min,10min,14min, and 20min, respectively.

The discussion about the GaN crystallographic etching is already detailed in the publication chapter (Chapter Five). The final tracing algorithm for the GaN wet etching process has also been calibrated Based on Figure 74 and Figure 75 to ensure faster tracing of an m-GaN morphology evolution with TMAH, as illustrated in Figure 76.

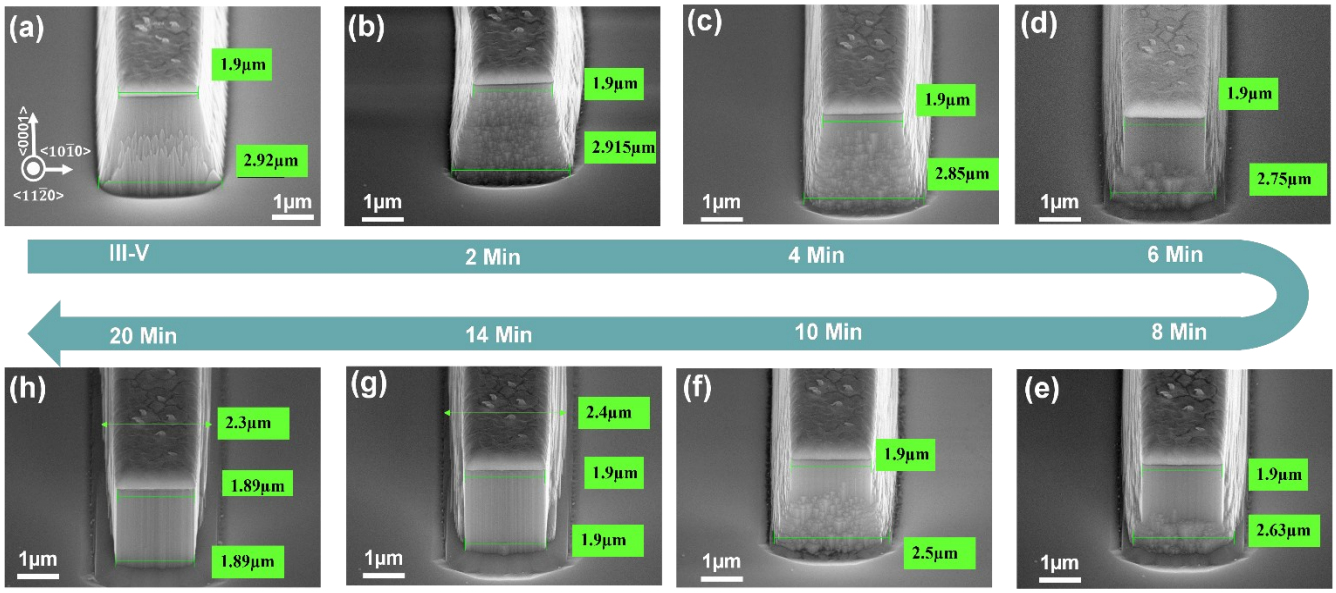

Figure 75:wet etching process for m-GaN oriented FIN channel engineering. (a)to(h); III-V,2min, 4min,6min,8min,10min,14min, and 20min, respectively.

The design of the experiment for the GaN wet etching process has been illustrated in Figure 76. Accordingly, after the deoxidation step, the wet etching started by immersing the GaN wafer in TMAH solution for 5 min, followed by SEM characterization. Another 5 min of wet etching will be performed if the total time of etching is less than 10 min. Otherwise, an additional 2min step etching process is being done, followed by SEM characterization. If the FIN channel sidewalls are totally straightened, the undercut profile starts to be investigated. Another 2 min step of wet etching shall be done, followed by characterization to investigate the undercut profile creation. If this happens, the experiment will be finished. Otherwise, another 2 min step etching will still be performed until the desired undercut profile is explored with (50-80) nm depth. It is worth mentioning that, before any wet etching process is done, a GaN deoxidation step shall be done by using HCL: H_2O with (1:10) dilution.

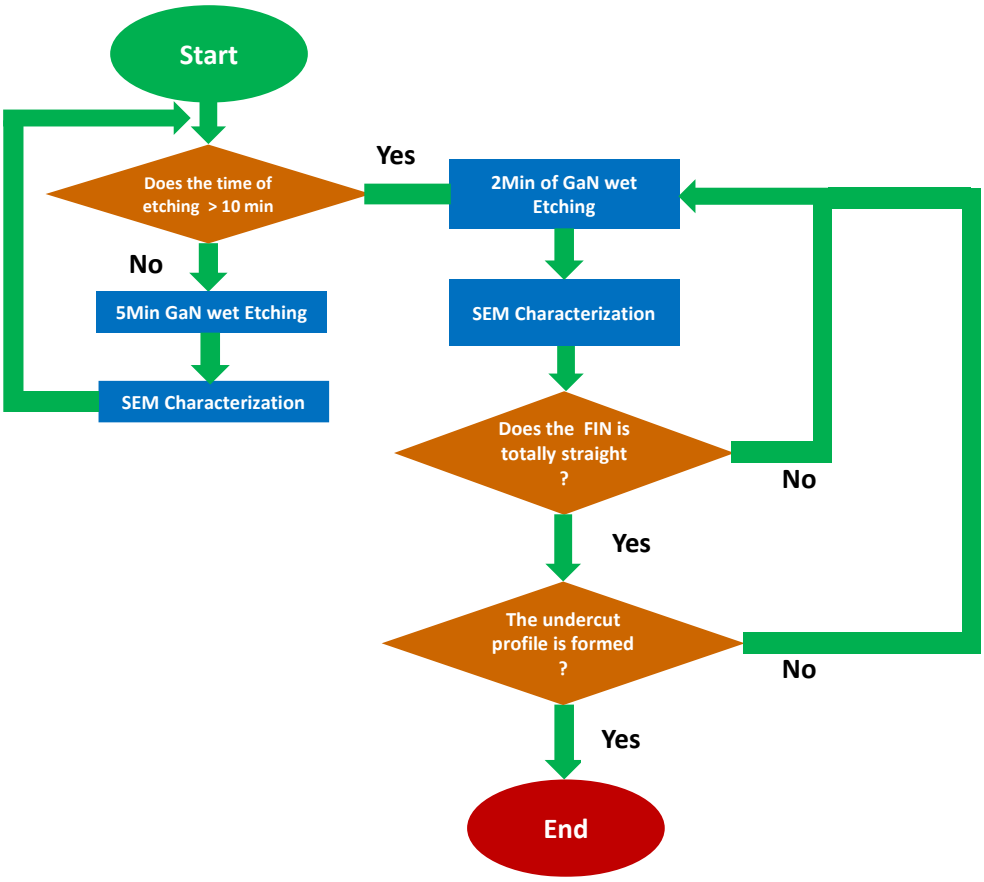

Figure 76:GaN wet etching algorithm toward post-dry etching channel engineering

6.5 Optimization of Gate metallization process (GM)

Two scenarios have been proposed and optimized for the Gate metallization processing module for the process; the first is to use electroplating. The second is to use the evaporation with rotation and angle. We optimize the electroplating process to isolate the Gate metal from the source by depositing the Seedlayer at certain places. As previously mentioned, the GaN wet etching process has been optimized to create undercut regions at FIN channel sides. This region will act as a shadowing area and block the Seedlayer from being deposited in that region. Thus, when the electroplating is carried out, only the region covered by the seed layer will be coated with the gold metal while not at the other regions. The main objective behind isolating the gate metal from the source is to decrease the C_{GS} value by increasing the space between the two contacts. The idea behind the second proposition is because the device will operate in the DC mode. Therefore, C_{GS} will be an open circuit, and there is no concern about the coupling between the source and Gate. But it must be emphasized that evaporation to deposit the gate shall be carried out with rotation and angle.

6.5.1 Optimization of Gate metallization by Electroplating:

Electroplating is an important step in microfabrication to quickly increase the thickness of undersized parts up to a few micrometers at a low cost. An optimized electroplating process can lead to a superior gate metal quality with low resistance compared to the evaporation process. Therefore, electroplating has been chosen to deposit the gate metal in our process[119]. The optimization started by depositing a Ti/Au/Ni metal stack with (20nm/200nm/20nm) thickness, respectively everywhere on 1cmX1cm silicon sample by evaporation. This metal stack will act as the seed layer for the electroplating process. A film of 1µm thick SiO_2 is then deposited everywhere in the sample by the PECVD process.

Consequently, the UV-lithography has been done using the GM mask from the testing mask, as detailed in Table 11. The advanced oxide etching machine is used to pattern the SiO_2 mask, followed by a cleaning process to strip off the resist. The configuration of the electroplating process is shown in Figure 77.

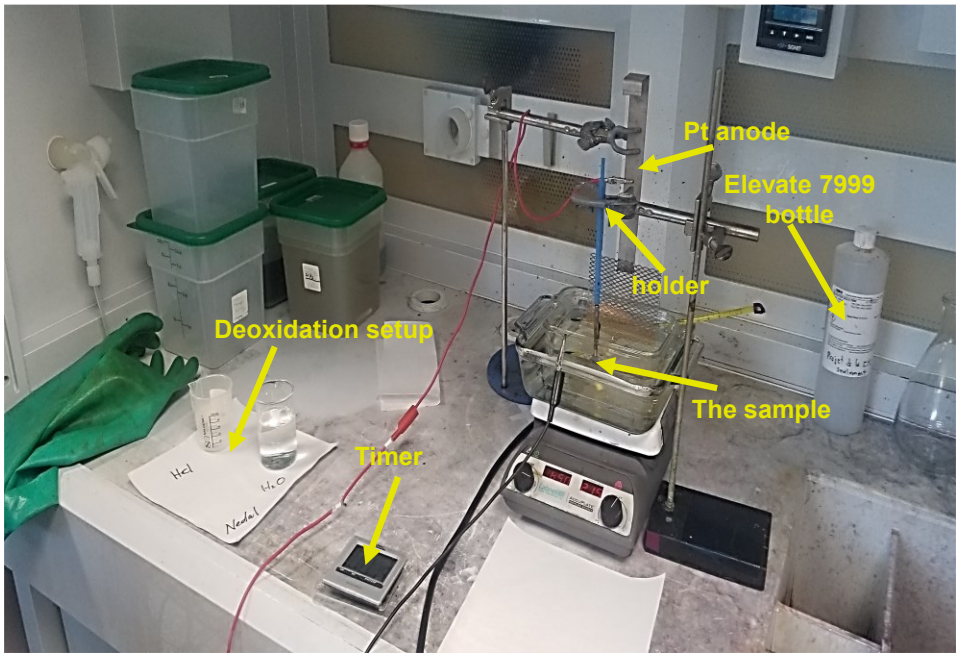

Figure 77:The electroplating process setup

The ELEVATE GOLD 7990 ST2 solution is added to an individual beaker inside a big dish of water stabilized at 55˚C. The platinum anode is connected to the source generator's positive side, configured to operate as the current source. One sample side has been attached to a tweezer connected to the cathode (negative side) and positioned

parallel with the anode using a holder. The design of the experiment starts by varying the current density 1 to 5 mA/Cm^2 with 1mA/Cm^2 step while the time of electroplating is fixed on 2 min. Since the power generator will conduct a current value, therefore, to have the desired current density, the opening area on the sample surface should be calculated for our process with a 1.2cmx1.2cm sample (patterns (1cmx1cm) +EBR area), the calculated opening area was 0.92 cm^2. Accordingly, the current value delivered from the power generated is calculated by multiplying the desired current density with the opening area. The DOE used for the electroplating optimization has been illustrated in Table 19.

Table 19:The DOE for electroplating process optimization

Test		Density of Current (mA/cm^2)	Temperature (C)	Duration (min)
1		1	55	00:02:00
		2		
		3		
		4		
		5		
		6		
2	Range between the best 2 values from test 1	()+0,2	55	00:02:00
		()+0,4		
		()+0,6		
		()+0,8		
3		Optimum value of current density	45	Optimum duration For the desired thickness
			50	
			55	
			60	
			65	
4		Optimum value of current density	Optimum value of temperature	00:01:00
				00:01:30
				00:02:00
				00:02:30
				00:03:00
				00:03:30
				00:04:00

As described in Table 19, six samples have been electroplated as in the first part of the DOE, followed by optical microscope characterization. It has been observed that the sample with 1 mA/Cm^2 current density has the worst uniformity while the sample with 4mA/Cm^2 has the best uniformity; as shown in Figure 78, the poor uniformity of the coated metal appeared again for the sample with current density equals to 5mA/cm^2.

The sample with 3mA/cm^2 is also had poor uniformity. However, the deposition uniformity for this sample is better than the one with 5mA/cm^2. Considering all the mentioned observations, the second part of the DOE was conducted using four samples (SSE#1008A-D). The current density swept from 3.4 to 4 mA/cm^2 while fixing all

other parameters as in part1. The four samples have been characterized using the optical microscope, as illustrated in Figure 79.

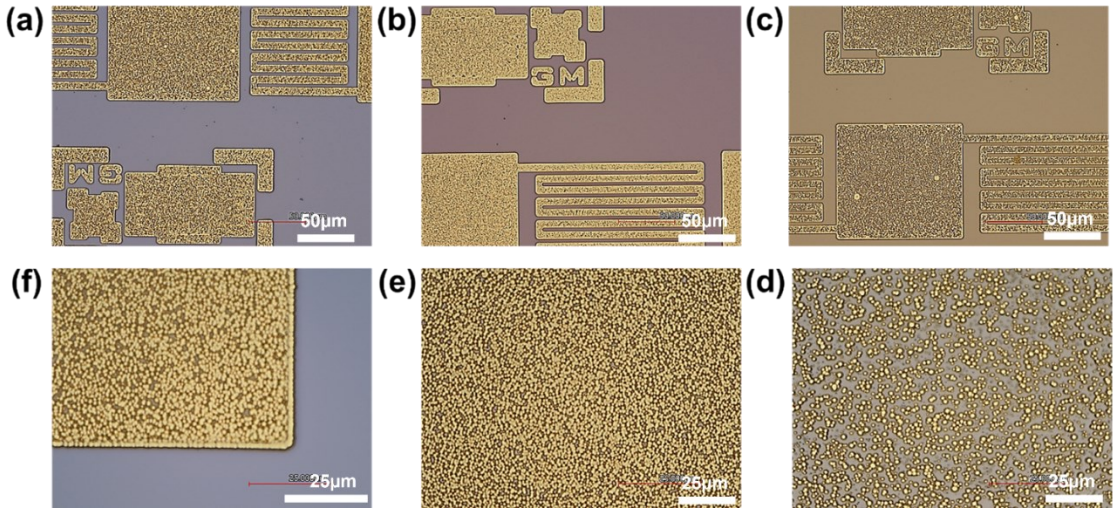

Figure 78: Optical microscope of selected samples after electroplating, a), b),and c) are the samples with current density 3mA/cm2, 4mA/cm^2,and 5mA/cm^2,respectively.D),e),and f) are the magnified image for the samples with 5mA/cm^2, 4mA/cm^2,and 3mA/cm^2, respectively.

It is observable from Figure 79 that the sample with 3.8 mA/Cm^2 has the best metal uniformity, which is in Figure 79(c). The samples with 3.6 and 4 mA/cm^2 have a lower uniformity coating than when 3.8mA/cm^2 is used.

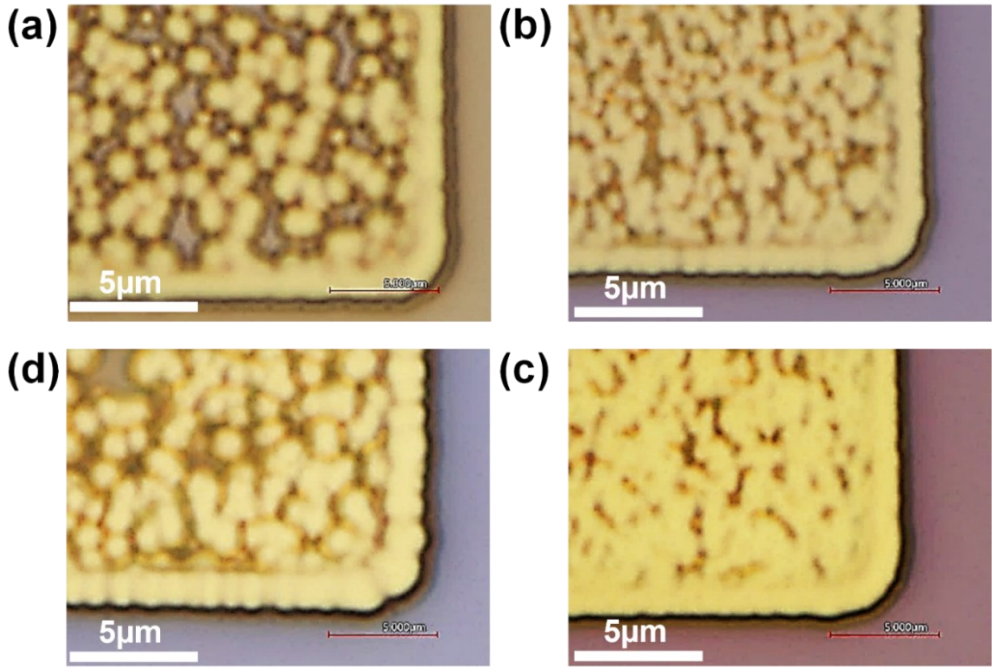

Figure 79:Optical microscope of selected samples after electroplating, a),b),c),and d) are the samples with current density 3.4mA/cm^2, 3.6mA/cm^2,3.8mA/cm^2,and 4mA/cm^2,respectively.

The samples with 3.4 mA/cm^2 and 3.8 mA/cm^2 have been characterized using SEM, as shown in Figure 80.

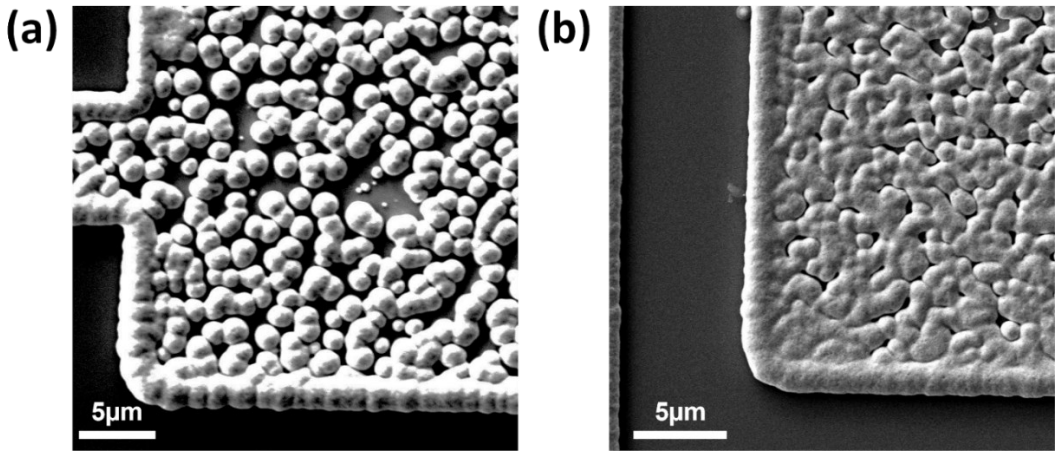

Figure 80:SEM characterization after electroplating, a)3.4mA/cm2 sample) 3.8mA/cm2 sample

Based on the SEM characterization, even for the optimal value of current density, it is worth mentioning that there is still a poor uniformity for the coated metal. This problem has been investigated in detail and might be related to the following reasons:

- ✓ The seed layer resistivity is not equal at all parts of the sample (the resistance close to the sample corner connected to the tweezer is less than the resistance at the other corner). So, it won't be easy to attract the Au+ ions from the solution toward being plated on the sample's surface.
- ✓ The electric field is not equally distributed, explicit; the coating uniformity is higher at the edge of the pads from the area far away from the edges. This means that the electric field is concentrated on the Sio2 mask while it is lower elsewhere on the sample.
- ✓ The cathode to anode ratio is very small (1:10); hence the Pt anode area is (10cmx10cm). According to the literature, the anode to cathode ratio shall be between1:1 and 1:2 to have a uniform distribution of electric field lines exiting the anode and crossing the cathode area, which is not the case in our electroplating setup[120].

A new setup has been proposed to overcome all potential problems. The sample has been stuck on the copper plate using copper tape from all sides. The plate has the same anode area. A plastic tape covers the copper plate to

avoid contaminating the solution and block coating anywhere except the sample opening areas. The tweezer is then connected to the corner of the copper plate and not explored to the solution to avoid any migration of the Au+ to the tweezer side. The new electroplating setup has been described in Figure 81.

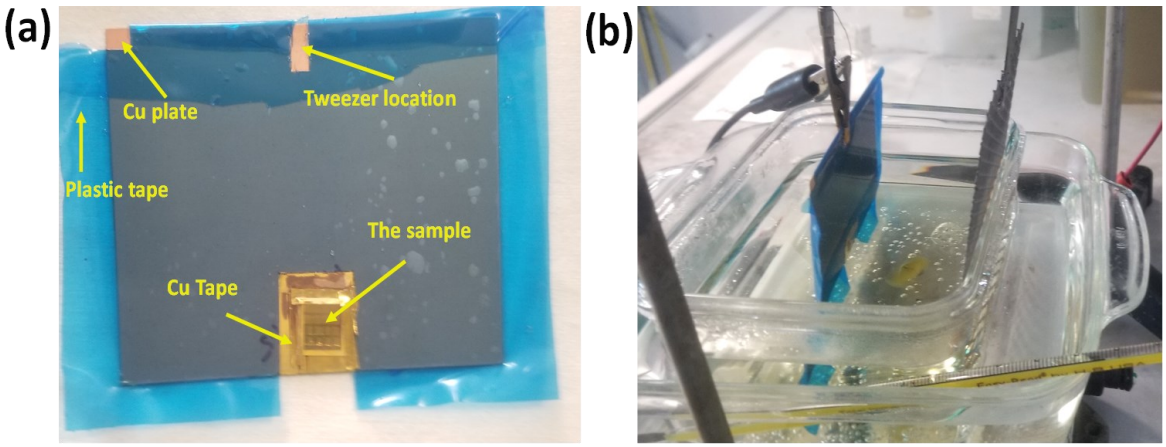

Figure 81:The new electroplating setup. a)The cathode side contents,b) the cathode to anode setup

After the electroplating has been done using the 3.8mA/cm^2 current density, it is easy to observe from the SEM characterization shown in Figure 82 for the previous and new setup that the new one exhibits a high-quality gold coating.

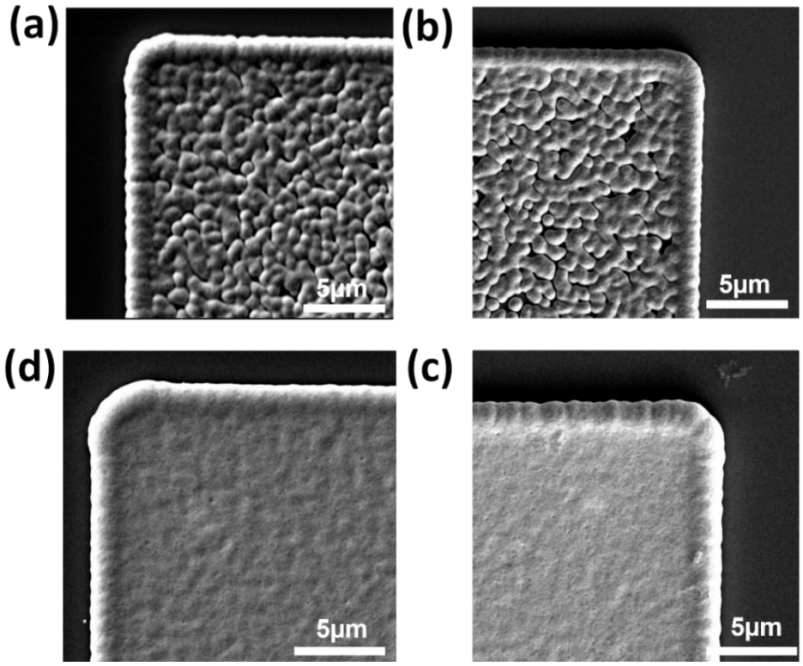

Figure 82:Comparison between old and new electroplating setup. a)The old setup pad left side,b) the old setup pad right side c) the new setup, pad right side,d) new setup, pad left side.

The SEM characterization for different patterns using the new setup is depicted in Figure 83. The patterns include the gate deposition lines, the alignment marks, and the pads for different positions.

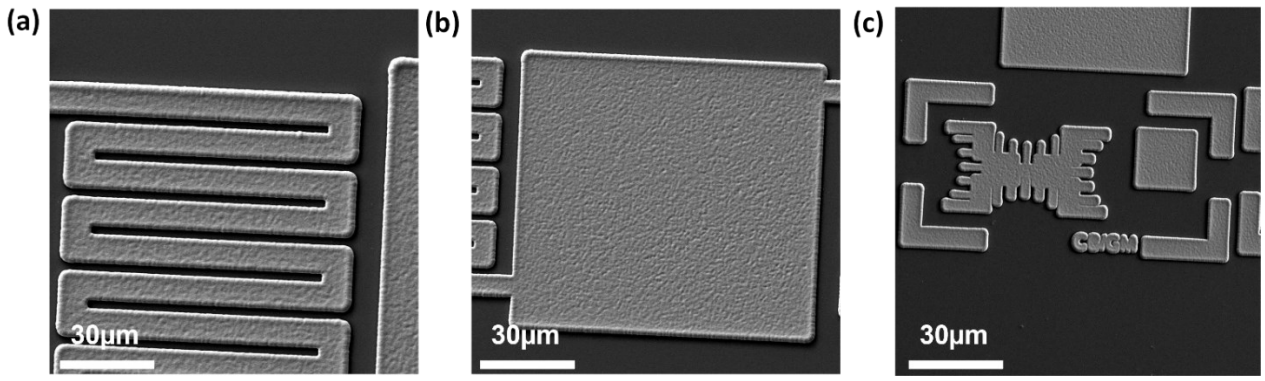

Figure 83: SEM characterization for different patterns using the new electroplating setup. a)Gate metallization, b) the gate pads and c) the alignment marks.

The thickness of the deposited film has been measured using the DEKTAK150 profilometer with 773nm thick for 2min of electroplating; therefore, the gold deposition rate is around 387nm/min.

6.5.2 Optimization of Gate metallization by Evaporation with rotation and angle:

The 2nd option to deposit the gate is by using the evaporation with rotation and angle; as all known, the evaporation process is directional; therefore, to be able to deposit the Gate metal on the FIN channel sidewalls, the sample should be evaporated with angular position from the source and with rotating status during the evaporation process. This step is already optimized and widely used in our lab. It must point out that the main motivation to use the evaporation option is that the C_{GS} value will be zero in the DC mode of operation of our device. Therefore, it will not be a source of the problem to degrade vertical GaN FinFET.

CHAPTER SEVEN: GENERAL CONCLUSIONS AND PERSPECTIVES

7.1 Conclusions générales et perspectives (en français)

En conclusion, cette thèse étudie la conception, la simulation et l'optimisation du processus de fabrication du dispositif de puissance FinFET vertical GaN normalement bloqué. La structure de départ a été construite sur la base de celle rapportée par le groupe de Sun et al. [12]. Les modèles physiques utilisés pour la simulation et l'optimisation sont ensuite calibrés sur la base de cette structure. Le processus d'optimisation intègre divers paramètres physiques et structurels et étudie leur impact sur les performances globales du dispositif. Une fois le dispositif optimisé, le processus de fabrication a été identifié; les masques d'optimisation ont été fabriqués avec un procédé dépendant entièrement de le lithographie UV. Quatre modules de traitement critiques sont respectés dans le processus d'optimisation, la détermination de l'orientation (OD), le dépôt de la source (OH), la gravure du GaN (GaN) et la métallisation de la grille (GM).

Pour le processus final, la recette EBL et le composite de l'empilement de métallisation pour le dépôt de la source ont été optimisés pour être compatibles avec tous les modules de traitement. Il a été constaté que l'utilisation d'un empilement métallique composé de Cr/Au/Cr/Ni avec 20 nm/250 nm/50 nm/130 nm sera suffisante pour notre procédé de fabrication. Il convient de mentionner que l'approche de la source en premier est une nouvelle technique et qu'elle n'a jamais été utilisée auparavant pour fabriquer le transistor FinFET vertical GaN en raison de la difficulté à identifier un empilement de métallisation de la source qui soit entièrement compatible avec tous les modules du processus de fabrication.

La procédure de détermination de l'orientation permet d'identifier précisément la zone plate de la gaufre puisque nous travaillons sur un coupon de dimensions 1cmx1cm découpé à partir de 2 pouces GaN épitaxiés/GaN avec la possibilité d'un écart de ± 2˚ par rapport à la zone plate. Pour la métallisation de la source, une combinaison d'ELL11% et de PMMA est la meilleure recette EBL pour le procédé de lift-off. De plus, le Cr/Au/Cr/Ni s'avère également être la métallisation compatible pour tous les modules du procédé de fabrication. En ce qui concerne la

gravure du GaN, la gravure sèche du GaN est utilisée pour la définition des canaux. Le système ICP-RIE (III-V) est utilisé pour cette étape. Le Groupe GaN a précédemment développé la gravure sèche du GaN dans LN2-3iT. Pour la gravure humide du GaN, différents types d'agents de gravure ont été étudiés. Enfin, nous avons réalisé que l'utilisation d'une solution de TMAH avec une concentration de 25% à 80-85°C avec une source assistée par UV est la recette optimale pour l'ingénierie des parois latérales du canal GaN FIN après l'étape de gravure sèche GaN. Avant tout processus de gravure humide de GaN, l'étape de désoxydation est nécessaire pour éliminer toute couche de GaOx, qui bloquera le processus de gravure humide en interdisant aux ions OH- d'être attirés par les ions Ga+ sur les parois latérales des canaux FIN. Pour l'étape de métallisation de la grille, nous avons identifié deux options pour déposer le métal de la grille; la première est l'électroplacage, et la seconde est l'évaporation. Pour l'électroplacage, une nouvelle configuration a été mise en place pour un dépôt d'or de haute qualité en utilisant la solution ELEVATE GOLD 7990 ST2 à une température de 55°C. Nous avons également constaté que l'utilisation de 3,8 mA/Cm^2 conduirait à un dépôt de métal exceptionnel avec une vitesse de 380 nm/min. Pour la deuxième option, le métal sera déposé par évaporation ; puisque la grille sera également déposée sur les parois latérales du canal, il est nécessaire d'effectuer le dépôt en rotation et directionnel d'une manière à rendre la paroi latérale accessible à l'accès de l'évaporation.

En général, ces efforts considérables permettent de développer et d'optimiser un procédé de fabrication à bas coût, fiable et reproductible d'un transistor vertical FinFET à base de GaN. La version optimisée de ce composant portera une amélioration considérable au niveau électrique par rapport aux autres dispositifs verticaux FinFET déjà existants dans la littérature. En outre, la comparaison entre les performances électriques selon une orientation cristalline a-GaN ou m-GaN donnerait plus de possibilités d'optimisation du procédé de fabrication en se rapprochant des valeurs théoriques de R_{ON} et le V_{BR}.Une deuxième version plus améliorée pourrait être obtenue en adaptant la structure verticale à l'hétérostructure AlGaN/GaN. En effet, une recroissance sélective par épitaxie d'une couche d'AlGaN sur les deux flancs permettrait d'améliorer la conduction de la zone du canal de transistor.

7.2 General conclusions and perspectives (English)

In conclusion, this thesis investigates the design simulation and optimization of the normally-off vertical GaN power FinFET fabrication process. The starting structure has been built based on the one reported by Sun *et al*. group [12]. The physical models used for the simulation and optimization are then calibrated based on such structure. The optimization process incorporates various physical and structural parameters and investigates their impact on the device's overall performance. After the device was optimized, the fabrication process was identified; The optimization masks were fabricated with a totally UV-lithography dependence process. Four critical processing modules are adhered to in the optimization process, the orientation determination (OD), the source deposition (OH), the GaN etching (GaN), and the gate metallization (GM).

For the final process, Both the EBL recipe and metallization stack composite for the source deposition has been optimized to be compatible with all processing modules. It has been found that using a metal stack consisting of Cr/Au/Cr/Ni with 20nm/250nm/50nm/130nm will be sufficient for our fabrication process. It is worth mentioning that the source first approach is a new technique and was never used previously to fabricate the vertical GaN FinFET transistor due to difficulty to identify a source metallization stack that is fully compatible with all process's modules.

The orientation determination procedure is found to precisely identify the flat zone of the wafer since we are working on a coupon with 1cmx1cm dimensions diced from 2 inches GaN epitaxial /GaN with the possibility of ± 2˚ deviation from the flat zone. For the Source metallization, a combination of ELL11% and PMMA is the best EBL recipe for the lift-off process. In addition, the Cr/Au/Cr/Ni is also found to be the compatible metallization for all fabrication process modules. Concerning the GaN etching, the GaN dry etching is used for channel definition. The ICP-RIE (III-V) system is used for this step. Group GaN has previously developed the GaN dry etching in LN2-3iT. For the GaN wet etching, different type of etchant has been investigated. Finally, we realized that using TMAH solution with 25% concentration at 80-85˚C with UV-assisted source is the optimum recipe for engineering the GaN FIN channel sidewalls after GaN dry etching step. Before any GaN wet etching process, the deoxidation step is necessary to remove any GaO_x layer, which will block the wet etching process by forbidding the OH- ions from being attracted by Ga+ ions on the FIN channel sidewalls. For the Gate metallization step, we have identified

two options to deposit the gate metal; the first is the electroplating, and the second is the evaporation. For the electroplating, a new setup has been set toward high-quality gold deposition using ELEVATE GOLD 7990 ST2 solution at 55˚C temperature. We also found that using 3.8mA/Cm^2 will lead to an outstanding metal deposition with a rate of 380nm/min. For the second option, the metal will be deposited by evaporation process; since the Gate will also be deposited on the channel sidewalls, it is necessary to perform the rotational and directional deposition in a way that makes the sidewall accessible to the access of the evaporation.

Overall, these fruitful efforts led to a fully optimized process to fabricate the vertical GaN FinFET transistor with low-cost and novel processing modules. The optimized version will significantly improve the classical GaN FinFET, considered version 1. Further improvement could be achieved by using vertical AlGaN /GaN in which a two-layer of AlGaN films will be grown on both channel sides by epitaxial regrowth. In addition, the capability to compare the electrical performance of a-GaN and m-GaN oriented devices will provide important information about how to optimize new versions from the device being fabricated with capable of operating within its theoretical limits concerning R_{ON} and V_{BR}.

7.3 Current and upcoming publications

This thesis concluded with several publications currently in progress or published in the near future. There are two primary reasons to postpone the publication of these results. The first is that our debut study is novel because we developed a new device with an innovative fabrication process. The group GaN (LN2-3iT) (headed by Prof. Hassan Maher) leads this cutting-edge research in Canada. Keeping the optimized fabrication process confidential until we have the first device in hand would be better. The second reason is the current COVID-19 pandemic, which led to the suspension of work in the lab for more than four months. The following publications have relevance to the thesis work:

I. **Al Taradeh, Nedal**, Eric Frayssinet, Christophe Rodriguez, Frederic Morancho, Camille Sonneville, Luong-Viet Phung, Ali Soltani, Florian Tendille, Yvon Cordier, and Hassan Maher. 2021. "Characterization of m-GaN and a-GaN Crystallographic Planes after Being Chemically Etched in TMAH Solution" Energies 14, no. 14: 4241. https://doi.org/10.3390/en14144241 (***Published***).

II. **Al Taradeh, Nedal**, Eric Frayssinet, Christophe Rodriguez, Frederic Morancho, Camille Sonneville, Luong-Viet Phung, Ali Soltani, Florian Tendille, Yvon Cordier, and Hassan Maher. "Design and Optimization of New Vertical GaN/ AlxGaN**1-x** Power FinFET Using Sentaurus TCAD software. (***In submission***).

III. **Al Taradeh, Nedal*, et al.***, " Sensitivity Analysis of Vertical GaN FinFET Design Parameters Using Sentaurus TCAD Software" (***in Progress***).

IV. **Al Taradeh, Nedal*, et al.***, "Optimization of Vertical GaN FinFET Gate Metallization Process By Electrodeposition" (***in Progress***).

V. **Al Taradeh, Nedal*, et al.***, "Fabrication and characterization of normally-off vertical GaN power FinFET using source first approach" (***in Progress***).

VI. **Al Taradeh, Nedal*, et al.***, "Characterization and analysis of a and m-GaN oriented vertical GaN power FinFET devices" (***in Progress***).

References

[1] T. Uesugi and T. Kachi, “T . Uesugi and T . Kachi , " Which are the Future GaN Power Devices for Automotive Applications , Lateral Structures or Vertical Structures ?,” in *The International Conference on Compound Semiconductor Manufacturing Technology*, 2011, no. 1, pp. 307–310.

[2] C. T. Ma and Z. H. Gu, “Review of GaN HEMT applications in power converters over 500 W,” *Electron.*, vol. 8, no. 12, 2019, doi: 10.3390/electronics8121401.

[3] M. Kanechika, T. Uesugi, and T. Kachi, “Advanced SiC and GaN power electronics for automotive systems,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 13.5.1-13.5.4, 2010, doi: 10.1109/IEDM.2010.5703356.

[4] M. A. Briere, “The power electronics market and the status of GaN based power devices,” *Tech. Dig. - IEEE Compd. Semicond. Integr. Circuit Symp. CSIC*, pp. 1–4, 2011, doi: 10.1109/CSICS.2011.6062462.

[5] A. Villamor and Z. Zong, “POWER GaN 2017 : EPITAXY , DEVICES , APPLICATIONS , AND TECHNOLOGY TRENDS 2017,” 2017.

[6] A. Longoni, E. Gatti, and R. Sacco, “Trapping noise in semiconductor devices: A method for determining the noise spectrum as a function of the trap position,” *J. Appl. Phys.*, vol. 78, no. 10, pp. 6283–6297, 1995, doi: 10.1063/1.360509.

[7] M. Meneghini, A. Tajalli, P. Moens, A. Banerjee, E. Zanoni, and G. Meneghesso, “Trapping phenomena and degradation mechanisms in GaN-based power HEMTs,” *Mater. Sci. Semicond. Process.*, vol. 78, no. October 2017, pp. 118–126, 2018, doi: 10.1016/j.mssp.2017.10.009.

[8] I. E. Fragkos, V. Dierolf, Y. Fujiwara, and N. Tansu, “Physics of Efficiency Droop in GaN:Eu Light-Emitting Diodes,” *Sci. Rep.*, vol. 7, no. 1, pp. 1–12, 2017, doi: 10.1038/s41598-017-17033-6.

[9] M. Okada *et al.*, “Novel vertical heterojunction field-effect transistors with re-grown AlGaN/GaN two-dimensional electron gas channels on GaN substrates,” *Appl. Phys. Express*, vol. 3, no. 5, pp. 3–6, 2010, doi: 10.1143/APEX.3.054201.

[10] T. Oka, T. Ina, Y. Ueno, and J. Nishii, “1.8mΩ·cm^2 vertical GaN-based trench metal-oxide-semiconductor field-effect transistors on a free-standing GaN substrate for 1.2-kV-class operation,” *Appl. Phys. Express*, vol. 8, no. 5, pp. 5–8, 2015, doi: 10.7567/APEX.8.054101.

[11] D. Ji, A. Agarwal, H. Li, W. Li, S. Keller, and S. Chowdhury, “880 V/2.7 mΩ cm 2 MIS Gate Trench CAVET on Bulk GaN Substrates,” *IEEE Electron Device Lett.*, vol. 39, no. 6, pp. 863–865, 2018, doi: 10.1109/LED.2018.2828844.

[12] M. Sun, Y. Zhang, X. Gao, and T. Palacios, “High-performance GaN vertical fin power transistors on bulk GaN substrates,” *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 509–512, 2017, doi: 10.1109/LED.2017.2670925.

[13] G. Systems *et al.*, “Gallium Nitride Semiconductor Devices Market Worth $ 4 . 3 Billion By 2025,” pp. 3–7, 2019.

[14] I. Ben-Yaacov, Y. K. Seck, U. K. Mishra, and S. P. DenBaars, “AlGaN/GaN current aperture vertical electron transistors with regrown channels,” *J. Appl. Phys.*, vol. 95, no. 4, pp. 2073–2078, 2004, doi: 10.1063/1.1641520.

[15] H. Amano *et al.*, “The 2018 GaN power electronics roadmap - IOPscience,” *J. Phys. D Appl. Phys. Top.*, vol. 51, no. 16, p. 3001, 2018, doi: http://dx.doi.org/10.1088/1361-6463/aaaf9d.

[16] B. Vassilakis and A. Cova, “Comparative analysis of GaAs/LDMOS/GaN high power transistors in a digital predistortion amplifier system,” *Asia-Pacific Microw. Conf. Proceedings, APMC*, vol. 2, 2005, doi: 10.1109/APMC.2005.1606487.

[17] R. Kucharski, T. Sochacki, B. Lucznik, and M. Bockowski, “Growth of bulk GaN crystals,” *Journal of Applied Physics*, vol. 128, no. 5. American Institute of Physics Inc., Aug. 07, 2020, doi: 10.1063/5.0009900.

[18] H. Shin *et al.*, “Comparison of the microstructural characterizations of GaN layers grown on Si (111) and on sapphire,” *J. Korean Phys. Soc.*, vol. 63, no. 8, pp. 1621–1624, 2013, doi: 10.3938/jkps.63.1621.

[19] F. M. Abou El-Ela and A. Z. Mohamed, “Electron Transport Characteristics of Wurtzite GaN,” *ISRN Condens. Matter Phys.*, vol. 2013, pp. 1–6, 2013, doi: 10.1155/2013/654752.

[20] G. Sozzi and R. Menozzi, “A review of the use of electro-thermal simulations for the analysis of heterostructure FETs,” *Microelectron. Reliab.*, vol. 47, no. 1, pp. 65–73, 2007, doi: 10.1016/j.microrel.2006.03.014.

[21] R. F. Gan, “RF GaN market :Applications, players, devices, and technologies 2018–2023,” Paris, 2018.

[22] K. Nishikawa, “GaN for automotive applications,” *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meet.*, pp. 143–150, 2013, doi: 10.1109/BCTM.2013.6798163.

[23] S. K. Yadav, J. Wang, and X. Y. Liu, “Ab initio modeling of zincblende AlN layer in Al-AlN-TiN multilayers,” *J. Appl. Phys.*, vol. 119, no. 22, Jun. 2016, doi: 10.1063/1.4953593.

[24] M. Meneghini, G. Meneghesso, and E. Znoni, *Power GaN Devices: Materials, Applications and Reliability*, 1st ed. italy: This Springer imprint, 2016.

[25] A. Villamor, “From Technologies to Market GaN Power 2018 : Epitaxy , Devices , Applications and Technology Trends,” 2018.

[26] J. He *et al.*, “On-wafer fabrication of cavity mirrors for InGaN-based laser diode grown on Si,” *Sci. Rep.*, vol. 8, no. 1, pp. 1–9, 2018, doi: 10.1038/s41598-018-26305-8.

[27] T. J. Flack, B. N. Pushpakaran, and S. B. Bayne, “GaN Technology for Power Electronic Applications: A Review,” *J. Electron. Mater.*, vol. 45, no. 6, pp. 2673–2682, 2016, doi: 10.1007/s11664-016-4435-3.

[28] C. Hemmingsson, B. Monemar, Y. Kumagai, and A. Koukitu, “Growth of III-Nitrides with Halide Vapor Phase Epitaxy (HVPE),” *Springer Handb. Cryst. Growth*, pp. 869–896, 2010, doi: 10.1007/978-3-540-74761-1_26.

[29] Y. G. Cao *et al.*, “Synthesis and Raman characteristics of hexagonal Al x Ga 1-x N alloy nanocrystalline solids through ammonothermal routes,” *Appl. Phys. A Mater. Sci. Process.*, vol. 72, no. 1, pp. 125–127, 2001, doi: 10.1007/s003390000714.

[30] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, “Recessed-gate structure approach toward normally off high-voltage AlGaN/GaN HEMT for power electronics applications,” *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 356–362, 2006, doi: 10.1109/TED.2005.862708.

[31] P. Leiderer and V. Shikin, “On the correlation between properties of multielectron dimples and bubbles,” *J. Low Temp. Phys.*, vol. 150, no. 3–4, pp. 247–251, 2008, doi: 10.1007/s10909-007-9540-5.

[32] D. H. Youn *et al.*, “Investigation on the P-ype activation mechanism in Mg-doped GaN films grown by metalorganic chemical vapor deposition,” *Japanese J. Appl. Physics, Part 1 Regul. Pap. Short Notes Rev. Pap.*, vol. 38, no. 2 A, pp. 631–634, 1999, doi: 10.1143/jjap.38.631.

[33] J. Hu, Y. Zhang, M. Sun, D. Piedra, N. Chowdhury, and T. Palacios, “Materials and processing issues in vertical GaN power electronics,” *Mater. Sci. Semicond. Process.*, vol. 78, no. July, pp. 75–84, 2018, doi: 10.1016/j.mssp.2017.09.033.

[34] S. Chowdhury, M. H. Wong, B. L. Swenson, and U. K. Mishra, “CAVET on bulk GaN substrates achieved with MBE-regrown AlGaN/GaN layers to suppress dispersion,” *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 41–43, 2012, doi: 10.1109/LED.2011.2173456.

[35] D. Cho and K. Kim, “Trench Power MOSFET using Separate Gate Technique for Reducing Gate Charge,” *J. IKEEE*, vol. 16, no. 4, pp. 283–289, 2012, doi: 10.7471/ikeee.2012.16.4.283.

[36] H. S. Kang, J. H. Seo, Y. J. Yoon, M. S. Cho, and I. M. Kang, “DC and RF analysis of geometrical parameter changes in the current aperture vertical electron transistor,” *J. Electr. Eng. Technol.*, vol. 11, no. 6, pp. 1763–1768, 2016, doi: 10.5370/JEET.2016.11.6.1763.

[37] S. Brochen, J. Brault, S. Chenot, A. Dussaigne, M. Leroux, and B. Damilano, “Dependence of the Mg-related acceptor ionization energy with the acceptor concentration in p-type GaN layers grown by molecular beam epitaxy,” *Appl. Phys. Lett.*, vol. 103, no. 3, pp. 1–5, 2013, doi: 10.1063/1.4813598.

[38] H. Obloh *et al.*, “Self-compensation in Mg doped p-type GaN grown by MOCVD,” *J. Cryst. Growth*, vol. 195, no. 1–4, pp. 270–273, 1998, doi: 10.1016/S0022-0248(98)00578-8.

[39] L. Wang, J. Zhang, L. Li, Y. Maeda, and J. P. Ao, “Plasma-assisted surface treatment for low-temperature annealed ohmic contact on AlGaN/GaN heterostructure field-effect transistors,” *Chinese Phys. B*, vol. 26, no. 3, 2017, doi: 10.1088/1674-1056/26/3/037201.

[40] A. Zubair, J. Perozek, J. Niroula, O. Aktas, V. Odnoblyudov, and T. Palacios, “First Demonstration of GaN Vertical Power FinFETs on Engineered Substrate,” *Device Res. Conf. - Conf. Dig. DRC*, vol. 2020-June, no. 3, pp. 2020–2021, 2020, doi: 10.1109/DRC50226.2020.9135176.

[41] M. Xiao, X. Gao, T. Palacios, and Y. Zhang, “Leakage and breakdown mechanisms of GaN vertical power FinFETs,” *Appl. Phys. Lett.*, vol. 114, no. 16, pp. 2–7, 2019, doi: 10.1063/1.5092433.

[42] Marie-Clara Pépin, “CONCEPTION D’ UN TRANSISTOR VERTICAL DE TYPE MOSVFET À BASE DE NITRURE DE GALLIUM,” UNIVERSITÉ DE SHERBROOKE, 2018.

[43] S. Chowdhury, B. Swenson, and U. Mishra, “Enhancement and Depletion Mode AlGaN / GaN Current Blocking Layer,” *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 543–545, 2008.

[44] N. E. Substrates and S. P. Denbaars, “(12) United States Patent Sacrificial in GaN 202 Sacrificial in GaN,” 2015.

[45] H. Huang *et al.*, “Gallium Nitride Normally-Off Vertical Field-Effect Transistor Featuring an Additional Back Current Blocking Layer Structure,” *Electronics*, vol. 8, no. 2, p. 241, 2019, doi: 10.3390/electronics8020241.

[46] W. Li and S. Chowdhury, “Design and fabrication of a 1.2 kV GaN-based MOS vertical transistor for single chip normally off operation,” *Phys. Status Solidi Appl. Mater. Sci.*, vol. 213, no. 10, pp. 2714–2720, 2016, doi: 10.1002/pssa.201532575.

[47] R. M. Abdul Khadar, C. Liu, R. Soleimanzadeh, and E. Matioli, “Fully Vertical GaN-on-Si power MOSFETs,” *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 443–446, 2019, doi: 10.1109/LED.2019.2894177.

[48] H. Nie *et al.*, “1.5-kV and 2.2-m-cm2 Vertical GaN Transistors on Bulk-GaN Substrates,” *IEEE Electron Device Lett.*, vol. 35, no. 9, pp. 939–941, 2014.

[49] I. Ben-Yaacov, Y. K. Seck, U. K. Mishra, and S. P. DenBaars, "AlGaN/GaN current aperture vertical electron transistors with regrown channels," *J. Appl. Phys.*, vol. 95, no. 4, pp. 2073–2078, 2004, doi: 10.1063/1.1641520.

[50] D. Shibata, R. Kajitani, M. Ogawa, K. Tanaka, S. Tamura, and T. Hatsuda, "1.7 kV / 1.0 mΩcm2 Normally-off Vertical GaN Transistor on GaN substrate with Regrown p-GaN/AlGaN/GaN Semipolar Gate Structure," in *016 IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 248–251, doi: 10.1109/IEDM.2016.7838385.

[51] A. Agarwal, O. Koksaldi, C. Gupta, S. Keller, and U. K. Mishra, "Demonstration of GaN Current Aperture Vertical Electron Transistors With Aperture Region Formed by Ion Implantatio," *Appl. Phys. Lett.*, vol. 111, no. 23, pp. 483–487, 2017, doi: 10.1063/1.5003257.

[52] Y. Tian *et al.*, "Direct growth of freestanding GaN on C-face SiC by HVPE," *Sci. Rep.*, vol. 5, pp. 1–8, 2015, doi: 10.1038/srep10748.

[53] Y. C. Wu and Y. R. Jhan, *3D TCAD simulation for CMOS nanoeletronic devices*. 2017.

[54] E. Zanoni, M. Meneghini, A. Chini, D. Marcon, and G. Meneghesso, "Algan/gan-based hemts failure physics and reliability: Mechanisms affecting gate edge and schottky junction," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3119–3131, 2013, doi: 10.1109/TED.2013.2271954.

[55] B. Lu and T. Palacios, "High Breakdown (> 1500 V) AlGaN/GaN HEMTs by Substrate-Transfer Technology," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 951–953, 2010, [Online]. Available: http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5518357.

[56] G. B. Stringfellow, "Thermodynamic aspects of organometallic vapor phase epitaxy," *J. Cryst. Growth*, vol. 62, no. 2, pp. 225–229, 1983, doi: 10.1016/0022-0248(83)90300-7.

[57] P. D. Dapkus, "A critical comparison of MOCVD and MBE for heterojunction devices," *J. Cryst. Growth*, vol. 68, no. 1, pp. 345–355, 1984, doi: 10.1016/0022-0248(84)90436-6.

[58] A. R. Barron *et al.*, *Chemistry of Electronic Materials*, 9th ed. Houston, Texas: Rice University, Houston, 2011.

[59] M. Kumagai, N. Uchiyama, E. Ohmura, R. Sugiura, K. Atsumi, and K. Fukumitsu, "Advanced dicing technology for semiconductor wafer - Stealth dicing," *IEEE Trans. Semicond. Manuf.*, vol. 20, no. 3, pp. 259–265, Aug. 2007, doi: 10.1109/TSM.2007.901849.

[60] W. Liu, S. Zhang, M. Stutzman, and M. Poelker, "Effects of ion bombardment on bulk GaAs photocathodes with different surface-cleavage planes," *Phys. Rev. Accel. Beams*, vol. 19, no. 10, pp. 1–8, 2016, doi: 10.1103/PhysRevAccelBeams.19.103402.

[61] M. Goorsky, *ION IMPLANTATION*, 1st editio. Rijeka, Croatia: InTech, 2012.

[62] B. L. Sharma, "Ion Implantation in Microelectronics—III-V Compounds," *IETE J. Res.*, vol. 36, no. 3–4, pp. 149–155, May 2015, doi: 10.1080/03772063.1990.11436876.

[63] D. Berkoh and S. Kulkarni, "Challenges in lift-off process using CAMP negative photoresist in III-V IC fabrication," *IEEE Trans. Semicond. Manuf.*, vol. 32, no. 4, pp. 513–517, 2019, doi: 10.1109/TSM.2019.2944133.

[64] F. S. Ozdemir, "Electron beam lithography," *Proc. - Des. Autom. Conf.*, no. December 2012, pp. 383–391, 1979, doi: 10.1109/DAC.1979.1600140.

[65] A. Merlos, M. Acero, M. H. Bao, J. Bausells, and J. Esteve, "TMAH/IPA anisotropic etching characteristics," *Sensors Actuators A. Phys.*, vol. 37–38, no. C, pp. 737–743, 1993, doi: 10.1016/0924-

4247(93)80125-Z.

[66] Y. Zhang *et al.*, “Trench formation and corner rounding in vertical GaN power devices,” *Appl. Phys. Lett.*, vol. 110, no. 19, 2017, doi: 10.1063/1.4983558.

[67] T. Wei *et al.*, “Microstructure and optical properties of nonpolar m-plane GaN films grown on m-plane sapphire by hydride vapor phase epitaxy,” *Jpn. J. Appl. Phys.*, vol. 47, no. 5 PART 1, pp. 3346–3349, 2008, doi: 10.1143/JJAP.47.3346.

[68] K. Dannecker and J. Baringhaus, “Fabrication of crystal plane oriented trenches in gallium nitride using SF 6 + Ar dry etching and wet etching post-treatment,” *J. Vac. Sci. Technol. A*, vol. 38, no. 4, pp. 3204–3208, 2020, doi: 10.1116/6.0000120.

[69] M. Tsai, B. Leung, and G. T. Wang, “Understanding and Predicting GaN Anisotropic Wet Etch Facet Evolution Practical Motivation Etch rates of c-plane GaN for various chemistries,” in *Electronic Material Conference*, 2016, no. 2011, pp. 1–26.

[70] S. J. Pearton, R. J. Shul, and F. Ren, “A review of dry etching of GaN and related materials,” *MRS Internet J. Nitride Semicond. Res.*, vol. 5, no. 2000, pp. 1–38, 2000, doi: 10.1557/S1092578300000119.

[71] M. Tautz and D. Díaz Díaz, “Wet-Chemical Etching of GaN: Underlying Mechanism of a Key Step in Blue and White LED Production,” *ChemistrySelect*, vol. 3, no. 5, pp. 1480–1494, 2018, doi: 10.1002/slct.201702267.

[72] Y. Zhang *et al.*, “Origin and Control of OFF-State Leakage Current in GaN-on-Si Vertical Diodes,” *IEEE Trans. Electron Devices*, vol. 62, no. 7, pp. 2155–2161, 2015, doi: 10.1109/TED.2015.2426711.

[73] M. F. Fatahilah, K. Strempel, F. Yu, S. Vodapally, A. Waag, and H. S. Wasisto, “3D GaN nanoarchitecture for field-effect transistors,” *Micro Nano Eng.*, vol. 3, no. December 2018, pp. 59–81, 2019, doi: 10.1016/j.mne.2019.04.001.

[74] J. M. Hwang, K. Y. Ho, Z. H. Hwang, W. H. Hung, K. M. Lau, and H. L. Hwang, “Efficient wet etching of GaN and p-GaN assisted with chopped UV source,” *Superlattices Microstruct.*, vol. 35, no. 1–2, pp. 45–57, 2004, doi: 10.1016/j.spmi.2004.03.072.

[75] R. J. Powell and G. F. Derbenwick, “Vacuum ultraviolet radiation effects in SiO 2(Vacuum UV irradiation of silicon dioxide, discussing positive charging for photon energies above threshold for electron-hole pair creation),” *IEEE Trans. Nucl. Sci.*, vol. 18, pp. 99–105, 1971.

[76] J. L. Liu *et al.*, “Status of GaN-based green light-emitting diodes,” *Chinese Phys. B*, vol. 24, no. 6, pp. 7804–7810, 2015, doi: 10.1088/1674-1056/24/6/067804.

[77] H. J. Jang, K. Joong Lee, K. W. Jo, H. E. Katz, W. J. Cho, and Y. B. Shin, “Top-down Fabrication and Enhanced Active Area Electronic Characteristics of Amorphous Oxide Nanoribbons for Flexible Electronics,” *Sci. Rep.*, vol. 7, no. 1, pp. 1–9, 2017, doi: 10.1038/s41598-017-06040-2.

[78] M. S. P. Reddy, W. S. Park, K. S. Im, and J. H. Lee, “Dual-Surface Modification of AlGaN/GaN HEMTs Using TMAH and Piranha Solutions for Enhancing Current and 1/f-Noise Characteristics,” *IEEE J. Electron Devices Soc.*, vol. 6, no. June, pp. 791–796, 2018, doi: 10.1109/JEDS.2018.2849444.

[79] B. Leung *et al.*, “Crystallographic etching of GaN : Fundamentals and applications to nanostructure synthesis,” New Mexico, 2011. [Online]. Available: https://www.osti.gov/servlets/purl/1338032.

[80] Y. Y. Lai *et al.*, “The study of wet etching on GaN surface by potassium hydroxide solution,” *Res. Chem. Intermed.*, vol. 43, no. 6, pp. 3563–3572, 2017, doi: 10.1007/s11164-016-2430-1.

[81] J. He *et al.*, “On-wafer fabrication of cavity mirrors for InGaN-based laser diode grown on Si,” *Sci. Rep.*,

vol. 8, no. 1, pp. 1–9, 2018, doi: 10.1038/s41598-018-26305-8.

[82] J. Zúñiga-Pérez *et al.*, "Polarity in GaN and ZnO: Theory, measurement, growth, and devices," *Appl. Phys. Rev.*, vol. 3, no. 4, 2016, doi: 10.1063/1.4963919.

[83] G. Nowak, X. H. Xia, J. J. Kelly, J. L. Weyher, and S. Porowski, "Electrochemical etching of highly conductive GaN single crystals," *J. Cryst. Growth*, vol. 222, no. 4, pp. 735–740, 2001, doi: 10.1016/S0022-0248(00)00988-X.

[84] J. Emsley, "Gallium," *Royal Society of Chemistry*, 2012. https://edu.rsc.org/elements/gallium/2020009.article (accessed Sep. 29, 2021).

[85] T. R *et al.*, "Self-cleaning and surface chemical reactions during hafnium dioxide atomic layer deposition on indium arsenide," *Nat. Commun.*, vol. 9, no. 1, Dec. 2018, doi: 10.1038/S41467-018-03855-Z.

[86] G. M. Jenkins, "Optical Spectrum of SO ; Radicals produced from the Photolysis of Dithionate Ions in Solution Dimeric and Tetrameric Complexes of Copper (0): a Correction Disruption of Glassy Carbon in Potassium Vapour Electron Microscopy of Muscle Phosphorylase Molecu," vol. 218, no. 1967, pp. 1967–1968, 1968.

[87] R. P. Buck, S. Singhadeja, and L. B. Rogers, "Ultraviolet Absorption Spectra of Some Inorganic Ions in Aqueous Solutions," *Anal. Chem.*, vol. 26, no. 7, pp. 1240–1242, 1954, doi: 10.1021/ac60091a051.

[88] A. Perosa, M. Selva, V. Lucchini, M. Fabris, and M. Noè, "Kinetic parameter estimation of solvent-free reactions monitored by 13C NMR spectroscopy, a case study: Mono- and di-(hydroxy)ethylation of aniline with ethylene carbonate," *Int. J. Chem. Kinet.*, vol. 43, no. 3, pp. 154–160, 2011, doi: 10.1002/kin.

[89] H. J. Quah, W. F. Lim, Z. Hassan, R. Radzali, N. Zainal, and F. K. Yam, "Effects of ultraviolet-assisted electrochemical etching current densities on structural and optical characteristics of porous quaternary AlInGaN alloys," *Arab. J. Chem.*, vol. 12, no. 8, pp. 3417–3430, 2019, doi: 10.1016/j.arabjc.2015.10.003.

[90] J. A. Bardwell, J. B. Webb, H. Tang, J. Fraser, and S. Moisa, "Ultraviolet photoenhanced wet etching of GaN in K2S2O8 solution," *J. Appl. Phys.*, vol. 89, no. 7, pp. 4142–4149, 2001, doi: 10.1063/1.1352684.

[91] S. M. George, "Atomic layer deposition: An overview," *Chem. Rev.*, vol. 110, no. 1, pp. 111–131, 2010, doi: 10.1021/cr900056b.

[92] M. Ritala and M. Leskelä, "Atomic layer deposition," *Handb. Thin Film.*, pp. 103–159, Jan. 2002, doi: 10.1016/B978-012512908-4/50005-9.

[93] A. S. H. Makhlouf and R. Rodriguez, "Bioinspired smart coatings and engineering materials for industrial and biomedical applications," *Adv. Smart Coatings Thin Film. Futur. Ind. Biomed. Eng. Appl.*, pp. 407–427, Jan. 2019, doi: 10.1016/B978-0-12-849870-5.00018-5.

[94] R. Li, Y. Cao, M. Chen, and R. Chu, "600 V/1.7 - Normally-off gan vertical trench metal-oxide-semiconductor field-effect transistor," *IEEE Electron Device Lett.*, vol. 37, no. 11, pp. 1466–1469, 2016, doi: 10.1109/LED.2016.2614515.

[95] G. Conole, M. Hall, and S. Smith, "Enabling professional communication for practitioners across Europe," *Proc. - Int. Conf. Comput. Educ. ICCE 2002*, vol. 47, no. 12, pp. 659–660, 2002, doi: 10.1109/CIE.2002.1186034.

[96] B. J. Baliga, "Power Semiconductor Device Figure of Merit for High-Frequency Applications," *IEEE Electron Device Lett.*, vol. 10, no. 10, pp. 455–457, 1989, doi: 10.1109/55.43098.

[97] B. J. Baliga, "Gallium nitride devices for power electronic applications," *Semicond. Sci. Technol.*, vol. 28, no. 7, 2013, doi: 10.1088/0268-1242/28/7/074011.

[98] J. Y. Tsao *et al.*, "Ultrawide-Bandgap Semiconductors: Research Opportunities and Challenges," *Advanced Electronic Materials*, vol. 4, no. 1. Blackwell Publishing Ltd, Jan. 2018, doi: 10.1002/aelm.201600501.

[99] S. Chowdhury and U. K. Mishra, "Lateral and vertical transistors using the Algan/GAN Heterostructure," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3060–3066, 2013, doi: 10.1109/TED.2013.2277893.

[100] A. Chakroun *et al.*, "AlGaN/GaN MOS-HEMT device fabricated using a high quality PECVD passivation process," *IEEE Electron Device Lett.*, vol. 38, no. 6, pp. 779–782, 2017, doi: 10.1109/LED.2017.2696946.

[101] D. J. Cheney *et al.*, "Degradation mechanisms for GaN and GaAs high speed transistors," *Materials (Basel).*, vol. 5, no. 12, pp. 2498–2520, 2012, doi: 10.3390/ma5122498.

[102] M. Xiao, X. Gao, T. Palacios, and Y. Zhang, "Leakage and breakdown mechanisms of GaN vertical power FinFETs," *Appl. Phys. Lett.*, vol. 114, no. 16, pp. 35–38, 2019, doi: 10.1063/1.5092433.

[103] M. Xiao, T. Palacios, and Y. Zhang, "ON-Resistance in Vertical Power FinFETs," *IEEE Trans. Electron Devices*, vol. 66, no. 9, pp. 3903–3909, 2019, doi: 10.1109/TED.2019.2928825.

[104] R. Sokolovskij *et al.*, "Precision Recess of AlGaN/GaN with Controllable Etching Rate Using ICP-RIE Oxidation and Wet Etching," *Procedia Eng.*, vol. 168, pp. 1094–1097, 2016, doi: 10.1016/j.proeng.2016.11.350.

[105] A. P. Shah, A. Azizur Rahman, and A. Bhattacharya, " Temperature-dependence of Cl 2 /Ar ICP-RIE of polar, semipolar, and nonpolar GaN and AlN following BCl 3 /Ar breakthrough plasma ," *J. Vac. Sci. Technol. A*, vol. 38, no. 1, p. 013001, 2020, doi: 10.1116/1.5123787.

[106] K. Zhu *et al.*, "Evolution of surface roughness of AlN and GaN induced by inductively coupled Cl 2/Ar plasma etching," *J. Appl. Phys.*, vol. 95, no. 9, pp. 4635–4641, 2004, doi: 10.1063/1.1688993.

[107] K. W. Kim *et al.*, "Effects of TMAH treatment on device performance of normally off Al 2O3/GaN MOSFET," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1376–1378, 2011, doi: 10.1109/LED.2011.2163293.

[108] Y. Sun *et al.*, "Optimization of mesa etch for a quasi-vertical gan schottky barrier diode (Sbd) by inductively coupled plasma (icp) and device characteristics," *Nanomaterials*, vol. 10, no. 4, 2020, doi: 10.3390/nano10040657.

[109] S. Lee *et al.*, "Smooth and selective photo-electrochemical etching of heavily doped GaN:Si using a mode-locked 355nm microchip laser," *Appl. Phys. Express*, vol. 10, no. 1, pp. 10–13, 2017, doi: 10.7567/APEX.10.011001.

[110] D. A. Stocker, E. F. Schubert, and J. M. Redwing, "Crystallographic wet chemical etching of GaN," *Appl. Phys. Lett.*, vol. 73, no. 18, pp. 2654–2656, 1998, doi: 10.1063/1.122543.

[111] D. Zhuang and J. H. Edgar, "Wet etching of GaN, AlN, and SiC: A review," *Mater. Sci. Eng. R Reports*, vol. 48, no. 1, pp. 1–46, 2005, doi: 10.1016/j.mser.2004.11.002.

[112] J. He *et al.*, "On-wafer fabrication of cavity mirrors for InGaN-based laser diode grown on Si," *Sci. Rep.*, vol. 8, no. 1, pp. 1–8, 2018, doi: 10.1038/s41598-018-26305-8.

[113] J.-Y. Hsu, "Wet Etching of P-Gan for Crystallographically Smooth Vertical Sidewalls," 2019.

[114] W. Chen *et al.*, "GaN nanowire fabricated by selective wet-etching of GaN micro truncated-pyramid," *J. Cryst. Growth*, vol. 426, pp. 168–172, 2015, doi: 10.1016/j.jcrysgro.2015.06.007.

[115] F. Horikiri *et al.*, "Simple wet-etching technology for GaN using an electrodeless photo-assisted

electrochemical reaction with a luminous array film as the UV source," *Appl. Phys. Express*, vol. 12, no. 3, 2019, doi: 10.7567/1882-0786/ab043c.

[116] Y. H. Hsieh, Y. J. Huang, J. Y. Shih, J. Leu, and K. N. Chen, "Exploring the Correspondence between Chemical States and Adhesion Property for Cr, Co Metal/AZ 4620, BCB Polymer Interface," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 8, no. 2, pp. 195–201, 2018, doi: 10.1109/TCPMT.2017.2786031.

[117] K. Eriguchi and K. Ono, "Impacts of plasma process-induced damage on MOSFET parameter variability and reliability," *Microelectron. Reliab.*, vol. 55, no. 9–10, pp. 1464–1470, 2015, doi: 10.1016/j.microrel.2015.07.004.

[118] Z. Wang, J. Ackaert, C. Salm, F. G. Kuper, and E. De Backer, "Plasma charging damage reduction in IC processing by a self-balancing interconnect," *Microelectron. Reliab.*, vol. 44, no. 9-11 SPEC. ISS., pp. 1503–1507, 2004, doi: 10.1016/j.microrel.2004.07.047.

[119] N. N. Le, T. C. H. Phan, A. D. Le, T. M. D. Dang, and M. C. Dang, "Optimization of copper electroplating process applied for microfabrication on flexible polyethylene terephthalate substrate," *Adv. Nat. Sci. Nanosci. Nanotechnol.*, vol. 6, no. 3, 2015, doi: 10.1088/2043-6262/6/3/035007.

[120] Free Online Library, "Electroplating of copper, Part 4: anode-cathode placement and secondary current distribution. -." https://www.thefreelibrary.com/Electroplating+of+copper%2C+Part+4%3A+anode-cathode+placement+and...-a0189552836 (accessed Nov. 07, 2021).