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Thermal scanning probe lithography is a direct-write patterning method that uses a heated scanning probe tip to remove thermal resist. The most widely used thermal resist is polyphthalaldehyde (PPA). Another alternative thermal resist, parylene C is introduced in this letter. It has been found that, parylene C has a wide process latitude as a thermal resist under our experimental conditions. High resolution of ~40 nm can be achieved in our optimised process. In addition, patterns in parylene layer can be transferred directly into the substrate with deep reactive ion etching without an additional hard mask, thus simplifying the fabrication process.

Introduction: The semiconductor industry has been experiencing exponential growth during the past decades, where greater integration density and higher precision of the fabricated devices are needed. As one of the crucial methods in microelectromechanical systems (MEMS) or nanoelectromechanical systems (NEMS) field, lithography has been experiencing great development. For example, electron beam lithography (EBL) provides high resolution of sub-10 nm by scanning a focused beam of electrons into a layer of electron sensitive resist to pattern custom shapes [1].

Amongst all kinds of nanolithographic methods, scanning probe lithography (SPL) has demonstrated its advantages, including low cost, rapid prototyping, 3D patterning and high patterning quality [2][3]. SPL utilises a nanometre-sharp tip to induce modifications locally and create patterns. SPL methods are manifold and can be classified by the primary interaction mechanism. For example, some SPL techniques utilise force-induced interactions, such as mechanical SPL (m-SPL); others use near-field optical techniques; or ink, such as dip-pen nanolithography (DPN); or nanoprobe coated with e.g. Pt, Au, Pd as the catalyst to trigger surface reactions [4]. The limitation of most SPL techniques lies in the slow writing speed, which has been overcome by one type of SPL, thermal scanning probe lithography (t-SPL) [3].

In t-SPL, the tip is heated to trigger the endothermic decomposition of a thermally sensitive resist and evaporation of its monomer to create a pattern in the resist. In addition to the common advantages of SPL, t-SPL is reliable in the relatively high writing speed and the simple mechanism in tip actuation, while still limited in throughput, tip degradation, and the uncertainty in tip-sample contact temperature [3][4]. The applications of t-SPL include the fabrication of room temperature single-electron transistors (SETs) based on point-contact tunnel junctions, nanofluidic rocking Brownian motors and single-nanometre master templates for nanoimprint lithography [5][6][7].

Thermal resist materials need to have high sensitivity to heat and low activation energy for thermal degradation for them to work [3][8]. The most widely used thermal resist for t-SPL process is polyphthalaldehyde (PPA) due to its outstanding temperature properties. In addition, there are other materials being studied and applied in t-SPL. For example, poly(methyl methacrylate) (PMMA), polypropylene carbonate (PPC), poly(olefin sulfones), and CSAR 92 have been used as thermal resists under certain conditions [4][8].

In this letter, another thermally-sensitive material, parylene C, is introduced as an alternative thermal resist material to PPA. The chemical structure of parylene C, namely, poly(chloro-p-xylylene), is shown in Fig. 1. Since parylene C is coated by chemical vapour deposition (CVD) rather than spin coating, the parylene C layer shows excellent conformality and uniformity. It has been found that parylene C, as a thermal resist, has a large process latitude under certain experimental conditions. In addition, the resolution has been demonstrated to reach ~40 nm. Silicon substrate can be etched with deep reactive ion etching (DRIE) using parylene directly as a mask due to the high selectivity between parylene and silicon. The characterisation of parylene C as a thermal resist is reported in the following sections.

Theory: Scanning probe lithography (SPL) creates patterns by scanning a nanometre-sharp tip over the sample to locally induce modifications [4]. In t-SPL, the modification is induced by removing thermal resist with a heated tip. Combined with other steps, the written pattern can be transferred into a certain layer.

The most widely used resist material for t-SPL, PPA, has a low ceiling temperature of ~-40°C that leads to a strong tendency to decompose into its monomers. By breaking one chemical bond with the hot tip, the whole polymer will completely unzip into its volatile monomers, which will not remain on the sample. At the same time, the endothermic nature of the reaction keeps it highly localized since there is little lateral heat spread, which is perfect for writing accurately and achieving high resolution [8].

For other materials that have been found and used as thermal resists, some of them have lower ceiling temperatures and are even more suitable for patterning, but there are other limitations like high tip contamination preventing them from being applied widely.

Parylene is the trade name for poly(p-xylylene), a kind of semicrystalline, thermoplastic polymer. There are more than 10 variants of poly(p-xylylene) commercially available these days [9]. In this paper, only one variant of them, parylene C is discussed.

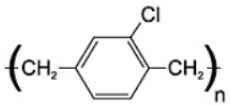

Fig. 1 *Chemical structure of parylene C, poly(chloro-p-xylylene).*

Besides being a popular material in biology, parylene C can be applied to the MEMS field because of its compatibility with micromachining processes and other advantageous properties. With high chemical inertness because of its benzene backbones, as well as the conformal, uniform deposition process, parylene C can be applied to encapsulation. At the same time, its high dielectric strength makes it an ideal material as a coating for implantable electronics [10] [11].

Parylene C has a low melting point (280°C). Theoretically, parylene C can evaporate when heated by the thermal tip, leaving behind written patterns. The glass transition point of parylene C is also low (60-90°C). The high temperature softens the polymer above its glass transition point. Upon reaching 125°C, the parylene C undergoes thermal oxidative degradation (i.e. loss of material when exposed to an oxygen-rich environment) [9].

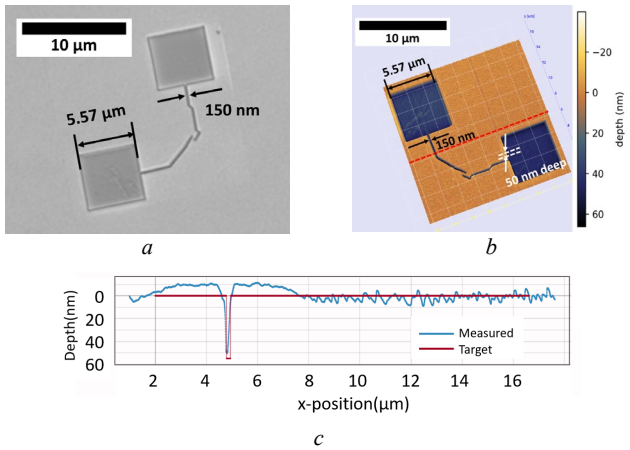

Fig. 2 *Large-area pad and narrow line patterned with parylene C.*
a Two-dimensional Leica microscope image (×150).
b Three-dimensional AFM (built in the Nanofrazor) topography image with a depth bar.
c Cross-sectional view of the topography along the red dash line in *b*, where the depth is 50 nm.

Characterisation: A 67-nm-thick layer of parylene C has been deposited on silicon substrate and a t-SPL tool, NanoFrazor (from

Heidelberg Instruments) has been used to pattern the parylene. Patterns have been drawn successfully, demonstrating the possibility of direct writing in parylene C with t-SPL. An example is shown in Fig. 2, which was carried out with the tip temperature of 1150°C and tip height of 500 nm above the sample. Fig. 2*a* and 2*b* are the optical and 3D atomic force microscopy (AFM) topography images of the designed pattern written in parylene C, respectively. It can be observed that the sidewalls are vertical and patterning depth is uniform. The depth is shown in Fig. 2*c*. Both the large-area pads (5.57 µm×5.57 µm) and the 150-nm-wide narrow line have been patterned ~50 nm deep into the parylene material. For PPA patterning, highest resolutions are achieved only for shallow patterns [12]. However, too thin resist layer cannot act directly as a mask for transferring the pattern into the substrate.

Resolution is the minimum feature dimension that can be patterned with high fidelity in a resist film on a semiconductor wafer [13]. To investigate the resolution limit of t-SPL in parylene, a resolution test has been conducted with parallel-line-array features. By changing the line widths and pitches, lines as narrow as 40 nm wide have been patterned optimally in the parylene layer. The AFM topography image is shown in Fig. 3*a*. The cross-sectional view along the red line in Fig. 3*a* is shown as the blue curve in Fig. 3*b*. The red curve in Fig. 3*b* is the target depth.

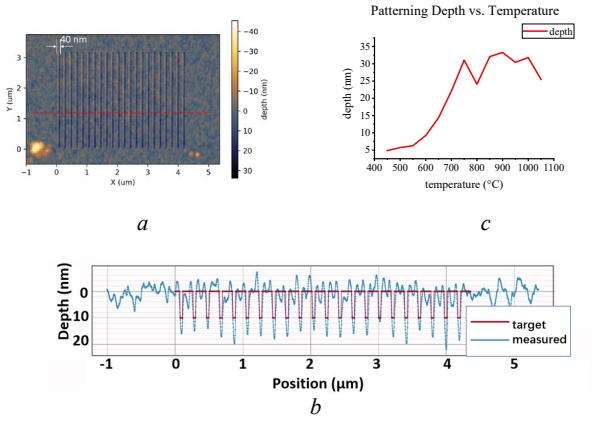

Fig. 3 *Characterisation of patterning in parylene C.*
a Three-dimensional view of the tested line-array pattern, which consists of 22 lines of the same width of 40 nm.
b Cross-sectional view along the red dashed line in a, where the red curve is the target depth and the blue curve is the real topography.
c The patterning depth of parylene C as a function of the tip temperature, where the line widths are 160nm.

The tip temperature has been found to be an important factor that affects the t-SPL performance. In addition to the patterned width of the structures, an important indicator of the process performance is the patterning depth. To investigate the relationship between the tip temperature and the patterning depth, parallel-line arrays have been drawn with varying temperatures, with the line width fixed at 160 nm. Temperatures from 450°C to 1050°C in 50°C increments have been used to test the writing performance.

The average depth of the patterned lines has been recorded as a function of temperature, as is shown in Fig. 3*c*. The patterned trenches are very shallow at low temperatures, less than 10 nm from 450°C to 600°C. In the range of 700-1050°C, the patterning depth reaches around 29±5 nm, which is a wide temperature range, indicating that parylene C has wide process latitude as a thermal resist.

Pattern transfer: Similar to other lithographic methods, the t-SPL patterned features need to be transferred into the substrate layer for fabricating MEMS/NEMS devices. In t-SPL, high resolution often involves thin layers, resulting in shallow patterning depth [12]. For PPA patterning, a silicon dioxide hard mask is needed in most cases for transferring the lithographic pattern into the silicon substrate. The high selectivity between silicon dioxide and silicon helps to amplify the etching depth.

When using parylene as a thermal resist, the oxide mask is optional, since the selectivity between the parylene and silicon is relatively high. To etch into the silicon, the selectivity can be ~30 with SF_6 and C_4F_8. In our process, the parylene layer can be deposited directly on the silicon substrate by CVD and patterned by t-SPL. After a short oxygen plasma treatment, which helps to remove the residues, the silicon is etched with deep reactive ion etching (DRIE) method using parylene directly as a mask. Finally, the residual stack is removed, leaving only the substrate with the designed pattern. The depth into silicon substrate is determined by the depth of patterned parylene layer and the etch selectivity. The process and SEM image of an example, concentric circles, are shown in Fig. 4.

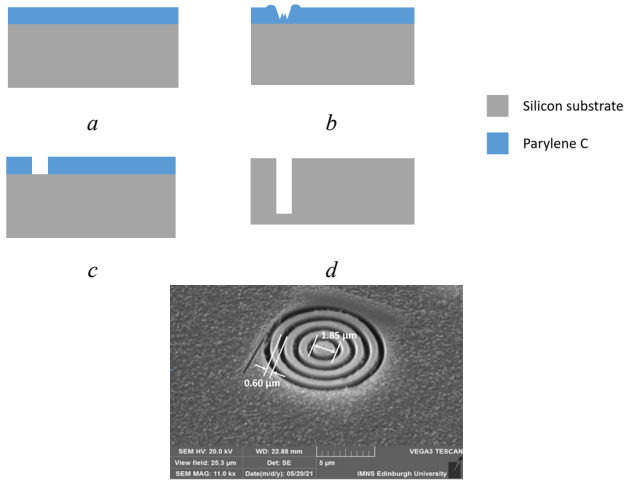

Fig. 4 *Process flow and result of transferring patterns from the parylene C resist layer into Si substrate using DRIE, parylene C used as an etch mask.*
a Parylene C deposited onto the silicon substrate by CVD.
b Parylene C thermally patterned according to the design.
c Oxygen plasma treatment to remove residual material.
d DRIE into silicon with parylene C as an etch mask.
e SEM image of concentric circles etched into silicon substrate.

Conclusion: Parylene C, an alternative thermal resist material for t-SPL is introduced and characterised in this letter, which can be deposited with great uniformity and conformality by CVD. Advantages of this new material include resolution of ~40 nm and wide process latitude (650-1050°C). Thermally patterned features can be transferred to the silicon substrate with or without a silicon dioxide hard mask.

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