Heterostructure Tunnel Diodes for Terahertz and mm-Wave applications

A Thesis submitted to the University of Manchester for the degree of

Doctor of Philosophy

In the Faculty of Science and Engineering

2021

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Contents

This thesis contains exactly 38,300 words

ABSTRACT

The primary work presented in this thesis is the development and improvement of zero-bias detector diodes, for mm-Wave and THz applications. These devices were based on Asymmetric Spacer Layer Tunnel (ASPAT) diodes made on the GaAs and InP platforms.

Accurate physical models of two state of the art ASPATs were created, which showed close agreement to experimental results obtained from ASPAT devices grown by Molecular Beam Epitaxy and processed using i-line photolithography techniques. These models were then used to develop two new novel device structures, one based on InP and one based on GaAs, in which quantum wells were added to the conventional ASPAT structures.

These new QW-ASPAT devices showed curvature coefficients of $32V^{-1}$ and $35V^{-1}$ for $In_{0.18}Ga_{0.82}As$/AlAs/GaAs and $In_{0.8}Ga_{0.2}As$/AlAs/$In_{0.53}Ga_{0.47}As$ devices respectively. This represents an increase by a factor of over 2.5 from the standard ASPAT devices. The addition of quantum wells also reduced the zero-bias capacitance of both QW-ASPAT devices. The cut-off frequencies were estimated for devices with $4\times4\mu m^2$ mesa areas, with values of 532GHz being achieved for the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs devices and over 800GHz for the $In_{0.8}Ga_{0.2}As$/AlAs/ $In_{0.53}Ga_{0.47}As$ device. These are both substantial improvements over the values achieved for the standard ASPAT diodes. The lower cut off frequencies for the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs devices are largely due to their inherently higher series resistance.

A third novel device structure based upon the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs QW-ASPAT, was also investigated. This structure used $Al_xGa_{1-x}As$ spacers to reduce the AlAs barrier height under forward bias. This new device structure allowed a zero bias curvature coefficient value of $42V^{-1}$ to be achieved. This is higher than the inherent Schottky diode limit of $40V^{-1}$ and represents the highest zero-bias curvature co-efficient achieved on a GaAs platform to date. The introduction of $Al_xGa_{1-x}As$ spacers also reduced the zero-bias capacitance of the devices when compared with the QW-ASPATs. The cut-off frequencies of $4\times4\mu m^2$ mesa area devices were estimated with

the highest value of 804GHz representing a 256% increase when compared with the standard GaAs ASPAT. As such the new device structure shows promise as a zero-bias mm-Wave and THz detector diode, achieving higher curvature coefficients than the Schottky diode as well as increasing the cut-off frequency of the ASPAT significantly.

This thesis also investigated the growth of $In_{0.53}Ga_{0.47}As$/AlAs ASPATs on GaAs substrates through the use of metamorphic buffer layers. This work is intended to take advantage of the lower cost and easier processing available to GaAs substrates compared to InP, whilst maintaining the advantages of the $In_{0.53}Ga_{0.47}As$ system. These metamorphic ASPATs (mASPAT) showed much lower detection characteristics than standard $In_{0.53}Ga_{0.47}As$/AlAs/InP ASPAT devices with cut off frequencies of 180GHz for devices with $4\times4\mu m^2$ mesa areas, mainly due to the large dislocation network in the metamorphic structure.

DECLARATION

No portion of the work referred to in the thesis has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning.

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ACKNOWLEGMENTS

I would first like to acknowledge and thank my PhD supervisor Professor Mohamed Missous, for his advice, knowledge, time and guidance over the course of my studies and research. His supervision has been invaluable and allowed me to continuously improve my knowledge throughout my PhD.

I would also like to extend my gratitude to Dr James Sexton and Dr Abdelmajid Salhi for their expertise and willingness to help during this research. I would also like to acknowledge my PhD colleagues, Saad Muttlak and Omar Abdulwahid for their friendship and contributions.

I would like to thank my parents and all my family for their unconditional support throughout my life and for encouraging me in all my endeavours. I would not be the person I am today without them.

Finally, I would like to thank my partner Hannah for her love and support which have brought me such joy in the last few years. I cannot imagine a future without her in my life.

PUBLICATIONS

1. A. Hadfield, A. Salhi, J. Sexton, and M. Missous, "Novel Barrier-Well Heterostructure Diodes for Microwave and mm-Wave Detection Applications," *Solid. State. Electron.*, p. 107963, 2021, doi: https://doi.org/10.1016/j.sse.2021.107963.

2. A. Salhi, **A. Hadfield**, S. G. Muttlak, J. Sexton, M. J. Kelly, and M. Missous, "Design and analysis of GaAs/AlAs asymmetric spacer layer tunnel diodes for high-frequency detection" Physica E: low dimensional systems and nanostructures. Volume 130, 2021, 114723, ISSN 1386-9477, https://doi.org/10.1016/j.physe.2021.114723.

3. A. Salhi, J. Sexton, S. G. Muttlak, O. Abdulwahid, **A. Hadfield**, and M. Missous, "InGaAs / AlAs / GaAs metamorphic asymmetric spacer layer tunnel (mASPAT) diodes for microwaves and millimeter-waves detection." J. Appl. Phys., vol. 194505, no. April, 2020, doi: 10.1063/5.0010369.

4. **A. Hadfield**, J. Sexton, A. Salhi, and M. Missous, "Experimentally Validated Physical Modelling of Asymmetric Spacer Layer Tunnel Diodes for THz Applications," in the 12th UK-Europe-China Workshop on Millimetre Waves and THz Technologies, 2019, pp. 47–49, doi: 10.1109/UCMMT47867.2019.9008347.

PRESENTATIONS

1. **A. Hadfield**, J. Sexton, A. Salhi, and M. Missous, “Experimentally Validated Physical Modelling of Asymmetric Spacer Layer Tunnel Diodes for THz Applications,” in the 12th UK-Europe-China Workshop on Millimetre Waves and THz Technologies, 2019 Poster Presentation.

2. **A. Hadfield**, M. Missous, “Experimentally Validated Physical Modelling of Asymetric Spacer Layer Tunnel Diodes” in the UK semiconductors conference, 2019 Oral Presentation.

3. **A. Hadfield**, M. Missous, “Experimentally Validated Physical Modelling of GaAs/AlAs Asymetric Spacer Layer Tunnel Diodes,” in the Semiconductor and Integrated Optoelectronics Conference, 2019. Oral Presentation.

4. **A. Hadfield**, M. Missous “Simulation of Avalanche Photodiodes (APDs) Integrated with Distributed Bragg Reflectors (DBRs) for Telecom and Datacom Applications” in UK semiconductors conference, 2018 Poster Presentation.

AWARDS

Best Student Poster Paper UCMMT 2019, London.

CHAPTER 1

INTRODUCTION

1.1. Terahertz and mm-Wave technologies

In the last two decades the number of people using the internet has exploded from 413 million in the year 2000 to 4 billion in 2019 [1]. This has been accompanied by large increase in the amount of data consumed across the world. It is estimated that the world data traffic will be 350 exabytes per month by 2022 [2]. This has been fuelled by the rise of video streaming, mobile communications and machine to machine communication (also referred to as the internet of things). As these technologies improve and as the number of internet users grow, the wireless internet infrastructure will need to be improved drastically to cope with the demand for high speed data transmission.

As such there has been a widescale push across the world to develop the 5th generation (5G) wireless and mobile communication networks. This is a paradigm shift in the way that cellular networks operate and not just an incremental improvement over the previous 4G LTE standard. It comprises of three new approaches. The first is the move to higher frequencies in the mm-Wave spectrum. The current microwave spectra used for cellular and Wi-Fi communications have become saturated and cannot keep up with the necessary improvements in data-rate that 5G will require. As such the 5G network will add new frequencies from the mm-Wave spectrum (30-300GHz), though operations starting at 6GHz will be used first.

These mm-Wave frequencies will be capable of higher data rates than the currently used bands [3], [4]. However, the reason they have not been previously used is due to their unfavourable transmission properties in air. The mm-Wave frequencies propagate in direct line of sight paths and are not reflected by the ionosphere. This limits the effective range of a mm-Wave communication system to a few kilometres[5]. They also suffer from atmospheric attenuation by oxygen and water vapour. This can be negated by operating in windows outside these absorption spikes.

Due to the short-range nature of these frequencies, the next part of the 5G approach is the extreme densification of cells. This could lead to cells with sub $1km^2$ areas and cells with similar ranges to Wi-Fi. This allows for greater spectral efficiency and the reuse of frequencies to send signals within an area which was previously one cell. This leads to the third area of the 5G approach which is the massive multiple-input multiple-output (MIMO) or large-scale antenna systems. The purpose of this is to allow the transmission and reception of multiple data signals over the same radio channel. This would allow for the increase in the network's capacity without the need for additional frequency bands. This is achieved by using beamforming techniques with many antennas. The move to the higher frequency mm-Wave bands is advantageous in this regard as beamforming is easier at higher frequencies and the shorter wavelength reduces the size of the antennas needed allowing for more compact systems.

Whilst 5G technology deployment is currently underway, with various enterprises demonstrating their 5G systems, there is already talk of what the next generation beyond 5G would entail [6]. As 5G increased the frequency bands used to the mm-Wave spectrum the next step would be to increase data carrier frequencies even further into sub mm-Wave frequencies in the THz regime (0.3THz - 3THz) [7].

This regime is sometimes termed the "THz gap" as it falls between mature microwave technologies in the highest frequencies of the radio spectrum and the well-developed optical engineering of infrared detectors in their lowest frequencies. THz and mm-Wave radiation have may potential applications beyond communications including non-destructive testing[8], security imaging[9], biomedical applications[10], [11] and automotive radar[12]. Figure 1.1.1 shows the output power plotted against frequency of various THz and mm-Wave radiation emitters. As can be seen from the figure there is a significant gap in the THz region from 0.3THz - 3THz.

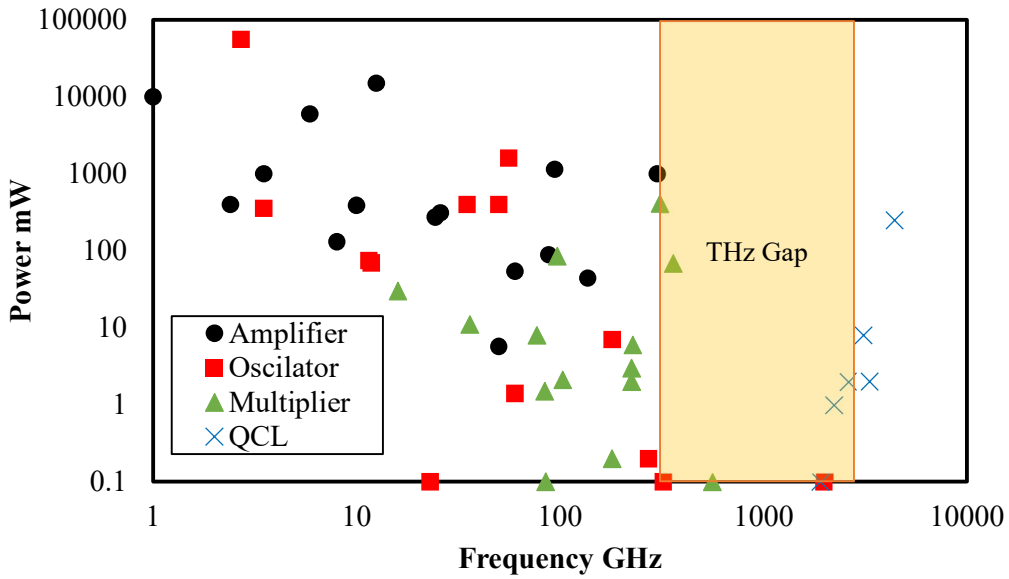

Figure 1.1.1 Output power and frequencies of different THz technologies; Amplifiers[13]–[28], Oscillators[29]–[41], Mixers [42]–[55] and Quantum Cascade Lasers[56]–[61].

Due to mm-Wave and THz radiations ability to penetrate clothing and their non-ionizing nature, they are ideal for use in airport security full body scanners and other security related fields. Imaging systems fall into two types of categories passive and active. Active systems produce a THz or mm-Wave signal and then form an image from the reflected radiative signal. Recently, Rohde & Schwarz introduced an active mm-Wave based scanner which operates at 70-80GHz to produce high resolution images with no moving parts. The system outputs mm-wave radiation at a power of 1mW[62].

Passive systems do not require a radiation source and measure the thermally emitted THz radiation of the imaged objects. This simplifies the imaging system and reduces cost however it requires a detector with low noise and a high sensitivity. The Fujitsu company has developed a passive image scanning system based around a frequency of 94GHz [63]. The sensor includes a high electron mobility transistor (HEMT), a low noise amplifier (LNA) and a zero-bias Schottky diode.

Another promising commercial application for THz and mm-Wave radiation is in the field of automotive radar [12], [64], [65]. As autonomous vehicles become more prevalent the need for the vehicle to have an accurate picture of the surrounding environment is paramount to ensure the safety of passengers and pedestrians. As such automotive radar systems have been developed to determine the distance, angle, velocity and position of nearby objects. This is achieved through the use of radio signals in the band 76-80GHz [66]. These systems when combined with active safety measures reduce the probability of accidents by being less sensitive to environmental conditions such as fog and darkness.

As such it is imperative that the THz gap is filled and that THz technologies are developed from both ends of the spectrum. These THz technologies fall into three categories sources, mixers and detectors. The purpose of sources is to generate the THz carrier frequencies in the case of communications and to provide the illumination in the case of imaging systems and radar systems. This has been one of the main blockages in the filling of the THz gap as the generation of high power THz frequencies requires large bulky systems such as gyrotrons [67] or can only be generated at ultra-low powers in the case of solid-state systems [41].

THz detectors have been created using both heterodyne and direct detection techniques. Direct detection directly demodulates the incoming signal without altering the frequency. By contrast, heterodyne detection mixes the signal with a local oscillator to down-convert the signal to a lower frequency. The signal is then demodulated from this lower intermediate frequency. This requires the use of a mixer to mix the local oscillator frequencies and the received signal. The detection process uses non-linear semiconductor devices for both the mixing and direct detection processes. It is common to use Schottky barrier diodes and complementary metal oxide semiconductors (CMOS) for these purposes, however tunnel diodes have shown recent development for this role and show promise in this area for a number of reasons as will be outlined later.

1.2. Semiconductor THz devices

The development of the Molecular Beam Epitaxy (MBE) and Metal Organic Chemical Vapour Deposition (MOCVD) techniques have allowed for the development of high-

quality semiconductor heterojunction devices to bridge the THz gap. These techniques allow for extremely well controlled semiconductor growth down to the monolayer level. This has led to the development of a large number of devices which could be used as THz emitter sources or THz and mm-Wave receivers.

MBE has been used to grow Gunn diodes and Resonant Tunnelling Diodes (RTD), which have been used to create THz and mm-Wave oscillators. Gunn diode oscillators are usually based on the GaAs platform and have achieved oscillations at 125GHz with output powers of 32mW[68]. Whilst Gunn diodes based on the InP platform have reached oscillation frequencies of over 300GHz these have been achieved with a low output power of 28μW[69].

RTDs are the current devices with the highest oscillation frequency demonstrated in the literature with the Asada group demonstrating an oscillator at 1.98THz based on the InP platform [41]. This group has also demonstrated wireless transmission rates of 34Gbit/s at a frequency of 500GHz using RTDs as the emitter [70]. Our group at the University of Manchester has recently developed RTDs capable of oscillation up to 2.7THz [33]. RTDs have also been developed on other platforms such as GaN [71] and show potential to be the leading device for compact, room temperature THz emitters.

THz detectors and mixers have been achieved using both two terminal [72]–[76]and three terminal devices[77]–[79]. Three terminal devices such as HBT and HEMT transistors require external biasing and must be fabricated at the nanoscale if they are to achieve mm-Wave operating frequencies. This increases the cost and complexity of device fabrication and is undesirable. As a result, a large number of two terminal devices have been developed using MBE and MOCVD to be used as mixers and detectors.

The current standard device is the Schottky diode created with a metal-semiconductor junction. This diode controls the flow of current with the barrier created at the semiconductor-metal interface. The main transport mechanism of the Schottky diode is thermionic emission and as such it is more susceptible to temperature fluctuations than a device which operates through quantum tunnelling. Similarly, the Schottky

diodes curvature coefficient, which is directly proportional to the voltage sensitivity, is inherently limited to $40V^{-1}$ [80].

Due to these limitations several alternative devices have been attempted. These include the Sb-Heterojunction backward diode [75], [81]–[85] which boasts curvature coefficients of $47V^{-1}$ at 94GHz making it ideal as a mm-Wave detector. However, the backward diode is not yet commercially available and utilises a complex epi-layer structure. The back diode also exhibits a junction capacitance of $15fF\mu m^{-2}$ which requires sub-micron fabrication to achieve THz and mm-Wave operation.

Another competitor to the Schottky diode is the Asymmetric Spacer Layer Tunnel (ASPAT) diode which was developed by R.T. Syme and M. J. Kelly [86] and optimized by M. Missous at the University of Manchester [87]–[89]. The ASPAT shows a greater temperature independence than the Schottky diode and a maximum curvature coefficient at zero-bias. However, it does not match the Schottky diodes curvature coefficient. The main aim of this work is to develop the ASPAT diode so that it can surpass the Schottky diode as a detector diode for mm-Wave and THz applications. To do this the devices curvature coefficient will need to be increased above $40V^{-1}$. Other improvements to the ASPATs characteristics such as reducing the junction capacitance and reducing cost will also be explored.

1.3. Thesis Outline

This work focusses on the improvement of the ASPAT diode as a zero-bias detector diode. This will be done using a combination of experimental work, in which devices will be grown in house at the University of Manchester using molecular beam epitaxy, and simulation work, in which TCAD tools such as Silvaco ATLAS and circuit simulators such as Agilent Advanced Design Systems will be used to explore new device concepts.

This chapter has introduced the demand for mm-Wave and THz technologies and briefly discussed some of the current semiconductor devices used in this area. It will also briefly outline the structure and content of the remaining thesis chapters.

Chapter 2 will focus on the background and theory of III-V semiconductors and tunnel devices. It will discuss the properties of semiconductor materials and how

semiconductor heterojunctions are formed. It will then go on to provide a brief overview of the physics of quantum and resonant tunnelling before moving on to look at specific semiconductor tunnel diodes. These diodes will include the Esaki diode, the ASPAT and the RTD. The characteristics of each of these diodes will be discussed before the chapter moves on to the applications of tunnel diodes. The use of RTD and Esaki diodes as part of THz and mm-Wave oscillator sources will be discussed and the use of ASPAT devices as direct detectors will also be covered. Finally, the chapter will discuss the use of non-linear components such as tunnel diodes as mixers for heterodyne detection systems.

Chapter 3 will cover the synthesis of semiconductor wafers and the fabrication of devices. This chapter will contain an overview of MBE and MOCVD growth techniques. Following this device fabrication techniques will be discussed. This will include photolithography, wet and dry etching techniques and metal deposition. The final part of this chapter will focus on the measurement and characterisation of devices including the components that make up the series resistance, the parasitic capacitance and inductance.

Chapter 4 will cover the modelling and simulation of devices. This will mainly be focussed on the implementation of physical models in Silvaco ATLAS TCAD software. These physical models will be used throughout this work to explore new device concepts and simulate their characteristics. The chapter will discuss the atlas file structure, syntax and methods of specifying a structure before moving on to the material and transport simulation models which will be used in this work. This chapter will also discuss the implementation of traps and defects in the model. After this the chapter will discuss the equivalent circuit models created in Agilent Advanced Design Systems (ADS) to model the devices RF parameters.

Chapter 5 will characterise the DC and RF characteristics of two well-understood ASPAT diodes grown via MBE at the University of Manchester. One GaAs/AlAs structure grown on a GaAs substrate and an $In_{0.53}Ga_{0.47}As$/AlAs ASPAT grown on an InP substrate. From this characterisation accurate physical models will be created for use in the rest of this work. These ASPATs will form the benchmark of performance against which new structures, developed in chapters 7 and 8, will be measured against.

The ASPATs in this chapter are designed for applications as part of a detection circuit for microwaves, mm-Waves and the low end of the THz spectrum.

Chapter 6 will cover the growth of $In_{0.53}Ga_{0.47}As$/AlAs ASPATs on GaAs substrates through the use of metamorphic layers. The purpose of this would be to maintain the superior qualities of $In_{0.53}Ga_{0.47}As$/AlAs ASPATS whilst removing the need for costly and difficult to work with InP substrates. The effect of the growth temperature of the metamorphic layers on the devices DC and RF characteristics will be investigated and discussed. The overall performance of the new metamorphic ASPAT (mASPAT) devices will be compared to conventionally grown $In_{0.53}Ga_{0.47}As$/AlAs ASPATs on InP substrates with the same active device structure. The physical models developed in chapter 5 will also be used as part of the analysis of the new mASPAT structures.

In chapter 7 two new diode structures with quantum wells added to the short spacer side of the device will be explored as a method of increasing the devices curvature coefficient. This will be done for both the GaAs ASPAT and the $In_{0.53}Ga_{0.47}As$ ASPAT. These new quantum-well ASPAT (QW-ASPAT) structures will be explored using the physical models developed in chapter 5. The new structures DC characteristics will be simulated, and the DC parameters extracted. Once these have been compared with the standard reference ASPATs the effects of varying the AlAs barrier thickness and quantum well thickness on the devices DC characteristics will be explored to optimize the device structure. The effect of adding quantum wells to the devices on the junction capacitance and cut-off frequency will also be explored using AC simulations of the physical models.

Chapter 8 will focus on the use of $Al_xGa_{1-x}As$ in the QW-ASPAT to reduce the barrier height on the long spacer side of the devices. These new structures will be investigated using Silvaco ATLAS by modifying the QW-ASPAT models used in chapter 7. DC simulations of the new structures will be performed, and the devices junction resistance and curvature coefficients will be extracted. The new devices parameters such as barrier thickness, quantum well thickness and $Al_xGa_{1-x}As$ composition will be explored in detail via simulation to determine their effect on the device performance. The emitter and collector layer doping and thickness will also be explored in this chapter as a method to improve the device performance. The devices C-V characteristics will also be simulated to determine the devices suitability for high

frequency detection. The cut-off frequency of the new devices will be estimated and compared with the QW-ASPAT devices from chapter 7 and the standard ASPAT devices from chapter 5.

Chapter 9 will recap the research conclusions of this work as well as providing recommendations for future work in this field.

CHAPTER 2

BACKGROUND AND THEORY OF SEMICONDUCTOR DEVICES AND TUNNEL DIODES

2.1. Introduction

This chapter will focus on the background and theory of semiconductor devices, with particular emphasis on tunnel diodes. It will initially start with explanations of the electronic band gap seen in semiconductor crystals and the formation of semiconductor homojunctions and heterojunctions. Following this, the impact of the lattice constant on constraining the material systems used will be discussed including how metamorphic and pseudomorphic layers can be used to circumvent this.

The principles of quantum tunnelling and resonant tunnelling are included in this chapter and semiconductor devices which utilise these mechanisms will be discussed. These devices include the Esaki diode, the Asymmetric Spacer Layer Tunnel (ASPAT) diode and the Resonant Tunnelling Diode (RTD). Their principles of operation will be explored, and their relevant characteristics discussed, such as negative differential resistance (NDR). To finish this section, the applications of tunnel diodes as microwave emitters and detectors will be discussed. This will include discussion on their use in higher frequency regimes such as mm-Wave and the THz regimes and the implications for higher frequency data communications technologies such as 5G.

2.2. III-V Semiconductors and Heterojunctions

2.2.1. Bandgap and Discontinuities

Semiconductors are materials which fall between traditional insulators and conductors and can therefore be influenced to act as both insulators or conductors in different circumstances. This allows them to be used to create active devices whose electrical properties can change during operation such as diodes, and transistors. Most semiconductor devices in the world today are made from silicon; however, there are

applications in which using silicon is not preferable. For example, the III-V compound semiconductors are frequently used in optoelectronic and photonic applications due to their direct bandgap, a property that silicon does not possess. These III-V compound semiconductors are crystalline compounds of group III and group V elements such as Gallium Arsenide, Aluminium Arsenide and Indium Phosphide[90], [91].

To understand semiconductors, we must consider the structure of crystalline solids. In a single atom the electrons are bound in quantum states with specific energies. The energy for two identical states in two identical atoms will be identical in normal circumstances. In the case of crystal structures, as the atoms come closer together the electronic states of the outermost electrons, and their corresponding wave functions, will begin to overlap. Since two fermions cannot have the same quantum numbers according to the Pauli Exclusion Principle[92], and electrons are fermions, the energy levels of the electrons are shifted to create a series of close energy levels with a difference of the order 10^{-22} eV[93]. As this is a very small difference, it is easier to consider these close energy levels as energy bands. There are usually considered to be 2 bands in most solids, the valence band and the conduction band. The valence band is the band of the outermost electrons of the atom and the conduction band is the next highest energy band in which electrons can freely move. A diagram of this is shown in Figure 2.2.1.

The bandgap is a left-over area between the bands in which no energy states form. The size of the bandgap is very important in determining the electrical, optical and thermal properties of crystalline solids. Materials with high bandgaps are generally insulators. Conductors often have a small bandgap or no bandgap at all as the valence and conduction bands overlap.

A semiconductor is a material in which the band gap is capable of being overcome with a small amount of help in the form of thermal energy or small applied electric field.

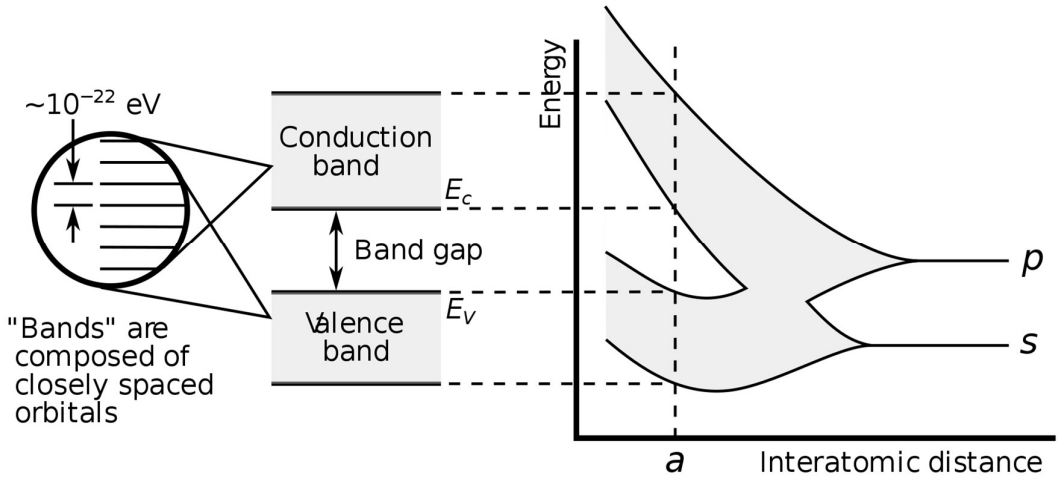

Figure 2.2.1 Diagram showing the formation of conduction and valence energy bands when interatomic distance is reduced. [90]

The position of the conduction and valence bands can be adjusted by the addition of impurities to the semiconductor. This process is called doping. In the case of silicon, a group IV element, the dopants can be group III acceptors and group V donors. The group III elements will have an additional space or “hole” in which an electron can be accepted, these holes act as positive charge carriers and hence semiconductors doped with acceptors are called p-type. Similarly, the group V dopants will have an additional free electron which can act as a negatively charged carrier and semiconductors doped with donors are called n-type. A junction is formed when n-type and p-type semiconductors are brought together. A diode for example is made of a p-type and n-type silicon junction. These types of junctions are called homo-junctions.

In an intrinsic (i.e. undoped) semiconductor, the Fermi level lies in the middle of the band gap at room temperature. The Fermi level represents the energy at which the probability of an energy state being filled is ½ according to the Fermi-Dirac distribution. When a semiconductor is doped, the position of the conduction and valance bands move in relation to the Fermi level. For an n-type semiconductor, the Fermi level is closer to the conduction band and for a p-type semiconductor the Fermi level is closer to the valence band [94].

In equilibrium the Fermi level is constant throughout the device and as such when a p-n junction is formed there is a significant difference in the conduction and valance

bands positions, relative to the Fermi level, on either side of the junction. The bands then bend smoothly at the junction so that they can meet. This is shown in Figure 2.2.1 below.

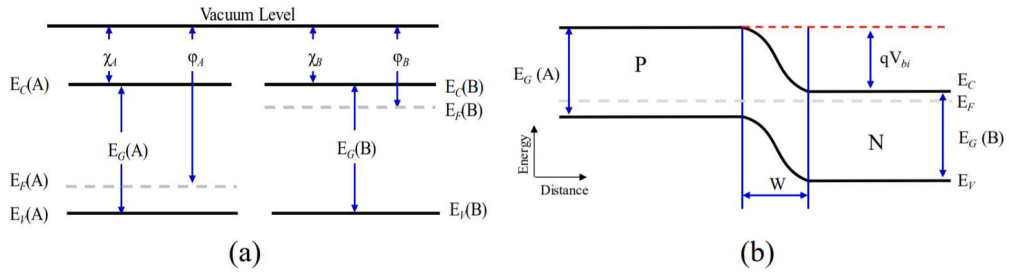

Figure 2.2.2 Homojunction between two semiconductors A and B, (a) in isolation (b) in contact. Notes: E_G = Bandgap, E_C = Conduction Band, E_V = Valence Band, V_{bi} = Built-in Potential, χ = Electron Affinity, φ =Work function.

The properties of the junctions are entirely dependent on the doping concentrations which can be varied to produce a wide range of devices. As, such homojunctions like these are used in silicon diodes, solar cells [95], light emitting diodes (LEDs)[96], [97] as well as transistors such as Bipolar Junction Transistors (BJTs)[94], [98], [99].

Where homo-junctions are created by two different doping levels of the same semiconductor, a heterojunction is created at the interface of two different semiconductors with different band gaps, irrespective of doping polarities in the two sides. Unlike homo-junctions, heterojunctions have sharp discontinuities in the bands at the junction[100]. These sharp discontinuities can be used to create barriers and wells for charge carriers and allow for different physics behaviours to be exploited such as quantum tunnelling [86]–[88], [101]–[103] and resonant tunnelling [33], [41], [104]–[106].

The behaviour of any device that utilises heterojunctions will be heavily dependent on the nature of the band gap discontinuities. It is vital that they are understood properly. The simplest method of calculating band gap discontinuities is Anderson's rule, also called the electron affinity rule, in which it is assumed that the vacuum level of the electrons on either side of the junction are aligned[107]. The electron affinity, defined as the difference between the bottom of the conduction band and the vacuum level,

and the bandgaps of the two semiconductors are then used to determine the band gap discontinuities. This is shown in Figure 2.2.3.

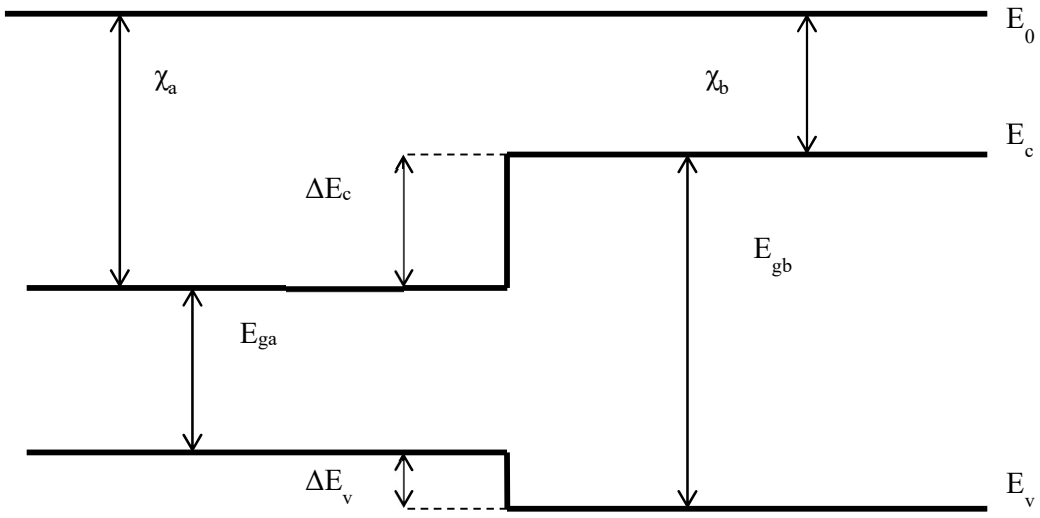

Figure 2.2.3 Diagram of Conduction and valence band offsets for two materials A and B with affinities $\chi_{a,}$ $\chi_{b,}$ and bandgaps E_{ga} and E_{gb}.

If we assume that two semiconductors, A and B with bandgaps E_{gq} and E_{gb} and affinities $\chi_{a,}$ and χ_{b} the conduction band discontinuity ΔE_c will be given by

$$\Delta E_c = (\chi_a - \chi_b)$$

2.2.1

and the valence band discontinuity will be given by

$$\Delta E_v = (\chi_a + E_{ga}) - (\chi_b + E_{gb})$$

2.2.2

From here the Femi level of both semiconductors will be calculated and band bending effects will be considered to produce the full band diagram.

There are three different types of heterojunctions[100], the most common being straddle gap or type I heterojunctions. In these heterojunctions, the conduction and

valence bands of the smaller bandgap semiconductor lie inside the bandgap of the larger bandgap semiconductor. Type II heterojunctions, also called staggered gap heterojunctions, see both the conduction and valence bands of one semiconductor lying below their corresponding bands in the second semiconductor. The final type of heterojunction is the broken gap, or type III heterojunction, in which the conduction band of one of the semiconductors is below the valence band of another. These heterojunction types are all shown below in Figure 2.2.4.

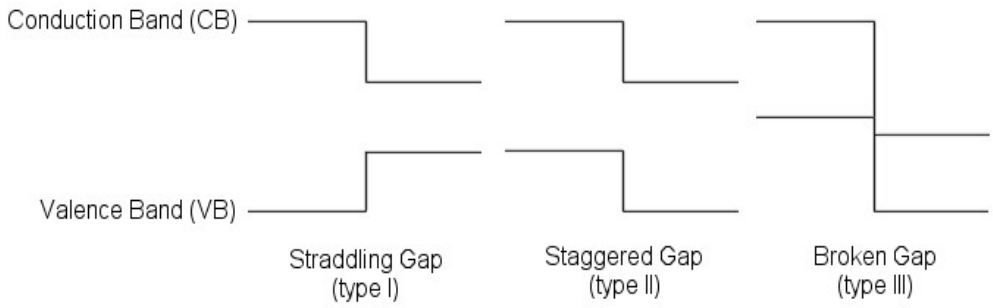

Figure 2.2.4 Diagram of Type I, Type II and Type III heterojunctions conduction and valence band alignments.

The formation of heterojunctions is usually performed using a range of epitaxial techniques, in which the semiconductor crystal is formed one atomic layer at a time. Examples of these techniques include Molecular Beam Epitaxy (MBE)[108] and Metalorganic Vapour-Phase Epitaxy (MOVPE)[109]. These methods allow for very precise control over the growth of the crystal in the vertical growth direction and allow structures to be formed that are only a few monolayers thick.

2.2.2. Lattice Matching and Pseudomorphism

Bandgap is not the only parameter to be considered when growing heterojunction structures, the lattice constant is also of vital importance. The quality of the interface between two semiconductors is determined, in a large part, by the number of dislocations the interface suffers from. To reduce these, it is imperative that the lattice constant of the two semiconductors is near identical or there will be dislocations. This condition is called lattice matching. For electronic devices, it is common to work only with semiconductors that are lattice matched to the substrate upon which the structure is grown. This is not necessarily true for photonic and optoelectronic devices, in which

the advantages of modifying the bandgap outweigh the disadvantages of an increased number of dislocations. Figure 2.2.5 depicts the lattice constants and bandgaps of various III-V semiconductors. One clear example of closely matched lattice constants is the GaAs and AlAs pair. This combination has been used to produce semiconductor devices for some time. Another less obvious combination is the ternary semiconductor alloys of InGaAs and InAlAs, where the proportion of indium is varied to match the lattice constants. It is common to lattice match these two semiconductors to the lattice constant of InP which can be used as a substrate for the growth of the epitaxial layers forming the structures. The lattice constants and bandgaps of common III-V compound semiconductors are given below in Table 2.2.1.

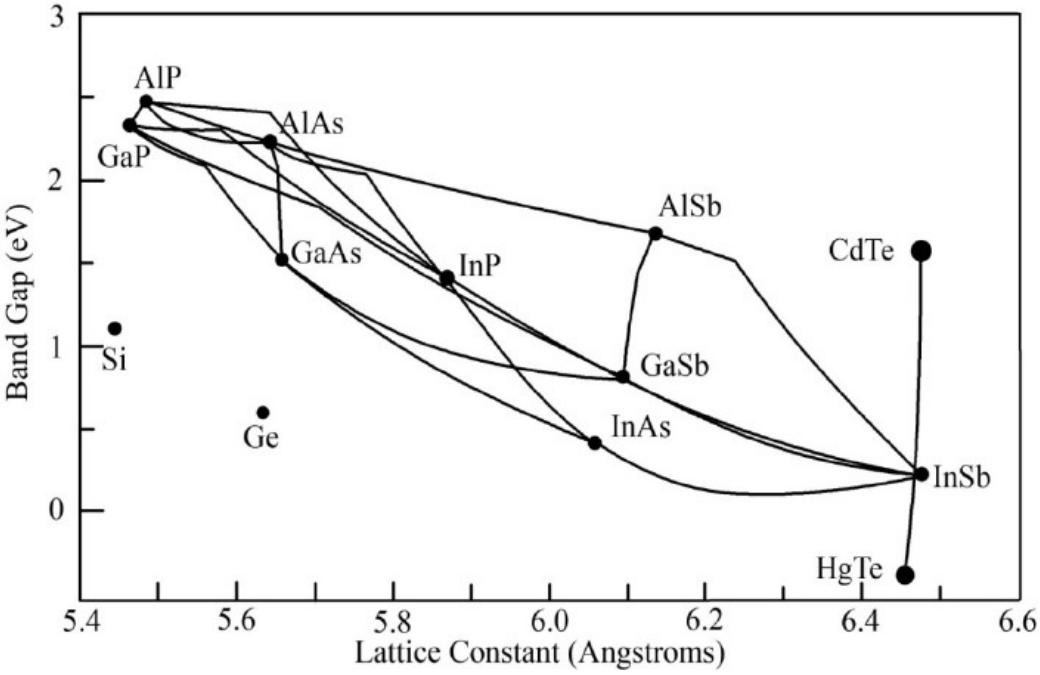

Figure 2.2.5: Lattice constant versus bandgap for III-V and group IVsemiconductors. Image from [110]

Table 2.2.1: Table of lattice constants and bandgap energies for III-V semiconductors [91], [111]–[113]

Alloy	Lattice constant, a_0 (Å)	Band gap, Eg (eV)
GaAs	5.653	1.42
AlAs	5.661	2.16
InAs	6.058	0.37

InP	5.869	1.35
$Al_{0.52}Ga_{0.48}As$	5.657	2.07
$In_{0.53}Ga_{0.47}As$	5.868	0.76
$In_{0.52}Al_{0.48}As$	5.852	1.48

Whilst choosing a lattice matched material system is preferable, it is sometimes necessary or even advantageous to grow structures with a lattice mismatch. One method of doing this is lattice grading in which the lattice alloy composition is slowly changed, from one that lattice matches the substrate to a composition with the desired lattice constant.

This technique is used in metamorphic high electron mobility transistors (mHEMTs) [114]–[116] to change the lattice constant of the structure, from that of the GaAs substrate at the bottom to the value needed by the active device on the top. This allows for the use of larger, cheaper GaAs substrates instead of more expensive and difficult to work with InP substrates.

Another example of a lattice mismatched device is the pseudomorphic high electron mobility transistor (pHEMT)[117]–[120]. Unlike the mHEMT, the pHEMT does not gradually change the lattice constant to the desired value. Instead it has a thin layer of the lattice mismatched alloy. This layer undergoes strain and its thickness must be kept below a critical thickness or dislocations will form. These dislocations will form localised states which trap electrons and holes degrading the electrical properties of the device.

The strain, ε, of a system with two lattice mismatched semiconductors can be given by

$$\varepsilon = \frac{a_0 - a_1}{a_0} \qquad 2.2.3$$

Where a_0 and a_1 are the lattice constants of the semiconductors. From, this the critical thickness, h_c, of the pseudomorphic layer can be determined simplistically by Equation 2.2.4. A more accurate determination of the critical thickness must also consider growth conditions, surface conditions and dislocation kinetics. However,

Equation 2.2.4. can be used for a simple two-layer system with a given lattice mismatch.

$$h_c = \frac{a_0}{2\varepsilon}$$

2.2.4

The use of pseudomorphic layers allows for heterojunctions to be grown with larger bandgap discontinuities than would be achievable using only lattice matched systems.

2.3. Quantum Tunnelling Principles

2.3.1. Single Barrier Quantum Tunnelling

In classical physics for a particle to pass a potential barrier, the particle must have an energy higher than the value of the barrier. It must in essence "get over" the barrier. This fundamental assumption is untrue for quantum mechanics. As particles exhibit wave like properties and are described by wave functions, there becomes a small but finite probability that a particle will simply pass through a finite potential barrier. This phenomenon is known as quantum tunnelling. For most barrier structures this is usually a small enough number to have little or no difference from the expected results of classical physics. It is only when the barrier becomes very thin that tunnelling occurs in any significant amount.

To explain this phenomenon, we must first look at the wave function of particles such as electrons travelling through semiconductor crystals. This wave function, often denoted by Ψ, contains all the relevant information of a specific particle. The evolution of the particle and its wave function is governed by the time independent Schrodinger Equation. The one-dimensional time-independent Schrodinger Equation is shown below in Equation 2.3.1

$$-\frac{\hbar^2}{2m^*}\frac{d^2\psi}{dx^2} + V(x)\psi = E\psi$$

2.3.1

Where x is the position of the particle, $m*$ is the effective mass of the particle, E is the energy of the particle and $\hbar$ is the reduced Planck's constant. After some rearranging this can then become

$$\frac{d^2\psi}{dx^2} + \frac{2m^*}{\hbar}[V(x) - E]\psi = 0$$

2.3.2

The solution to this equation will then be in the form

$$\psi = Ae^{ikx}$$

2.3.3

where k is yet to be defined. If we imagine a situation in which a particle is incident on a square potential barrier of height U_0 and width W, as shown in Figure 2.3.1, then the wave functions on both the left and the right hand sides of the barrier will be plane waves in which k is the wavenumber and can be given by

$$k = \frac{\sqrt{2m^*E}}{\hbar}$$

2.3.4

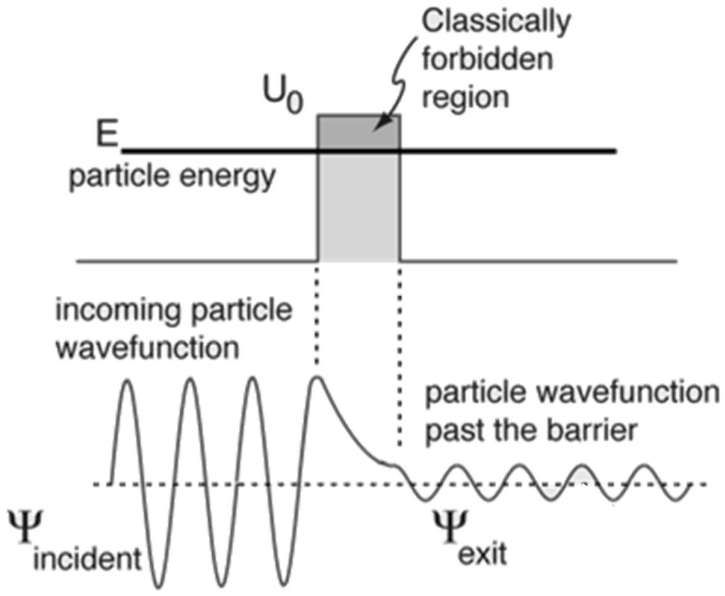

Figure 2.3.1: Wavefunctions and potential barriers of a particle tunnelling thorough a single barrier.

If we then consider the situation of the particle inside the potential barrier the wavenumber will be given by

$$k = \frac{\sqrt{2m^*(E - U_0)}}{\hbar}$$

2.3.5

In the case that the energy *E* of the electron is higher than the barrier, then the wave function will again be a simple plane wave. However, in the case that the energy of an incoming electron is lower than the barrier, the contents of the square root will be negative, and the wavenumber will become imaginary. This corresponds to an evanescent wave function which decays when in the barrier.

It is to be noted that the amplitude of the wave function does not represent the energy of the electrons and is only related to the probability of finding the electron at a particular position. To calculate the probability of tunnelling, we must find the ratio of the amplitudes of the plane waves on either side of the barrier.

If we assume that on the left of the barrier, we have

$$\psi_1 = Ae^{ikx} + Be^{-ikx}$$

2.3.6

which represents an incident wave with amplitude *A* and a reflected wave with amplitude *B*. In the barrier we will have the wave function representing two evanescent waves with amplitudes *C* and *D* where *K* is the wavenumber from Equation 2.3.5.

$$\psi_2 = Ce^{Kx} + De^{-Kx}$$

2.3.7

On the right-hand side of the barrier we will simply have the transmitted plane wave function with amplitude *F*.

$$\psi_3 = Fe^{ikx}$$

2.3.8

Since wave functions are continuous and well behaved then at the boundaries on either side of the barrier, we can say that

$$\psi_1(0) = \psi_2(0)$$

2.3.9

$$\frac{d\psi_1(0)}{dx} = \frac{d\psi_2(0)}{dx}$$

2.3.10

$$\psi_2(W) = \psi_3(W)$$

2.3.11

$$\frac{d\psi_2(W)}{dx} = \frac{d\psi_3(W)}{dx}$$

2.3.12

We can substitute our wave functions into these equations and evaluate them at $x = 0$ and $x = W$ to get

$$Ae^0 + Be^0 = Ce^0 + De^0$$

2.3.13

$$A + B = C + D$$

2.3.14

$$Aike^0 - Bike^0 = CKe^0 - DKe^0$$

2.3.15

$$CKe^{KW} - DKe^{KW} = Fike^{ikW}$$

2.3.16

From these four equations it can be shown that the ratio of the amplitudes A and F is given by

$$\frac{F}{A} = \frac{i4Kk}{(K+ik)^2 e^{-KW} - (K-ik)^2 e^{KW}}$$

2.3.17

If we assume that the barrier height is a lot higher than the energy of the particle. i.e $U_0 \gg E$ and that the barrier is wide enough that $KW > 1$ then the above equation can be simplified to

$$\frac{F}{A} \approx \frac{-i4Kk}{(K-ik)^2} e^{-KW}$$

2.3.18

To find the probability of a particle passing through the barrier we need to multiply the amplitudes by their complex conjugates. This will give us the tunnelling coefficient *T*.

$$T = \frac{F^* F}{A^* A} = \frac{(4kK)^2 e^{-2KW}}{(k^2 + K^2)^2}$$

2.3.19

The tunnelling probability is then usually given in terms of the electron energy and the barrier height as shown below

$$T = \frac{16(U_0 - E)}{{U_0}^2} e^{-2\frac{\sqrt{2m^*(E-U_0)}}{\hbar}W}$$

2.3.20

As can be seen from Equation 2.3.20, the tunnelling probability is exponentially dependent on the width of the barrier. This means that any devices which utilise quantum tunnelling must control the barrier width to a very high level of precision to ensure uniformity in the characteristics of devices across the whole device yield.

2.3.2. Double Barrier Resonant Tunnelling

Resonant tunnelling is another quantum tunnelling process in which particles pass through potential barriers similarly to the way described in the previous section. However, in the case of two potential barriers a more interesting result occurs. Let us consider a situation in which two barriers exist separated by a distance, *a*, the barriers will have transmission and reflection coefficients $t_1,\ t_2$ and r_1, r_2.

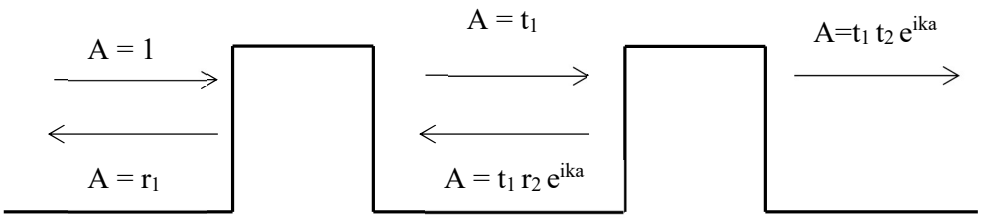

Figure 2.3.2: Amplitudes of wavefunctions for particles travelling through a double barrier resonant tunnelling structure with transmission and reflection coefficients. $t_1,\ t_2$ and r_1, r_2.

Now let's consider a particle travelling towards the double barrier structure. This particles wave function will essentially be that of a plane wave as described by

$$\psi = Ae^{ikx-\omega t}$$

2.3.21

Where *A* is an arbitrary constant, *k*, is the wavenumber and *ω* is the angular frequency. Now consider the form of the waves after passing through the barrier structure. These will be similar to the form given by Equation 2.3.21 but with the amplitude multiplied by some factor. The first case is a wave which passes straight through the barrier as shown in Figure 2.3.2. This will have an amplitude of

$$A = t_1 t_2 e^{ika}$$

2.3.22

where *ka* is the phase change of a particle with energy $E = {\hbar^2 k^2}/{2m}$ after travelling a distance *a*.

Now consider the case in which a particle tunnels through the first barrier, is reflected by both barriers inside the quantum well and then tunnels through the second barrier to leave the structure. In this case the Amplitude will be given by

$$A = t_1\, t_2\, r_1\, r_2\, e^{i3ka}$$

2.3.23

This is because it has tunnelled through both barriers once and been reflected by both barriers once. The phase change is 3ka as the particle has travelled the length of the well three times. This can also be done for the case in which the particle reflects off both sides twice to give and amplitude of

$$A = t_1\, t_2\, {r_1}^2\, {r_2}^2 e^{i5ka}$$

2.3.24

This can go on indefinitely with more internal reflections being added.

Due to the theory of superposition the amplitude for the particles which tunnel through both barriers can be found through summing the amplitude for all cases to give.

$$t = t_1 t_2 e^{ika} + t_1\, t_2\, r_1\, r_2\, e^{i3ka} + t_1\, t_2\, {r_1}^2\, {r_2}^2 e^{i5ka} + \cdots$$

$$= t_1 t_2\, e^{ika} \sum_{n=0}^{n=\infty} (r_1\, r_2\, e^{i2ka})^n$$

2.3.25

This is the sum of a geometric series and as such can be written as

$$t = t_1 t_2\, e^{ika} \left[\frac{1}{(1 - r_1 r_2 e^{i2ka})}\right]$$

2.3.26

In quantum mechanics the transmission probability, T, for both barriers is given by the squared modulus of the total amplitude t. Therefore

$$T = |t|^2 = \frac{|t_1|^2|t_2|^2}{1 + |r_1|^2|r_2|^2 - 2|r_1||r_2|\cos\Psi}$$

2.3.27

Where $\Psi = 2ka + \psi r_1 + \psi r_2$. This is the phase change due to the additional travel time when being reflected and the inherent phase change that occurs with reflection. Clearly Equation 2.3.27 is maximised when $\cos\Psi = 1$. This occurs when $\Psi = 2ka + \psi r_1 + \psi r_2 = 2n\pi$. Where n is an integer. This can be thought of as the case when all the contributions for multiple reflections are in phase and combine constructively. If the barriers are of equal thickness so that $t_1 = t_2$ and $r_1 = r_2$ then the transmission probability on resonance is given by

$$T_{resonance} = \frac{|t_1|^4}{(1 - |r_1|^2)^2}$$

2.3.28

Since $|t_1|^2 + |r_1|^2 = 1$ this becomes

$$T_{resonance} = \frac{|t_1|^4}{|t_1|^4} = 1$$

2.3.29

This is a remarkable result which shows that provided the incoming electron or particle has a wavenumber and therefore energy that matches the resonance condition the probability that it will pass through the barrier structure is 100%. This wave number corresponds to the same wavenumber of the confined energy states of the well between the two barriers.

2.4. Tunnel Diodes

2.4.1. Esaki Diodes

The Esaki diode was the first tunnel diode to be invented and won Leo Esaki, after which it is named, the Nobel prize in 1973 [121]. This diode was based on an extremely highly doped p-n junction with a very thin depletion region and overlapping valence and conduction bands. As the diode is biased, band to band tunnelling occurs and electrons tunnel between the n-type conduction band and the p-type valence band.

The Figure 2.4.1 below shows the band structure and current voltage curve of an Esaki diodes. When the device is reverse biased at point a) the electrons from the p-type valence band tunnel into the n-type conduction band. At point b) at zero bias the device is in equilibrium and no current flows. When the device is first forward biased the electrons tunnel from the n-type conduction band to the p-type valence band. As the device is further biased at point c) the p-type valence band becomes misaligned with the n-type conduction band and no tunnelling can occur leading to a drop in the current of the device. This continues to happen until the voltage is high enough for standard current flow to occur in the same manner as all p-n junctions at point d). After this the diode behaves in the same manner as a standard p-n junction e).

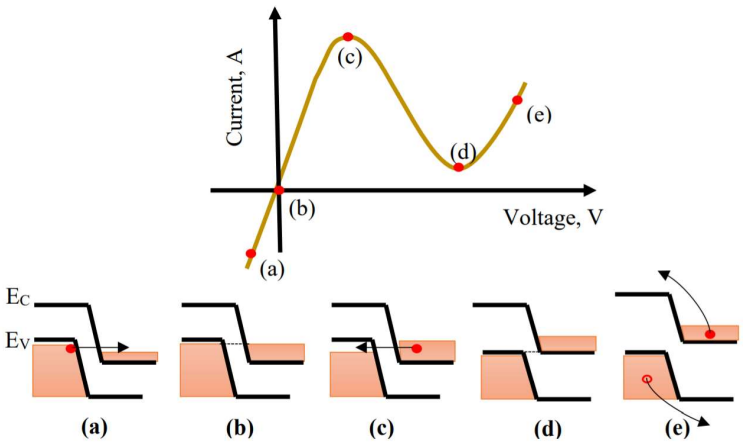

Figure 2.4.1 Current-Voltage characteristic and band diagram of an Esaki diode at different bias points. a) reverse bias, b) zero-bias c) peak bias d) valley bias e) forward bias.

The interesting piece of physics in this device is the current drop as the voltage increases after the n-type conduction band to the p-type valence band are no longer aligned. This is a negative differential resistance and the uses of negative resistances will be explored later in the chapter.

2.4.2. ASPAT Devices

As discussed before, when two dissimilar semiconductors are brought together as a heterojunction, band gap discontinuities can form. These band gap discontinuities can be used to create potential barriers such as those seen in section 2.3.1. These potential barriers can then be used as part of active devices. One example of such a device is the Asymmetric Spacer Layer Tunnel Diode (ASPAT). This device, first invented in 1992 by Syme and Kelly [86], comprises of a single very thin barrier (of the order a few nm) sandwiched between two layers of intrinsic semiconductor. The two intrinsic layers are spacers from the doped layers used for contacts and carrier providers. These layers are asymmetric in thickness with a typical ratio of 40:1.

As can be seen from Figure 2.4.2, under forward bias the electrons accumulate at the base of the barrier in the small triangular quantum well. From here the electrons can either jump over the barrier via thermionic emission or tunnel through the barrier providing a current. Under reverse bias conditions this accumulation layer does not form and so the current is significantly reduced giving rise to an asymmetric current voltage curve as shown in Figure 2.4.3. This asymmetric behaviour allows for the ASPAT to behave as a rectifying diode.

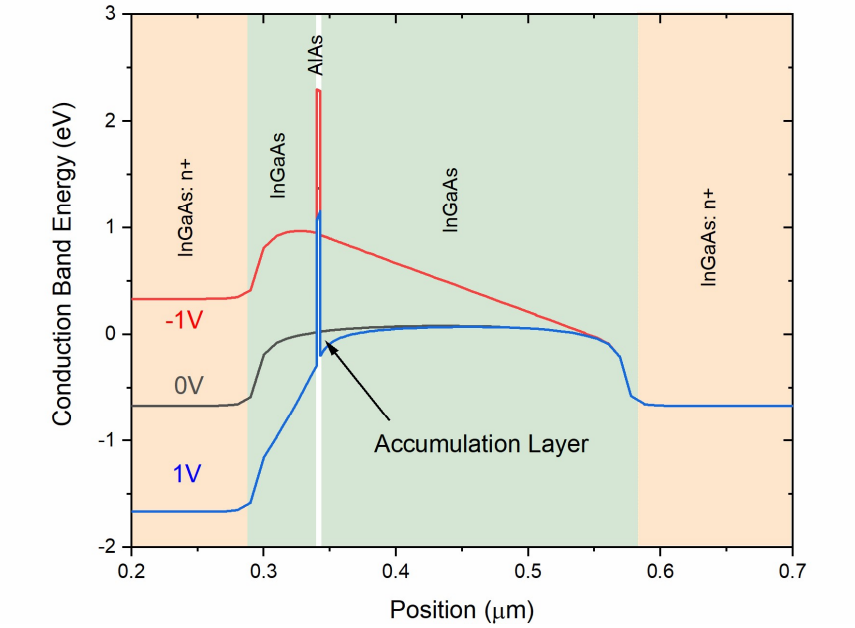

Figure 2.4.2 Conduction band diagram of an InGaAs ASPAT diode under forward and reverse bias conditions showing the formation of an accumulation layer.

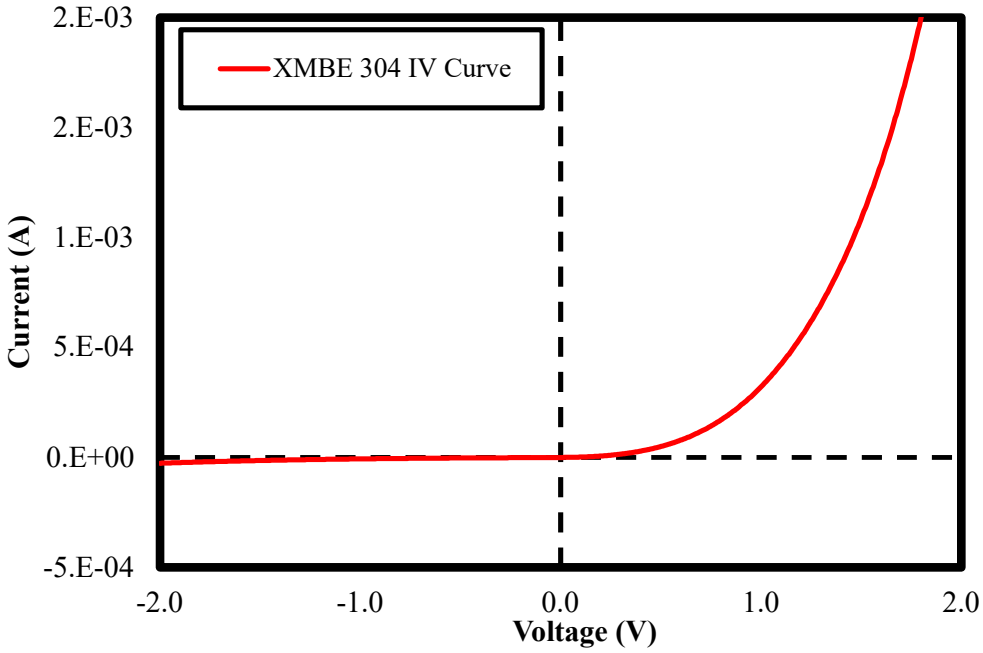

Figure 2.4.3 Measured current-voltage curve form -2V to 2V for a GaAs/AlAs ASPAT diode denoted XMBE304.

The current-voltage curve for the ASPAT diode can be determined theoretically by solving the Schrodinger and Poisson equations. To do this we make the assumptions

that the tunnelling is only from the accumulation layer and only through the direct gamma valley of the bandgap. The current in the x and y directions is taken to be uniform reducing the problem to a one-dimensional solution of the Schrodinger equation in the z direction.

$$-\frac{\hbar^2}{2m^*}\frac{d^2\psi}{dz^2} + e(\phi - \Delta\phi)\psi = E_z\psi$$

2.4.1

where is (ϕ) the potential at point $\boldsymbol{z}$, and ($\Delta\phi$) is a correction term which reduces the effective barrier height and can be neglected since there is virtually no band bending when the bias (V) increases. The current density in the z-direction (J_z) is then calculated by solving Equation 2.4.1 at different values of E_z. Thus, J_z is expressed as:

$$J_z = \frac{-e\hbar}{2m^*}\left(\psi^*\frac{d\psi}{dz} - \psi\frac{d\psi^*}{dz}\right)$$

2.4.2

Due to the heavily doped contacts on either side of the barrier the wavefunction can be described as plane waves as was shown earlier in the chapter for single barrier tunnelling. Thus giving

$$\psi_L = e^{ik_l z} + Re^{-ik_l z}$$

2.4.3

$$\psi_R = Te^{ik_R z}$$

2.4.4

From here T and R can be found using a transfer matrix method for all possible values of E_z. If this is then multiplied by the fermi function

$$f(E) = \frac{1}{1 + e^{\left(\frac{E_Z - E_F}{k_B T}\right)}}$$

2.4.5

and integrated across all possible energy values a final expression of the current density is achieved.

$$J_z = \frac{em^* k_B T}{2\pi^2 h^3} \int_0^\infty T(E_z) \ln\left\{ \frac{1 + e^{\left(\frac{E_F - E_z}{k_B T}\right)}}{1 + e^{\left(\frac{E_F - \mathrm{eV} - E_z}{k_B T}\right)}} \right\} dE_z$$

2.4.6

Current ASPATs are typically made using AlAs barriers and either GaAs or InGaAs as the main semiconductor. In the case of InGaAs the percentage of Indium is typically 53% to lattice match it to InP which is typically used as a substrate for the growth. These ASPATs are grown using the Molecular Beam Epitaxy (MBE) technique in which the semiconductor crystal is grown in a vacuum, with semiconductor elements heated to the point that they sublime into atoms. These atoms then condense on the substrate growing the crystal.

It is necessary to use MBE to grow ASPAT structures to control the barrier layer thickness. As discussed earlier, quantum tunnelling is exponentially dependent on the width of the barrier. It has been shown in simulations that for an AlAs barrier a single monolayer difference results in a 270% difference in current in the device [101], [102]. As industry requires devices with a variation of less than 15% the control of the barrier thickness is one of the key barriers preventing large scale manufacture of ASPAT diodes. However, recent work has shown that through careful growth, a 1% variation across the wafer can be produced and a 1% variation from wafer to wafer [101]. Allowing for the possibility that ASPATs and other tunnel diodes may be manufactured in large scales in the future.

The ASPAT has potential applications as part of a detection circuit for both microwaves, millimetre waves and the low end of the THz spectrum. Current ASPATs are comparable to Schottky and Planar doped diodes in terms of dynamic range, low noise performance, and have a comparable transfer function[88]. The ASPAT diode is especially suited to zero bias detection and due to the fact that the main carrier process is quantum tunnelling and not thermionic emission, the ASPAT shows a much-reduced temperature dependence[87] allowing it to be used in applications in which temperature insensitivity is a key requirement.

2.4.3. Resonant Tunnelling Diodes

An example of a typical RTD structure is the double barrier quantum well which consists of an undoped quantum well of low bandgap semiconductor (GaAs, InGaAs, etc) sandwiched between two thin barriers of high bandgap semiconductor (AlAs, InAlAs, etc). This creates a band diagram similar to the potential barrier shown in Figure 2.4.4.

Most RTD structures created with III-V semiconductors are created using molecular beam epitaxy (MBE)[33], [122] to deposit layers of semiconductor with high precision. This is of key importance as the barrier widths have a large impact on the tunnelling probability. MBE techniques allow for control of the crystal growth to the atomic monolayer level. Some RTD devices have been created using metal-organic vapour phase epitaxy (MOVPE)[123], however MBE remains the most common method of growth for RTD devices.

To further understand RTDs. we must look at the effects of biasing the RTD. Figure 2.4.4 shows the band diagram for an RTD under various bias points as well as the I-V characteristics of the RTD.

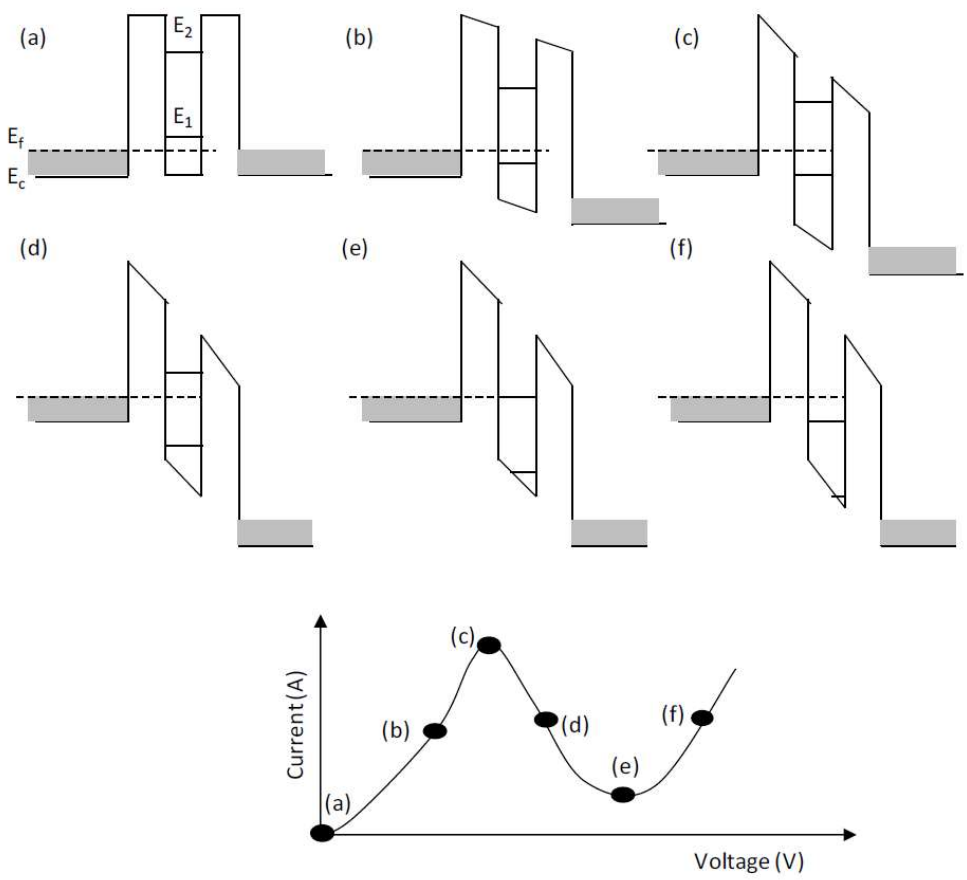

Figure 2.4.4: RTD band diagrams and IV characteristics at various bias points. a) zero-bias c) peak bias e) valley bias f) forward bias. b) and d) are intermdeiate bias points. [124]

At zero bias (point (a)) the electrons on either side of the barrier act as a Fermi gas populating the energy levels up to the fermi level. As the fermi level is below the first resonant energy E_1 the electrons cannot tunnel through the barrier. In this condition no current flows. As the voltage is increased, a small current flows as the resonant energy drops below the fermi level allowing electrons to tunnel across the structure (b). When the resonant level is at the same energy as the conduction band on the emitter (left) side of the device the current due to tunnelling is at a maximum (c). This is the peak voltage of the RTD. After the resonant level falls below the conduction band the current falls again (d) to a minimum (e). After this point electrons gain the necessary kinetic energy to overcome the barrier and current again starts to rise until the second resonant level allows electrons to tunnel through the barrier (f). After this

point the voltage is high enough that the main current mechanism is through thermionic emission.

If we look at the I-V curve of the RTD in Figure 2.4.4 the current decreases as the voltage increases between the peak voltage at (c) and the minimum at (e). This implies, as with the Esaki diode, that the RTD displays negative differential resistance. The use of this NDR region in microwave emission and detection will be discussed in the next section.

2.5. Applications of Tunnel Diodes as Microwave Emitters and Detectors

2.5.1. Tunnel Diodes as Emitters

As discussed previously, the Esaki diode and the RTD both exhibited a negative differential resistance. This property allows for their use as amplifiers and as part of oscillator circuits. These oscillators can then be used to emit radiation for the purposes of data communication and imaging. To better understand this, we will start by exploring the properties of circuits including negative differential resistance.

If we consider a simple RLC circuit containing a resistor, *R*, an inductor, *L*, and a capacitor, *C*, and then add an element with a negative resistance, *-r*, as shown below, we can further understand negative resistance.

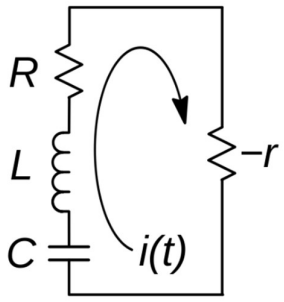

Figure 2.5.1: Circuit diagram of and RLC circuit with a negative resistor.

From Kirchhoff's voltage law the current, $i\{t\}$ around this circuit can be given as

$$\frac{di\{t\}}{dt}L + i\{t\}(R - r) + \int \frac{i\{t\}}{C}dt = 0$$

$$\therefore \frac{d^2 i\{t\}}{dt^2} + \frac{di\{t\}}{dt}\frac{(R-r)}{L} + \frac{i\{t\}}{LC} = 0$$

2.5.1

This is the differential equation for damped simple harmonic motion and has the solution

$$i\{t\} = i_0 e^{-\alpha t}\cos(\omega t + \varphi)$$

2.5.2

Where

$$\alpha = \frac{(R-r)}{2L}$$

$$\omega = \sqrt{\frac{1}{LC} - \left(\frac{R-r}{2L}\right)^2}$$

From this it is clear that if α is negative the current will oscillate with an exponentially increasing current. For real devices, such as the Esaki diode and the RTD, the current would stabilise as the device moves to the edge of the negative differential resistance region, where $R = r$. The frequency of operation, f, at the point of stability is easy to find and is given by Equation 2.5.3.

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{LC}}$$

2.5.3

As we have seen both the Esaki diode and the RTD exhibit negative differential resistance. A common figure of merit for these types of devices is the peak to valley current ratio (PVCR) which is simply the ratio of the current at the peak (Figure 2.4.4 (c)) to the current at the valley (Figure 2.4.4 (e)). As given by Equation 2.5.4.

$$PVCR = \frac{I_P}{I_V}$$

2.5.4

The negative differential resistance, R_d, itself can be characterised simply by Equation 2.5.5

$$R_d = \frac{V_p - V_v}{I_p - I_v} = \frac{\Delta V}{\Delta I}$$

2.5.5

The gain provided by the negative differential resistance allows free running oscillations, which are limited by the capacitance of the circuit. As such it is important to reduce the capacitance of the Esaki diodes or the RTD to as low a figure as possible. Both devices can be considered to be two charged layers separated by undoped semiconductor and as such the standard capacitor equation can be used to approximate the capacitance. This is shown in Equation 2.5.6.

$$C = \frac{A\varepsilon_0\varepsilon_r}{t}$$

2.5.6

Where A is the device area, t the thickness of the double quantum barrier structure and undoped spacer layers for the RTD and the size of the depletion region for the Esaki diode, ε_0 the permittivity of free space and ε_r the relative permittivity of the undoped regions of the device.

The theoretical maximum power emitted by the device as radiation can be described by the relation given in Equation 2.5.7.

$$P_{Max} = \frac{3\Delta V \Delta I}{16}$$

2.5.7

Clearly to generate large amounts of RF power, the voltage and current differences between the peak and the valley must be as large as possible. Practical device RF power at high frequency will not be as high as the power given by the relation due to the transit time of the electrons across the device [33]. This becomes more of a factor as the frequency of operation is increased and a more accurate power equation is given by

$$P_{RF} = \frac{3\Delta V \Delta I}{16} \cos \omega\tau \qquad 2.5.8$$

where ω is the angular frequency and τ is the transit time across the device.

The Esaki diode was a promising element for room temperature emitter applications. However, the thin barrier and consequently high junction capacitance, as well as the slow transit time of minority carriers limits its use at high-frequency and as such RTDs are the subject of a more concentrated effort in recent years. The current highest measured frequency for RTD oscillators was reported by the Asada group to be 1.98THz [41]. No power output was reported for this frequency, however previous work showed an output power of 0.4μW for a frequency of 1.92THz [125]. Whilst RTDs with the capability to operate at frequencies above 2THz have been shown by the University of Manchester[33], direct measurement of these frequencies has not been possible.

As data communications such as 5G and the IEEE 802.11ad WiFi standard move towards higher frequency [4], [6], [126]–[128], low power emitter technologies, the advantages of the RTD become more relevant. High frequencies in the mm-Wave and THz regimes allow for extremely high data rates. These frequencies have previously been ignored due to their poor propagation properties limiting their range. However, the 5G proposals to utilise small cells with high density mitigate these problems. As such recent research by the Asada group has shown wireless data rates of 34Gbit/s utilising RTD oscillator circuits[70].

2.5.2. Tunnel Diodes as Detectors

One of the main applications of all diodes is rectification. That is to allow current to pass through in only one direction. Rectification is of vital importance in the detection of microwave and radio wave communications. As such one of the key applications of some of the tunnel diodes discussed in the previous section is as a detector for telecommunications and data communications purposes. There are two types of detection in which tunnel diodes can be useful. The first is direct detection in which the diode is used in the detector circuit to demodulate the signal from the carrier wave. To better understand how this is achieved, we shall look at a simple diode detector.

One of the simplest diode detector circuits is used to detect amplitude modulated radio signals[129]. So, let's imagine a signal carried by a cosine wave with amplitude, A, and angular frequency ω_c. If the modulating signal is some function $f(t)$. Then the signal seen by the detector will be given by Equation 2.5.9 and look like Figure 2.5.3(A)

$$signal = (\mathrm{A} + f(t)) \cos \omega_c t \qquad 2.5.9$$

The detector circuit will consist of an antenna with some filtering to match the carrier frequency, a diode and a low pass filter. The diode and low pass filter are shown in Figure 2.5.2. The low pass filter will filter out the carrier frequency leaving just the modulating signal. If just the low pass filter was used, there would be two modulating signals one positive and one negative, and these would cancel out and the signal would be lost. This can be seen in Figure 2.5.3 (B). To stop this, the diode rectifies the signal before the low pass filter, removing the negative modulation. After the signal passes through the low pass filter only the positive modulation remains, and the full original signal is recovered. This is clearly demonstrated in Figure 2.5.3.

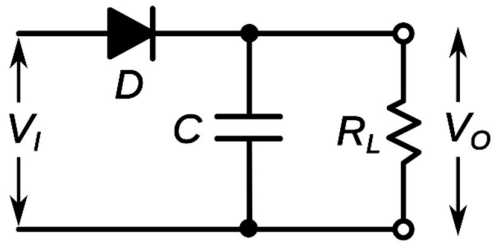

Figure 2.5.2:A simple microwave detector circuit containing a diode *D*, a capacitor *C* and a load resistor R_L.

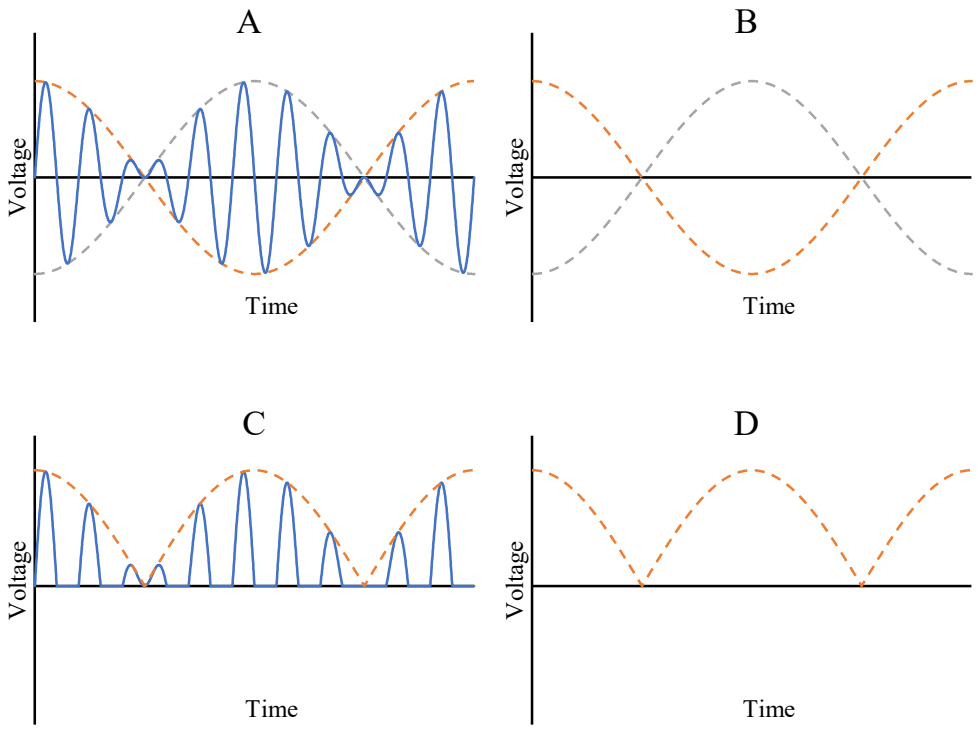

Figure 2.5.3 Plots of an amplitude modulated signal after various processing stages A) Full signal recieved from antena B) Signal after low pass filter only C) Signal after rectification. D) Signal after low pass and rectification.

This is the simplest form of RF modulation and direct detection, other more complex modulation processes such as frequency modulation and pulse modulation also exist using more complex detector circuit designs. These more complex detector circuits still make use of the non-linear nature of the diodes to recover the signal from the

carrier wave. Of the tunnel diodes discussed so far in this section the ASPAT diodes are the more suitable diodes for direct detection applications.

The suitability of a diode for direct detection is determined by a few key factors. The most important of which is the voltage sensitivity. This is given by the ratio of the output voltage to the input RF power and is given in units of V/W. The voltage sensitivity is easily measured at low frequency using a 50Ω RF source. The unmatched voltage sensitivity is given by

$$S_V = 2Z_s k_V$$

2.5.10

where Z_s is the source impedance, and k_V is the curvature coefficient [82]. k_V is one of the most important figures of merit for detector diodes, as it is a measure of the non-linearity of the diode. This is done by taking the quotient of the second and first derivatives of the current voltage curve as given by

$$k_v = \frac{\partial^2 I}{\partial V^2} \Big/ \frac{\partial I}{\partial V}$$

2.5.11

For the Schottky diode, in which thermionic emission is the main transport method, the curvature coefficient can also be calculated using the expression ($q/k_b T$). For Schottky diodes, this has an upper theoretical limit of ~40V^{-1}. Moreover, Schottky diodes are often biased to the point of highest non-linearity to improve sensitivity. This adds additional complexity to the circuit compared with a zero-bias detector device such as the ASPAT diode, in which k_v is at a maximum at 0V. As the ASPATs main transport mechanism is quantum tunnelling, it is possible that the ASPAT could be engineered to a value of k_v above 40V^{-1}.

As impedance matching is necessary to maintain voltage sensitivity for high frequency applications, another important detector property is the junction resistance. If the junction resistance is overly high, then the dimensions of any matching circuit would be impractically large to match the device input impedance to the standard 50Ω. The

junction resistance can be easily calculated from the current-voltage curve of the device using the equation.

$$R_j = \left(\frac{\partial I}{\partial V}\right)^{-1}$$

2.5.12

The final important property of detector diodes is the cut off frequency, f_t. This defines the maximum operating frequency of the diode and limits the frequency regime it can operate in. This is mainly determined by the junction capacitance of the device, C_j, along with the series resistance, R_s, and is given by

$$f_t = \frac{1}{2\pi R_s C_j}$$

2.5.13

The series resistance is comprised of multiple contributions from the structure of the device including the contacts and device geometry. The specific makeup of the series resistance for the ASPAT diode will be explored in chapter 3. As can be seen from Equation 2.5.13 it is important that both the junction capacitance and the series resistance are minimized to maximise the device cut-off frequency.

The second type of detection in which tunnel diodes can be used is heterodyne detection. In heterodyne detectors the incoming signal is combined with a signal from a local oscillator via a mixer. A perfect mixer operates by multiplying the two signals together. This can be seen schematically in Figure 2.5.4.

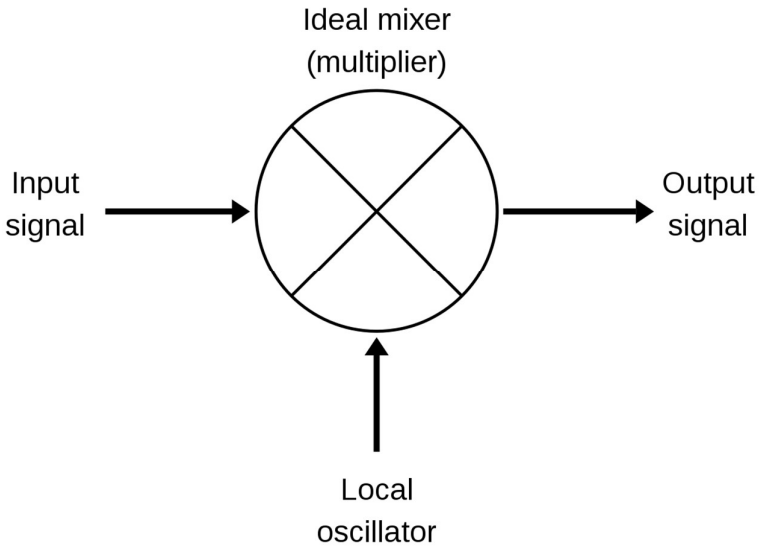

Figure 2.5.4: Schematic of an ideal frequency mixer using a local oscillator and a multiplier.

If we have two sine waves of frequency f_{LO} and f_{RF} to represent the local oscillator signal and the incoming RF signal, then through the trigonometric identity we can write.

$$\sin 2\pi f_{LO} \sin 2\pi f_{RF} = \frac{1}{2}[\cos 2\pi(f_{LO} - f_{RF})t - \cos 2\pi(f_{LO} + f_{RF})\, t] \qquad 2.5.14$$

This produces two signals one at the sum of the local oscillator and RF frequencies $f_{LO} + f_{RF}$ and one at the difference $f_{LO} - f_{RF}$. The lower signal at $f_{LO} - f_{RF}$ is particularly useful as it allows for the conversion of a high frequency signal to a lower frequency. This allows for heterodyne detectors to demodulate high frequency carrier signals to lower frequency signals for processing. This allows for the use of carrier frequencies in higher frequency bands that can then be downconverted to the operating frequencies of mature radio and microwave technologies such as filters and amplifiers.

As discussed previously negative differential resistance can be used to create free running oscillators. This means that devices like the RTD described above have potential use as local oscillators in heterodyne detection systems. The other potential

use that tunnel diodes have in the heterodyne systems is as a mixer. This function can be performed by any device with a nonlinear IV characteristic and so is an application that tunnel diodes of all types are well suited for.

2.6. Summary

In this chapter the background and theory of semiconductor devices and tunnel diodes was discussed. Heterojunction formation was investigated, and it was shown how band gap discontinuities can be used to create barrier and well structures. The importance of matching the lattice constants of the two materials used in a heterojunction was discussed and common lattice matched material systems such as the GaAs/AlAs system and the $In_{0.53}Ga_{0.47}As$/InP system were identified. The use of metamorphically graded lattices to allow for the growth of materials on un-matched substrates was discussed as was the use of pseudomorphic strained layers to engineer band gap discontinuities,

The principles of quantum tunnelling and resonant tunnelling were included in this chapter. The use of these mechanisms in devices such as the Esaki diode, the ASPAT diode and the RTD was also discussed. The electrical characteristics of these didoes were explored, including negative differential resistance exhibited by the RTD and Esaki diode, as well as the more traditional rectification exhibited by the ASPAT. The principles of free running oscillation using NDR were explored and the suitability of RTD and Esaki didoes oscillators for high frequency applications was discussed. The principles of direct microwave detection were also discussed and the figures of merit for detector diodes such as, curvature coefficient, junction resistance and cut off frequency given. The suitability of the ASPAT for this application was commented upon and will form a large part of this work. The principles of heterodyne detection were also discussed and the suitability of tunnel diodes for this application as local oscillators and mixers was explored.

CHAPTER 3

SEMICONDUCTOR MATERIALS SYNTHESIS AND DEVICE FABRICATION

3.1. Introduction

In this chapter the fabrication of semiconductor devices will be explored. This will include the growth of semiconductor wafers utilising both molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD), which is also sometimes referred to as metal organic vapour phase epitaxy (MOVPE). Following this the methods of device fabrication will be explored; this will include lithography techniques using wet and dry etching as well as the deposition of metal contacts on the device. The final part of this chapter will focus on the measurement and characterisation of devices including the components that make up the series resistance, the parasitic capacitance and inductance.

3.2. Semiconductor Synthesis

3.2.1. Molecular Beam Epitaxy

Molecular Beam Epitaxy is an extremely precise method of growing semiconductors crystals, capable of growing epitaxial layers to monolayer precision. Furthermore, semiconductor heterostructures grown using MBE show extremely abrupt junctions. As such, the technique is routinely used to grow semiconductor wafers for III-V based transistors[78], [130], semiconductor lasers [61] and high precision diodes such as RTDs [41] and ASPATs [101].

MBE growth starts with the heating of high purity elements or compounds as sources. These sources will sublime or evaporate, depending on their initial state (for this work all sources are solids). The now gaseous sources will then be directed to a rotating substrate under ultra-high vacuum. The gases will then condense on the substrate and react to form a single high-quality crystal. In the case of Gallium and Arsenic the

crystal formed would be Gallium Arsenide. The rate of growth is controlled by the temperature of the source and abrupt junctions between different semiconductors can be achieved by opening and shutting shutters on the source heating elements.

The state of the growth during operation is determined utilising the reflection high energy election diffraction (RHEED) technique[131]. The layout and schematic of an MBE system is shown in Figure 3.2.1.

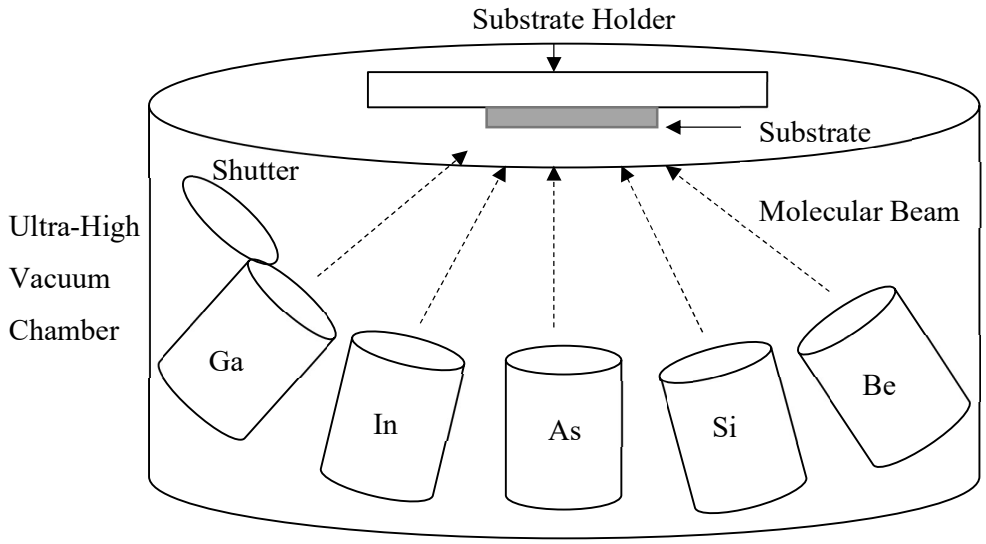

Figure 3.2.1 Simplified schematic of a Molecular Beam Epitaxy (MBE) system for the growth of GaAs and InP technologies [132].

3.2.2. Metal Organic Vapour Phase Epitaxy

Metal Organic Vapour Phase Epitaxy is an alternative method of producing similar structures to those grown using the MBE technique. In this technique there is no need for an ultra-high vacuum as the elements are incorporated into the substrate using a chemical reaction. The elements to form the semiconductor crystal are introduced using precursors. These precursors are volatile compounds which are introduced to a heated rotating substrate. The precursors then undergo pyrolysis and the subspecies are absorbed into the semiconductor wafer as a new layer [133]. To create a GaAs semiconductor wafer, precursors for Gallium and Arsenic are necessary, such as

trimethyl gallium $(CH_3)_3Ga$ and trimethyl aluminium $(CH_3)_3Al$. An example of a GaAs MOCVD system is shown in Figure 3.2.2.

When compared to MBE the main difference between the two techniques is growth rate. MOVPE is capable of 5-25μm/hr which is significantly faster than MBE which achieves rates of 1μm/hr. However, the hazardous nature of the chemical precursors means that the necessary safety precautions for MOVPE are higher than those for MBE, and there is some difficulty in the precuring of the necessary high-quality gasses.

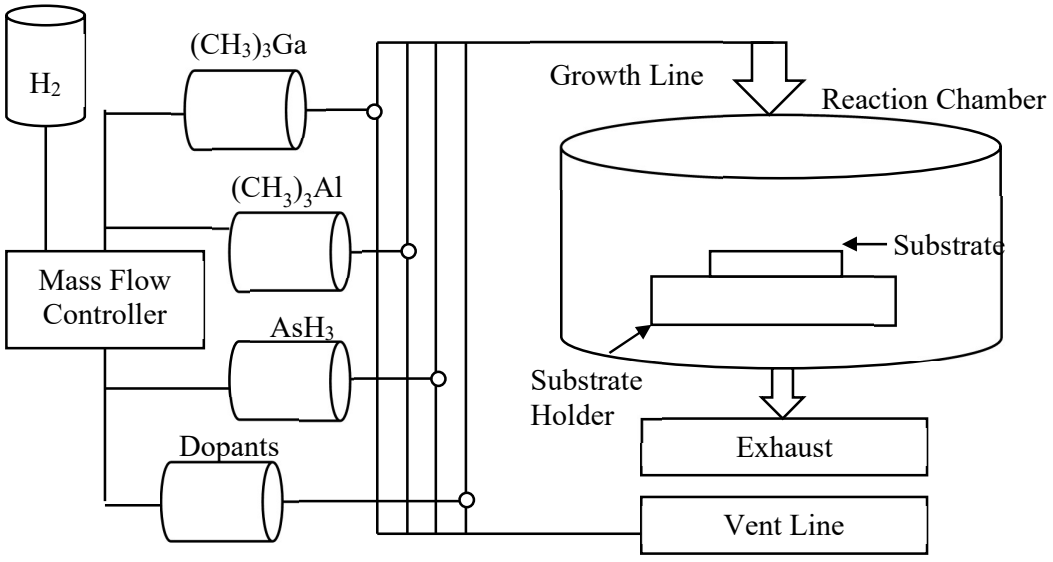

Figure 3.2.2 Simplified schematic diagram of a GaAs/AlAs Metal-Organic Vapour Phase Epitaxy (MOVPE) system [132].

3.3. Device Fabrication

3.3.1. Sample Cleaning

During fabrication of samples, contaminants on the device surface can be detrimental to device performance. As such all processing was performed in a class 1000 clean room, in which air quality was controlled using laminar flow and air filtration systems. However, samples can still be contaminated by human handling and by the tools used

during the fabrication process. As such it is necessary to clean samples before each fabrication step. The standard method of sample cleaning is as follows.

- The sample is placed in N-Methyl-Pyrrolidone (NMP) to remove any contaminants on the surface.
- The sample is then placed in an ultra-sonic bath for some time (approximately 5mins) to remove the NMP from the surface
- The sample is rinsed using de-ionised (DI) water.
- The sample is dried using a nitrogen gas (N_2) gun

After this cleaning regime the sample can then be processed in one of the fabrication steps.

3.3.2. Photolithography

The purpose of device fabrication is to turn a wafer consisting of epitaxial layers in the Z-direction into complete three-dimensional devices. To do this the X-Y geometry of the devices need to be imprinted onto the wafer. This is done through the process of photolithography, also commonly referred to as optical lithography. This type of lithography uses UV light, typically from the mercury i-line of 365nm, and has a minimum feature size of ~0.5μm. Other lithography techniques such as electron beam lithography are preferred for submicron processing [134].

The first step of photolithography is the deposition of photoresist. This is a polymer which undergoes a chemical reaction when exposed to UV light. The photoresist is deposited onto the sample and a uniform coating is achieved by spinning the sample at high speed. The thickness of the photoresist layer is inversely proportional to the speed at which it is spun. After spinning the photoresist is placed on a hotplate to harden. The temperature of the hotplate is determined by the type of photoresist used.

There are two types of photoresists: negative resist and positive resist. In the case of negative resist, the photoresist will be polymerised when exposed to UV light so that when it is submerged in a developer solution the areas which have not been exposed will dissolve. This is the opposite of positive photoresist in which the areas of the sample which are exposed to UV light will be dissolved by the developer and areas

which have not will remain. Table 3.3.1 gives details of different photoresists and Figure 3.3.1 shows an example of the lithography process for both types of resist.

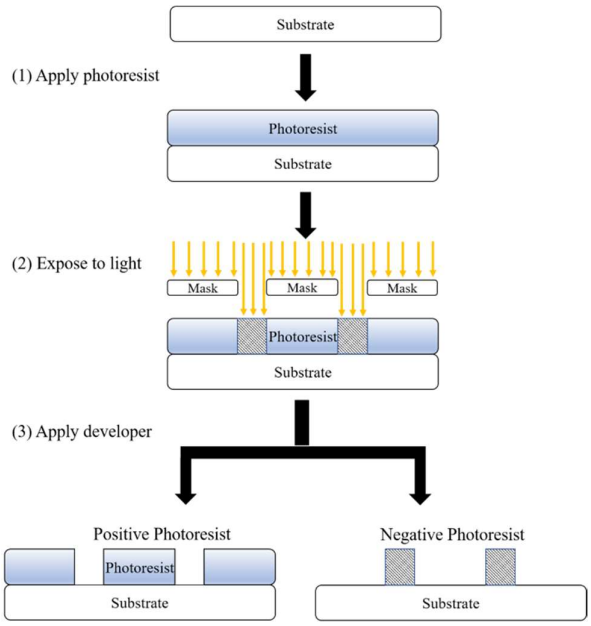

Figure 3.3.1 Photolithography process showing deposition, exposure and development for positive and negative photoresists.

After the application of photoresist, the sample is exposed to UV light which has been partially obscured by a "mask". This mask will pattern the sample in the manner necessary for the fabrication process. After UV exposure, the sample will be placed in a developer solution to remove areas of photoresist leaving exposed wafer which can be etched away or have metal deposited on as necessary.

The alignment of the mask is one of the limiting factors in the minimum feature size of a device. As a device fabrication requires multiple photolithography steps small misalignments within 0.5μm can be compounded and device performance reduced.

Table 3.3.1 Table of photoresist properties.

Photoresist	*Type*	*Thickness (μm)*	*Bake Temperature (C)*
AZnLOF 2020	Negative	2.0	110
S1805	Positive	0.5	115
S1813	Positive	1.3	115

3.3.3. Chemical Wet etching

In order to turn the flat wafer into 3D devices it is necessary to remove parts of the wafer. This can serve multiple purposes, the most important is the formation of a device mesa which can be thought of as one single device, the second is the exposure of doped contact layers onto which metal contacts can be added to, and finally to isolate devices from one another electrically. To do this, the semiconductor wafer is etched using acidic solutions or etchants.

The area to be etched is exposed using the photolithography technique described in the previous section and an Orthophosphoric based solution is used to etch away layers of GaAs, AlAs and InGaAs at specific rates. This allows the depth of the etch to be calibrated by the length of time the sample is submerged in the etchant. The Orthophosphoric solution is prepared with a standard mixture of Orthophosphoric acid (H3P04), Hydrogen Peroxide (H2O2) and water (H20) with a ratio of 3:1:50 [135].

Unfortunately, the Orthophosphoric etchant does not only etch in the vertical direction but also laterally. As such an undercut is formed underneath the photoresist layer and devices created are often smaller than nominally designated in the mask design. This effect must be accounted for when determining current density and other area dependent device properties, especially on smaller devices in the range ~10μm^2 where the size of the undercut is proportionally larger than on large devices in the range ~100μm^2.

3.3.4. Metallisation and Lift-off

For devices to be biased and to communicate with the outside world it is necessary to create metal contacts. This is done by the deposition of metal onto heavily doped contact layers forming ohmic contacts. There are two processes to add metal to semiconductor wafers namely evaporation and sputtering. The evaporation process was used throughout this work and will be described in this section.

The area upon which metal will be deposited is exposed using photolithography as described earlier. The metal to be evaporated is placed in a resistive tungsten boat inside an airtight chamber and the samples held above the metal sources using

magnets. The chamber is then vacuum pumped to a pressure below 1×10^{-6} mbar and a current of the order 5A is applied through the resistive boat. This current heats the metal until evaporation occurs and the metal is deposited on the sample. The rate at which metal is deposited is monitored using a built-in thin film thickness monitor.

Once the metal has been deposited upon the sample the photoresist must be removed using a lift-off technique. This is done by submerging the sample in an NMP solution, this dissolves the layer of photoresist and lifts-off the metal above it leaving only the metal deposited directly on the substrate. A negative photoresist is used for this purpose as it has an undercut profile which allows for a separation between the metal on the photoresist and that on the substrate. This is demonstrated in Figure 3.3.2

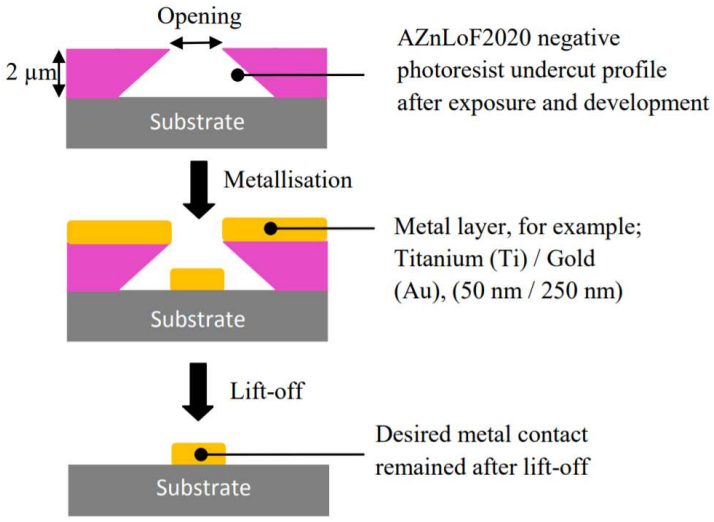

Figure 3.3.2 Diagram showing the metallisation and lift-off process of Ti/Gold contacts on a substrate using negative photoresist.

3.3.5. Device Fabrication Process

Two terminal devices like those discussed in this work have a simple fabrication process, especially when compared with three terminal devices such as transistors. The general process for a two terminal device is as follows

- Top contact deposited onto doped top contact layer using metallisation and lift off.
- Device mesa is etched exposing doped bottom contact layer.

- Devices are isolated from one another by way of a second etch.
- Bottom contact is deposited using metallisation and lift off.

As semiconductor devices are often small, it is difficult to connect directly to the top contact of a device. As such the top contact is usually connected to a bond pad via an airbridge. This is shown in Figure 3.3.3 below.

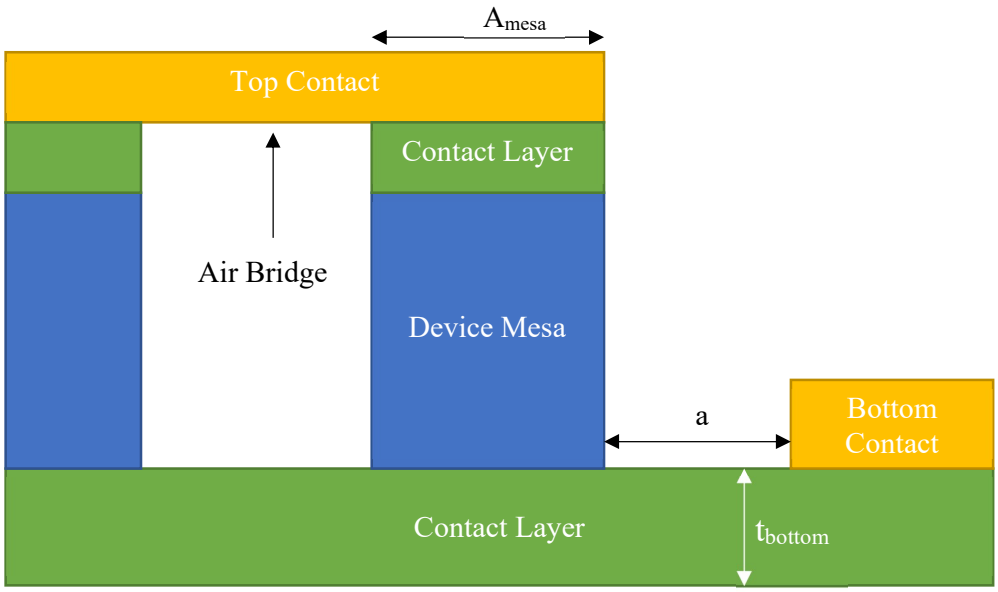

Figure 3.3.3 Side view of a fabricated device with an air bridge top contact.

One method of creating an airbridge is to allow the lateral undercut of the etchant to create the gap under the top contact. This is quite difficult as the exact amount of time needed to achieve this must be determined by trial and error. A second method to create the air bridge is to add an additional step before the top contact is deposited in which a trench is etched. This trench can then be filled with photoresist and the metal bridge deposited on top. This metal bridge now acts as a hard mask and the device mesa area can be etched without the need for another lithography step. This method using metal contacts to define the etch area is called a self-aligned process and allows for a better device fabrication process, as one of the largest sources of error in the fabrication process is in the alignment of the various mask plates for photolithography.

3.4. Device Testing

Throughout this work two types of device testing were used: DC characterisation and RF characterisation. The DC measurements will be used to determine device curvature coefficients and junction resistances. The measurements were taken with a semiconductor parameter analyser (e.g. Agilent B1500) at room temperature unless stated otherwise.

The RF characteristics of the device are determined by utilising measurements of the Scattering parameters (S-parameters). Specifically, the S_{11} reflection coefficient for one port devices. A calibrated Vector Network Analyser (VNA, Anritsu 37369A) was utilised to collect the S_{11} data of devices up to a frequency of 40GHz at various bias points. From this data the RF characteristics of the device can be extracted utilising an equivalent circuit model. This model will consist of the device junction resistance R_j, series resistance R_s, junction capacitance C_j, as well as contributions from the surrounding device circuitry in the form of the parasitic capacitance C_p and the parasitic inductance L_p.

3.4.1. Series Resistance & Transmission Line Method

The series resistance of a device is determined by the losses of the diode structure across the layers and contacts. For a diode that utilises a planar structure as shown in Figure 3.3.3 this will also include a contribution from the spreading resistance. As such the total series resistance R_s can be given by Equation 3.4.1 where R_{spr} is the spreading resistance, R_{epi} is the resistance from the doped epitaxial layers, ρ_c is the specific contact resistance and A_{mesa} is the area of the device mesa.

$$R_s = R_{spr} + R_{epi} + \frac{\rho_c}{A_{mesa}} \tag{3.4.1}$$

The spreading resistance is due to the resistance to lateral current flow across the bottom doped contact layer and can have a significant impact on the series resistance. The spreading resistance can be determined from Equation 3.4.2. Where μ_n is the mobility, N_D is the doping concentration t_{bottom} is the thickness of the bottom contact doping layer and a is the distance from the mesa to the bottom contact.

$$R_{spr} = \frac{1}{\pi e \mu_n N_D t_{bottom}} \ln \frac{a}{A_{mesa}}$$

3.4.2

R_{epi} is the resistance of the doped epilayers in the diode and can be determined for each layer with Equation 3.4.3 where t_{layer} is the thickness of the layer.

$$R_{epi} = \frac{1}{e \mu_n N_D} \frac{t_{layer}}{A_{mesa}}$$

3.4.3

To determine the specific contact resistance of the device, the transmission line model is used [136][137]. To use this model, a series of rectangular contacts are etched into the wafer with gaps of distance d_n between them. d_1 is equal to 5μm and the gaps increase by 5μm each time up to a distance d_8 of 40μm.The TLM structure has two sheet resistances. One under the metal pads denoted as R_{sk} and the sheet resistance between pads $R_{sh.}$ The structure also has a transfer length L_T which is the effective distance that current flows under a given pad. This is illustrated in Figure 3.4.1 below.

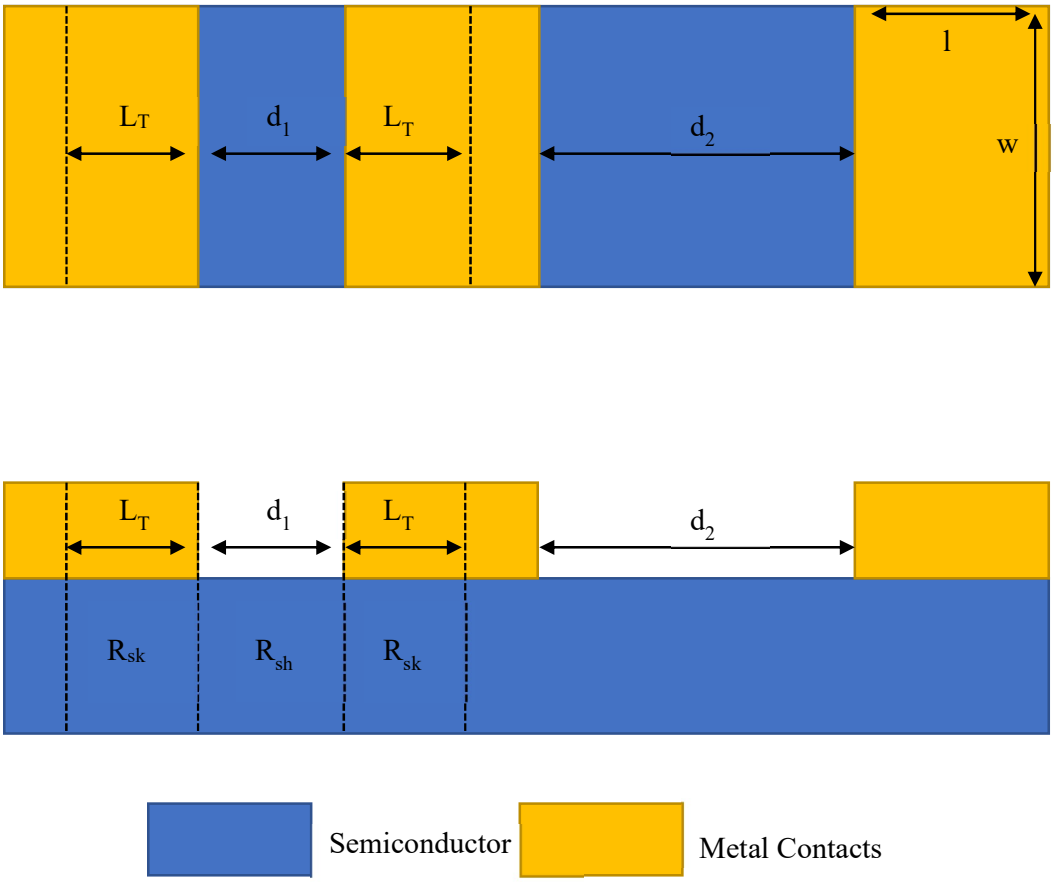

Figure 3.4.1 diagram of top and side views of transmission line method structure to determine specific contact resistance.

As such the total resistance R_T between two pads will be given by

$$R_T = 2R_{sk}\frac{L_T}{W} + R_{sh}\frac{d_n}{W}$$

3.4.4

A probe is then used to measure the resistance between the pads across d_1 through to d_8. The term $R_{sk}\frac{L_T}{W}$ will remain constant and can be denoted as the contact resistance R_c giving

$$R_T = 2R_c + R_{sh}\frac{d_n}{W}$$

3.4.5

From the measurements R_T can be plotted as a function of d_n with the y-intercept equal to $2R_c$ and the x-intercept equal to $2L_T$. This is shown in Figure 3.4.2.

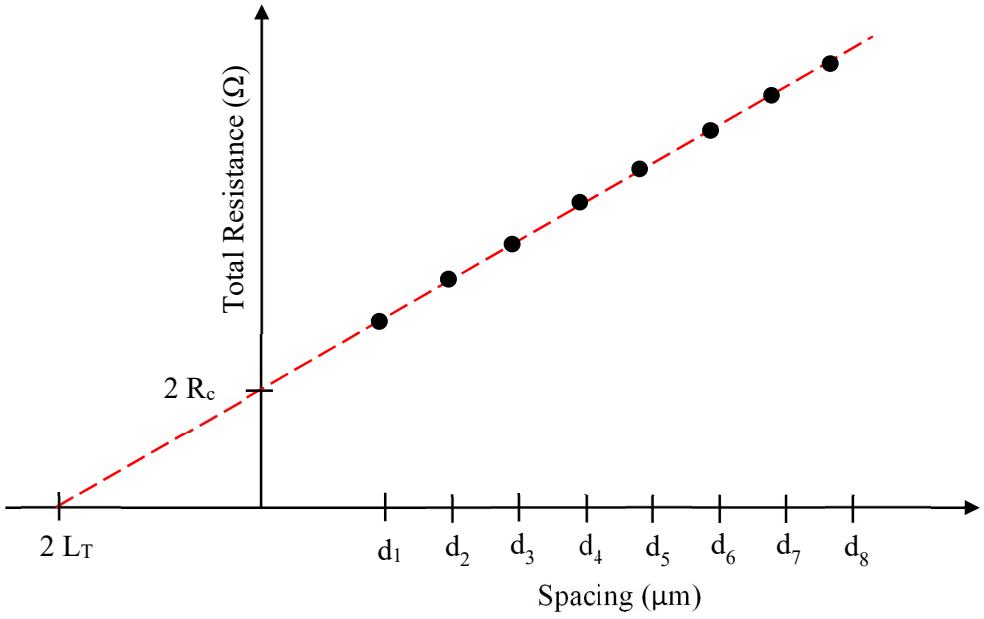

Figure 3.4.2 Example total resistance versus pad spacing for a TLM measurement structure.

After extracting L_T and R_c, it is trivial to calculate the specific contact resistance using Equation 3.4.6. The gradient of the line will be equal to $\frac{R_{sh}}{W}$ and can be used to determine the sheet resistance R_{sh} provided the width of the TLM is known.

$$\rho_c = R_c L_T W$$

3.4.6

3.4.2. De-embedding procedure

As discussed previously the intrinsic RF characteristics of the devices are extracted from the measured S_{11} reflection coefficient data using an equivalent circuit model. However, the measured data will also contain influences from parasitic capacitances and inductances from the co-planar waveguide (CPW) transmission lines and the GSG patterned bond pads. To remove these from the data, a 2-step de-embedding procedure is used [138]. This involves the fabrication of two structures with the GSG CPW configuration used for the devices however one of the structures will be shorted and the second left open. The S_{11} parameter of these open and short structures was then measured up to a frequency of 40GHz. These measurements can then be used to determine the parasitic capacitance and inductance of the bond pads by way of an equivalent circuit method. Equivalent circuits of the short and open structures were created in Agilent Advanced Design Systems software and S_{11} simulated for both structures. The values of C_p and L_p were then tuned until a good match between the measured and simulated S_{11} parameter was found. In the case of an ideal short bond pad the equivalent circuit is simply an inductor whilst for the open bond pad the equivalent circuit is given by a capacitor.

3.5. Conclusion

In this chapter the growth, fabrication and testing of two terminal semiconductor devices was discussed. The methods of growth included were molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD). The principles of i-line photolithography were discussed along with its use in patterning the semiconducting wafer for the purposes of wet etching and metallisation. The details of the wet etching used through this work were also described including the undercut effect which reduces the nominal area of the device mesa. The metallisation process

used to deposit metal contacts on the devices was described including both the evaporation and the lift-off processes. The general fabrication process for devices was described and a more specific self-aligned air bridge technique was detailed which reduces the number of alignments needed which introduce error into the process.

The process of testing the DC and RF characteristics of the devices was outlined. This included discussions on the contributions to the device series resistance from the device epi-layers, spreading resistance and the contact resistance. The transmission line method used to determine the device the device specific contact resistance was described. The 2 step de-embedding procedure used to determine the parasitic inductance and capacitance of the device introduced by the devices bond pads and co-planar wave guide structures was outlined. This procedure involves the creation of open and shorted de-embedding structures. The S_{11} parameter up to 40GHz for these structures is measured and equivalent circuit models used to determine the devices extrinsic parasitic capacitance and inductance.

CHAPTER 4

PHYSICAL MODELLING

4. Introduction

As the fabrication of semiconductor devices is a lengthy and expensive process it is often quicker and cheaper to explore new device ideas with the aid of physical modelling and simulation. This has been made even easier over time with the help of Technology Computer Aided Design (TCAD) software such as SILVACO ATLAS. During this work, physical modelling has been used extensively to guide and inform the direction of new device structures and to optimize device performance.

This chapter will begin with a brief look at the fundamentals of numerical simulation before going on to focus on the specifics of SILVACO ATLAS TCAD software. This will include discussion about how devices are specified in ATLAS as part of the physical model. As well as discussion of the material models used in this work, the implementation of traps and defects, the physical simulation models used, the specification of doping levels and the implementation of contacts.

This chapter will also contain a section on the implementation of equivalent circuit modelling in Agilent Advanced Design Systems software and its use in extracting the RF parameters of devices.

4.1. Fundamentals of Numerical Analysis

Before the widespread adoption of computational simulation, new devices were explored using classical numerical solutions. For semiconductor devices the most important of the equations to solve was the Schrödinger equation. This equation governs the behaviour of all particles and is directly implemented into SILVACO ATLAS. From this equation the macroscopic properties of the device can be extracted such as the electron-density, mean velocity and charge concentration. This differs from the Monte-Carlo approach to modelling in which it is difficult to extract the macroscopic properties of the device.

4.1.1. The Schrödinger Equation

The Schrödinger equation is the defining equation of quantum mechanics. In the same way that Newtons 2nd law $F = ma$ is the defining equation of motion in classical mechanics. In Schrödinger's equation the wavefunction of a particle defines its movement, energy and momentum. However, the Schrödinger equation only describes the evolution of the wave function, not its physical meaning. It was Max Born who was later able to determine that the wave function represented the probability amplitude of the particle, with the square modulus of the wavefunction defining the probability distribution of finding a particle in a specific location [139]. As such the wavefunction represents a probability even though its evolution through time is deterministic. This implies a probabilistic interpretation of the universe in which future events cannot be predicted as would be the case in a classical deterministic universe. This dismayed many of the initial discoverers of quantum mechanics including Albert Einstein who believed the universe to be deterministic and stated, "*God does not play dice with the universe*". To better interpret the meaning of these new equations, the scientific community developed the Copenhagen interpretation, and its principles are stated below.

- A system is described by its wavefunction, usually represented by the Greek letter Ψ.
- The wavefunction obeys the Schrödinger equation over time.
- Nature is probabilistic. The probability of an event—for example, where on the screen a particle shows up in the double-slit experiment—is related to the square of the absolute value of the amplitude of its wave function.
- It is not possible to know all the values of the properties of a system at once (Heisenberg's Uncertainty Principle)
- Matter and Energy both exhibit wave particle duality.
- The results provided by measuring devices are essentially classical and should be described by ordinary language (This point was contested by Heisenberg and Bohr for some time and is one of the main factors in the development of alternate theories)
- The quantum mechanical description of a large system should approach the classical description.

The Copenhagen interpretation remains the most popular interpretation of quantum mechanics to date. However, other interpretations, such as the many worlds interpretation, are also under development and the true meaning of quantum mechanics is still being debated. This is beyond the scope of this work and as such the Copenhagen interpretation will be used.

The Schrödinger equation is given below in Equation 4.1.1

$$\widehat{H}(t)\psi(t) = i\hbar\frac{\partial}{\partial t}\psi(t)$$

4.1.1

Where $\widehat{H}$ is the Hamiltonian operator which evaluates the total energy of the system. It contains contributions from the kinetic energy and the potential energy. As such it is also possible to write the Schrödinger equation as Equation 4.1.2.

$$\left(\frac{\hat{p}^2}{2m} + V(r,t)\right)\psi(t) = i\hbar\frac{\partial}{\partial t}\psi(t)$$

4.1.2

Where $\hat{p}$ is the momentum operator given by $\hat{p} = i\hbar\nabla$, *V(r,t)* is the potential as a function of space and time and *m* is the mass of the particle. Using these, the Schrödinger equation can finally be written as

$$\left(\frac{-\hbar^2}{2m}\nabla^2 + V(r,t)\right)\psi(t) = i\hbar\frac{\partial}{\partial t}\psi(t)$$

4.1.3

where $\hbar$ is the reduced Planck constant, *r* is the position vector, *t* is time and ∇ the differential operator.

4.2. SILVACO ATLAS

ATLAS is a physically based device simulator. These types of device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions. To do this the device is approximated onto a two- or

three-dimensional mesh. The transport of carriers through this grid, defined by a set of differential equations derived from Maxwell's equations, can then be calculated at each point of the mesh. This then means that the electrical performance of the device can now be modelled.

Physically based simulation differs from empirical modelling in that, the physics-based simulation of the device can be predictive and incorporate theoretical knowledge in new applications. By contrast, empirical modelling simply provides an accurate approximation of already existing devices. Whilst this is very useful in the design of circuits and applications of these devices, it does not help to understand how a new device structure may behave.

To make sure that an accurate physics-based simulation has been achieved it is of paramount importance that all relevant physics are incorporated in the device model. Also, as analytic solutions to the differential equations are not guaranteed, numerical algorithms must be used to solve them. As, such ATLAS provides a range of iterative methods for the user [140].

In Atlas, a physically based device simulation is performed by defining:

• The physical structure to be simulated.

• The physical models to be used.

• The bias conditions for which electrical characteristics are to be simulated.

The basic flow chart of inputs and outputs into ATLAS is shown in Figure 4.2.1. Two input files are used, these are the command file, containing the instructions for ATLAS to execute, and the structure file, containing the device structure and models which will be simulated. ATLAS produces three types of output file, first is the runtime output which shows the progress of the simulation as well as providing warning and error messages. The second is the log file which stores the voltages and currents of any analysis. The third type of output is a solution file which provides the state of the device structure at a given bias. This structure file can be probed to find device characteristics at any point of the device and is useful in determining the dynamics of a device under operation.

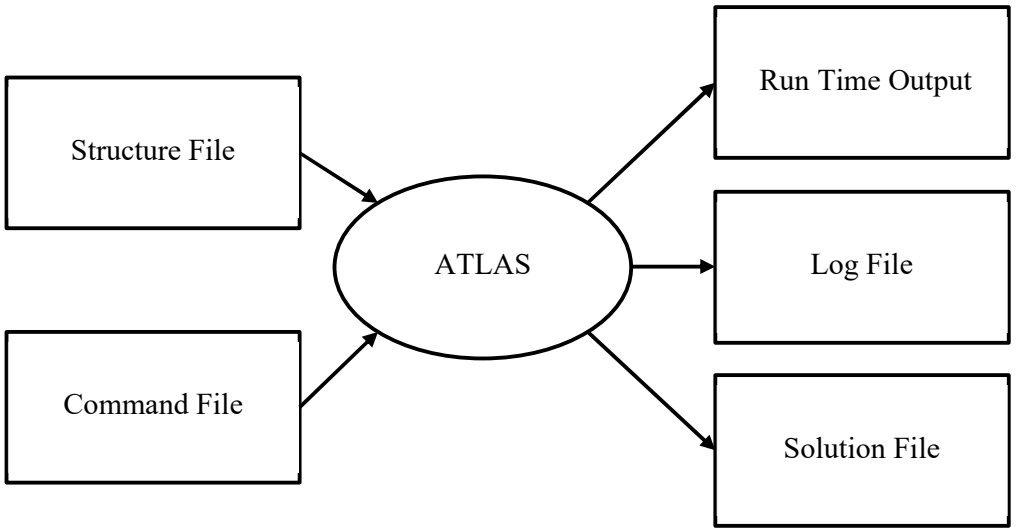

Figure 4.2.1 Diagram showing the input and output files of SILVACO ATLAS programs.

The structure and command files for ATLAS can be automatically generated from a single input file created in the ATLAS DeckBuild runtime environment [140].

4.2.1. ATLAS Syntax

To execute the command and structure files correctly, the correct syntax must be used when creating the input file in DeckBuild. This is true both of the individual commands and of the order in which the commands are input. The general structure of a command in DeckBuild is as follows

$$\langle Statement \rangle \langle Parameter \rangle = \langle Value \rangle$$

There are five different groups of statements used in ATLAS. Structure statements, material models statements, numerical method statements, solution specification statements and results analysis statements. These statement groups must be given in this order for the input file to run successfully. Within these statements are a series of subdivisions which again must be given in the correct order. For example, in the structure statements the mesh must be defined before the device regions are defined or an error will occur. Table 4.2.1 shows all the relevant statements needed for a complete input file.

Table 4.2.1 Table of ATLAS statements.

Statement Group	Statement	Purpose
Structure	Mesh	Defines the mesh for the simulation
	Region	Defines the regions of the device and their materials
	Electrode	Defines the position of electrodes
	Doping	Defines the doping of regions
Material Models	Material	Defines material properties e.g. bandgap, affinity, etc
	Models	Defines which models to use
	Interface	Defines interface properties
Numerical Method	Method	Defines the algorithm or numerical method used.
Solution	Log	Specifies values to log e.g. current, capacitance, etc
	Solve	Specifies solution type e.g. voltage sweep, frequency sweep.
	Save	Saves log or solution file.
Results Analysis	Extract	Extracts device parameters from solution file
	Plot	Plots log or solution files.

4.2.2. Structure Specification

The first thing to be defined within the input file is the *mesh*. This is done by a series of statements outlining the meshes coordinates and the mesh spacing between the coordinates. ATLAS can define structures in both 2D and 3D cartesian coordinate systems as well as in a 2D cylindrical system. To determine the real solutions of the 2D systems, the 2D simulation is them integrated as a series of slices. In the case of the cartesian system this is done through a *width* statement determining the third dimension and in the cylindrical system through a rotation about the centre axis point (0,0). As the simulation models used in this work, such as the *semiconductor-insulator-semiconductor* (SIS) model, are quasi 1D and the device structures are square mesas, a 2D cartesian system was used throughout, with all coordinates specified in micrometres.

After the *mesh* has been defined, the device is defined using a series of *region* statements. These regions are numbered, and the semiconductor material of each region stated. The 2D cartesian system designates X as the horizontal axis and Y as the vertical axis, however unusually the Y axis goes from the top to the bottom of the device It is in the *region* statements that the quantum region of the device is defined for the SIS model.

As well as the *mesh* and *region* statements, the structure specification also includes the *doping* of the device. This is done by simply setting the doping at the desired level in an already specified region. All doping is set to silicon doping by default by ATLAS.

The *electrode* statement is the final statement of the structure specification this specifies the location of the electrical terminals for the simulation. The physical attributes of the electrodes can be specified using a *contact* statement. All electrodes attached to semiconductors are assumed to be Ohmic by default in ATLAS unless a work function is specified, then the contact is treated as a Schottky contact.

4.2.3. Material Models

After the structure specification is complete, material models must be specified. ATLAS contains a large library of semiconductor properties and models. For the most part this work is based on the GaAs, AlGaAs and InGaAsP system models within ATLAS. The InGaAsP model was used to simulate InGaAs by setting the P fraction to 0. However, there are areas in which the material parameters used were defined to better match the specific physics involved in the device operation. These parameters included the affinity, bandgap and effective mass of materials. The default GaAs system was used throughout the work unmodified as it is a well understood system. The ternary systems of $In_{(1-x)}Ga_{(x)}As$ when not lattice matched to InP and $Al_{(x)}Ga_{(1-x)}As$ however required manually input parameters, as did the affinity of AlAs when used as a thin barrier.

$In_{(1-x)}Ga_{(x)}As$ Parameters

The user defined inputs for the $In_{(1-x)}Ga_xAs$ system used the gallium composition, x, as the defining variable. This was then used to determine the affinity, χ, room temperature band gap, E_g, and effective mass, m^*, for $In_{(1-x)}Ga_{(x)}As$ of any composition using the standard book value equations below. [141], [142]

$$\chi = (4.9 - 0.83x)eV \tag{4.2.1}$$

$$E_g = (0.36 + 0.63x + 0.43x^2)eV \tag{4.2.2}$$

$$m^* = (0.023 + 0.037x + 0.003x^2)m_e \tag{4.2.3}$$

$Al_{(x)}Ga_{(1-x)}As$ Parameters

As with the InGaAs system the affinity, χ and room temperature band gap, E_g for $Al_{(x)}Ga_{(1-x)}As$ were found using standard book equations [141]. The main variable in

this case was the aluminium composition not the gallium composition. The equations used are shown below

$$\chi = (4.07 - 1.1x)eV$$

4.2.4

$$E_g(\Gamma) = (1.42 + 1.16x + 0.37x^2)eV$$

4.2.5

AlAs Tunnel Parameters

Standard bulk AlAs has an indirect band gap at the X valley of 2.16 eV. However, for thin tunnelling barriers the tunnelling occurs through the direct Γ-Γ valley[86]. Therefore, throughout this work the AlAs bandgap used for thin tunnelling layers is the direct Γ-Γ bandgap of 2.82eV. The effective mass of electrons in the thin barrier is related to the curvature of the conduction band and this relation is given by Equation 4.2.6. As is apparent from Figure 4.2.2 the curvature of the Γ valley and the curvature of the X valley are not the same and this must be taken into account and as such the effective mass of AlAs used throughout this work is $0.15m_e$ as given in the standard book values [91].

$$m^* = \frac{\hbar^2}{d^2E/dk^2}$$

4.2.6

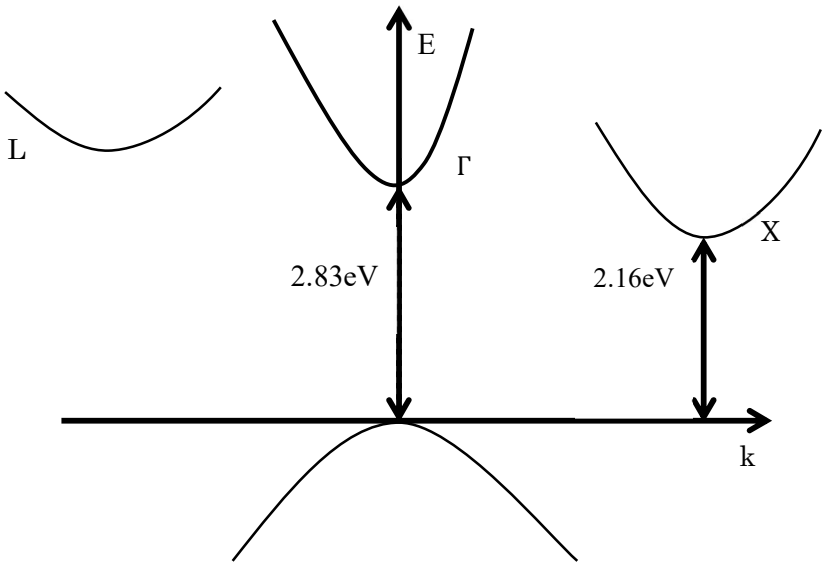

Figure 4.2.2 Simplified diagram of the dispersion relation of band energies *E* vs wavenumber *k* of AlAs showing the Γ-X-L valleys

The final important parameter which needs to be carefully considered for thin AlAs barrier layers is the affinity. As ATLAS creates heterojunctions using Andersons rule, as described in Chapter 2, the affinity determines the conduction and valence band offsets for a heterojunction. To conform with the well-known 65:35 conduction band valance band offset split in GaAs/AlAs heterojunctions evidenced extensively in [91]. (It should be noted that this rule only applies to the direct Γ-Γ bandgap and not indirect bandgaps as seen for AlGaAs with Al fractions higher than 40% [143]), the affinity of thin AlAs layers was set as 3.15 eV throughout this work. This value ensures that the ratio between the conduction band and valence band offsets is 65:35 when the affinity of GaAs is 4.07 eV and the band gap is 1.42eV as is the case in the ATLAS library.

4.2.4. Simulation Models

The next step after the material models are specified is to specify the simulation models. This is done using the *model* statement. ATLAS provides a large number of models that can be used for a wide range of applications. These include whether the simulation uses Fermi-Dirac statistics or Boltzmann statistics. For the purposes of this work the Fermi-Dirac model was used for carrier statistics as the device physics are mainly quantum mechanical in nature. The other model used predominantly in this

work is the *semiconductor-insulator-semiconductor* (SIS) model. In this model the transmission probability is obtained by solving the 1D Schrodinger equation using a transfer matrix method. This is done for all possible values of the carrier energy to create a transmission probability function *T(E)*. From this the current density flowing through the barrier can then be determined utilising Equation 4.2.7 below.

$$J = \frac{qm^{*}kT}{2\pi^{2}h^{3}} \int_{0}^{\infty} T(E) \ln \left\{ \frac{1 + e^{\left(\frac{E_{Fr} - E}{kT}\right)}}{1 + e^{\left(\frac{E_{Fl} - E}{kT}\right)}} \right\} dE$$

4.2.7

Where m^{*} is the material effective mass, k is Boltzmann's constant and h is the Planck constant. E_{Fr} and E_{Fl} represent the quasi fermi levels of the spacers located at the right and left side of the barrier. From the current density, the electrical characteristics of the device can be determined by the device geometry. For this model to work, it is important to define the regions in which the tunnelling occurs using the statement *qtregion*.

4.2.5. Traps and Defects

Traps are caused by defects in the semiconductor crystal. These can be due to discontinuities in the lattice periodicity at interfaces or other crystal defects. The traps provide deep lying energy states in the forbidden bandgap region. These deep lying states trap charge carriers degrading device performance.

There are two types of traps: acceptor trap and donor trap. When implemented in ATLAS, traps alter the Shockley-Read-Hall equations of recombination to reduce the

carrier lifetimes. The conduction band and valence band have acceptor and donor traps respectively with energies E_{ta} and E_{td}. This is shown in Figure 4.2.3.

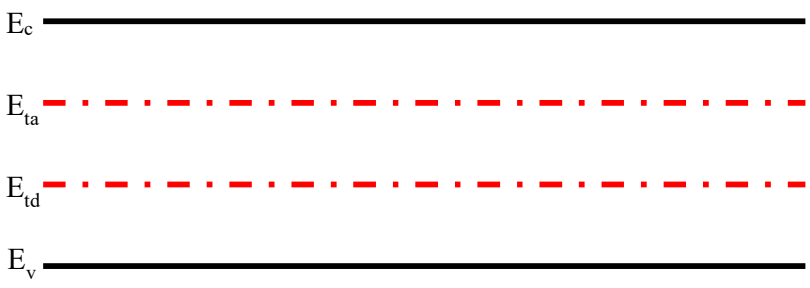

Figure 4.2.3 Definition of trap energy levels for acceptor and donor traps relative to the conduction and valance bands.

In ATLAS traps can be implemented at interfaces between materials or uniformly distributed throughout a region. This is done using the commands *inttrap* and *trap* respectively. In this work traps were implemented as interface traps between AlAs barriers and intrinsic spacer layers. Figure 4.2.4 shows the effect of traps implemented in DC simulations of GaAs/AlAs ASPAT diodes.

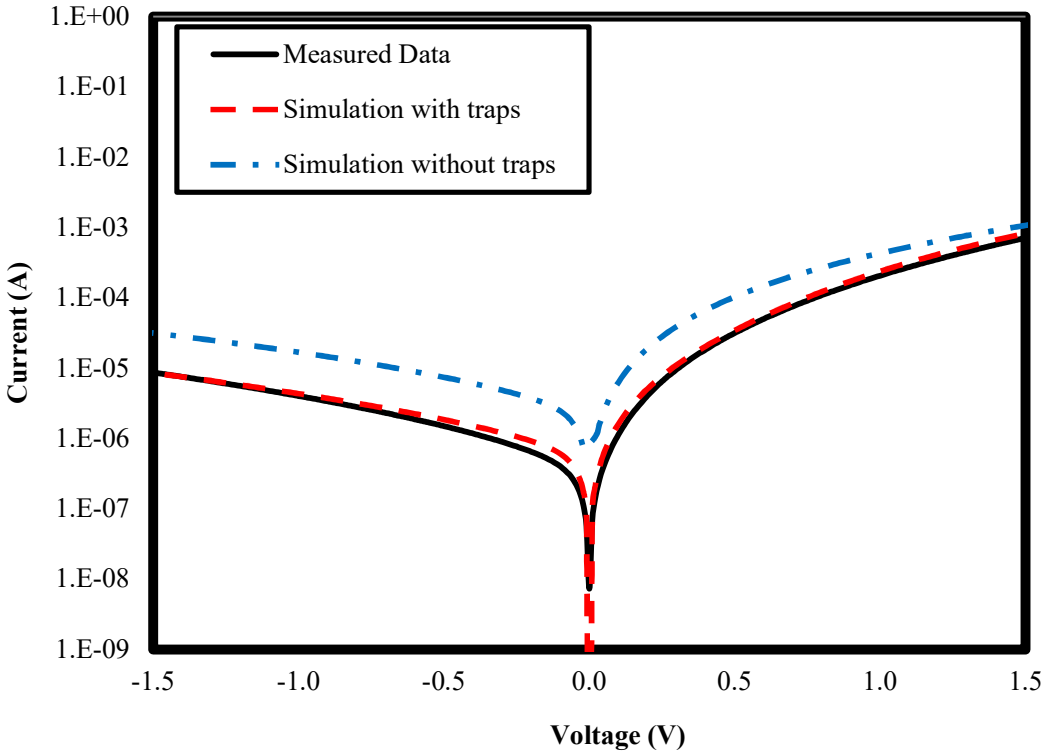

Figure 4.2.4 ATLAS simulations of GaAs/AlAs ASPAT with and without traps.

4.3. Equivalent Modelling and Parameter Extraction

As has been discussed previously in Chapter 3, the RF characteristics of the device were extracted from measured S_{11} data up to 40GHz using an equivalent circuit model. This model was created in Agilent Advanced design systems (ADS) software and the S_{11} parameter of the equivalent circuit were simulated up to 40GHz. Figure 4.3.1 shows the equivalent circuits of the intrinsic device parameters such as the junction resistance, R_j, the junction capacitance C_j, and the series resistance, R_s, which as described in Chapter 3 contains contributions from the epilayers, contacts and spreading resistance, whilst Figure 4.3.2 shows a full equivalent circuit model including the parasitic capacitance C_p and inductance L_p. The values of the parasitic components are determined by the two step de-embedding process as described in Chapter 3. The value of the junction resistance is determined from the devices current-voltage curve as it is several orders of magnitude larger than the series resistance. The remaining parameters are extracted by tuning their values until a close fit is observed between the measured S_{11} parameter and the simulated S_{11} parameter. An example of this is shown in Figure 4.3.3 for GaAs/AlAs and InGaAs/AlAs ASPAT devices.

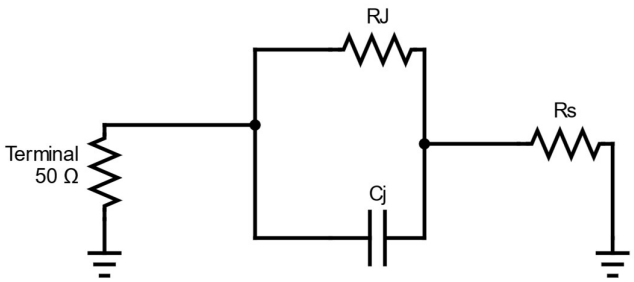

Figure 4.3.1 Equivalent circuit of intrinsic device parameters.

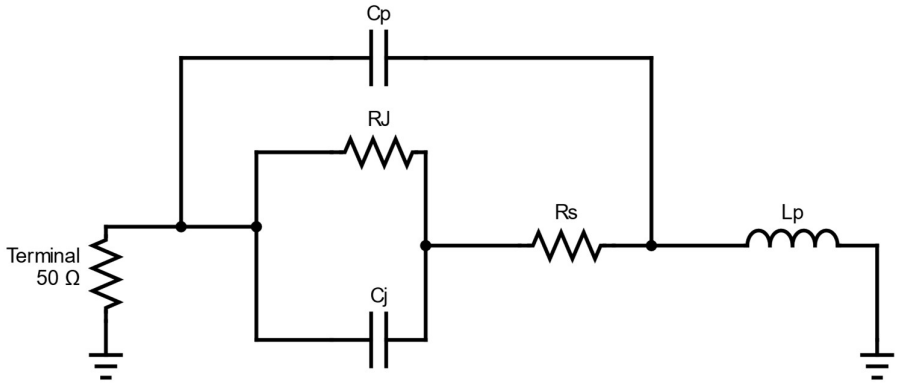

Figure 4.3.2 Full equivalent circuit of device parameters including parasitic components.

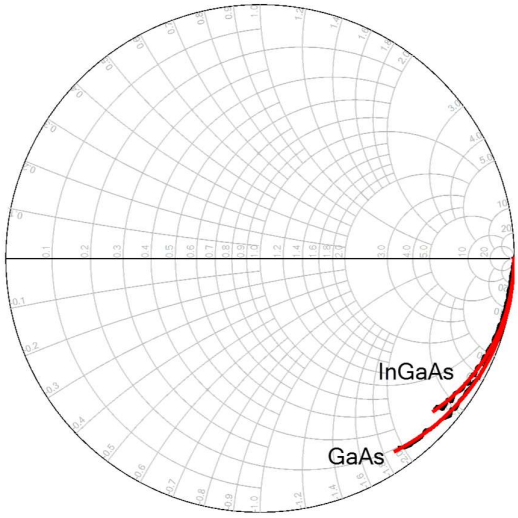

Figure 4.3.3 Smith Chart of measured and simulated S_{11} parameter for $4\times4\mu m^2$ GaAs/AlAs and InGaAs/AlAs ASPATs showing a close fit.

4.4. Conclusion

In this chapter the fundamentals of physical models and numerical simulation were briefly discussed. The specifics of SILVACO ATLAS simulation and its implementation in this work was discussed in detail. This included a run-down of the ATLAS file architecture and syntax. It was noted that for the input file to run successfully it was necessary that the statement groups were correctly ordered. The specifics of the coordinate system used in this work and the specification of the device structure was discussed.

The material models used in this work were discussed in depth, especially the InGaAs system and AlGaAs system and their dependence on indium and aluminium composition respectively. As the devices simulated in this work used thin AlAs barriers in which tunnelling occurs across the Γ-Γ direct band gap, the band gap and effective mass in these layers were changed to reflect this. The affinity of AlAs used in this work was also changed to adhere to the well-known 65:35 conduction valence band offset split.

The *semiconductor-insulator-semiconductor* model used in this work to model the quantum tunnelling mechanism was discussed in detail. This model solves the Schrödinger equation using the transfer matrix method to find the transmission

probability as a function of energy. This is then integrated across the particle energies to determine the current density of the device. The implementation of traps and defects at semiconductor interfaces was discussed.

The implementation of equivalent circuit models to extract the RF characteristics of devices was discussed. This included specifics about the intrinsic equivalent circuit and the full equivalent circuit including parasitic components. Agilent ADS is then used to simulate the S_{11} parameter of these equivalent circuits and the circuit parameters tuned until a close fit to measured data is achieved. From this the device parameters can be extracted.

CHAPTER 5

ASPAT DIODES

5.1. Introduction

As discussed in Chapter 2 the Asymmetric Spacer Layer Tunnel Diode (ASPAT) is a tunnel diode, first invented in 1992 by Syme and Kelly [86], consisting of a single thin AlAs barrier (of the order 3nm) sandwiched between two layers of intrinsic semiconductor. The two intrinsic layers are spacers from the doped layers used for contacts and carrier providers. These layers are asymmetric in thickness with a typical ratio of 40:1.

The devices discussed in this chapter and throughout this work were grown using MBE. As discussed earlier in Chapter 2, quantum tunnelling is exponentially dependent on the width of the barrier and as such it is necessary to control the growth of the barrier to extreme precision. A single monolayer difference results in a 270% difference in current in the device [101], [102]. However, recent work has shown that through careful growth conditions, a 1% variation across the wafer can be produced and a 1% variation from wafer to wafer [101][144].

Before the design and modelling of new structures can be performed, it is necessary that an accurate model of existing ASPAT structures is created. The University of Manchester group has two well understood ASPAT device structures. The first one is a GaAs/AlAs structure grown on a GaAs substrate and the second a $In_{0.53}Ga_{0.47}As$/AlAs ASPAT grown on an InP substrate. This chapter will focus on the accurate modelling of these ASPAT structures and the characterisation of their DC and RF properties. These ASPATs will form the benchmark of performance against which the new structures that form this work will be measured against. The ASPATs in this chapter are designed for applications as part of a detection circuit for both microwaves, millimetre waves and the low end of the THz spectrum.

5.2. Diode Structures

The two standard ASPAT devices for the University of Manchester Group were both grown in house using a Riber V100H solid source molecular beam epitaxy system. Both devices were developed on semi-insulating (SI) GaAs and InP substrates for GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPAT devices, respectively. The wafers were processed using i-line optical photolithography techniques to create devices of mesa areas 10× 10 μm², 6 × 6 μm² and 4 × 4 μm². The contacts of the GaAs/AlAs ASPAT diodes used an alloy of Au/Ge/Ni, whereas the $In_{0.53}Ga_{0.47}As$ ASPAT diodes used non-alloyed Pd/Ti/Pd/Au. Both ASPAT diodes applied the Ti/Au metal scheme as their Ground-Signal-Ground (GSG) coplanar waveguide for both DC and AC characterisations.

Table 5.2.1 Epitaxial layers of standard GaAs and $In_{0.53}Ga_{0.47}As$ ASPAT diodes

	GaAs ASPAT	*$In_{0.53}Ga_{0.47}As$ ASPAT*
	GaAs 4×10^{18} cm^{-3}	$In_{0.53}Ga_{0.47}As$ 1.5×10^{19} cm^{-3}
	GaAs 1×10^{17} cm^{-3}	$In_{0.53}Ga_{0.47}As$ 1×10^{17} cm^{-3}
5nm	GaAs (spacer 2)	$In_{0.53}Ga_{0.47}As$ (spacer 1)
2.8nm	AlAs (barrier)	AlAs (barrier)
200nm	GaAs (spacer 2)	$In_{0.53}Ga_{0.47}As$ (spacer 2)
	GaAs 1×10^{17} cm^{-3}	$In_{0.53}Ga_{0.47}As$ 1×10^{17} cm^{-3}
	GaAs 4×10^{18} cm^{-3}	$In_{0.53}Ga_{0.47}As$ 1.5×10^{19} cm^{-3}

The epitaxial profiles of these devices are shown in Table 5.2.1. As can be seen, the active spacer and barrier layers of the devices are of identical thickness. Therefore, any differences in device performance are due to the different spacer materials. The two spacer thicknesses are 5nm and 200nm to give a ratio of 40:1. The AlAs barrier is 2.83nm for both devices corresponding to a thickness of 10 monolayers. Both devices

contain lightly n-doped emitter and collector layers with a doping concentration of 1×10^{17} cm^{-3}. The doping of the ohmic contact layers for both devices was not the same with the GaAs/AlAs device having a doping of 4×10^{18} cm^{-3} and the $In_{0.53}Ga_{0.47}As$/AlAs device having a doping of 1.5×10^{19} cm^{-3}. This was done to reduce the contact resistance of both device structures and as a footnote it is possible to dope $In_{0.53}Ga_{0.47}As$ to much higher values than GaAs to reduce the contact resistance even further.

It should be noted that the strain on the AlAs barrier is greater in the $In_{0.53}Ga_{0.47}As$/AlAs device compared with the GaAs/AlAs device due to the difference in lattice constant. However, as the barrier thickness is well below the critical thickness for pseudomorphic growth on InP, the layer thickness is not different between the devices.

5.3. Diode Models

5.3.1. Model Definition

Models were made in SILVACO ATLAS for both ASPAT diodes. The devices were specified with 7 regions with each region corresponding with an epitaxial layer. An example of this model is given in Figure 5.3.1

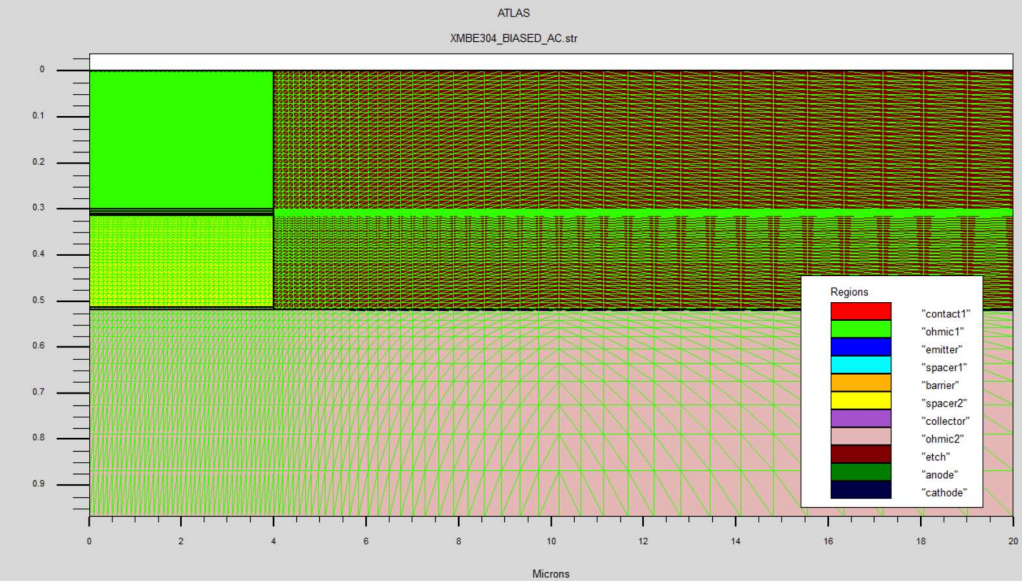

Figure 5.3.1 Side view of a SILVACO ATLAS model of GaAs ASPAT with mesh shown in green.

Both emitter and collector regions rely on the biasing condition. The left and right areas of the collector and the emitter contacts are in quasi-equilibrium, whereas the central device region with the barrier structure was treated as being in non-equilibrium using the *Semiconductor-Insulator-Semiconductor* (SIS) solver. When the devices are biased, the band structure bends allowing for an accumulation layer to form at the base of the barrier as described in Chapter 2. This can be seen in Figure 2.4.2.

The tunnelling current is then calculated by solving the 1D Schrödinger equation using the transfer matrix method to give a transmission probability for all values of electron energy. This is then integrated according to Equation 4.2.7 to give the current density. This is then integrated over the device geometry to find the simulated characteristics of the device.

5.3.2. Material Definition

When modelling the characteristics of the device the most important factor is the accurate definition of the material parameters. The most important of these parameters are the band gap, affinity and effective mass of the materials. The material models used in the simulation of the ASPAT devices are described in detail in Chapter 4. However, they will also be summarised here.

The standard ATLAS library values of the affinity, bandgap and effective mass were used for GaAs in the simulation of the GaAs/AlAs ASPAT. However, the values of these parameters for AlAs were changed to reflect the nature of the thin barrier. Firstly, the direct Γ-valley bandgap of 2.83eV instead of the indirect 2.12eV X-valley was used as this is the tunnelling mechanism for the ASPAT. Secondly, the affinity was changed from the 3.5eV book value for bulk AlAs to 3.15eV so that the 65.35 rule for conduction and valence band offsets in GaAs/AlAs interfaces was observed when the band structure was calculated using Anderson's rule. The effective mass of the AlAs barrier was chosen to be close to the Γ-valley book value while still providing a good fit and was defined as $0.12m_e$.

The values of the bandgap, affinity and effective mass for $In_{0.53}Ga_{0.47}As$ were calculated from the equations in Chapter 4. These were then user defined in ATLAS for the simulation. The value of the affinity was 4.5eV. The value of the bandgap was

0.74eV and the value of the effective mass was $0.041m_e$. Table 5.3.1 summarises the values used for the parameters for all materials.

Table 5.3.1 Affinity, Bandgap and effective masses of material models

Material	Effective Mass m_e	Affinity (eV)	Bandgap (eV)
GaAs	0.067	4.07	1.4
$In_{0.47}Ga_{0.53}As$	0.041	4.5	0.74
AlAs	0.12	3.15	2.8

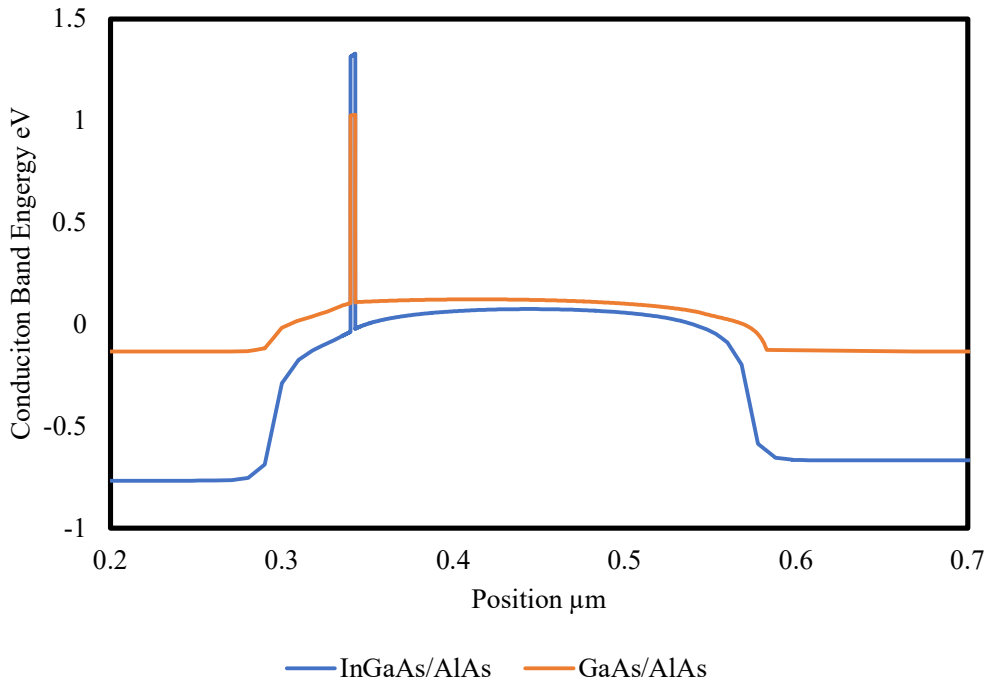

Figure 5.3.2 Conduction band profiles for GaAs/AlAs and InGaAs/AlAs ASPATs

The band diagram for both ASPATs can be extracted from ATLAS and the barrier heights measured. As can be seen from Figure 5.3.2, the $In_{0.53}Ga_{0.47}As$/AlAs ASPAT has a much higher barrier in the conduction band due to is lower band gap. The barrier height of the GaAs/AlAs ASPAT is 0.92 eV whilst the $In_{0.53}Ga_{0.47}As$/AlAs ASPAT has a height of 1.35 eV. This means that the $In_{0.53}Ga_{0.47}As$/AlAs ASPAT has a suppressed thermionic emission mechanism compared to the GaAs/AlAs device.

5.4. DC Characteristics

The DC characteristics of the GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs fabricated ASPAT devices were measured for 10×10 μm², 6×6 μm² and 4×4 μm² devices using a semiconductor parameter analyser (i.e. Agilent B1500). The current-voltage characteristic was measured from -1.5V to 1.5V with bias steps of 0.01V at room temperature. This was then compared with the simulated DC characteristics of devices of the same size to ensure that the models used throughout this work show good agreement with experiment.

The junction resistance and curvature coefficient of the devices were also extracted from the measured and simulated data using equation 2.5.11 and equation. 2.5.12 The devices current densities were also determined by dividing by the device mesa area. It is important that the effects of the undercut are taken into consideration when determining the device mesa area for the purposes of calculating current density and as such the nominal device areas used to label the devices are not the same as the area used in these calculations.

The current-voltage characteristics of the ASPAT devices are shown on logarithmic scales for the GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPATS in Figure 5.4.1 and Figure 5.4.2 respectively. As can be seen from these figures, a good match between the measured and simulated data was achieved for both types of ASPAT. The Current-density voltage curves are plotted for both ASPATs on linear scales in Figure 5.4.3 and Figure 5.4.4. From these, it can be seen that the devices scale as expected with area and that there is a close agreement between the simulated and measured data.

The extracted DC parameters of the ASPATs are also shown below with Figure 5.4.5 and Figure 5.4.6 showing the devices junction resistances and Figure 5.4.7 and Figure 5.4.8 showing the extracted curvature coefficients.

Due to the k_v data being the ratio of two derivatives small amounts of noise in the measured I-V data leads to large amounts of noise in the extracted curves. This noise cannot be smoothed out of the data using averaging techniques as this reduces the accuracy of the derivative approximations and hence the extracted values of k_v.

Additionally, as the ASPATs IV curve is not a simple exponential function, fitting these curves to find the derivatives could not be achieved.

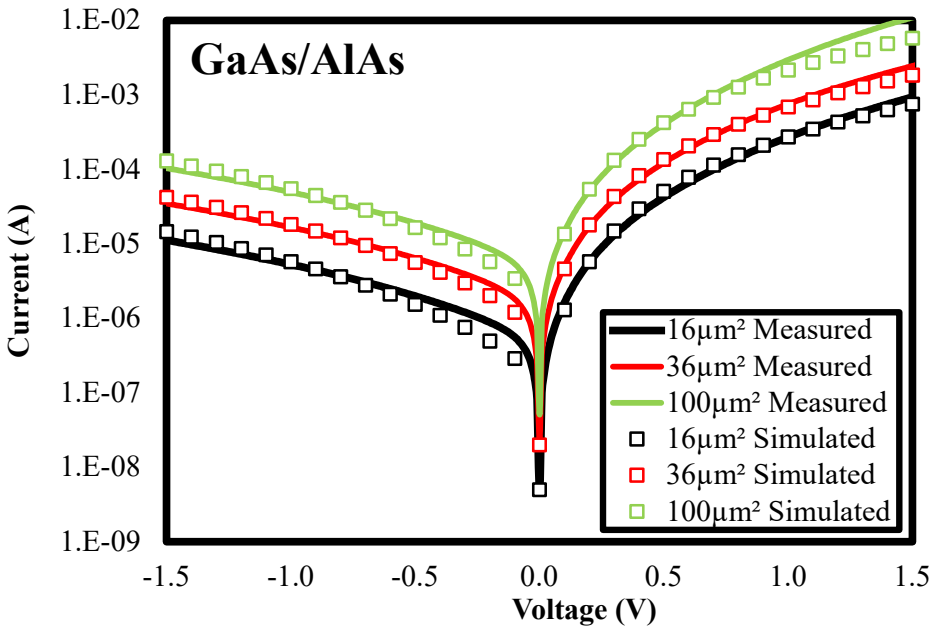

Figure 5.4.1 The measured and simulated Current-Voltage characteristics of GaAs/AlAs ASPAT diodes with mesa areas of 10×10 µm², 6×6 µm² and 4×4 µm²

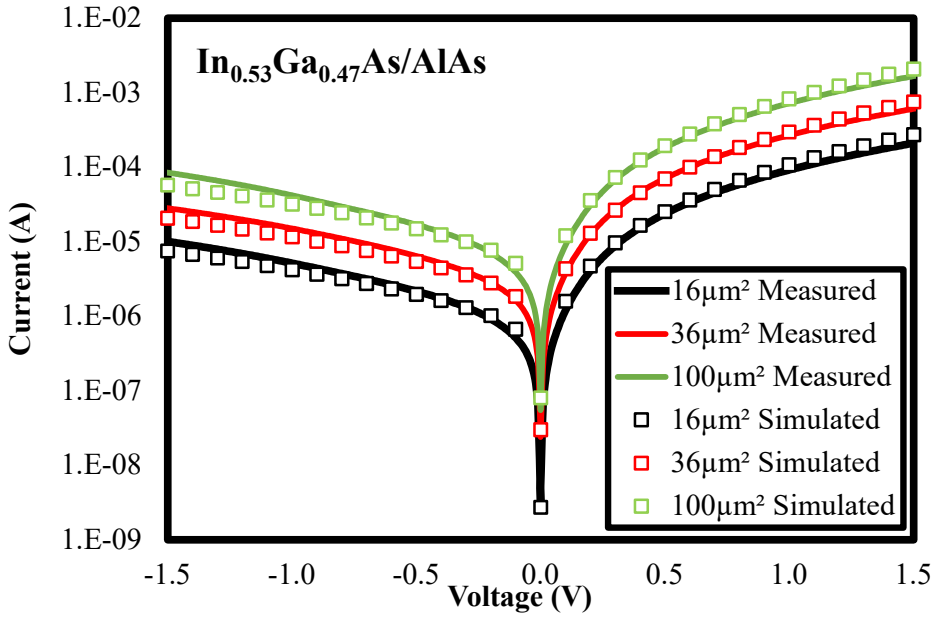

Figure 5.4.2 Current-Voltage characteristics of measured and simulated $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diodes with mesa areas of 10×10 µm², 6×6 µm² and 4×4 µm².

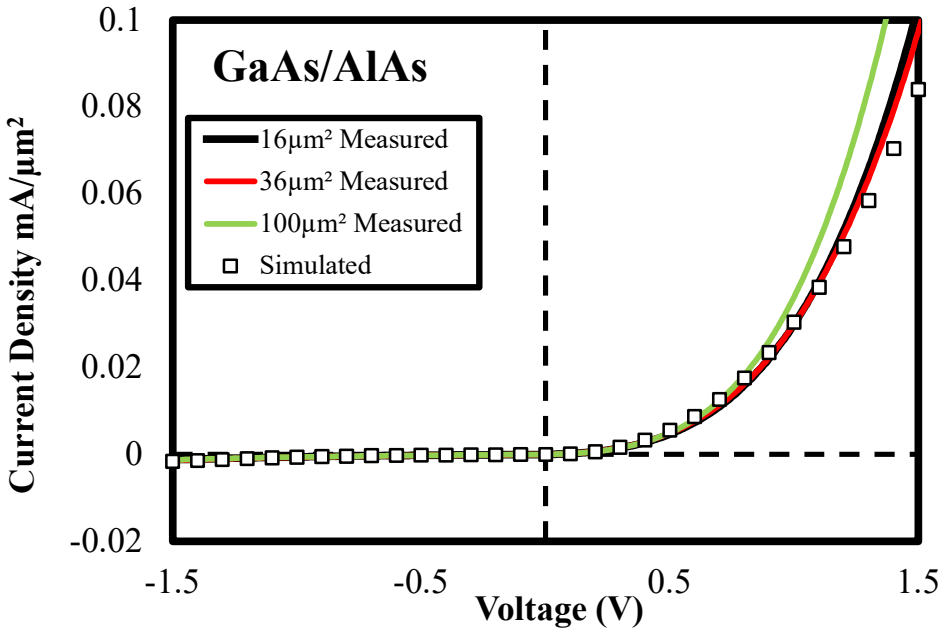

Figure 5.4.3 Current density of measured and simulated GaAs/AlAs ASPAT diodes with mesa areas of 10×10 µm², 6×6 µm² and 4×4 µm².

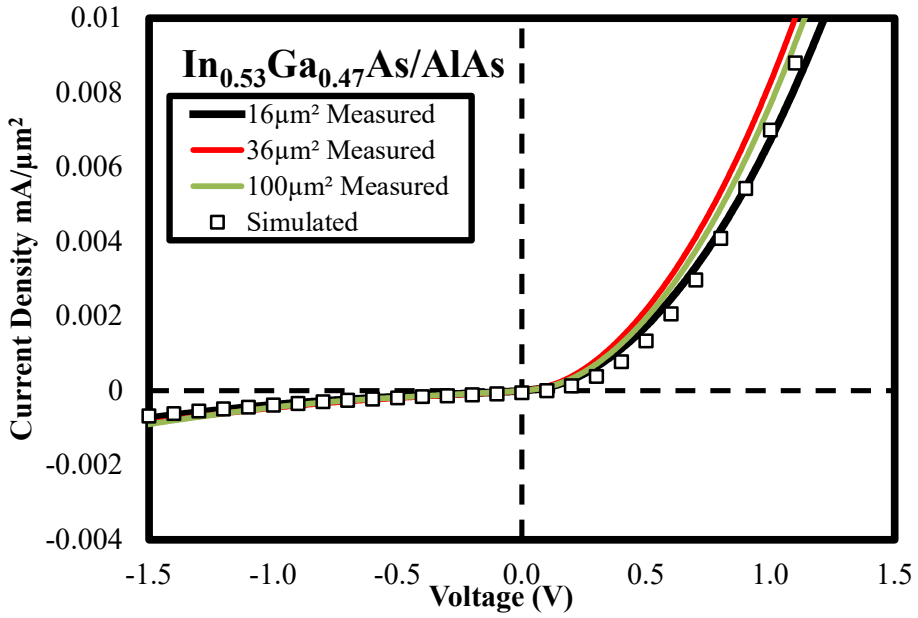

Figure 5.4.4 Current density of measured and simulated $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diodes with mesa areas of 10×10 µm², 6×6 µm² and 4×4 µm².

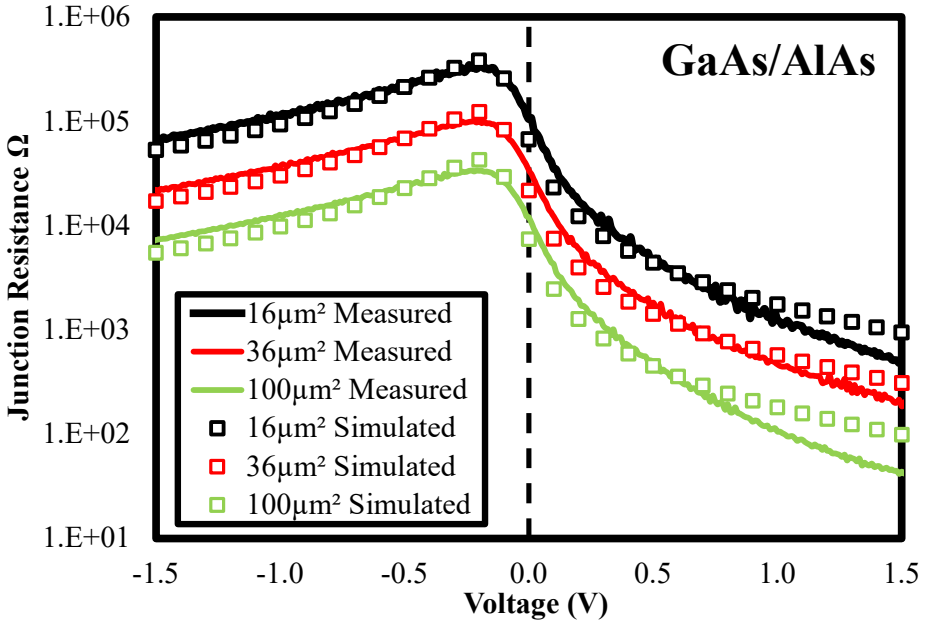

Figure 5.4.5 Junction Resistance of measured and simulated GaAs/AlAs ASPAT diodes with mesa areas of 10×10 µm², 6×6 µm² and 4×4 µm².

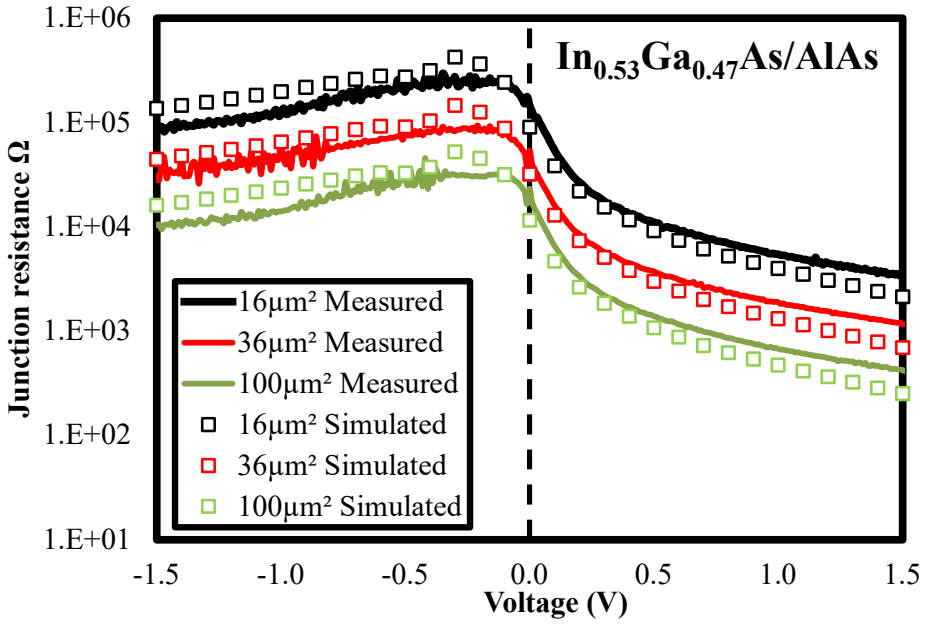

Figure 5.4.6 Junction resistance of measured and simulated $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diodes with mesa areas of 10×10 μm², 6×6 μm² and 4×4 μm².

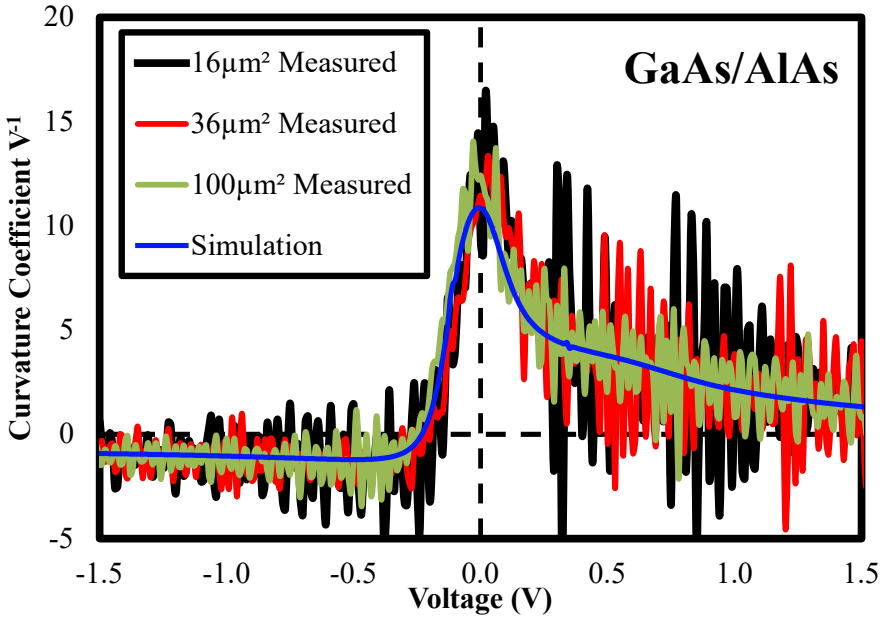

Figure 5.4.7 Curvature coefficient of measured and simulated GaAs/AlAs ASPAT diodes with mesa areas of 10×10 μm², 6×6 μm² and 4×4 μm².

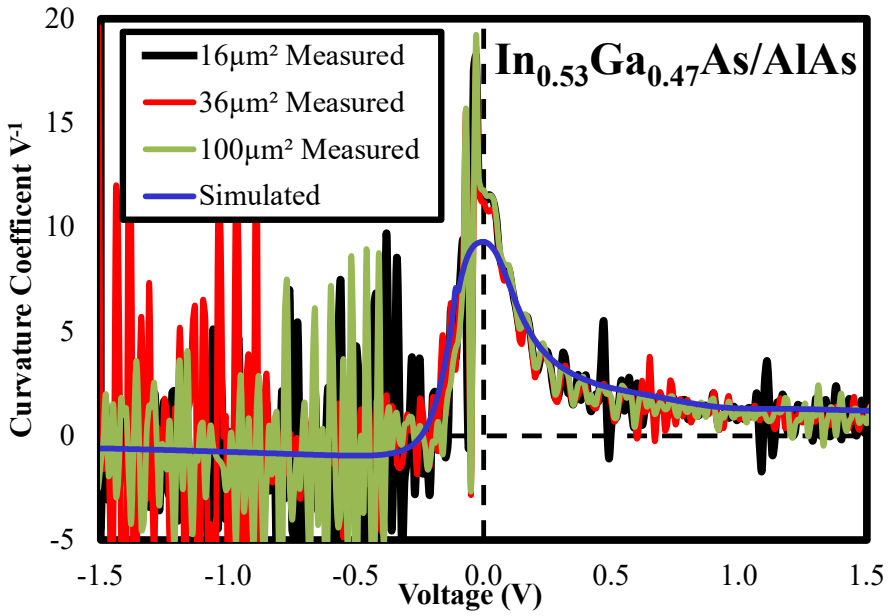

Figure 5.4.8 Curvature coefficient of measured and simulated $In_{0.53}Ga_{0.47}As/AlAs$ ASPAT diodes with mesa areas of 10×10 μm², 6×6 μm² and 4×4 μm².

From the data we can see that the junction resistance of the GaAs/AlAs devices is lower than the junction resistance of the $In_{0.53}Ga_{0.47}As$/AlAs ASPATs in the forward bias with an R_j of 1.2kΩ and 5.5kΩ at 1V for 16μm^2 GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPATs respectively. This is due to the higher barrier for the $In_{0.53}Ga_{0.47}As$/AlAs ASPATs supressing thermionic emission at higher forward biases. In reverse bias the junction resistances are comparable between the ASPATs with the $In_{0.53}Ga_{0.47}As$/AlAs ASPAT showing a junction resistance of 120kΩ at -1Vfor a 16μm^2 device compared with 114kΩ for the GaAs/AlAs ASPAT. At zero bias, which is the designed operating point of the ASPAT, the GaAs/AlAs ASPAT shows a junction resistance of 104kΩ for a 16μm^2 device compared with 147kΩ for the $In_{0.53}Ga_{0.47}As$/AlAs ASPAT. The junction resistances of the other device sizes at -1V, 0V and 1V are shown in Table 5.4.1.

The simulated junction resistances show a good agreement with the measured data in terms of shape however the simulation underestimates the R_j at zero bias by a factor of 20-40%. However, as this is the point at which the junction resistance drops by 2 orders of magnitude, the simulated results are acceptably close to allow the models to be used to simulate new structures, as will be demonstrated in Chapters 7 & 8.

Table 5.4.1 Table of measured and simulated device junction resistances at -1V, 0V and 1V

Device Size	16μm^2			36 μm^2			100 μm^2		
Junction Resistance kΩ	-1V	0V	1V	-1V	0V	1V	-1V	0V	1V
GaAs Measured	114	104	1.2	37	34	0.5	13	12	0.1
GaAs Simulated	93	67	1.7	30	22	0.6	10	7	0.2
$In_{0.53}Ga_{0.47}As$ Measured	120	128	5.5	64	54	1.9	14	17	0.7
$In_{0.53}Ga_{0.47}As$ Simulated	199	91	4	65	32	1.3	24	12	0.5

The curvature coefficient is at a maximum at 0V for both devices and remains constant for devices of all areas, as would be expected. The GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPATs show a 0V k_v of ~$12V^{-1}$ and ~$11V^{-1}$ respectively. The extracted curvature coefficient for the GaAs/AlAs simulated IV curve shows a curvature coefficient of $11V^{-1}$ whilst the extracted curvature coefficient for the $In_{0.53}Ga_{0.47}As$/AlAs simulation is also $11V^{-1}$. The exact values of the measured curvature coefficients are difficult to ascertain due to noise in the measurement. The curves can be smoothed by using larger voltage steps. However, this results in a change in the calculated curvature coefficient as the approximation of the derivatives becomes less accurate. As such the data has been left unsmoothed.

5.5. RF Characteristics

The RF characteristics of the fabricated ASPAT devices were explored by measuring the device S11 scattering parameters and then extracting the RF characteristics using an equivalent circuit model created in Agilent Advanced design systems software, as explained in Chapter 4. Figure 5.5.1 shows the equivalent circuit model used in these simulations. The measurements were made at room temperature from 40MHz to 40GHz in steps of 40MHz and from -0.5V to 0.5V in steps of 0.1V. The simulations were run using the same steps.

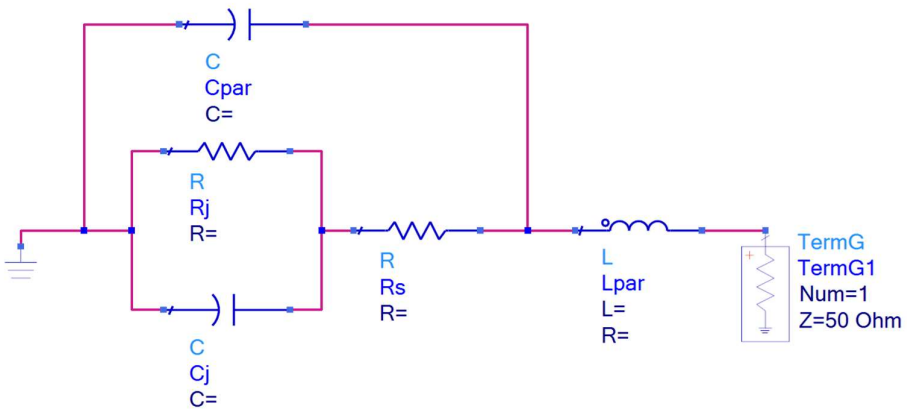

Figure 5.5.1: Equivalent Circuit model of ASPAT devices with parasitic inductance and capacitance L_{par} and C_{par}, series resistance R_s and junction capacitance and resistance R_j and C_j.

To determine the values of the parasitic capacitance and inductance a 2-step de-embedding procedure was used as described in Chapter 3. Open and short structures were fabricated and the S_{11} parameter measured up to 40GHz. The S_{11} parameters of the open and short equivalent circuits were then simulated and the values tuned until a close fit was achieved. Examples of these equivalent circuits for the open and short structures are shown in Figure 5.5.2 and the measured and simulated S_{11} parameters of the de-embedding structures for the GaAs and $In_{0.53}Ga_{0.47}As$ ASPATs are shown in Figure 5.5.3 and Figure 5.5.4 respectively. The parasitic inductance of the ASPATs was found to be 40pH in both cases and the parasitic capacitances were found to be 15fF for the GaAs ASPAT and 10fF for the $In_{0.53}Ga_{0.47}As$ ASPAT.

Once the values of C_p and L_p were found, the remaining values in the equivalent circuit simulation were tuned until a good match to the measured data was achieved. As R_j is much larger than the series resistance R_s it was assumed that the Rj derived from the DC characteristics was an appropriate value to use. R_s and C_j were then used as the free fitting parameters to achieve a good fit.

The zero-bias measured and simulated S_{11} data for $4\times4\mu m^2$, $6\times6\mu m^2$ and $10\times10\mu m^2$ GaAs and $In_{0.53}Ga_{0.47}As$ ASPATs are shown in Figure 5.5.5–Figure 5.5.10 and show excellent matches between measured data and simulation.

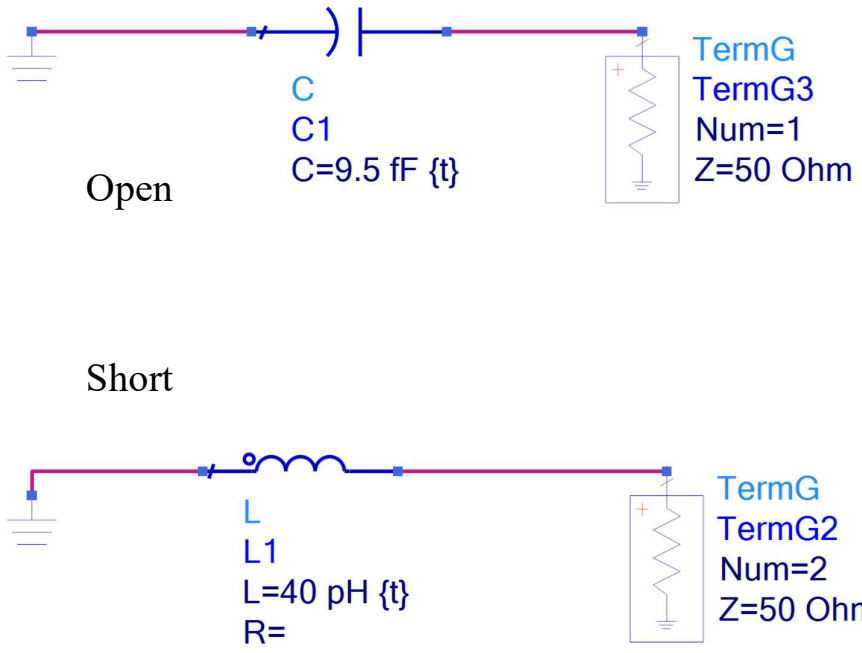

Figure 5.5.2 Equivalent circuits of open and short de-embedding structures for InGaAs ASPATs

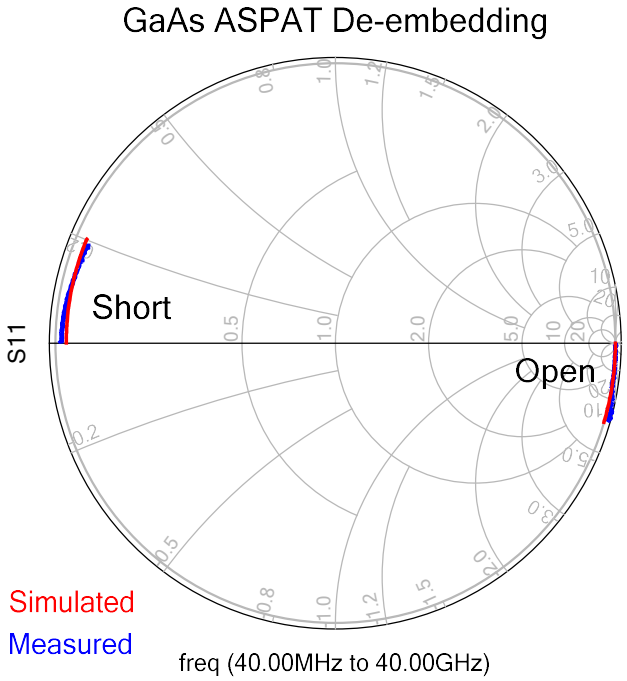

Figure 5.5.3: Smith chart showing measured and equivalent circuit S11 parameters of de-embedding structures for GaAs/AlAs ASPATs

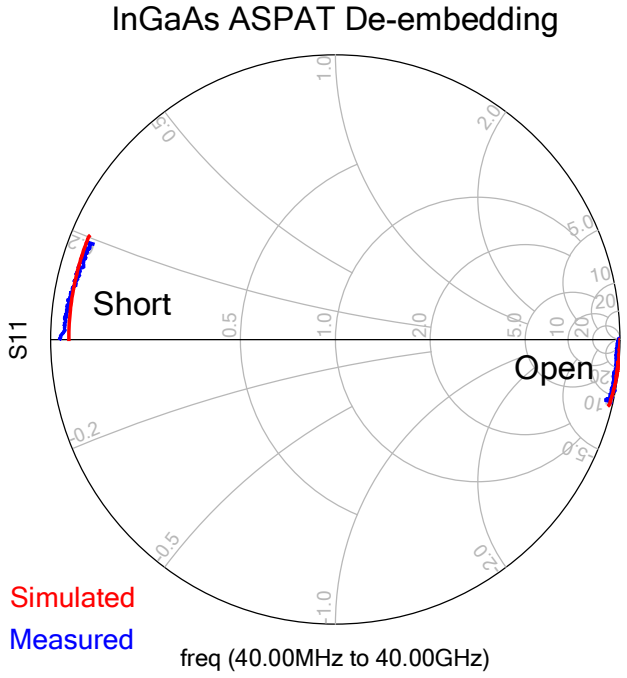

Figure 5.5.4 Smith chart showing measured and equivalent circuit S11 parameters of de-embedding structures for InGaAs/AlAs ASPATs

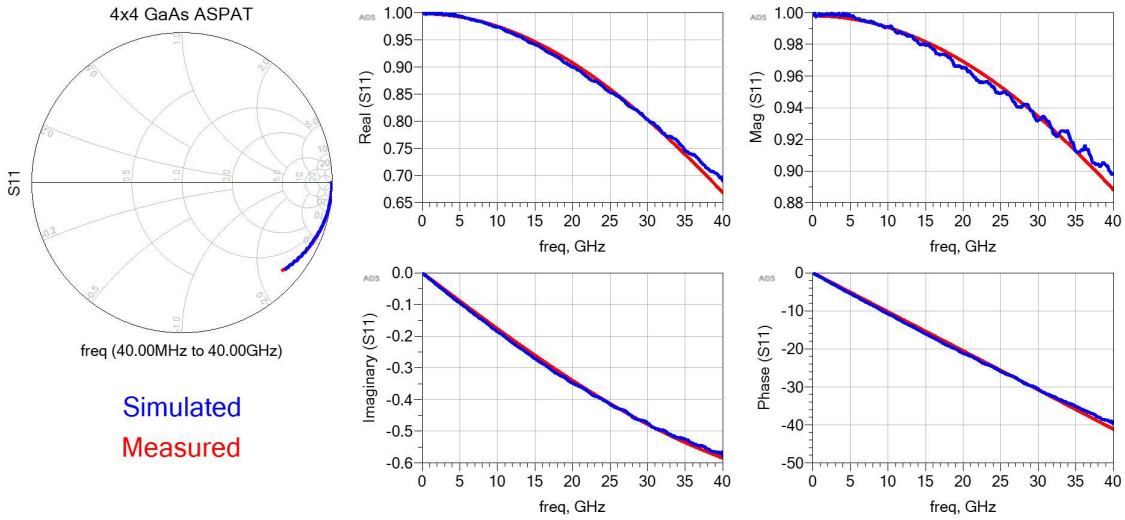

Figure 5.5.5 GaAs ASPAT measured and simulated S11 parameters for a $4\times4\mu m^2$ device at 0V

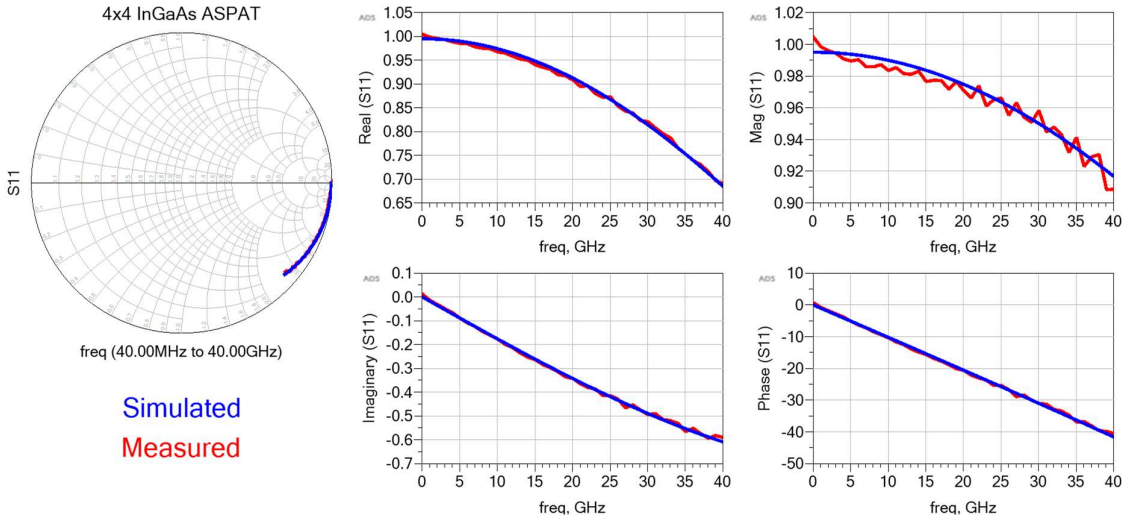

Figure 5.5.6 $In_{0.53}Ga_{0.47}As$ ASPAT measured and simulated S11 parameters for a $4\times4\mu m^2$ device at 0V

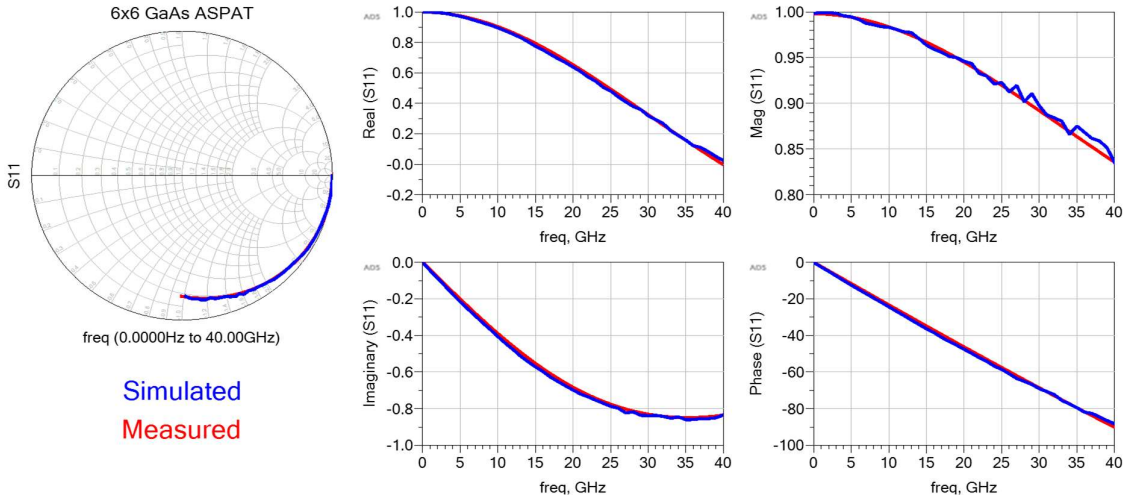

Figure 5.5.7 GaAs ASPAT measured and simulated S11 parameters for a 6×6μm^2 device at 0V

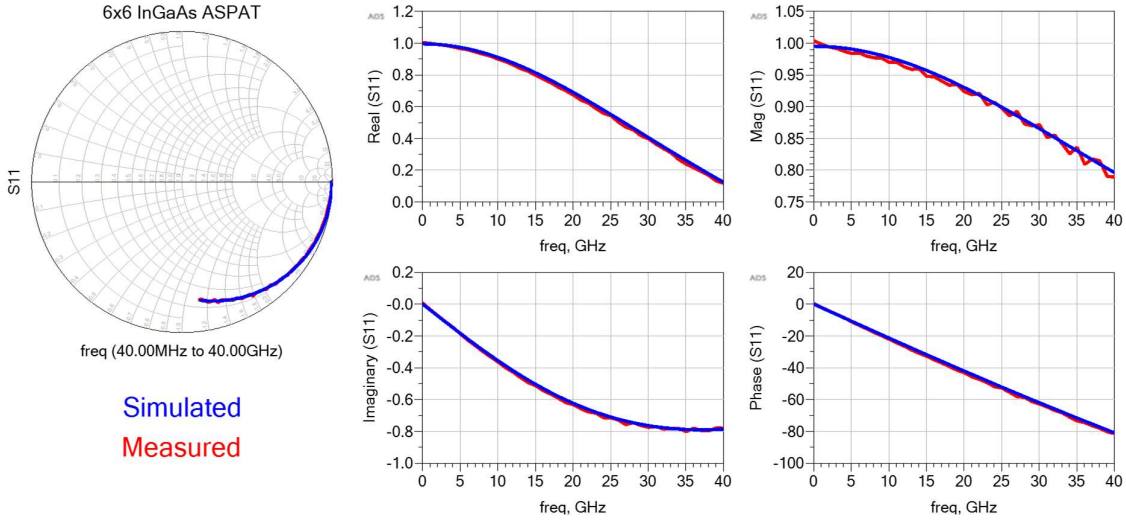

Figure 5.5.8 GaAs ASPAT measured and simulated S11 parameters for a 6×6μm^2 device at 0V

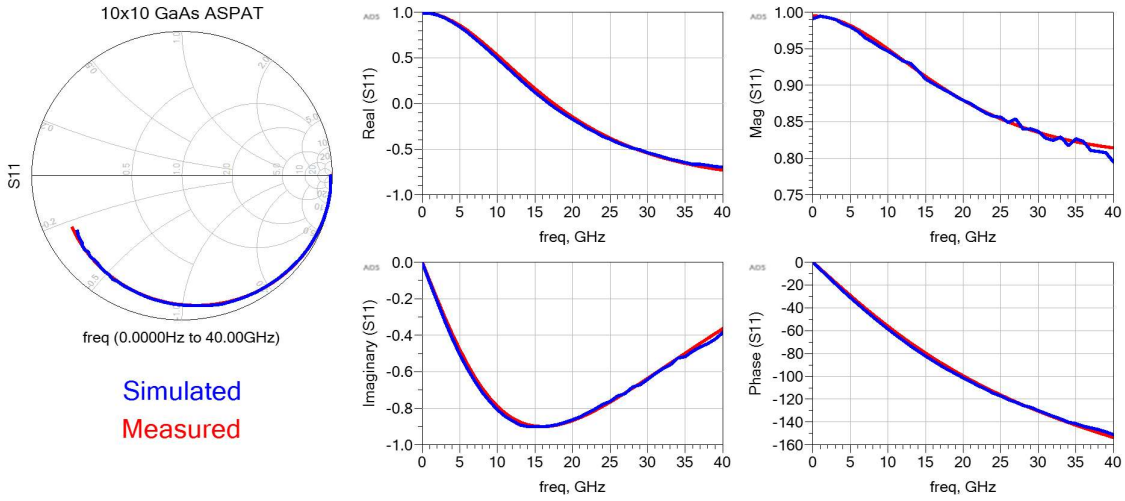

Figure 5.5.9 GaAs ASPAT measured and simulated S11 parameters for a $10\times10\mu m^2$ device at 0V

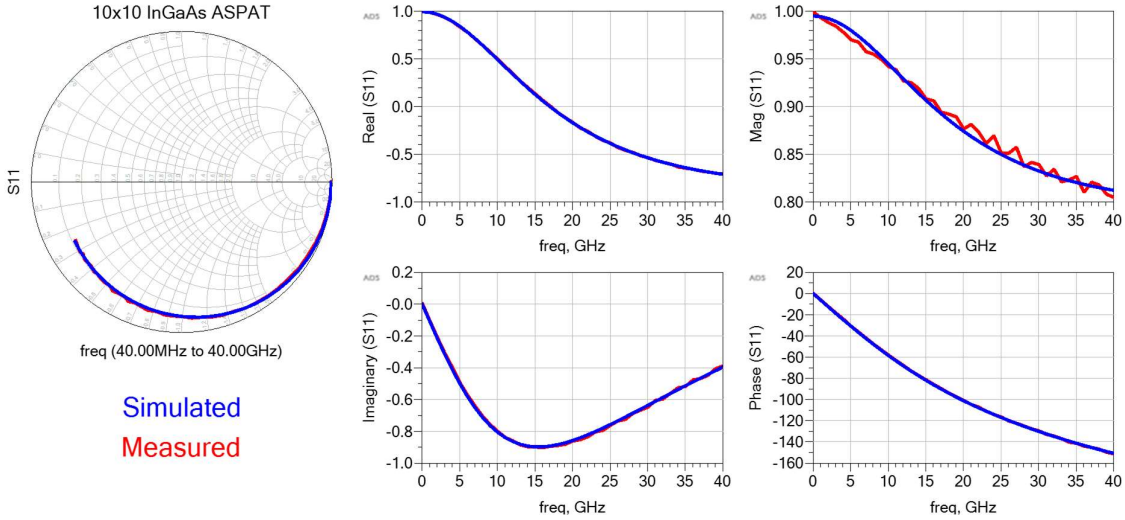

Figure 5.5.10 $In_{0.53}Ga_{0.47}As$ ASPAT measured and simulated S11 parameters for a $10\times10\mu m^2$ device at 0V

The junction capacitances of the two ASPAT devices are plotted against bias voltage below in Figure 5.5.11–Figure 5.5.13 for every device size. Figure 5.5.14–Figure 5.5.16 show the series resistances for every device size. As can be seen from the data, the devices showed higher junction capacitances at zero and forward bias despite having similar fully depleted capacitances at approximately -0.5V. The increase in capacitance under forward bias is caused by the 2-D states in the accumulation region at the base of the device barrier. The negative charge in this region is mirrored by the

positive charges in the device collector region. One method of reducing the zero bias and forward bias capacitance would be to increase the spacer between the barrier and the collector. However, this would degrade the device performance in terms of k_v as the spacer ratio is reduced.

The devices series resistance follows the behaviour of the junction capacitance and increases under zero and forward bias. This is due to the undoped spacer layers not being fully depleted. A similar effect has been previously reported for Schottky varactor diodes [145]. This is detrimental to the devices RF performance and reduces the devices cut-off frequencies. As such it is necessary to try and find a way to reduce this undoped spacer resistance. One method of achieving this would be to reduce the large spacer thickness. However, this would detrimentally affect the devices curvature coefficient due to the reduction in the spacer ratio.

The $In_{0.53}Ga_{0.47}As$ devices show consistently lower series resistance than the GaAs ASPATs. This is due to $In_{0.53}Ga_{0.47}As$ higher electron mobility and the increase in the ohmic contact layer doping to 1.5×10^{19} cm^{-3} compared with 4×10^{18} cm^{-3} for GaAs. This lowers the contribution to the series resistance from the spreading resistance R_{spr} as well as the contribution from the doped layers R_{epi}, as described in Chapter 3.

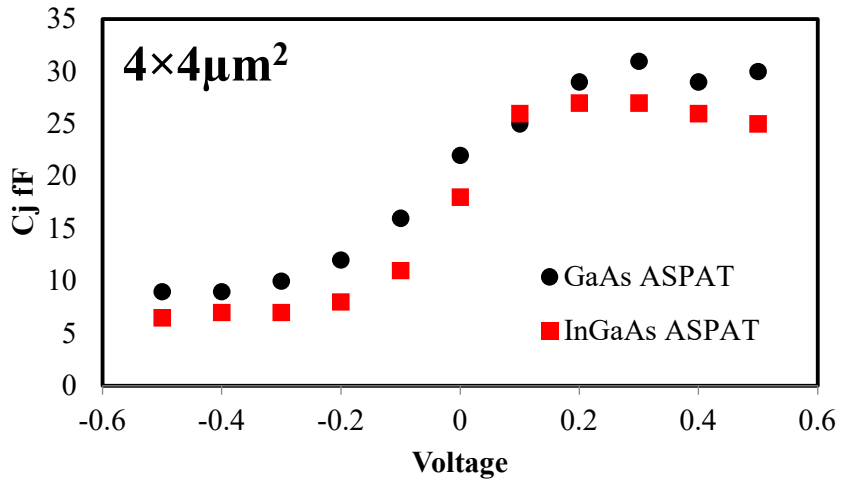

Figure 5.5.11 Extracted C_j of 16µm^2 GaAs and $In_{0.53}Ga_{0.47}As$ ASPATs plotted against voltage.

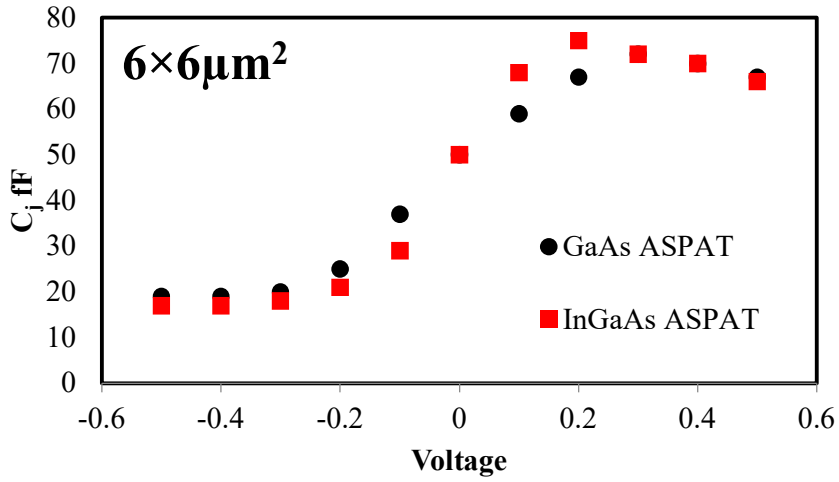

Figure 5.5.12 Extracted C_j of 36µm^2 GaAs and $In_{0.53}Ga_{0.47}As$ ASPATs plotted against voltage.

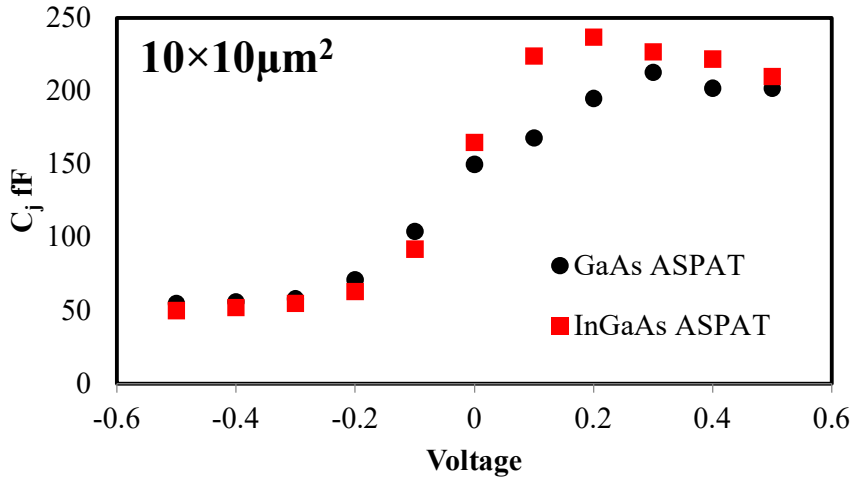

Figure 5.5.13 Extracted C_j of 100µm^2 GaAs and $In_{0.53}Ga_{0.47}As$ ASPATs plotted against voltage.

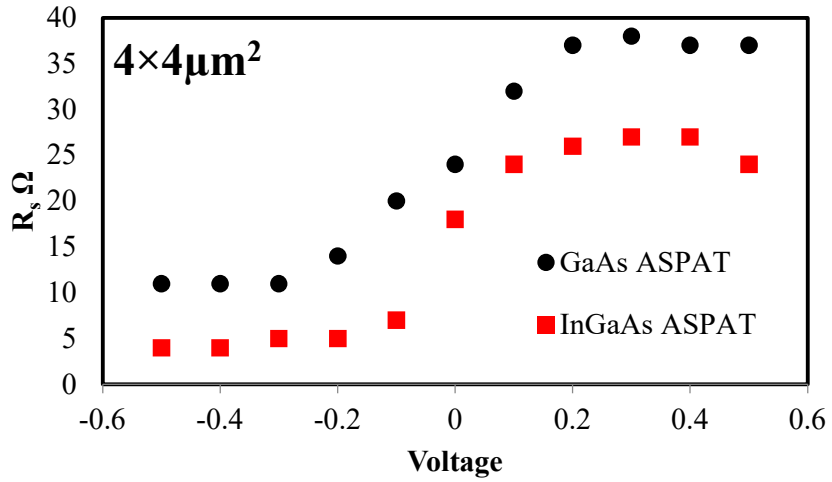

Figure 5.5.14 Extracted R_s of 16μm^2 GaAs and $In_{0.53}Ga_{0.47}As$ ASPATs plotted against voltage.

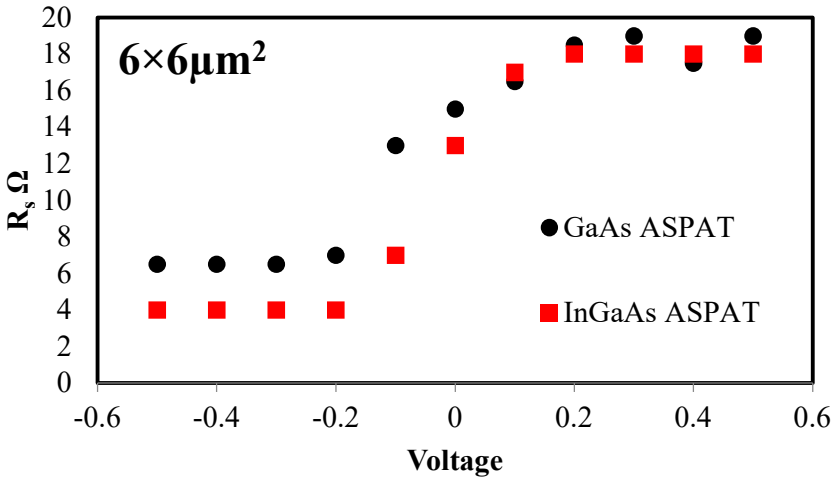

Figure 5.5.15 Extracted R_s of 36μm^2 GaAs and $In_{0.53}Ga_{0.47}As$ ASPATs plotted against voltage.

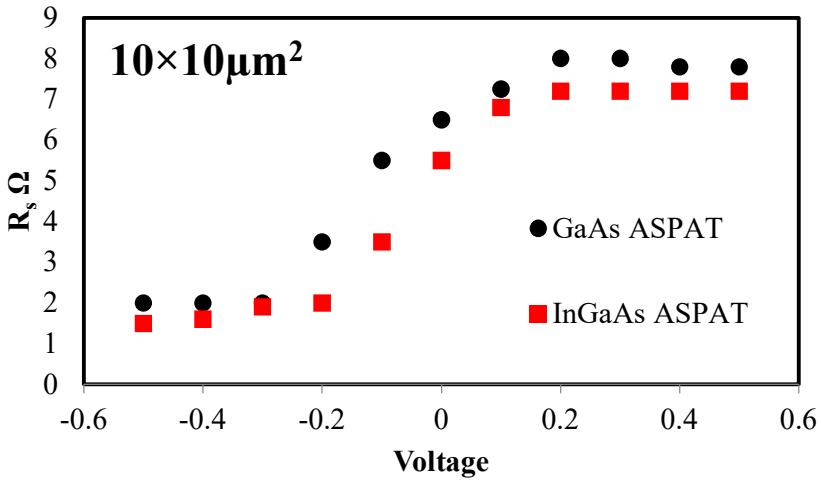

Figure 5.5.16 Extracted R_s of 100µm^2 GaAs and $In_{0.53}Ga_{0.47}As$ ASPATs plotted against voltage.

The extracted zero bias R_j, R_s and C_j are shown in Table 5.5.1 along with the device cut-off frequencies. As can be seen form the table, the cut off frequency of the $In_{0.53}Ga_{0.47}As$ devices is higher than those of the GaAs devices. This can be attributed mostly to the reduced series resistance of the $In_{0.53}Ga_{0.47}As$ devices.

Table 5.5.1 Extracted zero bias parameters and cut-off frequencies for GaAs and $In_{0.53}$-$Ga_{0.47}As$ ASPATs

Device Size	*Rj kΩ*	*Rs Ω*	*Cj fF*	*Cp fF*	*Lp pH*	*f_c GHz*
			GaAs ASPAT			
4×4µm²	104	24	22	15	50	301
6×6µm²	34	15	50	15	50	212
10×10µm²	12	7	150	15	50	163
			$In_{0.47}Ga_{0.53}As$ ASPAT			
4×4µm²	128	18	18	10	40	491
6×6µm²	54	13	50	10	40	245
10×10µm²	17	6	165	10	40	175

5.6. Conclusion

In this chapter, two standard ASPAT devices of size $4\times4\mu m^2$, $6\times6\mu m^2$ and $10\times10\mu m^2$ grown by MBE were explored. One based on the GaAs system and one based on $In_{0.53}Ga_{0.47}As$ lattice matched to InP. The devices were fabricated, and their DC characteristics measured. From the measured DC characteristics, the devices junction resistances were extracted and compared. The GaAs device showed a lower junction resistance than the $In_{0.53}Ga_{0.47}As$ devices owing to the higher band gap of GaAs causing a lower conduction band discontinuity at the GaAs/AlAs heterojunction and therefore a lower barrier than the $In_{0.53}Ga_{0.47}As$ devices. The devices curvature coefficients were extracted with the GaAs and the $In_{0.53}Ga_{0.47}As$ devices displaying zero bias curvatures of $12V^{-1}$ and $11V^{-1}$ respectively.

Physical models were created for both ASPAT devices in Silvaco ATLAS software. These models were used to simulate the DC characteristics of the ASPAT devices. The models show excellent agreement with the measured DC characteristics of the ASPAT devices and can be used and modified as part of this work to explore new concepts and ideas to improve the ASPATs performance. These models will form the basis of the work in Chapters 7 & 8.

The ASPAT devices RF performance was characterised using an equivalent circuit model. 2-step de-embedding processes were used to determine the parasitic inductance and capacitance of the devices. The devices series and junction resistances as well as the devices junction capacitance were found from fitting the equivalent circuits S_{11} parameters to the measured S_{11} parameters of the two diodes. The devices displayed a higher zero and forward bias junction capacitance than the fully depleted capacitances. This is caused by the charge in the device's accumulation region being mirrored by the positive charge in the collector layer. Methods of reducing this capacitance were discussed. This behaviour was also apparent in the series resistance which was caused by the undoped spacer region not being fully depleted. The $In_{0.53}Ga_{0.47}As$ ASPAT showed a reduced series resistance when compared to the GaAs ASPAT. This can be attributed to the increased mobility of $In_{0.53}Ga_{0.47}As$ and the increased level of doping in the ohmic contact layers.

The cut-off frequencies of the devices were calculated with the highest frequencies being reported for the $4\times4\mu m^2$ devices. The GaAs ASPATs showed a zero bias cut-off frequency of 301GHz and the $In_{0.53}Ga_{0.47}As$ devices showed a cut-off frequency of 491GHz. The higher cut-off frequency is attributed mainly to the reduced series resistance of the $In_{0.53}Ga_{0.47}As$ devices due to its higher mobility and doping.

CHAPTER 6

METAMORPHIC ASPAT DIODES

6.1. Introduction

In the previous section, the growth, fabrication and characteristics of ASPAT devices grown on both GaAs and InP substrates were discussed. One of the points not discussed is the additional cost and difficulty in the use of the InP substrates when compared with GaAs. As such in this section the growth of $In_{0.53}Ga_{0.47}As$/AlAs ASPATs on GaAs substrates through the use of metamorphic layers will be investigated.

The effect of the growth temperature of the metamorphic layers on the devices DC and RF characteristics will be investigated and discussed. The overall performance of the new metamorphic ASPAT (mASPAT) devices will be compared to conventionally grown $In_{0.53}Ga_{0.47}As$/AlAs ASPATs on InP substrates with the same active device structure. The physical models developed in Chapter 5 will also be used as part of the analysis of the new mASPAT structures.

6.2. Diode Structures

As for the standard ASPAT devices grown as described in Chapter 5, the mASPAT structures were grown in house using a Riber V100H solid source molecular beam epitaxy system. The wafers were processed using i-line optical photolithography techniques to create devices of mesa areas 6×6 μm², 5×5 μm², 4×4 μm², 3×3 μm², 2×2 μm² and 1.5×1.5 μm². The contacts of the mASPAT diodes were formed using thermal evaporation of 50nm Ti and 900nm Au. The devices DC characteristics were measured using an HP4142 semiconductor parameter analyser and the devices S_{11} parameters were measured using an Anritsu 37369AVector Network Analyzer. All these measurements were performed at room temperature.

Prior to the growth of the metamorphic layers, a GaAs/AlAs superlattice was grown followed by an AlAs spacer layer of 50nm thickness. Then 560nm graded metamorphic layer of $In_xAl_{(1-x)}As$ was grown starting with an Indium composition of x=0.06 and linearly increasing up to a composition of x=0.52 at which point the lattice constant of $In_{0.52}Al_{0.48}As$ is 5.87Å and lattice matched to InP. This was done for two wafers, one with a growth temperature for the metamorphic layer of 440ºC denoted as XMBE#463 and one at 500ºC denoted as XMBE#464. After this, the devices active layers were grown with n-type ohmic contacts with doping of 1.5×10^{19} cm^{-3} and 35nm n-type emitter and collector layers with doping of 1×10^{17} cm^{-3}. This is identical to the structure of the standard $In_{0.53}Ga_{0.47}As$ ASPATs grown on InP substrates in Chapter 5. The epitaxial layer profile of the mASPATs can be seen below in Table 6.2.1.

Table 6.2.1 Epitaxial layers of mASPAT diodes

	mASPAT
	$In_{0.53}Ga_{0.47}As$ 1.5×10^{19} cm^{-3}
	$In_{0.53}Ga_{0.47}As$ 1×10^{17} cm^{-3}
5nm	$In_{0.53}Ga_{0.47}As$ (spacer 1)
2.8nm	AlAs (barrier)
200nm	$In_{0.53}Ga_{0.47}As$ (spacer 2)
	$In_{0.53}Ga_{0.47}As$ 1×10^{17} cm^{-3}
	$In_{0.53}Ga_{0.47}As$ 1.5×10^{19} cm^{-3}
x=0.06-0.52	$In_xAl_{(1-x)}As$ (metamorphic layer)
	AlAs Spacer layer

6.3. mASPAT DC Characteristics

The DC characteristics of the devices were measured from -2V to 2V in steps of 0.01V for both XMBE#463 and for XMBE#464. From this measured data, the devices junction resistances, R_j, and curvature coefficients, k_v, were calculated using equations 2.5.11 & 2.5.12 as described in Chapter 2. The devices current densities were determined by dividing the current by the area of the device. The device areas were calculated to include the reduction in device area due to the undercut and the effect of partial areas under the airbridge. Figure 6.3.1 & Figure 6.3.2 show the current density-voltage characteristics of XMBE#463 and XMBE#464 grown at 440ºC and 500ºC respectively. As can be seen in the figures the devices scale excellently with area. With XMBE#463 showing more consistent area scaling, implying a lower amount of device to device variation. It should be noted that device curves stopped when the VNAs maximum allowable current was reached.

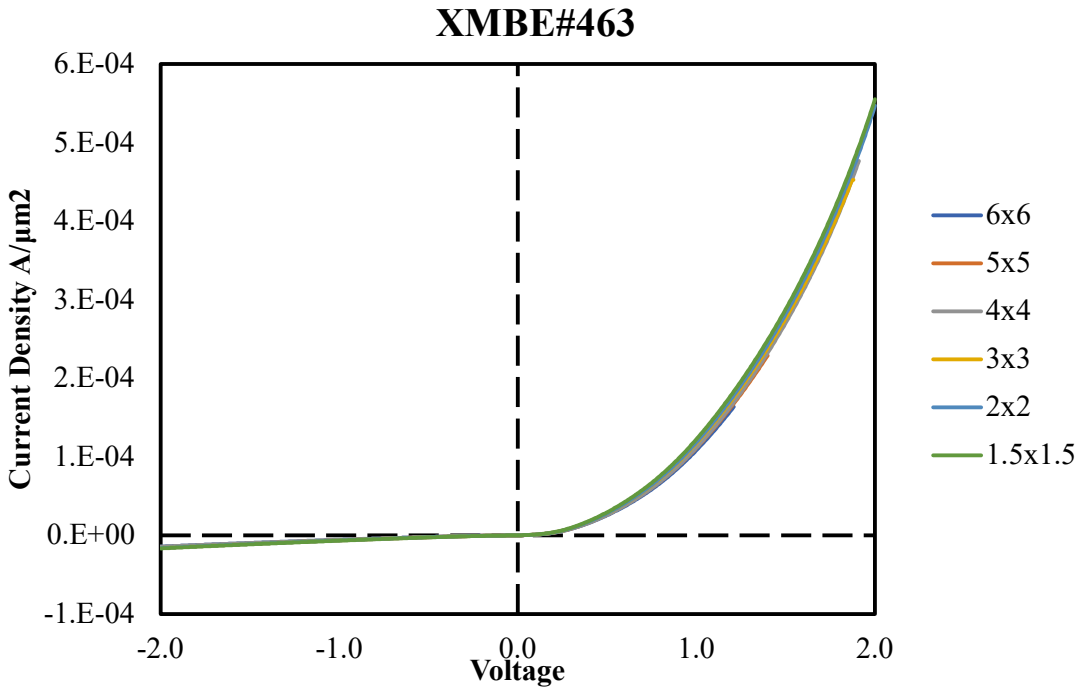

Figure 6.3.1 Current density plotted against voltage for XMBE#463 mASPAT diode

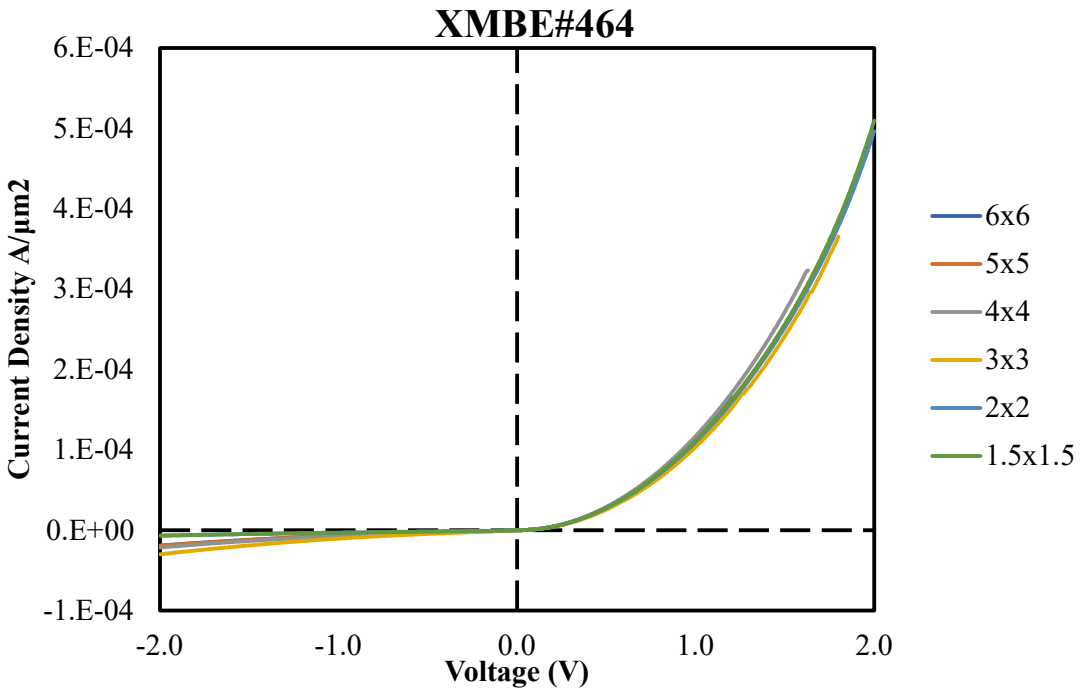

Figure 6.3.2 Current density plotted against voltage for XMBE#464 mASPAT diode

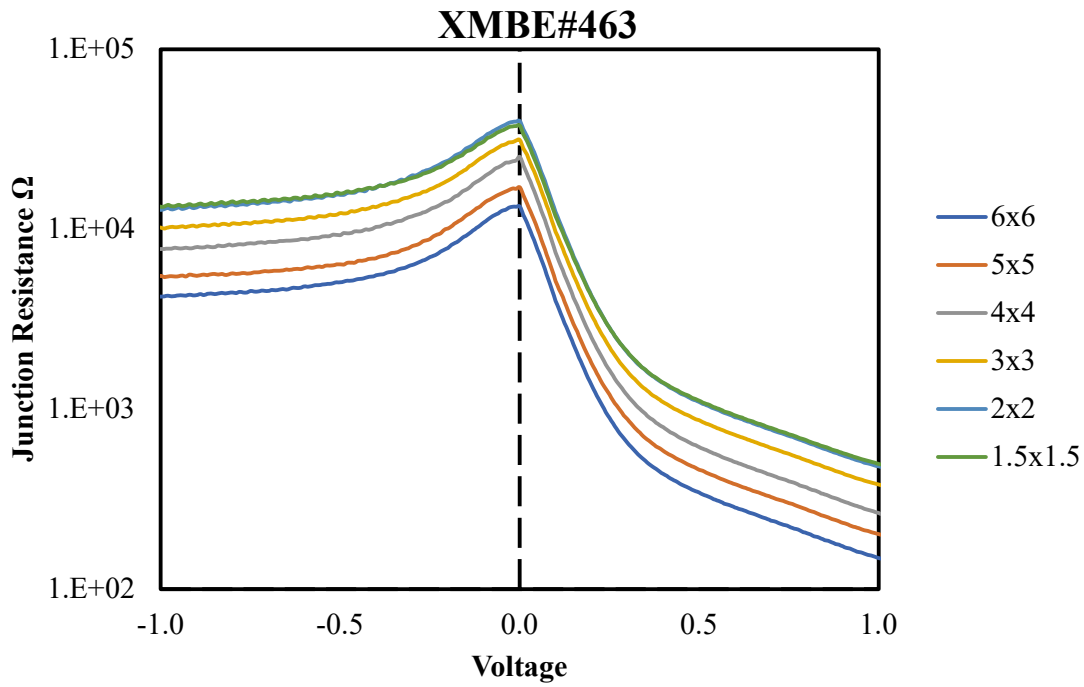

Figure 6.3.3 Junction resistance plotted logarithmically against voltage for mASPAT XMBE#463

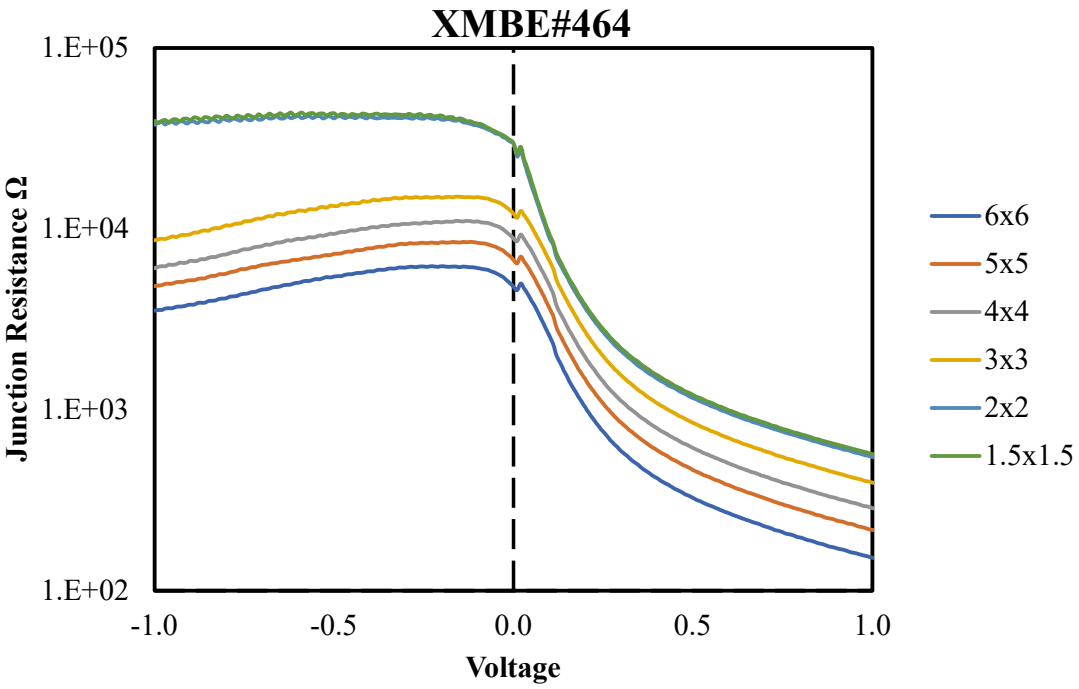

Figure 6.3.4 Junction resistance plotted logarithmically against voltage for mASPAT XMBE#464

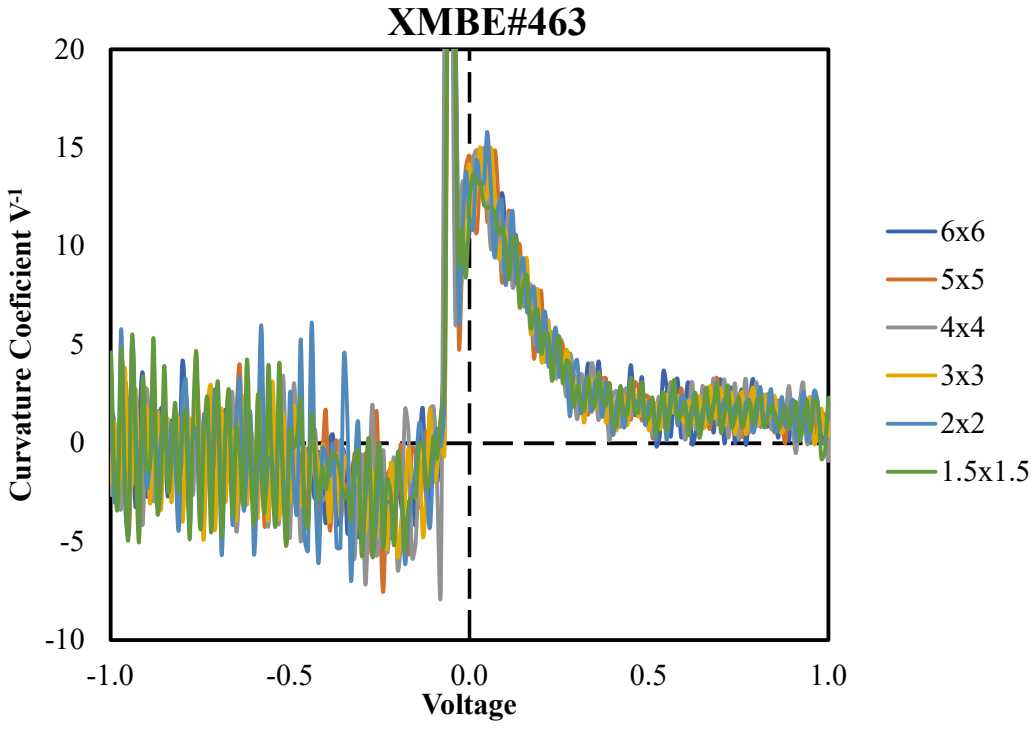

Figure 6.3.5 Calculated curvature coefficient of XMBE#463 mASPAT.

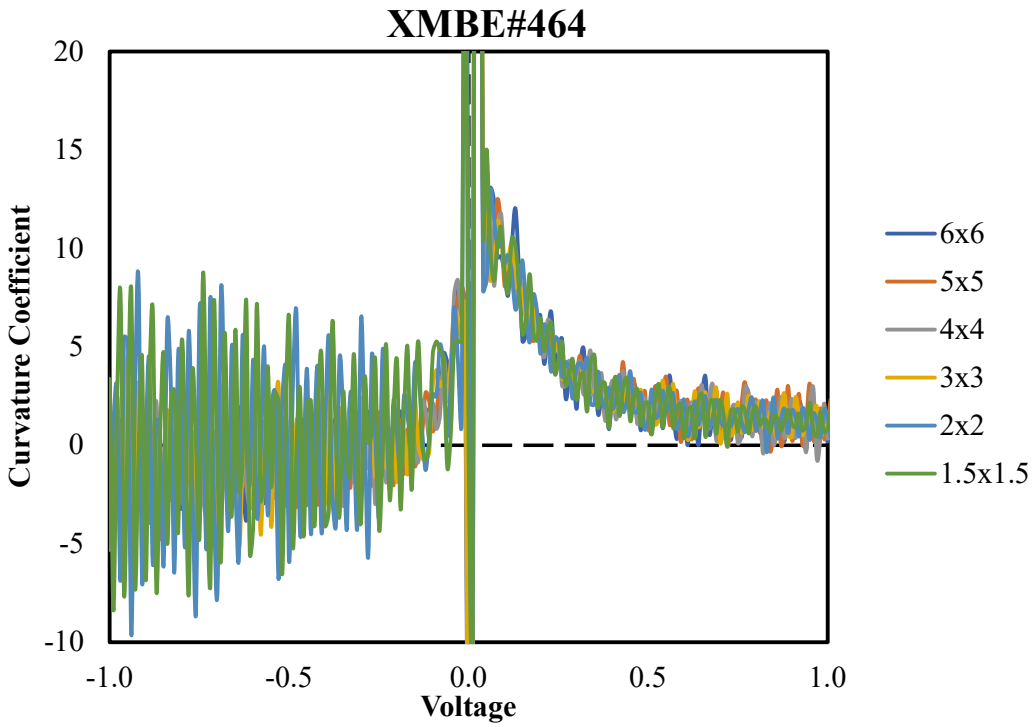

Figure 6.3.6 Calculated curvature coefficient of XMBE#464 mASPAT.

Figure 6.3.3 & Figure 6.3.4 show the calculated junction resistances of XMBE#463 and XMBE#464 respectively. The zero bias R_j are shown for both wafers at all device sizes in Table 6.3.1. As can be seen from the table, XMBE#464 shows a consistently lower zero bias junction resistance which corresponds to the lack of peak seen in Figure 6.3.4. This could be due to the higher growth temperature causing an increase in the density of threading dislocations. This would lead to an increase in leakage current and a reduction in junction resistance.

As in Chapter 5, the curvature coefficients of the two wafers have been calculated and left unsmoothed to preserve the accuracy of the approximation of the derivatives. As can be seen in Figure 6.3.5 & Figure 6.3.6 both wafers show a large amount of noise around zero bias and when smoothed this noise is averaged into the calculated k_v reducing the accuracy. XMBE#463 has an approximate curvature coefficient of ~$13V^{-1}$ whilst XMBE#464 has a curvature coefficient of approximately ~$11V^{-1}$. This is comparable to the curvature of the reference ASPAT which had a measured and simulated k_v of ~$11V^{-1}$ and in fact a slight improvement for XMBE#463.

Table 6.3.1 Table of mASPAT junction resistances at 0V

	Zero bias junction resistance kΩ					
Wafer	*6 × 6 μm²*	*, 5 × 5 μm²*	*4 × 4 μm²*	*3 × 3 μm²*	*2 × 2 μm²*	*1.5 × 1.5 μm²*
#463	13	17	25	31	40	37
#464	4	7	9	12	29	29

The current of 4×4 μm² XMBE#463 & XMBE#464 mASPT devices are plotted logarithmically against voltage in Figure 6.3.7, along with measured data from the standard $In_{0.53}Ga_{0.47}As$/AlAs ASPAT grown on InP presented in Chapter 5. As can be seen from the data, the mASPATs both show a much higher current when compared with the reference ASPAT and correspondingly a lower junction resistance. The zero bias R_j of the reference ASPAT is 128kΩ for a 4×4 μm^2 device which is over 980% of the value for XMBE#463

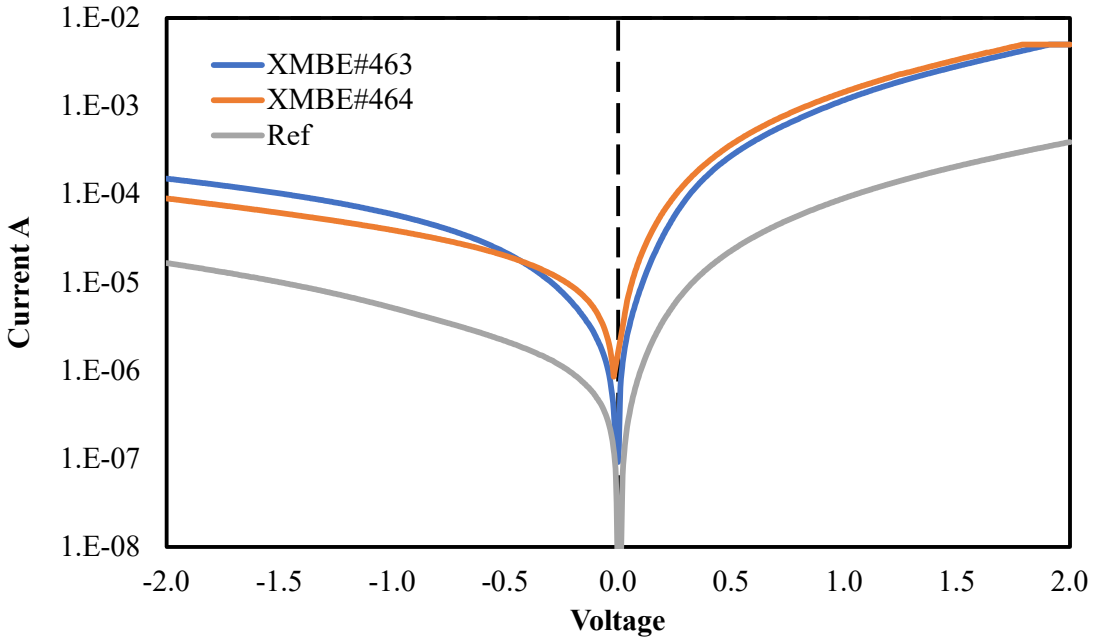

Figure 6.3.7 Logarithmic plot of XMBE#463, XMBE#464 and reference ASPAT current voltage curves for 4 × 4 μm^2 devices.

To explore this behaviour, the ATLAS model used in Chapter 5 for the reference ASPAT was modified. As current is exponentially proportional to the barrier thickness the barrier thickness of the model was reduced. It was found that by reducing the barrier thickness from 2.8nm to 2.3nm, which would correspond to a 2-monolayer reduction in the barrier thickness, the current of the model matched that of the mASPAT. This is shown in Figure 6.3.8.

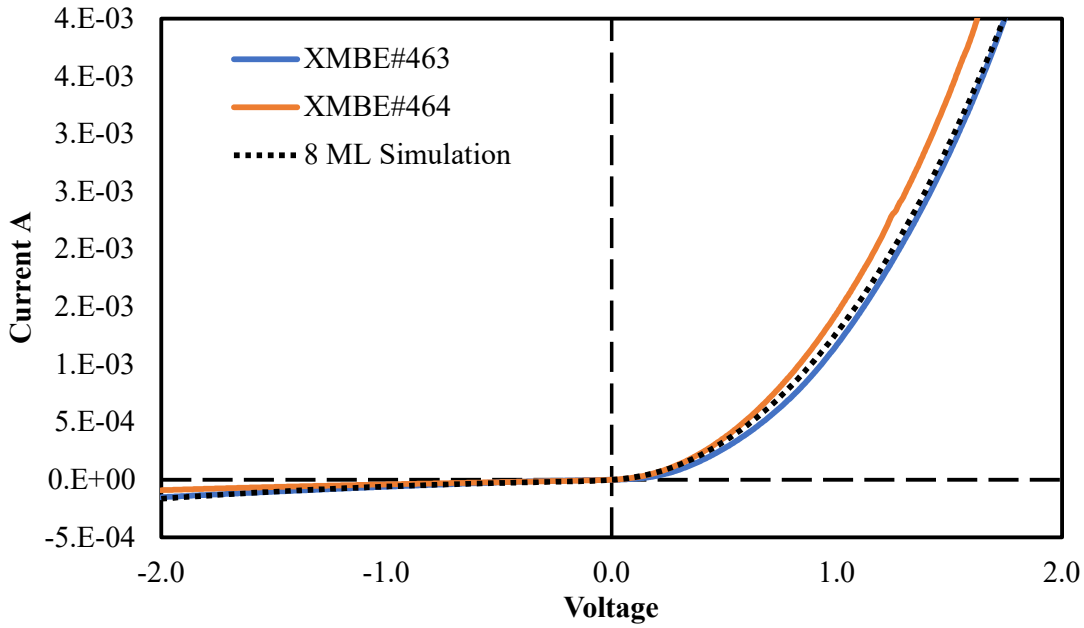

Figure 6.3.8 DC characteristics of XMBE#463, XMBE#464 and simulated ASPAT with 8ML barrier

Whilst, this could explain the reduction in mASPAT junction resistance, previous work has shown excellent control of barrier thickness during ASPAT growth [101], [144]. As such other explanations must be explored. These may include the existence of a higher number of threading dislocations in a metamorphically grown device. This could also be an explanation for the difference in R_j at zero bias between the two mASPAT wafers. As XMBE#464 was grown at a higher temperature this could have introduce more threading dislocations into the metamorphic buffer layer which propagated into the active device region [146]. This would allow for a larger leakage current and the corresponding reduction in R_j.

6.4. mASPAT RF Characteristics

The RF characteristics of the mASPAT devices were explored in the same manner as for the standard ASPATs in Chapter 5. The devices S_{11} parameters were measured from 40MHz–40GHz at bias voltages from -1V to 1V in steps of 0.01V. The RF characteristics of the devices were extracted using the equivalent circuit model described in Chapter 4 and is shown in Figure 6.4.1.

The two step de-embedding procedure described in Chapter 3 was used and the parasitic capacitance and voltage were extracted from the open and short structures. The mASPAT device exhibited a parasitic capacitance C_p of 6fF and a parasitic inductance L_p of 40pH. Once again, the junction resistance was assumed to be the same as was derived from the devices DC characteristics and the remaining intrinsic parameters were found by fitting the simulated S_{11} parameter of the equivalent circuit to the measured S_{11} parameter of the device. The measured and simulated S_{11} parameters are shown in Figure 6.4.2 & Figure 6.4.3 and show an excellent fit for both wafers.

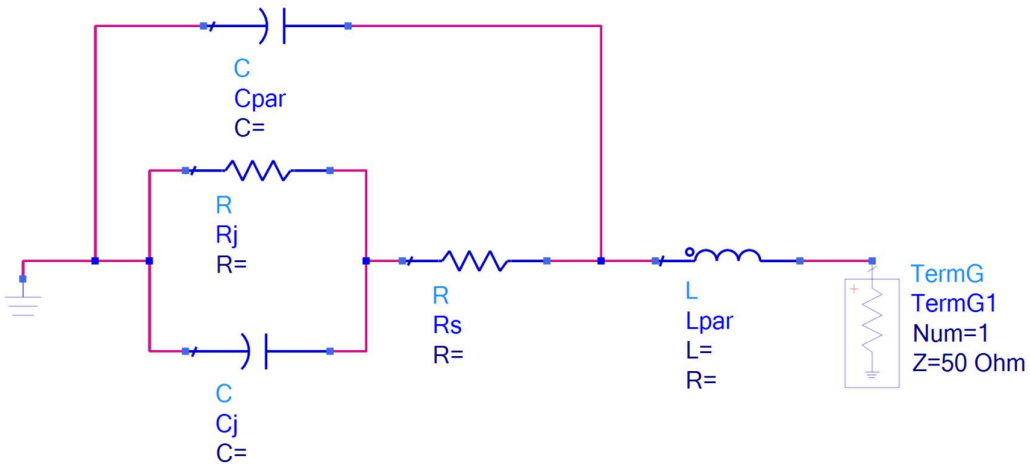

Figure 6.4.1 Equivalent circuit model of mASPAT device with parasitic inductance and capacitance L_{par} and C_{par}, series resistance R_s and junction capacitance and resistance R_j and C_j.

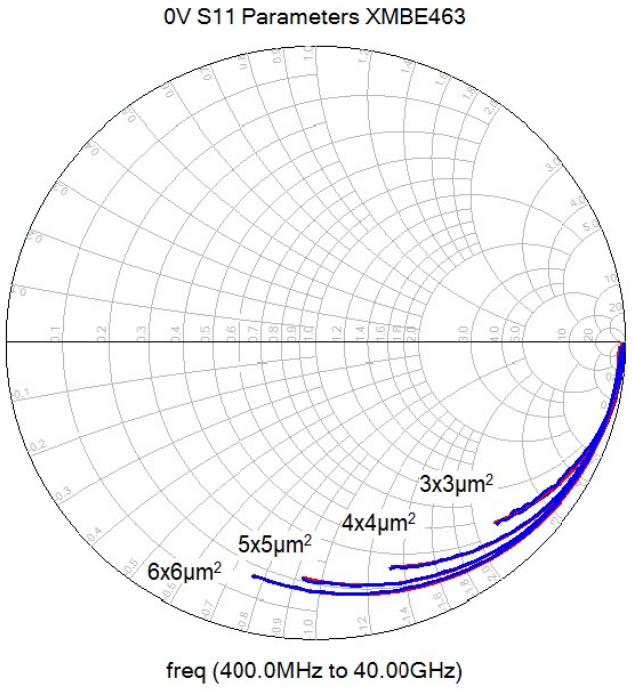

Figure 6.4.2 Measured and simulated S_{11} parameter data for XMBE 463 mASPAT devices

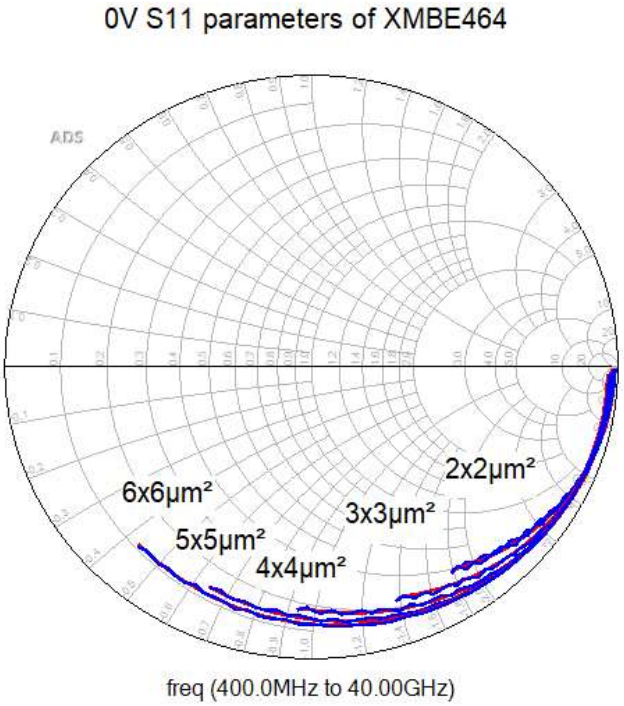

Figure 6.4.3 Measured and simulated S_{11} parameter data for XMBE 464 mASPAT devices.

Table 6.4.1 shows the zero bias R_s, C_j and cut-off frequencies of the devices for the XMBE#463 and XMBE#464 wafers. The zero bias capacitances of the devices are plotted against mesa area in Figure 6.4.4. From the figure it can be seen that capacitance scales well with device area as would be expected. XMBE#463 shows a clear advantage over XMBE#464 in terms of C_j.

However, this does not lead to an increase in the cut-off frequency due to the higher series resistance of XMBE#463. Table 6.4.1 also shows the RF characteristics of the reference $In_{0.53}Ga_{0.47}As$ ASPAT from Chapter 5. Both mASPAT wafers show a substantial increase in the junction capacitance when compared with the reference ASPAT. This has substantially reduced the cut-off frequency of the mASPATs from 491GHz for the 4×4 μm^2 reference ASPAT to 178GHz and 249GHz for XMBE#463 and XMBE#464 respectively. Explanations of this increase in capacitance are necessary if the mASPAT devices are to compete with the conventional ASPAT devices. As it currently stands, a conventional GaAs ASPAT has much better characteristics than the mASPAT devices in terms of cut-off frequency and junction capacitance.

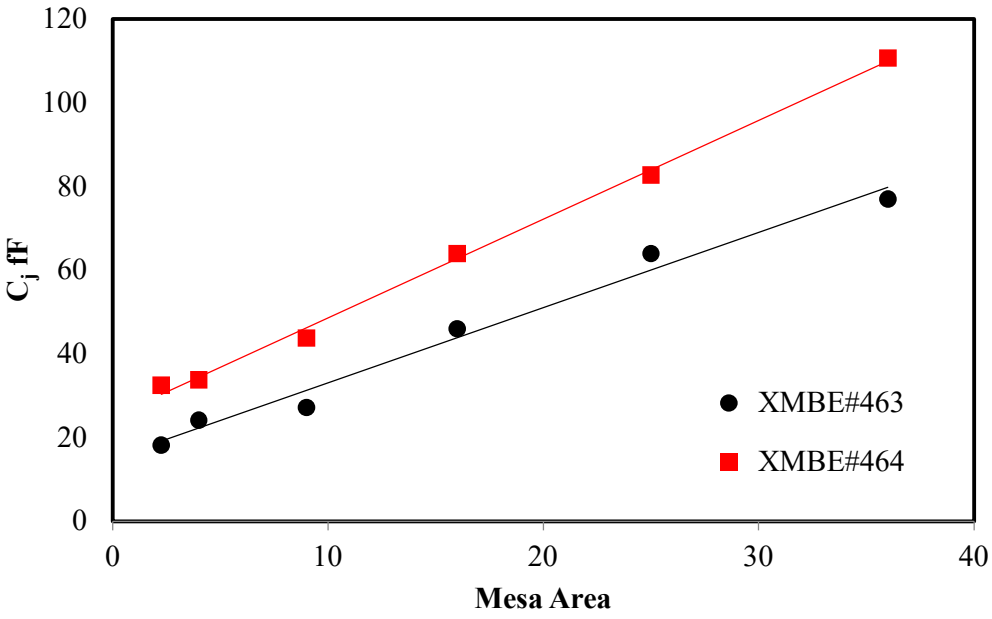

Figure 6.4.4 mASPAT zero bias capacitance plotted against device mesa area for XMBE#463 and XMBE#464 devices.

Table 6.4.1 Table of RF characteristics of mASPAT device and reference ASPAT at zero-bias

Wafer	Area μm^2	R_j kΩ	R_s Ω	C_j fF	C_p fF	L_p pH	f_c GHz
XMBE#463	36	13	9	76	6	40	229
XMBE#464	36	4	6	111	6	40	250
Reference	36	54	13	50	10	40	245
XMBE#463	25	17	12	65	6	40	205
XMBE#464	25	7	7	83	6	40	265
XMBE#463	16	25	19	46	6	40	178
XMBE#464	16	9	10	64	6	40	249
Reference	16	128	18	18	10	40	491
XMBE#463	9	31	39	27	6	40	151
XMBE#464	9	12	16	44	6	40	229
XMBE#463	4	40	42	24	6	40	158
XMBE#464	4	29	26	34	6	40	183
XMBE#463	2.25	37	31	18	6	40	286
XMBE#464	2.25	29	27	33	6	40	183

One potential explanation for the increase in capacitance is an increase in the threading dislocations in the active device caused by the metamorphic growth process. This would also account for the reduction in the junction resistance as described in Section 6.3 and would appear to indicate that XMBE#464s higher growth temperature of

500ºC compared with XMBE#463s growth temperature of 440ºC has caused an increase in the threading dislocation density. One potential method of improving device performance would be to increase the thickness of the metamorphic buffer layer to allow for the lattice to undergo less strain. Similarly, different grading profiles, such as S-grading and exponential grading, could be used for the metamorphic layer instead of the linear grading used for these mASPAT devices. This could allow for devices to be grown with better characteristics and could be investigated as part of future work.

6.5. Conclusion

In this chapter two $In_{0.53}Ga_{0.47}As$ ASPAT wafers were grown on GaAs substrates using a metamorphic graded buffer layer. These devices were then processed and compared to a reference $In_{0.53}Ga_{0.47}As$ ASPAT grown on a conventional InP substrate. The two mASPAT wafers were grown at 440ºC and 500ºC and the effects of the growth temperature on the device characteristics was discussed.

The mASPATs DC characteristics were measured, and the devices junction resistances and curvature coefficients calculated. Both mASPAT wafers showed good scaling with device area however XBE#463, grown at 440ºC showed less variation between devices than XMBE#464 which was grown at 500ºC. XMBE#463 also showed a higher junction resistance and curvature coefficient at zero-bias than XMBE#464. One possible explanation of this is that the higher temperature metamorphic layer growth induced more threading dislocations. Both mASPATs showed similar curvature coefficients to the reference ASPAT.

Both mASPAT devices showed much reduced junction resistances when compared with the reference ASPAT device. The effect of variation in the AlAs barrier thickness was explored using the Silvaco ATLAS ASPAT physical model from Chapter 5. It was determined that a 2ML change in the AlAs barrier would account for the reduction in the junction resistance. However, this is in contradiction to previous work by this group, which has shown that excellent control of the AlAs barrier thickness is possible. Threading dislocations from the metamorphic growth were also discussed as a potential cause.

The RF characteristics of the mASPATs were extracted from measured S_{11} parameter data using the Advance Design Systems equivalent model method described in

Chapter 4. This extraction showed that the mASPATs both displayed much higher junction capacitances than the reference ASPATs and as such had much lower cut-off frequencies. The causes of this increase in the junction capacitance were discussed as well as improvements that could be made to the growth process to improve the mASPAT devices. It was suggested that increasing the thickness of the metamorphic layer may be beneficial and that other grading profiles may be explored as part of future work.

CHAPTER 7

QUANTUM WELL ASPAT DIODES

7.1. Introduction

In Chapters 5 & 6 the DC parameters of GaAs and $In_{0.53}Ga_{0.47}As$ diodes were investigated including the devices curvature coefficients and junction resistances. The ASPAT curvature coefficients were in the range of 11-13V^{-1}. This is quite poor when compared with Schottky diodes which are inherently limited to a value of 40V^{-1} and other state of the art detector diodes such as Sb based tunnel diodes (k_v=47V^{-1})[75], [81], [82], [84], [85] and Ge based diodes (k_v=70V^{-1})[147]. In this chapter two new diode structures with quantum wells added to the short spacer side of the device were explored as a method of increasing the devices curvature coefficient. One of the new structures is based on the GaAs ASPAT and one on the $In_{0.53}Ga_{0.47}As$ ASPAT. These studies were done using the physical models developed in Chapter 5 for the standard ASPAT diodes.

The new structures DC characteristics were simulated, and their curvature coefficients and junction resistances extracted. Once these have been compared with the standard reference ASPATs the effects of varying the AlAs barrier thickness and quantum well thickness on the devices DC characteristics were explored. These simulations were then used to optimise the devices in terms of both k_v and R_j.

The effect of adding quantum wells to the devices on the junction capacitance was also explored. This was done using AC simulations of the structures in SILVACO. Cut-off frequencies for the new structures were estimated and compared with the standard ASPAT devices.

7.2. QW-ASPAT Structures

The purpose of adding quantum wells to the ASPAT diode are to increase the height of the AlAs barrier in reverse bias and therefore reduce the leakage current. This will cause a larger change in current flow at zero bias and subsequently increase the devices

curvature coefficient. The epitaxial layer structure of the two new devices is given in Table 7.2.1. The devices ohmic contact layers are the same as the reference ASPAT structures with the GaAs device having a doping of 4×10^{18} cm^{-3} and the $In_{0.53}Ga_{0.47}As$ devices having a doping of 1.5×10^{19} cm^{-3}. The devices also have emitter and collector layers doped to 1×10^{17} cm^{-3} as is the case for the reference ASPAT devices. Both devices contain undoped spacer layers of 200nm and 5nm to maintain the 40:1 spacer ratio.

The devices quantum wells are created by using a layer of $In_{1-x}Ga_xAs$ with a higher indium composition than the standard spacers. For the GaAs QW-ASPAT a quantum well composition of $In_{0.18}Ga_{0.82}As$ was used and for the $In_{0.53}Ga_{0.47}As$ device a composition of $In_{0.8}Ga_{0.2}As$ was used. These compositions were selected as they have been grown successfully previously for resonant tunnelling diodes and for ASPATs with two quantum wells added [148].

Table 7.2.1 Epitaxial layers of QW-ASPAT diodes

	GaAs ASPAT	*$In_{0.53}Ga_{0.47}As$ ASPAT*
	GaAs 4×10^{18} cm^{-3}	$In_{0.53}Ga_{0.47}As$ 1.5×10^{19} cm^{-3}
	GaAs 1×10^{17} cm^{-3}	$In_{0.53}Ga_{0.47}As$ 1×10^{17} cm^{-3}
5 nm	GaAs (spacer 1)	$In_{0.53}Ga_{0.47}As$ (spacer 1)
X nm	$In_{0.18}Ga_{0.82}As$ (well)	$In_{0.8}Ga_{0.2}As$ (well)
Y nm	AlAs (barrier)	AlAs (barrier)
200nm	GaAs (spacer 2)	$In_{0.53}Ga_{0.47}As$ (spacer 2)
	GaAs 1×10^{17} cm^{-3}	$In_{0.53}Ga_{0.47}As$ 1×10^{17} cm^{-3}
	GaAs 4×10^{18} cm^{-3}	$In_{0.53}Ga_{0.47}As$ 1.5×10^{19} cm^{-3}

Figure 7.2.1 shows the conduction band profiles for the QW-ASPAT devices with 6nm quantum wells. As can be seen from the figure, the forward bias AlAs barriers maintain their height, however in reverse bias the barriers are now 0.15eV and 0.23eV higher for the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs and $In_{0.8}Ga_{0.2}As$/AlAs/$In_{0.53}Ga_{0.47}As$ QW-ASPAT devices respectively.

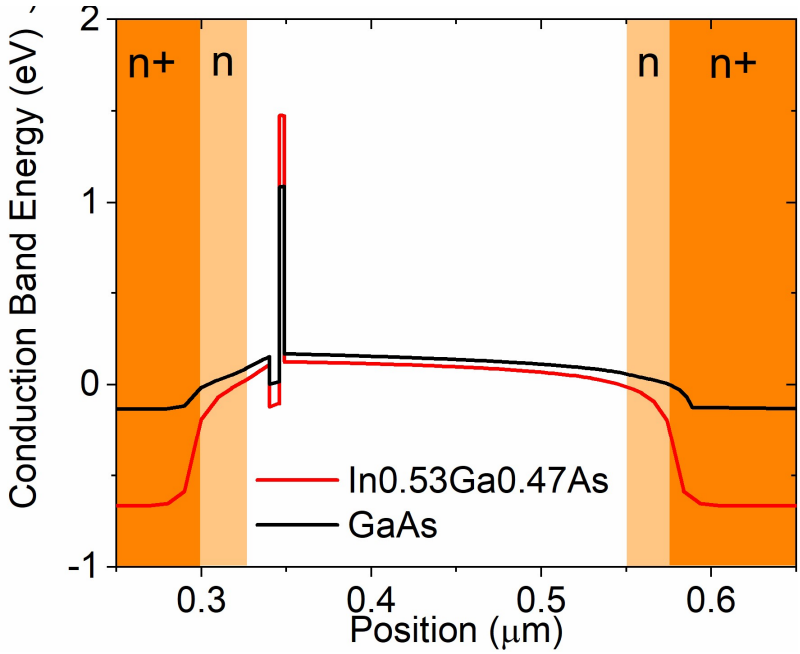

Figure 7.2.1 Conduction band profiles of $In_{0.18}Ga_{0.82}As$/AlAs/GaAs and $In_{0.8}Ga_{0.2}As$/AlAs/$In_{0.53}Ga_{0.47}As$ QW-ASPAT devices with 6nm quantum wells.

7.3. Physical Modelling

The new structures were modelled by modifying the models previously used in Chapter 5 for the standard ASPAT diodes. The DC characteristics of the device were simulated using the *semiconductor-insulator-semiconductor* model. This model solves the Schrodinger equation using a transfer matrix method to give the transmission probability as a function of energy, *T(E)*. From this, the current density is then found via equation 7.3.1, where, *m** is the material effective mass, *k* is Boltzmann's constant and *h* is the Planck constant. E_{Fr} and E_{Fl} represent the quasi fermi levels of the spacers located at the right and left side of the barrier.

$$J = \frac{qm^* kT}{2\pi^2 h^3} \int_0^\infty T(E) \ln\left\{\frac{1 + e^{\left(\frac{E_{Fr} - E}{kT}\right)}}{1 + e^{\left(\frac{E_{Fl} - E}{kT}\right)}}\right\} dE$$

7.3.1

The simulation parameters of all materials used to simulate the QW-ASPAT devices is shown in Table 7.3.1 An affinity of 3.15eV for AlAs was chosen to conform with the well-known 65:35 conduction band offset split for GaAs-AlAs interfaces. [91]. It should be noted that the bandgap of AlAs in these simulations was taken to be the direct Γ- Γ bandgap of 2.8eV through which the tunnelling mechanism occurs, as described in [86]. The affinity, χ, of the $In_{(1-x)}Ga_xAs$ layers was determined using equation 7.3.2. [142]

$$\chi = (4.9 - 0.82x)eV$$

7.3.2

The band gap, E_g of the $In_xGa_{(1-x)}As$ layers was determined using equation 7.3.3. [142]

$$E_g = (0.36 + 0.63x + 0.43x^2)eV$$

7.3.3

Conduction band offsets are then calculated in SILVACO using Andersons rule to produce full conduction band profiles for the simulations as can be seen in Figure 7.2.1.

Table 7.3.1 QW-ASPAT material parameters for ATLAS modelling

Material	*Affinity (eV)*	*Bandgap (eV)*
$In_{0.47}Ga_{0.53}As$	4.5	0.74
GaAs	4.07	1.4
AlAs	3.15	2.8
$In_{0.18}Ga_{0.82}As$	4.22	1.16
$In_{0.8}Ga_{0.2}As$	4.73	0.5

7.4. QW-ASPAT DC Characteristics

DC simulations of the new structures were then performed starting with devices with 6nm quantum wells and 2.8nm AlAs barriers to match the barrier thickness of the standard ASPAT diode. The bias voltage was simulated from -1V to 1V in steps of 0.01V. The devices used in the simulation were all $4\times4\mu m^2$ and were compared with equivalently sized ASPAT devices. The results of these simulations can be seen in Figure 7.4.1 & Figure 7.4.2. As can be seen, the addition of quantum wells has reduced the reverse bias leakage current dramatically. The $In_{0.18}Ga_{0.82}As$/AlAs/GaAs device now has a leakage current of 360nA and the $In_{0.8}Ga_{0.2}As$/AlAs/$In_{0.53}Ga_{0.47}As$ device has an even smaller leakage current of 205nA at -1V. These values are an order of magnitude lower than the equivalent -1V leakage currents for the standard GaAs and $In_{0.53}Ga_{0.47}As$ ASPATs which are 5.1µA and 4.3µA respectively for same sized devices.

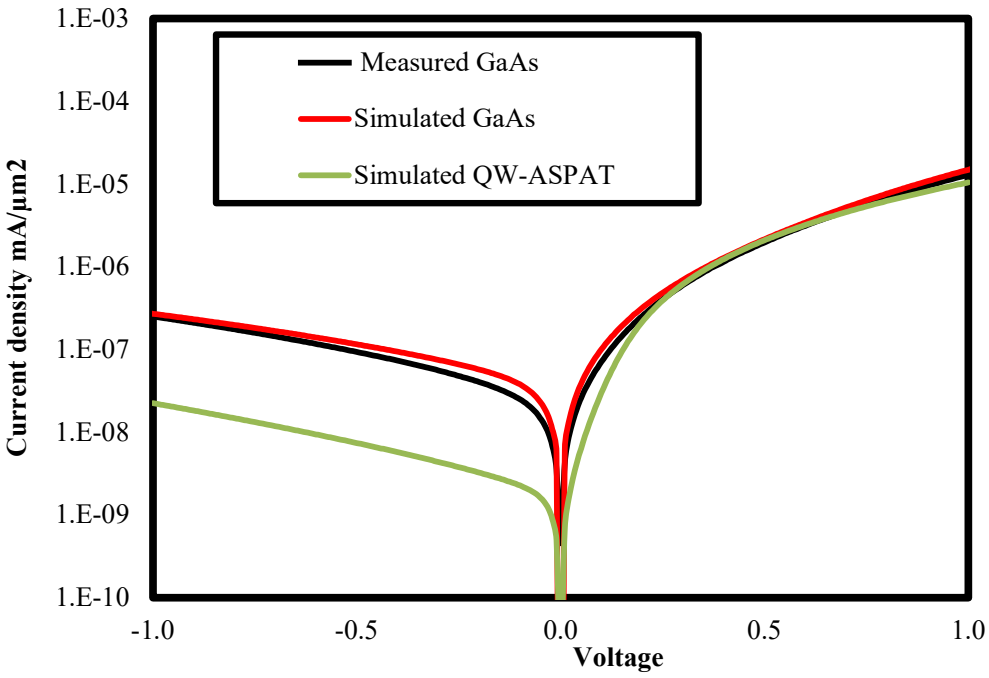

Figure 7.4.1 Measured and simulated I-V characteristics of standard GaAs ASPAT and simulated I-V characteristic of new structure with 6nm $In_{0.18}Ga_{0.82}As$ quantum wells

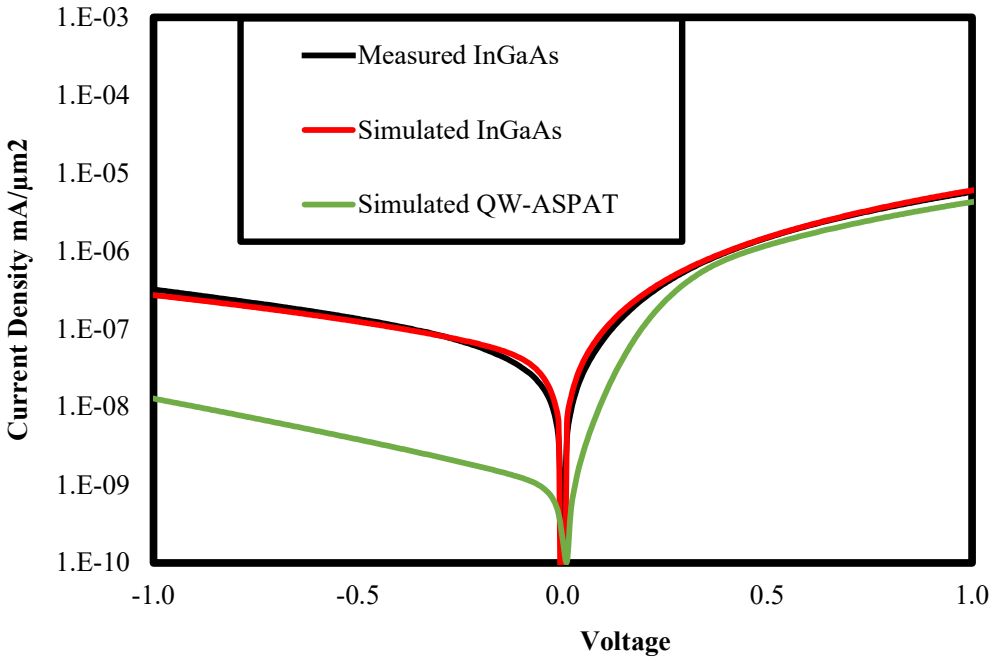

Figure 7.4.2 Measured and simulated I-V characteristics of standard $In_{0.53}Ga_{0.47}As$ ASPAT and simulated I-V characteristic of new structure with 6nm $In_{0.8}Ga_{0.2}As$ quantum wells

The curvature coefficients extracted from the simulated DC characteristics of the new structures are shown in Figure 7.4.3 & Figure 7.4.4. As can be seen, the new structures show a marked improvement in the curvature coefficient with the new structures both displaying a value of $32V^{-1}$. This improved on the values achieved for the reference ASPATs in Chapter 5 by a factor of ~2.5. It also puts the new structures much closer to the Schottky diode which is its main competitor.

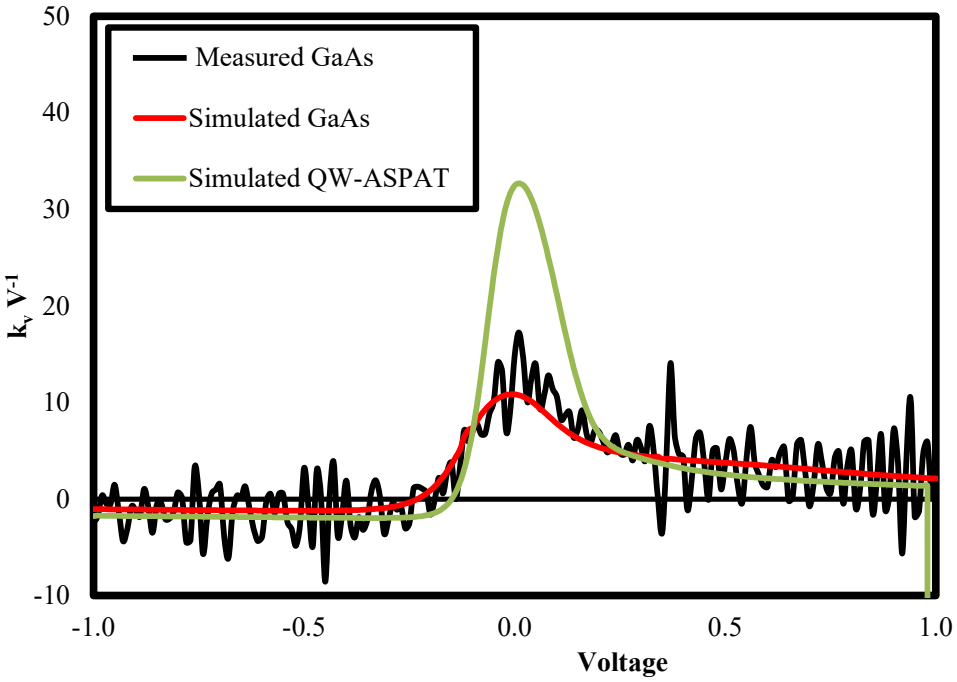

Figure 7.4.3 Curvature coefficient of GaAs QW-ASPAT with 6nm wells and reference GaAs ASPAT

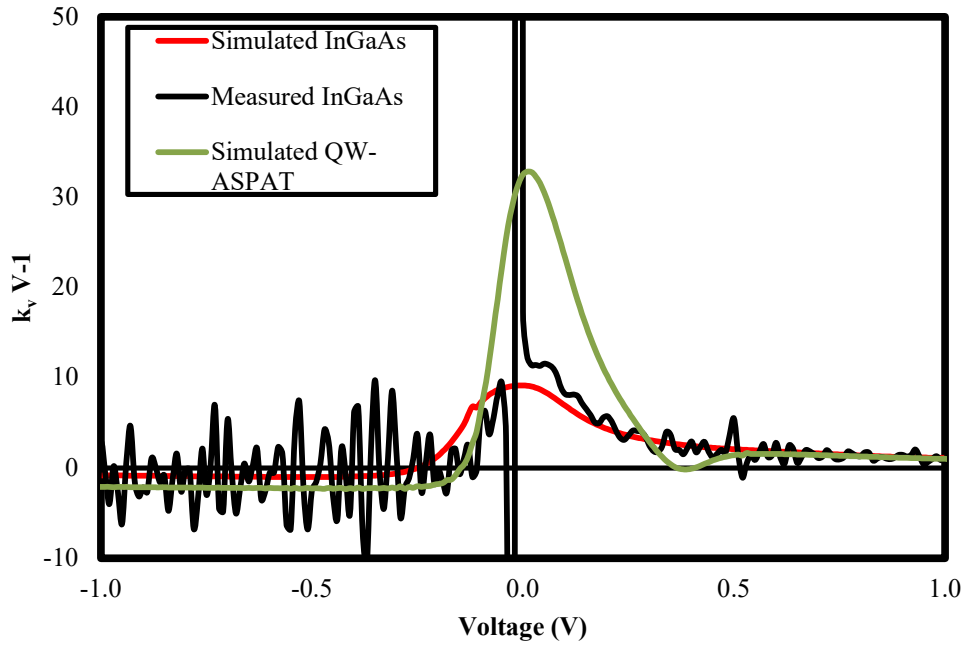

Figure 7.4.4 Curvature coefficient of InGaAs QW-ASPAT with 6nm quantum wells and reference InGaAs ASPAT

The junction resistances of the new structures are plotted in Figure 7.4.5 & Figure 7.4.6. As is apparent, the new structures have a much higher junction resistance in reverse bias which causes the reduction in the leakage current. This has also led to an order of magnitude increase in the zero bias junction resistance. This is not desirable as it increases the diode response time, which is dependent on the product of the junction resistance and the junction capacitance. High junction resistance also makes the fabrication of a matching circuit to correspond with the standard 50Ω impedance much more difficult, any matching circuit would be overly large and difficult to manufacture. As such more simulations were performed to optimize the device structure.

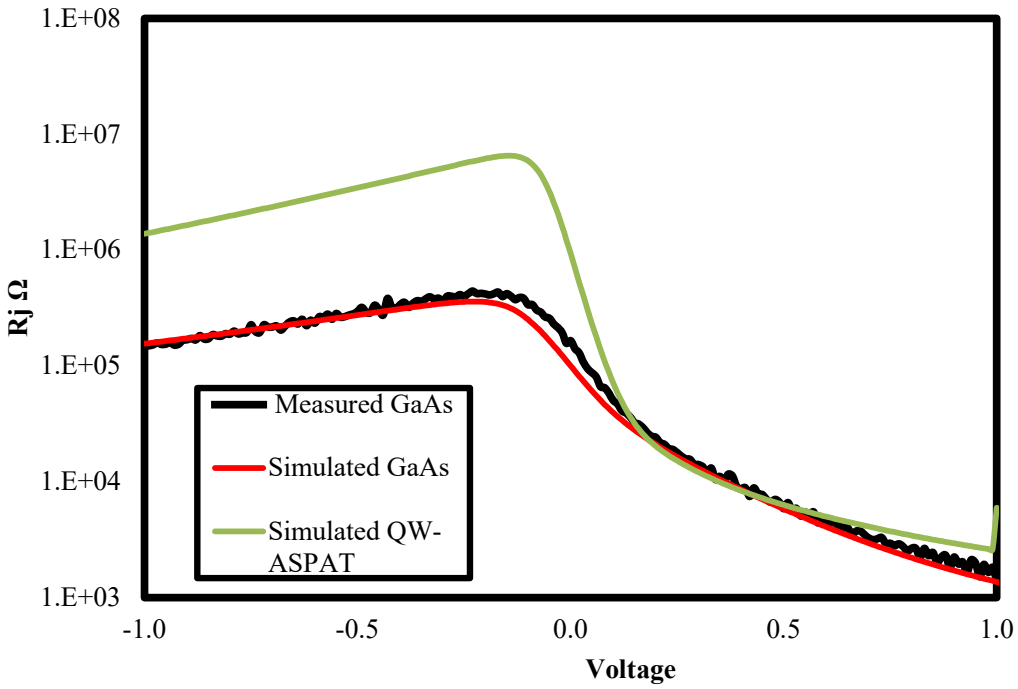

Figure 7.4.5 Junction resistance of GaAs QW-ASPAT with 6nm quantum wells and reference GaAs ASPAT

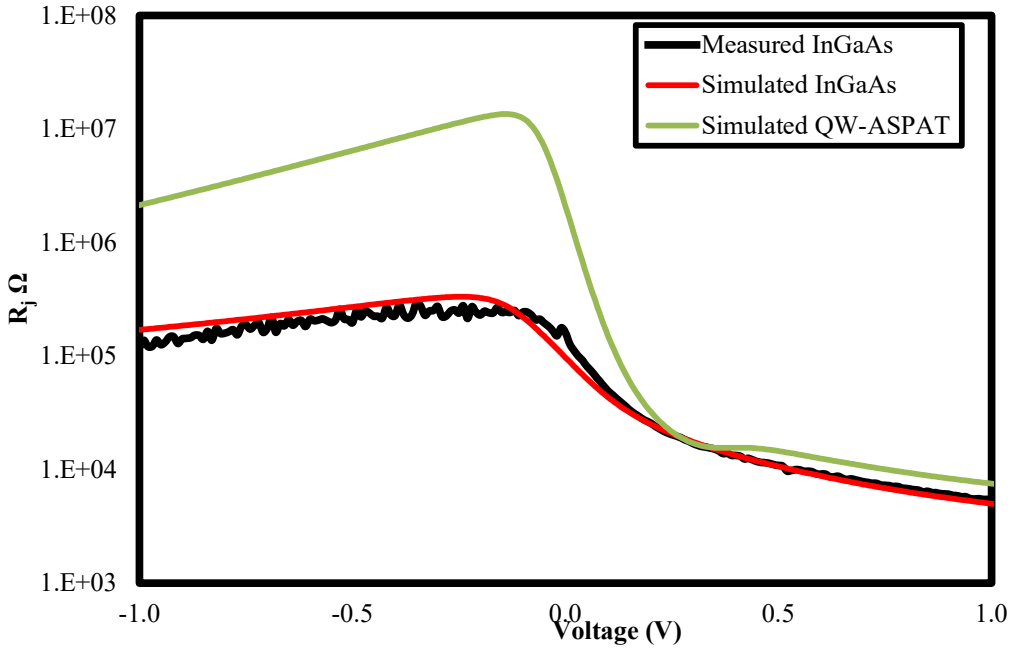

Figure 7.4.6 Junction resistance of InGaAs QW-ASPAT with 6nm quantum wells and reference GaAs ASPAT.

7.5. Device Optimisation

To optimise the device structures and reduce the junction resistance a series of simulations were carried out in which the devices quantum well thickness and AlAs barrier thickness were varied. The quantum well thickness was varied from 2nm to 8nm in steps of 1nm and the AlAs barrier thickness was varied from 3nm to 1nm in steps of 0.5nm. The R_j and k_v were extracted at zero bias for each simulation and the results plotted as maps. The k_v maps and R_j for the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs devices and the $In_{0.8}Ga_{0.2}As$/AlAs/$In_{0.53}Ga_{0.47}As$ are shown in Figure 7.5.1.

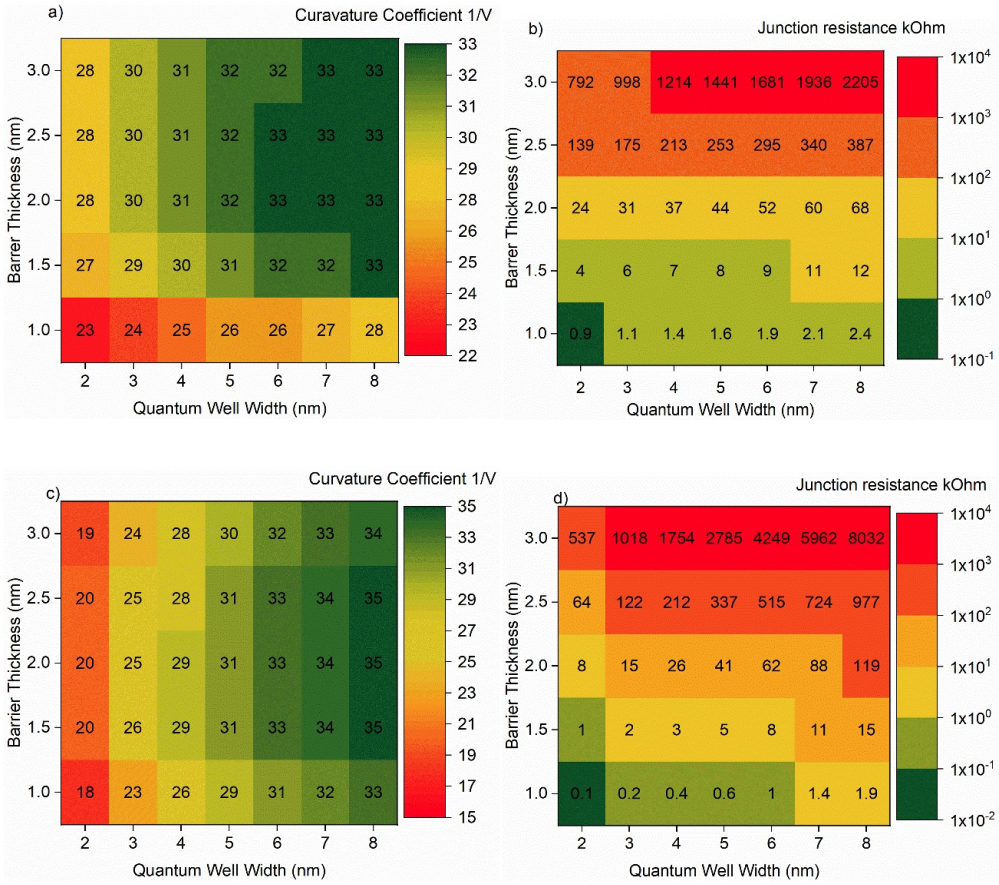

Figure 7.5.1 a) Extracted k_v values for simulations of the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs structures whilst varying quantum well thickness and barrier thickness. b) Extracted Rj values for simulated $In_{0.18}Ga_{0.82}As$/AlAs/GaAs structures whilst varying quantum well and barrier thickness. c) Extracted k_v values for simulated $In_{0.8}Ga_{0.2}As$/AlAs/$In_{0.53}Ga_{0.47}As$ structures whilst varying quantum well thickness and barrier thickness. d) Extracted Rj values for simulations $In_{0.8}Ga_{0.2}As$/AlAs/$In_{0.53}Ga_{0.47}As$ structures whilst varying quantum well and barrier thickness. Desirable properties such as high k_v and low R_j are coloured in green and undesirable properties in red.

It can clearly be seen that reducing the well width leads to a reduction in the junction resistance. However, this also comes with a reduction in k_v. Similarly, the results of these simulations show a strong exponential relationship between barrier thickness and junction resistance. It can be seen that by reducing the barrier thickness from 3nm to 1nm, R_j reduced from 1.7MΩ to 1.9kΩ for the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs devices with 6nm wells and from 4.2MΩ to 1kΩ for the $In_{0.8}Ga_{0.2}As$/AlAs/ $In_{0.53}Ga_{0.47}As$

devices with 6nm wells. These are much more suitable values of R_j for diode detector applications.

The highest k_v was $33V^{-1}$ for the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs structures whilst the highest k_v for the $In_{0.8}Ga_{0.2}As$/AlAs/$In_{0.53}Ga_{0.47}As$ structures was $35V^{-1}$. From Figure 7.5.1 it can be concluded that the most effective method of lowering the junction resistance is to reduce the barrier thickness, as this reduces R_j without significantly reducing k_v. It would be inadvisable to reduce quantum well width to reduce R_j as this would sacrifice k_v for a comparably smaller reduction in R_j.

7.6. QW-ASPAT CV Characteristics

To fully investigate the potential of the new structures as part of a detector circuit it is important to understand how the addition of the quantum wells changes the devices junction capacitance. As such CV simulations were performed for devices with 4, 6 and 8nm quantum wells. The simulation was performed from -1V to 1V in steps of 0.01V and the simulation frequency was 1MHz. The standard reference ASPATs were also simulated and the fully depleted and zero bias C_j showed good agreement with the C_j extracted from the S_{11} parameters in Chapter 5.

The CV simulations for the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs devices and the $In_{0.8}Ga_{0.2}As$/AlAs/$In_{0.53}Ga_{0.47}As$ devices are plotted in Figure 7.6.1 and Figure 7.6.2. As can be seen from the plots, the new structures show a much faster reduction in the forward and zero bias capacitance when compared with the standard reference ASPATs. The zero-bias capacitance for the 8nm quantum well $In_{0.18}Ga_{0.82}As$/AlAs/GaAs device is 13fF, a 10fF (~43%) reduction from the GaAs ASPAT device. Similarly, the $In_{0.8}Ga_{0.2}As$/AlAs/ $In_{0.53}Ga_{0.47}As$ device with an 8nm well has a zero bias C_j of 11fF down from 18fF (~40%) for the $In_{0.53}Ga_{0.47}As$ ASPAT This could be explained by the increase in the distance between the accumulation region at the base of the AlAs barrier and the doped collector layer. It is interesting to note that the new structures display a peak in the C-V curve which was not present in the standard ASPAT devices. This could potentially be explained by the build-up of charge in the potential well. This has been seen previously for resonant tunnelling diodes[149]. The fully depleted -0.5V and zero bias capacitances are presented in Table 7.6.1.

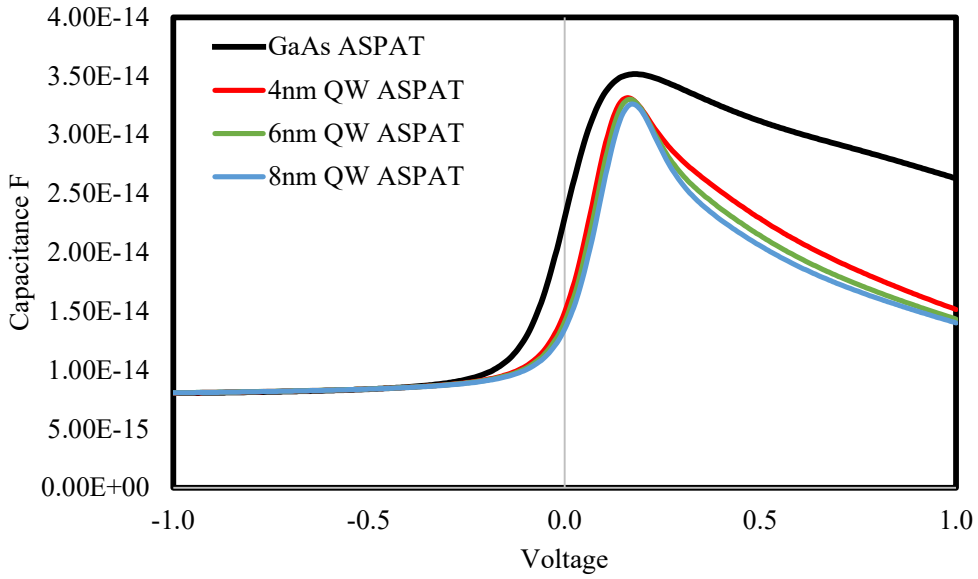

Figure 7.6.1 Simulated CV curves of GaAs/AlAs ASPAT and $In_{0.18}Ga_{0.82}As$/AlAs/GaAs structures with 4nm, 6nm and 8nm wells.

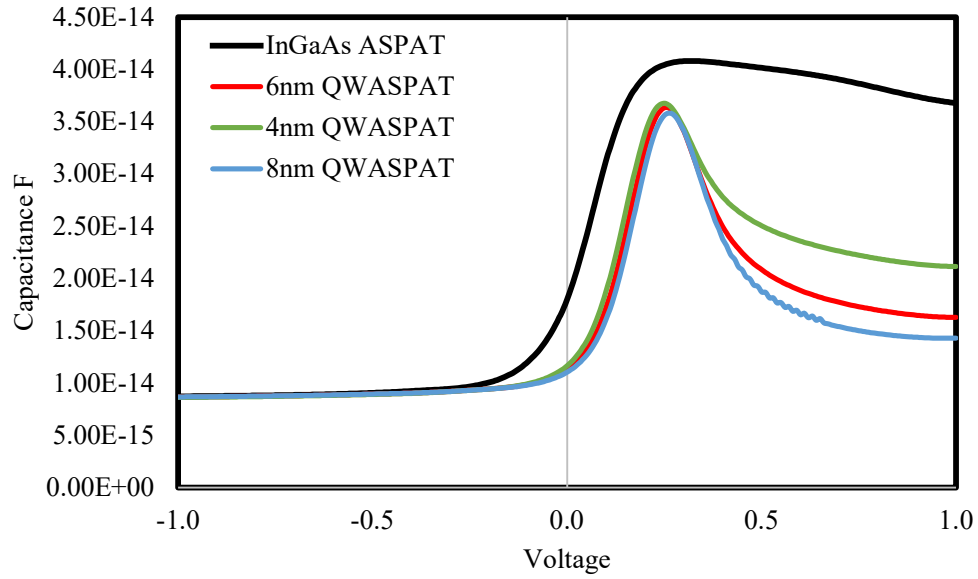

Figure 7.6.2 Simulated CV curves of $In_{0.53}Ga_{0.47}As$/AlAs ASPAT and $In_{0.8}Ga_{0.2}As$/AlAs/ $In_{0.53}Ga_{0.47}As$ structures with 4nm, 6nm and 8nm wells.

Table 7.6.1. Junction capacitances at 0V and -0.5V of ASPAT devices and proposed new QW-ASPAT structures.

Device	***-0.5V Cj fF***	***0V Cj fF***
GaAs ASPAT Measured [88]	8.8	22
GaAs ASPAT Simulation	8.4	23
GaAs 4nm well	8.4	15
GaAs 6nm well	8.4	14
GaAs 8nm well	8.4	13
$In_{0.53}Ga_{0.47}As$ *ASPAT Measured* [88]	9.5	18
$In_{0.53}Ga_{0.47}As$ *ASPAT Simulated*	9.1	18
$In_{0.53}Ga_{0.47}As$ *4nm well*	8.9	12
$In_{0.53}Ga_{0.47}As$ *6nm well*	8.9	11
$In_{0.53}Ga_{0.47}As$ *8nm well*	9	11

To explore the improvement in the diode's performance for detection purposes, their cut-off frequencies, f_c, were calculated using Equation 2.5.13. This is simply $f_c = 1/2\pi R_s C_j$ where R_s is the series resistance. Assuming that the series resistance of the new devices is similar to the values of 23Ω and 18Ω for 4×4μm^2 GaAs and $In_{0.53}Ga_{0.47}As$ ASPATs found in Chapter 5 (as would be expected since the key layers contributing to R_s are identical) then an estimated cut off frequency of the new devices at zero bias can be calculated. These figures are shown in Table 7.6.2. The highest cut-off frequencies were both exhibited by the devices with the 8nm quantum wells. The 8nm $In_{0.18}Ga_{0.82}As$/AlAs/GaAs device had an estimated cut-off frequency of 532GHz, which is a significant improvement of 69% when compared to the 314GHz of the standard GaAs ASPAT. The 8nm quantum well $In_{0.8}Ga_{0.2}As$/AlAs/ $In_{0.53}Ga_{0.47}As$ device exhibited an estimated cut-off frequency of 803GHz, which is a 63%

improvement when compared to the standard $In_{0.53}Ga_{0.47}As$ ASPAT. The lower cut off frequencies for the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs devices is largely due to their higher series resistances.

Table 7.6.2 Estimated cut off frequencies of standard ASPAT devices and proposed QW-ASPAT structures

Device	R_s **Ω**	C_j ***fF***	f_c ***GHz***
GaAs ASPAT Measured [88]	23	22	314
GaAs ASPAT Simulation	23	23	300
GaAs 4nm well	23	15	461
GaAs 6nm well	23	14	494
GaAs 8nm well	23	13	532
$In_{0.53}Ga_{0.47}As$ *ASPAT Measured* [150]	18	18	491
$In_{0.53}Ga_{0.47}As$ *ASPAT Simulated*	18	18	491
$In_{0.53}Ga_{0.47}As$ *4nm well*	18	12	737
$In_{0.53}Ga_{0.47}As$ *6nm well*	18	11	803
$In_{0.53}Ga_{0.47}As$ *8nm well*	18	11	803

7.7. Conclusion

In this section two new barrier-well heterostructure devices were proposed based upon GaAs and $In_{0.53}Ga_{0.47}As$ ASPATs. These new structures included a quantum well on the short spacer side of the AlAs barrier. These quantum wells would be created using $In_{0.18}Ga_{0.82}As$ for the GaAs devices and $In_{0.8}Ga_{0.2}As$ for the InGaAs devices. The addition of these quantum wells is intended to increase the barrier height in reverse bias and therefore reduce the leakage current of the devices. This would also improve

the devices curvature coefficients. To quantify the potential improvements to the devices the physical models of the ASPAT devices from Chapter 5 were modified to include the potential wells. After DC simulations were performed, the devices showed over an order of magnitude reductions in the leakage current from 5.1μA and 4.3μA for standard 4×4μm^2 GaAs and $In_{0.53}Ga_{0.47}As$ ASPATs respectively to 360nA and 205nA for the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs and $In_{0.8}Ga_{0.2}As$/AlAs/$In_{0.53}Ga_{0.47}As$ QW-ASPATs with 6nm quantum wells. This also drastically improved the k_v to 32V^{-1} for both QW-ASPAT devices. This represents an increase in curvature coefficient by a factor of approximately 2.5 over the reference ASPAT devices and is much closer to the Schottky diodes inherent 40V^{-1} limit.

The addition of the quantum wells also increased the devices junction resistance substantially. This is undesirable due to the ASPAT's already large junction resistance increasing the diodes response time and would pose significant challenges in the creation of a matching circuit if the devices were used as part of a detector. As such the devices quantum well and AlAs barrier thicknesses were varied in the simulation as part of an optimization strategy. The k_v and R_j of the devices were then extracted from the simulated data at zero-bias to create a map in the parameter space. The highest k_v of the two devices were 33V^{-1} and 35V^{-1} for the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs and $In_{0.8}Ga_{0.2}As$/AlAs/$In_{0.53}Ga_{0.47}As$ QW-ASPATs respectively.

From the optimization map it became clear that the best method of improving overall device performance was to reduce the thickness of the AlAs barrier. This would offer a significant reduction in R_j with only minimal drops in k_v. By reducing the barrier thickness from 3nm to 1nm R_j reduced from 1.7MΩ to 1.9kΩ for the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs devices with 6nm wells and from 4.2MΩ to 1kΩ for the $In_{0.8}Ga_{0.2}As$/AlAs/ $In_{0.53}Ga_{0.47}As$ devices with 6nm wells It would also be possible to reduce R_j by reducing quantum well thickness however this would come with a penalty in terms of k_v.

To understand the effect that the introduction of quantum wells would have on the device's RF characteristics C-V simulations were performed for devices with 4, 6 and 8nm quantum wells. These simulations showed a reduction in the zero-bias capacitance with the addition of quantum wells. The 8nm quantum well devices showed the largest reduction in the zero-bias capacitance with values of 13fF and 11fF

for he $In_{0.18}Ga_{0.82}As$/AlAs/GaAs and $In_{0.8}Ga_{0.2}As$/AlAs/$In_{0.53}Ga_{0.47}As$ structures respectively compared with 23fF and 18fF for standard ASPAT devices without quantum wells.

The estimated cut off frequencies of the new devices were obtained using the assumption that the series resistances would be similar to those of the standard ASPATs. This led to estimated cut-off frequencies of 532GHz for the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs device and over 800GHz for the $In_{0.8}Ga_{0.2}As$/AlAs/ $In_{0.53}Ga_{0.47}As$ device. These are both substantial improvements over the values of 314GHz and 491GHz obtained for the standard ASPAT diodes. The lower cut-off frequencies of the $In_{0.18}Ga_{0.82}As$/AlAs/GaAs devices are caused by the devices increased series resistance when compared with the $In_{0.8}Ga_{0.2}As$/AlAs/ $In_{0.53}Ga_{0.47}As$ devices.

CHAPTER 8

$Al_xGa_{(1-x)}As$-AlAs-$In_{0.18}Ga_{0.82}As$ Heterostructure Diodes

8.1. Introduction

In Chapter 7 the ASPATs characteristics as detector diodes were improved with the addition of quantum wells to the short spacer side increasing the reverse bias barrier height. This led to large reductions in the leakage current and an improvement in the device curvature coefficients to $33V^{-1}$ and $35V^{-1}$ for GaAs and $In_{0.53}Ga_{0.47}As$ structures respectively. These are substantial improvements over the standard ASPAT devices; however, they still fall short of the $40V^{-1}$ Schottky diode curvature coefficient. The logical next step to improve the curvature coefficient is to increase the current flow in forward bias. To do this a method of reducing the barrier height in forward bias is necessary.

This chapter will focus on the use of $Al_xGa_{1-x}As$ in the QW-ASPAT to reduce the barrier height on the long spacer side of the devices. These new structures will be investigated using Silvaco ATLAS by modifying the QW-ASPAT models used in Chapter 7. DC simulations of the new structures were performed, and the devices junction resistance and curvature coefficients extracted.

The new devices parameters such as barrier thickness, quantum well thickness and $Al_xGa_{1-x}As$ composition were explored in detail via simulation to determine their effect on the device performance. The emitter and collector layer doping and thickness were also be explored in this chapter as a method to improve the device performance.

The devices C-V characteristics were also be simulated to determine the devices suitability for high frequency detection. The cut-off frequencies of the new devices were estimated and compared with the QW-ASPAT devices from Chapter 7 and the standard ASPAT devices from Chapter 5.

8.2. Device Epitaxial Structures

In the previous section the reverse bias barrier height was increased with the addition of the quantum well. To further improve the ASPAT structure it could be beneficial to reduce the barrier height in the forward bias. This is easily achieved for the GaAs based devices with the addition of Al to the compound to create the ternary compound $Al_xGa_{1-x}As$. As AlAs and GaAs are lattice matched $Al_xGa_{1-x}As$ can be grown at any composition without straining the lattice or introducing dislocations. However, the upper limit for $Al_xGa_{1-x}As$ composition in this device will be x=0.4 as that is the point at which $Al_xGa_{1-x}As$ stops being a direct bandgap semiconductor. As AlAs has a higher bandgap than GaAs, increasing the Al composition, *x*, increases the bandgap of $Al_xGa_{1-x}As$. This reduces the bandgap discontinuity at the spacer-barrier interface in the conduction band and reduces the barrier height. Figure 8.2.1 shows the conduction band at the barrier for $Al_xGa_{1-x}As$ compositions x=0, x=0.1 and x=0.2. As is clear, the barrier is reduced by 0.09eV for x=0.1 and by 0.2eV for x=0.2.

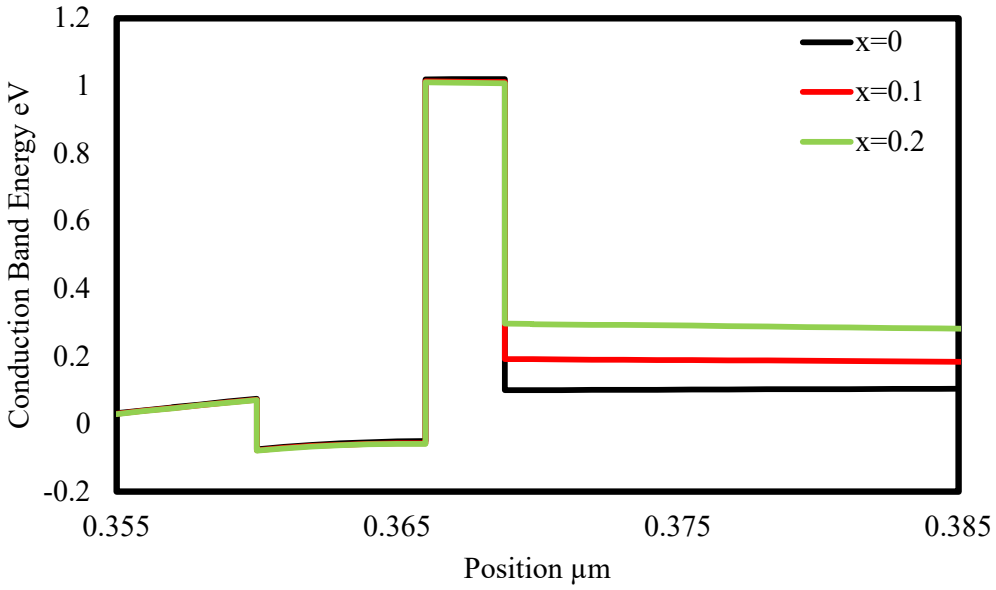

Figure 8.2.1 Conduction band profile of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure for various $Al_xGa_{1-x}As$ compositions.

The remaining device will be identical to the GaAs QW-ASPAT described previously in Chapter 7. The ohmic contacts are doped to 4×10^{18} cm^{-3} and the emitter and

collector layers will be 35nm and doped to 1×10^{17} cm^{-3}. The devices have 5nm short GaAs spacers and 200nm long $Al_xGa_{1-x}As$ spacers. The quantum wells are created with $In_{0.18}Ga_{0.82}As$ and initially is 6nm thick whilst the AlAs barrier is 2.8nm. Other quantum well and barrier thicknesses were also investigated later in the chapter. The full epitaxial structure of the device is described in Table 8.2.1. All devices were simulated at a size of $4\times4\mu m^2$ to allow for accurate comparison between the devices and to maintain consistency with all devices studied in this research.

Table 8.2.1 Epitaxial Layer structure of new device

	LAYER
	GaAs 4×10^{18} cm^{-3}
	GaAs 1×10^{17} cm^{-3}
5 nm	GaAs (spacer 1)
6 nm	$In_{0.18}Ga_{0.82}As$ (well)
2.8 nm	AlAs (barrier)
200nm	$Al_xGa_{1-x}As$ (spacer 2)
	GaAs 1×10^{17} cm^{-3}
	GaAs 4×10^{18} cm^{-3}

8.3. Device Models

As in the previous chapters, the devices were modelled in Silvaco ATLAS. The device models were based on the GaAs ASPAT model shown previously and modified to include the $In_{0.18}Ga_{0.82}As$ quantum well and the $Al_xGa_{1-x}As$ spacer. The DC characteristics of the device were simulated using the *semiconductor-insulator-semiconductor* model which has been previously explained in this work in Chapters 4, 5 & 7.

The material parameters for the devices were specified in ATLAS for each material. The AlAs bandgap was specified to be the direct 2.8eV as opposed to the standard indirect 2.2eV. This is due to the main tunnelling mechanism being between the Γ-Γ direct bandgap as shown in [86]. The value of the AlAs affinity was chosen to be 3.15eV so that the 65:35 conduction band valance band offset split at GaAs/AlAs interfaces was maintained.

The properties of the $In_{0.18}Ga_{.82}As$ quantum well were calculated as described in Chapter 4 using the equations

$$\chi = (4.9 - 0.82x)eV \tag{8.3.1}$$

and

$$E_g = (0.36 + 0.63x + 0.43x^2)eV \tag{8.3.2}$$

this led to values of 4.22eV for the electron affinity and 1.16eV for the bandgap.

The affinity and bandgap of $Al_xGa_{1-x}As$ were calculated using the equations

$$\chi = (4.07 - 1.1x)eV \tag{8.3.3}$$

and

$$E_g = (1.42 + 1.16x + 0.37x^2)eV \tag{8.3.4}$$

as described in Chapter 4. The material parameters of all the materials used in these models are shown in Table 8.3.1.

Table 8.3.1 Material parameters for $Al_xGa_{1-x}As$ heterostructure diodes.

Material	*Affinity (eV)*	*Bandgap (eV)*
GaAs	4.07	1.4
AlAs	3.15	2.8
$\boldsymbol{In_{0.18}Ga_{0.82}As}$	4.22	1.16
$\boldsymbol{Al_xGa_{1-x}As}$	4.07-1.1x	$1.42+0.63x+0.43x^2$

8.4. DC Characteristics

The DC characteristics of the devices were simulated form -1V to 1V in steps of 0.01V for devices with $Al_xGa_{1-x}As$ compositions of 0.1, 0.15 and 0.2. From these simulated I-V curves, the devices curvature coefficients and junction resistances were extracted. The I-V curves of the new devices are shown in Figure 8.4.1 and the junction resistances and curvature coefficients are shown in Figure 8.4.2 and Figure 8.4.3.

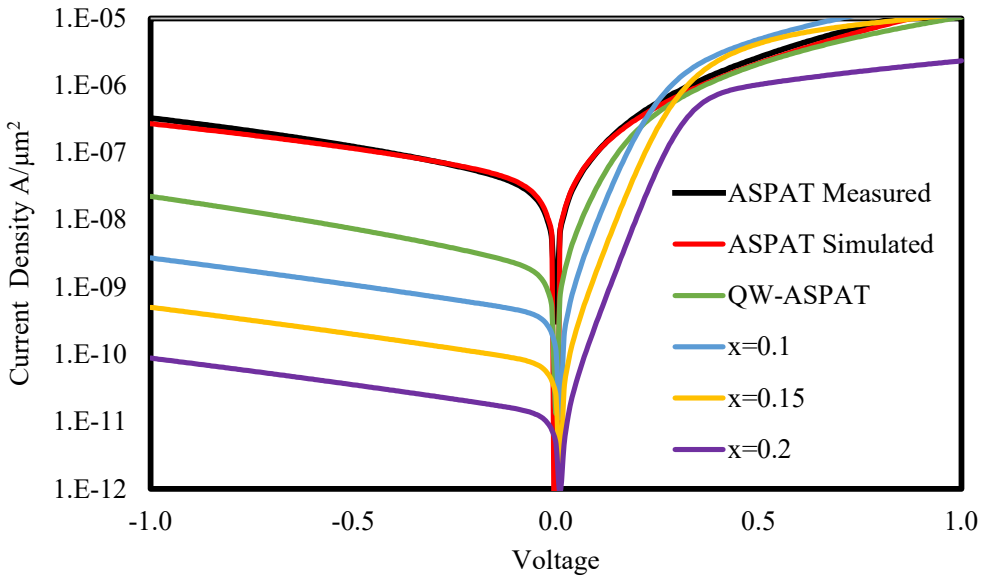

Figure 8.4.1 Simulated current-voltage curves of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes denoted structure #1 with different Aluminium fractions, an equivalent QW-ASPAT and measured and simulated standard ASPAT curves.

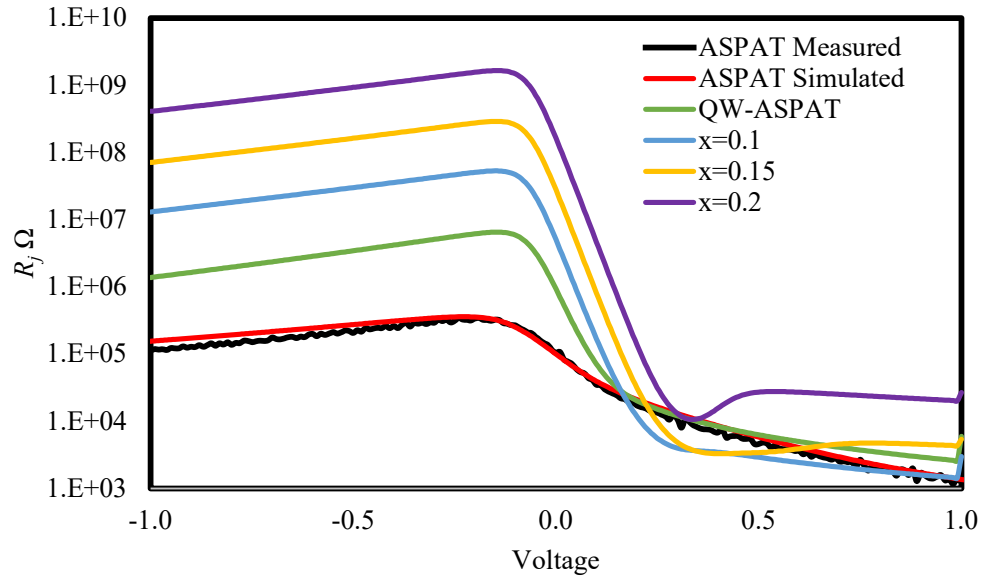

Figure 8.4.2 Simulated junction resistance of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes denoted structure #1 with different Aluminium fractions, an equivalent QW-ASPAT and measured and simulated standard ASPAT curves.

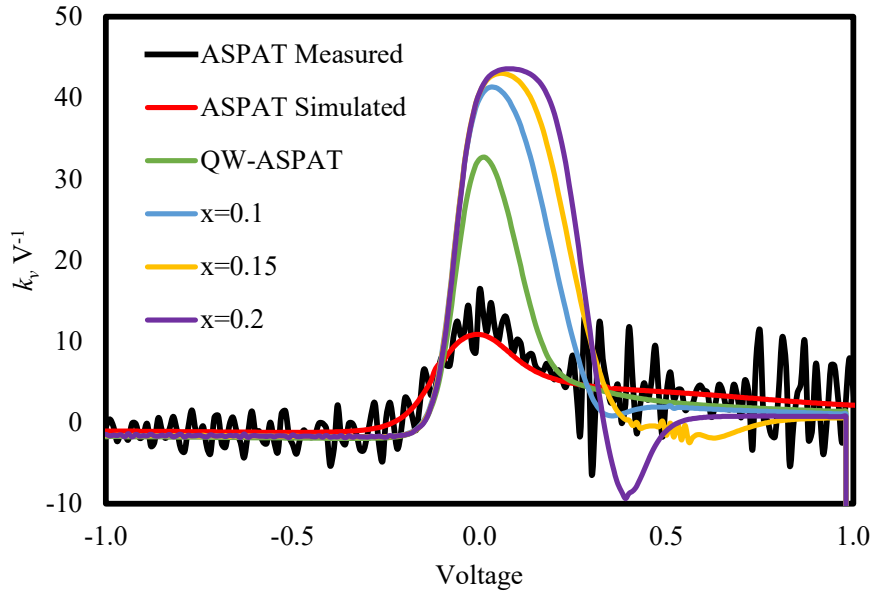

Figure 8.4.3 Simulated curvature coefficients of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes denoted structure #1 with different Aluminium fractions, an equivalent QW-ASPAT and measured and simulated standard ASPAT curves.

As can be seen from the figures, the new devices show a marked improvement in the device curvature coefficient at zero bias with x=0.1 leading to a k_v of 40V^{-1} and x=0.15 and x=0.2 showing k_v of 41V^{-1}, this puts the new devices above the inherent Schottky diode limit and would be the first diodes to do so based on the GaAs platform.

However, the new diodes show drastic increases in device junction resistance with zero bias R_j of 5MΩ, 27MΩ and 163MΩ for x=0.1, 0.15 and 0.2 respectively. This is to be expected as the electrons have a higher barrier to overcome when traveling from the doped emitter to form the accumulation region at the base of the barrier.

To improve the device performance, the junction resistance must be reduced substantially. As was discussed in the previous section, this can be achieved by reducing the barrier thickness. However, due to the extremely high nature of R_j other strategies may also be necessary such as improving the emitter and collector layer structures as shown in the next section.

8.5. Device Optimization

To reduce the devices high junction resistance a new emitter/collector doping profile was developed. The layers were reduced from 35nm thick to a thickness of 5nm and the doping concentration was increased to 4×10^{17} cm^{-3} from 1×10^{17} cm^{-3}. For the purposes of this section, the original structure shown in Table 8.2.1 will be denoted as structure #1 and the new structure will be denoted as structure #2. The effect of this change on the device characteristics was explored by simulating this new structure with $Al_xGa_{1-x}As$ compositions of 0.1, 0.15 and 0.2. The devices I-V curves are plotted on Figure 8.5.1 and the devices junction resistance and k_v are plotted on Figure 8.5.2 & Figure 8.5.3

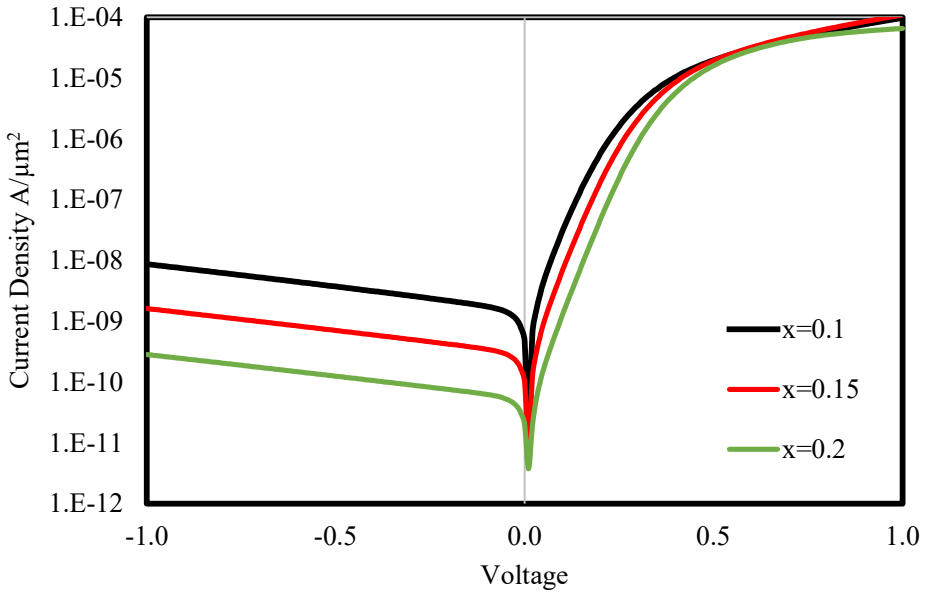

Figure 8.5.1 Simulated current-voltage curves of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes denoted structure #2 with different aluminium fractions.

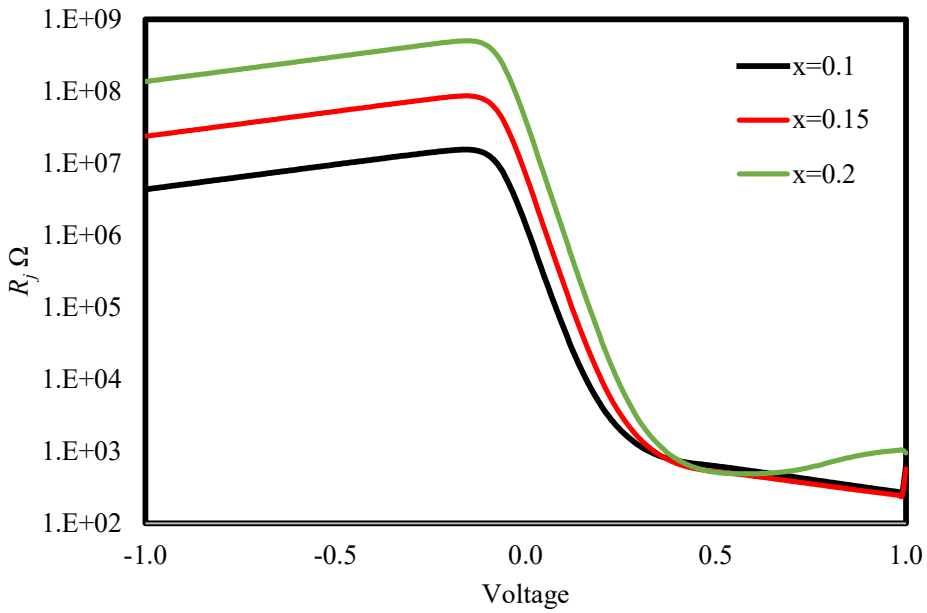

Figure 8.5.2 Simulated junction resistance of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes denoted structure #2 with different Aluminium fractions.

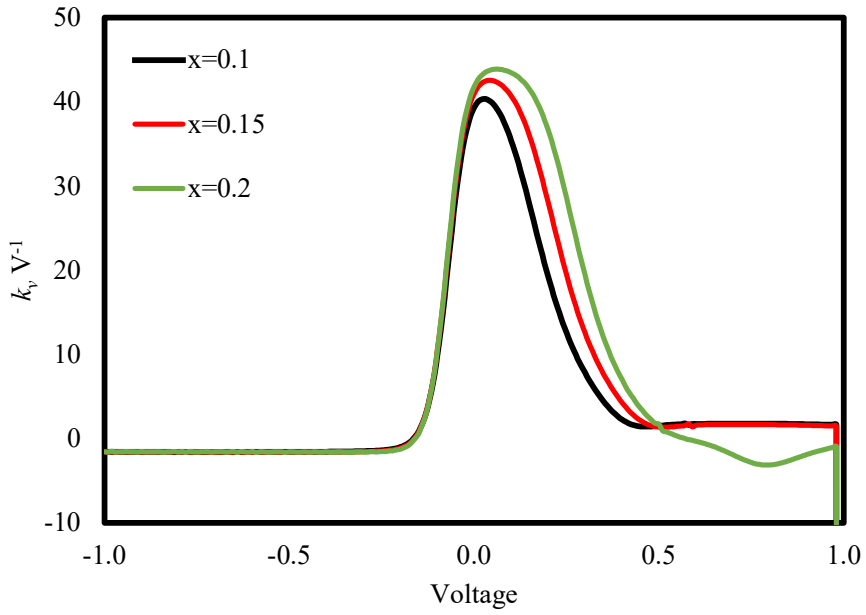

Figure 8.5.3 Simulated curvature coefficients of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes denoted structure #2 with different Aluminium fractions.

Figure 8.5.4 and Figure 8.5.5 show the zero bias k_v and the zero bias R_j of the two structures for each $Al_xGa_{1-x}As$ composition. As can be seen from the figures, the new emitter and collector structure have reduced the R_j for all compositions It is also apparent that the devices R_j increases exponentially with the Al fraction. The new structures have also improved the devices zero bias curvature coefficient to $42V^{-1}$ for x=0.2. It should be noted that the maximum k_v of the new devices are no longer at 0V but instead further into the forward bias regime. The maximum k_v for any of the devices is $44V^{-1}$ at 0.06V for x=0.2.

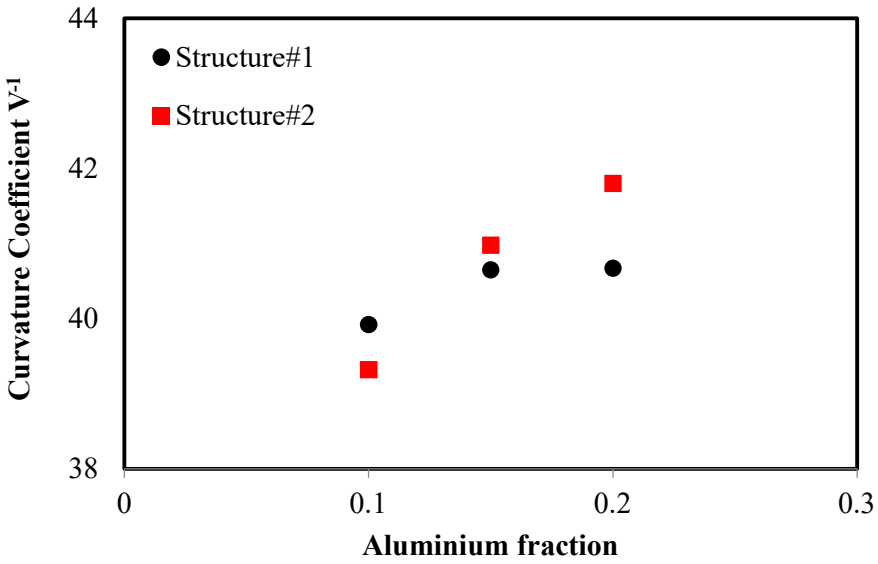

Figure 8.5.4 k_v versus Al fraction of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure devices with two different emitter/collector structures.

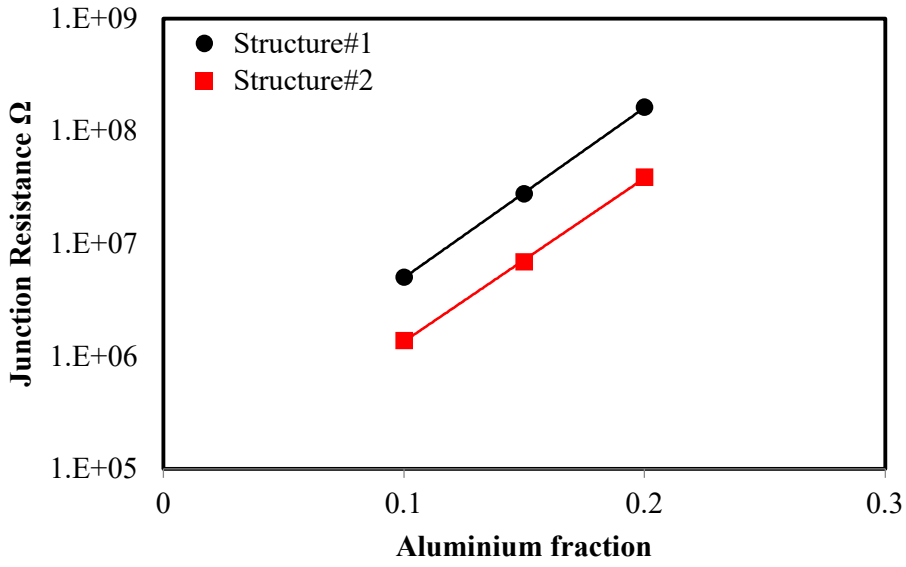

Figure 8.5.5 Zero bias R_j versus Al fraction of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes with two different emitter/collector structures.

Following the introduction of the new emitter/collector profiles, the devices were simulated with varying quantum well and barrier thicknesses at a series of $Al_xGa_{1-x}As$ compositions. The quantum well thickness, t_w, was varied from 2nm to 8nm in steps of 1nm, the AlAs barrier thickness, t_b, was varied from 1nm to 2.5nm in steps of 0.5nm and the Aluminium fraction, x, was varied from 0 to 0.15 in steps of 0.05. The zero bias R_j and k_v were extracted from the simulations and used to create optimisation maps. These are shown in Table 8.5.1 and Table 8.5.2. k_v is coloured with high values in green and low values in red reflecting their desirability. R_j is coloured with low values in green and high values in red as lower R_j values are desirable.

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Table 8.5.1 Optimisation maps of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes denoted structure #2 k_v against t_b, t_w, and x.

t_b=1nm	t_w nm			k_v V^{-1}			
x	2	3	4	5	6	7	8
0	11	16	19	22	25	27	28
0.05	24	29	32	34	35	36	36
0.1	35	37	38	39	39	40	40
0.15	39	40	41	41	41	42	42

t_b=1.5nm	t_w			k_v V^{-1}			
x	2	3	4	5	6	7	8
0	19	23	26	29	30	32	32
0.05	30	35	35	36	37	37	38
0.1	37	38	39	40	40	40	40
0.15	40	41	41	41	42	42	42

t_b=2nm	t_w nm			k_v V^{-1}			
x	2	3	4	5	6	7	8
0	21	25	28	30	31	32	33
0.05	31	33	35	36	37	37	38
0.1	37	38	39	40	40	40	40
0.15	40	41	41	41	41	41	41

t_b=2.5nm	t_w nm			k_v V^{-1}			
x	2	3	4	5	6	7	8
0	21	25	27	29	31	32	32
0.05	30	33	35	36	36	37	37
0.1	37	38	39	39	39	40	40
0.15	40	40	41	41	41	41	41

Table 8.5.2 Optimisation maps of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes denoted structure #2 R_j against t_b, t_w, and x.

	t_b=1nm		t_w nm			Rj Ω	
x	2	3	4	5	6	7	8
0	46	68	97	132	174	222	276
0.05	149	252	389	560	763	998	1.2k
0.1	696	1.2k	1.9k	2.9k	4.0k	5.3k	6.7k
0.15	4.1k	7.5k	12.1k	17.9k	24.9k	33.0k	42.0k

	t_b=1.5nm		t_w *nm*			Rj Ω	
x	2	3	4	5	6	7	8
0	191	309	463	653	877	1.1k	1.4k
0.05	705	1.9k	1.9k	2.8k	3.8k	5.0k	6.3k
0.1	3.2k	5.9k	9.4k	13k	19.0k	25.3k	32.2k
0.15	18.2k	33.6k	54.2k	80.1k	111k	148k	188k

	t_b=2nm		t_w nm			Rj Ω	
x	2	3	4	5	6	7	8
0	1.0k	1.6k	2.6k	3.6k	4.9k	6.3k	8.0k
0.05	3.7k	6.5k	10.2k	14.8k	20.3k	26.6k	33.7k
0.1	16.3k	29.5k	47.2k	69.3k	95.7k	126k	160k
0.15	85.5k	157k	254k	376k	521k	689k	878k

	t_b=2.5nm		t_w nm			Rj Ω	
x	2	3	4	5	6	7	8
0	5.8k	9.5k	14.4k	20.3k	27.4k	35.6k	44.8k
0.05	19.9k	34.8k	54.5k	78.9k	108k	142k	179k
0.1	82.5k	149k	238k	3449k	481k	634k	806k
0.15	406k	745k	1.2M	1.8M	2.4M	3.2M	4.1M

The optimization maps show that k_v is much more dependent on x than it is on either t_b or t_w. Whilst t_w influences low x devices such as x=0.05, for the higher values of x such as x=0.15 the increase in t_w has little effect on k_v as it plateaus. The influence of t_b on k_v is similar in that it can increase k_v up to a point before reaching a plateau where further increase is not possible.

The device junction resistance show a strong exponential dependency on both x and t_b this is clearly demonstrated in Figure 8.5.6 in which the zero bias R_j is plotted against t_b for x=0, 0.05, 0.1 and 0.15 for t_w=6nm. R_j also shows a dependency on t_w squared. This is shown in Figure 8.5.7 where R_j is plotted against t_w for x=1 and t_b=1nm. A second order polynomial has been fitted to the data and shows excellent agreement to the data with an R^2 value of 1.

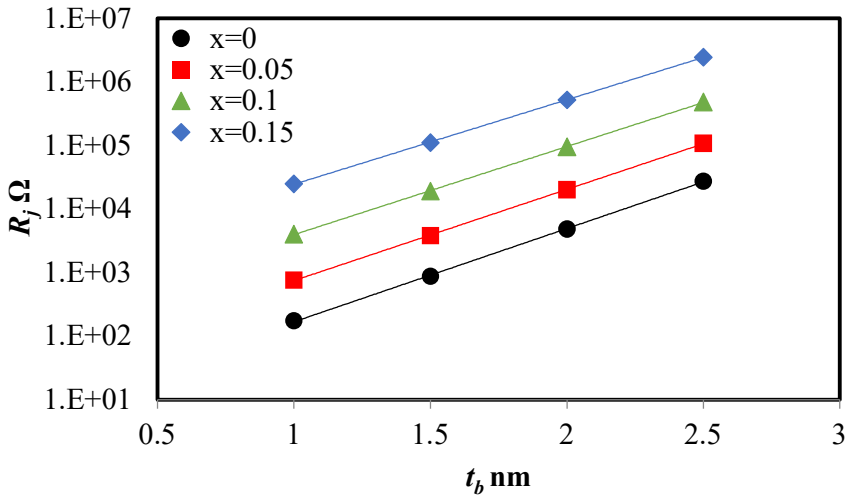

Figure 8.5.6 R_j of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes denoted structure #2 devices with t_w=6nm

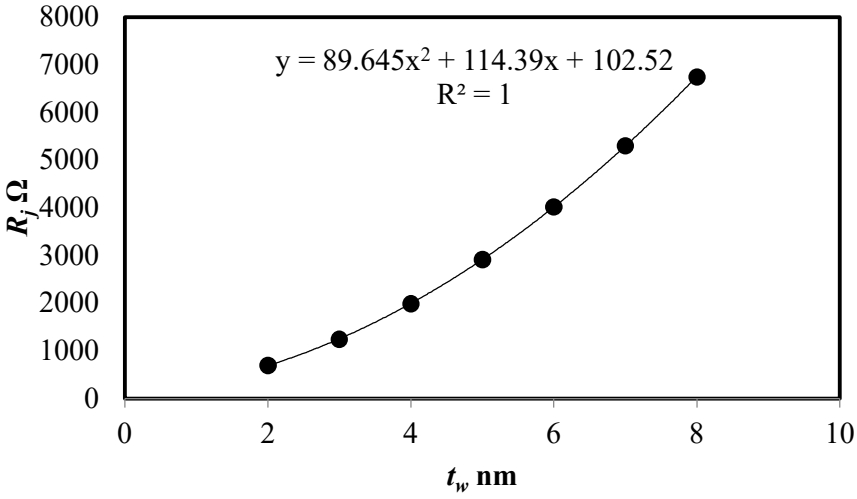

Figure 8.5.7 R_j of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes denoted structure #2 plotted against t_w for x=1 and t_b=1nm with a polynomial fit

From this data, it is clear that a thin ~1nm AlAs barrier is the best method of reducing device R_j to levels suited to detector diode applications. The remaining parameter choices would depend on the desired characteristics of the device. If the reduction of R_j is the most important aspect, then choosing devices with a low x such as 0.05 would be preferable. However, if the main objective is high k_v then the devices with higher x are more suited. Reducing t_w is an option to reduce R_j for the x=0.15 devices but the effects this may have on the device capacitance should first be explored, in the case of the QW-ASPAT devices reducing t_w increased the devices junction capacitance C_j.

8.6. Device C-V characteristics

As for the QW-ASPAT in Chapter 7 it is important to investigate the C-V characteristics of the new devices to determine their suitability to detection applications and quantify the frequency range these devices would be able to operate in. To do this, the structure #2 physical models were used to perform a series of C-V simulations for devices with t_w=6nm and t_b=2.8nm and x=0.05, 0.1, 0.15 and 0.2. The simulations were performed from -1V to 1V in steps of 0.05V at 1MHz and the results of the simulation are shown in Figure 8.6.1. The zero bias C_j is plotted against x for the devices in Figure 8.6.2. As can be seen from Figure 8.6.1 the fully depleted capacitance at -1V does not change significantly with x and all devices show a fully depleted C_j of ~9fF. It is in the forward and zero bias regimes that the value of x influences the devices C-V characteristics.

The zero and fully depleted capacitances of the devices are shown in Table 8.6.1. As can be seen, the devices show a similar fully depleted capacitance as the QW-ASPAT and GaAs ASPATs from Chapters 5 & 7. However, the devices also show a large improvement in the zero-bias Cj with the x=0.2 device showing a value of 8.6fF almost equal to the fully depleted capacitance. This is a large improvement from the equivalent QW-ASPAT and the GaAs ASPAT whose zero bias C_j were 22fF and 14fF respectively. It is difficult to provide estimated cut-off frequencies for these devices as the change to an $Al_xGa_{1-x}As$ spacer will have an impact on the series resistance R_s. However, the reduction in C_j is a significant improvement to the device performance and if an R_s of 23Ω is assumed as for the QW-ASPAT and GaAs ASPAT then the estimated cut-off frequency of the x=0.2 device would be 804GHz and represent an

increase of 256% from the standard GaAs ASPAT value of 314GHz. The estimated zero-bias cut-off frequencies, f_c, are shown in Table 8.6.1.

Table 8.6.1 fully depleted and zero bias C_j of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes denoted structure #2 devices and estimated cut-off frequencies

x	***-0.5V Cj* fF**	***0V Cj* fF**	***f_c* GHz**
0.05	8.9	14.6	474
0.1	8.7	11.5	602
0.15	8.5	9.6	720
0.2	8.5	8.6	804

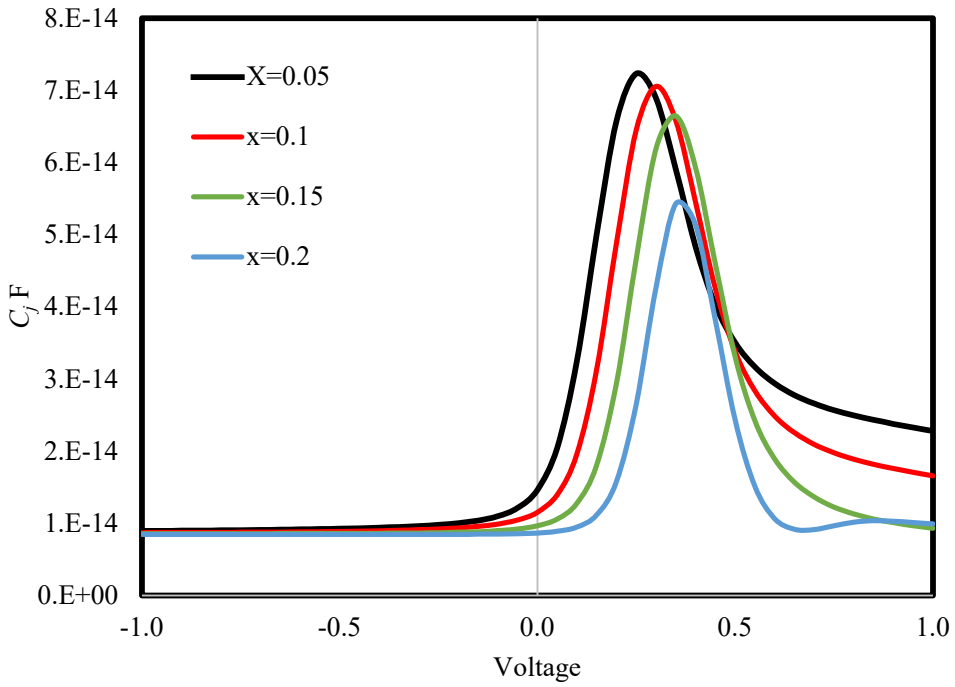

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Figure 8.6.1 C-V simulations of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes denoted structure #2 devices with t_w=6nm and t_b=1nm

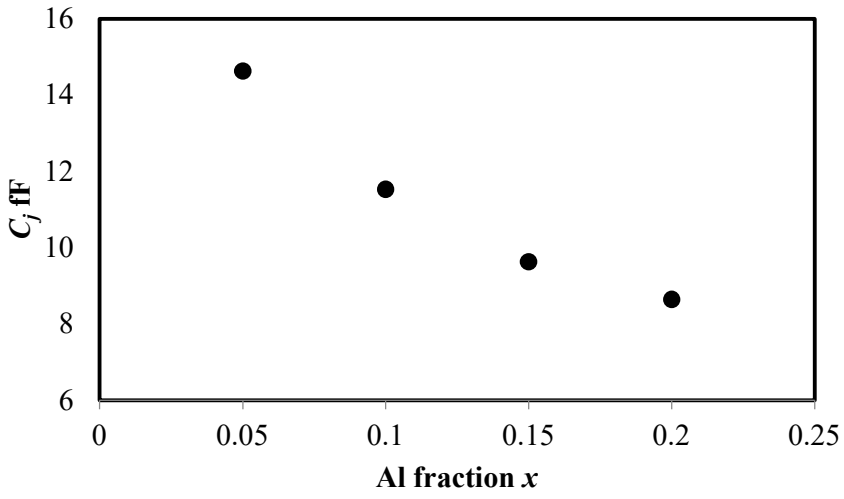

Figure 8.6.2 Zero bias C_j of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes denoted structure #2 devices with t_w=6nm and t_b=1nm plotted against Al fraction.

The devices all show peaks in the C-V characteristic as was seen in the QW-ASPAT devices. The height of the peaks reduces with increasing x and the peaks are shifted to higher biases with increasing x. The cause of the peaks could be explained by the build-up of charge in the quantum well whilst charge is also built up in the accumulation layer. The charge concentration profile in the device was extracted from the physical model at 0V, 0.3V and 0.5V for the x=0.1 device and are shown in Figure 8.6.3. As can be seen from the figure, at zero bias there is no charge in the accumulation layer, whilst at 0.5V there is little charge in the quantum well. It is only when the charge is in both areas separated by a small 2.8nm barrier that the capacitance is at its peak. This would also explain the reduction and shifting in the capacitance peaks with increasing x. As x increases, the energy required by the electrons to cross the large $Al_xGa_{1-x}As$ spacer and form an accumulation layer is increased. As such the amount of charge in the accumulation layer is reduced with increasing x reducing the peak height. Similarly, it requires a higher bias voltage for the accumulation layer to form, shifting the peaks to higher voltages.

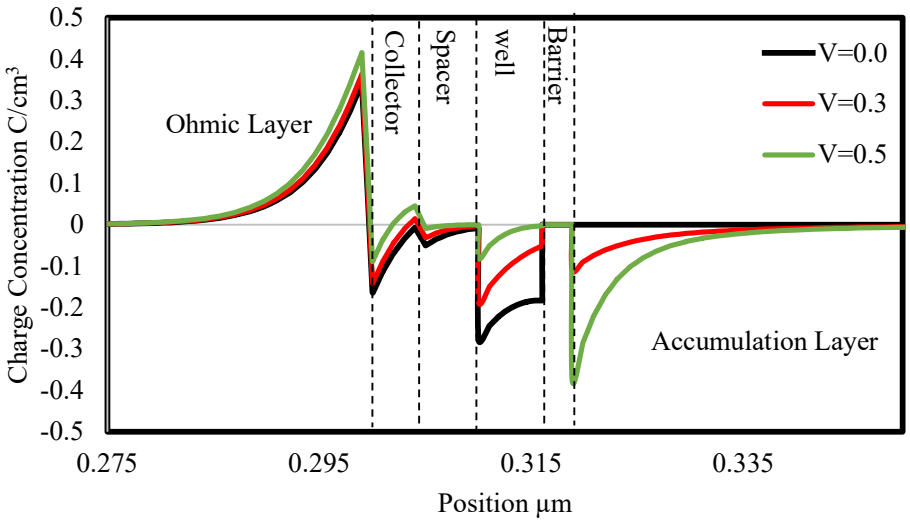

Figure 8.6.3 Charge profile of $In_{0.18}Ga_{0.82}As/AlAs/Al_xGa_{1-x}As$ heterostructure diodes denoted structure #2 device with x=0.1, t_b=2.8nm and t_w=6nm at 0V, 0.3V and 0.5V.

8.7. Conclusion.

In this section the effects of adding $Al_xGa_{1-x}As$ to the long spacer side of the QW-ASPAT were explored. This was done by modifying the physical models of the QW-ASPAT device from Chapter 7. The Al fraction x was varied from 0.05 to 0.2. This led to an increase in the curvature coefficient with the highest zero bias k_v value of $42V^{-1}$ being achieved for x=0.2. This is higher than the inherent Schottky diode limit of $40V^{-1}$ and would represent the highest curvature co-efficient achieved on a GaAs platform.

To reduce the large junction resistance a new emitter/collector doping profile was introduced. This led to a reduction in R_j for all devices. This new structure was then simulated with varying t_b, t_w and x to create device optimization maps. It was apparent that the device junction resistance was exponentially dependant on t_b, as seen for the QW-ASPAT, and exponentially dependent on x. R_j was also found to be quadratically dependent on the quantum well thickness t_w. k_v was found to be most dependant on x and t_w with the barrier thickness not having much effect. As such the most effective way to reduce the junction resistance of the device would be by using thinner 1nm barriers as opposed to the 2.8nm barriers used in the standard ASPAT devices.

The C-V characteristics were investigated for devices with t_w=6nm and t_b=2.8nm. This showed that increasing x reduces the zero-bias capacitance with the x=0.2 device leading to a zero bias C_j almost identical to its fully depleted C_j. The C-V curves of the devices contained peaks in the forward bias regime. This was attributed to the interaction of charge in the accumulation layer and the quantum well. The cut-off frequencies of the devices were estimated using the assumption that R_s would be similar to that of the GaAs ASPAT value of 23Ω. This led to an estimated cut-off frequency for the x=0.2 device of 804GHz representing an increase by a factor of 256% when compared with the standard GaAs ASPAT. This figure may not be entirely accurate as the effect of the $Al_xGa_{1-x}As$ spacer on the series resistance has not yet been quantified.

CHAPTER 9

CONCLUSIONS AND FUTURE WORK

9.1. Research Conclusions

The aim of this research was to improve and optimize the ASPAT diode so that it could surpass the Schottky diode as a zero-bias mm-Wave and THz detector element. This was done through the development of accurate physical models of current state of the art ASPAT diodes grown by molecular beam epitaxy on the GaAs and InP platforms. These physical models were then used to explore new device concepts and structures to improve the ASPATs curvature co-efficient above the inherent $40V^{-1}$ value of the Schottky diode.

In chapter 5 physical models were developed to accurately capture the behaviour of GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diodes with spacer layer ratios of 40:1. This was done for $4\times4\mu m^2$, $6\times6\mu m^2$ and $10\times10\mu m^2$ mesa area devices and compared with experimental data obtained from equivalent ASPATs grown via MBE and fabricated using i-line lithography. The simulated DC characteristics of the physical models show a close fit to the experimental data, validating the models which can then be used to investigate new structures. The extracted curvature coefficients of the ASPAT devices were $11V^{-1}$ and $12V^{-1}$ for the GaAs and the $In_{0.53}Ga_{0.47}As$ devices respectively.

The ASPAT devices RF performance was characterised using an equivalent circuit model. The devices series and junction resistances as well as the devices junction capacitance were found from fitting the equivalent circuits S_{11} parameters to the measured S_{11} parameters of the two diodes. The devices displayed a higher zero and forward bias junction capacitance than the fully depleted capacitances. This is caused by the charge in the device's accumulation region being mirrored by the positive charge in the collector contact. This behaviour was also apparent in the series resistance which was caused by the undoped spacer region not being fully depleted. The $In_{0.53}Ga_{0.47}As$ ASPAT showed a reduced series resistance when compared to the

GaAs ASPAT. This can be attributed to the increased mobility of $In_{0.53}Ga_{0.47}As$ and the increased level of doping in the ohmic contact layers.

The cut-off frequencies of the devices were calculated with the highest frequencies being reported for the $4\times4\mu m^2$ devices. The GaAs ASPATs showed a zero bias cut-off frequency of 301GHz and the $In_{0.53}Ga_{0.47}As$ devices showed a cut-off frequency of 491GHz. The higher cut-off frequency is attributed mainly to the reduced series resistance of the $In_{0.53}Ga_{0.47}As$ devices due to its higher mobility and doping.

Chapter 6 reports the development of $In_{0.53}Ga_{0.47}As$ metamorphic ASPAT (mASPAT) devices grown on GaAs substrates. The purpose of this was to maintain the advantages of using $In_{0.53}Ga_{0.47}As$ in ASPAT structures whilst also using cheaper, less brittle GaAs substrates and therefore reducing the overall expense and difficulty to manufacture $In_{0.53}Ga_{0.47}As$ ASPATs.

The effect of the metamorphic layer growth temperature on the device characteristics was also investigated by growing two identical structures, one at 440ºC and one at 500ºC. Following growth, devices were fabricated with mesa areas ranging from $1.5\times1.5\mu m^2$ to $6\times6\mu m^2$.The DC characteristics of the two mASPATs were measured with the 440ºC devices showing a higher zero-bias curvature coefficient of $13V^{-1}$ compared with the 500ºC devices $11V^{-1}$. The 440ºC devices also exhibited a higher junction resistance and scaled better with area than the 500ºC devices. Both metamorphic structures showed a reduced junction resistance compared with the standard $In_{0.53}Ga_{0.47}As$ ASPAT. This reduction amounted to approximately a factor of 10. The RF characteristics of the mASPATs were extracted from measured S_{11} parameter data using an equivalent circuit model. Both mASPAT devices showed higher junction capacitances than the standard ASPAT reducing the cut-off frequency. It was speculated that the cause of this increase as well as the reduction in junction resistance was due to an increased number of threading dislocations in the active device area caused by the metamorphic growth.

Chapter 7 reports two novel new device structures in which a quantum well is added to the short spacer side of the AlAs barrier, one based on the GaAs ASPAT and one based on the $In_{0.53}Ga_{0.47}As$ ASPAT. The characteristics of these new quantum well ASPAT (QW-ASPAT) structures were explored using the physical models developed

in Chapter 5. After DC simulations were performed, the devices showed order of magnitude reductions in their leakage currents. This also drastically improved the k_v to $32V^{-1}$ and $35V^{-1}$ for $In_{0.18}Ga_{0.82}As/AlAs/GaAs$ and $In_{0.8}Ga_{0.2}As/AlAs/In_{0.53}Ga_{0.47}As$ QW-ASPAT devices respectively. This represents an increase in curvature coefficient by a factor of approximately 2.5 over the reference ASPAT devices and is much closer to the Schottky diodes inherent $40V^{-1}$ limit.

Chapter 7 then goes on to investigate how the thickness of the quantum well and AlAs barrier affects the devices curvature coefficient and junction resistance. This was largely with the aim of reducing device junction resistance as overly large values would make the fabrication of a matching circuit as part of a detector too onerous. It was found that the junction resistance was exponentially dependent on the AlAs barrier thickness and as such reducing the barrier was determined to be the best way to reduce junction resistance whilst still maintaining high curvature values.

To investigate the impact of introducing the quantum wells on the device's RF performance C-V simulations were performed for devices with 4, 6 and 8nm quantum wells. These showed that the introduction of the quantum wells reduces the forward and zero-bias junction capacitances. The cut-off frequencies of these new devices were estimated with values of 532GHz being achieved for the $In_{0.18}Ga_{0.82}As/AlAs/GaAs$ devices and over 800GHz for the $In_{0.8}Ga_{0.2}As/AlAs/ In_{0.53}Ga_{0.47}As$ device. These are both substantial improvements over the values of 314GHz and 491GHz achieved for the standard ASPAT diodes.

Chapter 8 reports a new novel device based on the $In_{0.18}Ga_{0.82}As/AlAs/GaAs$ QW-ASPAT from chapter 7. This new device introduces $Al_xGa_{1-x}As$ as the long spacer reducing the AlAs barrier hight in the forward direction. This new structure was modelled, and DC simulations were performed. The Al fraction x was varied from 0.05 to 0.2. This led to an increase in the curvature coefficient with the highest zero bias k_v value of $42V^{-1}$ being achieved. This is higher than the inherent Schottky diode limit of $40V^{-1}$ and would represent the highest zero-bias curvature co-efficient achieved on a GaAs platform. Further simulations were performed to investigate the dependence of the DC characteristics on the thickness of the quantum well, AlAs barrier and aluminium fraction.

Chapter 8 then went on to explore the C-V characteristics of the new structures. It was found that increasing *x* reduces the zero-bias capacitance of the devices with Al fractions of 0.2 showing a zero bias capacitance almost identical to its fully depleted reverse bias capacitance. The cut-off frequencies of the devices were estimated with the highest values for the 0.2 Al fraction devices of 804GHz representing a 256% increase when compared with the standard GaAs ASPAT. As such the new device structure developed shows promise as a zero-bias mm-Wave and THz detector diodes, achieving higher curvature coefficients than the Schottky diode as well as increasing the cut-off frequency of the ASPAT significantly.

9.2. Future Work

In this work two new device concepts have been introduced, the QW-ASPAT and the $Al_xGa_{1-x}As$-AlAs-$In_{0.18}Ga_{0.82}As$ ASPAT Heterostructure Diode. However, the performance of these devices has only been simulated. The first step must be to verify the conclusions of this work by fabricating and testing these devices. As of the writing of this report, wafers have been grown for these structures and are awaiting fabrication. Ideally these would have been presented in this work, however due to the COVID-19 pandemic, the University of Manchester fabrication laboratory has had very limited access and therefore it was not possible to fabricate them during the course of this research.

Provided the new structures operate as intended, then further work should concentrate on the improvement of the RF characteristics of all the devices reported in this thesis. One aspect that should be investigated is the reduction of the spacer layer ratio in the QW-ASPAT and $Al_xGa_{1-x}As$ ASPAT heterostructure diode. This would mitigate the contribution to the series resistance from the undoped spacer layers at zero-bias increasing the device cut-off frequencies. This was not previously possible for the standard ASPAT due to the reduction of device curvature coefficient to unacceptable low levels.

Furthermore, the integration of the new device concepts into mm-Wave and THz detector circuits would be the logical end point of this research. This would require the design of matching circuits and antennas. If these devices are to achieve cut-off frequencies above 1THz then the fabrication of devices with sub-micron mesas is

necessary. This is not currently possible with the University of Manchester research groups facilities.

An additional area in which further research is recommended is the investigation of metamorphic layer growth. This would allow for $In_{0.53}Ga_{0.47}As$ devices to be achieved with reduced cost and an easier fabrication process. It should be noted that with metamorphic growth, the constraints of lattice matching would allow for devices to be grown with any Indium fraction (including InAs). This research should look into alternate grading profiles to grow metamorphic layers with reduced dislocations to ensure high quality devices are possible.

APPENDICES

Appendix A- ATLAS Simulation Physics

SILVACO ATLAS simulates the electrical characteristics of a general semiconductor device using a model derived from Maxwells equations for electromagnetism. This model consists of a set of fundamental equations which link together the electrostatic potential and carrier densities within the device. These equations can be split into three parts. The first of which is Poisson's Equation which relates electrostatic potentials with local charge densities. The second part is the carrier continuity equations, which ensure the conservation of charge in the device. The third part is the transport equations, these determine how the carriers are generated, recombined and move within the device.

I Poisson's Equation

Poisson's equation relates the space charge density to the electrostatic potential

$$\nabla^2\varphi = \frac{\rho}{\varepsilon}$$

I.1

where φ is the electrostatic potential, ρ is the space charge density and ε is the local permittivity. The reference potential can be defined in various ways. For ATLAS, this is always the intrinsic Fermi potential. The local space charge density is the sum of contributions from all mobile and fixed charges, including electrons, holes, and ionized impurities. The electric field of can be found by taking the gradient of the potential.

$$\vec{E} = -\nabla\varphi$$

I.2

II Carrier Continuity Equations

The continuity equations for electrons and holes in ATLAS are defined by the equations

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot \overrightarrow{J_n} + G_n - R_n$$

II.1

$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla \cdot \overrightarrow{J_p} + G_p - R_p$$

II.2

Where n and p are the electron and hole concentrations, $\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ are the electron and hole current densities, G_n and G_p are the electron and hole generation rates, R_n and R_p are the electron and hole recombination rates and q is the magnitude of charge for an electron. ATLAS solves both of these equations by default however, for certain applications, electron or hole continuity equations can be turned off when they are unnecessary.

III Transport Equations

Poisson's equation and the continuity equations provide a framework for simulation. However, specific models are needed to specify the electron and hole current densities and carrier generation and recombination rates. ATLAS provides a series of these models, the simplest being the Drift-Diffusion Model. This model is the default model for semiconductor simulation and the model that was used throughout this work, except when the Semiconductor-Insulator-Semiconductor model was specified for quantum tunnelling.

In the drift diffusion model, the current densities in the carrier continuity equations can be approximated as

$$\overrightarrow{J_n} = -q\mu_n \nabla \phi_n$$

III.1

$$\overrightarrow{J_p} = -q\mu_p \nabla \phi_p$$

III.2

Where μ is mobility and ϕ is the quasi-Fermi level. The quasi-Fermi levels are then linked to the carrier concentrations and electrostatic potential via the Boltzmann's approximations

$$n = n_i e^{\frac{q(\varphi - \phi_n)}{kT}}$$

III.3

$$p = -n_i e^{\frac{-q(\varphi - \phi_p)}{kT}}$$

III.4

where n_i is the intrinsic carrier concentration and T is the temperature of the lattice. These equations can then be re-written to define the quasi-Fermi potentials

$$\phi_n = \varphi - \frac{kT}{q} \ln \frac{n}{n_i}$$

III.5

$$\phi_p = \varphi + \frac{kT}{q} \ln \frac{p}{n_i}$$

III.6

If we then substitute these equations into the current density equations and take into account band bending effects and the effective electric fields for the carriers, we can reach the standard drift diffusion equations

$$\overrightarrow{J_n} = q\mu_n \overrightarrow{E_n} + qD_n \nabla n$$

III.7

$$\overrightarrow{J_p} = q\mu_p\overrightarrow{E_p} - qD_p\nabla p$$

III.8

where for Boltzmann statistics the Einstein relationship gives

$$D = \frac{kT}{q}\mu$$

III.9

for electrons and holes. This is modified to a more complex equation when Fermi-Dirac statistics are specified within ATLAS.

Appendix B-Example Silvaco Code for ASPAT simulation

```
GO ATLAS
##-------------------------------------------------------
# Simulation of In0.53Ga0.47As/AlAs ASPAT XMBE#326
# Mesa area: Scalable
# Models: SIS, Fermi
# Simulation Type: DC
# Emitter/collector Doping 1e17cm-3
# Ohmic layer doping 1.5e19 cm-3
# Spacer Ratio: 200nm:5nm
#-------------------------------------------------------
#    Device Epilayer Structure thicknesses in 'um'
#-------------------------------------------------------
# Thicknesses
set t_contact1=0
set t_ohmic1=0.3
set t_emitter=0.035
set t_spacer1=0.005
set t_barrier=0.00283
set t_spacer2=0.2
set t_collector=0.035
set t_ohmic2=0.4
set t_etch=0
set t_contact2=0

## Doping concentrations in cm-3
set d_ohmic1=1.5e19
set d_emitter=1e17
```

```
set d_collector=1e17
set d_ohmic2=1.5e19
set d_gap=1.5
set d_mesa=10
set d_device=20

## Layers
set I=$t_contact1
set A=$I+$t_ohmic1
set B=$A+$t_emitter
set C=$B+$t_spacer1
set D=$C+$t_barrier
set E=$D+$t_spacer2
set F=$E+$t_collector
set G=$F+$t_ohmic2
#-----------------------------------
# Mesh generator
#-----------------------------------
## The x.mesh and y.mesh specifies the location 'loc' of mesh
grid lines along the respective
## axis. 'spacing' determines the mesh spacing in microns at
the position specified by 'loc'
## parameter. The mesh spacing from one mesh statement to the
next is gradually changed and is managed by the simulator
itself.
mesh diag.flip width=$d_mesa
x.mesh location=0 s=0.5
x.mesh location=$d_mesa s=0.5
x.mesh location=$d_device s=0.5
# Ohmic1
y.mesh l=0.000 s=0.005
y.mesh l=$I s=0.01
y.mesh l=$A s=0.01
y.mesh l=$B s=0.005
y.mesh l=$C s=0.005
y.mesh l=$D s=0.005
y.mesh l=$E s=0.01
y.mesh l=$F s=0.01
y.mesh l=$G s=0.01

#-----------------------------------
# Regions definition
#-----------------------------------
region num=1 name=contact1 material=Gold y.min=0 y.max=$I
region num=2 name=ohmic1 material=InGaAs x.comp=0.47 y.min=$I
y.max=$A
region num=3 name=emitter material=InGaAs x.comp=0.47 y.min=$A
y.max=$B
```

```
region num=4 name=spacer1 material=InGaAs x.comp=0.47 y.min=$B
y.max=$C
region num=5 name=barrier material=AlAs y.min=$C y.max=$D
x.min=0 x.max=$d_mesa calc.strain qtregion=1
region num=6 name=spacer2 material=InGaAs x.comp=0.47 y.min=$D
y.max=$E
region num=7 name=collector material=InGaAs x.comp=0.47
y.min=$E y.max=$F
region num=8 name=ohmic2 material=InGaAs x.comp=0.47 y.min=$F
y.max=$G
region num=10 name=etch material=Air y.min=0 y.max=$F+$t_etch
x.min=$d_mesa x.max=$d_device
#--------------------------------
# Electrodes
#--------------------------------
electrode num=1 name=anode x.min=0 x.max=$d_mesa y.min=0
y.max=0 material=Gold
electrode num=2 name=cathode x.min=$d_mesa+$d_gap
x.max=$d_device y.min=$F+$t_etch y.max=$F+$t_etch
material=Gold
#--------------------------------

# Doping
#--------------------------------
doping uniform n.type conc=$d_ohmic1 Region=2
doping uniform n.type conc=$d_emitter Region=3
doping uniform n.type conc=$d_collector Region=7
doping uniform n.type conc=$d_ohmic2 Region=8
#--------------------------
#Interface
#--------------------------
interface s.s thermionic
interface s.i y.min=$C y.max=$C
interface s.i y.min=$D y.max=$D


#--------------------------
#Contacts
#--------------------------
contact name=cathode
contact name=anode
#----------------------------------------
# Material Definitions

#----------------------------------------
## The physical parameters for the materials are defined in the
following sub-sections

#AlAs
```

```
material material=AlAs eg300=2.83 affinity=3.15 mc=0.12

#In0.53Ga0.47As
material material=InGaAs eg300=0.74 affinity=4.5
#-----------------------------------------
#Traps and defects
#-----------------------------------------
inttrap acceptor structure=top midgap density=3e10 degen.fac=1
sign=1e-17 sigp=1e-17

#-----------------------------------------
#    INITIAL BAND DIAGRAM
#-----------------------------------------

output t.quantum band.param qfn qfp val.band con.band charge
polar.charge flowlines
solve init
save outf=XMBE326_INITIAL.str
#tonyplot XMBE326_INITIAL.str
#-----------------------------------------
# Models
#-----------------------------------------
models sis.el sis.ho sis.nlderivs qtregion=1
models srh fermi
method newton carr=2

#-----------------------------------------
#DC ANALYSIS
#-----------------------------------------
log outf=XMBE326_BIASED.log
solve init
solve vanode=-2 name=anode vstep=0.1 vfinal=2

save outf=XMBE326_BIASED.str
log off
#tonyplot XMBE326_BIASED.str
tonyplot XMBE326_BIASED.log


quit
```

Appendix C-Example Silvaco Code for QW-ASPAT simulation

```
GO ATLAS
##-------------------------------------------------------
```

```
# Simulation of GaAs/AlAs/In0.18Ga0.82As QW-ASPAT
# Mesa area: Scalable
# Models: SIS, Fermi
# Simulation Type: DC
# Emitter/collector Doping 1e17cm-3
# Ohmic layer doping 4e18 cm-3
#-----------------------------------------------------------
#    Device Epilayer Structure thicknesses in 'um'
#-----------------------------------------------------------
## Thicknesses
set t_contact1=0
set t_ohmic1=0.3
set t_emitter=0.035
set t_spacer1=0.005
set t_well=0.00
set t_barrier=0.00283
set t_spacer2=0.2
set t_collector=0.04
set t_ohmic2=0.45
set t_etch=0
set t_contact2=0
## Doping concentrations
set d_ohmic1=4e18
set d_emitter=1e17
set d_collector=1e17
set d_ohmic2=4e18
set d_gap=1.5
set d_mesa=4
set d_device=20
## Layers

set I=$t_contact1
set A=$I+$t_ohmic1
set B=$A+$t_emitter
set C=$B+$t_spacer1
set D=$C+$t_well
set E=$D+$t_barrier
set F=$E+$t_spacer2
set G=$F+$t_collector
set H=$G+$t_ohmic2
#-------------------------------------
# Mesh generator
#-------------------------------------
## The x.mesh and y.mesh specifies the location 'loc' of mesh
grid lines along the respective
## axis. 'spacing' determines the mesh spacing in microns at
the position specified by 'loc'
```

```
## parameter. The mesh spacing from one mesh statement to the
next is gradually changed and is managed by the simulator
itself.
mesh diag.flip width=4
x.mesh location=0 s=0.5
x.mesh location=$d_mesa s=0.5
x.mesh location=$d_device s=0.5
# Ohmic1
y.mesh l=0.000 s=0.01
y.mesh l=$I s=0.1
y.mesh l=$A s=0.01
y.mesh l=$B s=0.01
y.mesh l=$C s=0.001
y.mesh l=$D s=0.001
y.mesh l=$E s=0.001
y.mesh l=$F s=0.001
y.mesh l=$G s=0.1
y.mesh l=$H s=0.1

#----------------------------------
# Regions definition
#----------------------------------
region num=1 name=contact1 material=Gold y.min=0 y.max=$I
region num=2 name=ohmic1   material=GaAs y.min=$I y.max=$A
region num=3 name=emitter  material=GaAs y.min=$A y.max=$B
region num=4 name=spacer1  material=GaAs y.min=$B y.max=$C
region num=5 name=well           material=InGaAs      y.min=$C
y.max=$D x.comp=0.82  calc.strain qtregion=1
region num=6 name=barrier  material=AlAs   y.min=$D   y.max=$E
calc.strain qtregion=1
region num=7 name=spacer2  material=GaAs y.min=$E y.max=$F
region num=8 name=collectormaterial=GaAs y.min=$F y.max=$G
region num=9 name=ohmic2   material=GaAs y.min=$G y.max=$H
region num=10 name=etch material=Air y.min=0 y.max=$G+$t_etch
x.min=$d_mesa x.max=$d_device
#---------------------------------
# Electrodes
#---------------------------------
electrode  num=1  name=anode  x.min=0  x.max=$d_mesa  y.min=0
y.max=0 material=Gold
electrode     num=2     name=cathode     x.min=$d_mesa+$d_gap
x.max=$d_device       y.min=$G+$t_etch       y.max=$G+$t_etch
material=Gold
#---------------------------------

# Doping
#---------------------------------
doping uniform n.type conc=$d_ohmic1 Region=2
doping uniform n.type conc=$d_emitter Region=3
```

```
doping uniform n.type conc=$d_collector Region=8
doping uniform n.type conc=$d_ohmic2 Region=9
#-------------------------
#Interface
#-------------------------
interface s.s thermionic
interface s.i y.min=$D y.max=$D
interface s.i y.min=$E y.max=$E


#-------------------------
#Contacts
#-------------------------
contact name=cathode
contact name=anode
#----------------------------------------
# Material Definitions
#----------------------------------------
## The physical parameters for the materials are defined in the
following sub-sections
#AlAs
material material=AlAs eg300=2.77 affinity=3.15 mc=0.13

#GaAs
material material=GaAs

#In0.18Ga0.82As
material material=InGaAs  eg300=1.16  affinity=4.22

#----------------------------------------
#Traps and defects
#----------------------------------------

#inttrap   acceptor   structure=top   midgap   density=0.7e11
degen.fac=1 sign=1e-17 sigp=1e-17

#----------------------------------------
########INITIAL BAND DIAGRAM ####
#----------------------------------------

output t.quantum band.param qfn qfp val.band con.band charge
polar.charge flowlines
solve init
save outf=WELL_ASPAT_INITIAL.str
#tonyplot WELL_ASPAT_INITIAL.str
#----------------------------------------
# Models
#----------------------------------------
models sis.el sis.ho sis.nlderivs qtregion=1
```

```
models srh fermi
method newton carr=1

#----------------------------------------
#DC ANALYSIS
#----------------------------------------


log outf=WELL_ASPAT_BIASED.log
solve init
solve vanode=-2 name=anode vstep=0.01 vfinal=2

save outf=WELL_ASPAT_BIASED.str
log off
#tonyplot WELL_ASPAT_BIASED.str
tonyplot WELL_ASPAT_BIASED.log
quit
```

Appendix D-Example Silvaco Code of AlGaAs-QW-ASPAT

```
GO ATLAS
#-----------------------------------------------------------
# Simulation of AlGaAs/AlAs/In0.18Ga0.82As QW-ASPAT
# Mesa area: Scalable
# Models: SIS, Fermi
# Simulation Type: DC
# # Emitter/collector Doping 4e17cm-3
# Ohmic layer doping 4e18 cm-3
#-----------------------------------------------------------
# Device Epilayer Structure thicknesses in 'um'
#-----------------------------------------------------------
## Thicknesses
set t_contact1=0
set t_ohmic1=0.35
set t_emitter=0.005
set t_spacer1=0.005
set t_well=0.002
set t_barrier=0.0025
set t_spacer2=0.2
set t_collector=0.005
set t_ohmic2=0.35
set t_etch=0
set t_contact2=0
## Doping concentrations
set d_ohmic1=4e18
```

```
set d_emitter=4e17
set d_collector=4e17
set d_ohmic2=4e18
set d_gap=1.5
set d_mesa=4
set d_device=20
## Layers

set I=$t_contact1
set A=$I+$t_ohmic1
set B=$A+$t_emitter
set C=$B+$t_spacer1
set D=$C+$t_well
set E=$D+$t_barrier
set F=$E+$t_spacer2
set G=$F+$t_collector
set H=$G+$t_ohmic2
#-----------------------------------
# Mesh generator
#-----------------------------------
## The x.mesh and y.mesh specifies the location 'loc' of mesh
grid lines along the respective
## axis. 'spacing' determines the mesh spacing in microns at
the position specified by 'loc'
## parameter. The mesh spacing from one mesh statement to the
next is gradually changed and is managed by the simulator
itself.
mesh diag.flip width=4
x.mesh location=0 s=0.5
x.mesh location=$d_mesa s=0.5
x.mesh location=$d_device s=0.5
# Ohmic1
y.mesh l=0.000 s=0.01
y.mesh l=$I s=0.1
y.mesh l=$A s=0.01
y.mesh l=$B s=0.01
y.mesh l=$C s=0.001
y.mesh l=$D s=0.001
y.mesh l=$E s=0.001
y.mesh l=$F s=0.01
y.mesh l=$G s=0.1
y.mesh l=$H s=0.1
#-----------------------------------
# SECTION 2: Structure Specification
#-----------------------------------
#-----------------------------------
#    Regions definition
#-----------------------------------
region num=1 name=contact1 material=Gold y.min=0 y.max=$I
```

```
region num=2 name=ohmic1   material=GaAs y.min=$I y.max=$A
region num=3 name=emitter  material=GaAs y.min=$A y.max=$B
region num=4 name=spacer1  material=GaAs y.min=$B y.max=$C
region num=5 name=well          material=InGaAs      y.min=$C
y.max=$D x.comp=0.82  calc.strain qtregion=1
region num=6 name=barrier  material=AlAs   y.min=$D   y.max=$E
calc.strain qtregion=1
region num=7 name=spacer2  material=AlGaAs  y.min=$E  y.max=$F
x.comp=0.15
region num=8 name=collector material=GaAs y.min=$F y.max=$G
region num=9 name=ohmic2   material=GaAs y.min=$G y.max=$H
region num=10 name=etch material=Air y.min=0 y.max=$G+$t_etch
x.min=$d_mesa x.max=$d_device
#--------------------------------
#    Electrodes
#--------------------------------
electrode  num=1  name=anode  x.min=0  x.max=$d_mesa  y.min=0
y.max=0 material=Gold
electrode     num=2     name=cathode     x.min=$d_mesa+$d_gap
x.max=$d_device       y.min=$G+$t_etch       y.max=$G+$t_etch
material=Gold
#--------------------------------

#    Doping
#--------------------------------
doping uniform n.type conc=$d_ohmic1 Region=2
doping uniform n.type conc=$d_emitter Region=3
doping uniform n.type conc=$d_collector Region=8
doping uniform n.type conc=$d_ohmic2 Region=9
#--------------------------
#    Interface
#--------------------------
interface s.s thermionic
interface s.i y.min=$D y.max=$D
interface s.i y.min=$E y.max=$E


#--------------------------
#    Contacts
#--------------------------
contact name=cathode
contact name=anode
#----------------------------------------
#    Materials
#----------------------------------------
## The physical parameters for the materials are defined in the
following setions

#AlAs
```

```
material material=AlAs eg300=2.77 affinity=3.15 mc=0.13

#GaAs
material material=GaAs

#InGaAs
material material=InGaAs  eg300=1.16  affinity=4.22

#AlGaAs
#paramter equations to use        eg300=1.4242+1.155x+0.37x^2
affinity=4.07-1.1x
#material material=AlGaAs       eg300=1.66 affinity=3.905

#Traps and defects
#inttrap   acceptor   structure=top   midgap   density=0.6e11
degen.fac=1 sign=1e-17 sigp=1e-17

-----------------------------------------
#    INITIAL BAND DIAGRAM
-----------------------------------------
output t.quantum band.param qfn qfp val.band con.band charge
solve init
save outf=WELL_ASPAT_INITIAL.str
#tonyplot WELL_ASPAT_INITIAL.str
#-----------------------------------------
#    Models
#-----------------------------------------
models sis.el sis.ho sis.nlderivs qtregion=1
models srh fermi
method newton carr=2

#-----------------------------------------
#    DC ANALYSIS
#-----------------------------------------
log outf=WELL_ASPAT_Biased.log
solve init
solve vanode=-0.1 vstep=0.01 vfinal=0.1 electrode=anode

log off

#tonyplot WELL_ASPAT_BIASED.str
tonyplot WELL_ASPAT_BIASED.log
quit
```

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