João Mário Fernandes Gomes

Licenciatura em Engenharia Electrotécnica e Computadores

Development of a Step Down DC-DC Converter for Power Grid Energy Harvesting

Dissertação para obtenção do Grau de Mestre em

Engenharia Electrotécnica e de Computadores

Orientador: Nuno Filipe Silva Veríssimo Paulino, Professor Associado com Agregação,
Universidade Nova de Lisboa

Júri

Presidente: Professor Luís Bernardo
Arguente: Professor Carlos Carvalho

FACULDADE DE CIÊNCIAS E TECNOLOGIA
UNIVERSIDADE NOVA DE LISBOA

2021-12-04

Step Down DC-DC Converter for Power Grid Energy Harvesting

Este documento foi gerado utilizando o processador (pdf)LaTeX, com base no template "novathesis" [1] desenvolvido no Dep. Informática da FCT-NOVA [2].
[1] https://github.com/joaomlourenco/novathesis [2] http://www.di.fct.unl.pt

I want to dedicate this work to both my grandparents who unfortunately departed before the conclusion of this endeavour.

Acknowledgements

I would like first of all to express my gratitude and admiration to my adviser Professor Nuno Paulino, for all his coaching, patience and technical insight provided along this journey. I would also like to thank my parents Fátima and Manuel Gomes and my grandmother Julia Fernandes who have devoted some many hours to supporting and motivating me through these 6 years without them I would have never been able to complete such an enterprise. Furthermore, I would like to thank to my girlfriend Madalena Cilinio, for all the dedication and icentive she gave me. Last but not least, I would like to thank my friends for all their encouragement.

Abstract

This work contains an analysis of multiple topologies of DC-DC voltage buck converters. The main goal of this Thesis is to study and design a functioning Step Down converter for capacitive coupling devices used for energy harvesting from the power AC grid.

In order to achieve this goal, multiple topologies and circuits of this type of converter are studied and analysed, so that the requirements for the intended application are met. Since the input is obtained from the AC power grid and the output is connected to a supercapacitor, this results in a large input voltage (over 150V) and a low output voltage (between 1V to 3V), therefore the converter requires a step down voltage conversion ratio of around 130.

The DC-DC converter should also have a large input impedance (around 50Mohm) to maximize the energy transferred from the power grid. This mode of operation is not common for regular inductance based DC-DC converters, making this a challenging problem.

Moreover, since the amount of energy available from the capacitive coupling is very small, it is also necessary to develop a controller circuit that is capable of created a clock with a very low duty cycle while dissipating less than 50uW.

Keywords: DC-DC, Step-Down, Buck, Magnetic Coupling, Energy Harvesting, Internet of Things.

Resumo

Este trabalho visa analisar várias tipologias de conversores de tensão DC-DC denominados conversores Buck. O principal objectivo desta Tese é estudar e projectar um conversor DC-DC abaixador de tensão para sistemas de acopelamento electromagnético capacitivo utilizada em aplicações de *Energy Harvesting* a partir da rede AC.

De forma a cumprir este objectivo, várias tipologias são estudadas ao longo deste trabalho, de forma a cumprir as especificações exigidas. Uma vez que o sinal de entrada é obtido a partir da rede AC, e que o output está ligado a um supercondensador, isto faz com que a tensão de entrada seja elevado (Acima dos 150V) e a tensão de saída seja baixa (entre 1V e 3V), como tal o conversor precisa de um rácio de abaixamento bastante elevado de cerca de 130 vezes.

O conversor DC-DC deve também ter uma impedância de entrada elevada (cerca de 50MOhm) por forma a maximizar a energia transferida da rede de energia. Estas condições de funcionamento não são habituais para conversores DC-DC indutivos, o que torna este um problema muito desafiante.

Adicionalmente, uma vez que a energia disponivel devido ao acopelamento capacitivo é muito reduzida, é necessário desenvolver um circuito controlador capaz gerar um sinal de relógio com um duty cycle reduzido enquanto dissipa menos de 50uW de potência.

Palavras-chave: Conversor DC-DC redutor, Energy Harvesting, Indústria 4.0, Conversor DC-DC abaixador de tensão

Contents

List of Figures

List of Tables

Listings

Acronyms

AC	Alternate Current
AoI	Age of Information
CCM	Continuos Conduction Mode
CMOS	complementary metal-oxide-semiconductor
DCM	Discontinuos Condition Mode
EH	Energy Harvesting
ELMH	Electromagnetic Harvester
IC	Integrated Circuits
IoT	Internet of Things
LDO	Low Dropout Regulator
M2M	Machine to Machine Communication
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Track/Tracking
OTA	Operational Transconductance Amplifiers
PMS	Power Management System
PMU	Power Management Unit
PWM	Power Width Modulation
QSW	Quasi Square Wave
RFID	Radio Frequency Identification
SoC	System on Chip

TBJ Bipolar Junction Transisotr
TEG Thermoelectric Generator

VCO Voltage Controlled Oscillator

ZVD Zero-Voltage-Detector

Symbols

Chapter 1

Introduction

1.1 The Future of the Industry

In the past, most energy related systems would work based on AC current, therefore most of the power electronic and energy harvesting systems were directly supplied by AC converters[14]. However, in the present there is a growing need to use energy harvesting systems for DC current such as photovoltaic systems, and various appliances,[14] [48], plus the fact that DC power supply systems, do not suffer from energy wastage due to reactive power, thus being more efficient. In the future these devices will be even more important, with the 4.0 industry where multiple appliances will have the capability to interact and connect with each other, given that such appliances and devices mostly work with small power and small ammounts of DC current. In the case of industry 4.0, there is the need to apply a new concept called The Internet of Things.

This upcoming industry will require one key element called interconnectivity [40], in order for this interconnectivity to be possible there is the need to spread a large ammount of sensors and small parcels of actuators and transceivers that are able to interact with each other and communicate with one another in a orderly fashion and in real time applications for the most part.

Figure 1.1: Airbus Assembly Line in Hamburg

The figure above was taken from the following web site on October 18 2020.
https://werksfuehrung.de/en/english/group-offers/airbus-hamburg/

As can be seen by the image shown in 1.1, which depicts an example in this case in the aeronautics industry of a plant which would need sensors and actuators spread all over the plant to effectively communicate and have the plant it self take over the production and work with minimum human supervision. In order to do this there would be the need to supply all of those small sensors and actuators with small amounts of energy, as previously mentioned in most cases, with DC current and at regular intervals [11].

In order to do this the obvious and traditional solution would be to provide each sensor, actuator or device with its own set of energy transfer equipment such as an electrical plug, a transformer to convert AC into DC current and possibly any other equipment needed such as energy converters or cooling equipment and voltage regulators, since these devices operate at very low voltage when compared to grid voltages. Plus this solution would imply a large amount of voltage plugs spread around the factory, as well as large extensions of copper cable, which in a plant such as the one shown in the picture could be tens or even hundreds of kilometres, which is very expensive, heavy and occupies a lot of space.

To summarize this traditional solution would be very complicated due to the fact that all the equipment needed to provide energy to the devices would be very expensive, bulky and inefficient, specially when compared with the amount of energy and power transferred towards these devices, with an additional problem which would be the fact that this implementation would reduce the mobility of the factory equipment, because

each machine or assembly line would need a fixed number of sensors and actuators, which need its own support grid in order to have sufficient power and be able to operate properly. Thus, if the need to change such an assembly line or move a piece of equipment to another site of the facility, a new and different set of infrastructure would have to be made and planned in order for the sensors and actuators to keep working.

1.2 Addressing of the Energy Supply Problem

Ergo, the problem that this work tries to solve, picking up on the previous work of [8], is to develop a system that can transfer energy from the power grid to those devices without the usage of traditional methods. This will be done through electromagnetic coupling, meaning the extraction of electrial energy that is available from the magnetic and electric fields of electrical wiring on the walls of a building. The device in [8] can obtain energy from the wiring through capacitive coupling although it lacks the means to regulate the voltage applied to the devices.

In order to do that, since most of the sensors and devices work with low power DC voltages, a Buck converter, like the one shown in Figure 1.2, will be an extremely important device because it can lower the high voltage resulting from the capacitive coupling device in [8] to the lower voltages that these devices would normally use. Since these converters will be responsible for reducing the high voltage on the input side to a lower voltage on the output, while elevating the current from the input to the output. Ideally the value of the power delivered to the output should be close to the value of the power obtained from the input.

So, as previously mentioned, these devices are very important, because they will allow supercapacitors and batteries to be charged, allowing the hand shake between relatively high voltage capacitive coupling devices or other[36] and the battery or sensor to be fed directly by the converter. Therefore the main purpose of this work will be to develop a buck converter that is able to convert the relatively high voltage of the coupling device to a more usable voltage by the sensors and other equipment of the same nature and also to study and develop a controller unit that is able to operate such a converter in the desired operating point.

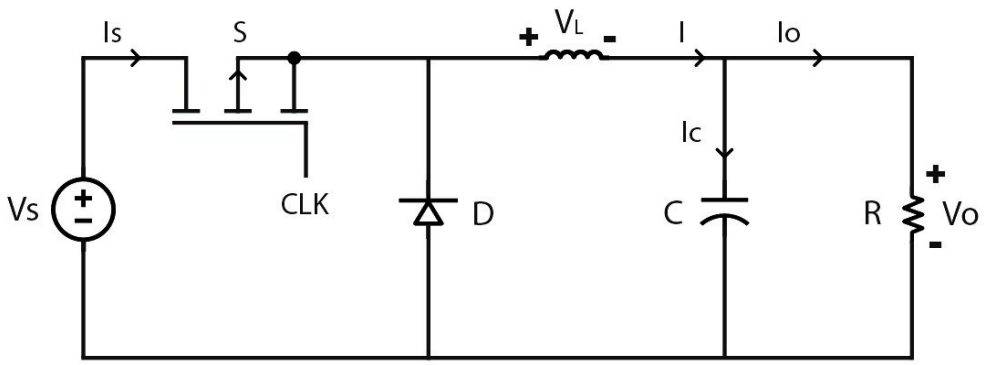

Figure 1.2: Schematic of a Generic Buck Converter

This circuit produces a lower output voltage due to the voltage drop caused by the impedance of the inductor. Since this impedance (ideally) is reactive, the voltage drop is achieved without energy loss, as would be the case if a resistor was used. When connected to the input voltage through transistor S, the inductor absorbs energy to its magnetic field causing a voltage drop. When the transistor opens, the inductor voltage increases, causing the diode to turn on so that the inductor current can continue to flow to the output, releasing the stored energy from the inductor's magnetic field. By controlling the duty cycle of the controlling CLK signal it is possible to define the ratio between the input and output voltages. The output capacitor provides an energy reservoir that reduces the output voltage ripple.

The two operation modes of the traditional Buck Converter are shown in Figure 1.3

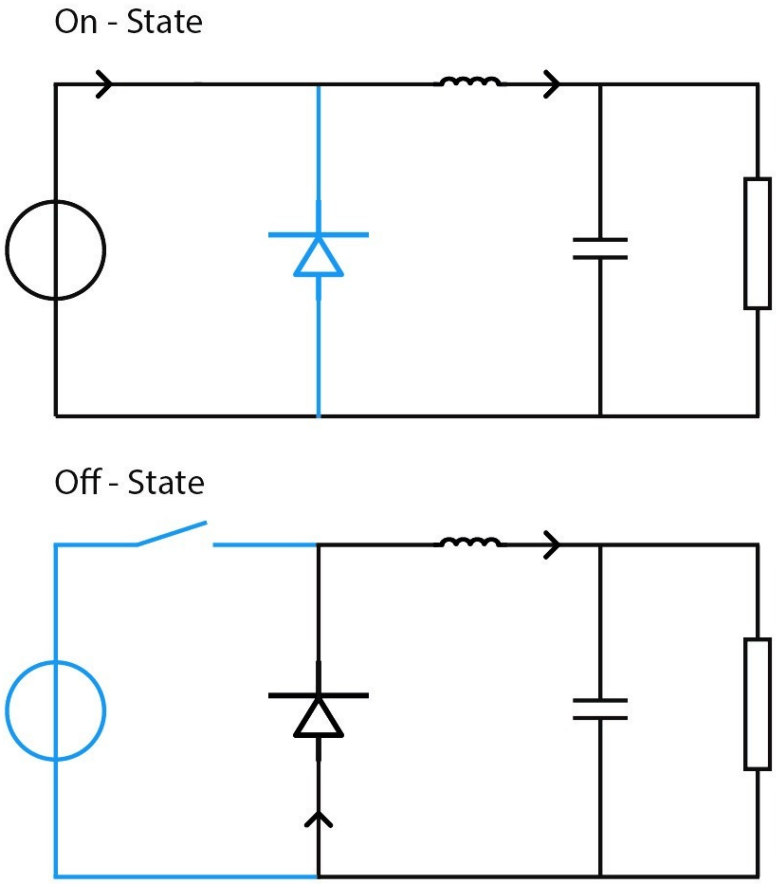

Figure 1.3: A Generic Buck Converter in operation

1.3 Thesis Organization

The work in this Thesis was carried out as follows, first there was some research done in order to better understand the concepts of Energy Harvesting and what to expect from such a system. Both these analysis were presented on Chapter 2 as the state of the art for this work. Also a research was made on different types of converters and how they operate, as well as the strong and weak points, the advantages and disadvantages of each one of them.

On Chapter 3, which is the main chapter of this work, based on the characteristics of such converters and their modes of operation as well as their different technical characteristics and implementation characteristics they were sorted out. Some topologies were ruled out due to the fact that they were inadequate, as explained and justified further on, while some others were selected for further studies and analysis. At the end of this section one topology, the one that showed more promising results and ease to manufacture was

selected and a second stage of calculations and studies was conducted, such as, how it behaves in both Discontinuos Condition Mode (DCM) and Continuos Conduction Mode (CCM) and wich mode of operation would best suit the purpose of this work. At the end of this section, a fully functioning converter with adjusted duty cycles and its components properly dimensioned was presented.

Chapter 4, presents the final steps of experimental work required, such as the studies conducted and made on the controller for this circuit as well as the experimental results and findings, that arose from the physical implementation and testing of the circuit at hand.

On Chapter 5, the final results and calculations are presented, as well as a possible implementation of a PCB prototype.

At last Chapter 6 presents both the technical conclusions that could be taken from this work as well as future works that could be done in the field in order to improve and further on develop this device and this architecture. As well as a brief economical study on how viable this device would be in order to actually put it into use on the industry for Industry 4.0 and how this financial aspect could be improved by future works in this field.

Chapter 2

State of the Art

In this chapter, it will be explained how an energy harvesting system works and how it can transfer energy from a source onto a load, which can be an energy storing device or a load directly. It will also explain the objective of this thesis and an explanation of the problem which it will try to solve.

2.1 Internet of Things

The Internet of Things (IoT) is an industry concept that, as we know it today, was first introduced in 1999, although the concept of a smart network of devices had been first recorded in 1982, when it was placed at Carnegie Mellon University a vending machine which could tell how many products inside it had been sold, how many were still there and list their temperatures. With this little experiment a new chapter in evolution started one which will culminate with a fully integrated network of devices as will be explained next. This is a simple concept which states that machines can communicate with each other transmitting data and information without the need for human intervention, called Machine to Machine Communication (M2M), therefore giving them a larger amount of autonomy and capacity to automate certain aspects of industrial operation. A formal definition of the concept has been given as: *"a dynamic global network infrastructure with self- configuring capabilities based on standard and inter-operable communication protocols where physical and virtual 'Things' have identities, physical attributes, and virtual personalities and use intelligent interfaces, and are seamlessly integrated into the information network."*[50]. This concept was first applied to Radio Frequency Identification (RFID). Later on, it started to be applied to a number of different devices, such as GPS receivers, and even actuators, which based on an input of a sensor, could operate on their own without the need for human interaction or acknowledgment[50]. This is due to the fact that nowadays

many more appliances in the industry have internet connectivity and because of that, to fully explore their capabilities, there is the need to use that connectivity. Therefore these devices have the need to communicate an increasing volume of information over increasingly longer distances and; in order to do that, they make a trade off between baud rate, battery life and installation cost[49]. So, among the many challenges that this concept poses, one of the most important, is efficient energy supply systems.

Given the fact that IoT applications need to meet multiple requirements of latency tolerance, mobility, and reliability[11], we can perceive that the internet of things will revolutionize the industry in the next few years, much like the steam engine did in the eighteenth century; a concept called industry 4.0. This concept states that in the next few years, many sectors of the market will be able to work autonomously or with very little human supervision, such as manufacturing, transportation, asset tracking, security, infrastructure monitoring[49]. However from here on, in this thesis, all these sectors, will be simply called the industry. Therefore we can see that, in order to do that it is absolutely indispensable that machines are able to communicate with each other and send information to each other throughout low power devices such as sensors or transceivers over Low Power Wide Area Networks known as LPWA or LPWAN. This will de-centralize the industry and allow for machines and assembly lines from different plants to be interconnected to each other[40] or the decentralization of medical services, which can boost the free flow of medical information and diagnosis to provide for a less standardised and more patient centred medical service[49]. Both of the previous situations given here as an example of what to expect from the industry 4.0 and the internet of things. In figure 2.1 we can see the chronological evolution of the industry and the developments that made those leaps possible

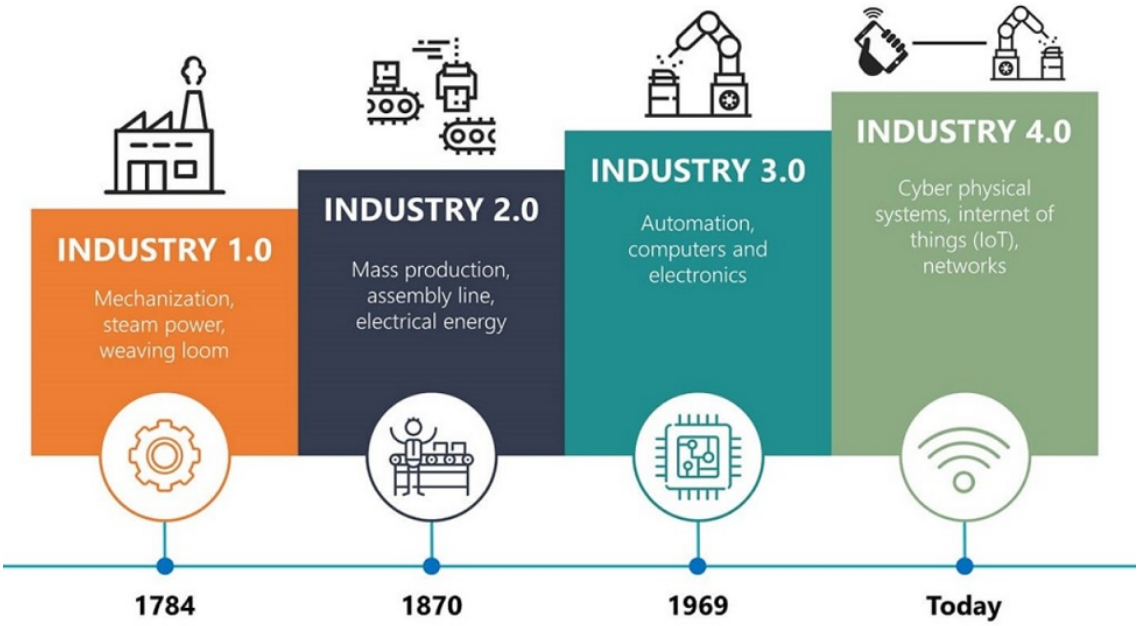

Figure 2.1: Industry evolution timeline over the centuries

The above figure was taken from the following website on January 3, 2020.

http://www.isitan.com/en/technology-industry-40-ready.html

All of that comes with the need to provide energy to all of these devices and sensors, spread throughout a factory or any building that employs this kind of technology.

This begs the question of how to provide energy to all of these devices that are part of such a network, keeping in mind that these devices, apart from actuators or heavy machinery, are for the most part sensors and small transceiver devices, which are scattered over the entire plant, and do not need a large amount of energy to operate.

The first and simplest solution, is to provide a large battery to the devices; a battery that would autonomously support them over a certain amount of time and when it is drained out, it would be replaced by a charged one. To optimize this solution, there are certain techniques which can maximize the battery endurance, for instance the Age of Information (AoI), which states that certain systems will only transmit information pertinent to the whole system using criteria based on how old that information is, how long it will take it to reach the appliance it has to reach and the level of priority it has[20]. Based on this implementation certain information might not be transmitted, for the sake of energetic efficiency.

Another problem with the battery system is that devices would have to stay dorment for some time in order to save energy, and this would pose some problems because when they come online, they might have a very short period of time to decide which information to relay or not based on the criteria previously seen in AoI.

The second and most obvious way of providing energy to these devices without the

concern of information relaying would be to plug them into the electric grid, this is also the most expensive and inefficient solution, because it would require a lot of extra electric wires to supply electric plugs and, on the devices themselves, it would require step down transformers for most of them or at least some sort of Power Management Unit (PMU), based on a power transformation and processing unit, to make the handshake between the low voltage sensor for instance and the relatively high voltage present on the electric grid. The problem is that this unit would have to be bulky, heavy and thus expensive, to provide the appropriate energy to the devices; this multiplied by all the sensors needed would become extremely expensive and impractical.

This leaves us with the third solution which is the one that this thesis will try to implement because it is much more efficient, practical, cheaper and energy efficient.

This third solution is based on energy harvesting and collecting energy from the electromagnetic field generated around electric power wiring. This way, there is a possibility to have each sensor and device fitted with its own power unit that could harvest energy from a close wire in the electric grid without adding plugs or more wiring to the installation, because the only thing needed would be for the device to be close to a wall where electric wires were passing through so as to be under the influence of their electric field, and therefore harvest part of the energy contained in that field. These devices would also have their own means of storing that energy, in small batteries or supercapacitors, so as to have that energy available at any time[49]. It is thought that due to the small dimensions of the devices even with their own energy storing built-in capability, they will be smaller and slenderer than the traditional solution. This would be the optimum solution because it could accommodate a small battery which takes up less physical room than solution number one, it wouldn't take all the equipment needed in solution two and using some sort of energy managing algorithms like the one described in solution one, fine adjustments could be made, trading off device online time for battery capacity and thus size, and vice-versa, according to the level of importance of the sensor or system in order to make it more energy efficient.

In the next section will be exploited the concepts and techniques associated with energy harvesting.

2.2 Energy Harvesting

Energy Harvesting (EH), is a technique of gathering energy for small applications which captures energy from external sources like light, solar energy, thermal energy or in this case, energy trapped in the magnetic or electric fields, of power wires and stores a certain amount of it in small batteries or capacitors for it to be used later on by sensor networks or other small electronic devices. The great advantage of using EH techniques instead of traditional energy sources is that despite producing very small amounts of energy, the one they convert is available as background in many places like walls where electric wiring is located or ambient light provided by artificial lighting both indoors or outdoors.

For the harvesting process to be possible there is the need to make a voltage and impedance conversion between the energy supply, in this case, the electromagnetic field and the load, in this case a supercapacitor. In order to make this conversion, there is the need to develop a PMU, which will be placed between the energy harvesting component of the device and the load for maximum efficiency[39]. This unit will comprise a PMU core and a PMU starter circuit[8]. The main goal of this thesis is to develop a PMU, more specifically the kernel of the PMU core which will be a DC-DC Buck Converter analysed further ahead.

2.2.1 Energy Harvesting from Electromagnetic Fields

An electromagnetic field is a composition of two sinusoidal waves which oscillate between a given maximum value, making a right angle between them, and a right angle with the direction to which they travel. The magnetic field represented by $\vec{H}$ and the electric field by $\vec{E}$; a graphic representation of the two fields can be seen in figure 2.2.

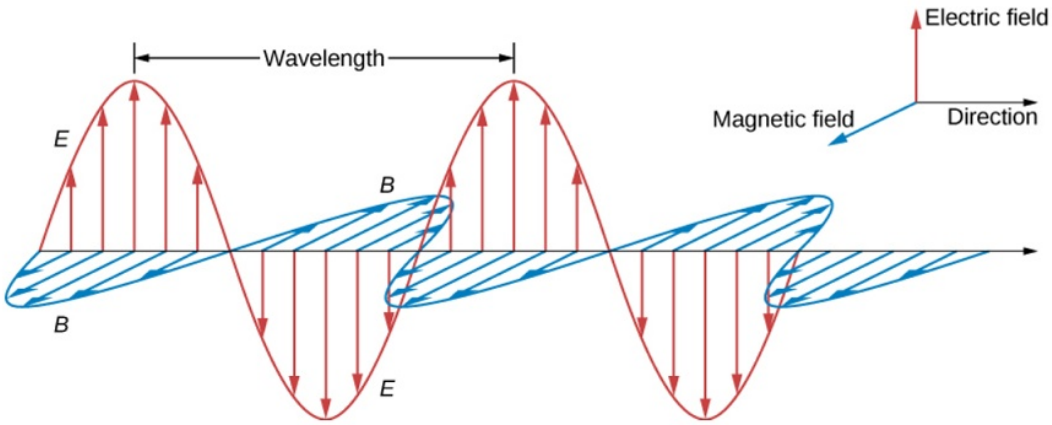

Figure 2.2: Graphic representation of the electromagnetic field

The above figure was taken from the following website on January 8, 2020.
https://openstax.org/books/university-physics-volume-2/pages/16-2-plane-electromagnetic

The energy in the magnetic and electric field can be harvested by the use of a coil or a capacitor respectively. The energy present in a coil is given by the expression:

$$W_{mag} = \frac{1}{2} \cdot L \cdot i^2 \tag{2.1}$$

With i being the current to which the coil was subjected to and L its inductance. The energy present in a capacitor is given by the expression:

$$W_{elec} = \frac{1}{2} \cdot C \cdot u^2 \tag{2.2}$$

With C being the capacitor capacitance and the u the electric voltage that its plates are subjected to. From the expressions of indutance and capacitance we can write:

$$L = \mu_r \cdot \mu_0 \cdot N^2 \cdot \frac{A_l}{l_l} \tag{2.3}$$

$$C = \epsilon_r \cdot \epsilon_0 \cdot \frac{A_c}{d} \tag{2.4}$$

So by replacing L and C in 2.1 and 2.2 by their respective value obtained by the expressions in 2.3 and 2.4 and then dividing 2.1 by 2.2 as done in the work of[8] we can conclude the magnetic field is 10^5 times more powerful than the electric field, which at first glance, would make the magnetic field a much more attractive prospect for EH than the electric one. This is not exactly the case because the magnetic field is only present when a current is present in the wire, while the electric field is always present as long as there is an electric potential difference between the two extremities of the wire. Therefore and specially in Low power EH applications, neither options can be disregarded.

2.2.2 General architecture of an Energy Harvesting System

In figure 2.3, we can see a Generic Energy Harvesting system and all of its components based on the work of[1] and[8]. As we can see in this figure, there are two main components of the PMU, which are the PMU core and the Start Up circuit.

The function of the startup circuit is to allow the harvesting circuit to start autonomously Since the image shown represents a Thermoelectric Generator (TEG), the starting voltages are very low and therefore, during the starting process, the circuit is prone to being unstable. The starting circuit enables a transition phase to occur in order for the output voltage to be more stable. A more detailed analysis of this circuit is presented in[1]. In the case of this thesis, since this is a ELMH and not a TEG, the voltage available at start is much higher, which means that there is not a need for a starter circuit in our implementation, The only issue that can occur is at the start when the output supercapacitor is discharged, meaning its voltage is 0V. This means that at start-up the DC-DC converter has to be capable of operating correctly with a short at its output, due to the large value of the supercapacitor[41].

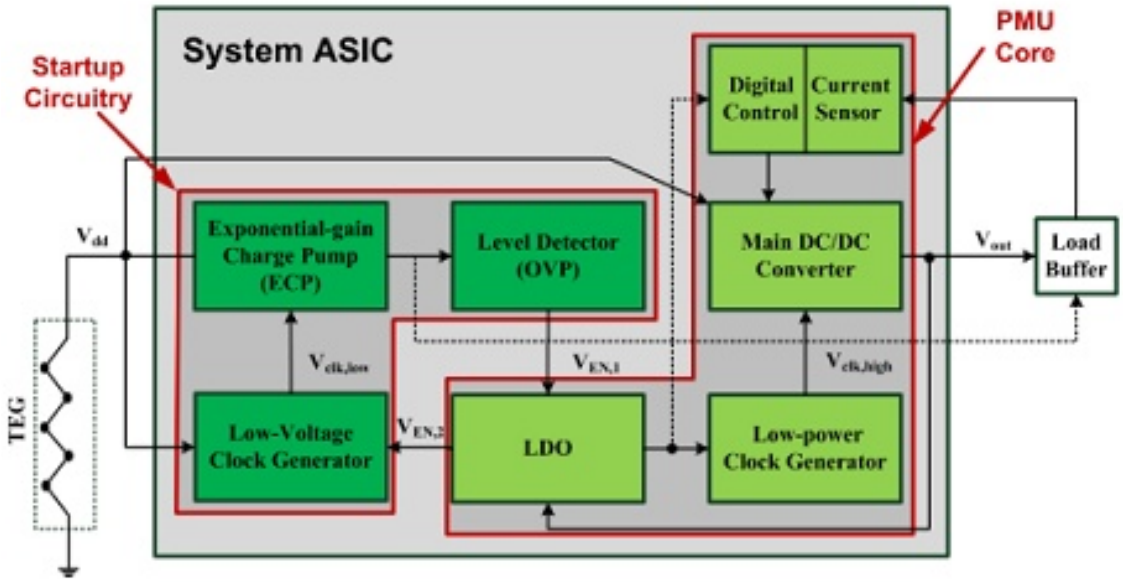

Figure 2.3: Generic architecture of the Energy harvesting system taken from [1]

The PMU core is used to actually deliver electric power to the load. It does so by storing the output voltage provided by a DC-DC converter in the Load-Buffer which in turn is controlled by a two-phase low power clock generator[1], The Low Dropout Regulator (LDO) is used ir order to disengage the starter circuit and engage the PMU core. The voltage level and Maximum Power Point Track/Tracking (MPPT) algorithm receives an input from the load buffer and keeps the power delivered at its maximum[1],[8]. Although this work is based on this architecture it cannot be equal because as previously said this is based on a very low voltage source while the ELMH is meant to harvest energy from the electric grid. So while this device main DC-DC converter was based on the Dickinson pump[8],[1],[7], which is a step-up also known as a boost DC-DC converter, the need here is for a buck or a step-down DC-DC converter which will be developed along this work.

As far as it is presently understood, the general architecture for this work would be as follows:

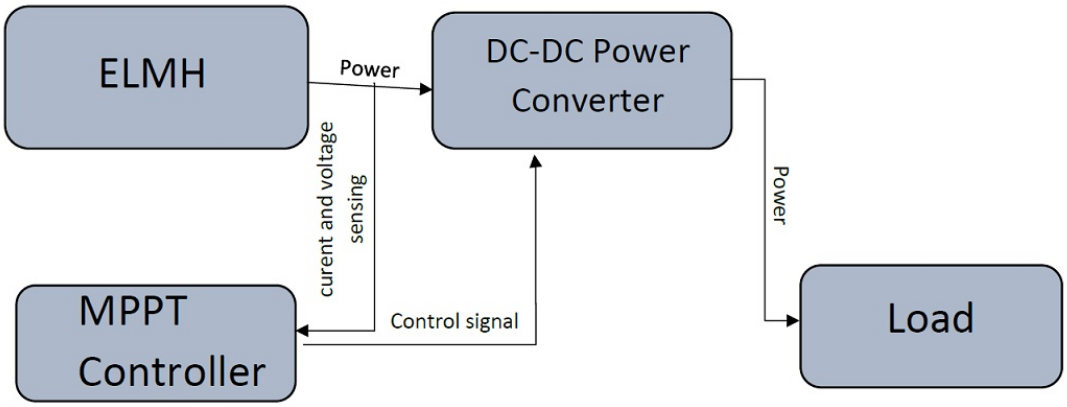

Figure 2.4: Generic architecture of the system developed in this work.

As we can see on the image above, there is an ELMH which has enough power to provide the start-up of the system without the need for a starting circuit, followed by the DC-DC converter module, which will be the main goal of this work. Additionally it will be implemented a digital control logic module with the purpose of keeping the MPPT, and at last the load which will be a supercapacitor in order to store energy to be provided to the sensor or other device to be supplied.

2.2.3 Generalizations and Considerations Regarding Power and Efficiency of the ELMH

Although the focus of this work will be to develop a Buck Converter using discrete analog components, it is important to analyse examples of power converters built using complementary metal-oxide-semiconductor (CMOS) technology, therefore the power dissipation of the whole circuit as well as the power dissipation on the Converter can be attributed to three main factors[46]:

- Static Dissipation
- Internal Power
- Switching Power

In a CMOS circuit, static dissipation depends on the parameters of the technology used and would be a constant[46].

The internal power dissipation of the circuit corresponds to the amount of power used by the components in the converter in order to operate correctly, such as the power needed to operate the various switches. In the rest of the architecture this power would be the one used to operate the Digital Control Unit for instance, as well as all the other components both in the PMU core and in the startup circuit.

The switching power is the power required to turn ON and OFF the switches in the converter. These switches are implemented using MOS transistors or diodes, and they have parasitic capacitances, that are charged to either the clock voltage and discharged or to an internal voltage and discharged. This creates a power dissipation that is proportional to the clock frequency. So in order to keep this parameter as low as possible, there should be a concern firstly in keeping these parameters variable and controllable from the Digital Control Unit, and secondly keeping them as low as possible.

Some of these concerns and factors that might affect directly or indirectly the value of the parameters described will be discussed in future sections of this work, such as the next one regarding MPPT capabilities and algorithms. These factors should be taken into consideration when developing the converter and during future work.

The dynamic power consumption of MPPT controller circuit when all of the above parameters are taken into consideration can be mathematically described as:

$$P_{dynamic} = \alpha \cdot C \cdot f_c \cdot V_{DD}^2 \tag{2.5}$$

In which α is the switching probability, C is the parasitic capacitance associated to the circuits nodes, V_{DD} is the supplied voltage and f_c is the operating frequency[46].

The previous equation would be valid for the entire circuit including the controller, the converter and any peripheral devices that would be attached to them. This represents the power loss of the system which affects the efficiency. This is a very important parameter since this type of system harvests a very modest quantity of power. Therefore, they are only feasible as long as the efficiency η given as P_{out} over P_{in}, with P_{in} the input power and P_{out} the output or useful power, is very high. Which is to say that the parameter $P_{dynamic}$ must be as small as possible.

2.2.4 Maximum Power Point Tracking

In order to harvest energy there is also the necessity to develop MPPT capabilities so that maximum efficiency is attained, given that these devices work with very small amounts of energy and there is not a lot of it available.

There are two categories of MPPT algorithms, direct and indirect algorithms [47]. Direct algorithms are based on the "perturb and observe"method which introduces a perturbation in the system and observes how the output varies, making adjustments accordingly. The indirect approach, consists of crossing data from the consumption data with the power curve of the energy available and throughtout different algorithms, predict how the energy necessity will evolve over time. Solutions of the two groups are presented below.

From the MPPT theorem [8], [39] we can determine that the device impedance has to be complex conjugate of that from the Load in order to attain maximum efficiency. Thus, the internal impedance of the supplying circuit should be variable in order to keep the

Maximum Power Point. This can be achieved by a variety of methods and the DC-DC converter can facilitate this process[39].

Other concerns are the amount of space available and the type of device that is going to be supplied. Besides these, parameters of the following list should be taken into account when programming a MPPT algorithm into the PMU core, more precisely in the Digital Control inside the PMU. Such regards are[18]:

- Environmental energy model: Predictable behaviour of the environmental conditions at which the device will operate.
- Energy Storage Type: The type of energy storing, if any, that will be used, if it is a Lithium Ion Battery or a supercapacitor.
- Ratio of Energy Storage Capacity to Energy Harvested: The amount of energy that can be stored in relation to the energy harvested. This parameter is directly related with the efficiency of the system.
- Time Granularity: The frequency at which the device is going to be operated, and the regularity of that operation. Being it every few mili seconds to a few days.
- Problem Size: The physical space available in order to build and place the whole energy harvesting device.

Several algorithms and practices have been explored to take better advantage as well as better manage the amount of energy across these types of systems. Most of these are based on the principle of dynamic power management[38]. This principle states that certain system components might be turned off when they remain in idle for an extended period of time, this will in turn alter the characteristics of the circuit which can be used to regulate the MPPT of the circuit in order to keep it at its best efficiency. Other techniques might include limiting the amount of current which flows across the device or altering its output voltage. In order to do so, the PMS, should comprise the following components, Power Manager(PM), Spr(Service provider), Queue buffer, and service requester(SR) based on [38], as we can see in 2.5.

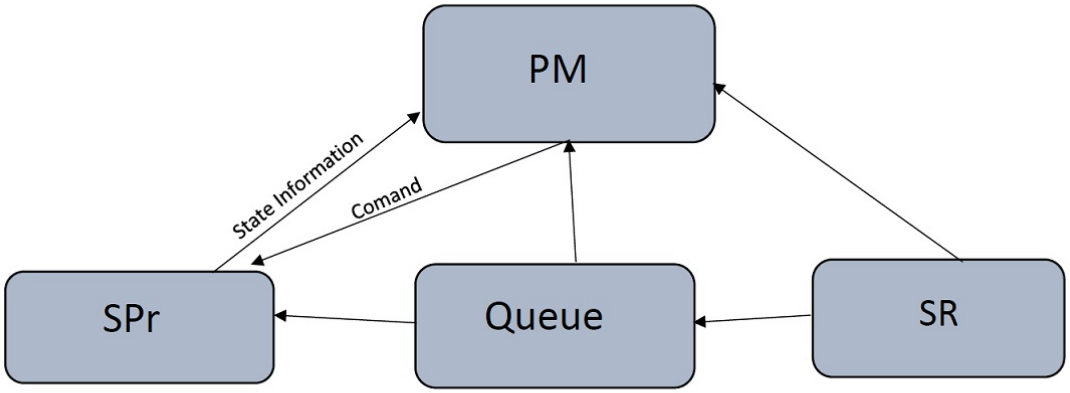

Figure 2.5: Architecture of a possible PMS after [8] and [38]

Some of the algorithms that could be implemented by the architecture in figure 2.5 are for instance the Time Fair Rate Assignment and the Progressive Filling both explored in[18], these algorithms are based on the premise that the energy must have a somehow deterministic behavior, which allows these algoritms to predict future needs of energy, and that the physical components are based on the model free approach which results in them having variable duty cycles and variable clock timers[18]. The disadvantage of these techniques is that they require very complex mathematical models previous to the implementation. They are difficult to implement when compared with the following techniques and although they should be projected with some tolerance they are always conditioned by the predicted behavior of the system. Other such techniques are the time-out technique which waits for a predetermined amount of time and shuts down components that have been idle for that amount. This is a much simplistic behaviour which requires much simple logic in the processor[38]. The disadvantage of this method is that it has a very high latency problem, because while waiting the predetermined amount of time for the PM to shut down the components, they are wasting power. Other approaches might include Continous-time Markov Decision Process, this technique instead of waiting a predetermined amount of time to shut down a component, it uses an asynchronous trigger based on events happening on the device in order to engage or disengage different modules. This technique is presented in the work [38], as well as variations of it that can be more efficient depending on the circumstances. This technique might drastically reduce the operating cycles inside the device which greatly reduces the internal power dissipated.

Another technique that can be taken into account is the Clock-gating technique which consists of placing digital logic components between the clock entry of the various digital components of the circuit[46], which in terms allows for the operation of these components at different passing and eliminates unnecessary clock cycles in order to reduce

power dissipation.

At last another technique of MPPT that might make sense in this system is the *Energy-Aware program*, based on the work of [39]. In this approach, the battery has a selfmonitoring device enabling it to control its own level of charge. When the latter gets below a certain threshold, it sends a message towards the main device which will wake up and start charging the battery once again. This approach has a disadvantage, because it requires a careful monitoring of the battery level and spends a small amount of energy while doing it, this amount that can be quantified by [39]:

$$I_{ave} = \frac{\sum_{n=1}^{k} I_w(t_n)\dot{\delta}t}{T_{sleep}} \tag{2.6}$$

Where I_{ave} is the average current that the module consumes during its sleeping operations, $I_w(t_n)$ is the instantaneous sleeping curent of the battery monitoring module, δt is the sampling time interval and the T_{sleep} is the total sleeping time.

Based on 2.6 we can infer that for relatively small intervals of time, the energy spent will be very small and so, this might be a more economical solution power wise. But in the case of longer waiting periods, meaning larger batteries, this might not be an interesting approach because the average current will be larger and thus results in a lot more wasted power. Therefore this might be a very interesting solution for medical applications for instance, which involve very small amounts of energy and need to operate almost continuously, making the sleeping time very small, but these are not very well suited for the industry.

In conclusion of this section it is important to mention that regardless of the application, for energy harvesting in general, it is necessary to choose an MPPT algorithm that minimizes MPPT overhead even at the expense of some loss of accuracy on the optimum operating point. This is due to the fact that Energy harvesting devices generate very limited power and the nodes fed by the energy harvesters also consume very low power, so there is the need to choose an MPPT solution that also consumes very low power and does not overload the harvester, even at the expense of not being able to operate at exactly the optimum MPP.

2.2.5 Energy Storing Devices and Energy Storing Processes

For this work two different options of storing energy were considered, supercapacitors and Lithium-Ion Batteries.

The batteries have some disadvantages over supercapacitors such as the fact that they do not endure as a large amount of cycles as the capacitors and typically require a complicated charging scheme where the current, voltage and temperature have to be carefully monitored and adjusted.

Moreover, most batteries have complicated charging procedures, where it is necessary to adjust the charging current in function o the battery voltage and temperature, which

requires a complex circuit to control the charging procedure.

Therefore supercapacitors were chosen over Lithium-ion batteries due to the fact that a supercapacitor has a much larger number of charging and discharging cycles than a battery, according to [41]. A supercapacitor can charge and discharge half a million times until its total capacity drops to around 80% of its original capacity. They have a longer life span, of around 10 to 20 years longer than batteries, given that it takes them 10 years for its capacity to reach 80% and 20 to reach 50% [41]. They have a larger current density that can be derived from them[47]. The capacitors have relatively low leakage currents, in the order of nano-amperes, which allows them to keep fully charged for longer periods of time [41]. At last, they are charged at the same voltage regardless of their voltage during the charging process, they are simpler to charge and therefore better suited for low power energy harvesting applications.

2.3 Analysis of DC-DC Step Down Converters Their Usage and Applications in the Industry

In this section, an introduction to DC-DC Step Down converters, also known as Buck converters, will be presented as well as the advantages and drawbacks of the various implementations and architectures. This section, as previously mentioned regards the most important part of this thesis, given that the main goal of this work is to develop a Buck converter that has a specific amount of characteristics and fulfils the requirements to be used in an ELMH as previously described.

The DC-DC converter, generically speaking, is a device of power electronics and power management that receives a direct current input at a designated voltage and converts into a either higher or lower output voltage. In this case, the Buck or Step Down converter turns the input voltage into a lower output voltage. An ideal converter has the same output and input power, thus if the output voltage is lower than the input voltage, the output current will be larger than the input current, therefore in an ideal Buck $V_{out} = DV_{in}$ where V_{out} is the output voltage, D is the duty cycle and V_{in} is the input voltage. The simplest topology of a Buck converter is as follows:

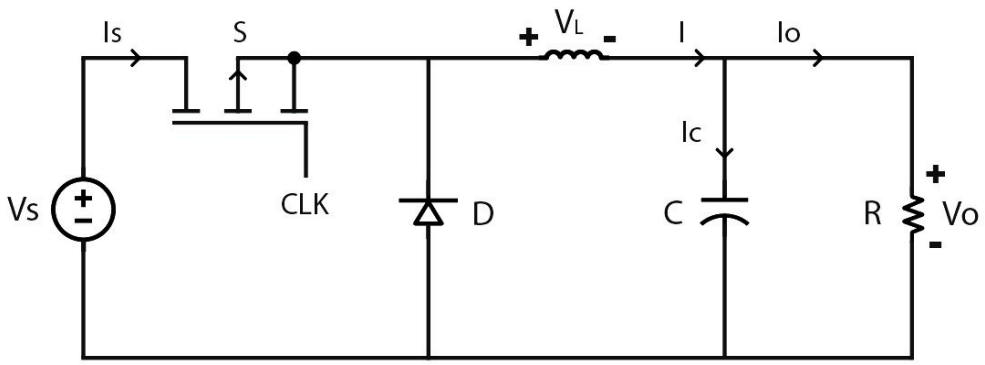

Figure 2.6: Simple and generic buck converter

2.3.1 General Considerations About the Buck Converters

The Buck converter is a very simple circuit consisting of an inductor and two switches. One switch is implemented by the transistor S (controlled by the clock signal) and the other by the diode D. The circuit operation is as follows: -When the clock signal is high, transistor S turns on allowing current to flow from the input voltage source into the inductor and into the load. This current is limited by the inductor because it is absorbing energy into its magnetic field. The current decreases as the inductor charges. This causes a voltage drop across the inductor resulting in an output voltage that is lower than the input voltage. As the switch remains closed both the current and the output voltage increase. -When the clock signal is low, transistor M1 turns off, stopping the flow of current from the input voltage. Since the current in the inductor cannot change instantly, its voltage will change abruptly, making the voltage of the node at the terminals of the coil capacitor and load negative, thus turning on diode D and allowing the current to continue to flow through the inductor and the load. The current decreases as the magnetic field of the inductor discharges.

The output capacitor reduces the output voltage variation (ripple) by absorbing energy from the inductor and releasing energy to the load. By adjusting the time duration of the ON and OFF phases it is possible to adjust the value of the output voltage [44].

DC-DC Stepdown converters can be grouped into two categories, these are the Isolated Converters and the Non-Isolated Converters[31].

The Isolated Converters are not referenced to Earth, so they have the advantage of having an output current which is more easily controlled using a Transformer for instance, and they can more easily achieve a very high step down conversion ratio. Although they have the disadvantage of being less generalist, as it is more difficult to make them adapt to any given value of a load or a battery, they occupy more physical space due to the presence of a transformer, they are more expensive and tend to waste energy due to the fact that the transformer core heats with usage[34]. The Non-Isolated Converters have the advantage of having a large power density, being more easily adaptable to a given output load and also work with very high efficiency, however it is more complicated to

achieve a very high step-down ratio using this type of converter[34]. Consequently, these converters are commonly used in low to medium power applications such as EH[31]. Although especially for EH as is the case, there is the need to have a very high step down ratio, this might become a drawback because although these converters have very good efficiency, cascading multiple modules reduces the performance, so among others one of the challenges of this work is to develop a module as efficient as possible so that the converter can be made of a single module or as little modules as possible.

2.3.1.1 Considerations to Be Taken During the Dimensioning Phase

During the sizing of these devices the following results, expressions and values to attribute to the components in order for the converters to be as efficient as possible and to work properly should be taken into consideration. These expressions have a certain degree of tolerance but an effort should be made to choose values as close to these as possible in order to achieve maximum operating capabilities [4].

$$D = \frac{V_0}{V_s} \tag{2.7}$$

$$L_{min} = \frac{(1-D)\cdot R}{2\cdot f} \tag{2.8}$$

$$L = 1.25 \cdot L_{min} \tag{2.9}$$

$$I_L = \frac{V_0}{R} \tag{2.10}$$

$$I_{max} = I_L + \frac{\Delta \cdot i_L}{2} \tag{2.11}$$

$$Imin = I_L - \frac{\Delta \cdot i_L}{2} \tag{2.12}$$

$$C = \frac{1-D}{8L\cdot(\frac{\Delta \cdot V_O}{V_O})\cdot f^2} \tag{2.13}$$

Based on 2.7, this means that the duty cycle can be expressed as the ratio between the output and input voltages. Expression 2.8 gives the minimum inductance of a coil placed in the circuit and to keep the circuit in the continuous mode. The minimum value of a coil in it should be at leat 25% greater than the value of L_{min} as expressed in 2.9. This is so that when the main switch of the circuit is open, the coils are large enough to keep feeding the load with the energy in their magnetic field. Expressions 2.10, 2.11, 2.12, give us an indication of the current flowing through the circuit as well as the ripple of that current which is an important measure because this ripple affects the efficiency of the device, and if the output voltage has very high peak values, although the average

value might be tolerable, the peak values might exceed the breakdown voltage of some components in the circuit.

The capacitor which acts as an energy storage to the load and low pass filter to reduce peak currents and harmonics, is given by 2.13, this capacitor shall always be able to absorb the peak voltage calculated by 2.11 and 2.12. Another consideration that should be taken into account is that diodes have a very large voltage drop and leakage currents, this can affect the efficiency of the converter, by lowering the output voltage, thus according to [4], Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) transistors can be used in diode configuration in order to reduce this phenomenon and increase the efficiency. In order to determine the specifications of the MOSFET to be used either as switches or as diodes should be taken into account the Body Diode Power Loss which can severely deteriorate the efficiency of the converter should be taken into account should also be taken into account the possible usage of Schottky diodes since these present less Power losses than normal diodes although they have the disadvantage of having more leakage currents. This power loss can be expressed by the following expression:

$$P_{Bodydiode} = V_{sdON} \cdot t_{BD} \cdot f_{sw} \cdot (I_{out} + 2I_{neg}) \tag{2.14}$$

$$I_{neg} = \frac{2Q_{sw}}{tQ_{sw}} \tag{2.15}$$

where $P_{Bodydiode}$ is the power loss through body diode effect, V_{sdON} is the voltage at which the transistor starts to conduct t_{BD} is the conduction time of the body diode, f_{sw} is the operating frequency of the device I_{out} is the current output of the device and I_{neg} is the negative value current given by 2.15 which is the negative current of the device which may happen in resonant operation and make current achieve a negative value.

As can be demonstrated by 2.14, the body diode loss depends on the voltage and specially the negative current, the frequency and the time might not be as important, because they work against each other because as faster the commutating frequency, the shorter the time the transistor is in the on state[34].

At last, in order to maximize the efficiency of the converter the total power loss should be kept to a minimum and this is achieved by minimizing the total power consumed by the converter, a very thorough analysis of loss and efficiency was made in [34] and will serve as support for the efficiency considerations of this work.

2.3.2 Specific Analysis of Different Converters

This section will present the analysis of some of the architectures of different converters which looked promising and that might serve as a starting point for the development of the one needed.

2.3.2.1 Isolated Converters

These types of devices have been recently used in ressonant converters, cascading two steps of the converter, the first one as an isolated converter in order to achieve a high step down ratio which is one of the biggest advantages of these devices, since they use a transformer to reduce their voltage[34] and the second stage is a closed loop with a coil and a capacitor, acting as a low pass filter, because in these devices, ripple currents are a problem specially if they are feeding a battery[31]. These devices are particularly used in high voltage and high power applications, so in this work the non-isolated ones might be more interesting than these due to the fact that there is a need to operate with low power settings achieve a very high efficiency and reduce the physical size of the devices, the only advantage of the isolated over the non-isolated is that they can more easily achieve a higher stepdown voltage than the latter.

2.3.2.2 Non-Isolated Converters

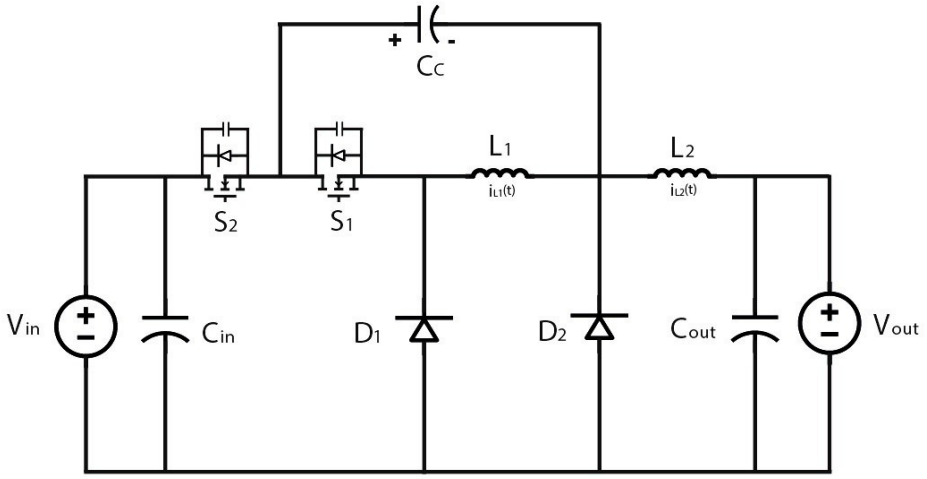

Figure 2.7: Non-Isolated Topology of [31].

One of the first converters to be analysed was the one developed during the work of[31] shown in 2.7. This converter falls into the category of the Non-Isolated Converters, as the author said, it works as a normal converter, thus the controller circuit would be the regular one used in any other kind of converter. This device has four operating modules which allows it to charge and discharge two different inductors, so that the load is constantly receiving energy. A a more detailed analysis can be found in [31]. Regarding the Steady State analysis of this converter, it can be said that it allows for a stepping down voltage of 2.25 which is far less than that needed for this work as summarized in table 2.1, also this converter operates with a power of 200W which is a lot more than the one which will be drawn from this ELMH.

Although this Converter has some drawbacks in regard to what it is intended in this

work, it has a crucial difference from other converters which is that for elevated step-down voltages the voltage stress to components can be very large so this device uses what the author called a Clamping capacitor known as C_c, which is mainly used to absorb that overvoltage and increase the components life span. This capacitor does not have any specific value as long as it is large enough to reduce the overvoltage to the desired setting[31]. In this case the author calculated that the C_c should be determined by:

$$C_c = \frac{i_c \dot{\delta} t}{\delta V_c} \tag{2.16}$$

Such as $i_c \delta t$ is the product between the current that flows though the node of the capacitor times the amount of time it does so. And δV_c is the variation of voltage to the capacitor plates in that interval; as long as C_c is kept over these values, to keep it from reaching its fully charge state, so as to keep absorbing electric charge that would otherwise stress the other components of the circuit. In this case the capacitor has to be larger than 2.5μ Farads.

The second converter to be analysed was also a Non-Isolated converter. This device can be operated both in CCM or DCM, this means that it can work with either a synchronous controller which keeps it at a continuous conduction state at regular intervals, or an asynchronous one which will keep operating with an irregular cadence[44]. Usually these types of converters are operated in CCM. Despite this type of operation is more stable and reliable, it is also less efficient since it causes large losses on switches [13]. These efficiency problems might be mitigated using resonant converters which are briefly discussed below. Largely, the behaviour of this device is achieved because this converter is based on the principle of using two identical coils, which in turn generate two loops, that feed the load constantly, both when the main switch of the converter is closed, and the load is fed from loop number one, and when it is opened in which case the load is fed from loop two[44], Therefore this device is very versatile and by altering its operating mode, both from the CCM to DCM and vice versa, large conversion ratios can be achieved. Although this is not entirely the conversion rate needed, it is still very high. The only issue with this converter is that it is used with a very high input voltage and current, thus power, and from what was presented in [44], this converter is not very well suited for smaller power applications, because its optimum efficiency is achieved with the values displayed in table 2.1, in [44] it is shown that when the load resistance is different then 50Ω or at higher frequencies, or lower power the efficiency plummets. Therefore this converter seems like a promising solution but it would require some further testing, either by reducing the inductance of the coils used or by making adjustments to the architecture in order to adjust it to the range of voltage and power to be used in this work.

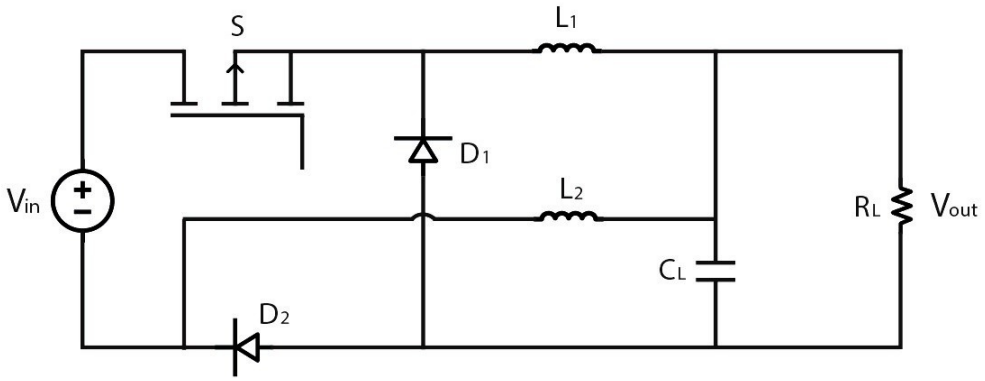

Figure 2.8: Non-Isolated Topology of [44].

Also taken into consideration was a Quasi Square Wave (QSW) shown in figure 2.9; this topology seems to be one of the most promising of these types of converters, since it presents one of the highest step-down voltage ratios as seen in 2.1. This converter is a resonant converter, with the inductor used having the function of both filter and energy storage device, for that reason it should be large enough to accommodate both roles simultaneously as stated in [34] by the following expression:

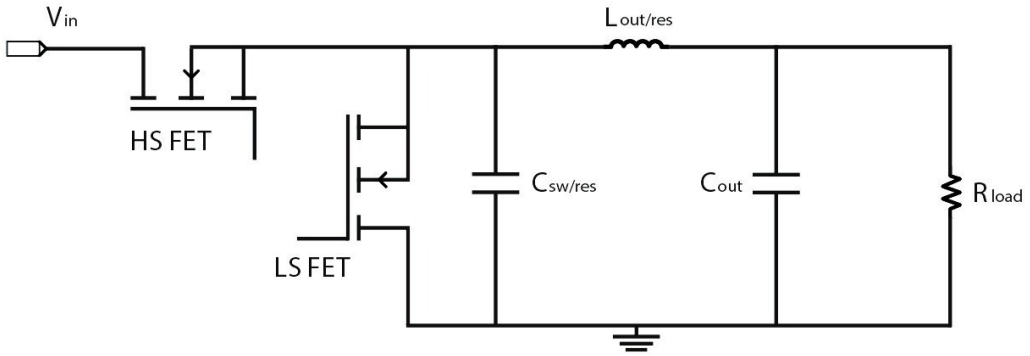

Figure 2.9: Non-Isolated Topology of [34].

$$L_{res} \cdot I_l^2 = C_{sw} \cdot V_{sw}^2 \tag{2.17}$$

Where L_{res} is the inductance of the coil that guarantees resonance, I_l is the current across the device, C_{sw} is connected to the switching node, the node where the main switch is connected to, capacitance and V_{sw} is the voltage across the switching node. Another possible implementation is a marginal resonant converter as presented in the work of [13]. This converter has a sophisticated control system inside it, which works by detecting the voltage across the free-wheel diode and when this voltage becomes equal to the input voltage it opens the input switch thus achieving for a brief period of time a resonant state. Despite the fact the control circuit and the general concept presented on this paper was very interesting, the experimental results of this converter were not presented because

this device has a step-down ratio of 1.4 and for this work as shown in table 2.1 there is the need for a step down ratio of 135.

In the work of [14] a group of multiple architectures of different converters as well as their characteristics, advantages and drawbacks can be found.

Two of the most simple of these complex implementations are the interleaved Buck converter and the quadratic buck converter. These two architectures are achieved by connecting in parallel simple converters and cascading them respectively. Because of this, the interleaved converter can enhance the power output, reduce the current ripple but it suffers a lot from voltage stress to its components [25] and the step-down voltage is not very large as seen in table 2.1, the quadratic Buck converter as said before works by cascading two or more conventional buck converters as the ones seen in figure 2.6, but with only one switch commanding all of them. This converter suffers from very high voltage stress but it theoretically achieves a higher conversion ratio than the interleaved, because its step down ratio is the product of the ratios of the conventional bucks in the architecture. In table2.1 we can see that they both have the same step down ratio, this might be due to the fact that the author of [14], has used regular diodes instead of using MOSFET transistors as diodes which have less current leaks and a faster commutating behaviour. In order to achieve the best performance from these two architectures there might be the need to use them together by interleaving two or more quadratic devices.

Another implementation studied in paper [14] was the Tapped-inductor Buck converter. This converter presents a split inductor that can be adjusted in order to present the optimum inductance to the circuit for the best efficiency possible, this topology is very useful for controlling the duty cycle of the converter more easily, and it reduces the conduction losses across the device; at the expense of a more complex controlling system and MPPT algorithm implementation, as discussed in section 2.2, and it has the disadvantage of keeping a very high voltage stress on the switches and diodes because with every slight fluctuation of the coil inductance value, there is an alteration of the flux across it, and very easily generate spike currents that exceed the circuit capacity [14]. An alternative to the previous architecture is the coupled inductors topology, in this case instead of a split coil, there are two conventional coils magnetically coupled to each other. This reduces the voltages stress across switches and other circuit components as well as current ripple although it does not reduce current ripple across the two coils themselves which translates in heating and power waste. This topology also has a very narrow duty cycle operation.

Another very interesting topology the switched inductor cells. In this case the converter coil is replaced by two coils in parallel of equal value, and two freewheeling diodes coupled to each one of the coils, so when the main switch is closed both coils are charging and connected in series, but when the switch opens, both coils discharge in parallel thus adding to the amount of current that can be supplied to the load for a smaller amount of time [3], thus it can be stated that this converter works in CCM. This results in the fact that these converters have a very high step down voltage and the expense of high ripple

and high voltage stress on components, the author [14] called these inductors L-switching cells, these converters are very good for low power applications [3]. There was also a brief study of Multilevel Buck converters, but although these have a lot in common with the previous one, they are better suited for high voltage applications as can be seen in the table below they were tested with 5000W [14].

Lastly there are the Buck converters with tristate cells. These reduce the peak currents and voltage stress on components, as well as an increase in the efficiency of the converter. This is part due to the fact that part of the energy is fed through a transformer unit. This tristate cell consists of two diodes, two transistors and two magnetically coupled inductors acting as transformers [14].

Based on the work of [25], a very interesting topology arose, the High step down single switch dc-dc converter. This device is primarily dimensioned to work in CCM, and consists of a quadratic buck cascaded with a diode based buck converter, with one single power switch across the entire device. This topology offers a very large step down ratio without the need for a very large duty cycle, which in terms mean a reduced voltage stress for a large duty cycle. This device works by charging a capacitor while the coils discharge to the load and then that capacitor charges the coils once they become discharged [25]. The experimental results can be seen on table 2.1.

So, to briefly summarize after the compilation and analysis of multiple papers where this type of device has been analysed, in different topologies and configurations, the most promising topologies are presented in table 2.1, and as seen below one of the most promising is the quasi-square wave buck converter and the L-switching devices, given that these are the ones which present the most step-down ratio and are also one of the most efficient at least for low power application such as this. Therefore, for further analysis, these might be a good starting point in this case, although there is the need to study the input impedance of these devices, because none of the papers studied had any value regarding this parameter, so for future analysis this should also be a concern.

At last one other topology that was looked into was the Cascaded Buck converter which is a derivative topology from the simple buck converter, it basically consists in cascading two or more of the regular buck converters to cite the work of [2], it can be concluded by the analysis of the previously mentioned document that voltage conversion ratio is determined by the combination of the duty cycle of both converters, this is very interesting, particularly in our case because it would allow us to divide such a large drop down voltage through multiple stages and thus reducing the specification of each one of the stages. In order to present a linear variation of the output voltage in regard to the duty cycle, in CCM mode these converters should not be operated at duty cycles below 20% nor higher than 80%. To this work, this might pose a problem, because even with two or more of these modules attached, the step down ratio required is very large. Thus, such a converter would have different modules operating at very low duty cycles, which accounts for some stranger behaviour and non-linearities in their operation according to [2].

Table 2.1: Table to compile the various converters studied.

List of Converter Parameters									
Topology and Article	Voltage Stress of Switches	Voltage Stress of Diodes	Ripple in Output Current	Power (W)	Efficiency	Vin (V)	Vout (V)	Step Down Ratio	Operating frequency
Desired Converter for this work	-	-	-	50m-100m	<90%	160	1.2	130	-
New High Step Down DC-DC Converter [31]	Vin-1 and (Vin-Vc)-2	Vin-1 and (Vin-Vc)-2	-	200	-	400	178	2.25	100KHz
A DC-DC Converter for unprecedent higher efficiency [44]	-	-	-	-	99.39%	1200	180	6.66(6)	8KHz
Quasi Square Wave Buck Converter [34]	-	-	-	-	95.7%	48	1.8	26.6(6)	1MHz
Interleaved Buck Converters with extended duty ratio [14]	Vin-1 Vin/2-2	Vin/2	$\frac{V_{in}D(1-2D)}{2LF_S}$	240	94%	200	40	5	100KHz
Quadratic Buck Converter [14]	$DV_{in}(1-D)$	$DV_{in} - 1$ D^2V_{in}	$\frac{V_{in}D^2(1-D)}{LF_S}$	9	93%	200	40	5	100KHz

Table 2.2: Table to compile the various converters studied (Continuation).

List of Converter Parameters (Continuation)									
Topology and Article	Voltage Stress of Switches	Voltage Stress of Diodes	Ripple in Output Current	Power (W)	Efficiency	Vin (V)	Vout (V)	Step Down Ratio	Operating frequency
Tapped Inductor with lossless clamp [14]	$\frac{nV_{in}}{D+n(1-D)}$	$\frac{V_{in}}{D+n(1-D)}$	$\frac{n^2V_{in}D(1-D)}{(D+n(1-D))LF_s}$	75	90%	200	40	5	100KHz
Buck Converter with switched inductor cells [14]	$\frac{2V_{in}}{2-D}$	$\frac{2V_{in}}{2-D}$	$\frac{V_{in}D(1-D)}{(2(2-D)LF_s}$	26	-	200	40	5	100KHz
Coupled inductor Buck Converter [14]	V_{in}	V_{in}	$\frac{V_{in}D(1-2D)}{L_kF_s}$	50	98%	200	40	5	100KHz
Buck converter with three state switching cell [14]	V_{in}	V_{in}	$\frac{V_{in}D(1-2D)}{2L_kF_s}$	1000	97%	200	40	5	100KHz
Multilevel Buck Convreter(5 level) [14]	$V_{in}/4$	$V_{in}/4$	$\frac{V_{in}D(1-4D)}{4L_kF_s}$	5000	-	200	40	5	100KHz
A new high step down single switch dc-dc converter [25]	-	-	-	100	-	200	10.5	19.5	10KHz
Switched-Inductor Semi-quadractic buck converter [3]	-	-	-	5	-	42	9	4.6(6)	100KHz

Chapter 3

Converter Selection Analysis and Dimensioning

In this section some of the work that has already been developed towards the implementation of the DC-DC converter and its integration into the ELMH will be presented.

3.1 Impedance study of the previously Analysed Topologies

As previously stated one of the main concerns about this work was to make a converter that was properly adapted to the energy system feeding it, given that the amount of energy available in these systems is very small, so the first step after selecting a converter was the analysis and optimization of the input impedance of the given converters on the state of the art.

Since no such analysis was made in any of the papers reviewed it was decided that before any further work could be done, at least a simple analysis of the input and output impedances of these devices should be made, in order to determine in accordance with the step-down ratio and their operating power namely which ones would be better suited for the task at hand and therefore provide a better starting point for this work.

Some topologies were discarded after a more exhaustive analysis because although they performed well as small step down converters they didn't do very well when a higher step down ratio and a lower power was involved. Some of such topologies were the resonant Buck converter. This type of converter is better suited for small step down ratios and large currents flowing through it as stated in [34].

The second topology of converters to be discarded were the square wave/quadratic converters, because after some experimentation and further research it was found that these type of converters are not very well suited for very high frequency due to the fact

that high frequency devices need a very fast commutation frequency [14] which degrades the performance of these converters and affects their efficiency.

At last the topologies that after a preliminary analysis were found to be promising for this work were the interleaved converter, the Tapped inductor/Magnetically coupled inductor, and the Cascaded Buck converter, further described and analysed in the next sections.

3.1.1 Analysis of the converters impedance

Due to the fact that we need a very high step down ratio, there is the need to make sure that the input impedance of this converter is high enough, larger than 50MΩ, and the output impedance is relatively low, smaller than 50Ω, in order to protect both the circuitry behind it as well as the supercapacitor that it will be feeding. Because the two latter mentioned work with very different voltage and current levels.

In order to analyse the Input impedance of the three topologies mentioned, first there was the need to determine the input voltage and the current flowing through them, both in the permanent regime, where the current and voltage had stabilized. In order to calculate these parameters the following expression was used:

$$Z_{in} = \frac{U_{in}}{\frac{\int_{t_0}^{t} I(t)dt}{T}} \tag{3.1}$$

Where the Z_{in} is the input impedance of the converter, U_{in} is the input voltage of the converter $I(t)$ is the current across the converter throughout the time considered, it should be at least one whole period, and T is the total time elapsed during the integration of the current.

This elevated input impedance is what will in fact ensure that the converter´s impedance is well adapted to the ELMH feeding it. So the concern should not only be about the output voltage and current but as well as the input voltage because according to the MPPT presented in the work of [8], at best will result in a 50% power transfer. How well the converter impedance is adapted to the ELMH is measured by the input voltage, which reflects how close together are the output impedance of the ELMH and the input impedance of the converter.

Later on a second approach was used in order to determine the input impedance of the converter and that was approaching the converter as a transformer[21], since the input voltage was limited to a maximum and the output voltage was also limited to a relatively small value that would be able to charge a supercapacitor some of the converters were looked and analysed by their conversion ratio, since the input impedance could also be expressed as:

$$Z_{in} = V_{cr}^2 R_L \tag{3.2}$$

Being V_{CR} the voltage conversion ratio from the entrance of the circuit to the exit, and R_L the impedance of the load. With this analysis in mind there are three parameters that can be constantly adjusted on order to get a satisfactory result, these being the Duty cycle of the converter, and the frequency of operation the latter one only becomes extremely relevant on the DCM mode. And the last one which is the maximum power available from the unit, which is highly condicioned by the load impedance attached to the converter [9].

3.1.2 Converter analysis

The first topology to be looked into was the one mentioned in [14], as the interleaved topology, which consists in connecting two regular buck converters in parallel. This topology did not produce such good results as the previous one, which would be expectable since it consists in a parallel connection, it presents the input voltage with a lower impedance, than the previous one, and the output voltage is larger than the 1.2V needed, stabilizing at around 2.8V.

This topology, might be an interesting one if the need to cascade multiple modules arises, because it doesn't lower the voltage to the exact value needed, which leaves some manoeuvering space to cascade another converter. The results obtained from simulation can be observed in the images below.

In figure 3.1, it can be observed the actual topology as the author in [14] proposes, as we can see it was tested with a very high commutation frequency, which is also not very good because the greater the frequency, the lesser the efficiency due to the fact that the increase in frequency causes a higher energy loss charging parasitic capacitances on the transistors gates.

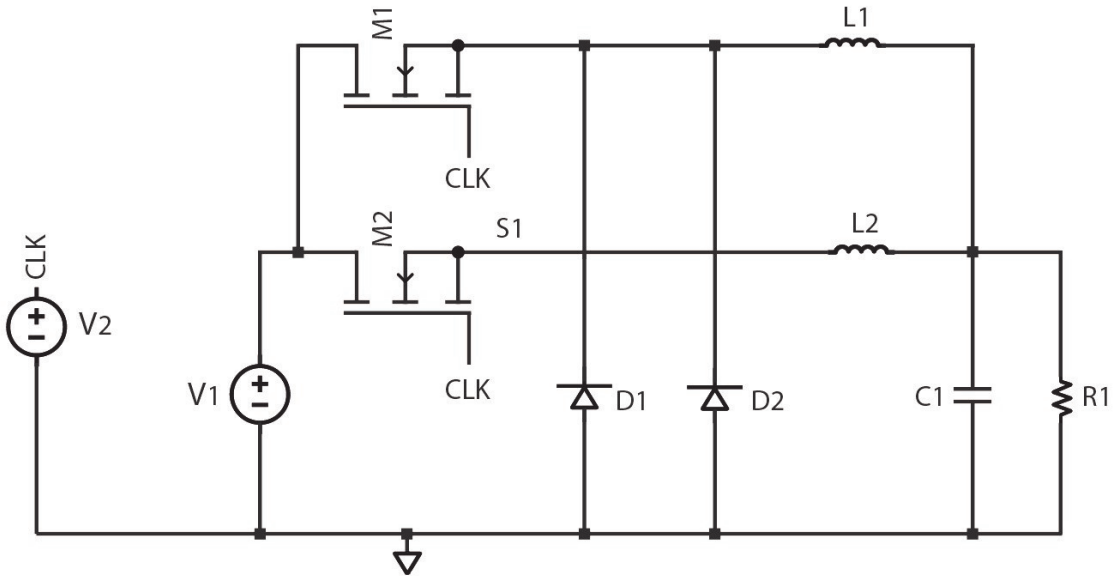

Figure 3.1: Schematic of an Interleaved Buck Converter

In figure 3.2 and 3.3 it can be seen both the output voltage and the output current across the load respectively. These results were obtained with a 100KHz commutation frequency as previously mentioned and a output resistance of 50Ω.

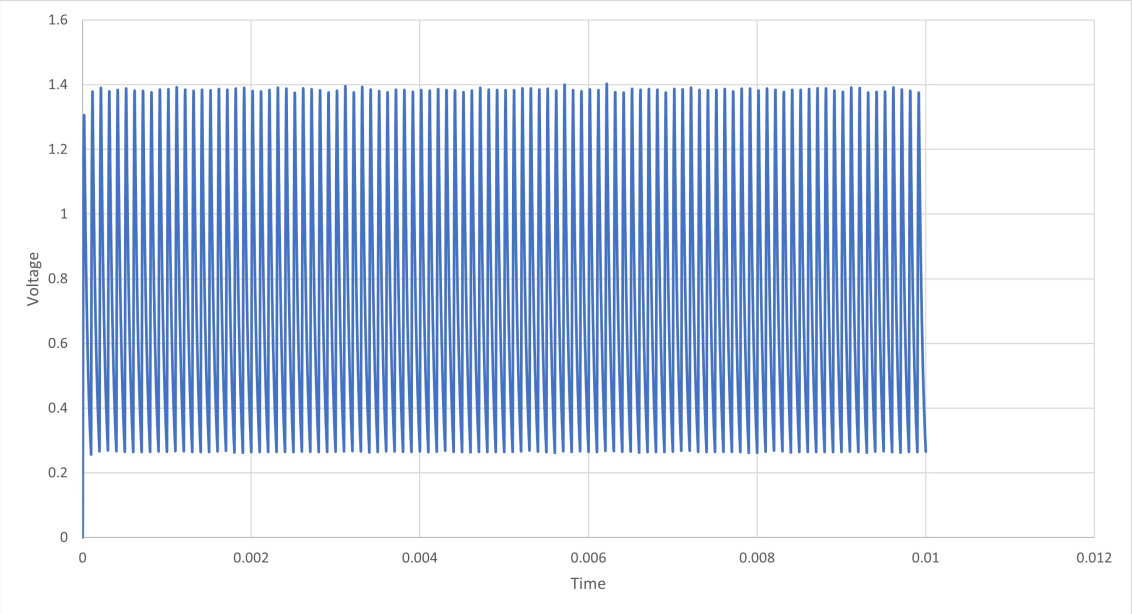

Figure 3.2: Simulation Results of the output voltage of this circuit.

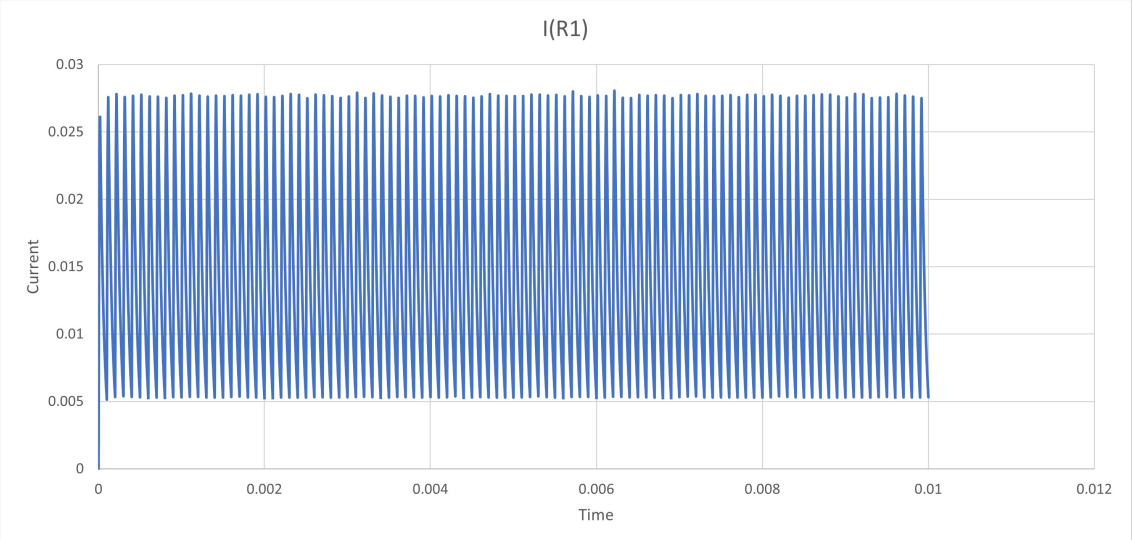

Figure 3.3: Simulation Results of the current in this circuit.

The total current obtained from the source in the permanent regime, is determined as follows:

$$V_{in} = V_{L1} + V_{out} \iff V_{L1} = V_{in} - V_{out} \iff L_1 \frac{dI_1}{dt} = V_{in} - V_{out} \iff$$
$$\iff I_1 = \int_0^{T_{on}} \frac{V_{in} - V_{out}}{L1} dt \iff I_1 = \frac{(V_{in} - V_{out})T_{on}}{L_1} \tag{3.3}$$

The same analysis is valid for the coil number two. Thus it can be concluded that the total current that is drawn from the source I_{tot} is given by:

$$I_{tot} = I_1 + I_2 \iff I_{tot} = (V_{in} - V_{out} T_{on}((\frac{1}{L_1}) + (\frac{1}{L_2}))) \tag{3.4}$$

$$Z_{in} = \frac{V_{in}}{(V_{in} - V_{out}) T_{on}((\frac{1}{L_1}) + (\frac{1}{L_2}))} \tag{3.5}$$

The graph depicted in Fig, 3.4 shows the input impedance as a function of the On period, of this topology.

The On time is defined by the duty cycle, in this case for a first analysis it was chosen 20% this was based on the work of [14] since the author of this paper had already conducted extensive analysis on many of the analysed topologies which made it easier to compare the simulation results done in this thesis between one another and with the work of the aforementioned author. As can be observed, this presents very small values of input impedance specially with lower frequencys. During the tests to plot this curve it was assumed a constant value for the two coils of the converter(300υH).

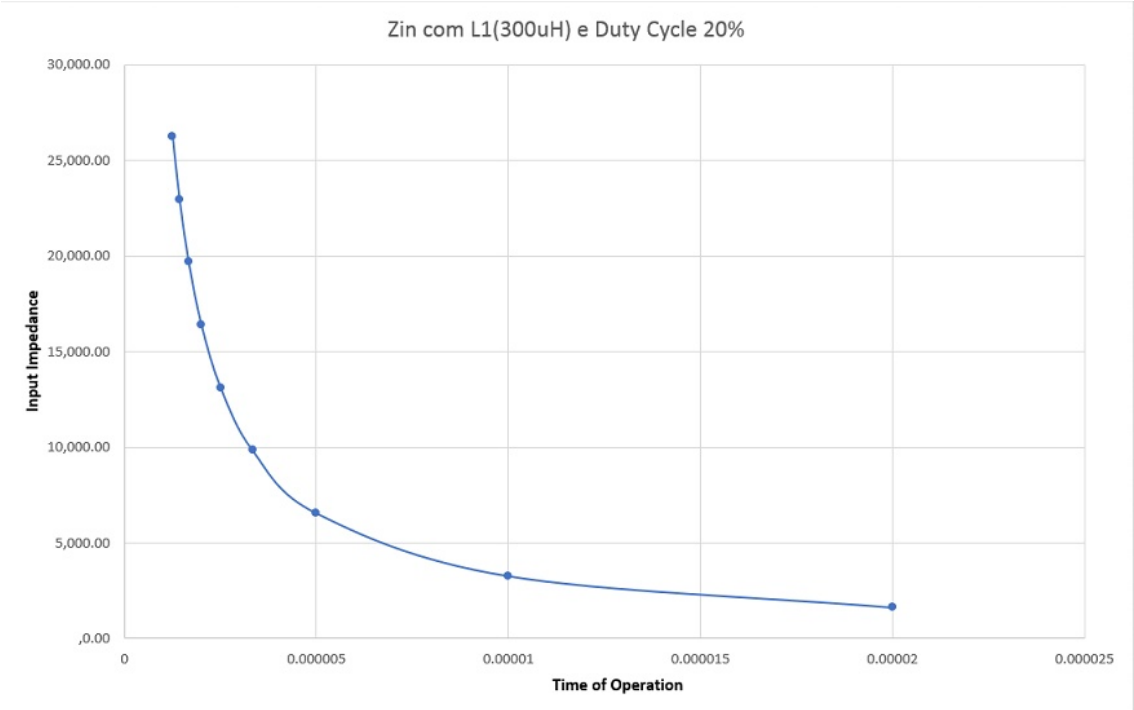

Figure 3.4: Graphical representation of the input impedance of this converter with the Time of Operation

In conclusion, this topology presents by default a lower input impedance than the one studied next although it does not lower the voltage so much, nervertheless it might be interesting to explore because this one is more favourable to be cascaded with another converter if necessary, since it does not lower the input voltage to the exact value needed.

Still it didn´t fully satisfied the converter requirements for this work because by manipulating the previous expressions about this converter it was found that it would only start to become interesting for the job at hand with an operating frequency of 1MHz or above and the physical components needed to do that were very expensive and made this project uninteresting from a comercial point of view.

The second topology to be fully analyzed and tested in this work was the simple buck converter as well as it´s derivative which consists of a cascaded buck converter, putting two stages of the simplest buck in cascade with each other. This topology alone could not make a large voltage conversion ratio without generating very high peak currents in all of the transistors, therefore the need to build a cascaded buck with more than one module cascaded [25].

Using the analysis previously mentioned to determine an expression of the input impedance of the converters, we could figure out that a simple buck converter would be:

$$V_{in} = VL1 + V_{out} \iff V_{in} - V_{out} = V_{L1} \iff V_{in} - V_{out} = L_1 \frac{dI_1}{dt} \iff \int_0^{T_{on}} \frac{V_{in} - V_{out}}{L1} = I \tag{3.6}$$

This is when the converter is on

$$V_{L1} = V_{out} \iff V_{out} = L_1 \frac{dI}{dt} \iff I = \int_{T_{on}}^{T} \frac{V_{out}}{L_1} dt \tag{3.7}$$

and for a converter which is off

Now since in a steady state the converter is alternating between the On and OFF state, the current never actually gets to zero, an offset has to be added to compensate for that fact:

$$\frac{(V_{in} - V_{out})T_{on} + V_{out}(T - T_{on})}{L_1} = I \tag{3.8}$$

At last by applying the generic expression 3.1 to 3.8 we can conclude that the input impedance expression of a simple buck converter is as follows:

$$Z_{in} = \frac{2V_{in}TL_1}{2(V_{in} - V_{out}))T_{on}^2 - V_{out}T_{on}^2} \tag{3.9}$$

Therefore it can be infered that as the cascaded converter is composed by n modules of the simple buck converter, its input impedance is:

$$\left(\frac{2V_{in}TL_1}{2(V_{in} - V_{out}))T_{on}^2 - V_{out}T_{on}^2}\right)^n \tag{3.10}$$

This is true as long as some considerations are taken into account such as the fact that the decoupling capacitors between the stages must be large enough to isolate one stage from the previous one and therefore diminishing the influence that one stage has on the next and acting as an independent voltage source, as well as the need for the control and

clock signals of the switches mustn´t overlap again in order for the stages of the converter to act as independent and minimize their impact on the working process of each other [2], [16].

In the images below it can be seen the schematic of the cascaded converter and the first test results that were very promising for the desired objective of this work.

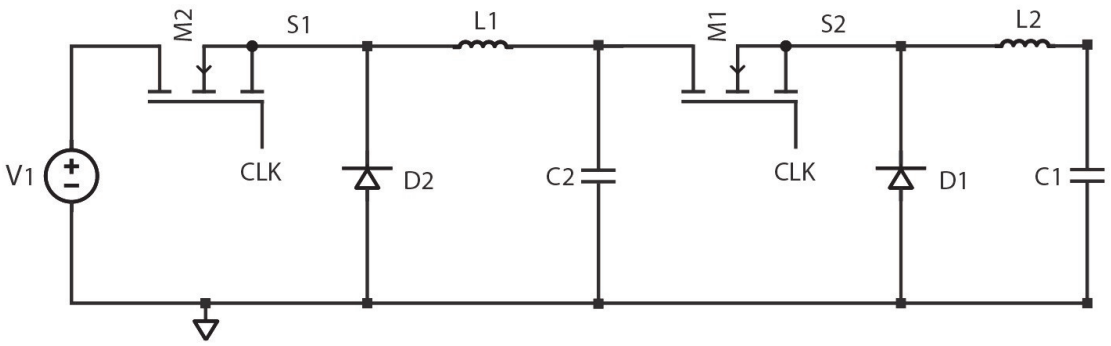

Figure 3.5: schematic of the cascaded buck converter with 2 stages

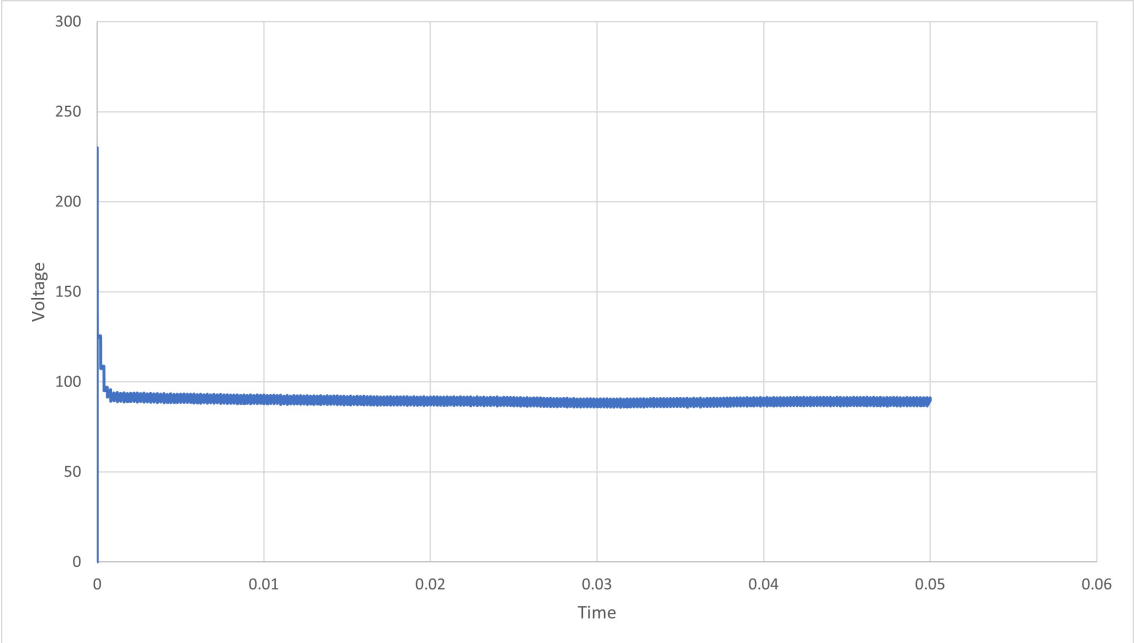

Figure 3.6: Voltage Evolution of the 2 Stage Buck Converter-Input Voltage

Figure 3.7: Voltage Evolution of the 2 Stage Buck Converter-Output Voltage

As can be observed on figures 3.6 and 3.7 the input voltage for the first stage of the buck converter is around 90V and the output voltage at the end of the converter is about 4V this is a very promising result, the capacitor between the stages had a 470nF a value which was determined experimentally. In this simulation this converter was tested with ideal voltage sources therefore assuming an infinite availability of input power still this

topology was very promising, showing a moderate level of eficiency attending to the objective of this work for frequencies between 10KHz and 1MHz with duty cycles of 20% with an efficiency varying from 12 to 25%. Further tests with different duty cycles were later performed in order to have a sweep analysis with different On times, nevertheless as previously explained the first tests were done with a 20% duty cycle in order to compare and analyse different topologies. The input impedance of this converter is shown below.

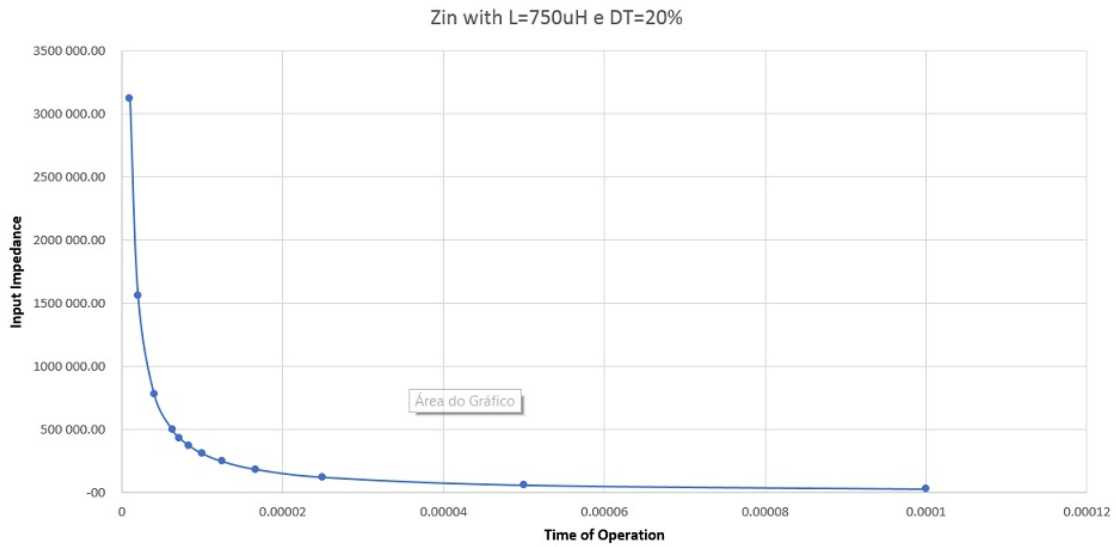

Figure 3.8: Evolution of the input impedance of the cascaded buck with the comutation period.

As can be seen from the previous graph, the converter input impedance is very high for large commutation frequency values but it decreases very rapidly. This phenomenon is due to the fact that for frequency values larger than 1MHz operating frequency the converter does not operate as desired due to parasitic effects on the gate of the transistors and large current spikes at the coils, rendering the mathematical model used not very accurate at such extreme conditions. Still at 500KHz frequency we can observe a very large input impedance as would be expected and the expression mentioned before becomes entirely valid. Also, of upmost importance is the fact that all these converters were tested with a relatively high duty cycle at this stage. For a real application and for further studies a smaller duty cycle will be used, allowing for a smaller power consumption and transfer as well as a larger step down voltage.

At last, the third and final topology to be fully analysed was the coupled inductor buck converter, this consists in a converter where there are two coils magnetically coupled to each other, this allowed for a very high step down voltage ratio with relatively small coils, at least theoretically [36]. The problem with this type of converter as is explained further is that each device would need to have its coils wound one by one and by hand in order to get the desired effects, therefore, this made the usage of the magnetically coupled inductor buck converter unfeasible for such a small energy harvesting device, although

it showed very promising results theoretically at least.

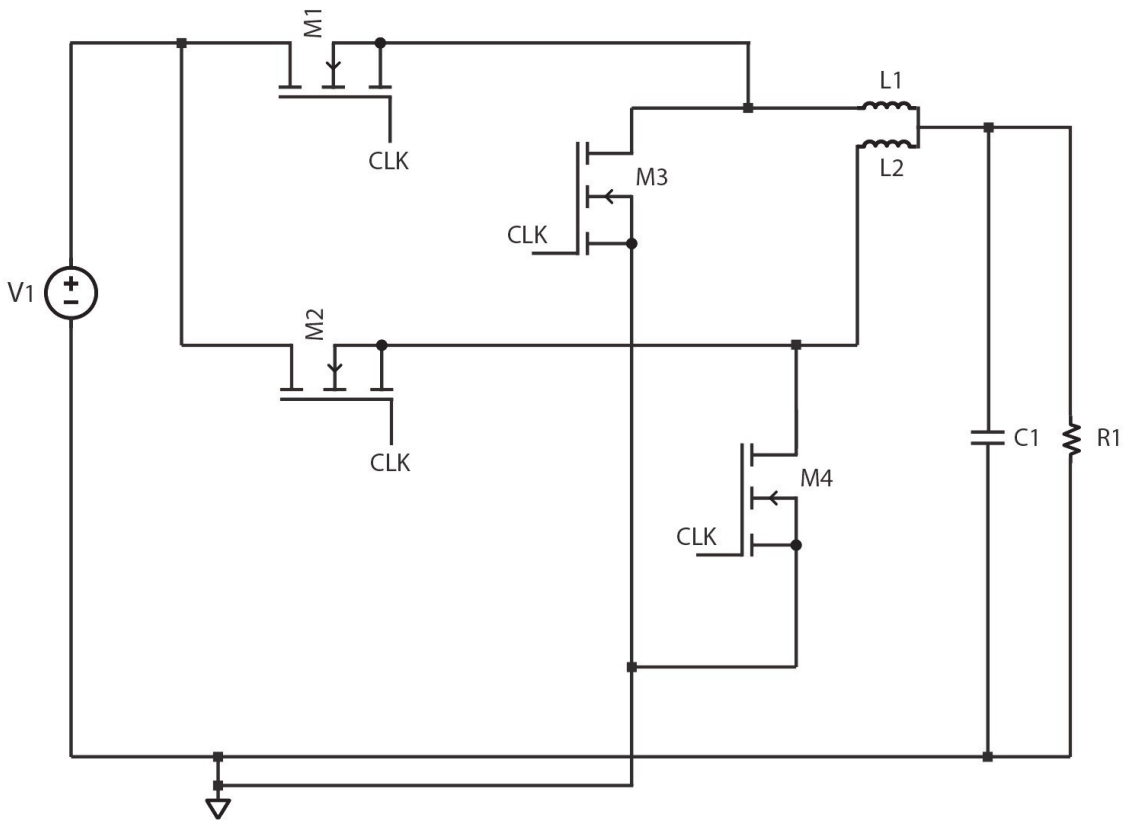

Figure 3.9: Coupled Inductor Converter Schematic

In figure 3.9 it can be seen the schematic for the coupled inductor buck converter, one aspect of this topology that must be taken into account is the fact that the two clock signals must not overlap, otherwise the input voltage would be short circuited to the ground and discharge a large ammount of current through it. This is undesirable since it is highly inefficent and creates large current spikes that can destroy the transistors.

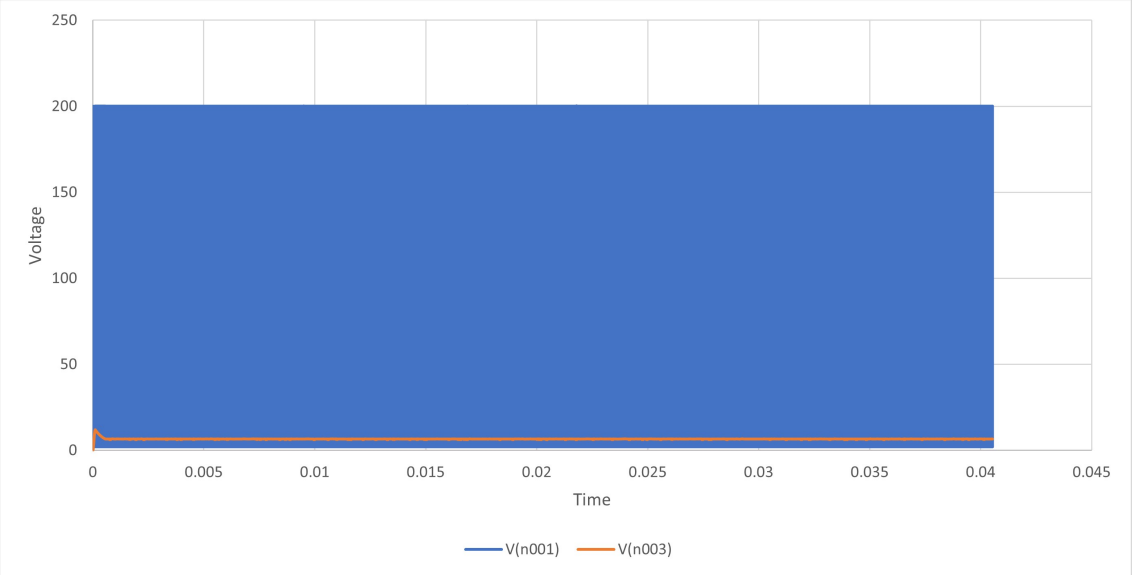

Figure 3.10: Coupled inductor converter voltage conversion in steady state

In figure 3.10 the steady state voltage conversion ratio of this converter is shown, it can be observed that it has a very large voltage conversion ratio, it can lower the voltage from 200V to about 6V, which is very desirable for the intended application.

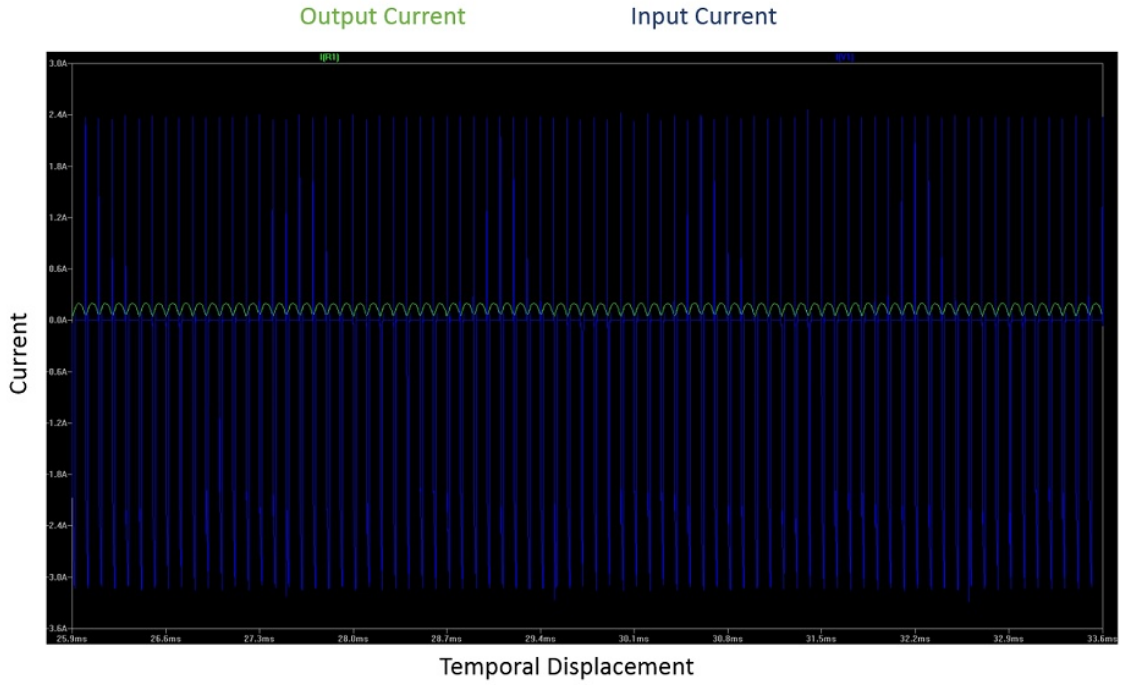

Figure 3.11: Steady State Current of the coupled inductor buck converter

In figure 3.11 we can observe that the current flow of this converter is fairly steady specially the output current represented in green, the input current which is in blue has large spikes, something that was observed at frequencies above 20KHz, not many studies

were presented towards solving this issue since there was a fair ammount of certainty that this converter wouldn´t be used for the reasons previously mentioned. Although the most probable cause of these spikes is the fact that coupled inductors carry a larger magnetic momentum because the same switch is in fact operating two coils and inducing currents in two coils at the same time [14]. Therefore the switches and the diodes on this converter should be faster to react and have less Gate parasitic capacitance in order to make for a quicker commutation and therefore eliminate those spikes [32]

Figure 3.12: Coupled inductor converter impedance evolution

As we can see on the figure above, the impedance on this type of converters is larger at a lower frequency, this might be due to the fact, once again, that at very large frequencies the converter cannot cope with the magnetic properties of the coils and induces current spikes on them. This increase in current, according to 3.1, will diminish the input impedance largely [32].

$$I_1(t) = \frac{V_{out}(T - T_{on})}{\sqrt{L_1 L_2}} + \frac{(L_1\sqrt{L_1 L_2}V_{out}) + (L_1 L_2 V_{out})(T - T_{on})}{L_1(L_1 L_2)\sqrt{L_1 L_2}} + \frac{(\sqrt{L_2 L_1}V_{out} + L_2 V_{out})(T - T_{on})}{L_1(L_1 L_2)} \tag{3.11}$$

3.2 Advanced study and testing selection of the final topology

Based on the preliminary analysis mentioned prior of the three topologies, the one that revealed more potential was the cascaded buck converter so it was decided that that topology would be the one that would be further analysed, disregarding the previous two. The number of stages was set at two stages which appeared to be enough to allow for the voltage conversion ratio necessary as well as maintainig the circuit simple and compact enough for this project, and also to use small enough components which allowed

to keep the circuit to be economically interesting. During the subsequent analysis some problems arose on the implementation of the converter, first of all the challenge to make it work with a circuit that simulates the actual ELMH from the work of [8]. This posed two problems at start, the first one was the fact that the energy harvesting system in question has a limited power output capability and the second one is the fact that the output impedance of the ELMH has to be precisely determined in order to get a proper line adaption to the converter. The output impedance of the ELMH was estimated as follows, based on the work of [8].

$$\frac{1}{2 * 250p * \pi} = Z_{out}(\Omega) \tag{3.12}$$

This gives an output impedance of the ELMH of about 12.7MΩ, therefore although in the preliminary testing we were interested on having a converter with an input impedance as large as possible, in order to have an ideal matching, the need and the converter would be readjusted for this calculated value of impedance. The advantage of having a converter with a margin to operate across a wide spectre of impedances is that all the circuit will not have a completly stable operating point, therefore it will need a controller circuit to keep it operating at the optimum point, this circuit will work by adjusting the duty cycle of the converter in order to control its input impedance and obtain the maximum efficiency from the converter as mentioned in [27] and [33]. This part about the controller, how it will work and what was done to cope with the challenges that arose is further debated in section 4.

From this point on, the basic requirements of the converter were completly set. There was the need for a converter that would ideally provide 12.7MΩ of input impedance, and worked at a very low power setting as well as could handle as much input voltage as possible to a maximum of 115V wich is the average value of 230 [28], and at the same time that could keep a step down voltage as high as possible in order to supply a supercapacitor[9].

With these goals set, the next task was to determine the expressions for the calculation of the value of the coils, capacitors throghout the circuit as well as the diodes and switches within it, the optimum operating frequency and the regime in which the converter would operate, being it DCM or CCM. All these problems are addressed in the sections that follow.

3.2.1 Detailed analysis for the final topology

After a final topology had been selected, in our case the cascaded buck converter, due to the fact that is was the one topology that showed the most prominent advantages as previously stated, and was the topology that allowed for a better energy transfer efficiency maitaining the step down ratio required and the input voltage to the converter as high as possible.

Therefore there was a need to study this architecture in more depth and obtain the actual expressions of the impedance [28] in order to modulate the behaviour of this converter and to be able to control its operating output. In order to do so there were two approaches that could be taken, the operation in CCM and the operation in DCM, both had their advantages and disadvantages. Because of that an analysis of both of them is shown below.

3.2.1.1 CCM mode Study

The CCM is characterized by the fact that the current inside the coils of the converter never drops down to zero, so even when the converter is in the off stage and only the diodes are conducting, there is always a remanescent value of current inside the coils [2]. Therefore the value of the voltage both in the coils as well as in the converter output is always rising until a certain value when it reaches equilibrium. In that state of equilibrium the ammount of power transfered to the output is equal the the ammount of power dissipated by joule effect in it, modulated in the schematic by a resistance, and therefore allows for a constant value of output voltage to be maintained [9]. These effects are better explained by the calculations and analysis below, this analysis was generalized for the simple buck converter and then it was made a specific analysis for the cascaded buck:

$$-V_s + R_{on}I_L + L\frac{di_l}{dt} + V_{out} = 0 \iff I_L + \frac{L}{R_{on}} * \frac{di_l}{dt} = \frac{V_s - V_{out}}{R_{on}} \tag{3.13}$$

As can be seen on equation 3.13 this analysis is similar to the one previously done for this type of converter, the only difference is that in this case the series resistance of the input source was taken into account, as calculated below, which gives the following complete expression for the inductor current in the buck converter during phase 1:

$$IL(t) = \frac{V_s - V_{out}}{R_{on}} * (1 - e^{-\frac{R_{on*t}}{L}}) + I_2'(0)e^{-\frac{R_{on}t}{L}} \tag{3.14}$$

In expression 3.14 is described the entire operating mode of the Buck converter in the first stage so the first member of the equation is the voltage gain derived from the fact that the switches are turned on and there is voltage being transfered from the input source to the output of the circuit. This forced regime has an exponential evolution because as it charges the supercapacitor at the output the evolution of the voltage tends to slow down and stabilize in a certain value. The second member of this equation is the current value that comes from the last phase and is added to the forced regime present in phase one.

In order to simplify this equation an approximation can be made, $e^x \approx 1 + x$ given that $X << 1$ in this case we can verify that because $X = \frac{R_{on}}{L} * T$ which is smaller than 1. In this condition an approximation can be made to the equation of phase one as well as to the equation of phase two.

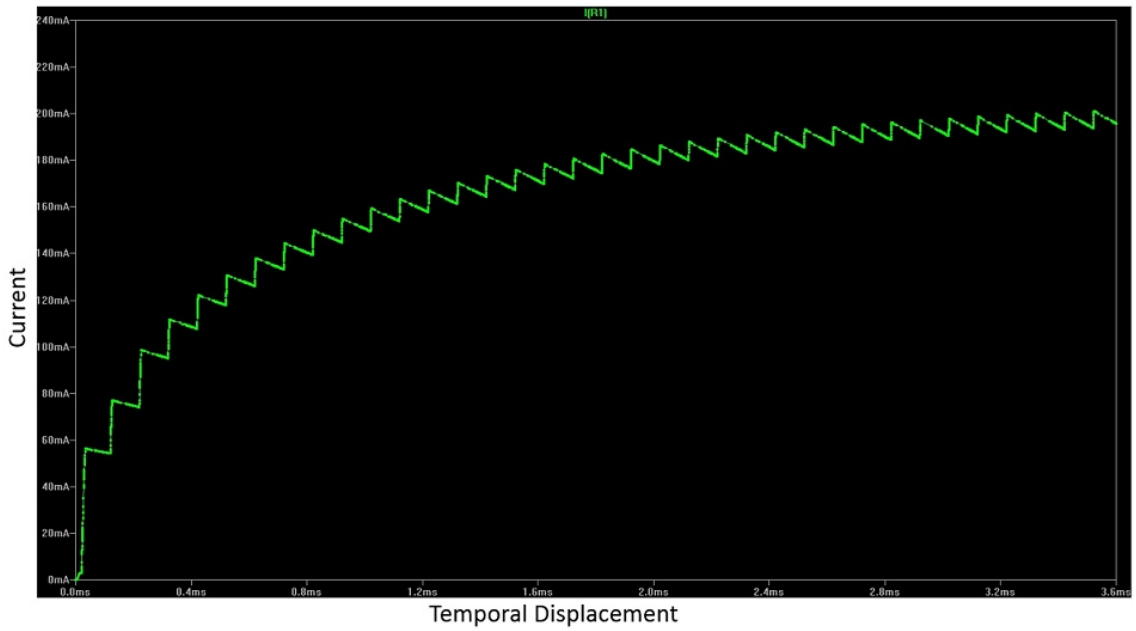

Figure 3.13: Evolution of the current until it stabilizes

As can be seen on the figure above, the current has a sawtooth exponential evolution towards a predetermined value. This only happens because the current on the next state is equal to the current in the coil plus a remanescent value from the previous state. As previously described this behaviour repeats itself until the circuit reaches a steady state where all the power and thus current that is transfered from the input is dissipated in the output and therefore the output capacitor does not charge anymore, leaving its voltage steady or at least oscilating around a stable average value.

$$\frac{V_s - V_{out}}{R_{on}} 1 - 1 + (\frac{R_{on}T}{L}) + I_2(1 - \frac{R_{on}T}{L}) \Rightarrow \frac{(V_S - V_{out})T}{L} + I_1(0) = i_l(t) \rightarrow t \in [0, T_{on}] \quad (3.15)$$

In much the same way, when phase 2 is active and the switches are turned off, the diodes are in freewheel and the same analysis can be made, in this case the expression for phase 2 will be:

$$\frac{-V_{out}T}{L} + I_{2L}(0) = il(t) \rightarrow t \in [T_{on}, T_{Clk}] \quad (3.16)$$

In conclusion of this analysis, keeping in mind that this circuit is an analog circuit that operates in continous mode, to verify the equilibrium condition, we can look at it as a discrete circuit, taking into account only the moments of comutation between phases. In this case, the equilibrium condition is when 3.15 = 3.16 from the previous comutation [9]. Given that for phase 1 $\frac{V_s - V_{out}}{L} = K_1$ and for phase 2 $\frac{-V_{out}}{L} = K_2$, for simplicity. We can further describe this particular converter for the steady state operation as:

$$I_{L1}[n] = K_1 * T_1 + K_2(T_{CLK} - T_1) + I_L[n-1] \quad (3.17)$$

This is for the first state of the converter and for the second we can describe it in much the same way as:

$$I_{L2}[n] = K_1 * T_2 + K_2(T_{CLK} - T_2) + I_L[n-1] \tag{3.18}$$

Given that this converter works in ping-pong configuration, so T_1 and T_2 were complementary and $T_1 + T_2 = T_{CLK}$.

In the case of our cascaded Buck converter since it is made up by two stages of simple buck converters, we can analyse both stages independently and consider that the output of the first stage is the input voltage of the second stage, this analysis is only valid as long as the intermediate capacitor, C2 on figure 3.6, is large enough to enable a full detachment between stages and thus behave as a voltage source [2] and [4].

3.2.1.2 DCM mode Study

Forcing the converters to operate in CCM mode has some disadvantages for the intended application. In order to achieve the desired power level which is very low and the desired voltage ratio which is very high, it is necessary to use a very low duty cycle in the converter's clock signal. Therefore, using the analysis described in [4], in order to maintain CCM it would be necessary to either use 10H coils or increase significantly the clock frequency (more than 10MHz). The first option would result in a very expensive and bulky system and the second option would not work because there is not enough power from the energy harvesting device to create a high frequency clock, given the amount of energy required to charge the parasitic capacities of transistors and diodes 2.14.

So the solution is to use a relatively low value for the coils and a frequency small enough to make this solution both economically attractive and feasible was to explore the operation of these converters in DCM [22].

The basic operation of this mode is that the current circulating in the coils drops down to zero and remains equal to zero for a significant part of the clock period[23].

This format of operation has some advantages and some drawbacks as well. The advantages are that it allows for a longer shutdown period of the circuit as mentioned in chapter 2, in practice, this allows for a reduction in the average current and thus power transferred from the input to the output because the converter remains in the off state and discharging the coils for a longer time [35]. This allows the converter to have a very high conversion ratio, benefitting from a longer operation period and thus a lower frequency. The drawback is that in DCM we have another degree of freedom, from the fact that period of the controller has to be constantly adjusted in order to optimize the amount of time it is in the off state in order to keep it with the appropriate step down ratio and as efficient as possible[22].

In DCM mode we will have the following equality regarding the times of operation of the converter: $T_{CLK} = T_1 + T_2 + T_3$, in which T_1 represents the amount of time the converter is turned on for the first step, the second time T_2 is the time the converter is turned off

for the second step and T_3 which is the time the converter remains in the off state but in this case, the current of the coils actually drops down to 0 and remains at 0 for a given time until the cycle starts all over.

So as in the previous state of operation, we will have the two main operating states, of the converter on and off plus a third state which will control the overall power that is transferred from the input to the output of the converter [23].

$$\frac{V_S - V_{out}}{L} * t = i_L(t) \longrightarrow t \in [0, T_1] \tag{3.19}$$

In this first state, the converter won´t have a current component to be added to it since it always starts off from 0 because of the time that the current in the coils drops down to 0.

$$\frac{-V_{out}}{L} * t + I_{L2} = i_L(t) \longrightarrow t \in [T_1, T_2] \tag{3.20}$$

In the second state a component must be added to represent the maximum current of the coils at the end of the first stage at how it drops down to 0 [23].

$$0 = i_L(t) \longrightarrow t \in [T_2, T_{CLK}] \tag{3.21}$$

Finally, the third state is just keeping the current in the coils at 0 in order to spread it along a longer time and thus making the current over time along the converter go down, and thus making the input impedance of the converter go up and so improving its efficiency by making it better adapted to the grid and being able to retain a higher level of voltage from the source.

Ergo a conclusion can be made that the steady state of this converter in DCM is given by the following expression:

$$\frac{(\int_0^{T_1} I_L(T)\,dt + \int_{T_1}^{T_2} I_L(T)\,dt + \int_{T_2}^{T_{CLK}} 0\,dt)^2 * R_L}{T_{CLK}} = \frac{V_s}{2R_{series}} \tag{3.22}$$

Which translates into the following expression if we substitute the generic term I_L by the actual expressions that it represents. which will be 3.19, 3.20 and 3.21 in this order.

$$\frac{(\int_0^{T_1} \frac{V_S - V_{out}}{L} * t\,dt + \int_{T_1}^{T_2} -\frac{V_{out}}{L} * t + I_{2L}\,dt + \int_{T_2}^{T_{CLK}} 0\,dt)^2 * R_L}{T_{CLK}} = \frac{V_s}{2R_{series}} \tag{3.23}$$

What it means is that the first state of a converter working in DCM has a rising flank from 0 to T_1 where its inductor current rises from 0 up to the maximum value possible. Then it has a state where its inductor current is discharging and dropping from the peak value until it reaches the value of 0. And at last, it has a third and final state in which the current in the inductor remains at 0 for the remainder of the cycle. This third term that extends from T_2 to T_{CLK} is the additional degree of freedom that can be used in DCM in order to control the values of power of the converter and guarantee that it is stabilized at a

lower voltage using smaller coils and a smaller frequency, because the period of operation is shortened to the extent that the converter remains for a certain amount of time in the off state and with its coils at 0 current.

Therefore the chosen mode of operation was the DCM mode, because although it is more complicated to implement from a controller point of view, it is easier to obtain high levels of impedance and therefore get a large amount of power from the ELMH to the output capacitor.

3.2.1.3 Problems That Arose From The Cascaded Topology and Possible Solution

After testing the 2 stage cascaded buck converter some problems arose that became unovercomable. These problems were detected after the testing of the circuit in Spice software and could not be foreseen in the theoretical analysis of the circuit. Most of these problems were connected to the fact that the circuit has a large amount of parasitic capacitances to be charged on each cycle especially if it is working in DCM mode [17].

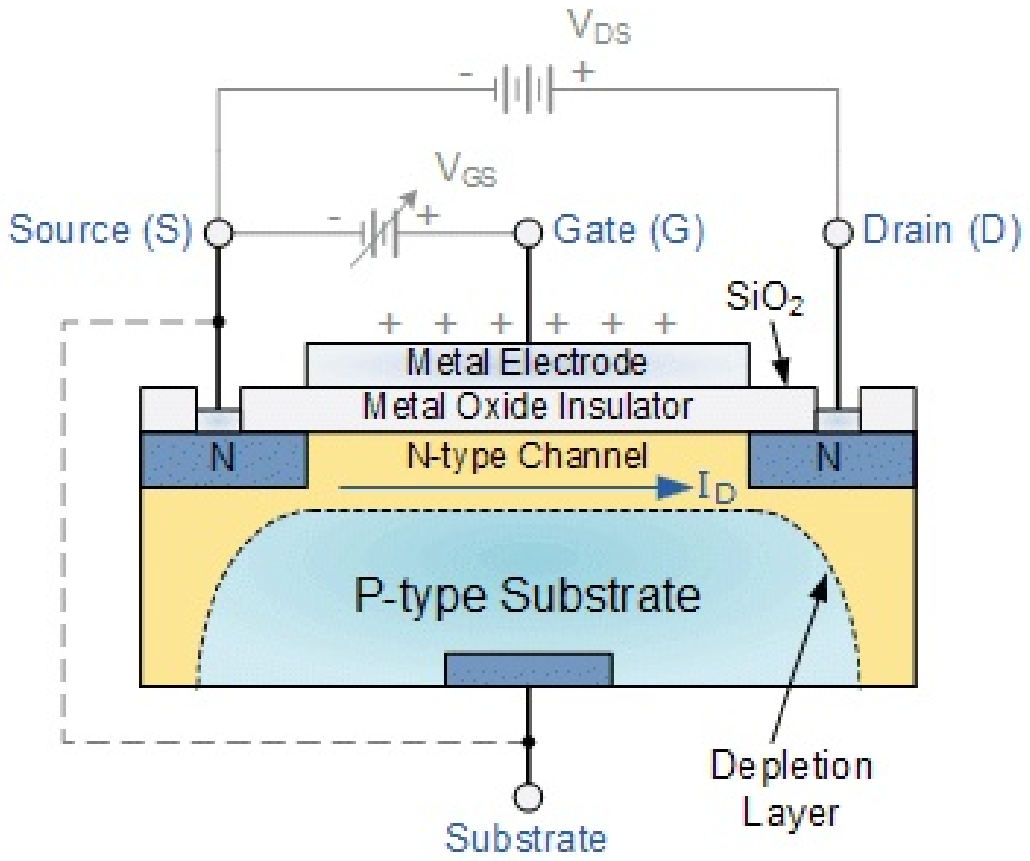

Figure 3.14: NMOS-transistor

The first of these problems is that each switch being a NMOS transistor has a certain gate capacitance between the gate and the substrate. Every time this switch is turned

on this capacitance has to be charged. Given that this circuit is meant to work with very small power levels this capacitance has to be very small otherwise the circuit efficiency collapses and in some cases, all the power the circuit could deliver was used to charge these capacitances [30]. The only solution is to search for or build very small transistors which offer a very small area. The other solution is to use a single stage converter in order to have just one switch and therefore just one capacitance to be charged.

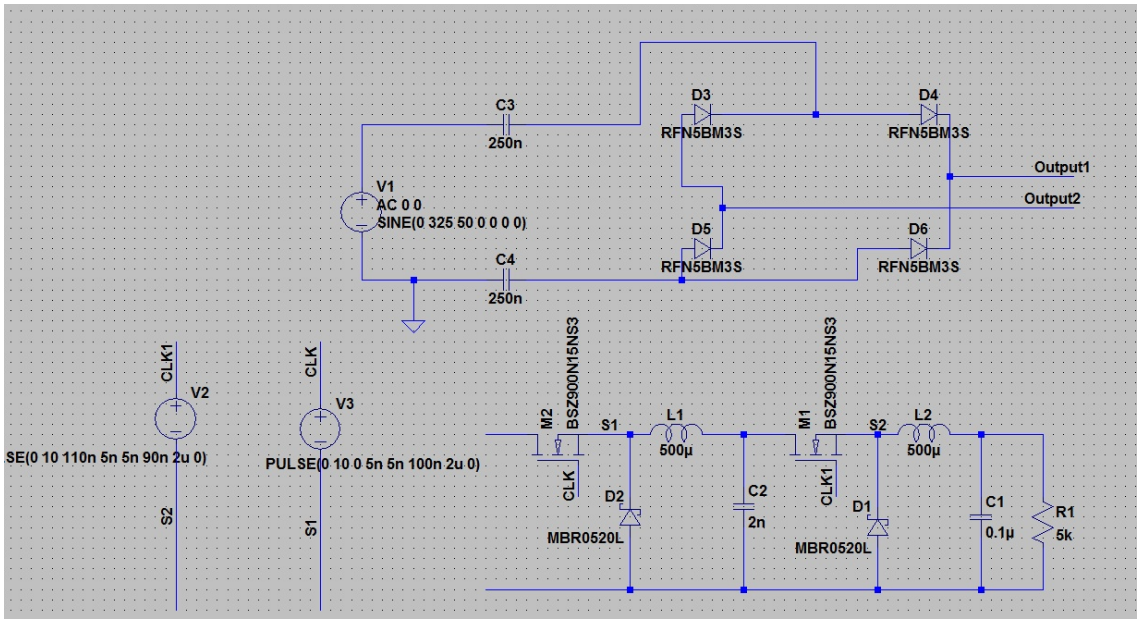

Figure 3.15: 2-stage Buck Converter Schematic.

The second problem that we faced which was more demanding and hard to overcome was the fact that with a two stage cascaded buck converter as seen on figure 3.15, the input capacitance of the converter which was the combined capacitance of the gate capacitance of the two switches, would be very close to the output capacitance of the ELMH. Therefore due to these parasitic effects the circuit would behave as two capacitors in parallel which caused the input impedance of the converter towards the ELMH to be very small and way below what was expected from the theoretical and ideal results.

Because of this in this particular topology, it was verified that the output voltage and the input voltage would be rising very rapidly and continue to rise way beyond any possible values when charged by the ELMH. This was because of this very low impedance that the circuit presented, the clock signals, which on this stage were represented by ideal voltage sources, would be providing large ammounts of current to the circuit, and both the output capacitor, as well as the parasitic capacitances from the switches would be charged using energy from the clock signals, as can be observed on the image below.

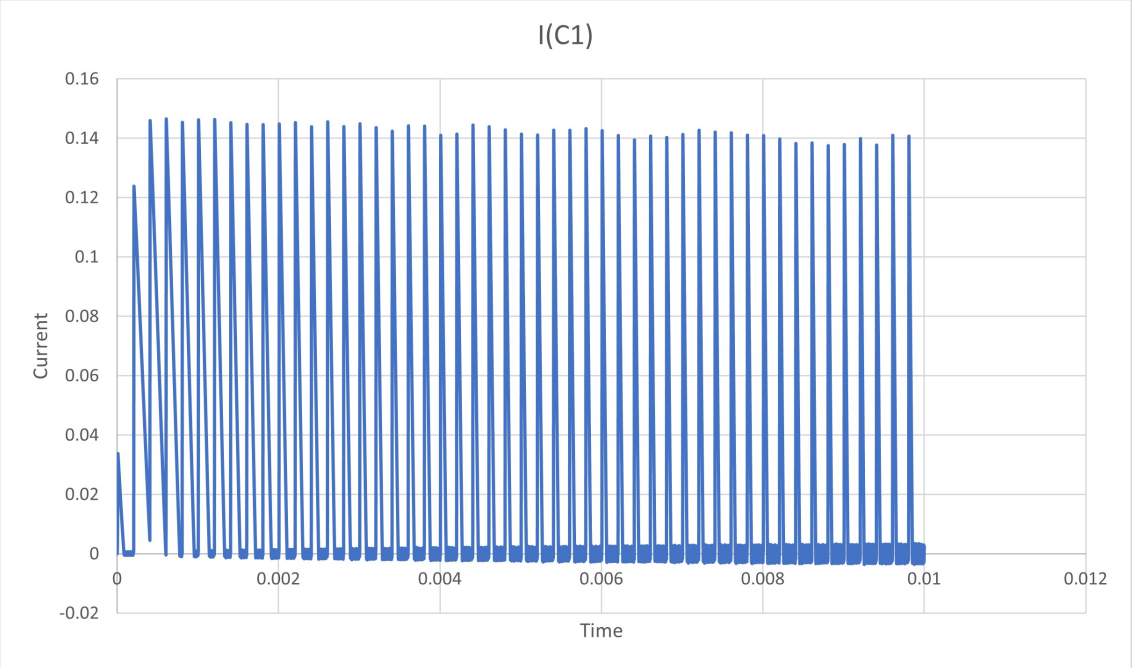

Figure 3.16: 2-stage Buck Converter Transient Analysis, Output Current.

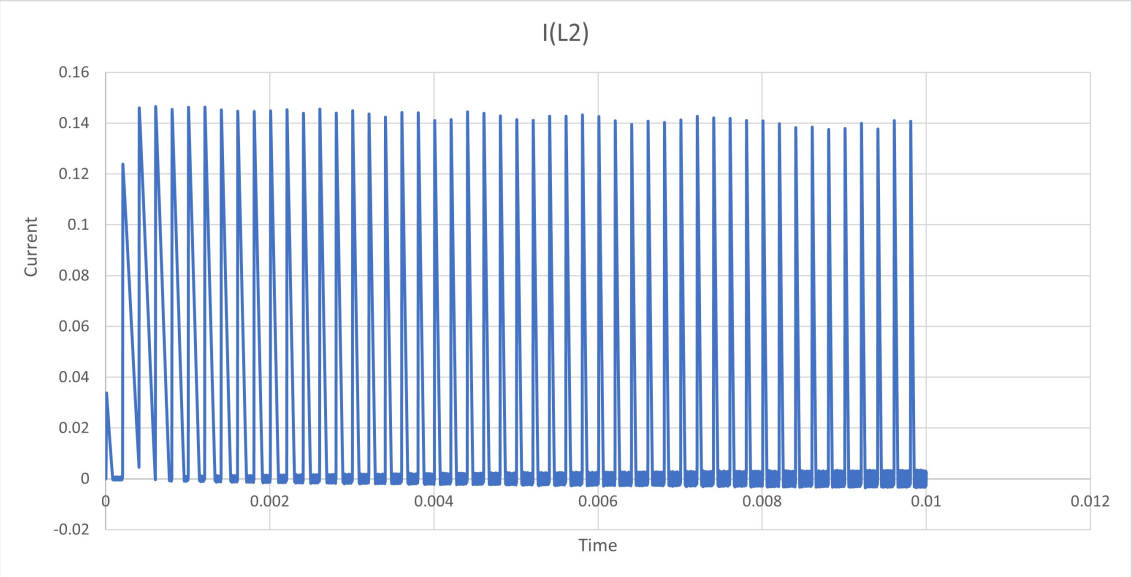

Figure 3.17: 2-stage Buck Converter Transient Analysis, Current on the Second Coil.

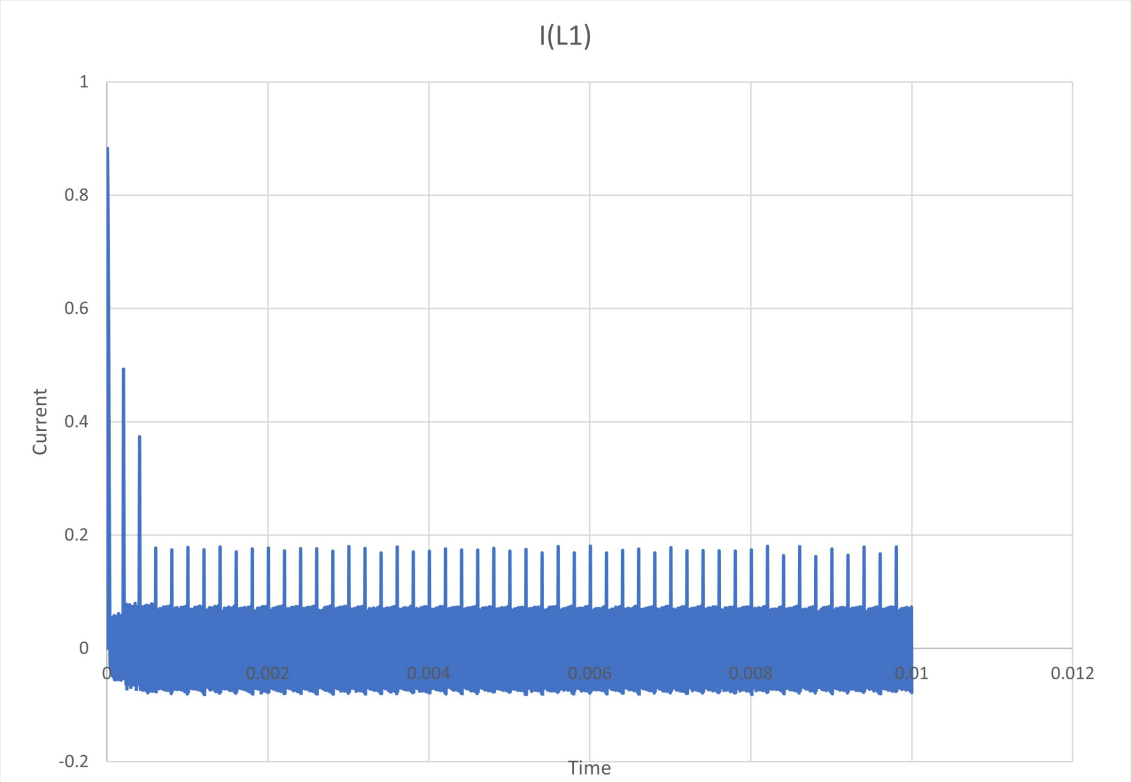

Figure 3.18: 2-stage Buck Converter Transient Analysis, Current on the First Coil

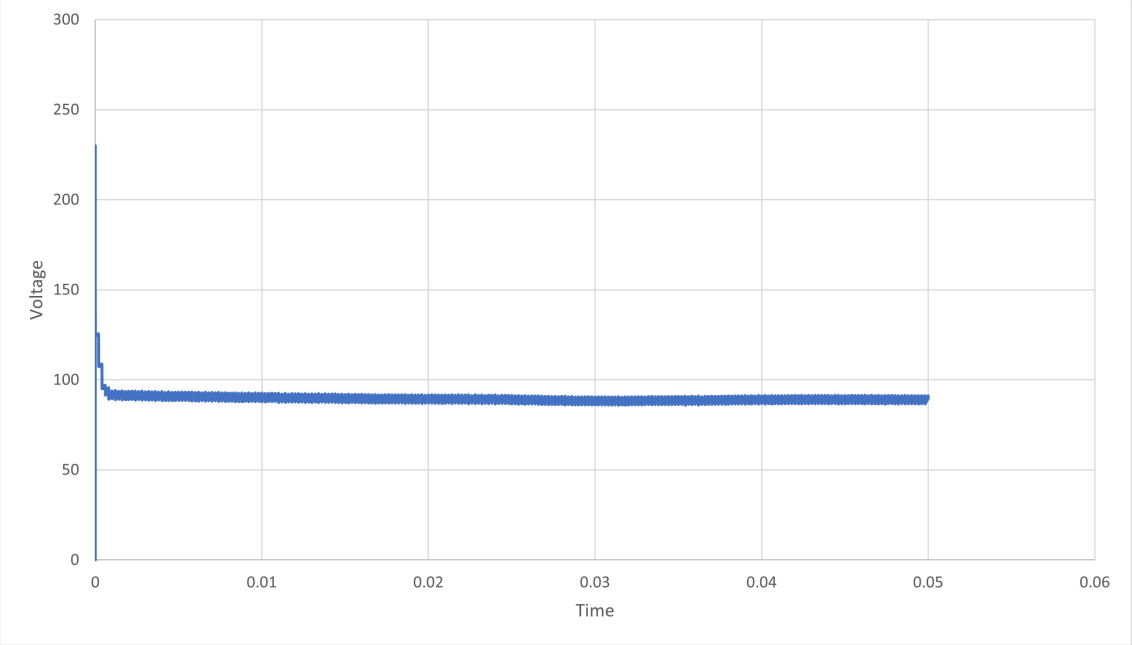

Figure 3.19: 2-stage Buck Converter Transient Analysis, Input Voltage.

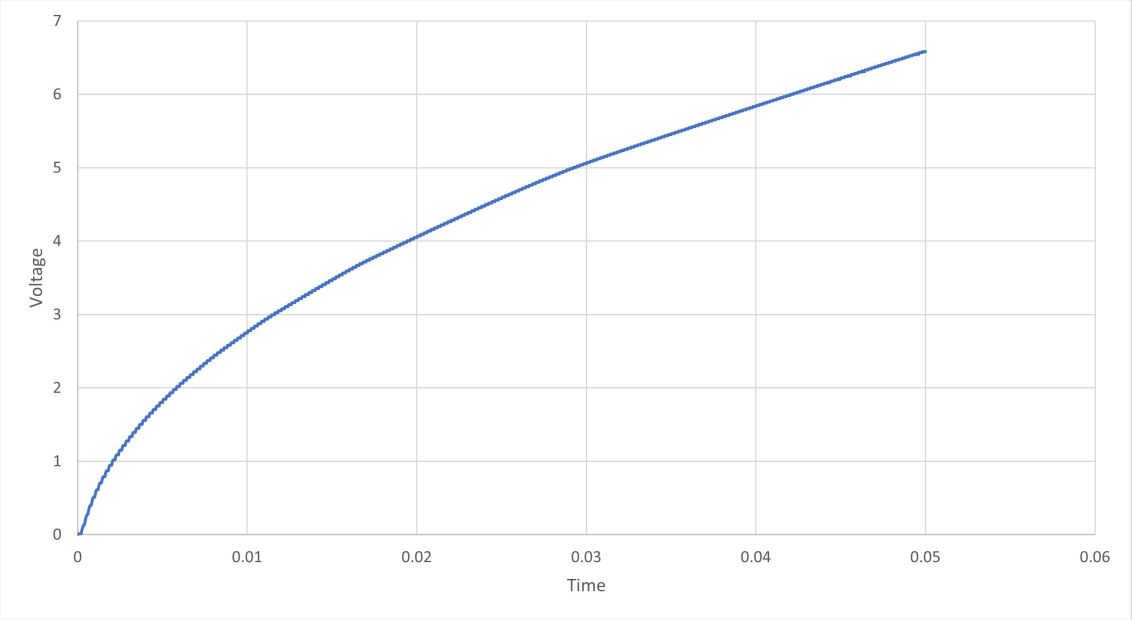

Figure 3.20: 2-stage Buck Converter Transient Analysis, Output Voltage.

As can be seen on figures 3.16 to 3.20 the green line represents the input voltage to the converter which is very close to the ideal results, but on the lower half of the graph the current from the clock signal sources can be observed as delivering a large amount of current, way beyond the maximum capacity of this circuit.

Due to these problems and concerns, the 2 stage cascaded buck converter had to be abandoned because it was simply a too large circuit with many devices that had to be charged and discharged in order for it to work, and unfortunately there was simply no power availability for it. So it was decided to try to replicate the same results using a simple buck converter, with just one stage, because this is a smaller circuit with way fewer components. Although this has an inconvenience, which is that to achieve the same step down voltage with just one stage, the components had to be larger in size have the circuit would most certainly had to operate at a larger frequency in order to boost both the input impedance as well as the efficiency.

3.2.2 Study of the Single Stage Buck Converter

As previously mentioned, the cascaded buck converter had to be abandoned, and replaced for a single stage simple buck converter as the one shown on figure 3.21, therefore a further study and analysis for this new, although simpler, circuit had to be conducted, such analysis was as follows:

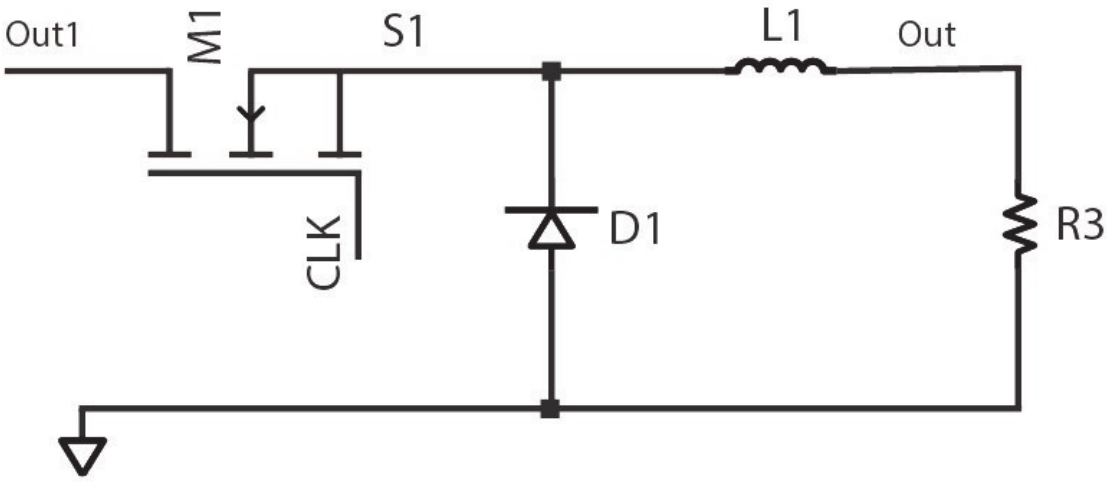

Figure 3.21: Single Stage Buck Converter Schematic

First the step down ratio which would be the duty cycle D, although in this particular case, given that the output voltage is not constant and is always rising, given that the output charge is a supercapacitor, but based on the analysis previously made by [4], we can reach a compromise between the duty cycle and the impedance of the converter, and the velocity at which the output voltage rises in order not to exceed the maximum voltage of the supercapacitor and also not to have the need of switching the converter on and off multiple times [26]. But more of that will be exploited in the section about the controller of the circuit.

So the components chosen and calculated for the operation of the converter shown in figure 3.21 were:

$$L = 1mH \tag{3.24}$$

$$c = 10\mu W or R = 1000K\Omega \tag{3.25}$$

$$f = 10KHz \tag{3.26}$$

$$D = 1\% \tag{3.27}$$

$$T = 100\mu s \tag{3.28}$$

These values were obtained from the mathematical analysis and sizing of the componnents for this converter, some of which are mentioned below as well as economical considerations about the price of the componnents and the size of each one of them and how this could affect the normal operation of the converter as well as its purpose as a mobile unit.

The second part to be analyzed was the impedance that the converter could present to the ELMH, because as it was explained on previous sections, there was the need to have the converter well adapted to the grid in order to achieve the maximum power possible. The theoretical expression of the simple buck converter was:

$$Z_{in} = \frac{U_{in}}{I_{in_avg}} = \frac{T_{CLK}}{T_1} \cdot \frac{L}{T_1} \cdot \frac{V_{out}}{V_{in} - V_{out}} \cdot 2 \tag{3.29}$$

Where T_{CLK} is the clock period, T_1 is the On time, L is the value of the inductance of the coil.

Based on expression 3.29 it could be concluded that the parcel $\frac{V_{out}}{V_{in} - V_{out}}$ is constant and the L parameter was fixed and sized to be as large as possible, within reasonable limits, such as economic cost of the component and physical size of it, in order to make a small compact circuit with very limited power loss, this value was optimized at 1mH.

Therefore the impedance of the circuit was sized based on the Duty cycle and the time between cycles that elapsed, in the DCM with all this in mind we reached a value of impedance of 6,8MΩ with a theoretical ideal frequency of 10KHz, which is around half the ideal value of 12,8MΩ [8].

Finally the third aspect that was designed and considered in order to start testing the new converter topology was the efficiency of the converter.

$$\eta = \frac{P_{out}}{P_{in} + P_{CLK}} \tag{3.30}$$

As can be seen on expression 3.30 the efficiency of the converter has to be measured based on the output to input ratio and the power supplied to the clock generator, because there is a chance that the power from the clock generator actually provides some current to the circuit, especially to charge the parasitic capacitances of the switches coming on and off. In order to calculate the efficiency of the circuit, since there was the need to use a very large amount of cycles of the circuit, for obtaining a better precision and accuracy of the results, the output capacitor was replaced by a very large resistor, this way the precision would not be compromised, since a very large resistor gives an electrical behaviour similar to the one of a discharged capacitor. There was a chance to measure the power output with less computing power. With this simulation we could obtain power levels of around 70μW.

This topology showed very promising results although those results came very far apart from the actual ideal results that were expected. As shown in the images below.

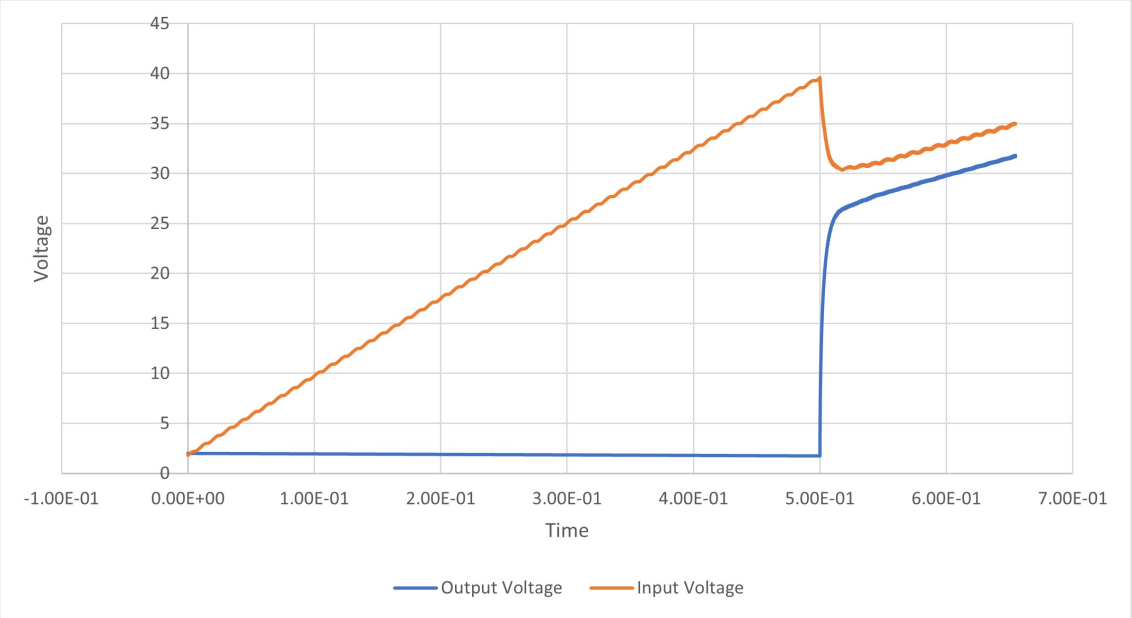

Figure 3.22: Ouput and Input Voltage of the Single Stage Buck Converter

As seen in the previous figure 3.22,those are the simulated results of the simple stage buck converter with a capacitor of 10nF, the value of the capacitor had to be adjusted empirically within certain limits, in order to have a large energy reservoir, which allowed the output voltage to increase slowly so the circuit would not be constantly turning on and off, but also small enough not to be too expensive and allow for the total impedance of the Converter to be reasonably high so the circuit and the power transfer could occur.

Worth noting in either figure is that the converter only starts after half a second from being coupled with the ELMH, this is due to the fact that with such large capacitances both in the output as well as in the intermediate portions of the circuit, at the beginning when all capacitances are discharged, the circuit presents a very low impedance to the ELMH and therefore if not given a few moments to build up its voltage during the start, and if connected all at once, the converter presents itself as a short circuit to the terminals of the ELMH.

As can be seen on figure **??** left unattended the output voltage would stabilize at around 4V, therefore we would need a killswitch in order to prevent the output voltage from exceeding 2V and the input, with a large capacitor such as this one is stable at around 7 to 8V, this allows for approximately the same levels of power transfer that we would find using a 1000KΩ resistor on the output as the one used on image 3.22.

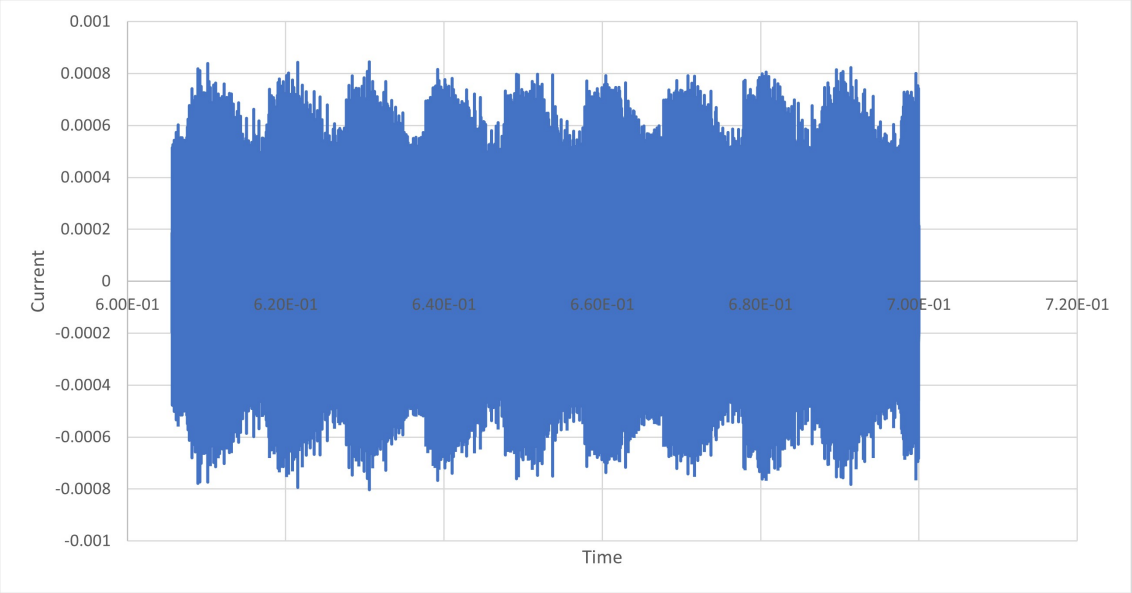

Figure 3.23: Current evolution on the coil of the buck converter

On figure 3.23, we can observe the current on the coil of the converter, as we can see there is some power loss due to reactance on the coil and switch. This is due to the fact that the power losses due to the swithcing of the parasitic capacitances associated to the circuits components represents a significant fraction of the small amount of available input power. So according to [15] and [13], this reactance can be explained by the fact that the parasitic capacitances of the gate from the switch and the parasitic capacitances of the PN junction of the diode are causing a resonance effect with the coil of the circuit and this is basically generating unwanted harmonics in this topology. According to [15] one way to deal with this is using another topology, the afore mentionned quadratic buck converter, although this is not usable in here because of the previously mentioned power loss on the switches, the other solution was to choose components with gate and junction capacities as small as possible, and try to mitigate this phenomenon.

In order to maximize the efficiency of the converter multiple types of transistors and diodes were chosen, in order to obtain one that could have the lowest possible parasitic capacitance and therefore provide a better efficiency of the circuit.

At first multiple types of transistors were considered and different results for the various power levels and efficiency levels were registered in order to compare them across the different clock frequency values, the results are shown on the tables below.

Transistor	Frequency	Pin_converter	PCLK	Pin_Source	P_out	Converter Efficiency	System Efficiency (measured at the Source)
IPP180N10N3							
	7KHz(a 200n)	7.60E-05	0.000196723	0.00011008	7.45E-05	2.73E+01	2.43E-01
	8KHz	7.55E-05	0.000215159	0.00010984	7.47E-05	2.57E+01	2.30E-01
	9KHz	7.65E-05	0.0002501	0.00010924	7.48E-05	2.29E+01	2.08E-01
	10KHz	7.78E-05	0.00026908	0.00010895	7.49E-05	2.16E+01	1.98E-01
	11KHz	7.37E-05	0.000295949	0.00010875	7.50E-05	2.03E+01	1.85E-01
	12KHz	7.30E-05	0.000328479	0.00010857	7.51E-05	1.87E+01	1.72E-01
Transistor	Frequency	Pin_converter	PCLK	Pin_Source	P_out	Converter Efficiency	System Efficiency (measured at the Source)
Fairchild FDS6961A(mauser)							
	7KHz(a 200n)	4.05E-04	0.00018141	0.00020452	9.66E-05	1.65E+01	2.50E-01
	8KHz	1.85E-04	0.000212618	0.0001883	9.06E-05	2.28E+01	2.26E-01
	9KHz	1.34E-04	0.000168238	0.00017631	8.60E-05	2.84E+01	2.50E-01
	10KHz	1.34E-04	0.000168238	0.00017631	8.60E-05	2.84E+01	2.50E-01
	11KHz	1.34E-04	0.000168238	0.00017631	8.60E-05	2.84E+01	2.50E-01
	12KHz	1.30E-04	4.27E-05	0.00015439	7.80E-05	4.50E+01	3.96E-01
Transistor	Frequency	Pin_converter	PCLK	Pin_Source	P_out	Converter Efficiency	System Efficiency (measured at the Source)
Rohm RSR020N06(mouser)							
	7KHz(a 200n)	1.77E-04	6.62E-05	0.00016157	8.25E-05	3.39E+01	3.62E-01
	8KHz	1.27E-04	6.98E-05	0.00015159	7.85E-05	3.99E+01	3.55E-01
	9KHz	1.25E-04	7.17E-05	0.00014444	7.61E-05	3.87E+01	3.52E-01
	10KHz	9.98E-05	8.07E-05	0.00013896	7.47E-05	4.14E+01	3.40E-01
	11KHz	7.36E-05	8.83E-05	0.00013493	7.38E-05	4.56E+01	3.31E-01
	12KHz	1.08E-04	9.38E-05	0.00013145	7.32E-05	3.63E+01	3.25E-01

Figure 3.24: Transistor analysis for better efficiency 1.

Transistor	Frequency	Pin_converter	PCLK	Pin_Source	P_out	Converter Eficiency	System Eficiency (measured at the Source)
Rohm RSQ015N06(mouser)							
	7KHz(a 200n)	1.74E-04	3.80E-05	0.00019793	9.75E-05	4.59E+01	4.13E-01
	8KHz	1.67E-04	4.21E-05	0.00018166	9.03E-05	4.32E+01	4.04E-01
	9KHz	1.89E-04	4.48E-05	0.00016928	8.52E-05	3.64E+01	3.98E-01
	10KHz	1.76E-04	4.65E-05	0.00016013	8.16E-05	3.67E+01	3.95E-01
	11KHz	1.64E-04	4.64E-05	0.00015301	7.91E-05	3.76E+01	3.96E-01
	12KHz	1.57E-04	6.24E-05	0.000147	7.72E-05	3.52E+01	3.68E-01
Transistor	Frequency	Pin_converter	PCLK	Pin_Source	P_out	Converter Efficiency	System Efficiency (measured at the Source)
Rohm RSF015N06 (Mouser)							
	7KHz(a 200n)	1.74E-04	3.94E-05	0.00019564	9.63E-05	4.52E+01	4.10E-01
	8KHz	2.02E-04	4.47E-05	0.00017978	8.94E-05	3.62E+01	3.98E-01
	9KHz	1.86E-04	4.56E-05	0.00016763	8.46E-05	3.66E+01	3.97E-01
	10KHz	1.74E-04	4.68E-05	0.00015883	8.11E-05	3.67E+01	3.94E-01
	11KHz	1.62E-04	4.88E-05	0.00015198	7.87E-05	3.74E+01	3.92E-01
	12KHz	1.51E-04	6.26E-05	0.00014609	7.69E-05	3.60E+01	3.68E-01
Transistor	Frequency	Pin_converter	PCLK	Pin_Source	P_out	Converter Efficiency	System Efficiency (measured at the Source)
Rohm RJP020N06 (Mouser)							
	7KHz(a 200n)	9.88E-05	1.56E-04	0.00013204	7.37E-05	2.89E+01	2.56E-01
	8KHz	9.17E-05	1.84E-04	0.00012734	7.29E-05	2.64E+01	2.34E-01
	9KHz	9.34E-05	2.04E-04	0.00012371	7.25E-05	2.44E+01	2.22E-01
	10KHz	8.63E-05	2.22E-04	0.00012148	7.25E-05	2.35E+01	2.11E-01
	11KHz	8.58E-05	2.50E-04	0.00011931	7.25E-05	2.16E+01	1.96E-01
	12KHz	8.06E-05	2.74E-04	0.00011772	7.26E-05	2.05E+01	1.85E-01

Figure 3.25: Transistor analysis for better efficiency 2.

Transistor	Frequency	Converter Efficiency	System Efficiency (measured at the Source)
	7KHz(a 200n)	3.30E+01	3.22E-01
	8KHz	3.24E+01	3.08E-01
	9KHz	3.12E+01	3.04E-01
	10KHz	3.14E+01	2.98E-01
	11KHz	3.18E+01	2.92E-01
	12KHz	3.19E+01	3.02E-01

Figure 3.26: Average efficiency for different clock values for all the transistors.

As can be seen on figures 3.24 and 3.25 the efficiency of the circuit ranges from 30%

to 45% and that the best transistors were those from the manufacturer Rohm, due to their very low gate capacitance. As well as the optimum frequency obtained experimentally was slightly below the 10KHz initially obtained, in the order of 8 to 9KHz. This is due to the fact that the theoretical expression is for the ideal case and in reality, the parasitic effects of multiple components greatly affects the behavior of the circuit since we are working with very small amounts of power, in the order of tens of μ watts, due to this fact the fast comutation of the switches would consume a vast amount of power from the circuit which reduces efficiency [30], so it was decided to adopt a smaller comutation circuit because the gain from the switches would compensate the decrease in the converter performance.

The components chosen were the ones with the lowest gate capacitance as stated and explained in the previous paragraph. A final study was conducted in which an average of all the efficiency from multiple transistors was taken into account in order to have a better understanding of the circuit efficiency and behavior overall. As can be seen on image 3.26, the best efficiency is slightly lower than the 10KHz from the theoretical analysis, this, as it was explained prior, can be explained from the nonideal effects of the switches which cause it to decrease the system efficiency with a larger amount of comutations. According to the final figure, the ideal frequency would be of 7KHz such as it would be for the transistor that was chosen the Rohm RSQ015N06, which grants the largest converter and overall circuit efficiency, for the analysis of the diodes this transistor was chosen as the final one.

Diode	Frequency	Pin_converter	PCLK	Pin_Source	P_out	Converter Efficiency	System Efficiency (measured at the Source)
RB705D(pharnell)							
	7KHz(a 200n)	2.57E-04	3.81E-05	0.000302907	1.68E-04	5.70E+01	4.92E-01
	8KHz	2.38E-04	4.69E-05	0.000279587	1.59E-04	5.56E+01	4.86E-01
	9KHz	2.16E-04	5.29E-05	0.000254843	1.44E-04	5.34E+01	4.67E-01
	10KHz	1.97E-04	5.80E-05	0.000234179	1.31E-04	5.15E+01	4.49E-01
	11KHz	1.80E-04	6.16E-05	0.00021643	1.20E-04	4.97E+01	4.33E-01
	12KHz	1.65E-04	6.64E-05	0.000200247	1.11E-04	4.77E+01	4.15E-01
Diode	Frequency	Pin_converter	PCLK	Pin_Source	P_out	Converter Efficiency	System Efficiency (measured at the Source)
RB706F-40(mouser)							
	7KHz(a 200n)	2.57E-04	3.81E-05	0.000302907	1.68E-04	5.70E+01	4.92E-01
	8KHz	2.38E-04	4.69E-05	0.000279587	1.59E-04	5.56E+01	4.86E-01
	9KHz	2.16E-04	5.29E-05	0.000254843	1.44E-04	5.34E+01	4.67E-01
	10KHz	1.97E-04	5.80E-05	0.000234179	1.31E-04	5.15E+01	4.49E-01
	11KHz	1.80E-04	6.16E-05	0.00021643	1.20E-04	4.97E+01	4.33E-01
	12KHz	1.65E-04	6.64E-05	0.000200247	1.11E-04	4.77E+01	4.15E-01
Diode	Frequency	Pin_converter	PCLK	Pin_Source	P_out	Converter Efficiency	System Efficiency (measured at the Source)
RB480Y-90(mouser)							
	7KHz(a 200n)	2.15E-04	4.35E-05	0.000279876	1.68E-04	6.49E+01	5.19E-01
	8KHz	2.18E-04	4.66E-05	0.000251038	1.35E-04	5.11E+01	4.55E-01
	9KHz	2.01E-04	5.05E-05	0.000227633	1.22E-04	4.85E+01	4.38E-01
	10KHz	1.77E-04	5.57E-05	0.000208513	1.11E-04	4.76E+01	4.19E-01
	11KHz	1.73E-04	6.04E-05	0.000192442	1.01E-04	4.35E+01	4.01E-01
	12KHz	1.44E-04	6.44E-05	0.000178928	9.38E-05	4.51E+01	3.86E-01

Figure 3.27: Diode Efficiency across the frequency range.

As can be observed on figure 3.27, the diodes that provide the best efficiency for the converter are the RB706F-40 series or the RB705D series either one of them since they have very similar characteristics regarding breakdown voltage and parasitic capacitances, as well as similar costs, however, the RB705D series seems to be easier to acquire, since there are more suppliers that stock them and it appears to be more of them in stock.

But later on in this thesis, the economical aspects of mass-producing this converter will be presented and analysed and more information about component availability will be presented. All the diodes are Schotckky diodes, since these present a better response for this circuit, although they don´t have such large breakdown voltages, they react quicker to voltage comutations, and generally speaking, have substantially less parasitic capacitances on the PN junction.

As can be seen in figure 3.27 the efficiency of the converter is between 50 and 55% for the optimum frequency range. Which is very good for this type of circuit given the extreme characteristics that it needs to work under. Unfortunately the efficiency of the whole circuit, the ELMH plus the converter is not that high it is around 1 to 0.5% but given that this circuit uses reactive power that is otherwise wasted and is always available as long as there are other devices around that need to be powered, it is always an interesting alternative to exploit them, as long as the production costs are small enough for it to be viable.

Chapter 4

Controller Implementation

4.1 Controller Study

In order to have a fully functioning buck converter there is the need to use a controller circuit, in order to regulate both the frequency and the duty cycle of the converter. In the beginning, these types of converters would receive a linear On/Off control algorithm, but those types of algorithms had problems because these circuits have many different variables and noise sources from the outside, therefore over time there was the need to develop more robust control thecniques[37]. There are a number of different topologies and algorithms in order to achieve this, generally speaking, there are two great families of controller type circuits, current based controllers or voltage based controllers [6], both with different pros and cons and different ways of being properly used. Some of those algorithms and control techniques are the Bat algorithm, the PID controller, the Fuzzy Logic Controller or sliding mode control [37], some of these algorithms are presented and analyzed in the sections that follow.

In our particular case, since the circuit was meant to work in DCM mode, there was the need to build a controller circuit that could operate in this regime thus being able to not only control the duty cycle as well as the width of the Power Width Modulation (PWM).

4.1.1 Different Control methods

For this type of converter, usually the most common type of controller circuit is the single loop voltage mode controller assisted by a PID controller. This type of architecture presents some drawbacks as it is reasonably inefficient and it performs poorly under load variations such as the ones encountered during the charging process of a supercapacitor[10].

Some of the topologies that will be presented and analyzed were the PI and PID controllers, as well as state feedback controllers, although these generally tend to have a poorer performance for small and limited power applications [19] such as this, therefore, other types of converters were analyzed such as hysteresis controller, sliding mode or boundary controller, as well as VCO oscillator based controllers.

One of the proposed topologies from [10] is the use of both voltage and current for the controller input combined. In this case, two different control loops would be used such as an outer voltage control loop and an inner current control loop with both the voltage and current dynamics governed by:

$$L * i_L(t) + v_0(t) = d(t) * v_i(t) \tag{4.1}$$

$$C * v_0(t) = I_L(t) - \frac{v_0(t)}{R} \tag{4.2}$$

As can be seen on 4.1 and 4.2 this method is based on the time evolution of the circuit, starting from the initial voltage and after that, it takes the natural tendency of the circuit in order to see how it evolves and from that feedback, it makes small adjustments to the duty cycle[6] and [10]. The major disadvantage of this topology is that although it is very efficient and has a very fast transient response, it requires two completely different control loops which represent an augmentation of the number of components to be used in the circuit, which translates into an increase of current and power in order to feed the control circuit, as well as the relatively high number of components means that this technique cannot be used in this particular application, since although it is very efficient it is also very power hungry from a controller point of view and it requires a lot of different components which would raise the price of each particular circuit.

Another interesting topology would be the use of Peak Current Control[24], in this technique the output current of the converter is used as a feedback signal and the objective is to maximize the current that circulates through the load in order to obtain maximum power output. This method is very interesting for battery charging applications, although it suffers from subharmonic oscillations especially in very high duty cycles[24], this is not the case in this converter since our circuit operates with a very small duty cycle. The major drawbacks in this particular application for this technique are that although it is a very robust technique it requires a lot of hardware such as a PI controller and therefore an integrator circuit. In such a limited power supply circuit, such as this one, this topology cannot be used.

A third possible implementation algorithm for the controller circuit of the converter was the use of a Sliding Mode Controller [42]. In this topology a PWM approach is used in order to regulate the width of the control pulses to the circuit and as such to vary the duty cycle of the converter. in this topology of converter, there are two sets of state-space equations in order to keep the controller working properly. From 0 to DT:

$$\frac{di_l}{dt} = \frac{1}{L} * V_d \tag{4.3}$$

$$\frac{dV_0}{dt} = -\frac{1}{C} * (\frac{V_0}{R}) \tag{4.4}$$

and the other from DT to T:

$$\frac{di_L}{dt} = \frac{1}{L} * V_0 \tag{4.5}$$

$$\frac{dV_0}{dt} = \frac{1}{C}(-i_L - \frac{-i_L}{-\frac{V_0}{R}}) \tag{4.6}$$

As can be perceived from the equations presented above, the mathematical model on which this topology relies upon is better suited for the CCM mode of operation, since there are only two stages of operation, one based upon the time that the converter is turned on and the other based upon the time the converter is switched off. As it was previously studied for this application it was found that the converter should be able to cope well with the DCM mode of operation since this was the mode of operation better suited for this energy harvesting application.

4.1.2 DCM Specific Control Methods

As it was previously analysed, the primary advantage of using a Buck converter working in DCM is that the parasitic capacitances that would dissipate a lot of power in CCM now will have their effects greatly reduced since those parasitic capacitances won´t have to be charged and discharged so many times [17] [22]. Now the problem is that the converters operating in this mode will need a different type of control unit, one that allows not only to control the width of the control pulses, also known as the duty cycle but also to control the frequency of commutation, also know as the length of time that the current inside the converter remains at 0.

One of such methods is the Zero-Voltage-Detector (ZVD), basically, this method uses a comparator to check when the voltage in a certain stage of the circuit, usually at the input, and letting it tend to a certain value, then leaving it there for a certain amount of time until the controller activates the circuit again. By controlling this amount of time at which the voltage from the circuit is left at the same value as a reference voltage, the frequency of commutation of the converter can be adjusted [22]. The main drawback of this type of implementation is that it consumes a lot of power feeding the comparators and that it has a lot of latency to respond and usually is very slow due to all the circuitry through which the electrical signals have to be passed through until they operate the switches. Although in [22] an interesting topology for the ZVD is proposed which makes the latency issue negligible, by using a pre-amplifying stage.

4.1.3 Chosen Controller Architecture and Results

For this particular case we needed a way to generate non-overlapping square waveforms, or in case of using only one transistor a simple square waveform. One way to do that is through cross-coupled logic gates. In that approach, the master clock signal would be split into two different signals and each would be fed to a chain of cascaded NAND logic gates and logic inverters. From each of the gates the outputs would be cross-coupled back into the inputs of the next stage gates, thus generating a non-overlapping clock signal from the delayed response from the gates themselves [51].

These sawtooth signals are then passed through an integrator circuit which generates a square wave signal, but keeping in mind that the amplitude of the sawtooth wave might decrease as the frequency increase because an integrator is also a low-pass filter, this phenomenon would happen until eventually at a very high frequency, the amplitude of the signal would be 0, some solutions for this problem are further discussed in [51].

On figure 4.1 is depicted the simplified diagram of the operating principle of the controller architecture to be analyzed.

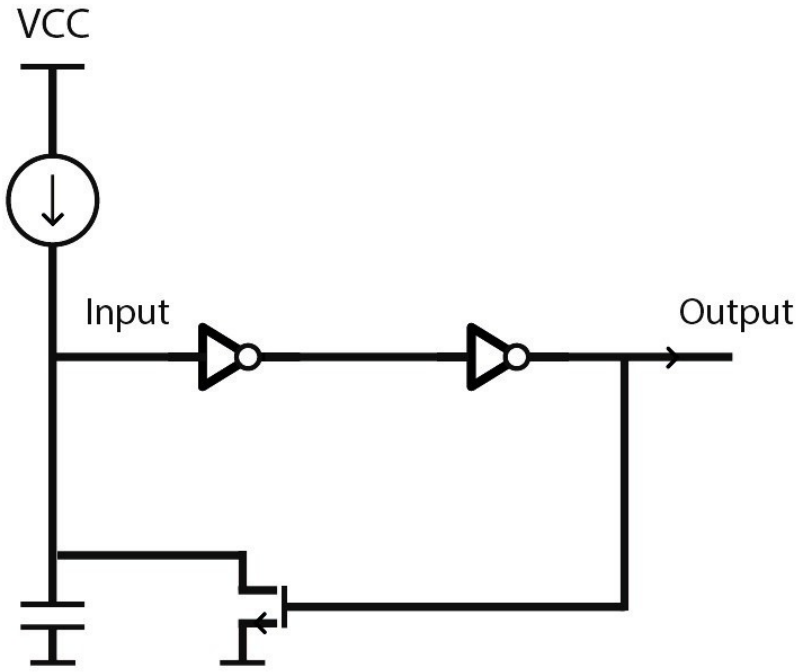

Figure 4.1: Diagram of Controller Circuit Componnents

The biggest problem with this architecture for the control circuit is that it is primarily designed to use Bipolar Junction Transisotr (TBJ) transistors and it is engineered to work with 10 transistors since this device is meant to generate two clock signals and for this converter, there will be one, the number of components could be reduced to 7, which is still a large amount, especially for TBJ transistors and so this small circuit cannot provide

all the power necessary for the circuit to work properly.

A second approach in order to have a more efficient circuit with less components was to research and test out a Voltage Controlled Oscillator (VCO) by cascading a Operational Transconductance Amplifiers (OTA) followed by a Schmidt Trigger Device. Generally speaking, these devices tend to be more power-efficient and to generate a PWM signal which happens to be basically a square wave signal, with less components and more power efficiency[43]. The only disadvantage of this circuit is that the frequency range is greatly affected by environmental conditions, such as temperature.

As the environment in a factory or plant would be fairly stable, and without very drastic temperature fluctuations, a modification of the implementation proposed in [43], based on a VCO followed by a Schmidt Trigger.

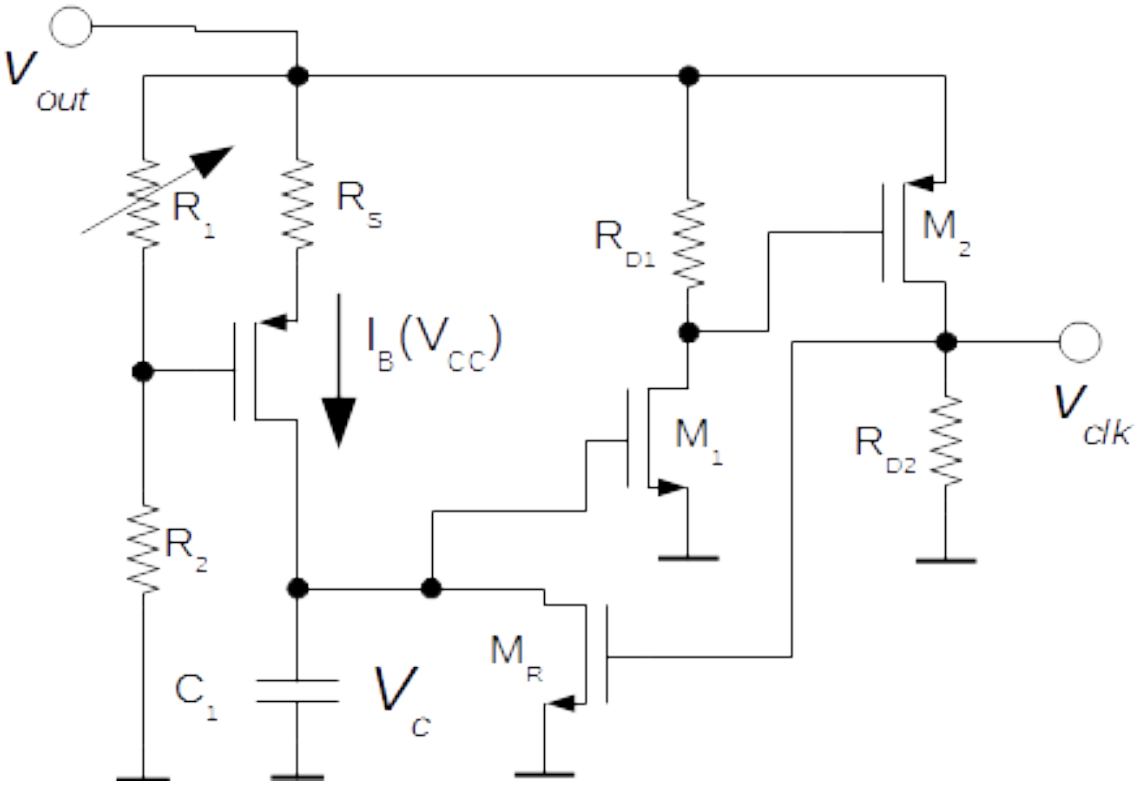

Figure 4.2: Controller Circuit Schematic.

On figure 4.2 is an example of the controller circuit used to generate the control signal for the converter. As can be seen this circuit topology has three stages the first one being a current source controlled by a potentiometer defined by R2 and R3, the total value of these two resistances can be adjusted throught the parameter x up to a maximum of 1000KΩ. By adjusting this parameter the output current of the source of the transistor M1 can be adjusted. This is a very important parameter, because of mainly two things, a larger output of current means that the circuit requires more power in order to work and also the frequency of the clock signal generated by our VCO is controlled and can be adjusted by varying the x parameter and the value of current that it puts out, because by

adjusting the value of the output current and the capacitance of the capacitor C1. The time the capacitor takes to be charged generates a sawtooth wave that depends on the value of such capacitor and the respective ammount of current, therefore ideally it should be chosen a small capacitor, which charges quickly whithout a large ammount of current since the power supply available to this circuit is relatively limited.

In the second and third stages of the controller we can observe the Schmidt Trigger device that actually works as an oscillator and develops the clock signal to be used.

The second stage of the controller is made by the transistor M2, M4, and the resistor R4, in this stage the there is another inverter used to change the logic value of the signal coming from the first stage. The third stage is made up by resistor R5 and transistor M3 this creates yet another inverter which in term inverts the logic value from the output of the second stage of the inverter. At last, this output value is inverted for the last time and fed back into the circuit. Now the output is a 1 which inverter will generate a 0 on the circuit output and after the final inversion will be another 0 on the input and so on and so forth. The ratio at which this inverter works and how fast it switches between logic values of 0 and 1 is defined by how fast the C1 capacitor can charge and discharge its voltage. Therefore by adjusting the supply of current to this capacitor through the current source made by the potentiometer, there can also be used the value of the capacitor to change the charging or discharging rate and frequency of the commutation.

This circuit was first implemented using TBJ transistors but these had a problem, that the voltages needed for propper operation were very high and required a large base current, which in turn forced a very high value of power to be fed to the controller circuit, so an effort was made based on the work of [45] to produce the same circuit using both N-MOS and P-MOS transistors which require lower voltages in order to function properly and since they work based on field effect, the power savings from the base currents were significant, as an example, with TBJ transistors, the power required to supply these circuits was around 300 to 500mW and by using MOSFET technology the power required was reduced to some hundreds of microWatts.

The results of the given controller are presented below as it was first tested isolated from any other circuitry and using an ideal 8V voltage supply, the results are displayed in the images below.

	Controller		
	R5=50K	voltage input 8V	
x parameter	frequency	power dissipation (W)	pulse width
0.1	11.822222KHz	3.69E-04	3.76E-05
0.2	10.44962KHz	3.29E-04	3.07E-05
0.3	8.18KHz	2.73E-04	3.76E-05
0.4	6.939KHz	2.36E-04	3.45E-05
0.5	5.232KHz	1.90E-04	2.82E-05
0.6	2.9018182KHz	1.47E-04	2.82E-05
0.7	1.68KHz	1.04E-04	2.82E-05
0.8	N/D	N/D	N/D
	Controller		
	new schematic with transistor(c=250p)	voltage input 8V	
x parameter	frequency	power dissipation (W)	pulse width
0.1	10.1KHz	4.15E-04	5.18E-05
0.2	8.5KHz	3.63E-04	4.50E-05
0.3	7.84198KHz	3.13E-04	4.20E-05
0.4	6.4905414KHz	2.64E-04	3.70E-05
0.5	4.91KHz	2.11E-04	3.87E-05
0.6	3.1969KHz	1.58E-04	4.23E-05
0.7	1.4896KHz	1.06E-04	3.86E-05
0.8	N/D	N/D	N/D

Figure 4.3: Controller Circuit Results-1.

	Controller		
	R5=500K	voltage input 8V	
x parameter	frequency	power dissipation (W)	pulse width
0.1	7.2727273KHz	3.25E-04	1.34E-04
0.2	6.6666KHz	2.89E-04	1.34E-04
0.3	5.7142857KHz	2.53E-04	1.66E-04
0.4	5KHz	2.17E-04	2.00E-04
0.5	4.0506329KHz	1.78E-04	2.44E-04
0.6	2.8571429KHz	1.41E-04	2.78E-04
0.7	1.47096KHz	9.92E-05	2.32E-04
0.8	N/D	N/D	N/D
	Controller		
	R5=500K and c=2n	voltage input 8V	
x parameter	frequency	power dissipation (W)	pulse width
0.1	4.1558KHz	3.07E-04	2.34E-04
0.2	3.555KHz	2.72E-04	2.03E-01
0.3	2.7586KHz	2.36E-04	2.66E-04
0.4	2.519685KHz	2.00E-04	2.59E-04
0.5	2.06622KHz	1.66E-04	2.52E-04
0.6	1.3190083KHz	1.29E-04	1.97E-04
0.7	N/D	N/D	N/D
0.8	N/D	N/D	N/D

Figure 4.4: Controller Circuit Results-2.

	Controller		
	R5=50K and c=200p	voltage input 8V	
x parameter	frequency	power dissipation (W)	pulse width
0.1	25.33KHz	4.98E-04	2.73E-05
0.2	22.334456KHz	4.33E-04	2.71E-05
0.3	19.558824KHz	3.81E-04	2.56E-05
0.4	16.0240KHz	3.19E-04	2.63E-05
0.5	12.17KHz	2.56E-04	2.21E-05
0.6	8.1511747KHz	1.91E-04	2.34E-05
0.7	3.72KHz	1.22E-04	2.20E-05
0.8	N/D	N/D	N/D

Figure 4.5: Controller Circuit Results-3.

The more interesting results for the controller operation are highlighted in yellow, being either by the fact that they produce the right frequency or they require a relatively low amount of power, as can be perceived multiple testing with different values for the R5 resistor and the C1 capacitor were made but in order to obtain the best results possible,

although the larger the value of the parameter x, the less current the circuit requires and therefore the lower the power, but also the lower the frequency since there was needed a frequency of about 7KHz to 12KHz. Through meticulous testing and experiment we reached the optimum combination of R5=50KΩ, the capacitor C1=200pF and an x parameter of 0,6 to 0,7. In this configuration the circuit had 7KHz of operating frequency and power dissipation of around 150 to 200μW.

Briefly, the controller was also tested using a transistor M4 in place of the R5 resistor, creating a CMOS inverter but since these circuits operate with a very elevated input voltage, and the NMOS transistors require a low value of Vgs to turn on there was a time interval where the transistor M3 and M4 would be turned ON at the same time and pulling a large amount of current from the supply bus, raise the input power required. Therefore the solution using a transistor as a resistor had to be abandoned and replaced by an actual resistor.

The final topology of the converter is the one on 4.2, with some adjustments on the resistor R4 which was used at 500KΩ, and resistor R2 and R3 were increased to a maximum value of 5000K. Also, the capacitor C1 was also reduced in order to achieve a higher operating frequency due to the faster charge and discharge cycle of the converter.

Chapter 5

Final Assembly and Experimental Work

5.1 Final Assembly

In this section the final assembly of the entire circuit is presented and discussed alongside with the experimental results and possible drawbacks from the implementation and interaction of the various components of the entire device, the experimental results will also be presented and analysed. Below it can be seen the final circuit with the various components, and how they are interconnected.

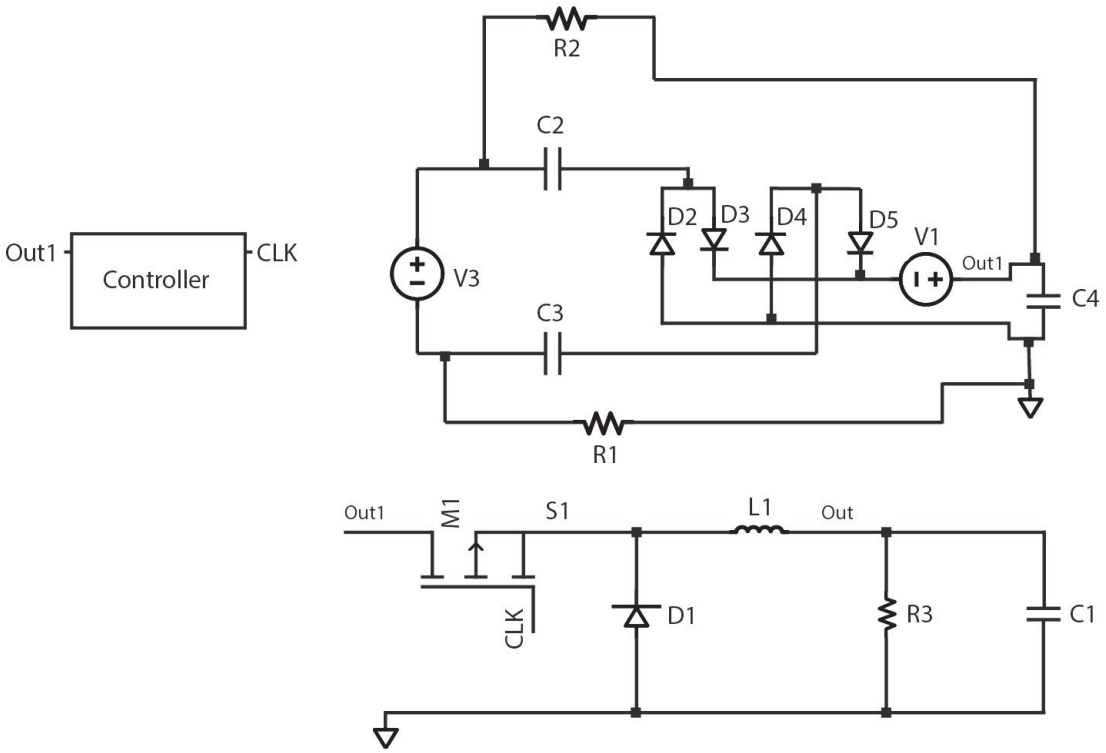

Figure 5.1: Final Assembly

In the final assembly of the circuit there were three components the main circuit of this work was the converter which was a simple buck converter using a 1mH coil and a transistor of low gate capacitance, plus a Schottky diode controlling the freewheeling part of the circuit. In order to run these simulations, the output capacitor was set at 10μ to simulate a supercapacitor at the output of the circuit. The initial simulation was tested with a resistor of very high value in order to simulate the condition of a supercapacitor at the output of the circuit with the benefit of having a faster simulation time.

Another component is the ELMH that can be seen on the top portion of the image, it was necessary to add to 1Gohm resistors between the input and output to allow the spice simulator to converge.

At last, the block shown at the top of the figure is the encapsulation of the controller circuit, previously depicted in figure 4.2. The only change that was made was the variation of the x parameter that had to be adjusted to 0.5 instead of the optimum 0.6, this was due to the fact that the ELMH can not provide the maximum amount of current needed to provide power to the controller, therefore the capacity to charge the capacitor C1 in figure 4.2, is reduced. Due to the limited amount of current available from the ELMH this in term forces us to use a lower value of X, as can be seen, by figures 4.3 and the operating frequency is also lowered well below the optimum operating frequency of 7KHz down to 1.8KHz. This results in a reduction of the input voltage from the optimum 8V down to about 4V due to the lower input impedance of the converter caused by the reduction of the operating frequency. This reduces the amount of power that can be transferred to the

supercapacitor.

5.1.1 Final Assembly simulation Results

In this subsection the simulation results of this work will be analyzed as to what they mean and the real functioning of the device from an simulation and ideal point of view.

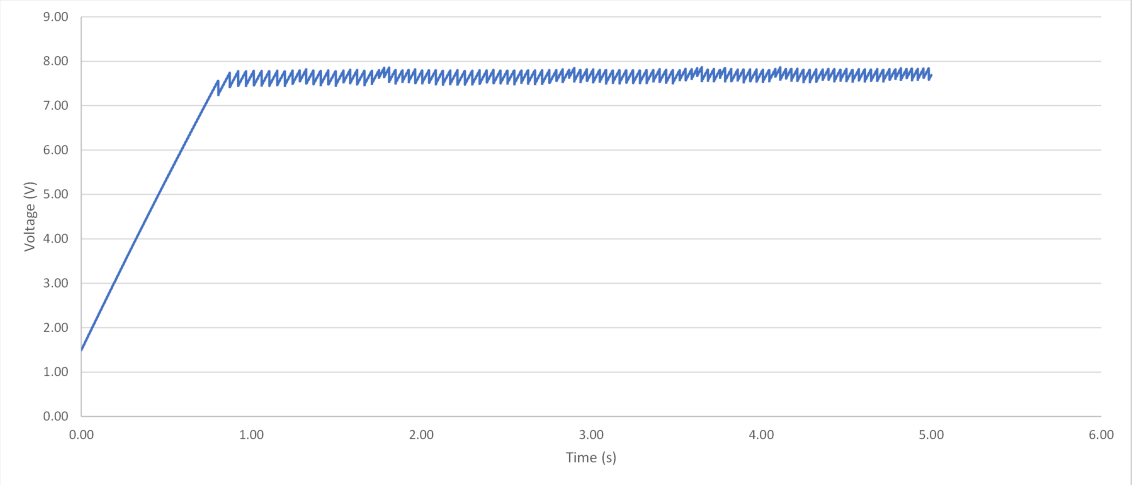

Figure 5.2: Final Assembly Results-Input Voltage

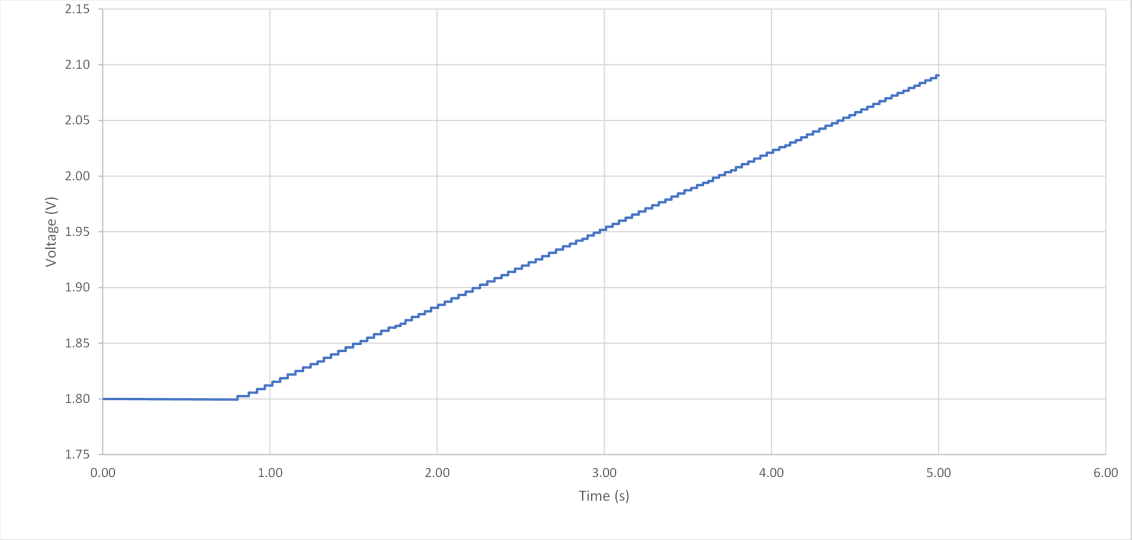

Figure 5.3: Final Assembly Results-Output Voltage

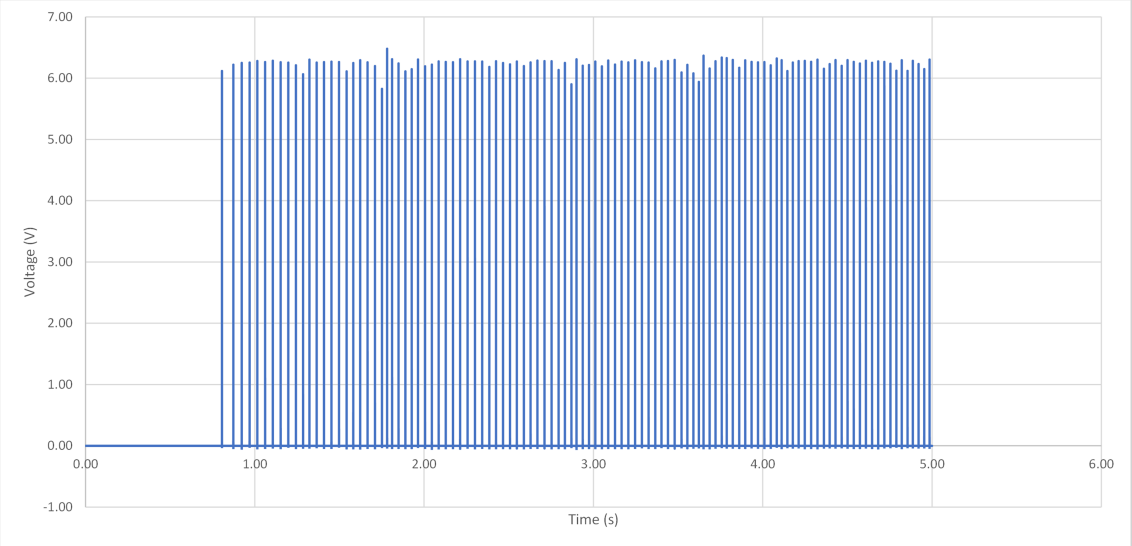

Figure 5.4: Final Assembly Results-CLK Signal

As can be observed in the figure above once the converter starts to operate the voltage from the capacitor keeps increasing steadily while the input voltage also increases but at a slower pace, the input voltage stabilizes at about 8V, while the output voltage keeps rising, in real operation what would happen is that the output voltage would be lowered as a device is connected to our supercapacitor and takes some energy harvested in it to function, if the voltage of the capacitor would rise too much without any control over it there would be placed a kill switch which could stop the conversion and let the converter die down until some of the energy of the capacitor is taken.

5.2 Experimental Work

Unfortunately although all the dimensioning and project of the circuits was done, due to the Covid-19 pandemic the access to the university laboratories and research facilities was greatly conditioned, therefore although all the components were bought there was no time to build a functioning prototype before the PCB design just as a proof of concept.

One attempt was made using discrete components and perforated cooper boards, nevertheless, this solution had to be discarded because as it was previously mentioned the components used had to have a very small dimension in order to minimize the parasitic capacitance effects. As shown in figure 5.5 the transistor used as a switch for this circuit is very small and hard to hand solder. Therefore the solution that was initially thought of was to place this transistor in a through-hole adapter as shown in figure 5.6. This solution had to be dropped out because of that said difficulty the pins on the transistor were inevitably short-circuited to each other as it was tried to solder them to the board.

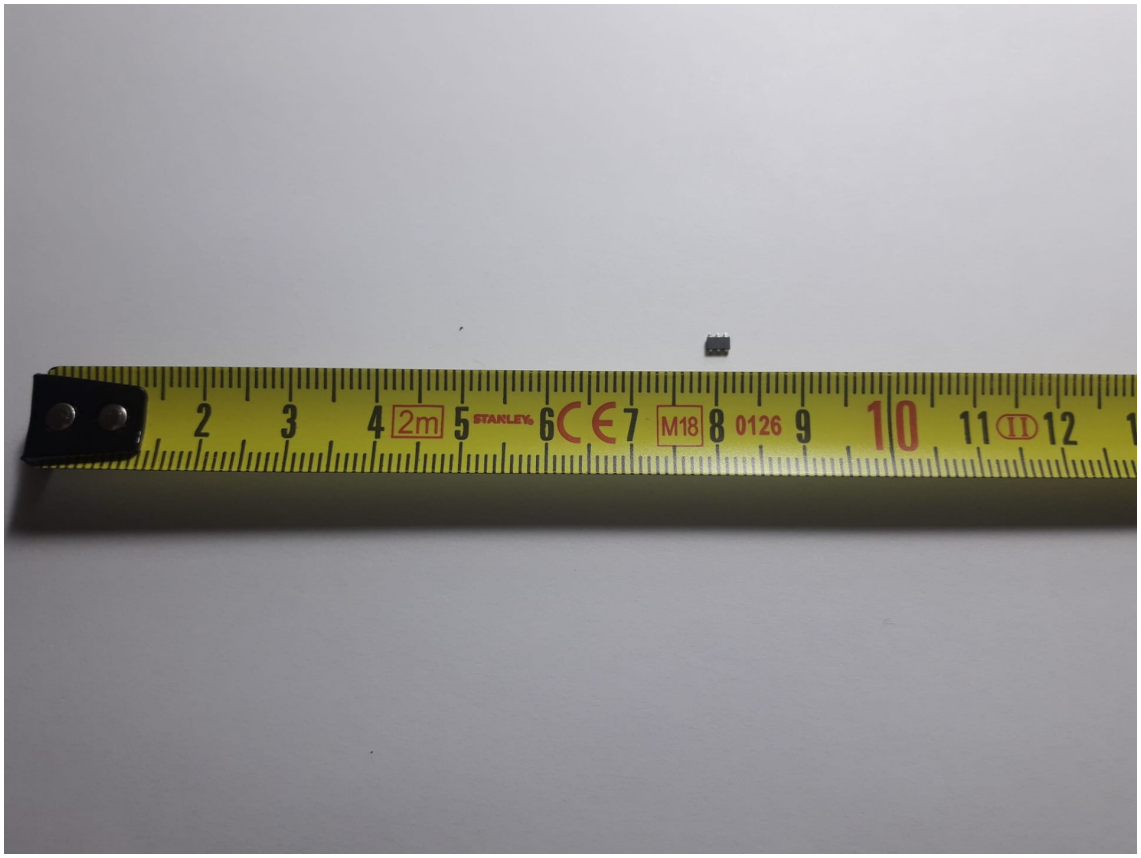

Figure 5.5: Transistor RSQ015N06

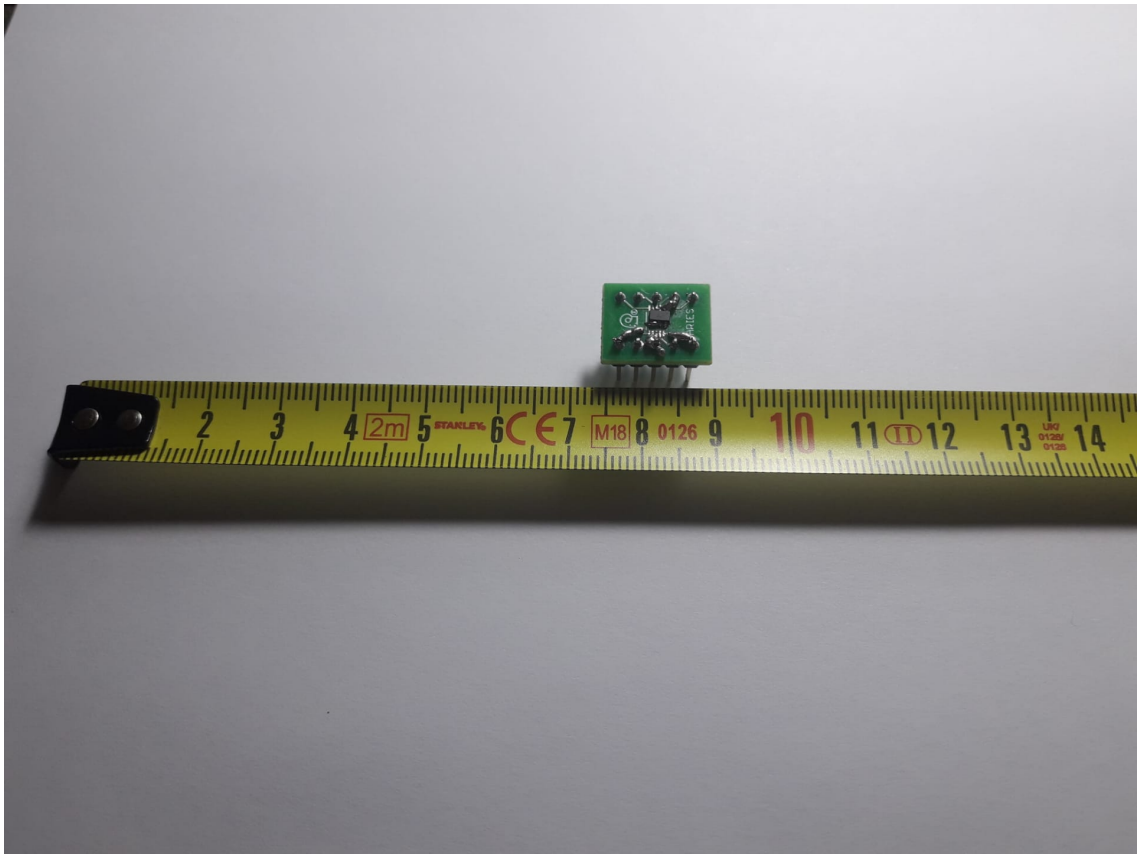

Figure 5.6: Transistor RSQ015N06-in through hole adaptor

5.3 PCB Design

This section presents the design and project of the integrated circuit and PCB project designed in KICad software.

This work was divided into 2 different circuits the converter and the controller circuits, in this case, both printed in different PCBs. As it was studied in [5], the integrated circuits Integrated Circuits (IC), show very different results when they are tested and implemented separately and then when they are put together in a unique PCB because the increment in noise and interference from electromagnetic effects from the board itself and from other components present in the board affect and interfere with the various components especially given the fact that the controller has a lot of commutating devices which generate a lot of ripple in both current and voltage. Since this converter is very sensitive to parasitic effects thus the decision to design the converter and the controller in two different circuits, might be problematic because it allows for undesired effects and parasitic effects between circuits and makes for a more complicated optimization problem when trying to make the best layout for the various circuits such as described in [29]. This was a calculated risk in order to have less parasitic effects between the various components of the circuit in exchange for a more complicated optimization problem in order to make the connection between both PCBs.

Another problem that might arise in the practical implementation of these devices is the handshake between different technologies as referred in the work of [5] and types of devices is the appearance of noise and slight degradation of efficiency from the fact that two different technologies are used such as through hole for resistors and some capacitors jointly with SMD for transistors and diodes. This poses a problem because the large resistors and large defects of the soldering might interfere with the other very small components and also degrade the efficiency of the circuit because of joule loss due to imperfections on the solder that might cause it to heat up and dissipate energy. These through-hole components were used because they are cheaper and easier to hand-solder since this is just a prototype. In future versions of this work, it is highly recommended that all the components might be changed to SMD.

Another consideration that was analyzed while developing these PCBs was the heat dissipation. Since the energy harvested is in the order of micro watts, in order to provide for sufficient heat dissipation an adequate spacing between the various components must be assured according to [12]. After a brief analysis it was concluded that in this circuit the heat dissipation did not impose a serious problem because the current and power levels are very low. Another two methods that might be used to improve heat dissipation characteristics are using special solder paste with better heat dissipation characteristics and/or leaving thermal vias for the same purpose, because of their increased complexity associated costs and technical difficulty it was decided that these methods would be implemented only if necessary on a further phase of development and optimization.

Finally one last consideration to be taken into account was the width of the PCB tracks. The default width of the software was substantially reduced due to the fact that the current circulating in the circuit was very small and thus did not need such a large track. This has the advantage that consumes fewer resources manufacturing the PCB and also the biggest advantage is that there are smaller parasitic capacities between the tracks on the PCB and thus an improved efficiency of the circuit.

Below in figures 5.7 and 5.10 there is the PCB design Silk layer for both circuits with the best possible component arrangement and the PCB tracks designed.

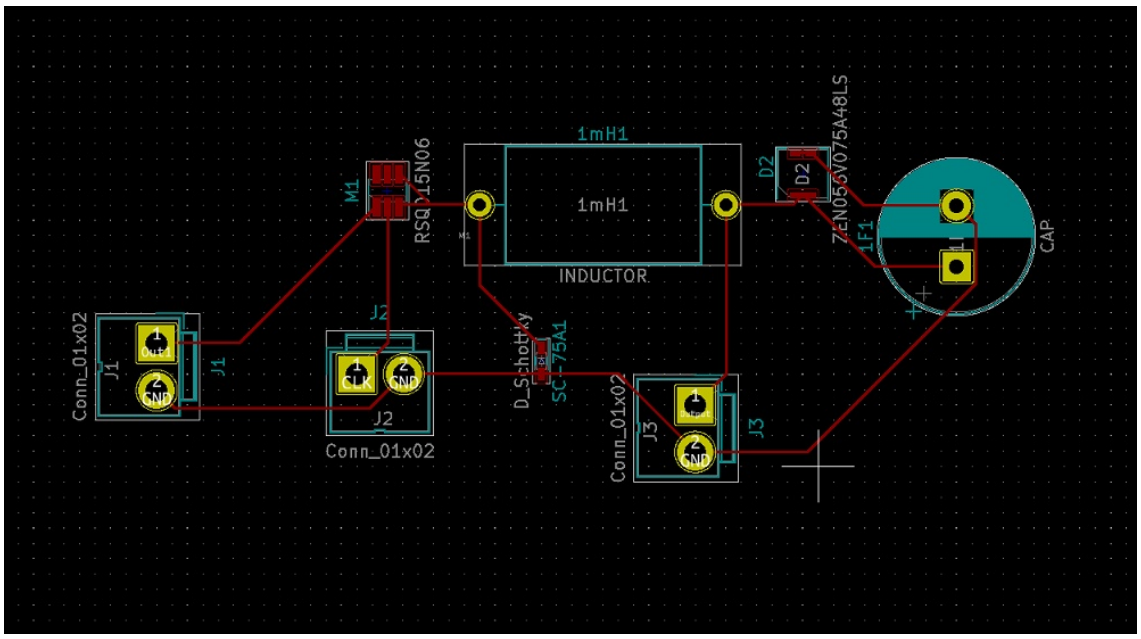

Figure 5.7: PCB Converter Silk Layer

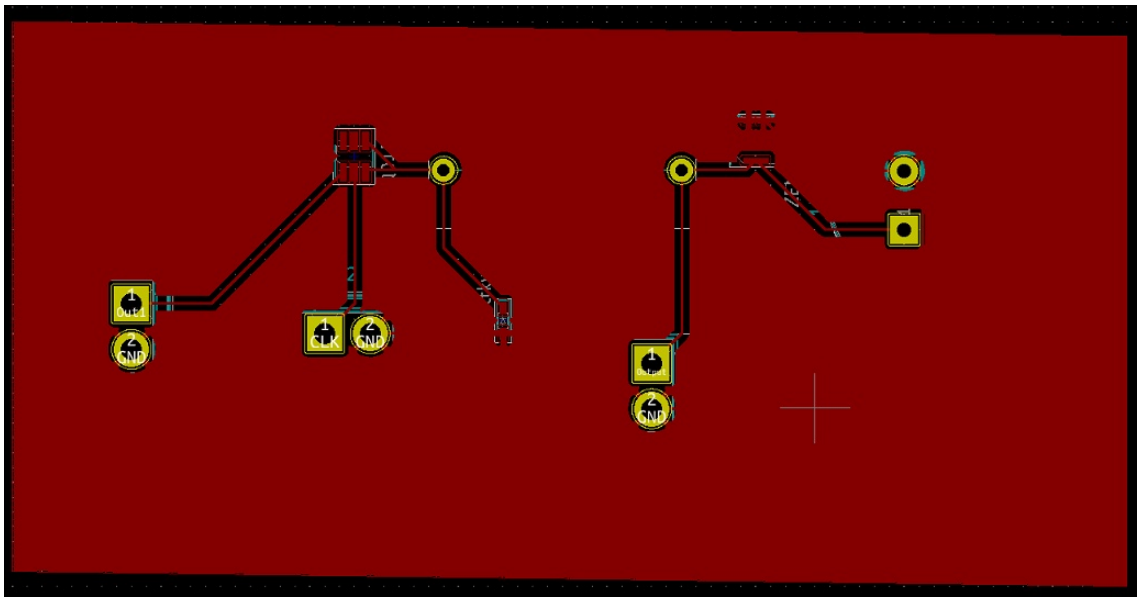

Figure 5.8: PCB Converter with Ground Plane

In figures 5.8, 5.9 for the converter and 5.12 and 5.11 for the controller are depicted the PCB printed board as well as the groundmass plan for both boards. This plan was made in two layers one at the bottom of the board depicted in green and another on top depicted in red. These are very important because the current flowing in the tracks of the PCB generates a magnetic field that might originate parasitic currents that would affect and interfere with the good functioning of the other components on the boards. Therefore with this mass plane, the whole substrate will be at the same potential and be able to compensate the induced parasitic currents from the passing of current through

the PCB tracks.

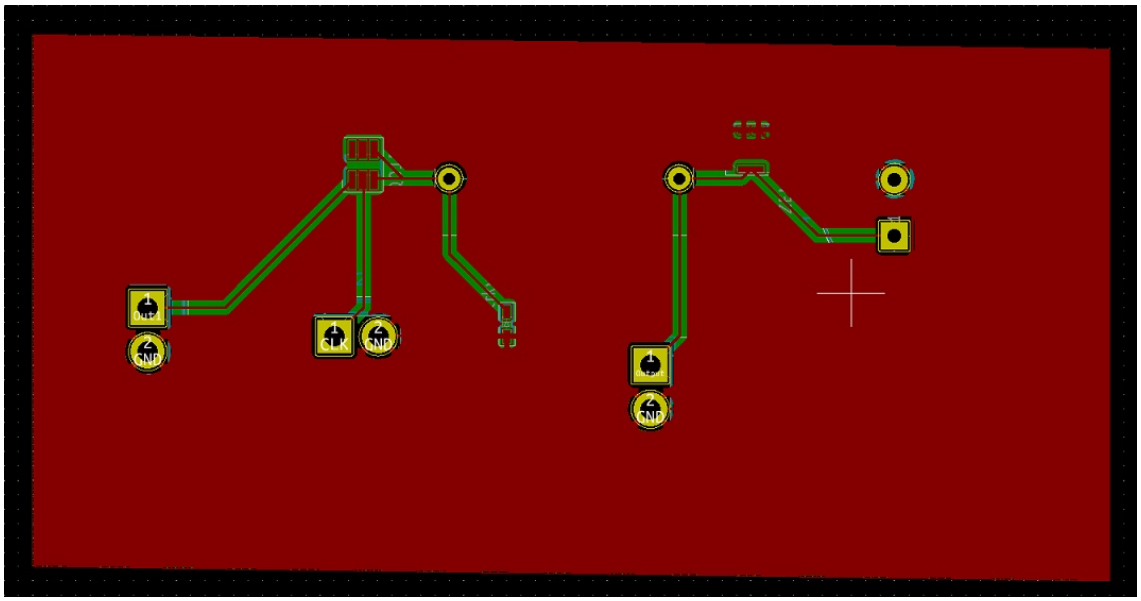

Figure 5.9: PCB Converter with Ground Plane

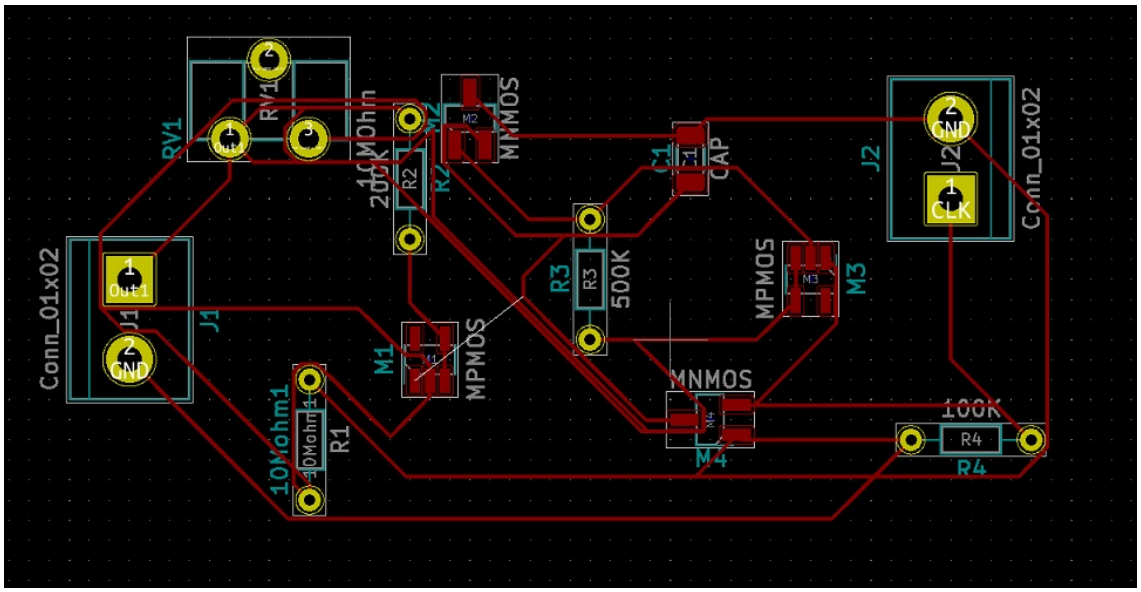

Figure 5.10: PCB Controller Silk Layer

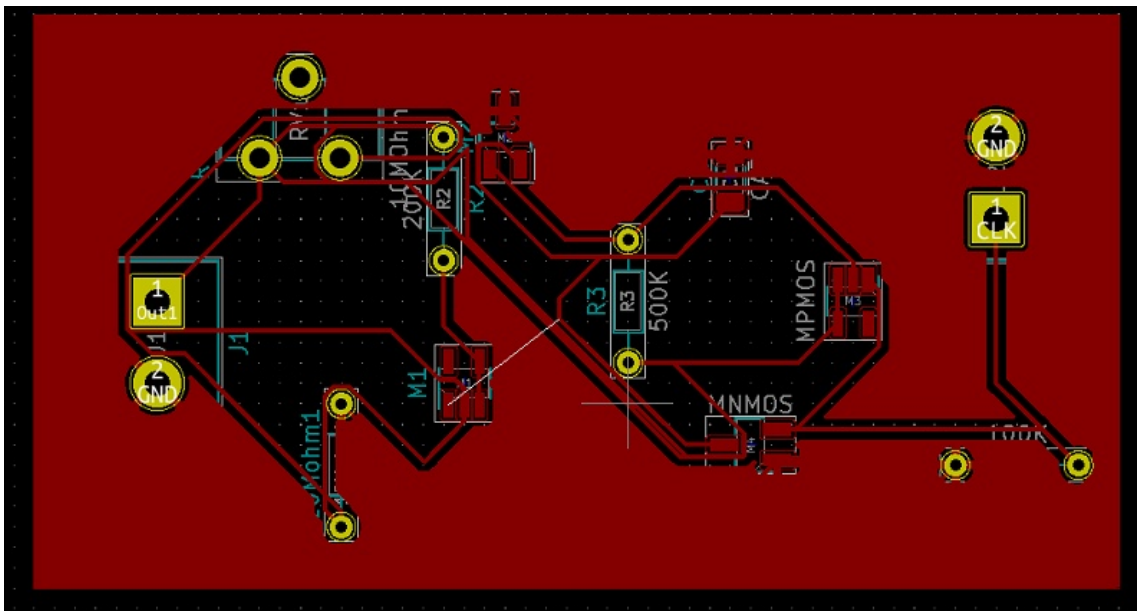

Figure 5.11: PCB Controller with Ground Plane

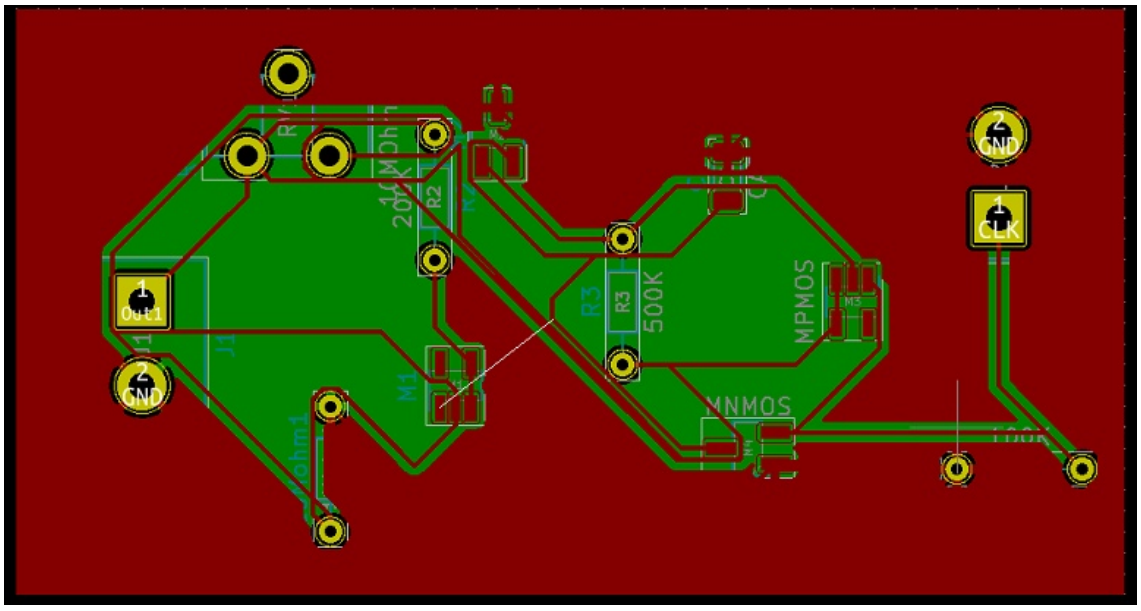

Figure 5.12: PCB Controller with Ground Plane

On images 5.13 and 5.14 there is depicted the 3D models of both the converter and the controller circuit respectively. As can be observed the components are welded on the board and the connectors to the boards are made of simple 2 jack pins one for the input or output signal and another one for the ground reference. These jacks in particular were chosen for the fact that the pins on them are relatively close to each other which reduces and improves upon noise and interference between the two signals.

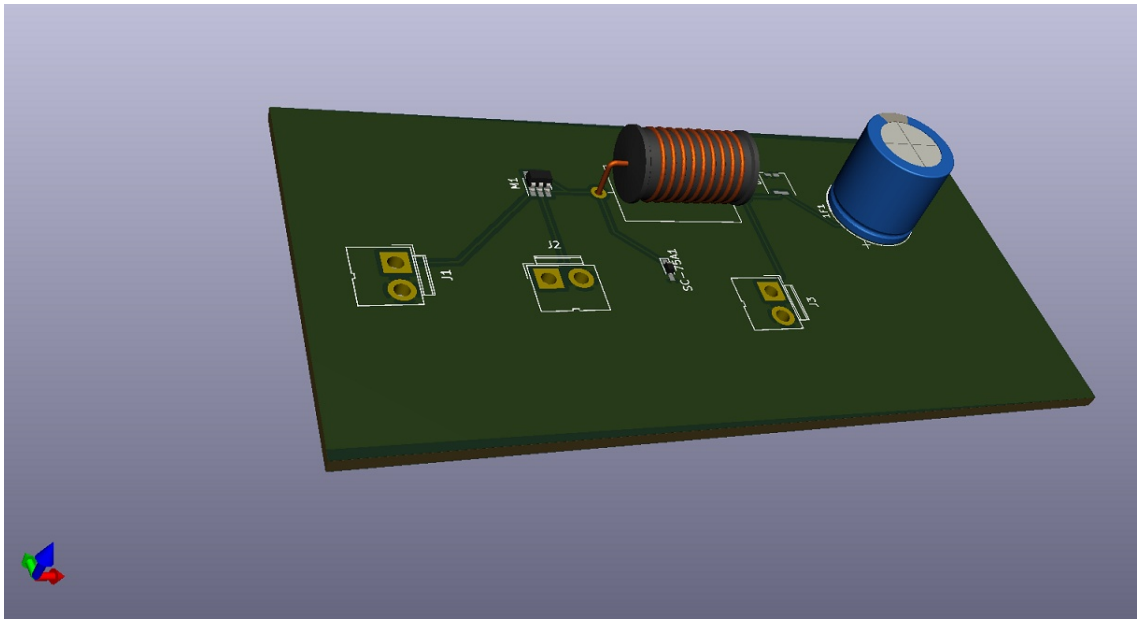

Figure 5.13: PCB Converter Circuit 3D Model

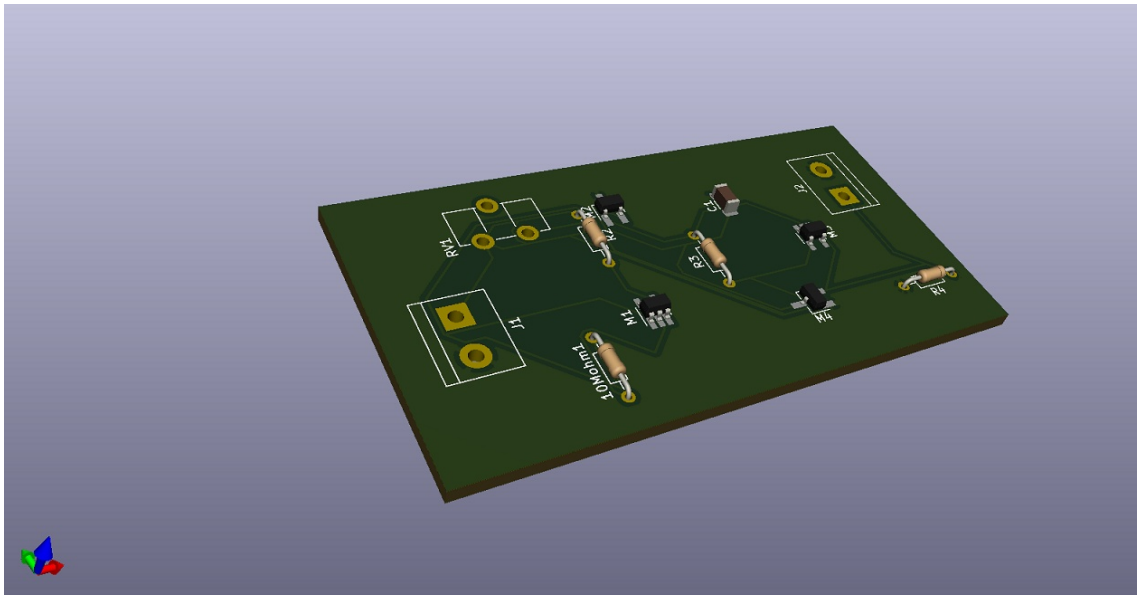

Figure 5.14: PCB Controller Circuit 3D Model

In conclusion both circuits were designed according to the principles and considerations aforementioned using KICad software as previously mentioned. This software facilitates greatly the conception and optimization process for the development of PCBs and as can be seen in the above figures the output and input signals for these boards are made by normal 2 pin jacks to which the exterior components will be hand soldered using a single coper wire. The layout and disposition of all other components was made attending to the aforementioned considerations and technics.

Chapter 6

Conclusions and Future Work Prospects

Along this chapter some final conclusions about this work shall be taken into consideration such as the multiple technical and technological solutions necessary in order to produce this device as well as the economical aspects of the various solutions and how good and profitable would they be when the technical aspects are set against the economical one. Finally, there are some advice and possibilities listed as to what could be done towards a better solution and further development of this device and this technique of harvesting and using reactive power in Industry 4.0.

6.1 Cost and Implementation Analysis

In order to make this a viable option from an economical viewpoint, there is a need to make this circuit as cheap as possible, in spite of the technical implementation chosen and the technical solutions at which the conclusions of this work arrived. Therefore in this section a small presentation about the price of the components and how much would it cost to implement this circuit in practice and at a large scale in order for it to be viable in the industry.

The intent of this device from an economical perspective was always to be a low-cost solution since the ELMH is intended to be a scavenger circuit for reactive power within the electrical grid, therefore the idea was always to work and develop a device that could work properly but also would be cheap to manufacture and produce in a large scale. During the experimental part of the work two different types of technologies were studied, both discrete components and PCB design.

cost of buck componnents componnents	Number	price per unit (unit)	total price (mouser)	comentaries
inductors (1mH)(NLFV32T-102K-EFT)	1	0.29 €	0.29 €	
transistors(DMT15H017LPS-13)	1	0.42 €	0.42 €	
diodes(V5PA22-M3/I)	1	0.37 €	0.37 €	
source capacitor (CGA5L3X7R2E104K160AA)	1	0.39 €	0.39 €	
super capacitor (0.1f)(EDS104Z5R5C)	1	2.11 €	2.11 €	
sum	-	-	3.57 €	-

Figure 6.1: Component Cost for the Converter

cost of controller componnents componnents	Number	price per unit (unit)	total price (mouser)	comentaries
RHK005N03_NMOS	2	0.31 €	0.62 €	
BSS84_PMOS	2	0.33 €	0.66 €	
potenciometer	2	1.19 €	2.38 €	
C0805C101FCGACAUTO (100pF capacitor)	1	0.47 €	0.47 €	
multiple resistors	4	0.15 €	0.60 €	
sum	-	-	4.73 €	-

Figure 6.2: Component Cost for the Controller

As shown above a cost of implementation analysis was made and the values obtained were the ones shown above in figure 6.1 and 6.2, the price of the controller circuit is even higher than the price of the converter, this is due to the fact that it has more components and especially two potentiometers which are very expensive components in this type of circuit because they need to be very large and also have a high degree of precision.

It can be concluded that the total cost of the circuit would be €8,3. The goal along this work was to develop a circuit with the necessary quality but also that was was cheap enough to produce a feasible financial solution, ergo it was set a threshold limit to develop a circuit that was below the €10 mark which was achieved. Also bear in mind that these costs do not take into account the man-hours and infrastructure necessary for the production and assembly of the circuits, only the cost of the actual components, but since these components were bought in a regular electronic store in this case Mouser Electronics, it is expectable that if these same components were to be bought directly from the manufacturer and in large quantities the components price and shipping would reduce in at least 50% which means that each circuit would have a components cost of €4,15. This seems a very interesting solution and well within the economical goals of this project for the technical specification of the circuit.

6.1.1 Discrete Components Analysis

The discrete components have an advantage over PCB design since they are easier to acquire and therefore to manufacture and replace parts within the circuit. However they proved to be less technically efficient as previously discussed and happen to make for an overall more expensive design of the circuit, some numbers and figures are as follows.

Another major problem with discrete components is that for this particular circuit in order to minimize losses by charging parasitic capacities in a variety of components very

physically small components had to be used. The problem with such devices is that they are very complicated to solder to a perforated board and they are very difficult to make the connections to each other. At last, the perforated boards on which these components are soldered would induce very high levels of noise and disturbances into the circuit, so it was estimated that even if the circuit was to work with these devices it would consume a very large amount of power much larger than the actual PCB version and much more than could be supported in this type of application.

Therefore the discrete component circuit was abandoned in favour of a PCB prototype.

6.1.2 PCB Analysis

In this subsection is presented the results from a small procurement study that was done in order to print the designed PCB boards analyzed below, in figures 6.3 and 6.4 is presented the specification of the board to be printed. And figures 6.5 and 6.6 are displayed the costs of implementation of such boards and the time they will be taken to produce.

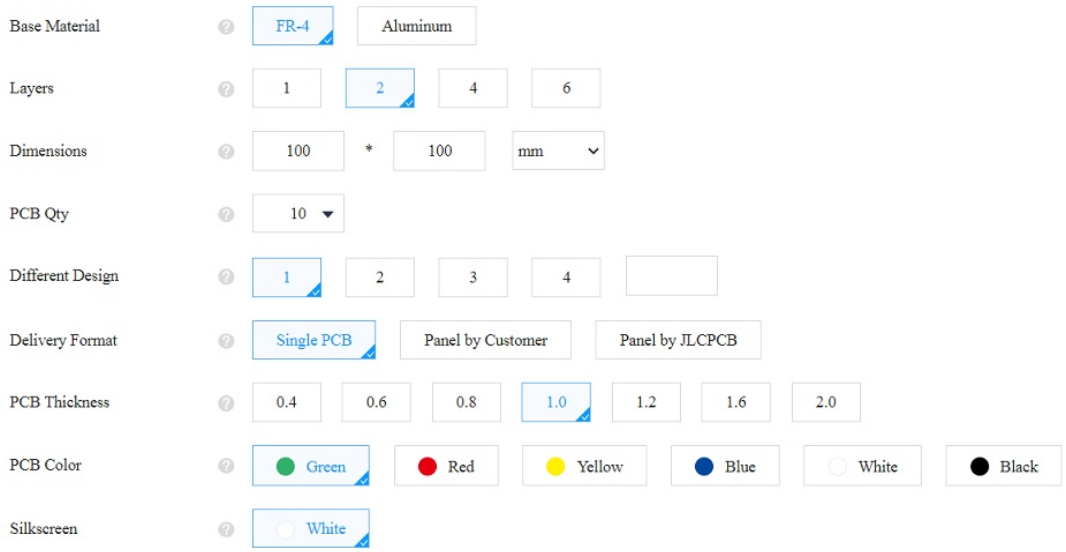

Figure 6.3: Specification of the printing of the PCB

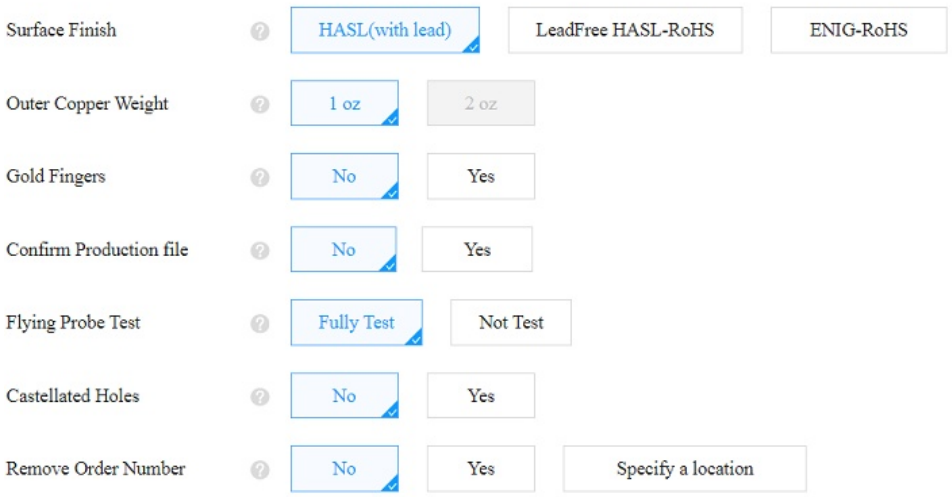

Figure 6.4: Specification of the printing of the PCB2

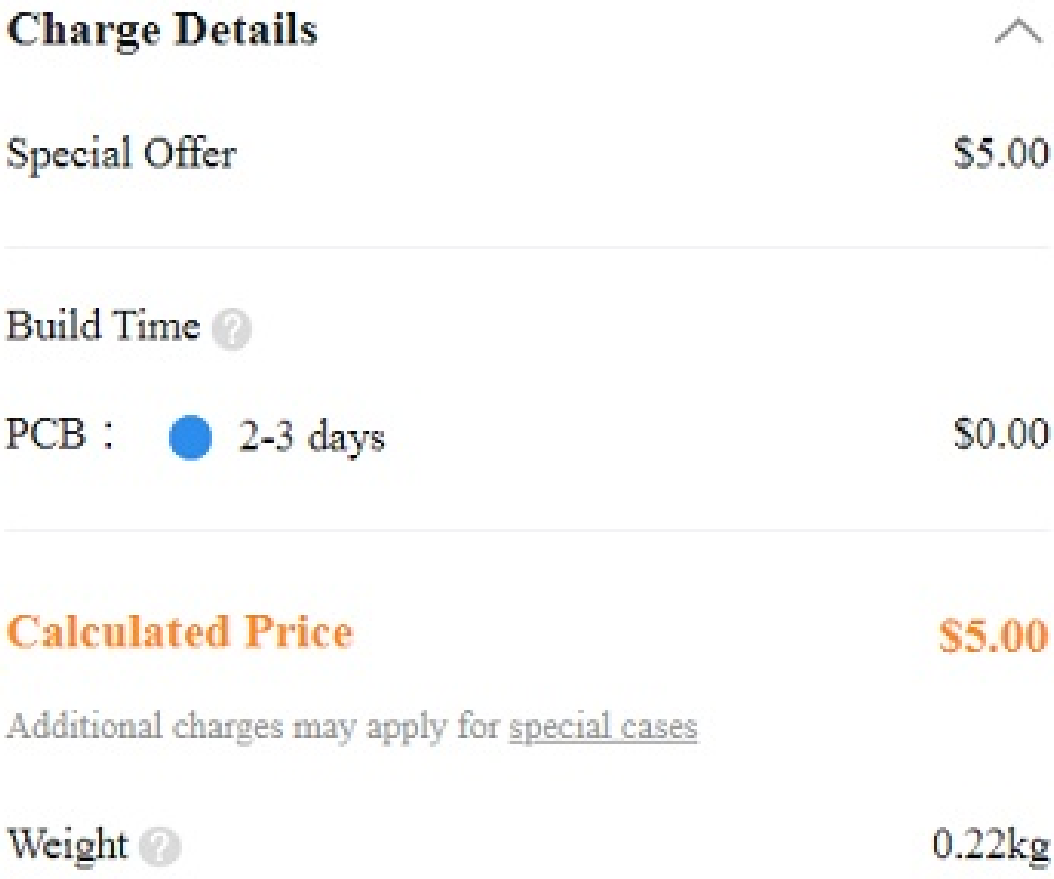

Figure 6.5: Printing Costs for a sample of 5 pieces

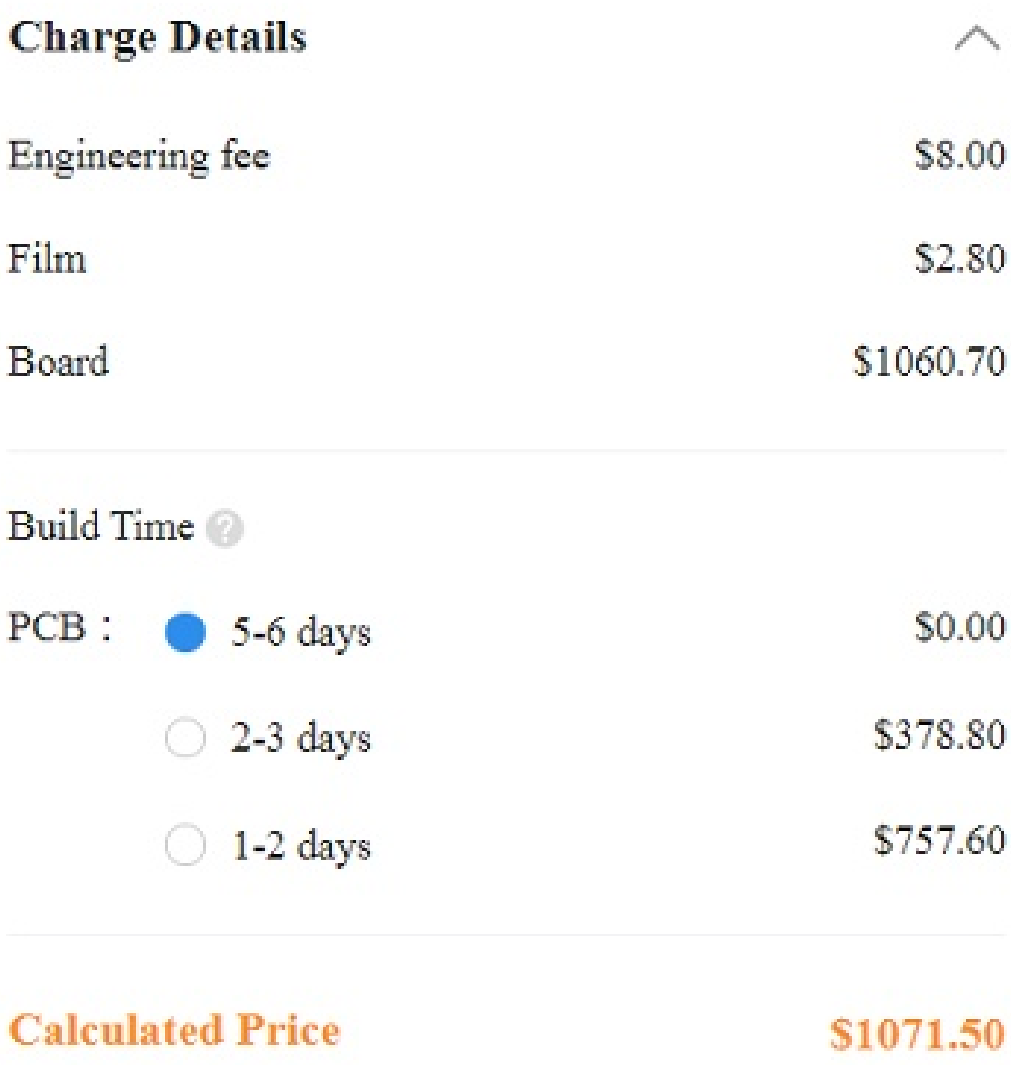

Figure 6.6: Printing costs for the maximum production setting of this manufacturer, 2000 pieces

As can be observed from the above figures the cost of production is very low, given that the 5 piece sample would cost about 1 dollar per unit but the 2000 piece order would take slightly over 50 cents per board, this cost would be added to the components cost already presented and analyzed on figures 6.1 and 6.2.

6.2 Final Conclusions

Along this work it can be concluded that this circuit works and is able to harvest energy from the reactive power of the grid and transfer it into a supercapacitor in order to have a small amount of energy available to power up small sensors or actuators. Although because of multiple technical difficulties and especially the presence of various parasitic capacitances and unwanted effects, the efficiency and the amount of energy that could be

transferred is substantially lower than the one first thought to be available. Especially the input impedance of the circuit could not be brought up to a very high value and because of all the parasitic capacitances and some compromises had to be made on the choice of the converter because the one that was supposed to be used, the two stages cascaded buck converter presented two capacitances paralleled to each other which behaved like a short circuit of the buck and when it attached itself to the previous circuit it would lower its input impedance and therefore the output voltage of the ELMH.

Because of these setbacks a single-stage buck converter was chosen due to its simplicity in building it and in order to get the same step-down ratio we chose to use a much smaller duty cycle, than what would have been necessary with a cascaded buck. This posed some problems on the choice of the transistor because with a smaller duty cycle and a larger operating frequency which was used in order to enlarge the input impedance, this results in a very large number of cycles to charge the parasitic capacitances of the input transistor and the diode so a very small component had to be chosen which makes this circuit viable to build only in PCB design and not as a discrete components circuit using perforated boards or breadboards because it cannot be soldered properly onto them.

About the controller circuit many different architectures and implementations were analyzed both in CCM as DCM but at last the architecture chosen was a DCM solution although this poses problems in the way that it has another degree of freedom which is basically the time that the voltage across the circuit stays at 0 voltage. This disadvantage of another variable within the control loop in our case is superseded by the extra degree of freedom that it gives us which enables us to boost the input impedance of the converter without needing to either increase the operating frequency which as explained previously increases the influence of the parasitic capacitances and without the need to use larger coils which makes the circuit overall more inefficient and more expensive.

The controller solution that was used was a set of three inverters based on the Schmidt trigger configuration fed from a current source that could be controlled by a potentiometer and that would load a capacitor. The charge and discharge rate of such capacitor sets up the f requency of the commutation cycles of the inverters, and consequently the frequency of operation of the controller circuit. This controller circuit could be used in multiple different configurations but yet again since the main concern of this circuit is that it takes as little energy as possible in order to run, it was decided that small MOS-FET transistors would be used.

At last the main concern was to use a small device that could implement a voltage cut-out switch so that the output voltage of the converter never exceeds the maximum voltage of the supercapacitor.

6.3 Future Work in The Field

For future work in this area I propose that the next investigator would invest more time in practical experimental work like printing and testing the PCB boards as well as a

prototype developed in discrete components and perforated board because it would be good to test both systems and compare their results in order to validate some of the results and predictions made on this thesis.

Another interesting aspect in order to enhance the performance of this circuit would be to develop a new type of controller more efficient than this one since the cascaded inverters based on the Schmit trigger implementation happen to consume a substantial amount of power in order to charge parasitic gate capacitances of the transistors. This is particularly bad in our case due to the limited amount of energy that we can work with, especially because the controller circuit consumes about half of the total amount of power available to power up the entire system.

Also it would be very interesting to develop a controlling solution that would be cheaper than this one since this controller architecture is slightly more expensive than the converter itself.

Finally it would be interesting when this whole system was built and properly optimized to build a fully functioning prototype integrated into an actual net powering a wireless sensor or an actuator and testing its true purpose.

Bibliography

[1] M. Abdelfattah, A. N. Mohieldin, A. Emira, A. K. Hussien, and E. Sanchez-Sinencio. "Ultra-low-voltage power management unit for thermal energy harvesting applications." In: *2012 IEEE 10th Int. New Circuits Syst. Conf. NEWCAS 2012* (2012), pp. 381–384. DOI: 10.1109/NEWCAS.2012.6329036.

[2] R. Aguilar-Najar, F. Perez-Pinal, G. Lara-Salazar, C. Herrera-Ramirez, and A. Barranco-Gutierrez. "Cascaded buck converter: A reexamination." In: *2016 IEEE Transp. Electrif. Conf. Expo, ITEC 2016* (2016). DOI: 10.1109/ITEC.2016.7520211.

[3] P. V. Anushka, N. Mani, and K. Issac. "Switched-inductor semi-quadratic buck converter." In: *Proc. 2017 IEEE Int. Conf. Technol. Adv. Power Energy Explor. Energy Solut. an Intell. Power Grid, TAP Energy 2017* (2018), pp. 1–6. DOI: 10.1109/TAPENERGY.2017.8397367.

[4] N. H. Baharudin, T. M. Mansur, F. A. Hamid, R. Ali, and M. I. Misrun. "Performance Analysis of DC-DC Buck Converter for Renewable Energy Application." In: *J. Phys. Conf. Ser.* 1019.1 (2018). ISSN: 17426596. DOI: 10.1088/1742-6596/1019/1/012020.

[5] R. Bhattacharya, J. Lohani, A. Gupta, V. Aggarwal, H. Singh, T. S. Kukal, C. Moll, D. Baldwin, and J. Park. "Enabling chip, package and PCB system co design and analysis in a heterogeneous integration environment - An EDA approach." In: *2019 IEEE 20th Wirel. Microw. Technol. Conf. WAMICON 2019* 2019-Janua (2019), pp. 2019–2022. DOI: 10.1109/WAMICON.2019.8765456.

[6] N. Bianchi and M. Dai Pre. "Active power filter control using neural network technologies." In: *IEE Proceedings-Electric Power Appl.* 150.2 (2003), pp. 139–145. ISSN: 13502352. DOI: 10.1049/ip-epa. arXiv: arXiv:1011.1669v3. URL: http://digital-library.theiet.org/content/journals/10.1049/ip-epa%7B%5C_%7D20030009.

[7] B. Bosnich, R. Bramley, R. S. Nyholm, and M. L. Tobe. "The Structure and Properties of the Diamagnetic Tris(o-phenylenebisdimethylarsine) nickel (II) Ion." In: *J. Am. Chem. Soc.* 88.17 (1966), pp. 3926–3929. ISSN: 15205126. DOI: 10.1021/ja00969a007.

[9] D. Bui, T. M. Mostafa, A. P. Hu, and R. Hattori. "DC-DC Converter Based Impedance Matching for Maximum Power Transfer of CPT System with High Efficiency." In: *2018 IEEE PELS Work. Emerg. Technol. Wirel. Power Transf. Wow 2018* (2018). DOI: 10.1109/WoW.2018.8450929.

[10] S. Chonsatidjamroen, K. N. Areerak, and K. L. Areerak. "The optimal cascade PI controller design of buck converters." In: *2012 9th Int. Conf. Electr. Eng. Comput. Telecommun. Inf. Technol. ECTI-CON 2012* (2012), pp. 1–4. DOI: 10.1109/ECTICon.2012.6254130.

[11] M. Costa, T. Farrell, and L. Doyle. "On energy efficiency and lifetime in low power wide area network for the Internet of Things." In: *2017 IEEE Conf. Stand. Commun. Networking, CSCN 2017* (2017), pp. 258–263. DOI: 10.1109/CSCN.2017.8088631.

[12] I. Damian, C. Branescu, and V. Soare. "Solder paste optimization in thermal pad padstack." In: *2012 IEEE 18th Int. Symp. Des. Technol. Electron. Packag. SIITME 2012 - Conf. Proc.* (2012), pp. 125–128. DOI: 10.1109/SIITME.2012.6384360.

[13] P. FALKOWSKI. "Analysis and design of high efficiency DC/DC buck converter." In: *Przeglad Elektrotechniczny* 1.5 (2016), pp. 158–163. ISSN: 0033-2097. DOI: 10.15199/48.2016.05.29.

[14] A. Farooq, Z. Malik, Z. Sun, and G. Chen. "A review of non-isolated high step-down Dc-Dc converters." In: *Int. J. Smart Home* 9.8 (2015), pp. 133–150. ISSN: 19754094. DOI: 10.14257/ijsh.2015.9.8.15.

[15] D. Farrakhov, K. Barabanov, A. Podguzov, I. Yamalov, and R. Urazbakhtin. "Quasi-resonant buck converter for high power application." In: *Proc. - ICOECS 2020 2020 Int. Conf. Electrotech. Complexes Syst.* (2020), pp. 2019–2022. DOI: 10.1109/ICOECS50468.2020.9278426.

[16] M. Fu, C. Ma, and X. Zhu. "A cascaded boost-buck converter for high-efficiency wireless power transfer systems." In: *IEEE Trans. Ind. Informatics* 10.3 (2014), pp. 1972–1980. ISSN: 15513203. DOI: 10.1109/TII.2013.2291682.

[17] R. X. Gong, L. L. Xie, K. Wang, and C. D. Ning. "A novel modeling method of nonideal Buck-Boost converter in DCM." In: *ICIC 2010 - 3rd Int. Conf. Inf. Comput.* 3 (2010), pp. 182–185. DOI: 10.1109/ICIC.2010.230.

[18] M. Gorlatova, A. Wallwater, and G. Zussman. "Networking low-power energy harvesting devices: Measurements and algorithms." In: *IEEE Trans. Mob. Comput.* 12.9 (2013), pp. 1853–1865. ISSN: 15361233. DOI: 10.1109/TMC.2012.154.

[19] P. R. Hemavathy, S. Y. Mohamed, and N. Sivaramakrishnan. "Design of State Feedback Controller with Integer Integrator and Fractional Integrator for Control of Buck Converter." In: *Proc. IEEE Int. Conf. "Recent Trends Electr. Control Commun. RTECC 2018* (2019), pp. 261–264. DOI: 10.1109/RTECC.2018.8625645.

[20] J. Hribar and L. Dasilva. "Utilising Correlated Information to Improve the Sustainability of Internet of Things Devices." In: *IEEE 5th World Forum Internet Things, WF-IoT 2019 - Conf. Proc.* (2019), pp. 805–808. DOI: 10.1109/WF-IoT.2019.8767256.

[21] Y. T. Jeon, A. Ahmed, and J. H. Park. "Transformer-less AC-AC system using dual inductor buck converter and multi-level inverter." In: *2017 7th Int. Conf. Power Electron. Syst. Appl. - Smart Mobility, Power Transf. Secur. PESA 2017* 2018-Janua (2018), pp. 1–4. DOI: 10.1109/PESA.2017.8277751.

[22] M. Jia, Z. Sun, and L. Siek. "A Novel Zero-Voltage-Detector for Buck Converter in Discontinuous Conduction Mode(DCM)." In: *2018 IEEE 4th South. Power Electron. Conf. SPEC 2018* Dcm (2019), pp. 2–5. DOI: 10.1109/SPEC.2018.8635909.

[23] H. Y. Kanaan and K. Al-Haddad. "Modeling and simulation of DC-DC power converters in CCM and DCM using the switching functions approach: Application to the buck and cùk converters." In: *Proc. Int. Conf. Power Electron. Drive Syst.* 1 (2005), pp. 468–473. DOI: 10.1109/peds.2005.1619732.

[24] S. Kancherla and R. K. Tripathi. "Nonlinear average current mode control for a DC-DC buck converter." In: *2008 IEEE Int. Conf. Sustain. Energy Technol. ICSET 2008* (2008), pp. 831–836. DOI: 10.1109/ICSET.2008.4747123.

[25] R. Khambuya and S. Khwan-On. "A New High Step-down DC-DC Converter for Renewable Energy System Applications." In: *Procedia Comput. Sci.* 86.March (2016), pp. 349–352. ISSN: 18770509. DOI: 10.1016/j.procs.2016.05.094. URL: http://dx.doi.org/10.1016/j.procs.2016.05.094.

[26] A. K. Khamis, M. Agamy, and R. Ramabhadran. "Split Duty Cycle Coupled Multiphase Boost-Buck Converter." In: *ECCE 2020 - IEEE Energy Convers. Congr. Expo.* (2020), pp. 621–627. DOI: 10.1109/ECCE44975.2020.9236259.

[27] N. Kondrath and M. K. Kazimierczuk. "Control-to-output and duty ratio-to-inductor current transfer functions of peak current-mode controlled dc-dc PWM buck converter in CCM." In: *ISCAS 2010 - 2010 IEEE Int. Symp. Circuits Syst. Nano-Bio Circuit Fabr. Syst.* 2 (2010), pp. 2734–2737. DOI: 10.1109/ISCAS.2010.5537022.

[28] S. G. Kriventsov and J. S. Mayer. "An exact expression for the input impedance of the buck converter in continuous conduction mode." In: *PESC Rec. - IEEE Annu. Power Electron. Spec. Conf.* 1 (2001), pp. 351–356. ISSN: 02759306. DOI: 10.1109/pesc.2001.954045.

[29] E. Kuliev, V. Kureichik, and V. Kureichik. "Mechanisms of swarm intelligence and evolutionary adaptation for solving PCB design tasks." In: *2019 Int. Semin. Electron Devices Des. Prod. SED 2019 - Proc.* (2019). DOI: 10.1109/SED.2019.8798449.

[30] M. Li, B. Zhang, and D. Qiu. "Sneak circuit analysis for a DCM flyback DC-DC converter considering parasitic parameters." In: *2016 IEEE 8th Int. Power Electron. Motion Control Conf. IPEMC-ECCE Asia 2016* (2016), pp. 1151–1155. DOI: 10.1109/IPEMC.2016.7512450.

[31] Z. R. Lin, N. A. Dung, H. J. Chiu, Y. C. Liu, J. S. Lai, and Y. C. Chang. "Analysis and Design of a Novel High Step-Down DC-DC Converter for Battery Applications." In: *2018 IEEE 4th South. Power Electron. Conf. SPEC 2018* (2019), pp. 1–5. DOI: 10.1109/SPEC.2018.8635864.

[32] H. Liu, Y. Ji, L. Wang, and P. Wheeler. "A family of improved magnetically coupled impedance network boost DC-DC converters." In: *IEEE Trans. Power Electron.* 33.5 (2018), pp. 3697–3702. ISSN: 08858993. DOI: 10.1109/TPEL.2017.2763153.

[33] K. E. L. Marcillo, D. A. P. Guingla, W. Barra, R. L. P. De Medeiros, E. M. Rocha, D. A. V. Benavides, and F. G. Nogueira. "Interval Robust Controller to Minimize Oscillations Effects Caused by Constant Power Load in a DC Multi-Converter Buck-Buck System." In: *IEEE Access* 7 (2019), pp. 26324–26342. ISSN: 21693536. DOI: 10.1109/ACCESS.2019.2901441.

[34] Y. Naeimi and A. Huang. "Design and optimization of high conversion ratio quasi square wave buck converters." In: *2017 IEEE 5th Work. Wide Bandgap Power Devices Appl. WiPDA 2017* 2017-Decem (2017), pp. 148–152. DOI: 10.1109/WiPDA.2017.8170538.

[35] J. D. Nascimento and V. J. Farias. "A quadratic buck converter with lossless commutation vincius miranda pacheco, acrísio." In: *IEEE Trans. Ind. Electron.* 47.2 (2000), pp. 264–272. ISSN: 02780046. DOI: 10.1109/41.836341.

[36] G. Nayak and S. Nath. "Voltage Mode Control of Magnetically Coupled SIDO Buck Converter." In: *Proc. 2018 IEEE Int. Conf. Power Electron. Drives Energy Syst. PEDES 2018* (2019), pp. 1–6. DOI: 10.1109/PEDES.2018.8707607.

[8] B. A. Nuno Paulino. "Study of a Low Power Energy Harvesting System for the Electrical Power Grid." In: *Universidade Nova de Lisboa, Faculdade de Ciências e Tecnologia, Monte da Caparica* (2019).

[37] P. Omer, J. Kumar, and B. S. Surjan. "Design of robust PID controller for Buck converter using Bat algorithm." In: *1st IEEE Int. Conf. Power Electron. Intell. Control Energy Syst. ICPEICES 2016* (2017). DOI: 10.1109/ICPEICES.2016.7853209.

[38] M. Pedram. "Power optimization and management in embedded systems." In: *Proc. Asia South Pacific Des. Autom. Conf. ASP-DAC* 2001-Janua (2001), pp. 239–244. DOI: 10.1109/ASPDAC.2001.913312.

[39] T. Ruan, Z. J. Chew, and M. Zhu. "Energy-Aware Approaches for Energy Harvesting Powered Wireless Sensor Nodes." In: *IEEE Sens. J.* 17.7 (2017), pp. 2165–2173. ISSN: 1530437X. DOI: 10.1109/JSEN.2017.2665680.

[40] M. et al Rüßmann. "Future of Productivity and Growth in Manufacturing." In: *Bost. Consult.* April (2015). ISSN: 9783935089296. DOI: 10.1007/s12599-014-0334-4. arXiv: arXiv:1011.1669v3.

[41] F. I. Simjee and P. H. Chou. "Efficient charging of supercapacitors for extended lifetime of wireless sensor nodes." In: *IEEE Trans. Power Electron.* 23.3 (2008), pp. 1526–1536. ISSN: 08858993. DOI: 10.1109/TPEL.2008.921078.

[42] P. Singh and S. Purwar. "Sliding mode controller for PWM based Buck-Boost DC/DC converter as state space averaging method in continuous conduction mode." In: *ICPCES 2012 - 2012 2nd Int. Conf. Power, Control Embed. Syst.* (2012), pp. 0–4. DOI: 10.1109/ICPCES.2012.6508100.

[43] M. Siripruchyanun and P. Wardkein. "A temperature-insensitive VCO and derivative PWM signal generator." In: *Int. Conf. ASIC, Proc.* (2001), pp. 224–227. DOI: 10.1109/icasic.2001.982538.

[44] S. N. Soheli, G. Sarowar, M. A. Hoque, and M. S. Hasan. "A DC-DC Step Down Converter for Unprecedented Higher Efficiency." In: *2018 Int. Conf. Adv. Electr. Electron. Eng. ICAEEE 2018* (2019), pp. 1–4. DOI: 10.1109/ICAEEE.2018.8643013.

[45] M. Spasova, T. Brusev, G. Angelov, R. Radonov, and M. Hristov. "Low Power Ramp Generator with MOSFET and CNTFET Transistors." In: *2019 28th Int. Sci. Conf. Electron. 2019 - Proc.* (2019), pp. 2019–2021. DOI: 10.1109/ET.2019.8878567.

[46] D. Sun, S. Xu, W. Sun, S. Lu, and L. Shi. "Low power design for SoC with power management unit." In: *Proc. Int. Conf. ASIC* (2011), pp. 719–722. ISSN: 21627541. DOI: 10.1109/ASICON.2011.6157306.

[47] Y. K. Tan and S. K. Panda. "Optimized wind energy harvesting system using resistance emulator and active rectifier for wireless sensor nodes." In: *IEEE Trans. Power Electron.* 26.1 (2011), pp. 38–50. ISSN: 08858993. DOI: 10.1109/TPEL.2010.2056700.

[48] M. D. Vecchia, G. Van Den Broeck, S. Ravyts, and J. Driesen. "Novel step-down DC-DC converters based on the inductor-diode and inductor-capacitor-diode structures in a two-stage buck converter." In: *Energies* 12.6 (2019), pp. 1–22. ISSN: 19961073. DOI: 10.3390/en12061131.

[49] X. Xiong, K. Zheng, R. Xu, W. Xiang, and P. Chatzimisios. "Low power wide area machine-to-machine networks: Key techniques and prototype." In: *IEEE Commun. Mag.* 53.9 (2015), pp. 64–71. ISSN: 01636804. DOI: 10.1109/MCOM.2015.7263374.

[50] L. D. Xu, W. He, and S. Li. "Internet of things in industries: A survey." In: *IEEE Trans. Ind. Informatics* 10.4 (2014), pp. 2233–2243. ISSN: 15513203. DOI: 10.1109/TII.2014.2300753.

[51] Y. Zhang and C. E. Saavedra. "A nonoverlapping clock generator circuit using bipolar differential pairs." In: *Proc. IEEE Int. Caracas Conf. Devices, Circuits Syst. ICCDCS* (2004), pp. 330–333. ISSN: 15416275. DOI: 10.1109/iccdcs.2004.1393407.