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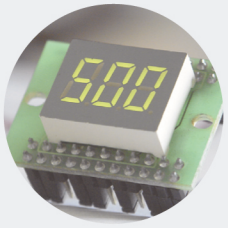


PCG and ECG Portable Acquisition System

JOSÉ MÁRIO MEIRA DA SILVA
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José Mário Meira da Silva

Master in Electrical and Computer Engineering
Specialization Area of Telecommunications

Departamento de Engenharia Eletrotécnica
Instituto Superior de Engenharia do Porto

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Candidate: José Mário Meira da Silva, No. 1150716, 1150716@isep.ipp.pt

Scientific Guidance: Prof. Dr. António Avelino Marques, aav@isep.ipp.pt

Departamento de Engenharia Eletrotécnica
Instituto Superior de Engenharia do Porto
Rua Dr. António Bernardino de Almeida, 431, 4200–072 Porto

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Abstract

Heart disease is the leading cause of death in the world, victimizing human beings in all age groups and from different geographic areas. Through the evolution of auscultation technology, the identification and analysis of heartbeats make it possible to prevent and treat heart pathologies with greater success. In this project, a portable, low-power system was developed that allows the acquisition of heart sound signals simultaneously in four different auscultation zones, as well as the acquisition of an electrical signal, subsequently conditioning and processing the different signals. The system also allows the transmission of signals in real-time via Bluetooth Low Energy to a mobile device where they can be recorded for future analysis.

The portable system records four phonocardiographs located at four auscultation areas, namely the aortic valve, the mitral valve, the pulmonary valve and the tricuspid valve. These sound signals are converted to analog electrical signals that will be amplified, filtered and converted into digital signals. There is also a two-electrode electrocardiograph in this system, which is also amplified and filtered before being converted to a digital signal and transmitted via wireless communication. The entire system is powered by a battery with a charge voltage of 4.2 V, which allows it to be charged through the USB interface.

Keywords: Heart, PCG, ECG, analog filters, Bluetooth Low Energy.

Resumo

As doenças cardíacas são a principal causa de morte no mundo, vitimizando seres humanos em todas as faixas etárias e de diferentes àreas geográficas. Através da evolução da tecnologia na auscultação, a identificação e análise dos batimentos cardíacos permitem prevenir e tratar patologias do coração com maior sucesso. Neste projeto foi desenvolvido um sistema portátil de baixa potência que permite a aquisição dos sinais sonoros do coração simultaneamente em quatro diferentes zonas de auscultação, assim como a aquisição de um sinal elétrico, fazendo posteriormente o condicionamento e processamento dos diferentes sinais. O sistema permite ainda a transmissão em tempo-real dos sinais via Bluetooth Low Energy para um dispositivo móvel onde podem gravados para futura análise.

O sistema portátil regista quatro fonocardiogramas localizados em quatro áreas de auscultação, nomeadamente na válvula aórtica, na válvula mitral, na válvula pulmónica e na válvula tricúspida. Estes sinais sonoros são convertidos para sinais elétricos analógicos que serão amplificados, filtrados e convertidos de novo para sinais digitais. O sistema regista também o electrocardiograma através de dois elétrodos, que é também amplificado e filtrado antes de ser convertido em sinal digital e transmitido via comunicação sem fios. Todo o sistema é alimentado por uma bateria com tensão de carga 4.2 V, que permite ser carregada através de interface USB.

Palavras-Chave: Coração, fonocardiograma, electrocardiograma, filtros analógicos, Bluetooth Low Energy.

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List of Acronyms

AC Alternate Current

ADC Analog-to-Digital Converter

ASIC Application Specific Integrated Circuit

ATT Attribute Protocol

aVF augmented vector foot

aVL augmented vector left

aVR augmented vector right

BLE Bluetooth Low Energy

CMOS complementary metal–oxide–semiconductor

CMRR common mode rejection ratio

DC Direct Current

DSP Digital Signal Processor

ECG electrocardiogram

EMI Electromagnetic Interference

GAP Generic Access Profile

GATT Generic Attribute Profile

GPIO General Purpose Input/Output

I2S Inter-IC Sound

LRPAN Low Rate PAN

MEMS micro-electromechanical systems

OpAmp Operational Amplifier

PC Personal Computer

PCB Printed Circuit Board

PCG phonocardiogram

PCM Pulse Code Modulation

PDM Pulse Density Modulation

PPI Programmable Peripheral Interconnect

RAM Random Access Memory

RFI Radio Frequency Interference

SAADC Successive Approximation Analog-to-Digital Converter

SD Secure Disk

SDK Software Development Kit

SMD surface mount device

SPI Serial Peripheral Interface

UART universal asynchronous receiver-transmitter

USB universal serial bus

WLAN wireless local-area network

WPAN wireless personal area network

Chapter 1

Introduction

In this chapter is presented a brief introduction to the dissertation, as well as a presentation of its schedule. There will also be made a contextualization of the problem and the solutions the dissertation's final prototype will provide.

1.1 Contextualization

Heart disease is the leading cause of death in most countries, being the number one cause of death in the world. It is estimated that 17.9 million people die from cardiovascular diseases every year, representing about 31 % of all deaths worldwide. The diagnose and detection of possible symptoms associated with such diseases has been a major concern in the medical field and will continue to be for the foreseeable future.

The role of diagnosis in the reduction of deaths from heart diseases is essential. Two common tools used for this diagnosis are the phonocardiogram (PCG) and electrocardiogram (ECG). The ECG is an effective and widely used instrument for detecting cardiac problems. It is reasonably priced, non-invasive and simple to use. However, it does have some drawbacks, one of which is the difficulty in detecting structural irregularities in heart valves and defects that cause heart murmurs. The PCG is a technique that evolved from the ECG, with the main advantage of being capable of detecting more irregularities than the ECG.

This dissertation bases itself on the development of a solution that allowed for real-time monitoring and acquisition of four simultaneous PCG signals and a ECG

signal. The overall goal of such hardware is to make it possible to study and analyze the differences in the auscultation between the different heart valves and find common patterns that might reveal early symptoms of a heart defect in a human being.

1.2 Goals

This dissertation aims to develop a miniaturized and portable system that acquires different heart sounds and signals from the same person, and is capable of transmitting those same signals in digital format to another device in real time. A more comprehensive list can be exposed as:

- Study of the technological component involved in the PCG and ECG;
- Study of the best microphones for the application;
- Study and development of electrical circuits needed for amplifying and filtering the signals;
- Development of the signal processing circuit;
- Study, analysis and creation of different power modules in order to make the system portable and functional;
- Development of software for signal processing and wireless transmission in that same hardware;
- Testing and experimental validation.

1.3 Timeline

	Mar	Abr	Mai	Jun	Jul	Ago	Set	Out
Report Writing								
Definition of objectives and requirements								
Study of the heart sounds auscultation								
Study of existing products on the market								
Study of PCG and ECG								
Circuit build and simulation								
Software development								
Electrical Schematics								
Bill of Materials								
PCB design								
Results Validation								

Table 1.1: Dissertation Schedule

1.4 Structure

This report is divided into five different chapters.

First there is the introduction, where the dissertation's main goal is exposed, referring to the context of the dissertation, the timeline, and the organization of the report.

In the second chapter a study of the state of the art is made where there is an explanation about every technology that was thought for implementation and a comparison is made between them in order to justify why any different technology or hardware was chosen over the other. There is also a debrief on the medical component of this dissertation, where a base is given for the comprehension of the problem this project aims to solve.

The third chapter reports the implementation of the hardware, and it's where the technical components of the projects are approached. This is done by presenting the project's architecture and by contextualizing what problems are solved within that context and what constraints were avoided or attenuated with each decision.

The fourth chapter reveals the circuit and software validation, presenting all the tests made from the dissertation's beginning to the end result.

Finally, a conclusion chapter is added where a reflection on the whole dissertation is made and future improvements are suggested.

Chapter 2

State of Art

In the following chapter several topics used for the elaboration of an acquisition system will be approached. Firstly, a study of the ECG was made so there is a wider initial knowledge of the heart functioning, as well as its definition and operation, deeming its study a requirement in order to connect the concepts covered in this dissertation. In the PCG, which appears chronologically after, it was studied its concept and its working principle. A research on the best hardware and technologies to be used in the development of the PCG is also presented in this chapter.

2.1 Heart

The heart is a vital organ in human beings that has the appearance and proportions of a closed fist. It has four cavities, two auricles and two ventricles, which are separated by the interventricular septum, and is situated in the mediastinum, just to the left of the sternum. It is the organ responsible for pumping the blood to all parts of the body [1]. A representative scheme of the human heart can be found in figure 2.1.

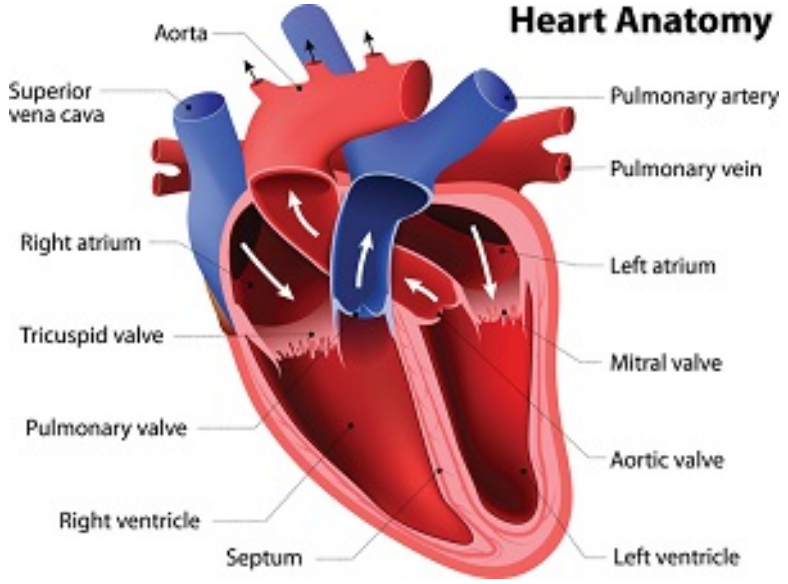

Figure 2.1: Heart [2].

The venous blood, rich in carbon dioxide and cellular waste and poor in nutrients, enters the right atrium through the superior and inferior vena cavas after flowing through the entire body. It also returns the blood that ran through the heart. After the venous blood enters the right atrium, it is pumped to the right ventricle through the tricuspid valve, where the blood is then pumped to the lungs, in order to be filled with oxygen again. This route corresponds to the pulmonary circulation. In the left atrium, the arterial blood enters the heart coming from the lungs, where it was filled with oxygen. The blood is then routed to the left ventricle, by the tricuspid valve, which impels blood to the entire organism. The left ventricle is usually thicker relative to the right ventricle, implying a greater associated pressure. This route corresponds to the systemic circulation.

The movements of the heart, associated with the two types of blood circulation, are correspondent to two different stages: the diastole, in which the auricles and ventricles are filled and the systole, where there is contraction of the heart muscle, which leads to blood being pumped, and which can be ventricular by contraction of the ventricle or auricular by the contraction of auricles. [1] [3].

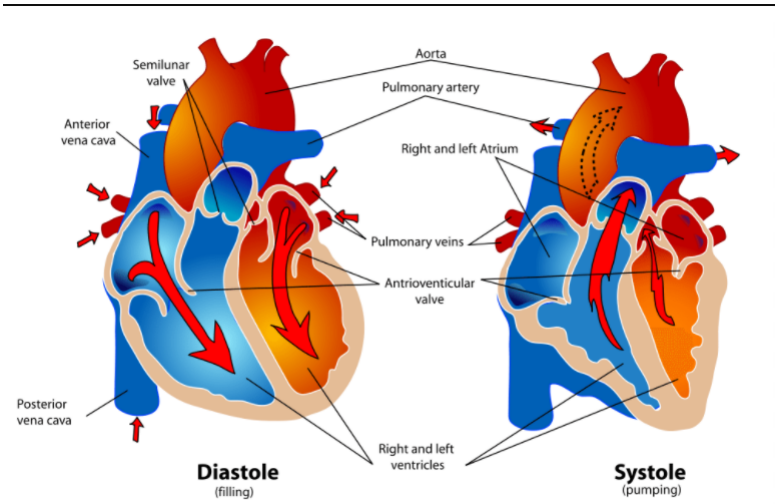

Figure 2.2: Heart systole and diastole [4].

2.2 ECG

The ECG is an exam that registers the electrical activity of the heart. The principle behind this diagnostic is to acquire an electrical signal and understand its relation to a mechanical event of the heart. While such study can be effective to understand and detect some heart anomalies, by not measuring the mechanical action of the heart it fails to obtain precious information such as the contraction force or the arterial pressure. Still, this examination is suitable for diagnosing cardiac arrhythmias and premature cardiac ischemies. The ECG also has a large validity in the diagnosis of different cardiac abnormalities, including valve diseases [5].

2.2.1 ECG Signal

The waves represented in the ECG chart in figure 2.3 demonstrate the operation of the auricles (P wave) and ventricles (QRS and T waves). The heart cells electrical stimuli is activated by their depolarization.

The P waves initiate by the depolarization of the right auricle, translating a contraction and end in the depolarization of the left auricle, again caused by a contraction. Next, the PR interval represents the time between the start of P wave and the start of the QRS complex. The evaluation of this interval allows to check if the conduction from the atria to the ventricles is regular [6].

The QRS can be decomposed into three different waves, Q, R and S, but for exam evaluation is usually mentioned as one wave complex. It is directly connected to the depolarization of the ventricles. The measurement of its time indicates how long it took for the left ventricle to depolarize. Longer intervals usually indicate a

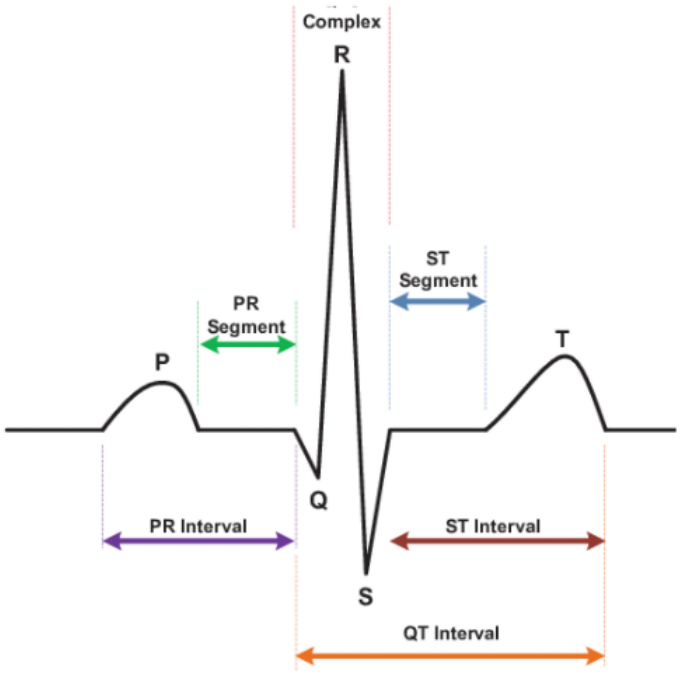

Figure 2.3: Representation of an ECG signal [7].

dysfunction in the conduction system, while shorter intervals usually mean a healthy heart.

The ST segment corresponds to the time between the S depression and the T wave. It is the segment with most variance and it is always subject to careful observation. The level of amplitude is measured against the PR wave amplitude, and any slight deviation can indicate a case of myocardial ischemia.

Finally, the T wave represents the repolarization of the heart cells that contracted before. The study of this wave is very contextualized with the prior waves in the ECG, and its study in isolation is seldom recommended, often causing false positives [6].

2.2.2 Einthoven Triangle

The Einthoven Triangle created by Willem Einthoven, is a theorized triangle used to provide the basis for where the electrodes have to be placed. The placement of these devices form an equilateral triangle that is constituted by the upper and lower limbs of the human body. It is usually setup in the right and left arm, and either the left or right leg. There are three leads, lead I corresponds to the electrical tension between the right and left arm, lead II, concerns difference between the right arm and the left leg and the lead III corresponds to the voltage between the left arm and the left leg, maintaining the right leg as a ground reference [8].

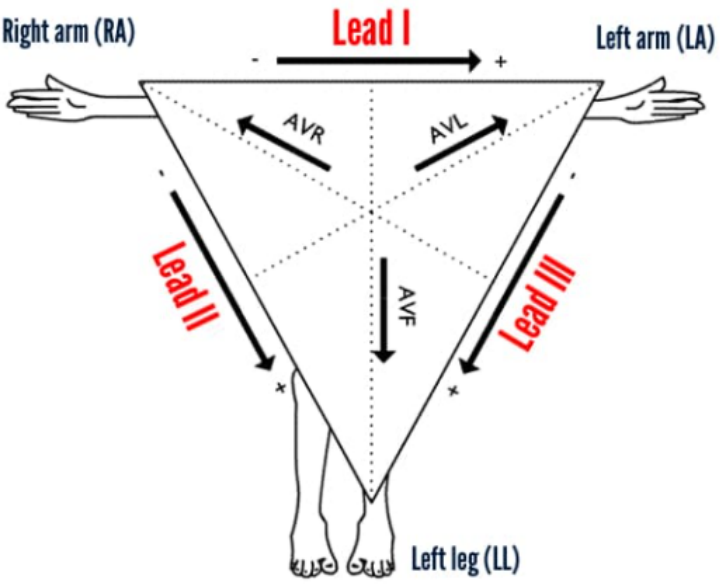

Figure 2.4: Einthoven Triangle [9].

The principle behind Einthoven's triangle is that the three leads form a closed circuit using the human body as a reference. Considering the lead placement as an electrical circuit, it implies that knowing the potential in two of the leads will permit to know the third lead potential by default, since it's known that the sum of the currents in the closed circuit must be zero, following Kirchoff's law. By Einthoven's law then, we can perceive derivation II as:

$$DerivationII = DerivationI + DerivationIII \tag{2.1}$$

While not used in modern ECG exams, the Einthoven triangle principles remain the base theory for the ECG electrode placement in the present.

2.2.3 ECG Derivations

A modern ECG in a hospital environment is usually made from 12 derivations, six leads from members(I, II, II, AVR, AVL, AVF), and six chest derivations called V1 to V6. Leads augmented vector right (aVR), augmented vector left (aVL) and augmented vector foot (aVF) are named unipolar leads because they are made from the amplification of the signal obtained with the positive electrode placed respectively on the upper right, upper left and lower left limb [10]. In a continuous monitor, it's possible to use only three to five leads to make a full diagnosis. The lead placement can be seen in figure 2.5.

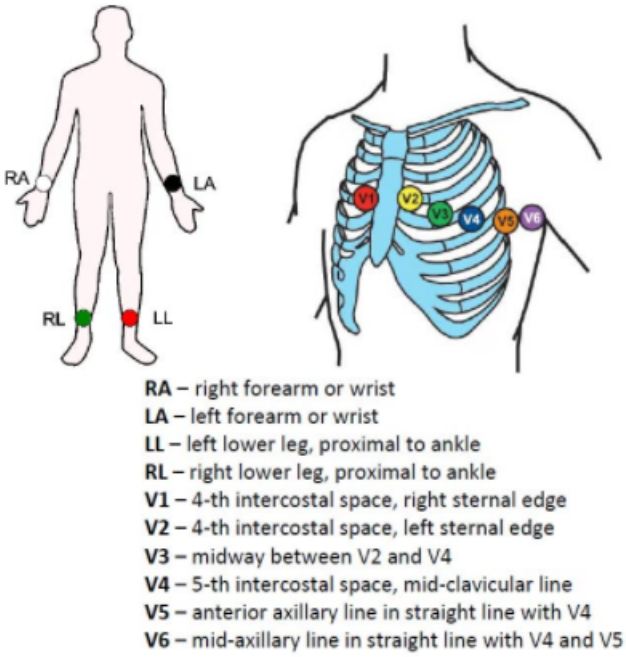

Figure 2.5: 12 lead ECG placement [11].

It's important to note that the ECG made in this dissertation uses only two leads and a third lead for reference. A two lead topology can measure an angle of the heart functioning, and is enough for monitoring the heart and detect possible anomalies like arrhythmia or tachycardias, however is not a substitute for a full ECG diagnosis, neither is intended to do so.

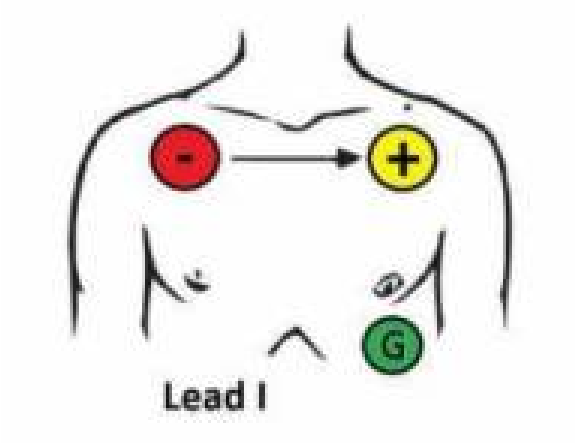

Figure 2.6: 2 lead ECG placement [12].

2.3 PCG

The PCG detects and records the sounds that result from the movements of the heart while pumping blood and the blood that flows in it. The PCG can be considered as a physiological signal that reflects the motion mechanics of the heart. The visualization of this signal is used for an evaluation of the cardiac valves and its hemodynamics. For the recording of cardiac beeps, the PCG analyzes heartbeats captured by a very sensitive microphone in order to allow the monitoring of the patient's cardiac condition. This technology offers the advantages of not being invasive, while it also does not require a high level of experience and technical skill to use and configure the system from a medical point of view. The equipment usually displays the various types of sounds emitted by the heart via electric signal observation [13].

2.3.1 Heart Sounds Characteristics

The PCG provides an accurate study of the effect of exercise in the heart. An athlete using this system can evaluate the effect of intensive exercise in his heart and subsequently evaluate potential benefits or disadvantages by studying the heart sounds produced in the exercise. Such measurement of cardiac sounds after and during physical exercise is a rather accessible technique compared to other tests.

The pounding heart and the resulting blood that flows into it produce heart sounds. Two heart sounds are common in healthy adults: the first (S1), which is caused by the closure of the atrioventricular valves, and the second (S2), which is caused by the closure of the semilunar valves. There are other signal events between S1 and S2 in the case of an irregular heart sound, such as S3, S4, or murmurs. The third heart sound (S3) is an extra sound caused by a rapid deceleration of blood flow into the left ventricle from the left atrium. While this sound is common in children and adults up to age 40, albeit in a discrete amplitude compared to S1 and S2, a third heart sound is usually irregular in patients with an older age, being associated with dysfunction or volume overload of the ventricles. The fourth heart sound (S4) is caused by the vibration of valves, supporting structures and the ventricular walls. During the diastolic phase, S4 has been shown to be an indication or symptom of heart failure. Murmurs are additional or irregular sounds found during a heartbeat that are divided into three categories: systolic, diastolic, and constant [14].

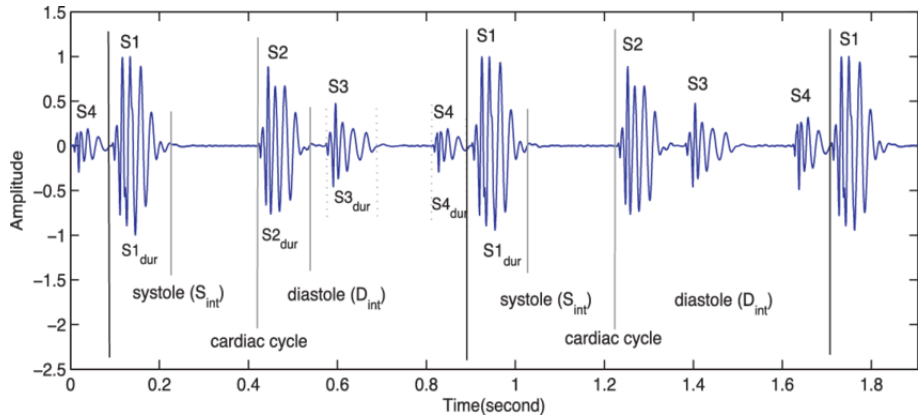

Figure 2.7: PCG Signal with S1-S4 sounds [15].

Overall, S1 has a lower frequency than S2, and S1 has therefore a longer period than S2. S1 frequency usually ranges between 50 and 150 Hz, with periods of 70 to 150 ms and has a higher amplitude than the other sounds in normal conditions. S2 has a larger range of frequency, between 50 and 200 Hz and has a lower amplitude compared to S1. S3 has lower frequencies, between 50 and 90 Hz and it is usually a indication of a possible heart disease when detected in older patients. It occurs 0.1 to 0.2 seconds after S2. S4 occurs 0.07 to 0.1 seconds before S1, and it has a frequency range of 50-80 Hz. Aside from these heart sounds, a variety of heart murmurs may develop as a direct result of heart attacks or diseases [13].

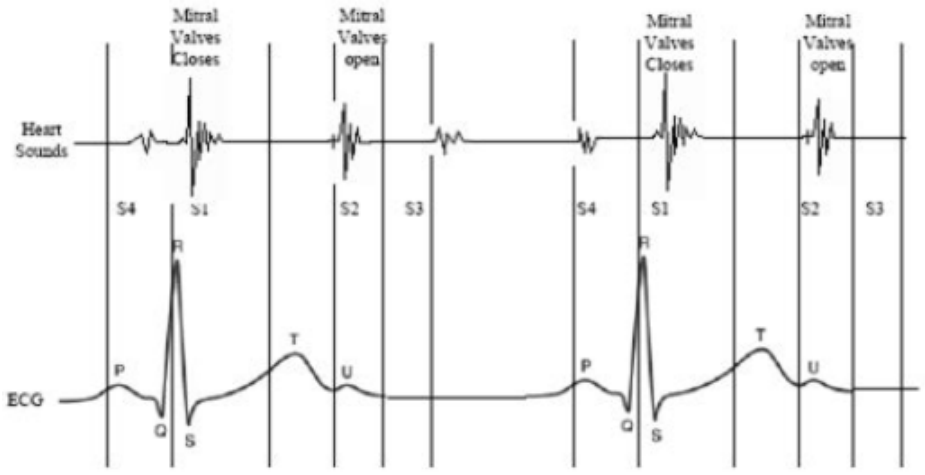

Figure 2.8: PCG and ECG signal comparison [16].

2.3.2 Auscultation Zones

To insure a correct analysis of a determined area it is required for the PCG system to be in the most indicated place to acquire the signal. While it's clear that the chest area left to the sternum, where the heart resides, is where the measurement should be made, it's possible to study the auscultation zones further.

In figure 2.9, we can see the auscultatory areas of the heart. The four valve areas described are not the actual anatomical locations of the valves, being instead where they are heard the best. Understanding that the sound is projected in the direction of blood flow, a good microphone placement in the valve areas makes it possible for a more accurate assessment of heart murmurs. The intercostal spaces are also mentioned for better comprehension of the auscultatory zone location [17].

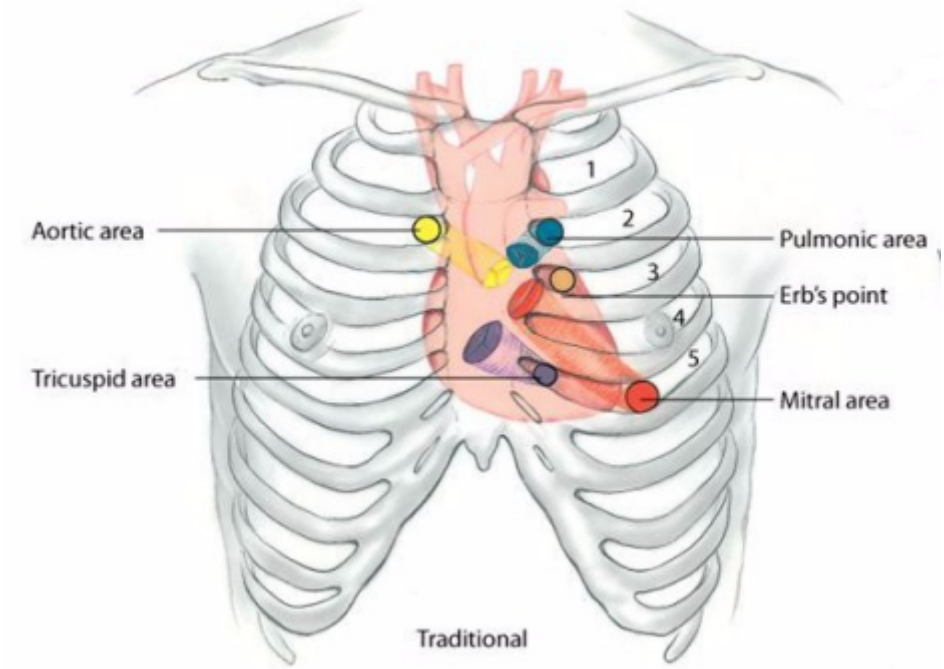

Figure 2.9: Diagram of ideal auscultation zones [18].

The valve areas described in the figure above are:

- Aortic valve area, placed in the second right intercostal space
- Mitral valve area in the 5th intercostal space at approximately the left mid-clavicular line
- Pulmonic valve area in the second left intercostal space
- Tricuspid valve area placed in the left lower sternal border

2.3.3 Heart sound sensors

For any PCG system, the microphone is a critical component since it is responsible for the acquisition of the signal. A non adequate microphone would right away compromise the good functioning of the entire system. Many variables must be taken into consideration, such as impedance, frequency response, mode operating temperature, sensitivity, and size. The sensors used to convert acoustic energy into electrical signals go by the name of transducers. The membrane that is installed in this type of component undergoes a movement that is subsequently converted into an electrical signal with an amplitude proportional to the intensity of its vibration. Impedance is the amount of resistance a component provides to current flow in a circuit at a given frequency. Any microphone in modern times has output impedances in the hundreds of ohms region.

For a correct design, the amplifier for this type of microphone should have an input impedance about 20 times greater than the output impedance of the microphone. This relationship results from a response in frequency with smaller oscillations, ideal to keep a flat response throughout the desired frequencies. For very low impedances, the microphone will demand more current and as a result will dissipate more power when the sound waves move its membrane, increasing the risk of distortion. In the case of higher impedances, they guarantee a better performance, with the counterpart of loss in higher frequencies.

There are several types of microphones in the market. The most common in similar applications are electrostatic and electromechanical microphones. Since the electromechanical microphone was a requirement in this application, an analysis of this microphone will follow.

Electromechanical Microphones

A micro-electromechanical systems (MEMS) microphone is a microphone that is produced using micro-electromechanical systems processing techniques. These microphones are engraved onto a silicon wafer that is semiconductive. Behind a stationary perforated plate, a pressure-sensitive moveable membrane called diaphragm is etched. A capacitor then is made out of the perforated stationary plate and the diaphragm (much like the design of a condenser microphone). After etching, the MEMS transducer element contains a moving diaphragm, a stationary yet perforated plate, and a housing around it. An Application Specific Integrated Circuit (ASIC) is then designed to fit with the transducer element of a MEMS microphone [19].

Sound waves enter the MEMS microphone through the perforated housing in its cover, allowing it to reach the diaphragm. Depending on the sound pressure applied, it will cause the diaphragm to move in a linear progression. Since the plate

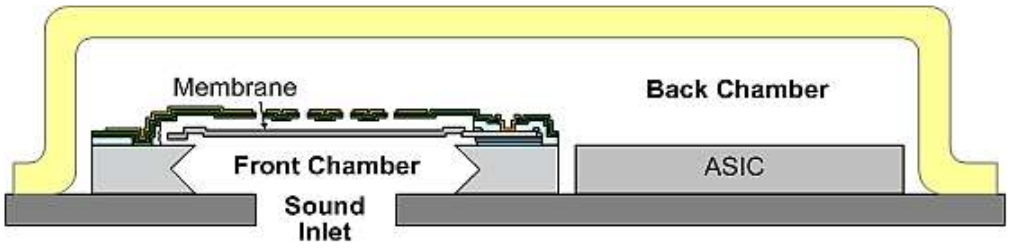

Figure 2.10: MEMS microphone [19].

is charged, the diaphragm motion will create a practical capacitor that can vary in capacitance. This capacitance change will create a voltage inverse to the capacitance variance, transforming the sound signal in an electrical one. The electrical signal is then amplified via a separate integrated circuit in the whole package, ensuring some level of low impedance [19].

Every MEMS microphone has similar functionality until this point. After the amplified signal, different solutions for the output are offered. Two outputs were studied for this dissertation, analog output, or digital outputs with Pulse Density Modulation (PDM).

MEMS microphones with analog outputs function exactly like the MEMS microphone explained above. The amplified signal will already function as the circuit output and can be connected directly to the signal conditioning circuit, only using a blocking capacitor in order to filter the Direct Current (DC) component of the microphone output. A typical application can be seen in the figure below.

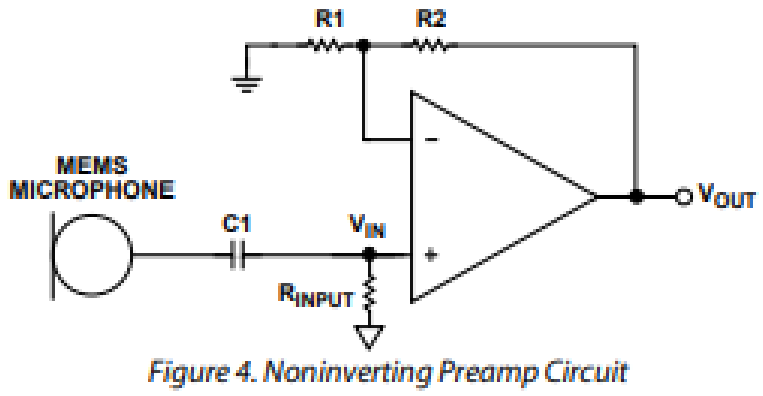

Figure 2.11: Analog MEMS microphone implementation example [20].

The output signals from MEMS microphones with a digital interface are similar to the analog microphones, but include an encoding circuit with either PDM or Inter-IC Sound (I2S). With PDM the analog signal voltage is converted into a single bit digital stream containing a corresponding density of logic-high signals. The PDM has some benefits over the analog output, being more immune to electrical noise, having a bit error tolerance due to its digital nature and can also allow direct connection to a microcontroller or Digital Signal Processor (DSP). In figure 2.12 is possible to see the connection of a PDM microphone to a host circuit [21].

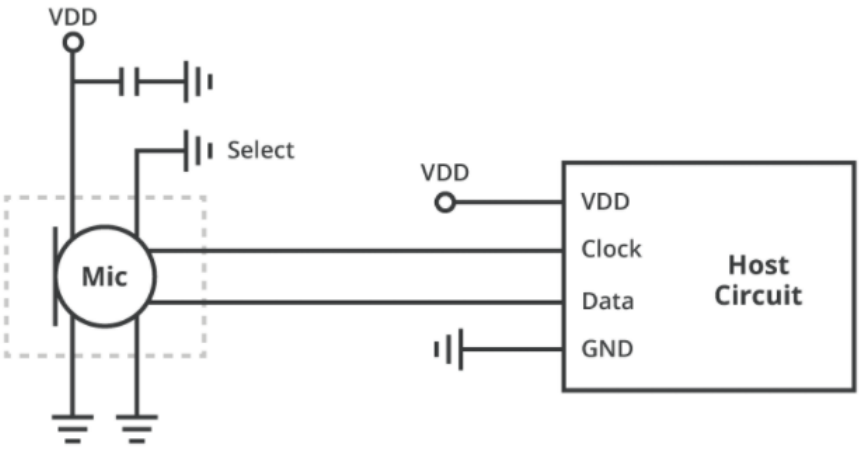

Figure 2.12: PDM microphone implementation example [21].

2.3.4 Digital Audio

In a digital audio system, an analog electrical signal representing the sound is converted with an Analog-to-Digital Converter (ADC) into a digital signal, typically using Pulse Code Modulation (PCM). This digital signal can then be used with any digital tool that supports audio processing. In this chapter a brief explanation of the PCM and PDM modulations will be done.

Pulse Code Modulation

Pulse code modulation is a technique used to represent analog signals in digital format. It samples the amplitude of the analog signal and changes it to binary data, being the standard in digital audio. In PCM, the audio signal is built out of a number of samples, each a fixed number of bits long. Two factors determine the performance of the system, the sampling rate, which will give the system's bandwidth, and the wordlength, which will dictate the SNR (signal-to-noise ratio) of the system [22].

The wordlength refers to the number of bits used to represent the amplitude. The more bits used, the bigger the range of values can be given to represent the signal amplitude, thus improving the system's SNR. The formula for the SNR for a PCM system, when N is the number of bits can be written as:

$$SNR = (6.02N + 1.76)dB[23] \tag{2.2}$$

As for the sampling rate, it represents the number of times per second that samples are taken. As a rule, following the Shannon-Nyquist theorem, the sampling frequency must be at least two times the maximum frequency expected for the signal that is to be modulated. The bigger the sampling rate, the larger the bandwidth is and the more precise the signal reconstruction will be.

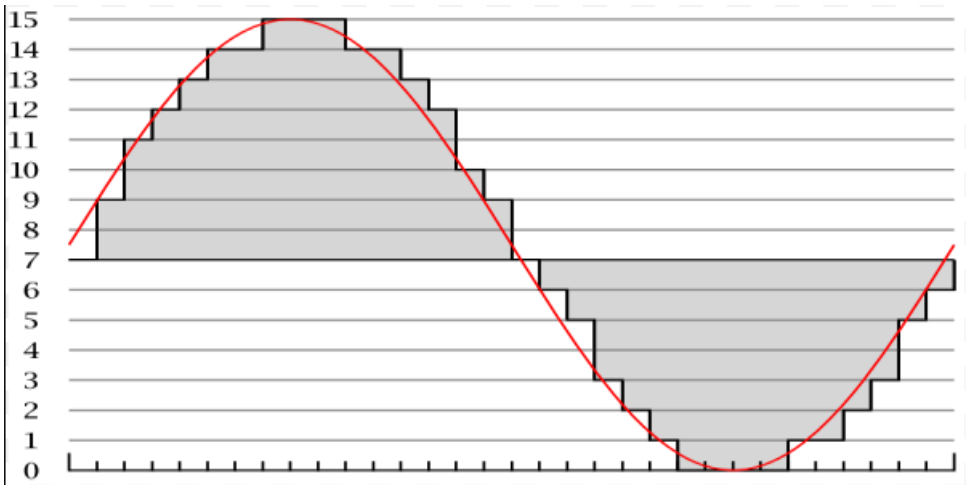

Figure 2.13: 4-bit PCM example [24].

Pulse Density Modulation

Pulse-density modulation, or PDM, is a form of modulation used to represent an analog signal with a binary signal. Having the PCM fundamentals as a base, it can be made the exercise of considering the PDM a PCM with a wordlength of only one bit. While at first glance such modulation shouldn't be capable of representing the integrity of an analog signal, it's possible to do so by increasing the sampling rate to compensate the lack of amplitude resolution. That technique is called oversampling.

By oversampling the overall goal is to produce a signal with very low noise in the passband. Usually the oversampling ratio used in a PDM microphone is of 64, which means that for a typical audio sample frequency of 48 kHz, the sample frequency of a PDM system will be 3.072 MHz. A PCM modulation example can be seen in figure 2.14, where the blue represents a logical value of 1 and the white represents a logical value of 0 [23].

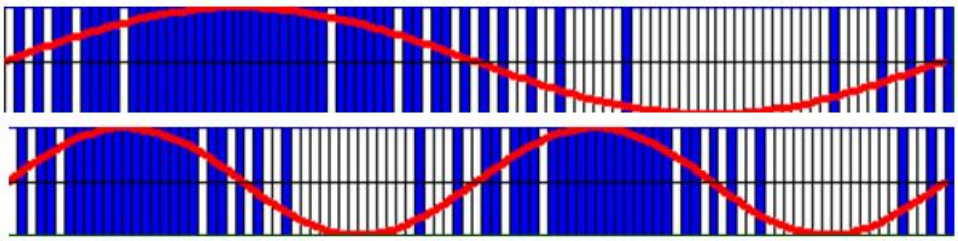

Figure 2.14: Example of a 100 Hz and a 200 Hz modulation [25].

A run consisting of all 1s would correspond to the maximum (positive) amplitude value, all 0s would correspond to the minimum (negative) amplitude value, and alternating 1s and 0s would correspond to a zero amplitude value. A PDM signal can be demodulated using only a low-pass filter. This is possible since the function of a low-pass filter is essentially to average the signal, and the average amplitude at a determined time is given by oversampling, deeming the low pass filtering of the signal almost an inverse process of a pulse density modulation.

2.3.5 PCG sensors in the market

In this subsection it is presented the outcome of the research made for the available state of art equipment on the market. For the studied models both functionality and technology features are approached.

Research was made for the following models:

- StethoMe
- Thinklabs One Digital
- iWorx HSM-300;

StethoMe

StethoMe is a small and portable digital stethoscope that examines and analyzes the heart sounds. It's a smart device that allows for real time perception of the user's health status. This equipment analyzes the functioning of the body and in the event that there is a cardiac or respiratory problem, and can be programmed to contact medical staff immediately.

Some of the features of the StethoMe include:

- Operation via wireless networks;
- Heart sound examination
- Monitoring of long-term illnesses;
- Heart Rate monitoring
- Tracking medical history
- Detect heart patterns through artificial intelligence

Figure 2.15: StethoMe stethoscope [26].

This device connects with the Smartphone (iPhone or Android) and synchronizes the medical data collected by the sensors with an application that manages the device. This miniaturized system works on a telemedicine platform, which shares the data collected from the patient with the respective physician [26].

iWorx HSM-300 Heart Sounds Monitor

The iWorx HSM-300 is a simple device that converts the sound waves, created by the cardiac valves during operation, into electrical signals that can be stored and subsequently checked. A piezoelectric sensor, mounted on the side of HSM-300, captures the vibrations created by the heart sounds. The piezoelectric crystals in the sensor convert the pressure changes created by voltage vibrations. These are usually recorded alongside the patient's ECG to identify the specific sounds of the heart occurring during contraction and ventricular relaxation. An image of the whole system is shown below [27].

Figure 2.16: HSM 300 full system [27].

Thinklabs One Digital

This stethoscope is developed by Thinklabs and defined by the brand as the smallest and most powerful in the world. It is a rather small stethoscope. It uses a patented capacitive transducer and has a graphic interface with accessible usability. To perform the auscultation, this equipment allows the use of audio headphones. Its amplifier can increase the signal amplitude up to 100 times while keeping signal integrity. In figure 2.17 a image of this model can be seen.

Figure 2.17: Thinklabs One digital stethoscope [28].

The Thinklabs One allows for the digital filters to be programmed according to the sound wanted to acquire. This equipment provides a 3.5 mm jack connection to save the signal data through either a Personal Computer (PC) or a mobile device. The software interface is provided by Thinklabs [28].

2.4 Analog Circuit and ADC

2.4.1 Operational Amplifier

In the 1960s, a component that allowed for arithmetic operations between analog signals called an Operational Amplifier (OpAmp) was developed. Being an element consisting of two inputs and one output, it has a high differential impedance in the input and low impedance in the output, allowing a high gain for an analog signal. This circuit has many use cases, ranging from frequency filtering to a simple voltage amplifier. Figure 2.18 shows an example of an inverting topology and a non-inverting one. Both were used in the dissertation.

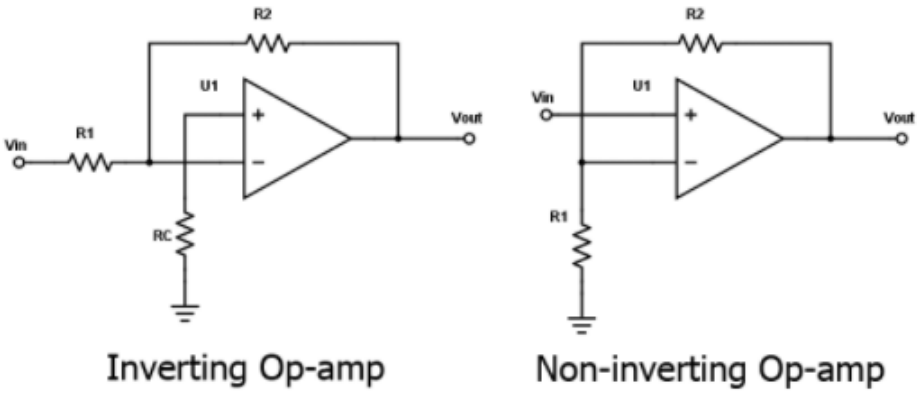

Figure 2.18: Non-inverting and inverting OpAmps [29].

The output voltages for the inverting Op-amp can be given as:

$$Vout = -\frac{R2}{R1}Vin \tag{2.3}$$

And the non-inverting can be seen as:

$$Vout = (\frac{R2}{R1} + 1)Vin \tag{2.4}$$

As a result of the operational amplifier development, the differential amplifier was created shortly after. This electrical circuit can calculate the difference between two analog inputs and then amplifies the output voltage. The instrumentation amplifier is created by combining some features seen in both the differential and operational amplifiers. Figure 2.19 shows an instrumentation amplifier topology.

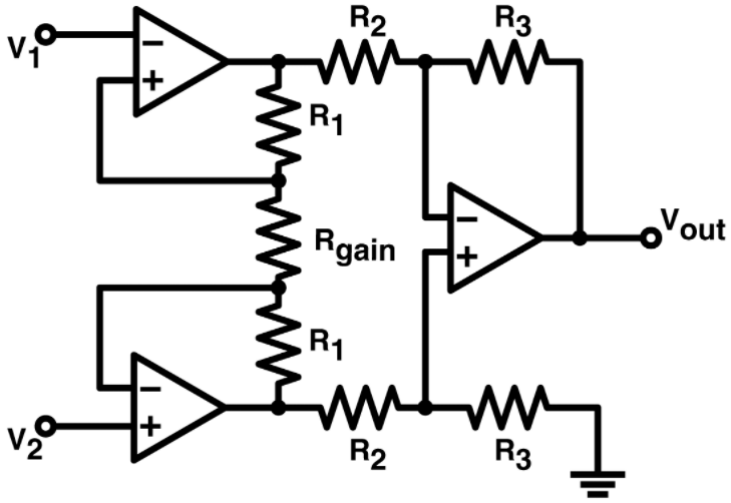

Figure 2.19: Instrumentation Amplifier Topology [30].

The output voltages for the instrumentation amplifier circuit can be given as:

$$Vout = (V2 - V1) * (1 + \frac{2 * R1}{R_Gain}) * (\frac{R3}{R2}) \tag{2.5}$$

2.4.2 Analog Filters

One of the most relevant electronic systems in today's technology is the filter. It's applied in some way or another in most modern hardware components. Some examples consist of radio communication, audio recording and image processing. Fundamentally, it is a circuit used to remove undesired frequencies from a signal. While there are many ways to classify a filter, this subchapter will focus on active and passive filters, and their frequency response.

Electronic filters can be classified by four different types of frequency response: low pass, high pass, band-stop and band-pass. Low pass and high pass filters are the most simple and common filters. The filters are designed to operate with a cut-off frequency, that will determine what frequencies are attenuated or not. It's possible to observe this behaviour in figure 2.20.

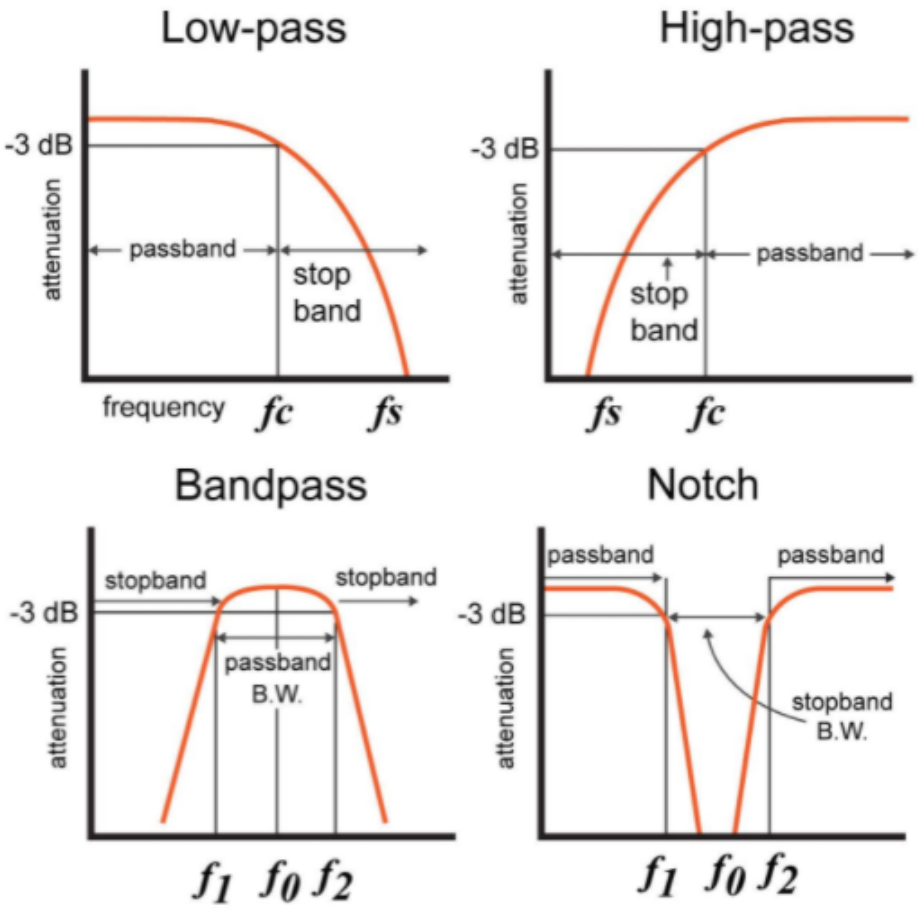

Figure 2.20: Filters classified by frequency response [31].

The low pass-filter, as the name indicates, will be designed so the frequencies below the cut-off frequency are not affected and the frequencies above are cut. The

reverse happens for the high-pass filter, where the frequencies above the cut-off frequency are not affected and the frequencies below are cut.

For the band-pass and band-stop (or notch filter as in the image) it's possible to do the exercise of imagining a low-pass and a high-pass filter connected in series, allowing for two cut-off frequencies to be dimensioned, creating a specific bandwidth that will either be accepted or cut from the circuit's output.

Since no electrical circuit is ideal, it's expected for the signal attenuation to increase or decrease gradually as the frequency changes. Even the cut-off frequency is already attenuated in relation to the input signal, being a standard to consider the frequency where the circuit gain is -3 dB as the cut-off frequency. A further analysis can be made to a filter's output signal [32].

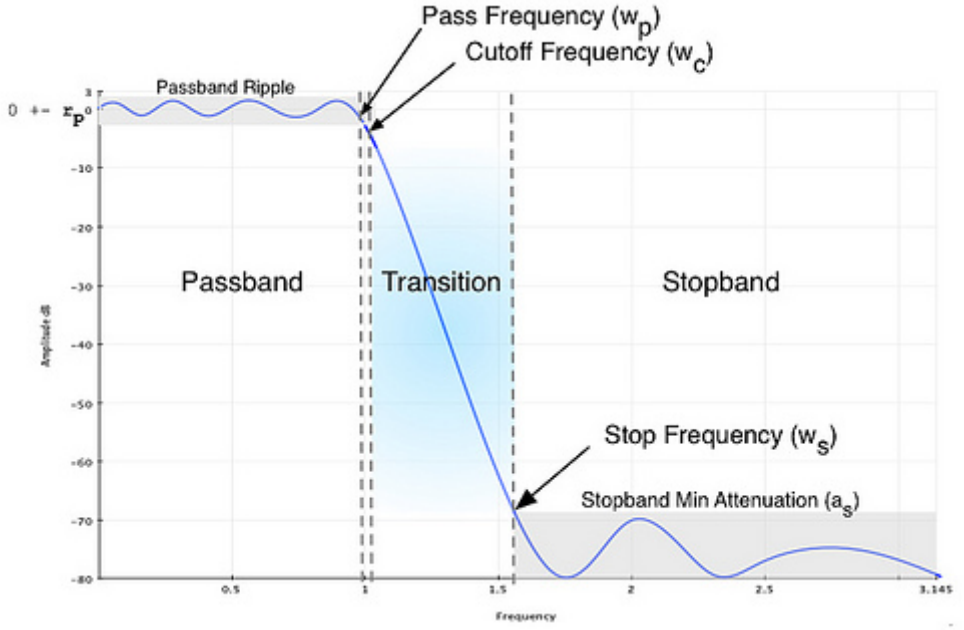

Figure 2.21: Low Pass filter frequency response [33].

A low-pass filter will be considered since it's the most used in this dissertation. Analyzing figure 2.21, it's possible to see the passband before the cut-off frequency as already studied prior. Next it can be seen the transition band, which is the band of frequencies after the cut-off frequency [32]. As it may be intuitive, a steeper transition band would be desired in almost every filter topology, when an ideal filter would cut any frequency right after the cut-off.

It's possible to create a steeper transition band by adding more filters with the same cut-off frequency to the circuit. If for example a circuit with three first order low-pass filters is made, it's called a third order low-pass filter, where the order means the amount of filter stages the circuit has. It's possible to visualize the frequency response in figure 2.22.

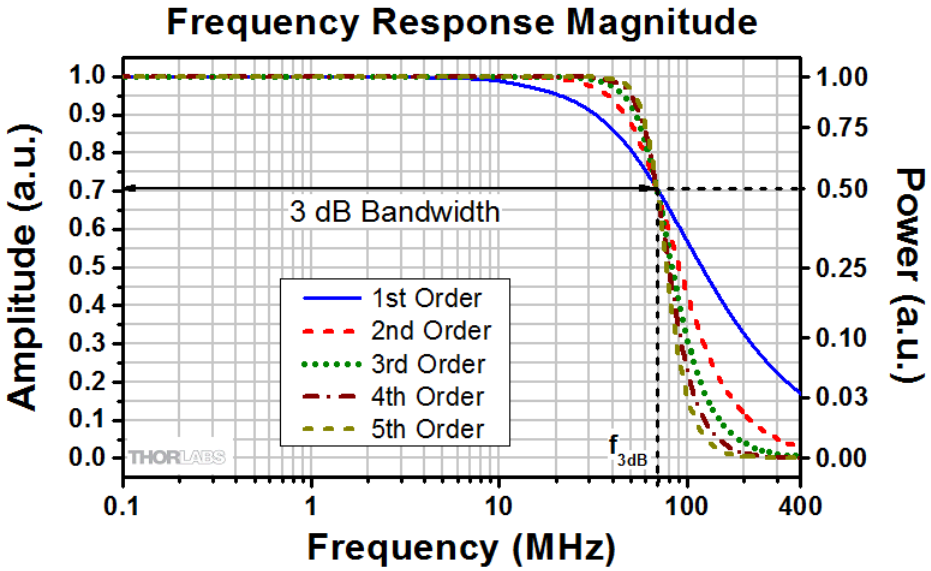

Figure 2.22: Low Pass filter frequency response in different orders [34].

The -3 dB bandwidth corresponds to 0.707 times the input voltage, or the inverse of square root of two. When calculating for power, the voltage will be multiplied by the current, that suffered an attenuation in the same ratio. The final result will be that a -3dB attenuation to the output signal will have half the power of the input. As it's possible to observe, as higher the order of the filter is, the steeper the transition band becomes.

It can be noticed that the payoff is bigger when going from a first order filter to a second order filter, compared to the transition for higher orders. A second order active filter can be designed with only one operational amplifier and four to five components depending on the topology used, making it a good design choice in general applications [32].

Second Order Low Pass Active Filters

Two low-pass second order active filter topologies were studied and used in this dissertation, the multiple feedback filter and the Sallen-Key.

The multiple feedback filter inverts the input signal and the calculation of its gain is the same as an inverting topology. The poles are determined by R1, R3, C1 and C2 values. The cutoff frequency for this filter can be calculated as:

$$F_Cut = \frac{1}{2\pi\sqrt{R2R3C1C2}} \tag{2.6}$$

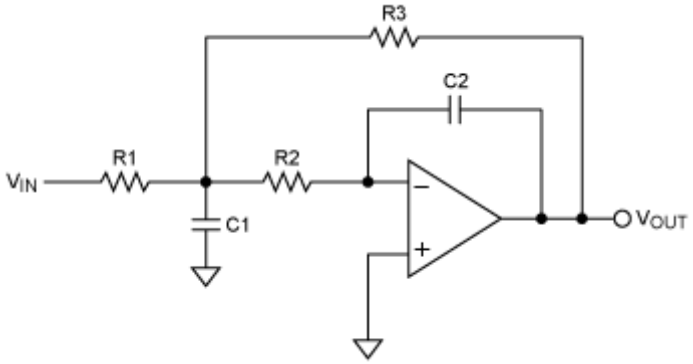

Figure 2.23: Multiple Feedback Low pass filter topology [35].

The Sallen-Key topology has a positive gain which follows the non-inverting topology. The poles are determined by the values of resistors and capacitors R1, R2, C1 and C2. The cutoff frequency for this filter can be calculated as:

$$F_Cut = \frac{1}{2\pi\sqrt{R2R1C1C2}} \tag{2.7}$$

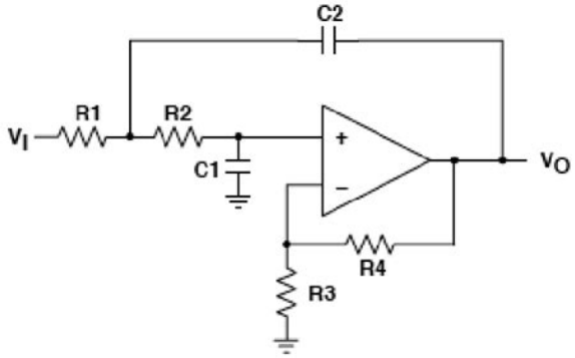

Figure 2.24: Sallen Key Low pass filter topology [36].

2.5 Communication Protocol

Since in this dissertation the goal is to have a portable system, a wireless communication protocol had to be chosen in order to perform data transmission to either a PC or a mobile device. Since most portable devices are designed for low-energy applications, the Bluetooth Low Energy (BLE) protocol seemed the right choice from the start. Nonetheless, more protocols were studied for this dissertation.

2.5.1 Bluetooth Low Energy

BLE is a wireless personal area network (WPAN) technology developed by the Bluetooth Special Interest Group. Uses frequency hopping in the 2.4 GHz band to connect with nearby devices and features maximum transmission rates of 1 Mbps with an energy consumption between 1-50 mW, depending on the application. Its theoretical maximum range is 100 meters (m), however, the practical range can vary between 10-20 m. It features a simple client-server model that allows for its development to be possible in less complex hardware devices. With these characteristics, this protocol is ideal for power constrained projects where only point-to-point communication is needed and the communication host can be close to the device, by either being in a close space or being also portable, such as a mobile phone [37].

2.5.2 Wi-Fi

Wi-Fi is a wireless local-area network (WLAN) technology (IEEE 802.11 standard) developed by the Wi-Fi Alliance. It can operate in the 2.4 GHz band and also in the 5 GHz band. This technology differs from other WPANs since it was not developed for the same purposes. By default its purpose is not to be used in low power applications, however as Wi-Fi is often accessible in the modern world, it offers a flexibility that might be desired in some applications where low power is desired but not critical [38].

2.5.3 Zigbee

The ZigBee protocol is a standard communication protocol, developed by the ZigBee Alliance, for wireless mesh networks, whose belonging devices require low power and a high-reliability factor for their operation. It is based on the IEEE 802.15.4 standard, referred to as Low Rate PAN (LRPAN) [39]. This protocol allows the transmission of data over long distances by passing information through a mesh network of intermediate nodes to reach distant ones. Faced against the BLE, it's a better option for situations where longer ranges are needed, for example farming and industrial systems. Its mesh network nature is a great advantage for longer transmissions that are often desired in one way or another in portable devices, but

it prevents every node that is able to extend the network to be idle. This forces a power consumption larger than the BLE protocol.

Chapter 3

PCG and ECG Acquisition Systems

In this chapter, the most relevant parts of the project will be presented in the following subchapters: system specifications, system architecture, PCG signal acquisition, ECG signal acquisition, microprocessor and the power circuit.

3.1 System Specifications

After studying the current state of art, it was possible to define the project requirements in a phased manner. The system will be developed based on the specifications defined in this chapter. The requirements are:

- Low power module;
- Compact and health compliant;
- Bluetooth Low Energy data transmission;
- Heart sound acquisition via PCG and ECG;
- Heart signal visualization from the different microphones, allowing comparison between each of the heart components.

For these requirements to be enforceable, all the necessary components and modules for the system well-functioning will be designed on a Printed Circuit Board

(PCB). The system will be composed of several independent modules responsible by the circuit power, acquisition and processing of the signal acquired by the microphone, the microprocessor and the antenna in order to send data via BLE. The power circuitry will include a battery and the respective charging and protection circuits. The module that regulates the voltage from 5 V to a 3.3 V voltage is also part of the system's power management. The microprocessor in addition to handling the received signal, creates a wireless network accessible to any mobile device that supports BLE. For all the components chosen for the project, dimensions and energy efficiency were taken into account. As of 2021, the market constraints for electronics and integrated circuits made somewhat of an impact in the execution of the final prototype, causing some deviations from the planned implementation, although not critical to the overall goal of this dissertation.

3.2 System Architecture

In order to explain the architecture, the signal acquisition circuit will be explained separately from the power module.

3.2.1 Signal Acquisition Circuit

The diagram presented in Figure 3.1 illustrates the blocks and components used in the system. It's comprised of four microphones each connected to a gain stage with a low pass filter stage before the microprocessor ADC. Each signal will then be converted from analog to digital data, which then will be encapsulated in raw information to send via BLE to a supported device. The ending device will have an interface capable of decoding the information sent via BLE and drawing each signal acquired from the microphones separately.

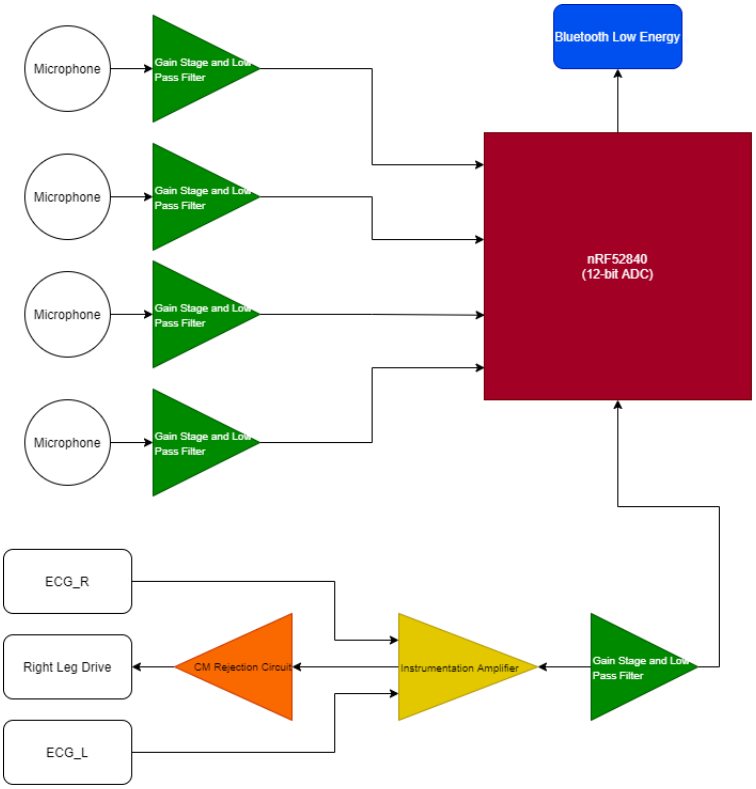

Figure 3.1: Signal Acquisition Architecture.

3.2.2 Power Architecture

For the power section, a charging battery topology was used, enabling the full module to be powered from a 4.2 V LIR2032 battery. It is also built in the circuit a universal serial bus (USB) connector in order to charge the battery and while the circuit can be powered from the USB for debug purposes, it's not recommended in its use case. A charge management controller is responsible for charging the battery if needed, while also protecting the power supply from reverse currents. The whole module uses 3.3 V as a power voltage, so a linear dropout regulator is used in order to achieve that voltage from either power supply.

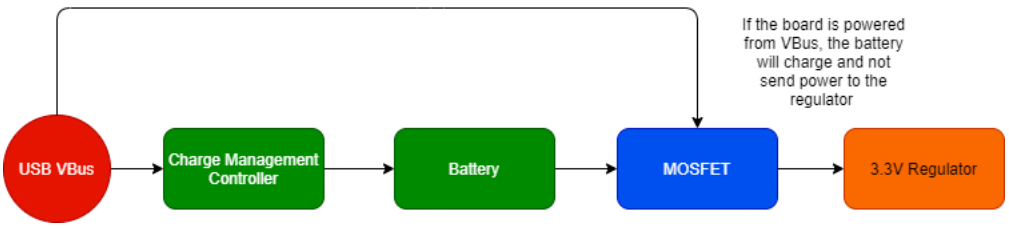

Figure 3.2: Power Architecture.

3.3 PCG Circuit

In this section there will be an exposure and explanation of all the components used for the PCG circuit, as well as the electric simulations made for its evaluation.

3.3.1 Microphone

One of the specifications for this project was to choose a MEMS microphone to acquire the heart sounds. Various parameters were taken into account such as the microphone impedance, RF immunity and frequency response. The final choice was the ICS-40180 from Invensense.

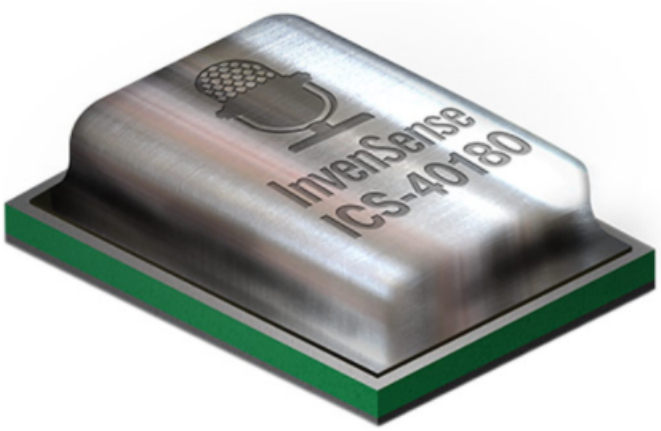

Figure 3.3: Microphone [40].

Some of the features of the ICS-40180 are listed below:

- High SNR of 65 dBA
- High Sensitivity of -38 dBFS
- Flat Frequency Response from 60 Hz to 15 kHz
- 350Ω output impedance

The frequency response of the microphone was a strong requirement due to the nature of the project. Most of the MEMS microphones in the market are built for audio and human voice application and have a functional frequency response with minimum frequencies of 100Hz. Since the heart sound has a medium range of 50-200 Hz, it was important to find a microphone with a good frequency response for lower frequencies [41].

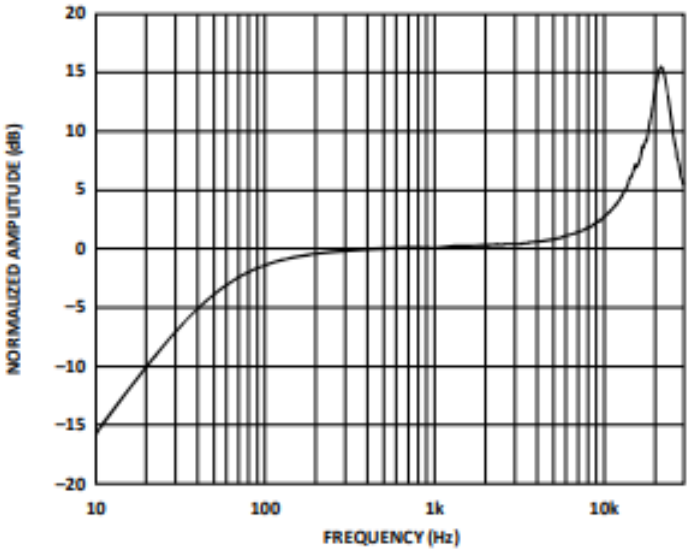

Figure 3.4: ICS 40180 Typical Frequency Response (Measured) [41].

The ICS-40180 functions as an analog microphone. As it's possible to perceive from the figure 3.5, it includes a MEMS microphone element, an impedance converter, and an output amplifier. The embedded circuit is enough to connect the output signal almost directly to any ADC, requiring only a decoupling capacitor between them [41].

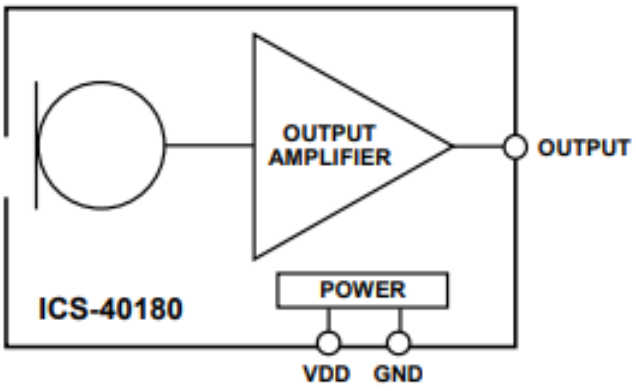

Figure 3.5: Microphone Functional Block Diagram [41].

Doing the exercise of treating the microphone as a voltage generator in order to study the PCG circuit implemented, we can assume a sine-wave with 0.7 V DC offset voltage and 100 mV peak-to-peak Alternate Current (AC) voltage.

3.3.2 Operational Amplifier

The chosen operational amplifier for the PCG circuit was the OPA333 and its OPA2333 variant. This series of complementary metal–oxide–semiconductor (CMOS)

operational amplifiers are able to provide very low offset voltage (10 µV, maximum) and near-zero drift over time and temperature, having ideal characteristics in providing high performance in driving ADCs without degradation of differential linearity. They offer high-impedance inputs that have a common-mode range 100 mV beyond the rails, and rail-to-rail output that swings within 50 mV of the rails [42].

Some of the specs of the OPA2333 include:

- Low Offset Voltage: 10 µV (Maximum
- Zero Drift: 0.05 µV/°C (Maximum)
- 0.01-Hz to 10-Hz Noise: 1.1 µVPP (10 µV, maximum)
- Quiescent Current: 17 µA temperature.
- Single-Supply Operation inputs that have a common-mode range 100 mV
- Supply Voltage: 1.8 V to 5.5 V

Since the OPA2333 is a surface mount device (SMD) component, initial prototyping was made in breadboards using TL074 op amps. While any operational amplifier would partially satisfy the requirements for the signal acquisition, the need for implementing a low power circuit without compromising much of the signal resolution justified the use of a more polished and application designed ICs (integrated circuits).

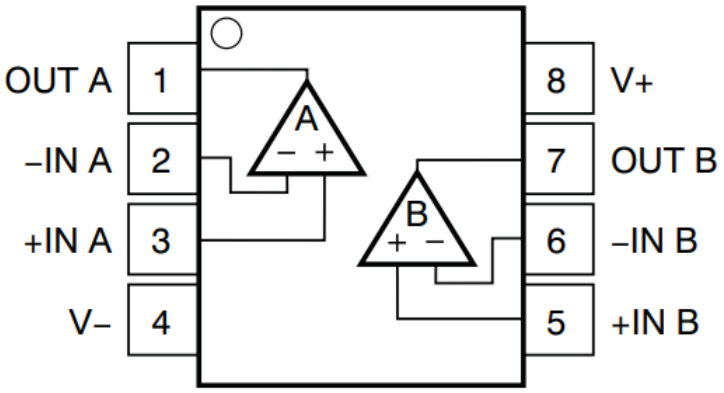

Figure 3.6: OPA2333 Pinout [42].

3.3.3 Gain Stage

In the gain stage, where VG1 represents the ICS-40180, an inverting operational amplifier was used. The capacitor C1 functions as a decoupling capacitor to block the DC component from the microphone output. A 2.2 µF capacitor was used to comply with the datasheet recommendations. The R1 and R4 resistors are designed to amplify the signal in a ratio of 15. R4 value can be adjusted according to the microphone output response. A simulation for this circuit was made with the TINA-TI software from Texas Instruments, as well as all the other simulations made in this dissertation.

$$Gain = \frac{-R4}{R1} \tag{3.1}$$

The inverting configuration will mean that the signal will invert in this stage. While the next stage has a filter with an inverting configuration as well, correcting the inversion, signal integrity will only be possible if the reference voltage is half of the voltage supplied to the OpAmp. A voltage of 1.65 V, being half of 3.3 V, is applied to the non-inverting input through a resistor parallel network with values similar to R1 and R4, as seen in figure 3.7.

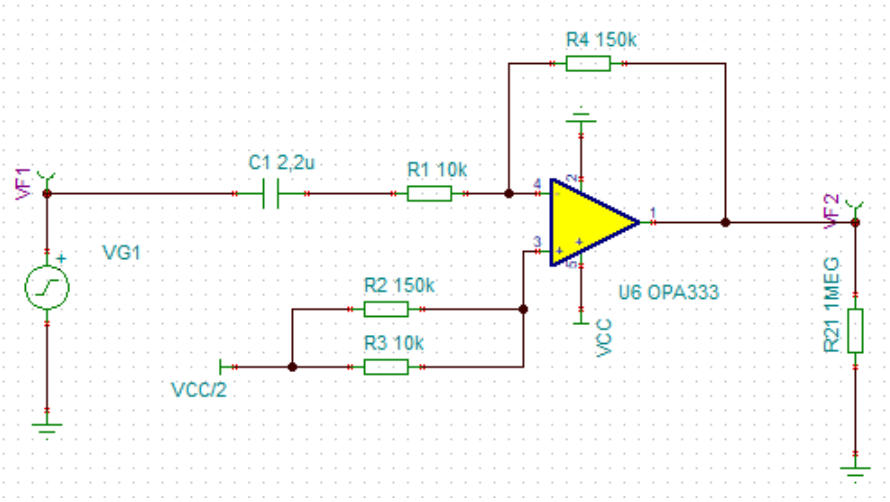

Figure 3.7: Gain Stage Schematic.

It's possible to see the output signal from the transient analysis in figure 3.8, where the brown signal is VG1 and the green signal is VF2. The circuit is designed so the output signal is contained with some margin from the 0 and 3.3 V respectively.

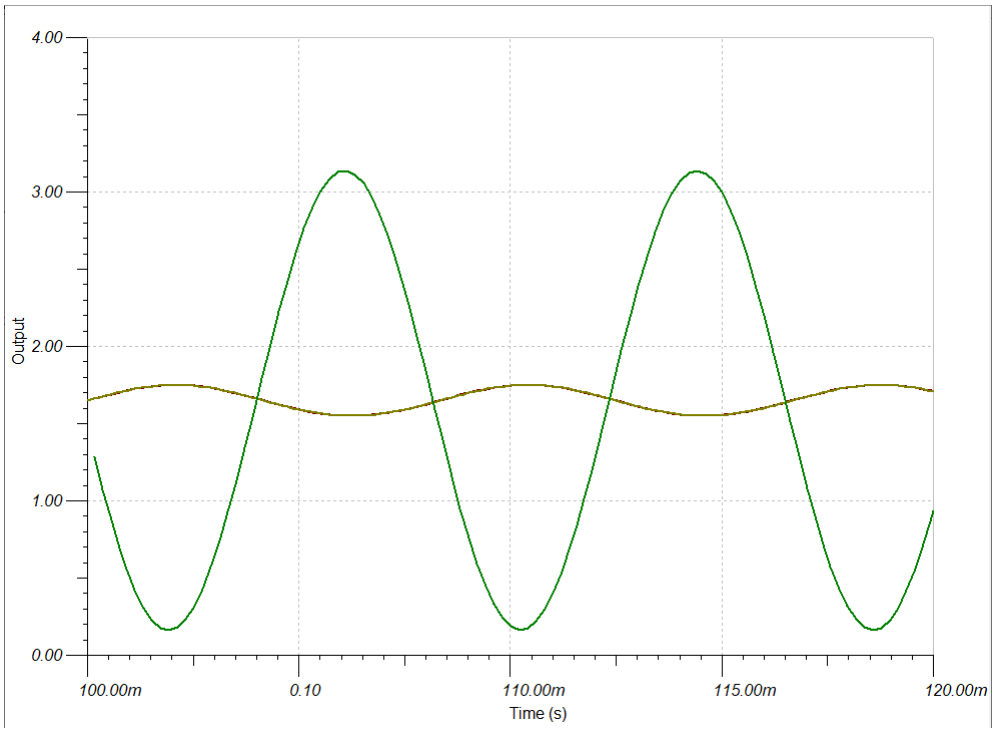

Figure 3.8: Gain Stage Transient Analysis.

3.3.4 Multiple Feedback Filter

The Multiple Feedback Filter used in the PCG circuit is a 2nd-order inverting signal route low-pass filter. This topology was chosen for the filter stage over the Sallen-Key filter for two main reasons:

- There is no gain for the non-inverting current noise and/or DC bias current. In this circuit the noninverting input is connected to the reference voltage.
- The in-band signal gain is set by – (R1/R2). This allows for R3 to be adjusted as desired, so it's possible to set the Q of the filter without changing the filter's central frequency.

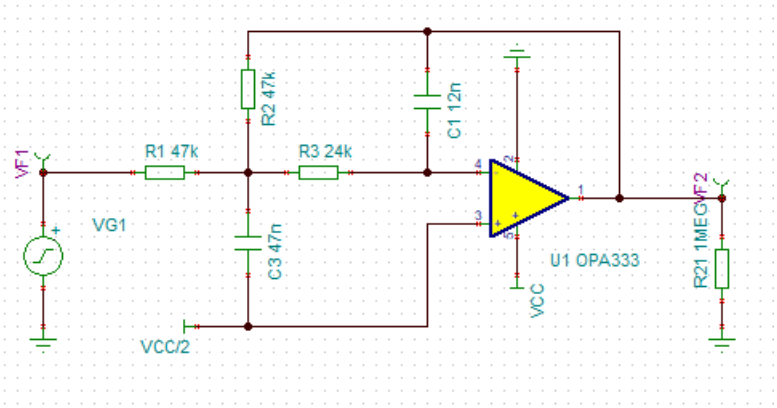

Figure 3.9: Multiple Feedback Low-Pass Filter Circuit.

Being able to set the desired Q in this filter was important so the circuit could represent an underdamped system. To explain briefly, an underdamped system is one where the Q factor is greater than a half. When a step impulse is delivered, systems with a Q factor of less than half may oscillate once or twice before the oscillation fades away. As the quality factor rises, the damping decreases, allowing oscillations to last longer. The oscillation would be maintained endlessly without the need for any further stimulus in a theoretical system where the Q factor is infinite. Some signal is fed back to offer an additional stimulation in oscillators, but a high Q factor usually results in a much cleaner outcome. Since there's some level of real time response wanted in this application, a Q factor over 0.5 was desired.

Since the circuit is designed for gain equal to 1, the Q function can be described as:

$$Q = \frac{\sqrt{R2R3C1C2}}{R2C1 + 2R3C1} \tag{3.2}$$

For the values chosen for this filter, the Q will be 0.707, making it an underdamped system. With this value a Butterworth frequency response can be expected.

$$Q = \frac{\sqrt{24k * 47k * 12n * 47n}}{24k * 12n + 2 * 47k * 12n} = 0.707 \tag{3.3}$$

The desired cut frequency for the low pass filter is 200 Hz. Heart sound signals are expected usually to go from 110 to 180 Hz, but a band ranging from 50 - 200 Hz is ideal for fully acquisition of these signals. As seen above in the microphone section, it only has an acceptable response from 60 Hz forward, removing the need for an high pass filter in the circuit. The cut frequency can be calculated in Hz as:

$$Fcut = \frac{1}{2\pi\sqrt{R2R3C1C2}} \tag{3.4}$$

$$Fcut = \frac{1}{2\pi\sqrt{24k * 47k * 12n * 47n}} = 200Hz \tag{3.5}$$

A full resolution of this filter can be consulted in Appendix A.7. In figure 3.10 it's possible to observe the AC analysis of the circuit. The simulation corroborates the 200 Hz cut frequency that the filter was designed for.

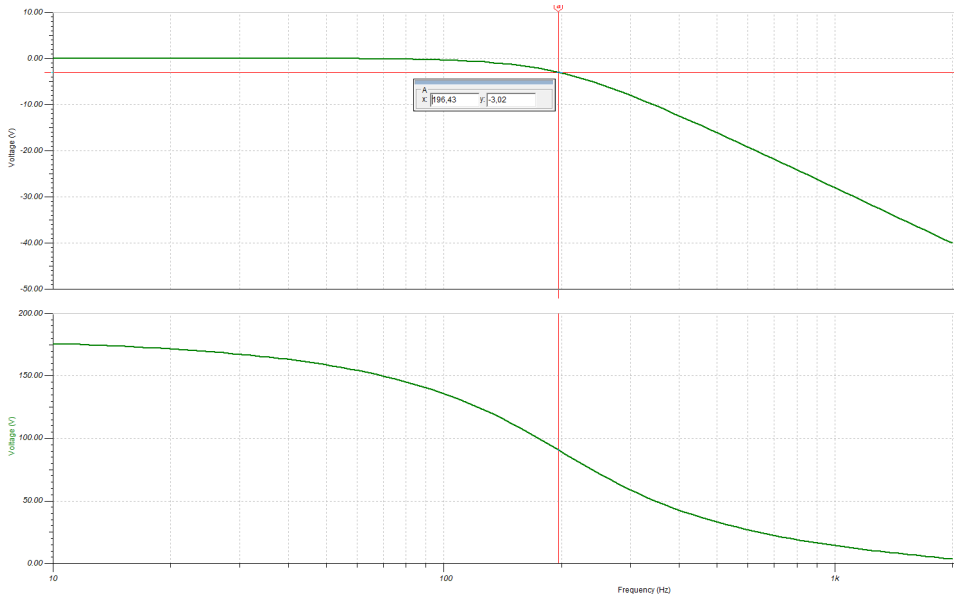

Figure 3.10: Multiple Feedback Low-Pass Filter AC Analysis.

3.3.5 Voltage Buffer

A voltage buffer (also called a unity-gain amplifier, a follower amplifier, and an isolation amplifier) is a op-amp circuit which has a voltage gain of 1. This means that the op amp does not provide any amplification to the signal.

Voltage buffers are generally used to isolate stages from each other. A voltage buffer has a high input impedance and a low output impedance. This means that no matter what circuit is supplying the input signal, it does not have to provide much current while the output of the voltage follower can maintain a constant voltage to the next stage.

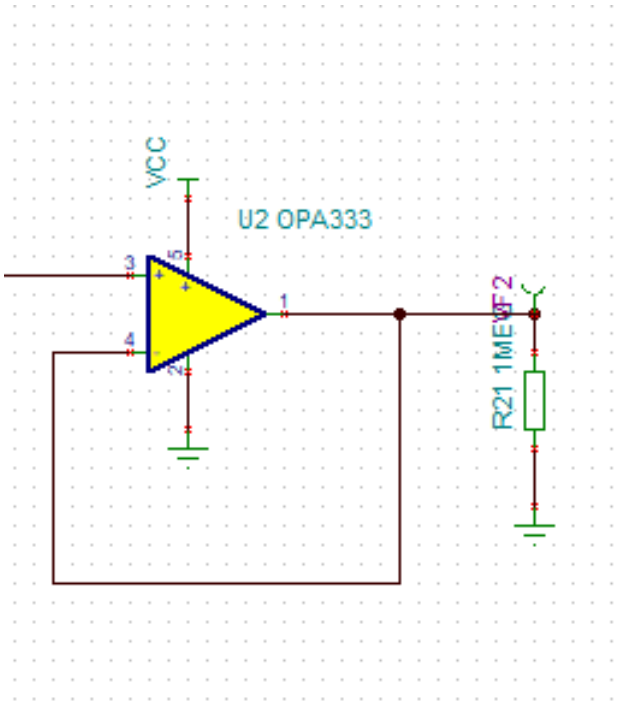

Figure 3.11: Voltage Buffer.

In the perspective of the PCG circuit, the voltage buffer will make sure the microprocessor's ADC circuit can measure the multiple feedback filter output without disturbing its integrity. The nRF52840's ADC has input protection that ensures it has minimal effect in the signal acquired, and this behavior was tested and verified in the making of the prototype.

Also, due to having 4 microphones in the final prototype, it's important to notice the cost adding 4 more operational amplifiers to the overall board, as it costs board space and some power to an extent. Ultimately, considering all the options, the compromise of using the voltage buffers was relatively low compared to the benefit of isolating the signal from the ADC.

3.3.6 Circuit Simulation

After studying the different stages of the signal conditioning, a simulation for the full circuit was done using the TINA-TI software from Texas Insrtuments. The PCG signal was emulated from an WAV file of a heart beating, provided by ThinkLabs from their Heart Sound Library. As seen in figure 3.12, it's easy to identify both S1 and S2 in a healthy heartbeat [43].

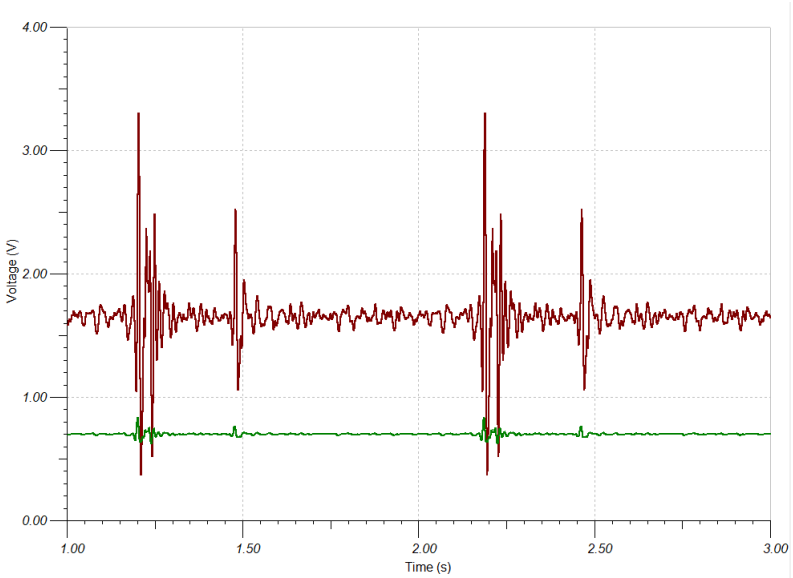

Figure 3.12: PCG Transient Analysis with a healthy heart signal.

It was also made a simulation to observe the output of a heart signal with congestive heart failure [43], shown in figure 3.13. It's possible to identify the added S3 component in the heart sound.

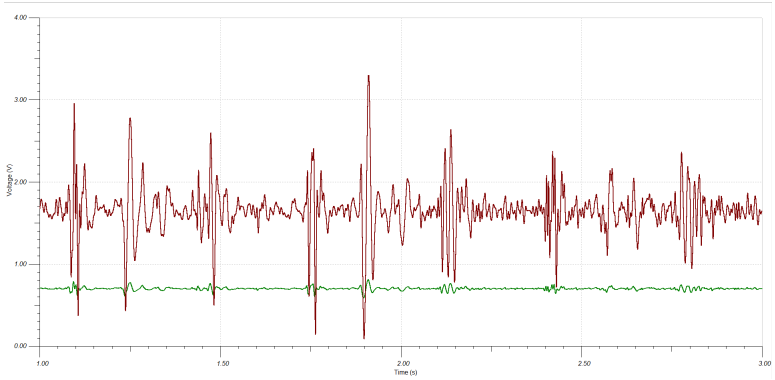

Figure 3.13: PCG Transient Analysis of a congestioned heart signal.

3.4 ECG Circuit

An added feature for this project is the acquisition of the ECG signal that was designed in the same board. The microprocessor will also be responsible for the analog-to-digital conversion of this signal, so only the inputs and a new signal conditioning circuit will be added. The ECG signals will be acquired from the patient's right and left arm. These signals will then be driven through an instrumentation amplifier in order to deliver its output to the processing stage. A third electrode will be connected to the patient, specifically in his right leg. This electrode purpose is not to be an input to the circuit, but to reduce amplifier interference in the circuit by enhancing its common mode rejection ratio (CMRR).

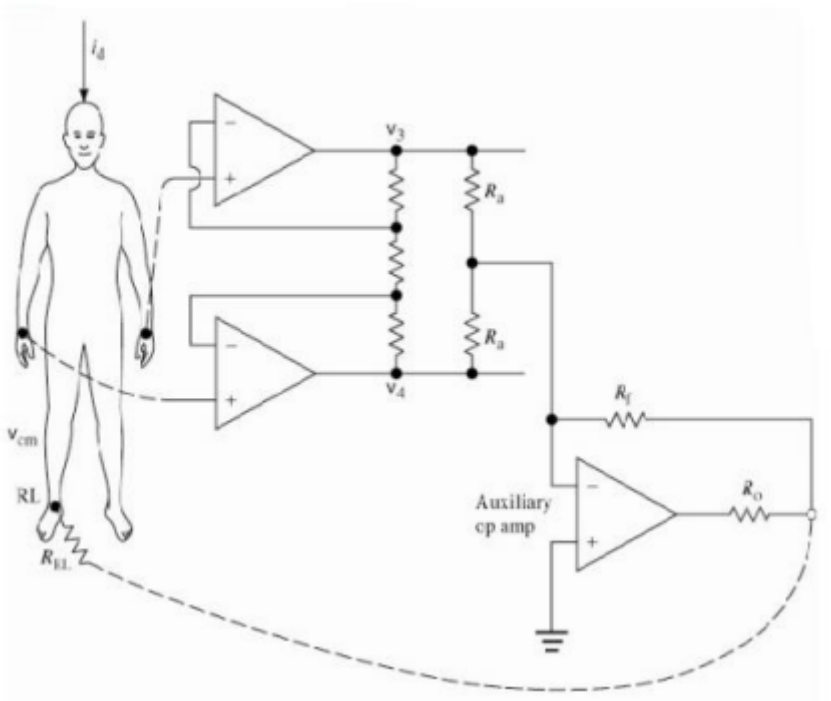

Figure 3.14: ECG patient connections [44].

3.4.1 Common Mode and Differential Filtering

In the previous sub-chapter about the PCG, a voltage generator was used to simulate the output signal from the MEMS microphone. In this circuit, we needed to simulate both the ECG signal coming from the patient, as well as modulate the resistive and capacitive effect of the electrodes used in the patient. In the software used for simulation, an ECG source was already pre-built.

The next stage is a common mode and differential filter used to mitigate Electromagnetic Interference (EMI) and Radio Frequency Interference (RFI) noise, and it's used and generally recommended by Texas Instruments in application notes and design guides. Taking into account that this module architecture implies radio communication, the usage of this circuit is indispensable to its well-functioning. While most common-mode signals present at an instrumentation amplifier input are normally greatly reduced by the amplifier's common-mode rejection, RF rectification will still occur because even the best instrumentation amplifiers have virtually no common-mode rejection at frequencies above 20 kHz.

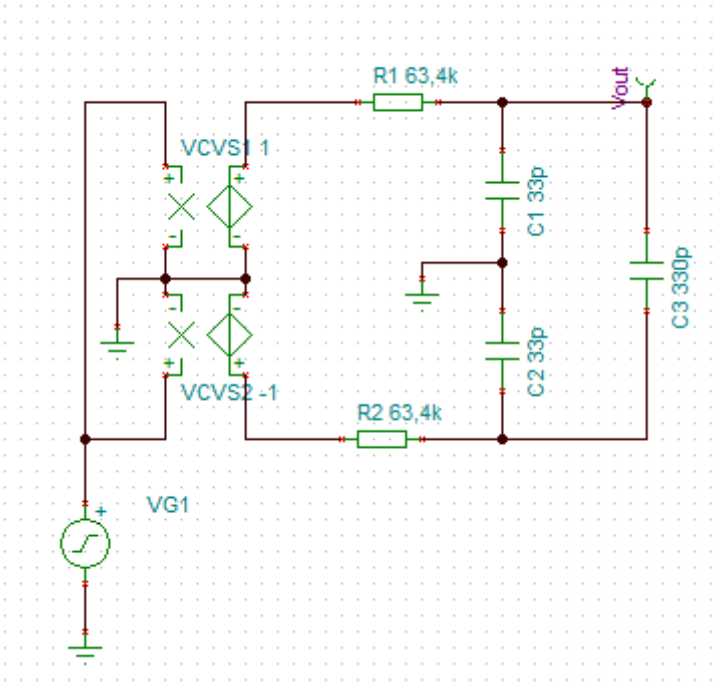

Figure 3.15: Differential Low Pass Filter.

The low pass filter is designed for 3622 Hz. For this circuit is critical that both the resistors and the capacitors from each input match. The resistors used in the PCB for this filter have 1% precision and both capacitors have 5% precision. The circuit differential cut-out frequency can be calculated as:

$$Fcut = \frac{1}{2.\pi.(R1 + R2).(\frac{C1.C2}{C1+C2} + C3)} \tag{3.6}$$

$$Fcut = \frac{1}{2.\pi.(63.4k + 63.4k).(\frac{33p.33p}{33p+33p} + 330p)} \tag{3.7}$$

$$Fcut = 3622Hz \tag{3.8}$$

An AC analysis was made for this filter. A differential voltage source was implemented by connecting two constant sources to both inputs. This is made because the TINA-TI software can only interpret a single input for an AC analysis. As it's possible to see in figure 3.16, the cut-off frequency for this circuit is 3.62 kHz, this being the expected value.

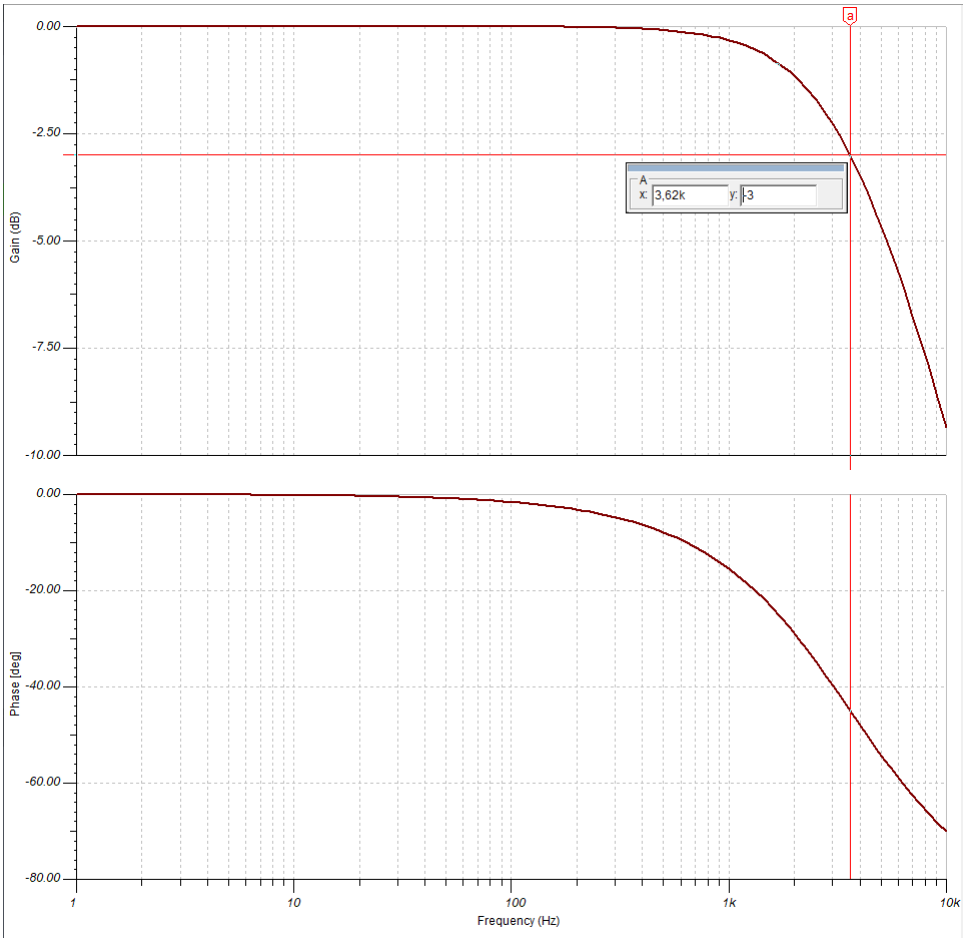

Figure 3.16: ECG EMI/RFI AC Analysis.

3.4.2 Right Leg Drive

The purpose of the right leg driving circuit is to reduce common-mode amplifier interference. Electrically, an ECG signal can be amplified and a DC common mode bias can be created using the differential amplifier's inputs. When this is done, however, there is a high risk of common mode interference, necessitating the use of the right leg drive. As indicated in figure 3.17, the right leg drive inverts and amplifies the average common mode signal before returning it to the patient's right leg. This procedure removes most of the 50/60 Hz noise from AC electricity, resulting in a clearer ECG signal. This enhances the ECG circuit's common mode rejection by a factor of (1 + A), where A is the feedback loop's gain.

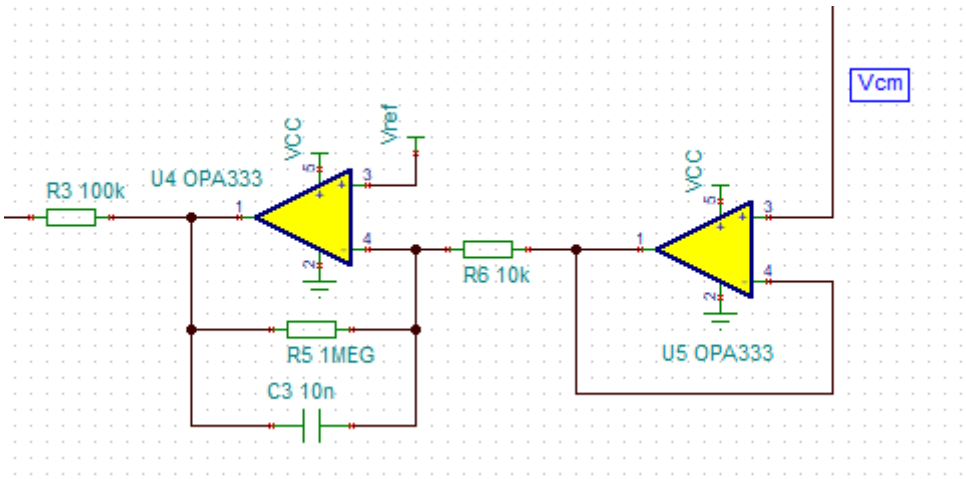

Figure 3.17: ECG Right Leg Drive Circuit.

This circuit uses two op-amps. The first one is a voltage buffer, driving the common mode voltage from the instrumentation amplifier into the next op-amp, with similar functions with the ones explained in the PCG chapter. The second operational amplifier uses an inverted topology and its used to amplify the signal, increasing the common mode rejection as previously explained. The capacitor C3 will filter the lower frequencies and its used to provide control over the circuit's bandwidth. Resistor R3 is used to reduce the maximum current driven to the patient. For 3 V powered circuits, a minimum value of 60 kΩ is recommended, making a 100 kΩ resistor a valid value for patient protection.

3.4.3 Instrumentation Amplifier

For the instrumentation amplifier in itself, the only design component to be approached was defining the RG resistor. Following INA126's datasheet, the formula for the in-amp gain is:

$$G = 5 + \frac{80k\Omega}{RG} \tag{3.9}$$

The right leg drive circuit requires the common-mode voltage to be connected as an input, so a 2-resistor network is used in RG. Two precision 6.3 kΩ resistors were used, making RG equivalent to 12.6 kΩ. The gain then becomes:

$$G = 5 + \frac{80k\Omega}{12.6k\Omega} \tag{3.10}$$

$$G = 11.34 \tag{3.11}$$

Since the ECG signal will be driven to the ADC, it needs a reference voltage to stay between 0 and 3.3 V. In order to do this the INA126 reference pin needs to be driven with the reference voltage. The reference voltage is driven through an OPA333, so it provides a low impedance input at the Ref pin, which is used as another common mode rejection technique.

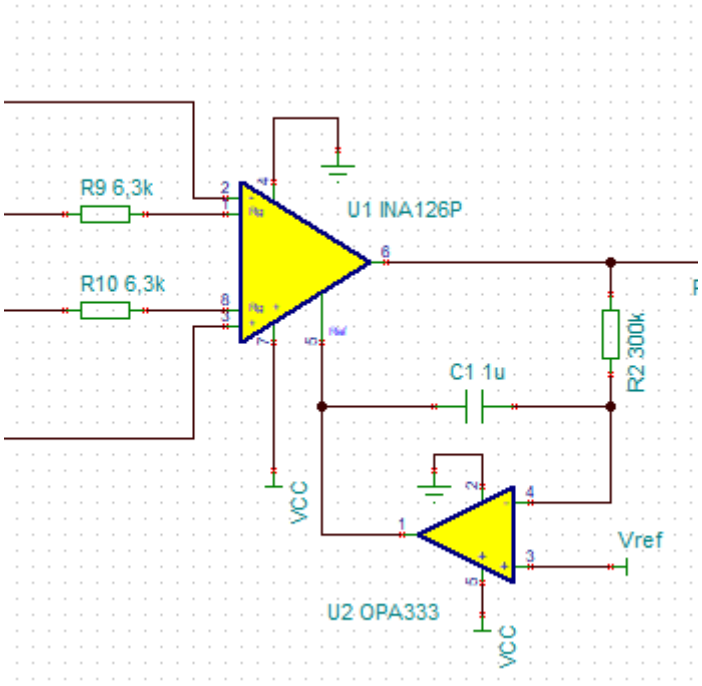

Figure 3.18: Instrumentation Amplifier.

3.4.4 Low Pass Filter

A low pass-filter was used in the ECG circuit. Since a voltage reference different than half the voltage power was used, inverting the signal was now undesired, making the Sallen-Key a better option this time against the Multiple Feedback Filter as shown in figure 3.19.

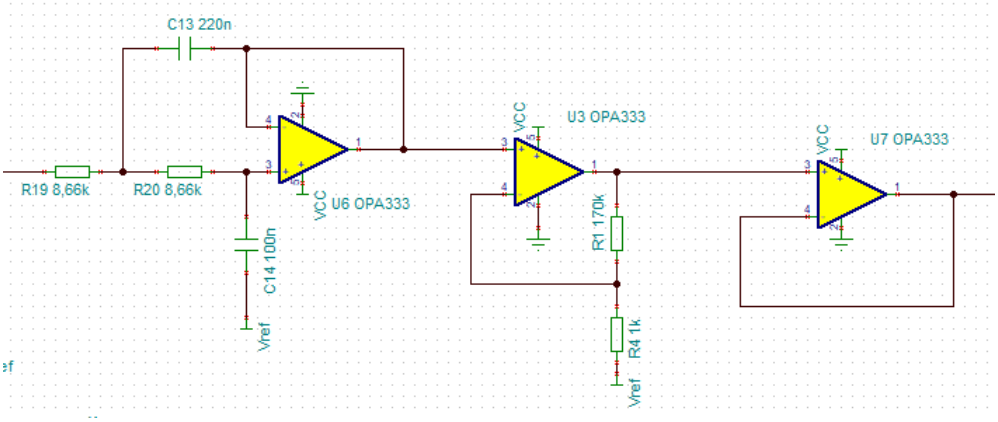

Figure 3.19: Sallen-Key Low Pass Filter.

The filter was designed to to have a cutoff frequency of 125 Hz. The filter was designed for similar Q values as the PCG circuit. For market availability effects, the capacitors were chosen first, and were dimensioned to be 220 nF for C1 and 100 nF for C2. For a 125 Hz value, 8.56 kΩ resistors were needed. Adjusted to market values, 8.66 kΩ resistors would work in this design, making the cut-off frequency 123 Hz, which is a valid compromise. The full design of this filter can be consulted in Appendix A.6. The cut-off frequency can be calculated as follow:

$$Fcut = \frac{1}{2\pi\sqrt{R1R2C1C2}} \tag{3.12}$$

The AC analysis of this filter is presented in figure 3.20. It's possible to verify the cut-off frequency at -3dB to be 123 Hz, which is the expected value. The signal phase of -90 degrees is also expected.

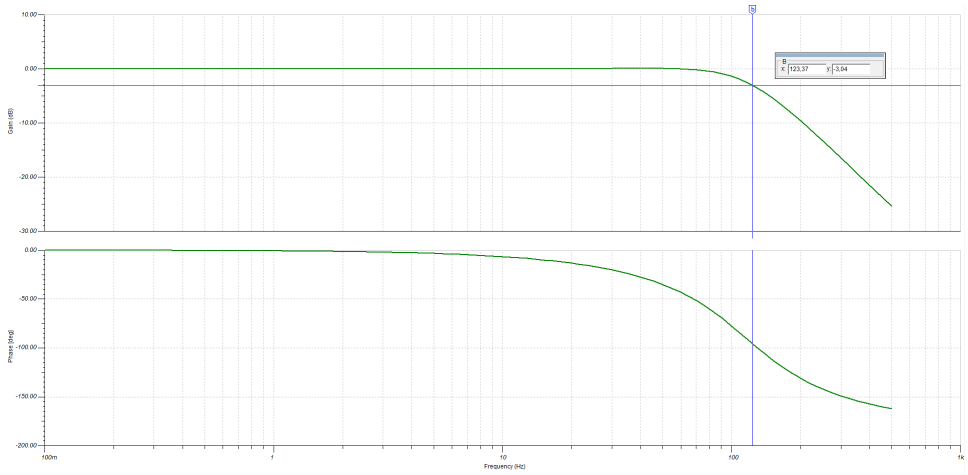

Figure 3.20: AC Analysis of the Sallen-Key filter.

The transient analysis of the full circuit can be seen in figure 3.21. Two ECG synthetic signals were used as the circuit input, and can be seen in the figure below as ECGn and ECGp. Analyzing the Vout signal it's possible to perceive the full use of the 3.3 V range, which will provide the best signal-to-noise ratio of the circuit output.

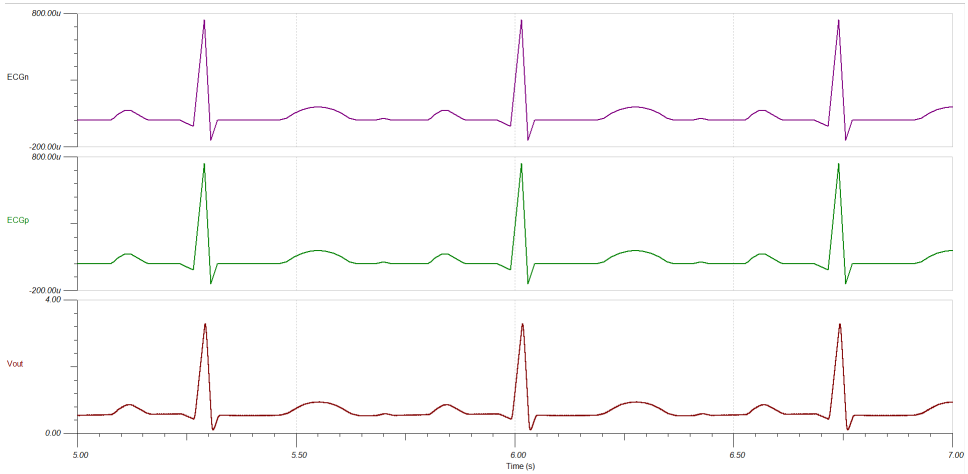

Figure 3.21: Transient Analysis of the full ECG circuit.

3.5 Microprocessor

An essential component of the project architecture was a piece of hardware to convert the PCG and ECG analog signals into digital. Having all post analog front-end specifications in mind, the ideal solution would be a module capable of taking all the analog signals as input and convert them into digital data to be sent via a wireless protocol, all while consuming the least possible power to do so. With this information in mind, the Nordic nRF52840 fulfilled all requirements for accomplishing the signal processing and communication tasks.

The nRF52840 consists of an ARM Cortex M4, at a frequency of 64 MHz. Supports BLE (high-speed 2 Mbps), and other proprietary 2.4 GHz protocols. Depending on the package, it can have 512 / 216 KB of Flash memory and 64 / 32 KB of Random Access Memory (RAM). Its operating voltage can vary between 1.7 and 3.6 V, facilitating its use with a battery. In terms of energy consumption, these devices are designed to have low current consumption, and in sleep mode, it can be only 2 to 3 mA [45].

Another important aspect is the peripherals. The nRF52840 has an ADC with a 12-bit resolution and 200000 samples per second. It also has Serial Peripheral Interface (SPI), I2S, universal asynchronous receiver-transmitter (UART) interfaces, and a 32-bit timer/counter. Furthermore, it also has 32 configurable General Purpose Input/Output (GPIO). The application of these devices is vast and can be used in home automation, personal area networks, including monitor and medical devices, remote controls, and computer peripherals [45].

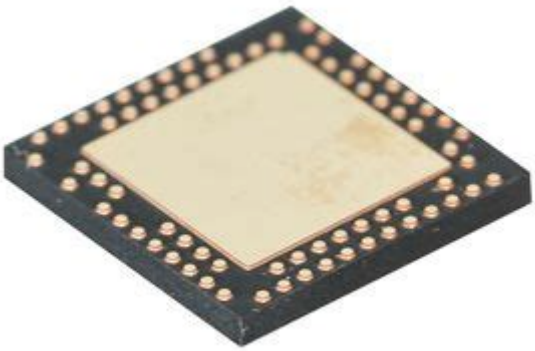

Figure 3.22: nRF52840 QFN package [46].

This microprocessor is very power-efficient, presenting a maximum 16.4 mA consumption when powered at 3 V. Also, it has a sleep mode when idle that has a consumption is the µA order, making it an ideal multiprocessor for low power applications [45].

An issue that surged when designing the prototype was that both packages the nRF52840 was available at the time required expensive manufacturing techniques from the PCB factory. While in a mass production perspective this situation would not be a constraint, it represented a monetary cost disproportionate to the nature of this dissertation.

Figure 3.23: Raytac MDBT50Q module [47].

The solution was to use the MDBT50Q module from Raytac. This module consists of a board designed with the nRF5240 main schematic, prompt to be used as a daughter-board in a larger design. It also comes with a pre-built antenna for BLE applications.

3.5.1 SAADC

The Successive Approximation Analog-to-Digital Converter (SAADC) peripheral has a configurable resolution, effectively going from 8-bit to 12-bit. It can reach 14-bit resolution through oversample technique. The nRF52840 SAADC has eight input channels, being able to operate in four different modes. One-shot mode, where the SAADC samples a single channel. Continuous mode, where only one channel is enabled, but the sampling rate can be configured either by the internal timer in the ADC or through general-purpose timers. It also has the oversampling mode, where an accumulator is used to average noise on the input channel, and makes possible to return values in the 14-bit resolution range.

At last, the ADC uses scan mode by default when more than one channel is enabled. In this mode, a sample task triggers one conversion for each enabled channel. As this project aims to obtain the values from more than one channel, scan

mode will be used. It's important to note that the oversampling technique cannot be used when multiple channels are being scanned, not being supported by the microprocessor.

The ADC may be configured as single-ended input (the internal ADC ground is the same as the external ground) or differential input (2 channels can be configured as "+" and "-"). The ADC also uses Easy Direct Memory Access (EasyDMA) to directly store the results in RAM, allowing for the CPU to consume less power [45].

In this project perspective, the SAADC was configured to have 5 channels as single-ended input, in scan mode (more than 4 differential channels are not possible). In scan mode the Programmable Peripheral Interconnect (PPI) is used to generate the SAADC sampling rate, which will allow the CPU to be spared of this task. As opposite, the EasyDMA will be running indefinitely, representing an expected consumption of about 1 mA [45]. This doesn't represent a big compromise as the nature of the project requires a continuous and precise sampling of the heart signals as a priority.

All signals were sampled at a frequency of 400 Hz, using a 12-bit resolution. As the maximum frequency wanted to acquire is the 200 Hz from the PCG signal, the minimum frequency at which is possible to sample the signal according to the Nyquist theory is two times that value, so 400 Hz. It would be optimal to choose a higher sample frequency in this scenario, as the increase in bandwidth would provide a more precise analysis of the signal and at first sight seems there's no constraint to do so. However, it must be taken into account that every acquired sample has to be transmitted via BLE. Data transmission via BLE would represent a higher constraint for increasing the sampling rate in this situation, so settling for the minimum frequency required to read the signal correctly would be the most sensible approach. A further explanation will be given in the next sub-chapter.

An analysis can be made on the flow of the implemented SAADC. After the timer initialization and the SAADC parameter configuration, the PPI will trigger an event that causes the SAADC to sample one of the 5 signals. For each event, only one signal can be sampled. After the event is done, the microprocessor will write the registered value in a external buffer. When this buffer is full, a bluetooth notification will be sent. This event can be dealt in parallel with the ADC, meaning that while the connection is active, the ADC will keep sampling the signals.

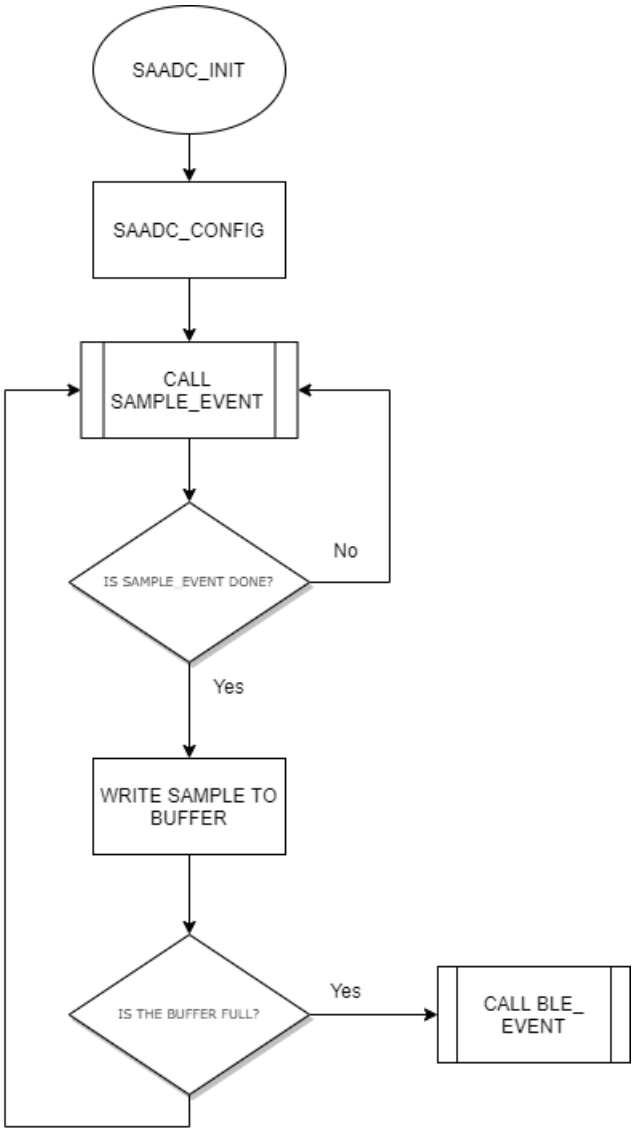

Figure 3.24: SAADC Fluxogram.

3.5.2 BLE

The BLE is the chosen wireless protocol used for data transmission. The BLE architecture can be divided in three different protocols, the Generic Access Profile (GAP) and the Generic Attribute Profile (GATT), which is built on top of the Attribute Protocol (ATT). The GAP will define the framework and the devices' roles when they engage with one another. It also takes care of advertisement related details including data and settings. The GAP can attribute four different roles, being:

- Broadcaster
- Observer
- Peripheral
- Central

The broadcaster is a device that broadcasts data packets on a regular basis but does not allow for the establishment of a link. The Observer listens for data packets but does not attempt to connect to the broadcaster. The Peripheral only advertises its presence rather than data packets and waits for a link to be established. Finally the Central waits for the peripheral to transmit the advertising packets before initiating communication [37].

The GAP is the protocol responsible for handling the communication between peripheral and central devices. The central device can establish various parameters that will define the communication between them. These parameters are the Connection Interval, the supervision timeout and the slave latency. The connection interval defines the time between data requests from the central, the supervision timeout defines the time the devices may try connect until a packet loss happens, and the slave latency is the number of connection events the peripheral is allowed to skip. An example of these values will be given further [48].

The GATT is concerned with the format of data transferred between devices, especially with the exchange of ordered attribute/value declarations. It adds a layer of hierarchy to declare these attributes as features of services inside profiles, building on the more generic Attribute Profile, which specifies a protocol for sharing Attribute Handle, type, UUID, and value data (the hierarchy is implemented by declaring some of these attributes in the ordered list as start-of-profile and start-of-service markers). Independent of the GAP connection, the network relationship between the exchanging devices is a typical client/server paradigm [48].

A GATT service is a container that aggregates conceptually similar characteristics into a single container. These qualities make up the service's Service Definition, which includes the following features and their descriptions. A GATT characteristic

is a data container that has a declaration attribute, a data value attribute, and possibly other descriptor attributes, together known as the Characteristic Definition. A service may be thought of as an object-oriented class, with its characteristics as members of that class [48] [37].

As mentioned in the previous sub-chapter, the BLE communication throughput is the biggest challenge when it comes to the sampling rate of the signal. The best strategy here was to understand the best compromise between throughput and packet integrity.

As of version 5.1 of the BLE protocol, the maximum theoretical protocol data unit (PDU) is 257 bytes. Of these 257, 2 bytes are locked for the data channel header, 4 bytes are used for integrity check and another 4 bytes are used the L2CAP header. The Nordic softdevice used for BLE communication in this project takes 3 bytes to configure an extra header, leaving then only 244 bytes free for communication.

Now, every sample taken by the ADC is saved in a 16-bit variable, which can be considered a two byte word. For every sample of all five signals, five words of two bytes each will amount to a total of ten bytes. Since there are 244 bytes available, it's possible to save up to 24 samples per signal on a signal PDU packet. For practical purposes, a 240 byte packet will be used since it's the maximum amount of information that can be sent where all the signals have the same number of samples.

The minimum connection interval between two BLE devices is 7.5 ms. In practice, a 15 to 25 ms interval is to be expected in good conditions (devices in close distance to each other).

For five signals sampled at 400 Hz, it means that 2000 samples must be transmitted in a second, or every sample must be transmitted every 0.5 ms. Knowing this, and since every packet contains 120 samples, we can conclude that a full packet must be sent every 60 ms. Sending a full packet is also the best strategy for power consumption, as this minimizes the number of connections needed for achieving a determined throughput.

Increasing the sampling rate would always carry the burden of increasing the number of connections made with the peripheral by default. Various tests were conducted for higher sampling rates, and it was possible to perceive an exponential loss of packets as the sample frequency went up. For the purpose of this system maintaining signal integrity had more priority, thus the sampling frequency chosen was 400 Hz.

3.6 Power Circuit

The portable acquisition system must have adequate power for each of its modules and components for proper functionality. Being a low-power device, the most common choice was to use a battery system. A lithium battery would be enough to power the whole system. For the prototype design, an USB connector was included in order to power the board directly from AC power, being also able to charge the battery.

3.6.1 Battery Charging Manager

When the system is connected to an external source of power, the battery is automatically charged until it reaches 100 % of its capacity, even the entire system is up and running. The component chosen to manage and charging the battery was the MCP73831 integrated circuit from Microchip, shown in the following image:

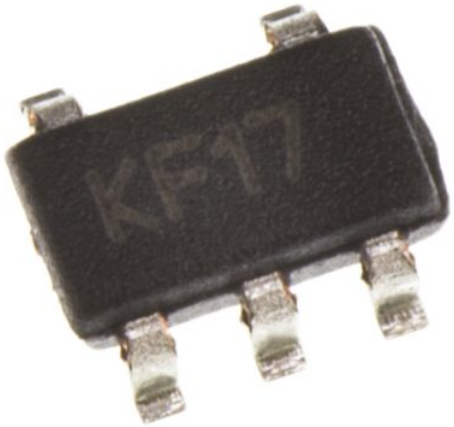

Figure 3.25: MCP73831 [49].

It is a complete linear constant current and voltage charger for single-cell lithium ion batteries. Because it is a component of reduced dimensions and in need of a reduced number of passive components, it is ideal for low-powered applications. This charging chip already has internal protections to block negative charge currents.

The voltage at which the battery is charged is 4.2 V, while the current can be programmed externally by changing the value of a single resistor. The charge cycle is completed only when the charge current drops 90 % relative to its programmed value. The charging current of the load can be analyzed, as well as the status the load and the presence of a voltage on the load. The typical circuit is shown in the following image:

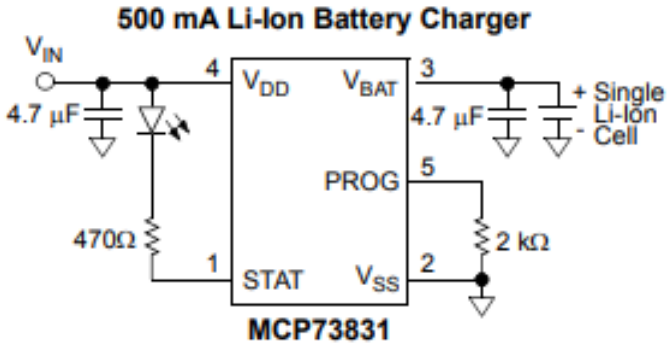

Figure 3.26: MCP73831 Typical Circuit [50].

In this example, the resistor between PROG and VSS is 2kΩ, which programs the charging current for 500 mA. The device has a linear formula for calculating the resistor to use for the desired current:

$$I_Reg = \frac{1000}{R_Prog} \tag{3.13}$$

The charging current can be as low as 15 mA and as high as 500 mA [50]. The tested operating point for the device is 100 mA and is also the value chosen in this project, deeming the R PROG value as:

$$R_Prog = \frac{1000V}{100mA} \tag{3.14}$$

$$R_Prog = 10k\Omega \tag{3.15}$$

3.6.2 Voltage Regulator

The nominal voltage values from the USB and the battery are 5 V and 3.7 V respectively. The signal acquisition circuit is built to operate in the 3.3 V range, so a voltage regulator is required to supply the proper voltage to the circuit.

Since this is a low power application and the power voltage can vary between 3 V to 5 V, due to the battery loss of power causing voltage loss, a Low Dropout linear regulator with low current supply current would be the ideal choice in this scenario. The chosen regulator was the Microchip MCP1727, with a 3.3 V fixed output.

The MCP1727 is a 1.5 A Low Dropout (LDO) linear regulator that provides high current and low output voltages. The MCP1727 comes in a fixed (or adjustable) output voltage version, with an output voltage range of 0.8 V to 5.0 V, being 3.3 V in this application. It presents 1.5 A of output current capability, exceeding by far the needs met for this design [49].

Also due to its CMOS construction, the quiescent current consumed by the MCP1727 is typically less than 120 µA over the entire input voltage range, making

it suitable for portable computing applications that demand high output current. When shut down, the quiescent current is reduced to less than 0.1 µA. The scaled-down output voltage is internally monitored and a power good (PWRGD) output is provided when the output is within 92 % of regulation. The overtemperature and short circuit current-limiting provide additional protection for the LDO during system fault conditions.

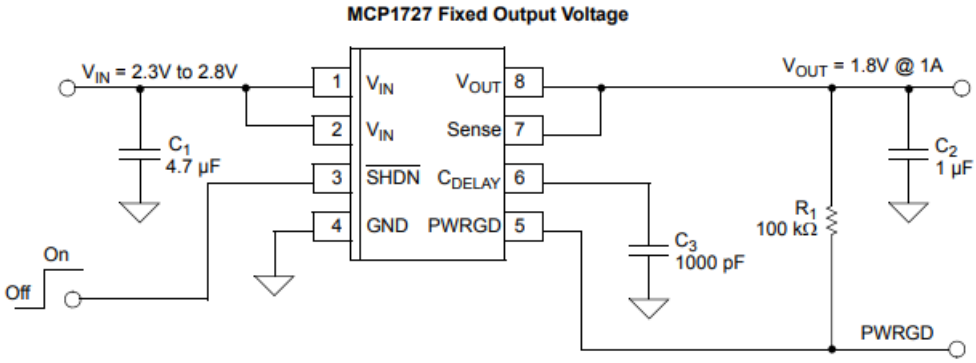

Figure 3.27: MCP1727 Typical Circuit [49].

Studying the MCP1727 recommended circuit, it uses an external capacitor for both voltage input and output. These capacitors are always recommended when designing with active components and are mainly used for ripple and power related noise attenuation. The SHDN pin is active low, and it's used to shutdown the regulator manually. The SENSE pin is used to provide the regulator feedback so it can compensate for voltage drops, improving load regulation. The C Delay pin allows for the designer to program the time threshold for the power good signal, which checks is the output voltage is within 92 % of the programmed value.

For the prototype schematic, the datasheet recommendations were used with the addition of some adjustments. Since this is the only regulator in the whole design, the SHDN pin must be always active and thus is connected directly to the power input via a 100 kΩ resistor. Having two functioning voltages for the input, some circuitry had to be implemented to manage the power usage. The design is made so the voltage from the battery (VBAT) works as the input only if VBus (voltage from the USB connector) is OFF. If VBus is ON, the P-channel MOSFET will turn OFF and VBus will be the regulator input voltage. A Schottky diode is also implemented so it prevents the current from VBat to leak to the VBus path.

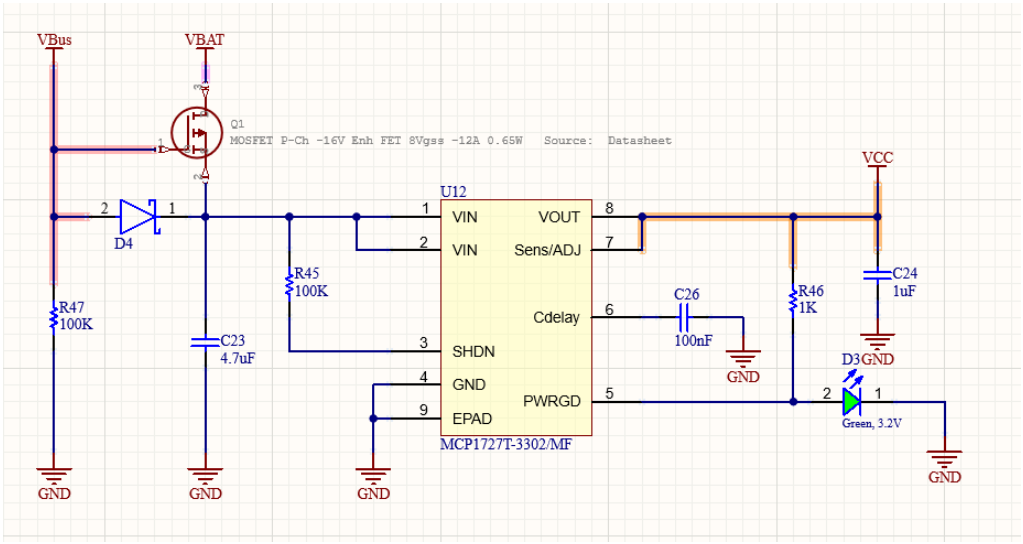

Figure 3.28: MCP1727 Schematic.

Chapter 4

Results and Validation

After all the validation tests and simulations, a prototype board was designed to have every system studied in this dissertation, from the signal acquisition to the BLE communication network. The board was designed to be as compact as possible, although it needed enough space to accomodate the four microphones to acquire all wanted auscultation zones. The final prototype of the PCG and ECG acquisition system is shown in images 4.1 and 4.2.

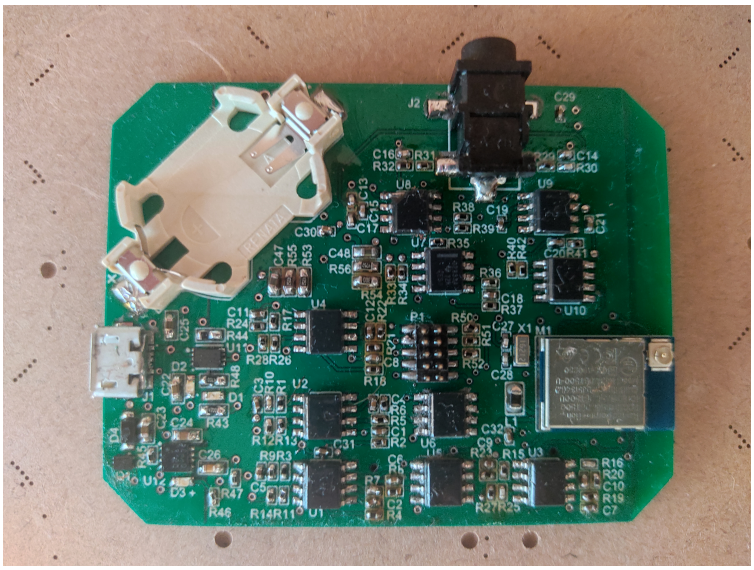

Figure 4.1: PCB Prototype front view.

The board dimensions are 64 mm long and 50 mm wide. Even though it's quite compact, it's still possible to distinguish the division between the power system at the left, the four PCG signal acquisition systems at bottom and the ECG signal circuit up. At the right side is the microprocessor module and the layer design for the antenna.

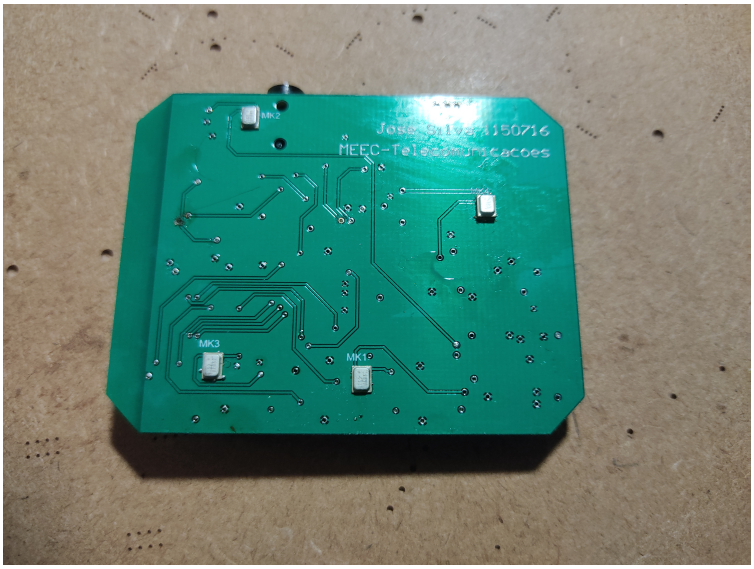

Figure 4.2: PCB Prototype back view.

4.1 Multiple Feedback Low Pass Filter Validation

Numerous tests have been carried out to verify the behaviour of the signal conditioning with several frequencies at the input and output of the conditioning signal circuit. The yellow signal is the multiple feedback filter input, and the cyan signal is the output. For this test the microphone was estimulated with a fixed frequency signal played from a column speaker. The validation was made for 100 Hz, 150 Hz, 200 Hz and 500 Hz.

As seen in figure 4.3, for a 100 Hz signal with 2.86 Vpp, the output has 2.68 Vpp, representing a very small attenuation. It can also be seen that the output signal is phased -135.8 degrees from the input. For the remaining of this sub-chapter consider each horizontal division is 200 ms and each vertical division is 500 mV.

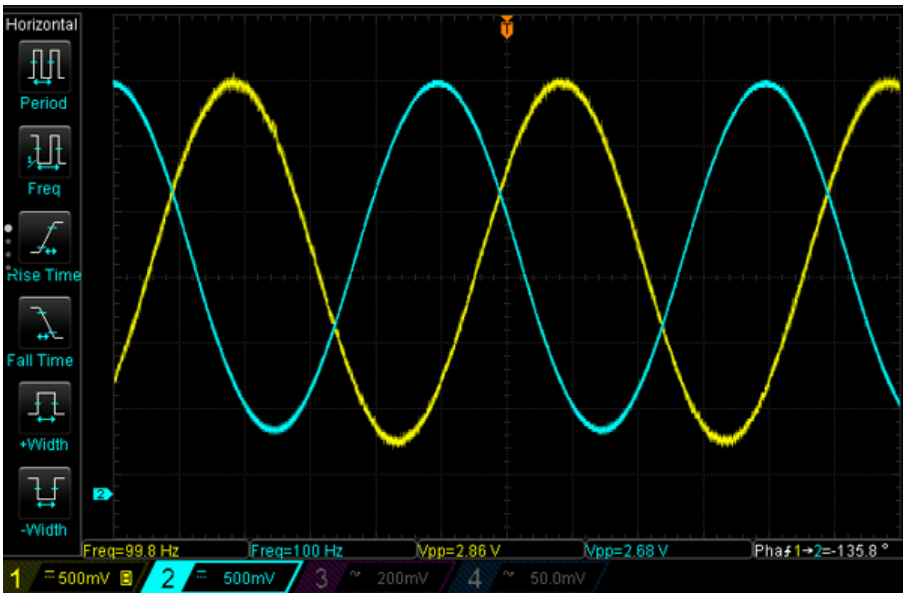

Figure 4.3: Filter input and output signal at 100 Hz.

The same test was made for a frequency of 150 Hz, as seen in figure 4.4. For a 3.04 Vpp input signal, the output signal had now a peak-to-peak voltage of 2.64 V. It's expected for the filter to attenuate the signal as the frequency gets closer to 200 Hz. Also the phase from the input signal to the output signal is now -108.5 degrees.

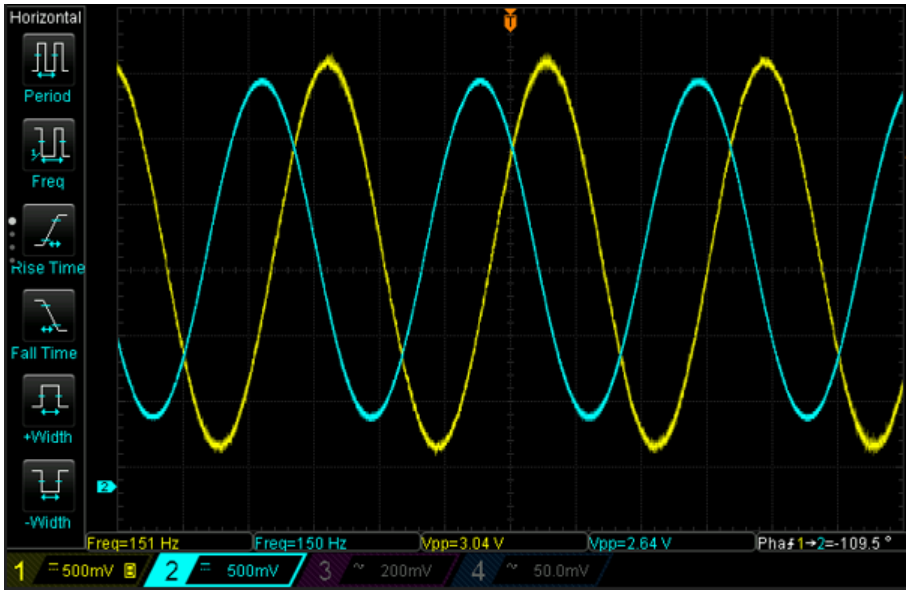

Figure 4.4: Filter input and output signal at 150 Hz.

Now for a frequency of 200 Hz that is the cutoff frequency of this circuit, as seen in figure 4.5, is expected an attenuation of 0.707, equivalent to the inverse of square root of two. For a 3.26 Vpp input signal, the output signal had now a peak-to-peak voltage of 2.26 V, which is almost exactly the expected value in this case. Also the phase from the input signal to the output signal is now -272.6 degrees, which corroborates the expected phase of 90 degrees.

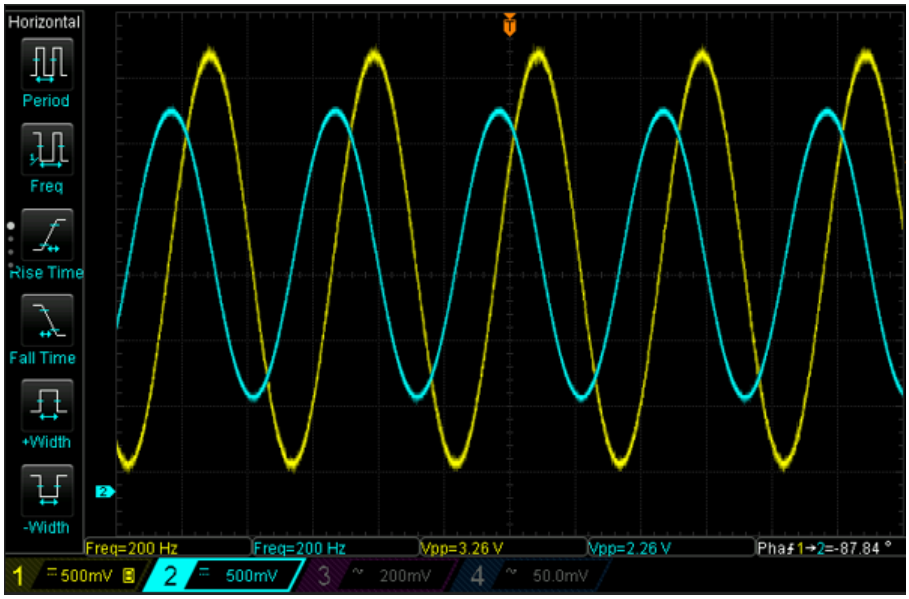

Figure 4.5: Filter input and output signal at 200 Hz.

Finally, a 500 Hz signal was tested in order to show the filter response to an undesired frequency. As shown in figure 4.6, the output signal is drastically attenuated, having 540 mVpp in comparison to the 3.10 Vpp input.

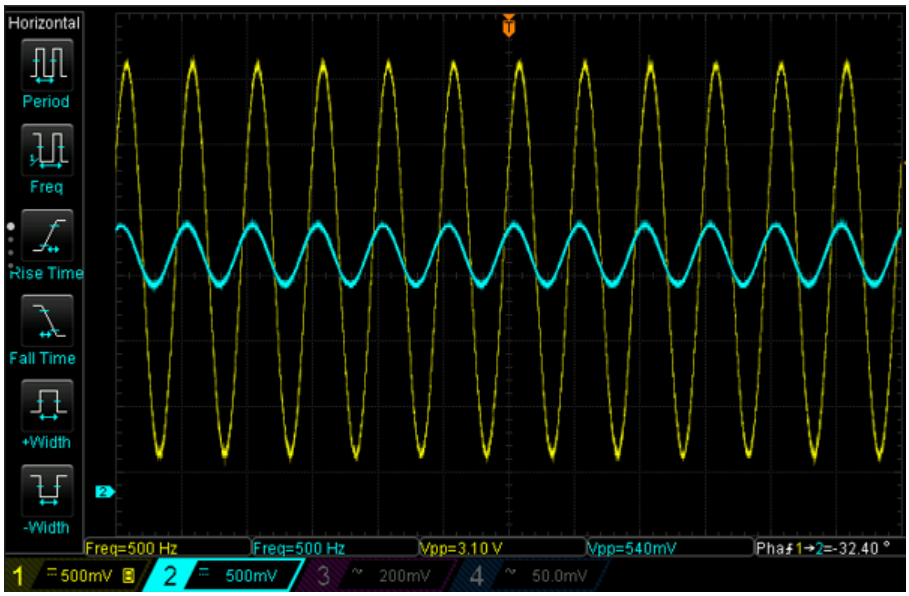

Figure 4.6: Filter input and output signal at 500 Hz.

4.2 Heart Sound Response Test

In this section is presented the signal acquisition and conditioning circuit validation by testing it using two synthetic signals with different diagnostics and a real heart signal acquired by the microphone.

4.2.1 Synthetic Heart Sounds

Two synthetic heart signals were used for this test, a healthy signal and a congestioned heart signal. Both of these samples were provided by the ThinkLabs heart library [43].

For the first test a healthy heart signal was used. As the section above, a sound speaker was used to provide a sound signal to the microphone. In the figure below it's possible to identify both S1 and S2 signals. For figure, each horizontal division represents 50 ms and each vertical division is 200 mV.

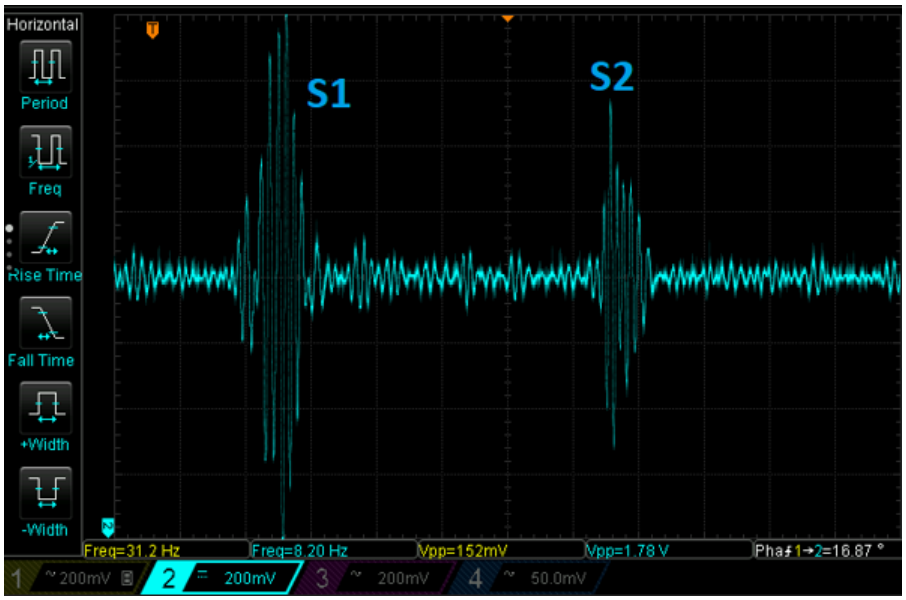

Figure 4.7: Healthy heart sound signal.

Another validation was made for the same signal at lower amplitude. In this figure is possible to verify two heartbeats, which helps to understand not only the S1 ans S2 sounds, but also the heartbeat frequency. From this image is possible to count 5 divisions between both S1 sounds from each heartbeat. Since each division is 200 ms, the signal period is 1 second, which means this signal has a 1 Hz frequency. For that value, the heart beats at exactly 1 beat per second, that amounts for 60 beats per minute. For figure 4.8, each horizontal division represents 200 ms and each vertical division is 200 mV.

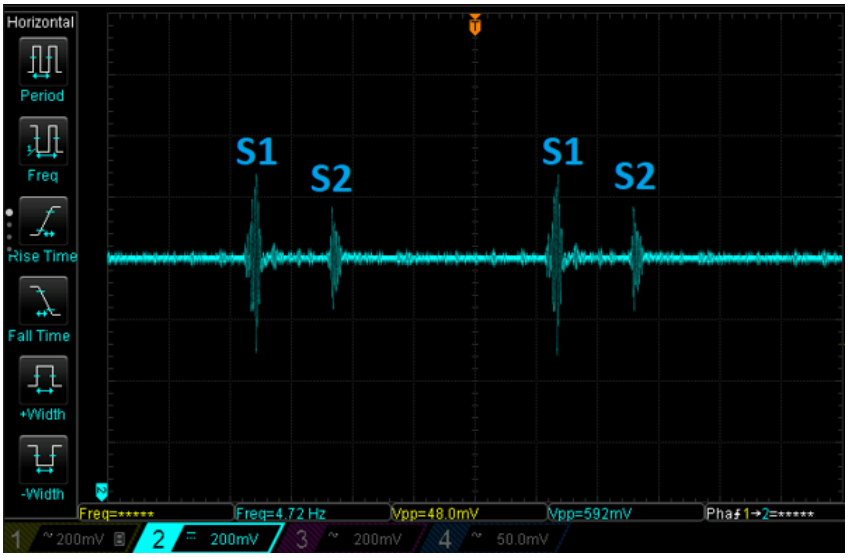

Figure 4.8: Healthy heart signal showing two periods.

In figure 4.9, a congestioned heart was used as the circuit input. Here it's possible to identify the S3 sound as well, and understand that it has a higher amplitude than S2. Consider each horizontal division represents 200 ms and each vertical division is 200 mV.

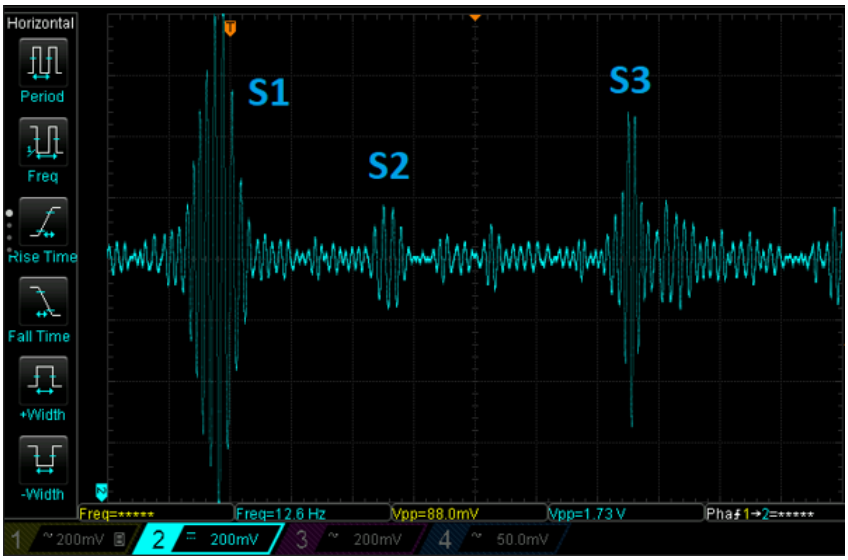

Figure 4.9: Congestioned heart signal.

4.2.2 Real Heart Sounds

Finally, the circuit was tested with a real auscultation. One microphone was placed in the chest, closer to the heart of a patient. The circuit output from the real signal can be seen in figure 4.10. It's possible to distinguish both the S1 sound and the S2 sound. The horizontal division represents 100 ms and each vertical division is 200 mV.

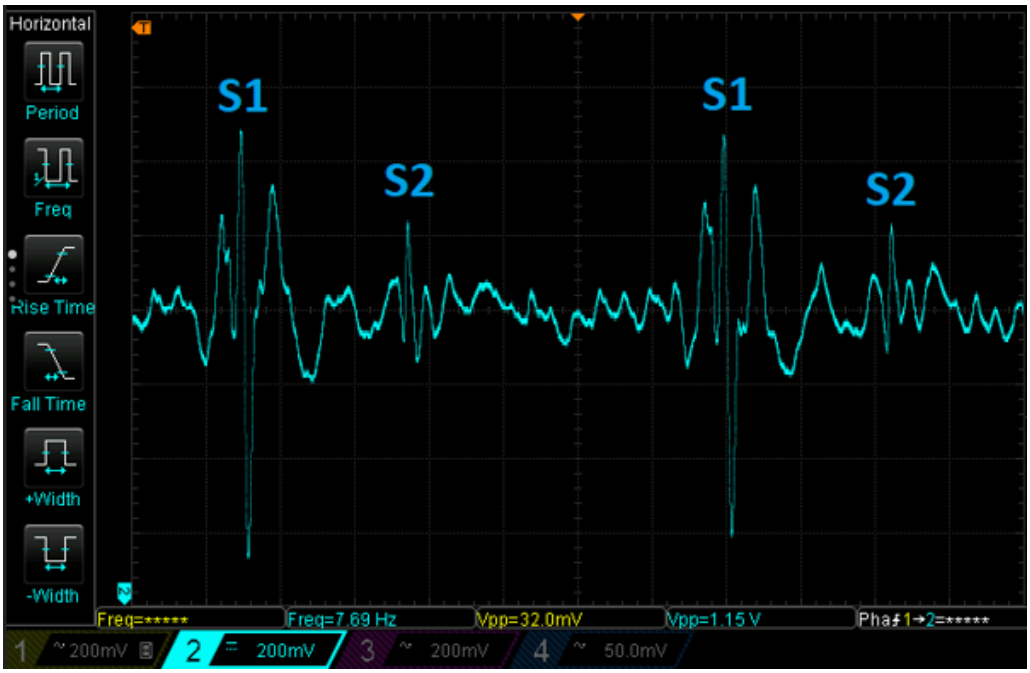

Figure 4.10: Real heart sound acquired directly from a human being.

In figure 4.11 it is easier to notice more periods of this signal, as well as the amplitude difference between S1 and S2. The horizontal division represents 200 ms and each vertical division is 200 mV. This measurement was made with the patience at rest, after he had a period of intense physical exercise. Counting the period between the S1 sounds we have about 640 ms, meaning a frequency of 1.56 Hz, which amounts to a heart beat of 94 beats per minute.

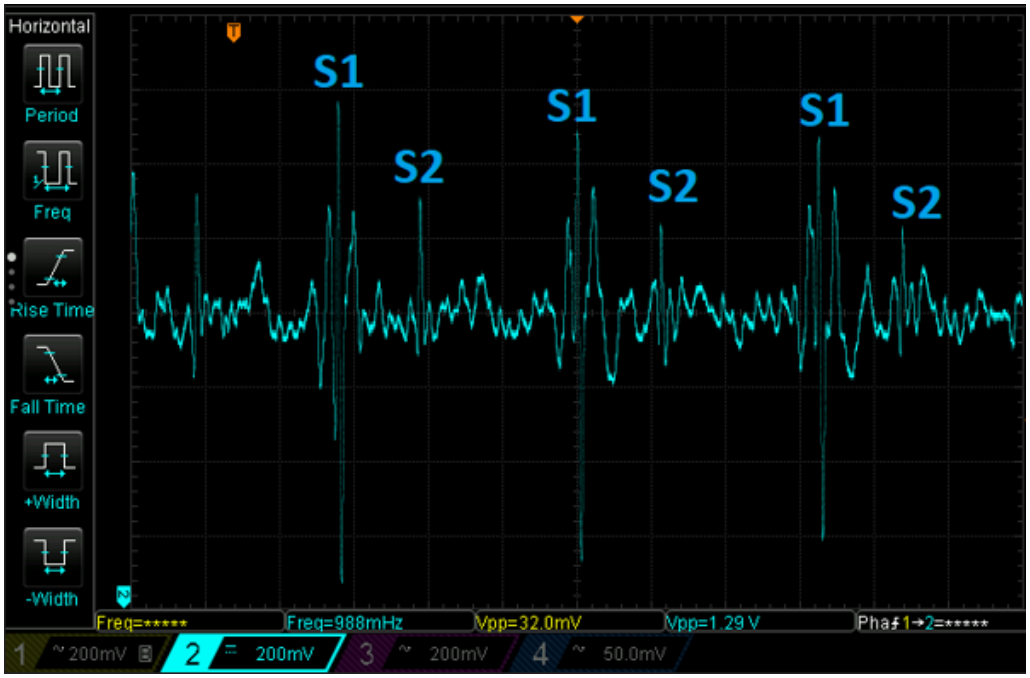

Figure 4.11: Real heart sound acquired directly from a human being (zoomed out).

4.3 Sallen Key Low Pass Filter Validation

Similar to the the multiple feedback filter circuit used for the PCG, more validation tests were made for the Sallen Key filter used in the ECG circuit. The yellow signal is the multiple feedback filter input, and the cyan signal is the output. For this test a synthetic ECG signal programmed in a signal generator was used. The validation was made for 20 Hz, 50 Hz, 80 Hz and 125 Hz.

As seen in figure 4.12, for a 20 Hz signal with 3.26 Vpp, the output has 3.08 Vpp, being a rather small attenuation. It can also be seen that the output signal is phased 10.8 degrees from the input. Each horizontal division in this graphic is 10 ms and each vertical division is 500 mV.

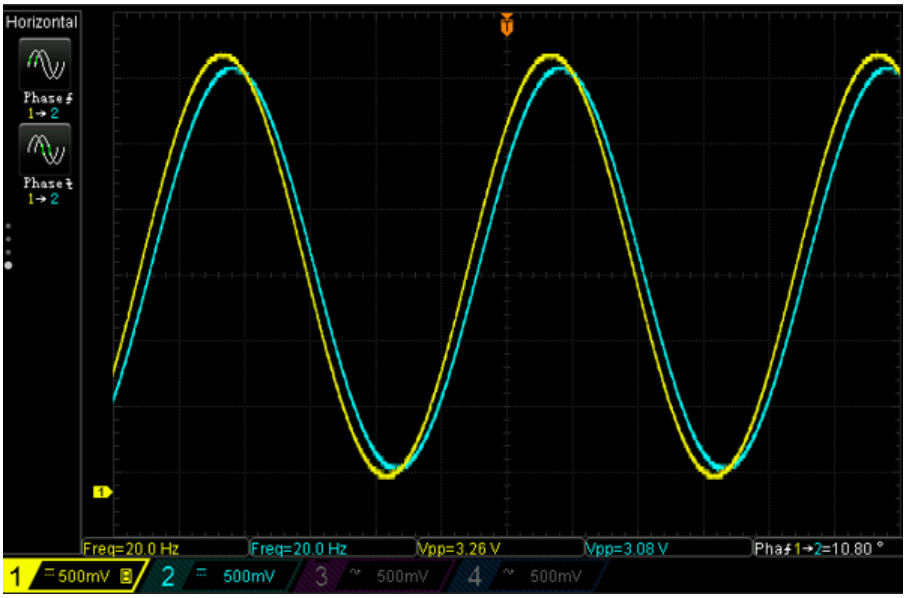

Figure 4.12: Sallen Key filter input and output at 20 Hz.

The same test was made for a frequency of 50 Hz, as seen in figure 4.13. For a 3.24 Vpp input signal, the output signal had now a peak-to-peak voltage of 2.68 V. It's expected for the filter to attenuate the signal as the frequency gets closer to 125 Hz. Also the phase from the input signal to the output signal is now 22.5 degrees. For this graphic and the remaining tests of this subsection consider each horizontal division to be 5 ms and each vertical division to be 500 mV.

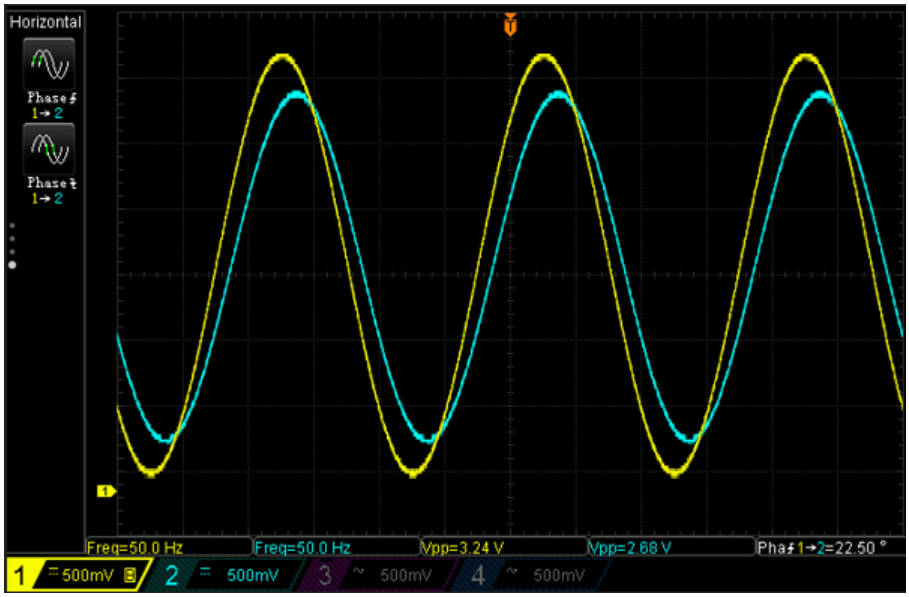

Figure 4.13: Sallen Key filter input and output at 50 Hz.

In the next test was used a frequency of 125 Hz that is the cutoff frequency of this circuit, as seen in figure 4.14. It is expected an attenuation of 0.707, equivalent to the square root of two. For a 3.22 Vpp input signal, the output signal has now a peak-to-peak voltage of 2.16 V, which is in the range of the expected value in this case. Also the phase from the input signal to the output signal is now 33.75 degrees. The phase in every test is less than theoretically expected, but it was practically expected since other values had to be used for the resistors, as 8.66k resistors were out of access, and not being the most critical aspect of this test, the values were tuned primarily for the cut-off frequency.

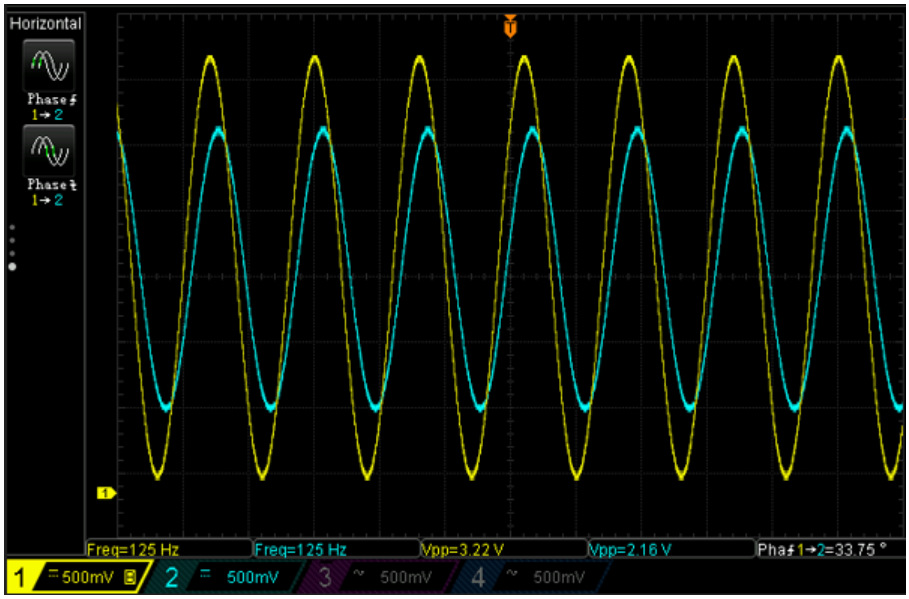

Figure 4.14: Sallen Key filter input and output at 125 Hz.

For the last test, a 350 Hz signal was used in order to show the filter response to an undesired frequency. As shown in figure 4.15, the output signal is already attenuated past the -3dB point, having 1.54 Vpp in comparison to the 3.22 Vpp input.

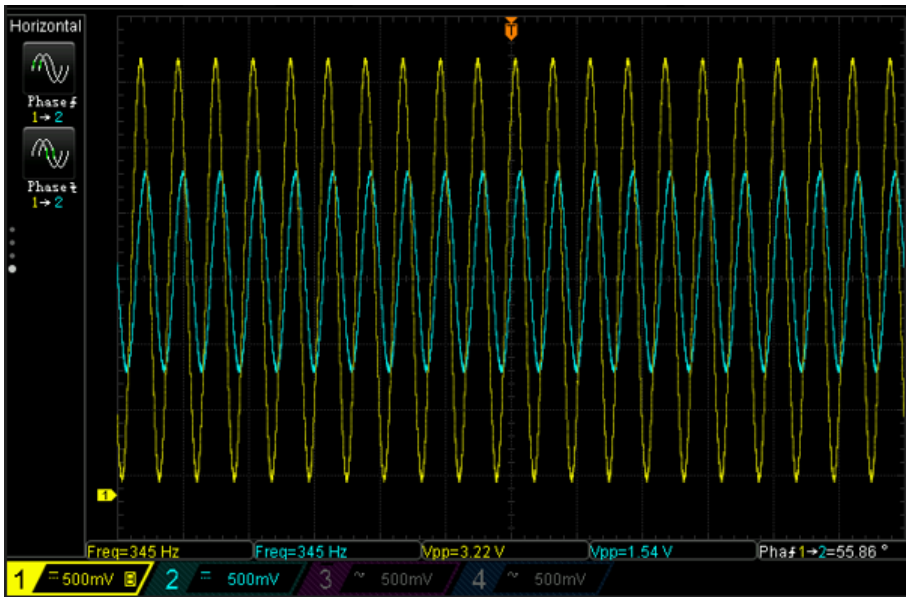

Figure 4.15: Sallen Key filter input and output at 350 Hz.

4.4 ADC Validation

Having the validation done for both the PCG and ECG signals, the next step was to validate the ADC component of the system. The full microprocessor development was made using the nRF52840 development kit, and the code was written and debugged with the nRF Connect toolchain that provides a pre-installation of the Segger Embedded Studio. The implemented firmware was based on Nordic's Software Development Kit (SDK), using a multi-channel SAADC based example which was then modified to be used with a BLE softdevice.

While the final prototype was designed for BLE data transmission, the development and validation of the ADC was firstly made using the UART. With this method it was possible to visualize and validate the data processed by the ADC before sending it via BLE.

Since the development kit was plugged to the PC and powered via Universal Serial Bus (USB), it was possible to communicate via UART right from the start. The application used to translate the data into visual signals was the SerialPlot app made by Hasan Yavuz Özderya et al. It is a Qt based software for plotting data from serial port in real time that allows for data separation in order to visualize various signals simultaneously. The UART communication was made at a baud rate of 250000, with 8 data bits, 1 stop bit no parity and no hardware flow control.

To test the ADC at this stage a sound speaker playing a synthetic heart was used for the four PCG circuit inputs and for the ECG signal two synthetic signals were driven through its respective circuit. It's possible to observe the results in figure 4.16.

Figure 4.16: Example of the 4 PCG signals plus the ECG acquired by UART.

4.5 BLE Validation

The next test to be made was to validate the BLE connection. Nordic supplies different applications for testing and debugging nRF modules. The ones used in this project were the nRF Connect to test the BLE connection and implementation, and nRF Logger to obtain log files from the transmitted data.

With the nRF Connect app, it was possible to understand if a connection was made and how it works. If the device is advertising, more specifically in the peripheral role, the device may be discovered by other devices. In figure 4.17 several parameters can be seen. At first it's possible to see the name of the device, being "PCG ECG Acquisition System" and below the nRF52840 MAC address. The other parameters like the flags mean the device can only be the discoverable in a limited period of time and that Bluetooth Classic mode is not supported.

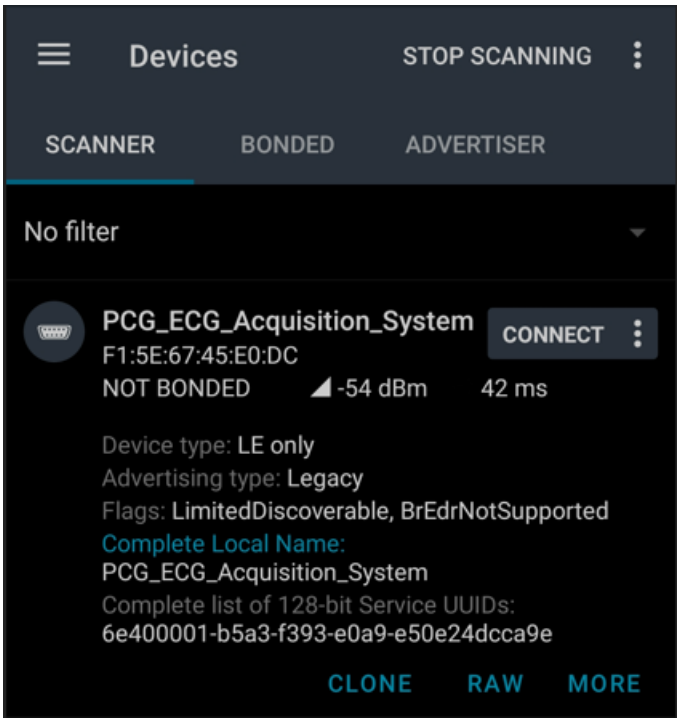

Figure 4.17: Device Advertising information.

By connecting the device we can see more information regarding the central-peripheral connection. In the Peripheral Preferred Connection Parameters, we can perceive three different values, being connection interval, slave latency and supervision timeout multiplier. The connection interval used for the test and the application was 7.5 ms as minimum and 25 ms as maximum. The slave latency parameter signifies the number of connection events the peripheral is allowed to skip, and while it was changed in the final application, for testing purposes it was set to zero. This allowed for testing the transmission and understanding the communication speed limits without any packet loss. Finally the supervision timeout multiplier meant the time allowed to be spent between two packet transmissions until the connection closed. A number of 400 ms was chosen for this parameter.

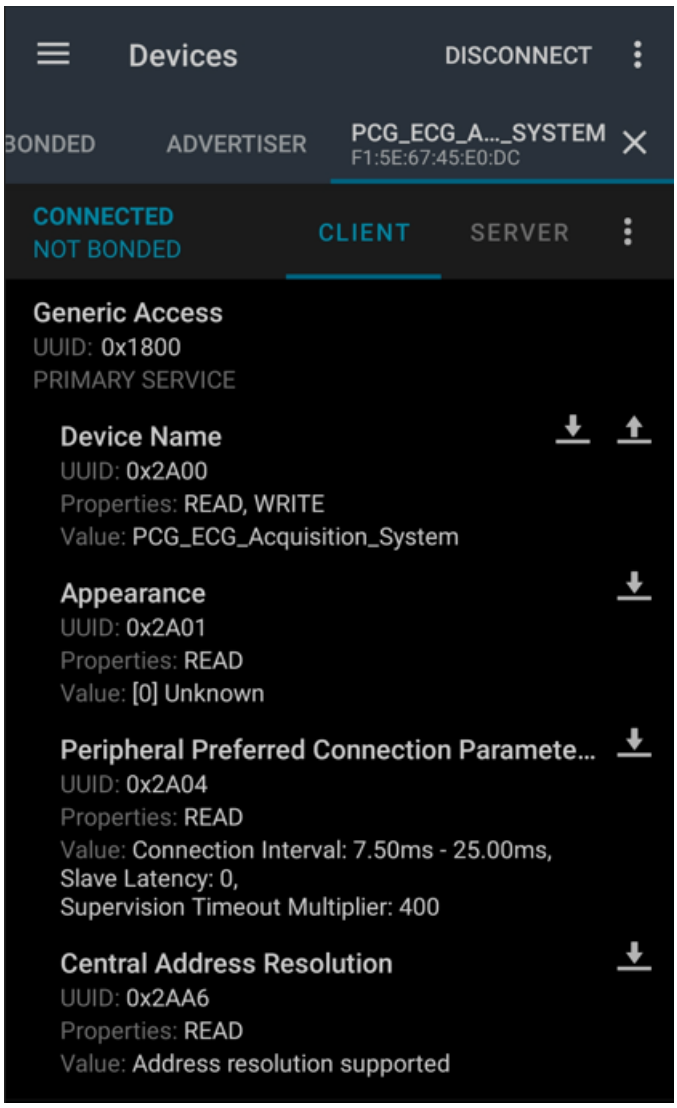

Figure 4.18: Connection Parameters.

Further it can be seen the communication service parameters, the RX characteristic allows for the application to write to the nRF if necessary. In the TX characteristic it's possible to see a notification and its content, and thus validating at least that a notification was sent. Since the used service is based on a UART service, the nRF Connect expects ASCII characters or a string to be sent, and automatically attempts to translate the received information. To properly visualize the content of a notification, the nRF Logger app can be used.

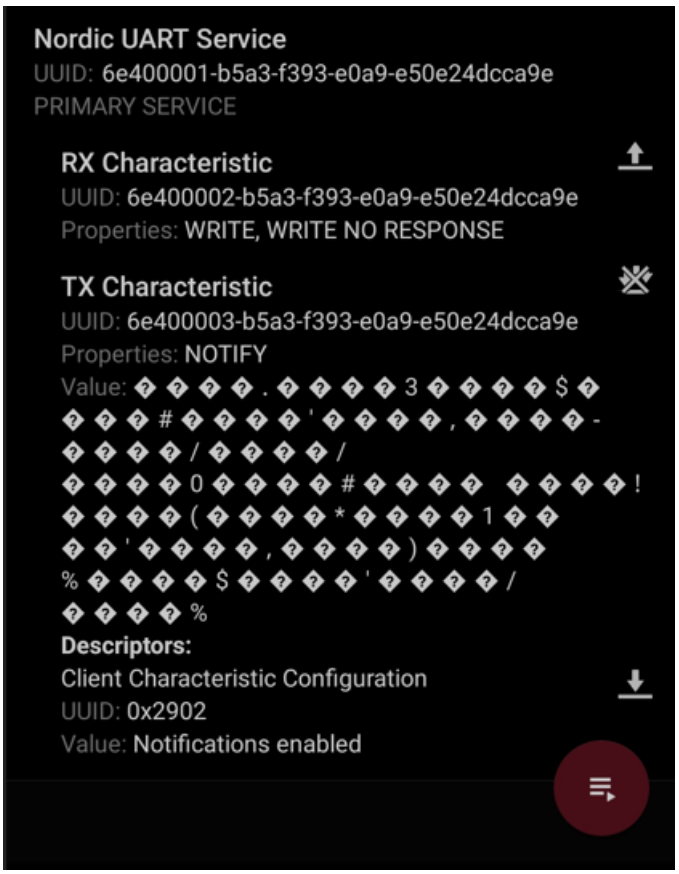

Figure 4.19: RX and TX characteristic.

Watching the log file can give a better perception of the communication made between the devices. We can see the connection being established, as the device name, appearance setting, connection interval, slave latency and supervision timeout are all sent and received. Two other notifications are sent before the first packet, the first validates the nRF MAC address for communication and the second one enables notifications so packets can be transmitted and received. Finally, it's possible to see the content of a 240 byte packet. The information is shown in hexadecimal format, and doing a quick analysis it's possible to see that all values can be read in the 0 to 4095 interval, which are the expected values for a 12-bit ADC. From this study, it was possible to conclude that the BLE worked properly, but this was still not enough to validate the full functioning of the system, as only by visualizing the five signals an accurate evaluation could take place.

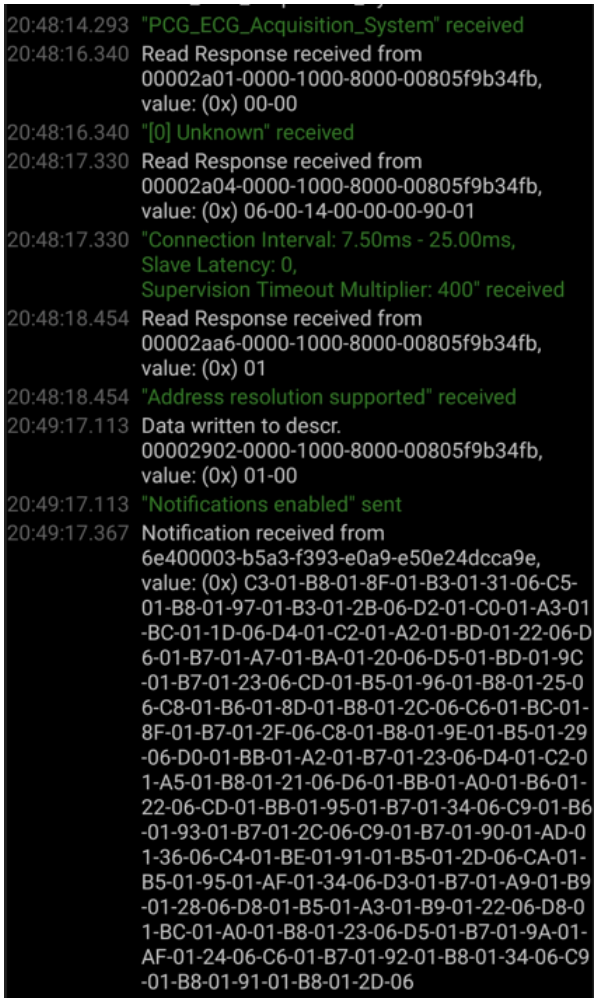

Figure 4.20: Notification logs.

4.6 Signal Validation

The last component of this project to be tested and validated was to acquire and visualize the data transmitted from the module in a mobile device or PC. A Python script was developed in order to process and separate the transmitted data into the 5 different signals, creating a text file that could then be used as an input to a MATLAB file to draw the signals. In figure 4.21 it's possible to see a full acquisition of all four PCG signals as well as the ECG signal. All PCG signals present a peak-to-peak voltage of about 700 mV. This value is well within the expected range, since the circuit is designed to not saturate at the microphone maximum AC input voltage, and it's not expected for the microphone to acquire the heart sounds with perfect gain response. As for the signals themselves, it's possible to identify both S1 and S2 components of the heart sounds, and perceive the events between the ECG and PCG signals with clarity.

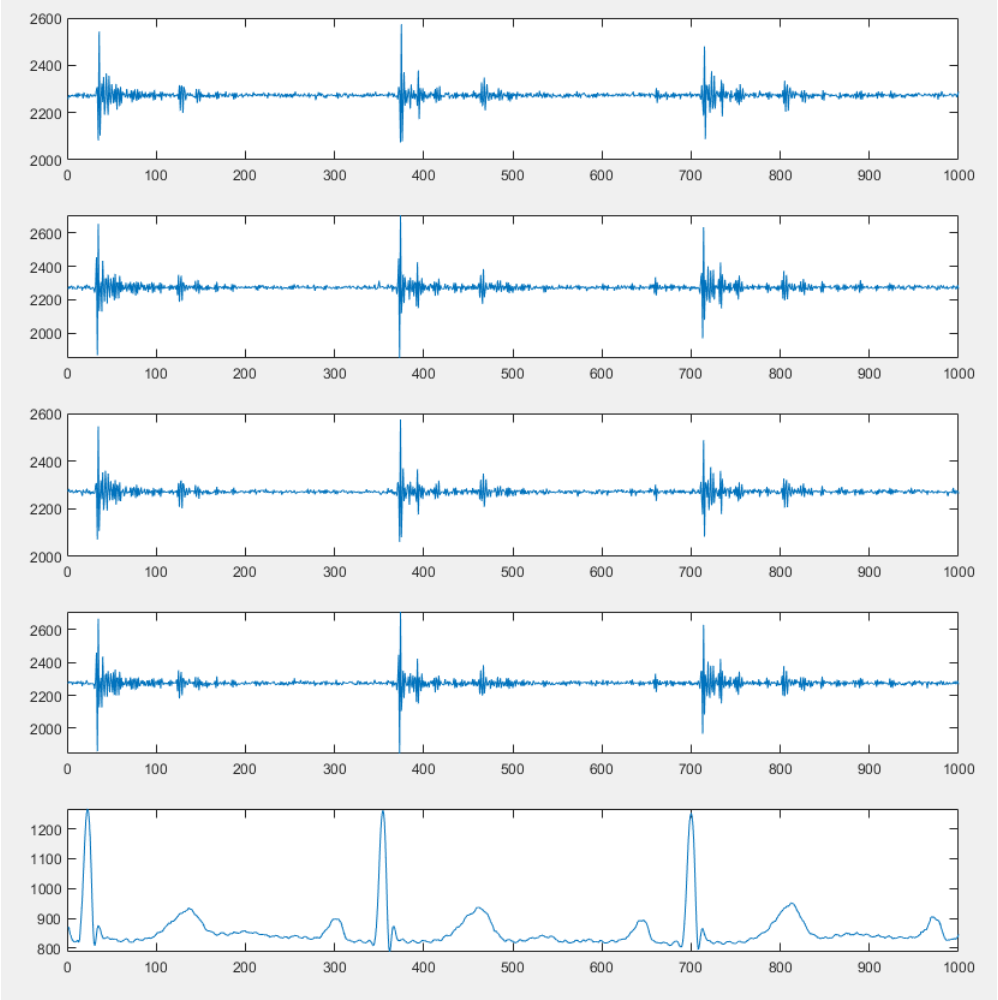

Figure 4.21: Full Circuit validation.

Comparing two different PCG signals, it's possible to perceive a lot of similarities, which is definitely expected. Still, in both S1 sounds and even to an extent the S2 sounds some differences can be noted from one signal to the other in the same heartbeat.

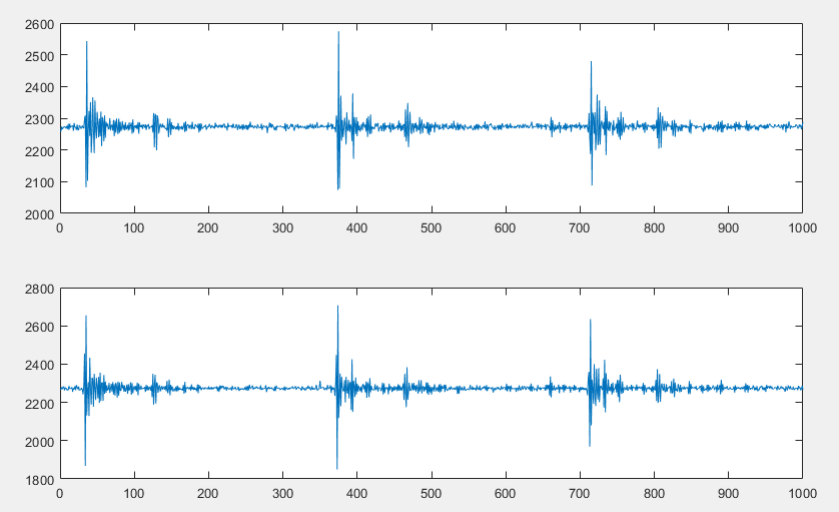

Figure 4.22: Comparison between two PCG signals.

Comparing a PCG signal to the acquired ECG it's possible to analyze the relationship between the QRS wave and the S1 signal, as well as it's possible to perceive the elevation in the T wave happening around the S2 sound. Overall, both signals presented perceivable results.

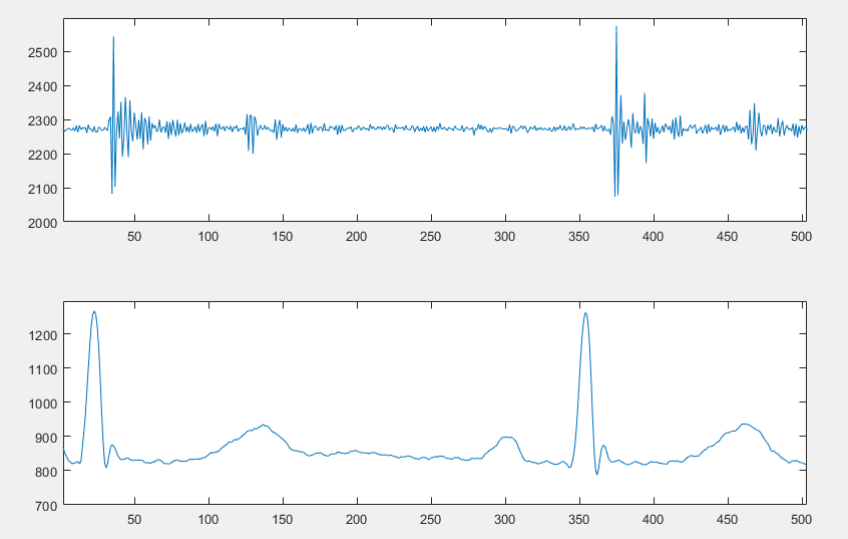

Figure 4.23: Comparison between a PCG and an ECG signal.

Chapter 5

Conclusions

During this thesis, a study of the heart and the identification of related diseases was conducted in order to develop a system capable of acquiring . It was possible to understand that the evolution of technology in the branch of cardiology is a constant key factor in saving human lives. As more and better data can be acquired and analyzed, hopefully a visible improvement will be seen in the overall population health.

Due to the academic nature of the project, functionality was always the priority. The main goal was the acquisition of more than one PCG signal, which can be considered a success as not only two but four PCG signals in different auscultation zones can be acquired. The ECG circuit was added as an extra functionality and while its implementation was always deemed as a possibility, it was only designed after the PCG and as a rule couldn't add any extra constraint to the functionality of the heart sound acquisition. It was still successfully implemented but it's worth noting that an eventual revision of this module would probably present some tweaks in the ECG design to improve CMRR and frequency response.

The MEMS microphones utilized had very satisfactory results. A worse response for frequencies under 100 Hz was always a constraint that had to happen, since the technology for a flat response in the 50 to 100 Hz range is not a reality for today's microphones, at least in a sensible price range. Nonetheless, it was possible to notice every expected pattern in the heart sounds with pleasant accuracy.

Another important aspect of the system was the wireless communication and to an extent the power consumption. Nordic's nRF52840 could almost be said to

be an ideal solution to accomplish these requirements. Both signal processing and data transmission duties were easily implemented with this integrated circuit, and the final signal validations proved the data transmission to very reliable. Doing an overall analysis, the developed system could be considered as an early prototype or proof of concept for a future market solution.

5.1 Future Developments

Mentioning future work, a direct revision of this module could see the optimization of BLE transmission speeds to allow for better signal sampling. Also the addition of a Secure Disk (SD) memory card could be a good solution for offline signal recording, allowing for power saving when real time monitoring is not needed. In a longer term perspective, it's possible to envision the development of a online application to provide a better interface for signal visualization, and even implementing machine learning algorithms for pathology identification.

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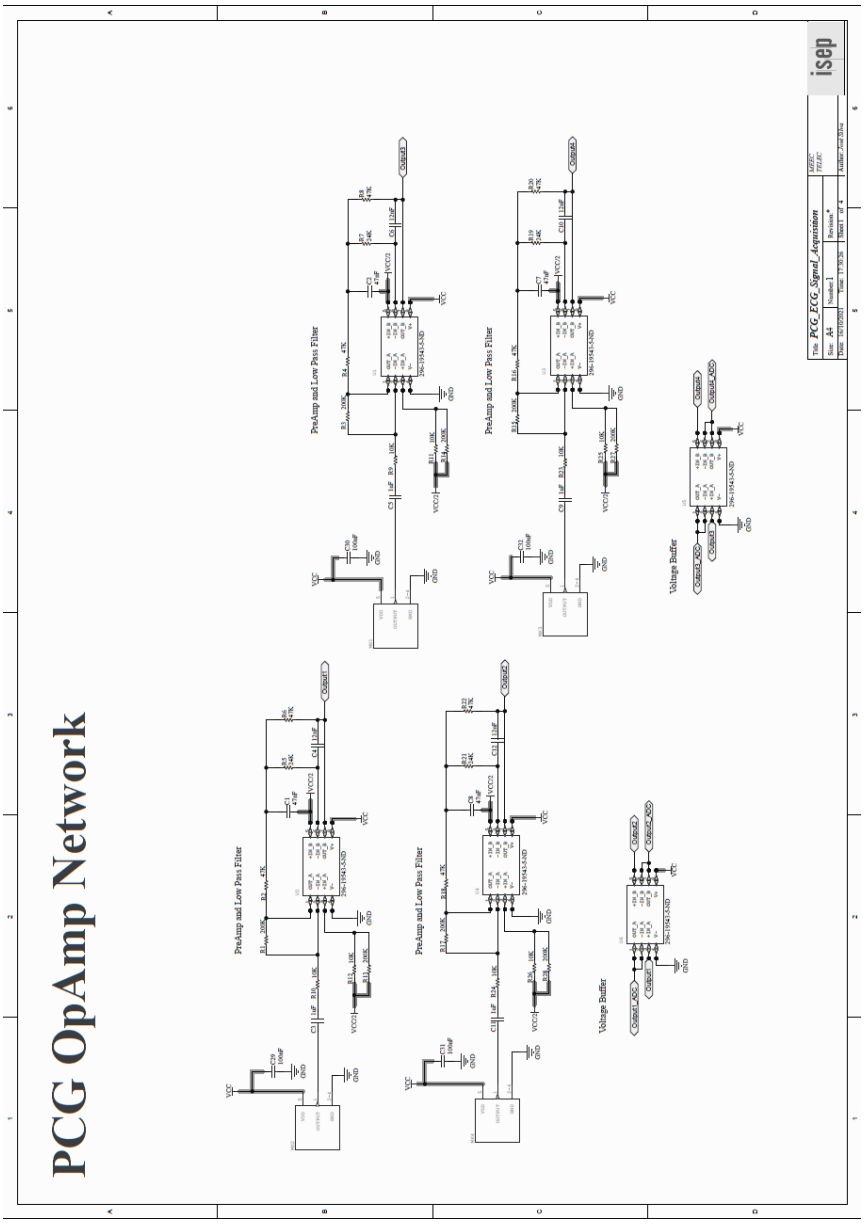
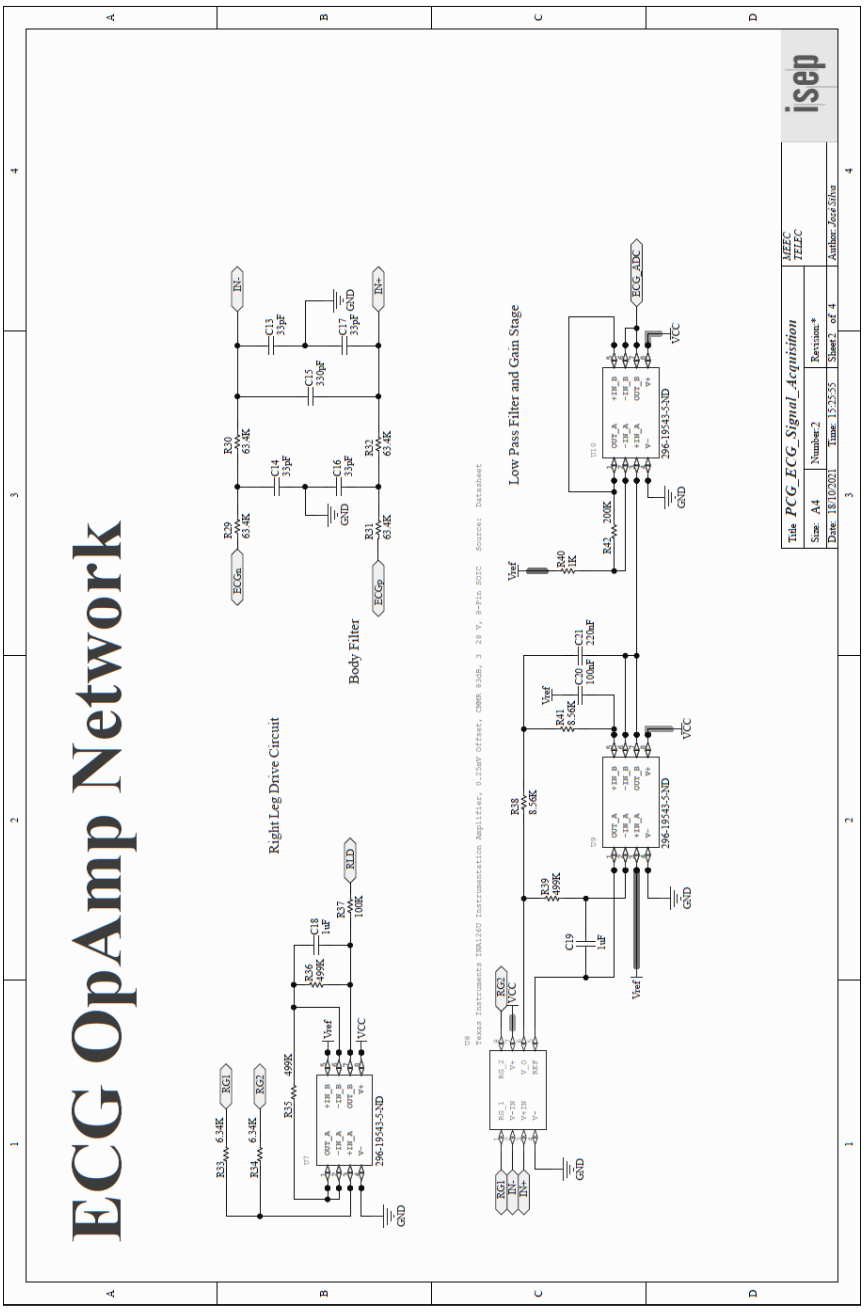
Appendix A

Appendix

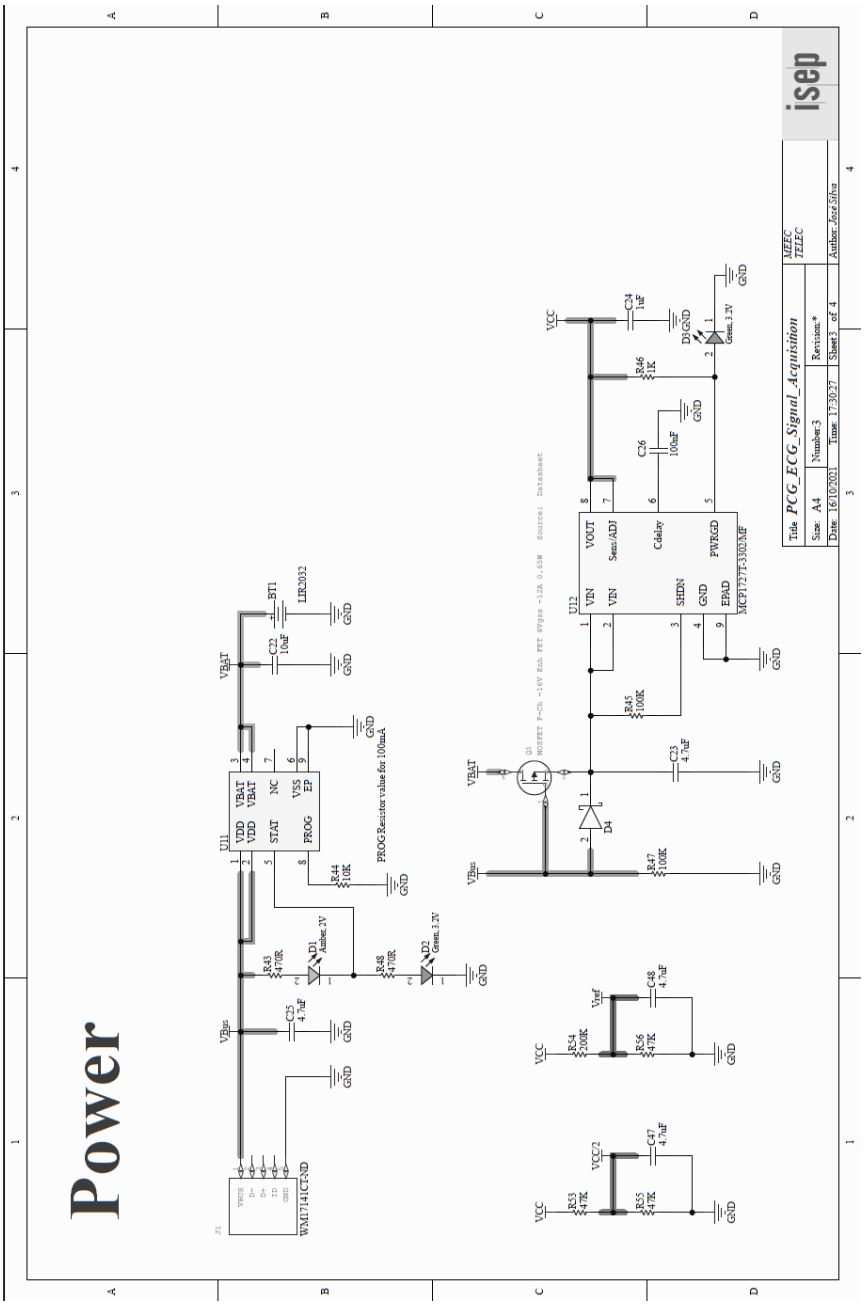
A.1 Final Prototype PCG Schematic



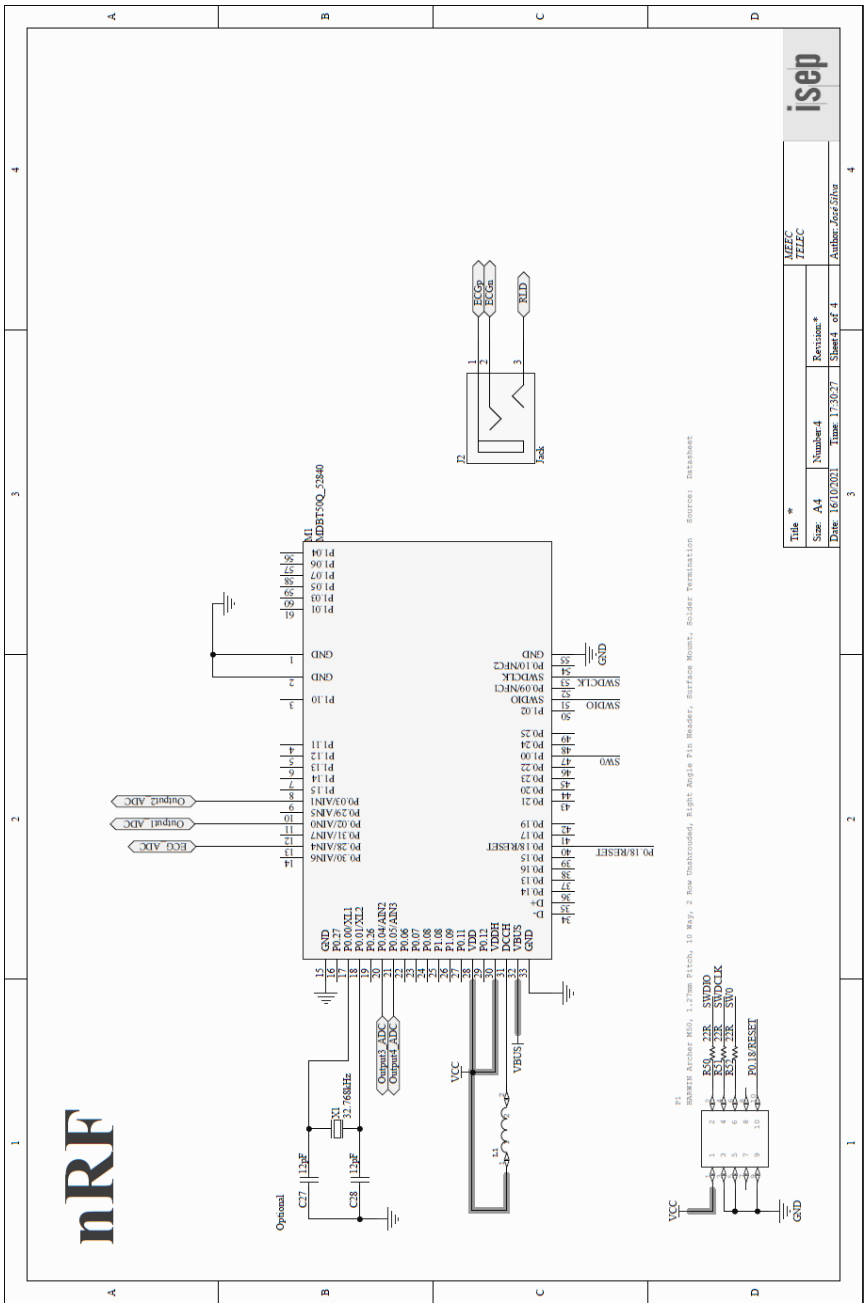
A.2 Final Prototype ECG Schematic



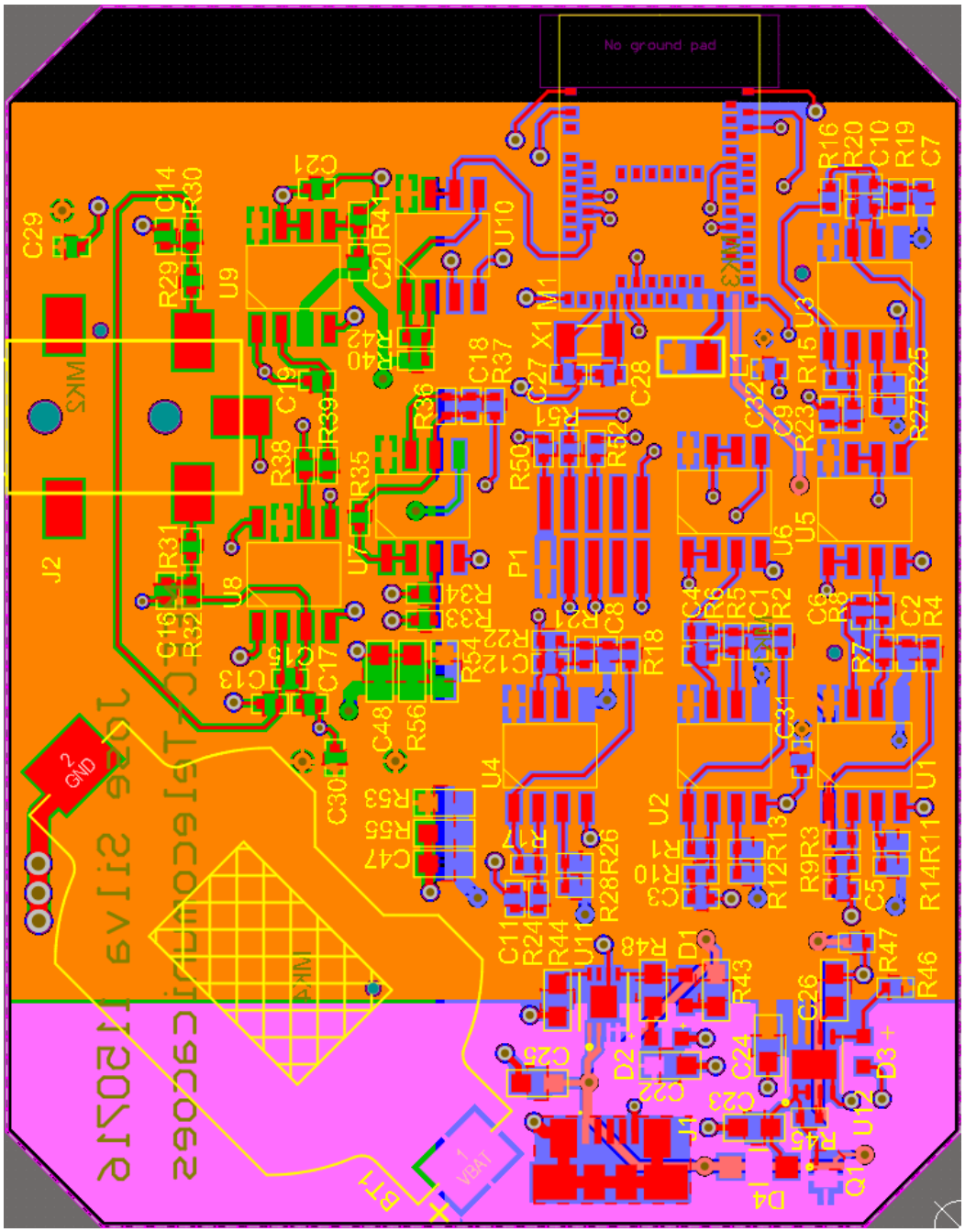
A.3 Final Prototype Power Schematic



A.4 Final Prototype nRF52840 Schematic

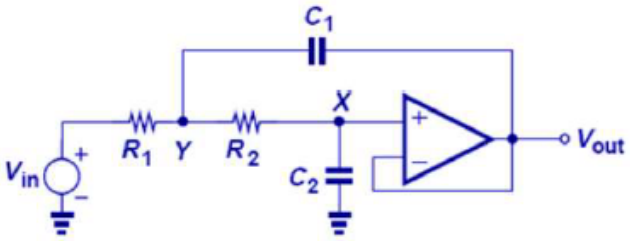


A.5 Final Prototype PCB



A.6 Sallen Key Filter Resolution

Sallen Key Filter Design



A second order active filter can be given as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$$

As for the Sallen-Key lowpass filter with unity gain the ideal transfer equation can be written as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{R_1R_2C_1C_2s^2 + (R_1 + R_2)C_2s + 1}$$

And then rearranged to:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\left(\frac{1}{\sqrt{R_1R_2C_1C_2}}\right)^2}{s^2 + \frac{1}{\sqrt{R_1R_2C_1C_2}}\frac{\sqrt{R_1R_2C_1C_2}}{(R_1 + R_2)C_2} + \left(\frac{1}{\sqrt{R_1R_2C_1C_2}}\right)^2}$$

w0

Q

Now, we can associate the Q factor and central frequencies with the component values chosen:

$$\omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \qquad Q = \frac{\sqrt{R_1 R_2 \frac{C_1}{C_2}}}{(R_1 + R_2)}$$

The values for the circuit were chosen with the capacitors in mind. If we dimension both resistors to have the same value, we can pick an optimal ratio between the two capacitors for a Butterworth response, and then adjust the resistor value accordingly.

$$C_1 = \frac{2Q}{R\omega_0} \qquad C_2 = \frac{1}{2R\omega_0 Q}$$

For Q = 0.707, we can infer that C1 = 2xC2. With that in mind, the chosen values for the capacitors were 100 nF for C2, and 200 nF for C1, which was then adjusted for the market value of 220 nF.

For these capacitor values we can calculate the value for the resistor through our desired cut-frequency. For a frequency of 125 Hz, C1 = 220 nF and C2 = 100 nF the best value for the resistors is 8.56k ohms. As no stock was available for this value, 8.66 kohms was chosen. Final values consist of:

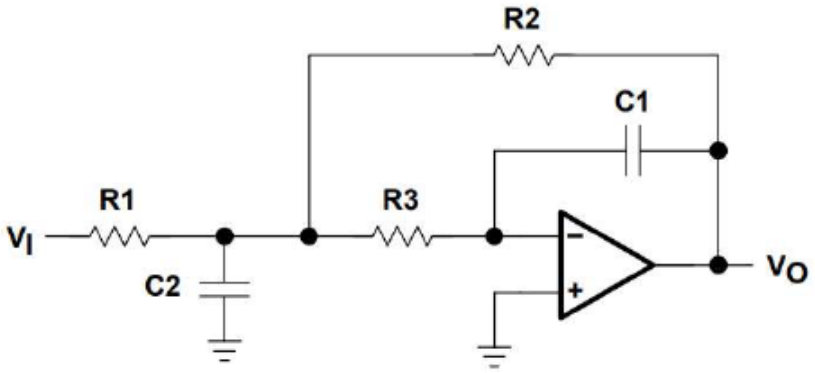
R1 = R2 = 8.66 kOhms

C1 = 220 nF

C2 = 100 nF.

A.7 Multiple Feedback Filter Resolution

Multiple Feedback Filter Design



A second order active filter can be given as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$$

As for the MFB lowpass filter the ideal transfer equation can be written as:

$$H(f) = \frac{\frac{-R2}{R1}}{(j2\pi f)^2(R2R3C1C2) + j2\pi f\left(R3C1 + R2C1 + \left(\frac{R2R3C1}{R1}\right)\right) + 1}$$

From the equation above it's possible to conclude the gain, central frequency and quality factor values:

$$K = \frac{-R2}{R1} \qquad fc = \frac{1}{2\pi\sqrt{R2R3C1C2}} \qquad Q = \frac{\sqrt{R2R3C1C2}}{R3C1 + R2C1 + R3C1(-K)}$$

Considering a unity gain circuit, where K = -1, we can write Q as:

$$Q = \frac{\sqrt{R3\,R2\,C1\,C2}}{R3\,C1 + R2\,C1 + R3\,C1}$$

In order to design the circuit, considering the gain to be -1 it's possible to choose the values by working with the ratios between the capacitors and the resistors for the desired Q and central frequency. By letting R2=R, R3=mR, C1=C, C2= nC we can follow the next equations:

$$fc = \frac{1}{2\pi RC\sqrt{mn}} \qquad Q = \frac{\sqrt{mn}}{1 + 2m}$$

Considering Q = 0.707 and fc = 200 Hz, and letting m be 0.5, it's possible to calculate n to be exactly 4. Following those values, we can pick C2 to be 47 nF and C1 to be 11.75 nF, adjusting its value to 12 nF. Having both C and n defined we can calculate R using the central frequency equation as:

$$R = \frac{1}{2\pi \times 200 \times 1.2 \times 10^{-8}\sqrt{2}} = 47\,k$$

Having now calculated all values, we have the adjusted component values as:

R2 = 47k,

R1 = 24k,

C1 = 12nF,

C2 = 47 nF.