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Temperature and electric field dependence of the carrier emission processes in a quantum dot-based memory structure

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Hole emission processes from self-organized $GaAs_{0.4}Sb_{0.6}/GaAs$ quantum dots embedded in a *p-n* diode are studied by capacitance-voltage spectroscopy. The method introduced allows the investigation of the temperature and electric field dependence of carrier emission with time constants from below nanoseconds up to thousands of seconds. Different emission processes are clearly distinguished, such as tunneling, phonon-assisted tunneling, and thermal activation, each important for quantum-dot-based memory structures. The erase time was determined to 1.5 ms for an electric field of about 200 kV/cm. At 500 kV/cm, 10 ns are predicted sufficient for fast erasing.
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Self-organized quantum dots (QDs) (Ref. 1) are ideally suited for studying fundamental physical properties in low-dimensional systems such as size and shape dependent exchange interaction, which is of immediate importance for optical devices such as single photon emitters for quantum cryptography.[2–4] The potential of QDs for revolutionary electronic devices such as QD-based memory devices[5,6] has been hardly explored. Recently, we proposed a memory concept[7,8] (QD-Flash) providing an all-electrical data access and, as an important advantage of QDs for a memory, ultrafast write speed irrespective of the storage time. The write time is only limited by the charge carrier relaxation time from the band edge into QD states. We reported a write time of 6 ns for InAs/GaAs QDs, already in the order of the access time of a dynamic random access memory (DRAM) cell.[8] In the QD-Flash, charge carrier emission from discrete QD states affects the storage time as well as the erase speed. Using type-II GaSb-based QDs, storage times at room temperature of much more than 10 years are expected,[9] a fundamental prerequisite for a nonvolatile memory. However, the prediction is only valid if the underlying charge carrier escape process is pure thermal activation. Erasing in the QD-Flash concept is realized by charge carrier emission in a large electric field. Thus, detailed understanding of charge carrier emission processes in QDs, in particular in the presence of an electric field, is essential.

In this letter, we present a method to study the carrier emission from QDs over an enlarged span of time constants, starting from below nanoseconds (only limited by the pulse generator used) up to thousands of seconds. Our approach enables us to clearly identify the carrier emission processes for different temperature and electric field situations in a QD-based memory structure. Additionally, the erase time is determined as a function of the electric field. Realization of short erase times in the order of nanoseconds is predicted.

Charge carrier emission from QDs embedded in a semiconductor matrix can be quite complex as several emission paths act in parallel.[10,11] In the presence of an electric field, the fundamental emission process is phonon-assisted tunneling,[12–16] e.g., thermal activation from a QD state into an intermediate state and subsequent tunneling through the remaining triangular barrier. In a simple approach, Vincent *et al.*[12] described phonon-assisted tunneling as thermal emission from a deep state into the tunneling density of states given by the conduction/valence band density of states multiplied by the transparency factor of the triangular barrier. The total emission rate is given by an integral over all indirect processes involving virtual states,

$$e(F) = e(0) + e(0)\int_0^{E/kT} \exp\left[z - z^{3/2}\frac{4(2m^*)^{1/2}(kT)^{3/2}}{3q\hbar F}\right]dz, \tag{1}$$

where E is the localization energy of the deep state, F is the electric field, and $e(0)$ is the emission rate for zero electric field, i.e., for pure thermal emission: $e(0) = \gamma T^2\sigma_\infty \exp(-E/kT)$, where σ_∞ is the capture cross section for $T=\infty$ and γ a temperature-independent constant. Vincent *et al.*[12] also gave analytical expressions of the total emission rate for the three important cases that are as follows: pure thermal emission for low electric field, pure tunneling emission for high electric field, and phonon-assisted tunneling in between.

We have studied samples with $GaAs_{0.4}Sb_{0.6}/GaAs$ QDs embedded into a n^+p-diode. The QDs can thus be charged or discharged by holes in a controlled way by an applied external bias.[8] The charge occupation of the QDs can be determined by measuring the depletion capacitance. The sample structure is described in detail in Ref. 17. There we determined a maximum hole localization energy in $GaAs_{0.4}Sb_{0.6}/GaAs$ QDs of 450 meV using deep level transient spectroscopy (DLTS). A charge of about 15 holes per QD for completely filled QDs was derived.

In Fig. 1(a), the capacitance-voltage curve of the sample at 100 K is shown. The voltage was swept in both directions and a clear hysteresis due to the memory effect of the QDs is observed. The maximum hysteresis opening C_{max} appears at a bias voltage of −7.2 V, defining the storage position (step 2 in Fig. 1). As known from DLTS measurements (see Ref. 17), in thermal equilibrium, the QDs are fully discharged at a

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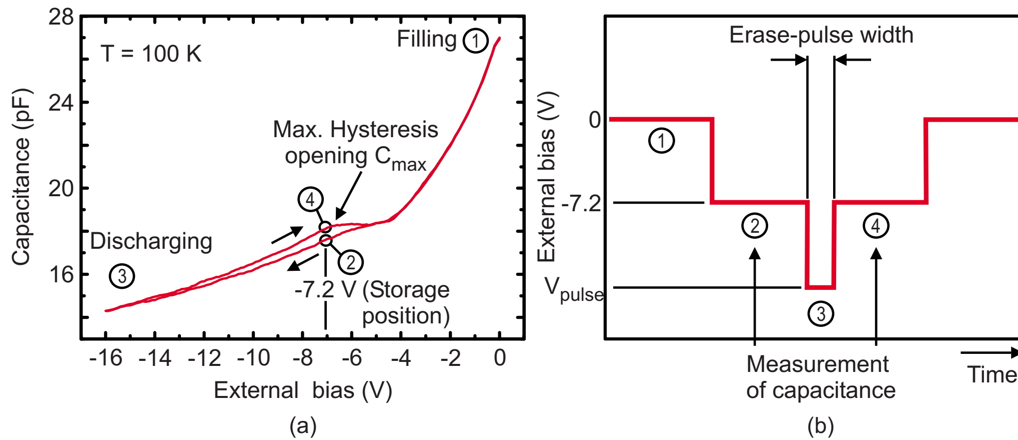

FIG. 1. (Color online) (a) Capacitance hysteresis curve. (b) Method to pointwise measure the emission transients. Step 1: filling the QDs, step 2: first capacitance measurement at maximum hysteresis opening, step 3: discharging the QDs with high reverse bias applied (erasing), step 4: second capacitance measurement.

bias voltage V_r below -10 V and completely filled above V_r=−4.5 V. If the bias voltage is switched from V_r> −4.5 V (QDs are fully occupied) to values below -10 V, the QDs are well inside the depletion region in a strong electric field, and they will be completely discharged by tunneling emission.

In conventional DLTS measurements, emission rates are determined by evaluating the capacitance transients, which are obtained by time-resolved measurements of the depletion capacitance.[18] Due to the limited time resolution of capacitance measurements, recording capacitance transients with a time constant below milliseconds is not possible. To overcome this restriction, we used an approach where each point of the capacitance transient is measured individually in a step-by-step manner. The method was already applied to measure the write times in QD-based memory structures.[8] The approach works as follows [see Fig. 1(b)]. At first, the QDs are completely filled by applying a voltage of 0 V (step 1 in Fig. 1). After filling, the first capacitance measurement is performed at the storage position at V_r=−7.2 V (step 2). Then, a short erase pulse to a high reverse bias V_{pulse} is applied to erase the information from the QDs (step 3). After the erase pulse, the storage voltage is applied again and a second capacitance measurement is taken (step 4). The difference of the two capacitance values yields the maximum hysteresis opening C_{max}. Emission rates are now obtained in the following way. By stepwise shortening the erase pulse width, the amount of charge escaping from the QDs during erasing is reduced successively. Since the hysteresis opening is directly related to the remaining charge in the QDs, after applying an erase pulse with a certain width, C_{max} decreases as well. Finally, the reduction of C_{max} is proportional to the capacitance value on a conventionally recorded capacitance transient after the applied erase time. The capacitance transient is thus recorded step-by-step by measuring C_{max} in a series of measurements with decreasing erase pulse widths.

Here, we applied erase pulse widths from 10^3 down to 10^{-6} s. Figure 2 shows normalized C_{max} against the erase pulse width for a selection of applied bias voltages from -20 to -10 V. The maximum bias was limited by the breakthrough voltage of the diode. The electric field strengths at the position of the QDs given in Fig. 2 are derived by using the Schottky approximation.[19] As expected, the hysteresis opening decreases if the erase pulse width is shortened and vanishes[20] when the QDs are not sufficiently discharged anymore. As previously done for the write times,[8] we defined the limit of the erase time at a value of 50% C_{max}. The erase time limit is strongly dependent on the electric field as we expect for both pure and/or phonon-assisted tunneling. The erase time limit increases from 1.5 ms at 206 kV/cm to 15 s at 95 kV/cm.

The inverse of the erase time limit can be interpreted as the total emission rate for 50% discharging, as described in Eq. (1). In Fig. 3, these emission rates are plotted against the inverse electric field for a set of different temperatures. In this depiction, an emission process based on pure tunneling shows a linear dependence, whereas phonon-assisted tunneling should show nonlinear and thermal activation should show no dependence on the inverse electric field [cf. Eq. (1)]. Below an inverse electric field of 6 cm/MV (left gray area), the expected linearity can clearly be seen for all temperatures indicating pure tunneling as the underlying emission process. Above an inverse electric field of 8 cm/MV, the opposite is the case. Almost no dependence on the inverse electric field is observed but a clear dependence on the temperature, indicating pure thermal activation as the underlying

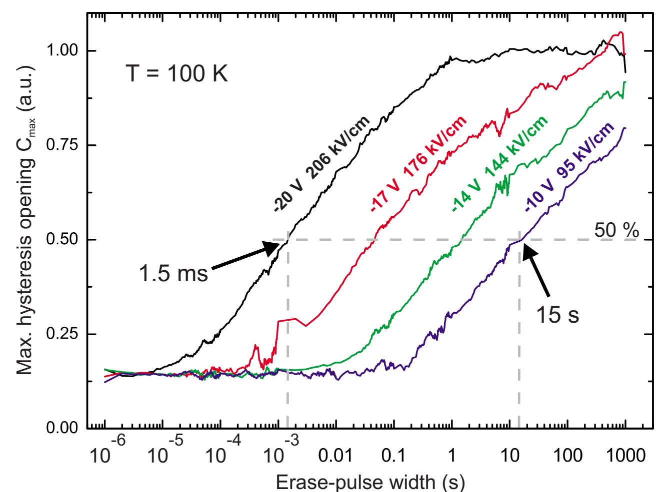

FIG. 2. (Color online) Selection of erase time transients at different applied bias voltages at 100 K. As the erase pulse width decreases, a decrease in the hysteresis opening is observed. The maximum reverse bias voltage is limited by the diode breakthrough voltage.

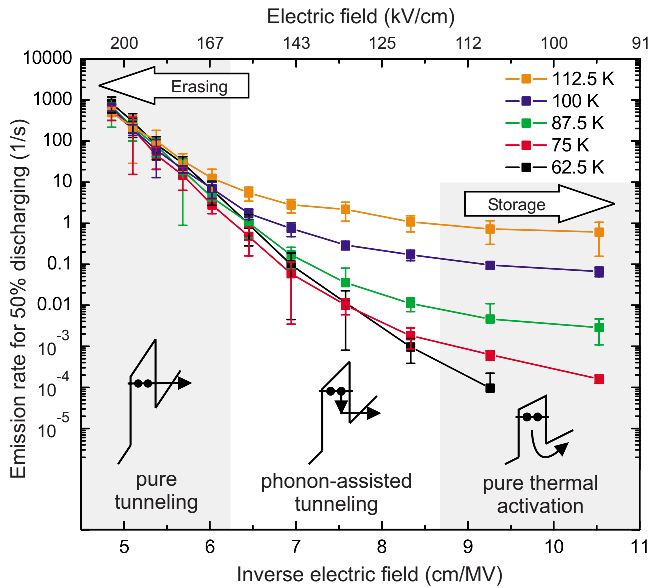

FIG. 3. (Color online) Emission rate for 50% discharging against the inverse of the electric field. A pure tunneling emission process has a linear dependence (left gray area), whereas pure thermal activation is independent of the electric field (right gray area), the area in between is governed by phonon-assisted tunneling.

emission process (right gray area). The area in between is governed by a combined emission process—phonon-assisted tunneling—which is both electric field and temperature dependent.

Since for a given temperature the emission rate increases with increasing electric field, carriers in a QD-based memory must be stored at low electric fields. The storage time is then limited by thermally activated escape of charge carriers as previously assumed in Ref. 9. In contrast, erasing should be done in the high electric field region as the emission rate is maximal for pure tunneling and the tunneling time, i.e., the erase time, can easily be adjusted by the electric field, which is strongly dependent on the doping concentration of the *p-n* diode and the applied bias.

Based on Eq. (1), the linear part can be extrapolated to obtain the electric field, which would be necessary to reach shorter erase times. From such an extrapolation, an electric field of approximately 500 kV/cm for an erase time of 10 ns and an electric field of approximately 700 kV/cm for an erase time of 1 ns is obtained. Although this is a rough estimate, the values are promising for future optimization of the QD-Flash, because the electric fields are still in a moderate range (in Flash memories electric fields of 8–10 MV/cm are used[21]), and a realization of higher electric fields in a QD-Flash can be easily achieved by increasing the doping concentrations in the *p-n* diode.

In conclusion, we have studied the erase times of a QD based memory with capacitance-voltage spectroscopy introducing a method where emission transients are measured pointwise. This enabled us to probe an enlarged span of time constants ranging from 10^{-6} up to 10^{3} s. We determined a 50% erase time of 1.5 ms at 100 K for type-II $GaAs_{0.4}Sb_{0.6}/GaAs$ QDs. A strong dependence of the erase time on the applied bias was observed and the underlying emission processes could be clearly distinguished to be either pure tunneling, phonon-assisted tunneling, or pure thermal activation. Storage conditions of a QD memory should be designed such that the storage time is governed by pure thermal activation whereas the erase process leading to the shortest erase times should be based on pure tunneling. An extrapolation for the pure tunneling range yields an electric field of ~500 kV/cm necessary for a 50% erase time of 10 ns and ~700 kV/cm for 1 ns, respectively. Such high electric fields can be easily realized by changing the doping concentration or the position of the QDs in the *p-n* diode.

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