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A write time of 6 ns for quantum dot–based memory structures

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The concept of a memory device based on self-organized quantum dots (QDs) is presented, enabling extremely fast write times, limited only by the charge carrier relaxation time being in the picosecond range. For a first device structure with embedded InAs/GaAs QDs, a write time of 6 ns is demonstrated. A similar structure containing GaSb/GaAs QDs shows a write time of 14 ns. These write times are independent of the localization energy (e.g., storage time) of the charge carriers and at the moment are limited only by the experimental setup and the parasitic cutoff frequency of the *RC* low pass of the device. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2890731]

Mainly, two memory types dominate the present semiconductor memory market: the dynamic random access memory[1] (DRAM) and the flash[2–4] memory. Both types have their advantages and disadvantages concerning access speed, endurance, and storage time. DRAMs provide fast access times (below 20 ns)[5] and good endurance ($>10^{15}$ read/write cycles), but the stored information has to be refreshed within tens of milliseconds (they are volatile). Flash memories are nonvolatile with storage times in the order of 10 years but exhibit a bad endurance (15^6) and a slow write speed ($\sim\mu$s). Development of faster flash memories with better endurance is presently actively pursued. Phase change memories and magnetic random access memories,[6] (MRAM) are two alternative memory concepts which have the potential to replace todays DRAM and/or flash memory. Both concepts are less scalable than charge-based memories. Therefore, charge-based memory concepts superior to present ones concerning speed, retention time, cost, and power consumption are searched for. They have to be scalable to a feature size below 32 nm to extend Moores' law beyond the year 2012.[7]

Self-organized quantum dots (QDs) might provide very fast write times due to their large capture cross section.[8] Earlier work on a nanowire-based memory[9] with multiple InAs QDs separated by thin InP barriers already showed a minimum write time of 15 ns, limited by the resonant tunneling time through the barriers. In this letter, we present a memory concept[10,11] based on QDs, which should enable very fast write times (<ns) independent of the carrier storage time, e.g., in combination also with a long storage time (>10 years). The write time in our concept is limited only by the charge carrier relaxation time from the band edge into the QD states, which is below picoseconds at room temperature,[8,12] more than four orders of magnitude faster than the write time of a DRAM cell. We previously showed for InAs QDs with an $Al_{0.9}Ga_{0.1}As$ barrier a storage time of seconds at room temperature and proposed more than 10^6 years for GaSb QDs in an AlAs matrix.[13] Here, we demonstrate a fast write time of 6 ns, three orders of magnitude faster than that of present flash memories, for such a QD-based memory structure. This value is at the moment limited only by the parasitic cutoff frequency of the *RC* low pass. Much faster write times are expected for improved device structures.

In a conventional flash memory, a Si-based floating gate placed between two SiO_2 barriers stores the electrons. The SiO_2 barriers have the enormous energetic height of 3.2 eV, essential to store electrons for more than 10 years at room temperature. The barrier height is fixed, and during the write process, the floating gate has to be charged with electrons by Fowler–Nordheim tunneling and/or hot-electron injection. Both charging mechanisms cause the two main disadvantages of a flash cell: the slow write time in the order of microseconds and the poor endurance in the order of 10^6 write/erase cycles.

Our concept of a QD-based memory eliminates the drawbacks of the "fixed height" of SiO_2 barriers by using a tunable barrier height which can be decreased during the write operation. In addition, using III-V compound semiconductors allows band structure engineering with an *adjustable* localization energy which determines the charge carrier storage time.[13,14] Our concept consists of the following three parts:

1. The QDs are used as storage units for the charge carriers (holes or electrons).
2. The QDs are placed inside a *p-n* or *p-i-n* diode structure, nearby or inside the depletion region. By modifying the depletion region, the memory operations—storage, writing, and erasing—are realized.
3. The read operation is realized by placing a two-dimensional electron gas below the QD layer, like in a conventional flash cell.[6] This principle was already demonstrated for the readout process in a QD-based memory by Balocco *et al.*[15]

The charge carrier storage and the write/erase operations work as follows, schematically depicted in Fig. 1: At zero bias, the doping concentration and the location of the QDs in the structure are adjusted such that the QDs are inside the depletion region. This represents the storage situation [Fig. 1(a)]. The width of the depletion region can be adjusted by an applied external bias. A forward bias reduces the width, and the QDs are outside the depletion region [Fig. 1(b)]. Hence, in contrast to the flash memory concept with fixed SiO_2 barrier height, the capture barrier is eliminated and very fast capture into the QD states is possible. To erase the in-

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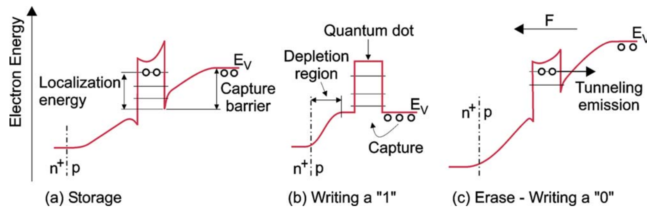

FIG. 1. (Color online) Schematic illustration of the storage (a), write (b), and erase (c) processes in the proposed QD-based flash memory based on hole storage. A fast write time is expected since the carrier capture process occurs directly from the band edge.

formation, a high reverse bias is applied to the diode [Fig. 1(c)]. The QDs are inside the depletion region with a strong electric field enabling tunneling of the charge carriers through the triangular barrier.

To prove the feasibility of this concept and to confirm fast write times independent of the storage times, we have measured the write time of two different structures containing type I InAs/GaAs and type II GaSb/GaAs QDs. The first structure contains InAs QDs embedded in a slightly p-doped GaAs matrix ($p \sim 3\times10^{16}$ cm^{-3}). On its top, a highly n doped ($n\sim 7\times10^{18}$ cm^{-3}) GaAs cap layer was deposited forming the n^+-p diode. The sample structure is described in detail in Ref. 16. The InAs QDs can now be charged with holes in a controlled way by an applied reverse bias. The second structure contains GaSb QDs inserted also in a slightly p-doped region of a n^+p-diode structure. This structure is described in detail in Ref. 17.

The holes in the QDs (which represent the stored information) were here read out by measuring the capacitance of the p-n diode. The capacitance of a diode structure with embedded QDs depends on the number of holes stored inside the depletion region. A larger capacitance corresponds to unoccupied QDs ("0"), while a smaller capacitance represents a "1," in which the QDs are filled with holes.

Figure 2 shows the switching between the two states by a hysteresis curve of the capacitance for both samples. At a

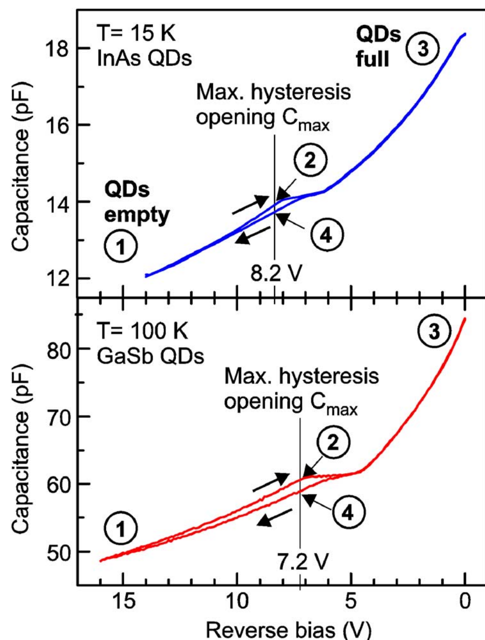

FIG. 2. (Color online) Capacitance sweeps of a p-n diode containing InAs/GaAs (a) and GaSb/GaAs (b) QDs.

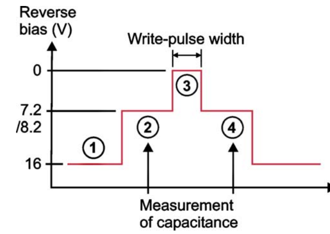

FIG. 3. (Color online) Operation principle for measuring the write time; the labeled numbers refer to the numbers in Fig. 2.

reverse bias of 16 V (point 1), the charge carriers tunnel out of the QDs (erasing of the information). If the reverse bias is now swept from 16 V to the storage situation at 8.2 V (InAs QDs) or 7.2 V (GaSb QDs), the QDs are empty and a larger capacitance is observed (point 2). If the bias is swept to 0 V (point 3), the QDs are charged with holes and a smaller capacitance is observed upon sweeping back to the storage situation (point 4). The maximum hysteresis opening is now defined at the storage position as the difference between both capacitance values for 0 and 1 states.[18]

To study the limit of the write time, series of write pulses were applied with decreasing pulse widths down to 300 ps. The operation principle is schematically depicted in Fig. 3. The cycle started with a 10 s long erase pulse at V_r=16 V (point 1). Then, the capacitance of the device structure was measured at the storage position (point 2) at 7.2 V (GaSb QDs) and 8.2 V (InAs QDs). A write pulse of V_r=0 V was applied to the device (point 3), and the capacitance was again measured at the storage situation (point 4). The maximum hysteresis opening $C_{\max}$ was plotted versus the write-pulse width in Fig. 4. The limit of the write time is reached when the QDs are not sufficiently charged anymore. The hysteresis opening $C_{\max}$ vanishes, and we define the limit as a drop in $C_{\max}$ to 50%. One measurement cycle takes tens of seconds. Therefore, we reduced the temperature down to 25 K for the InAs QDs to obtain a hole storage time that is longer than one cycle of the write time measurements. Analogously, for the GaSb QDs, a higher temperature of 100 K can be used to get a sufficiently long storage time, as the localization energy in GaSb QDs is more than twice as high than in InAs QDs.[13]

A minimum write time of 6 ns for the InAs QD sample is obtained. For the GaSb QD sample—having a hole localization energy which is more than twice as high—we mea-

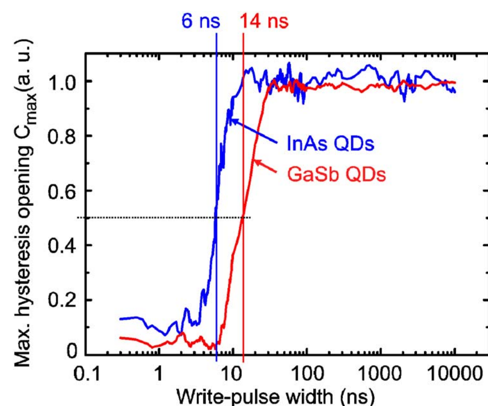

FIG. 4. (Color online) Maximum hysteresis opening $C_{\max}$ for varying write-pulse width. The InAs QD memory is sufficiently charged for write pulses down to 6 ns. Analogously, the information in the GaSb QD memory structure can be written down to 14 ns.

sured a write time of 14 ns, three orders of magnitude faster than that of present flash cells. Both write times are almost equal and already in the order of the write time of a DRAM cell. The measured write times are at the moment only limited by the experimental setup and the parasitic cutoff frequency of the *RC* low pass of the devices, which are slightly different. This assumption is confirmed by additional measurements at different temperatures on the same device which showed a temperature-independent write time and by previous measurements[8] of the same structure, in which average hole capture and relaxation times were found to be in the order of picoseconds. Therefore, much faster write times below 1 ns, as well at room temperature, which are independent of the localization energy should be feasible for improved memory structures having higher external cutoff frequencies.

In conclusion, we have presented a memory concept based on self-organized QDs, enabling very fast write times in combination with long storage times. The physical limitation of the write time of such a QD-based memory is given by the relaxation time of the charge carriers known to be in the picosecond range. We demonstrated here a write time of 14 ns for GaSb/GaAs QDs and 6 ns for InAs/GaAs QDs. These write times are at the moment limited by the experimental setup and the parasitic cutoff frequency of the *RC* low pass of the devices. Faster write times below 1 ns are expected for improved device structures.

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