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Hole-based memory operation in an InAs/GaAs quantum dot heterostructure

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We present an InAs/GaAs quantum dot (QD) memory structure with all-electrical data access which uses holes as charge carriers. Charging and discharging of the QDs are clearly controlled by a gate voltage. The stored information is read-out by a two-dimensional hole gas underneath the QD-layer. Time resolved drain-current-measurements demonstrate the memory operation. Present write times are 80 ns. © *2009 American Institute of Physics*. [doi:10.1063/1.3275758]

Distinct types of memories will combine the advantages of nonvolatility of the Flash-memory[1] and the performance and endurance of the dynamic random access memory (DRAM).[2] A large variety of such memory concepts has been proposed using different approaches, like FeRAM, MRAM, PCRAM, etc.[3] One of the most promising options for charge-based memories is based on self-organized quantum dots (QDs) as memory units. Memory operation for III-V QD structures has been demonstrated, either based on optically[4–6] or electrically controlled charge storage.[7–9] All these memory structures were based on electron storage. A two-dimensional (2D) electron gas was used to detect the state of the memory. We have recently proposed an alternative all-electrical memory concept based on III-V QDs (QD-Flash)[10,11] which allows the storage of holes.

Hole storage offers significant advantages with respect to scalability and storage time. The energy levels of confined holes in a QD are much more closely spaced than those of electrons due to their larger effective mass.[12,13] Thus, at least one order of magnitude more holes can be stored in a given volume than electrons. In addition, hole-confining type-II systems (e.g., GaSb/AlGaAs QDs) provide huge hole localization energies leading to storage times of more than ten years at room temperature,[14] a basic prerequisite for a nonvolatile memory.

In this letter, we present the prototype of an InAs/GaAs QD memory structure which uses holes as charge carriers instead of electrons. For monitoring, the commonly used electron channel is replaced by a 2D hole gas (2DHG) embedded underneath the QD layer. Static and time-resolved measurements of storage, write, and erase times demonstrate the feasibility of the hole-based QD-Flash concept.

The prototype consists of a quantum-well modulation-doped field-effect transistor with a single InAs/GaAs QD layer in close vicinity to the 2DHG. A schematic cross section of the layer structure grown by metalorganic chemical vapor deposition is shown in Fig. 1(a). A 1 μm thick undoped GaAs buffer layer was grown first on an undoped GaAs substrate. The 2DHG was formed with 40 nm p-doped ($p=2\times10^{18}$ cm^{-3}) GaAs, a 7 nm thick undoped GaAs spacer layer, and an 8 nm thick $In_{0.25}Ga_{0.75}As$ quantum well. Subsequently, 20 nm undoped GaAs was deposited, followed by a single InAs QD layer (nominally ~1.8 ML). Finally, the structure was completed by a 180 nm undoped GaAs cap. The heterostructure was processed into Hall bars with an active area of 310×460 μm^2 using chemical wet etching [see Fig. 1(b)]. The source and drain areas were metallized using a Ni/Zn/Au alloy which was annealed at 400 °C for 3 min to form ohmic contacts down to the 2DHG. The gate was formed by Ni/Au. Hall measurements yielded a charge carrier density and a mobility of the 2DHG at 77 K of 8×10^{11} cm^{-2} and 4350 cm^2/Vs, respectively.

Figure 2 schematically shows the valence band of the structure for the three memory operations: storage, writing, and erasing. At the storage position [Fig. 2(a)], the binding potential of holes in the QDs represents the emission barrier, needed to store a logic "1." To store a logic "0" (defined as empty QDs) a capture barrier is necessary, which is formed by the band-bending of the Schottky contact. The storage time for both logic states is limited by the emission and capture processes of the QDs.[15,16] In our structure, thermally assisted tunneling across the emission and capture barriers initiates the discharging and charging processes.[17,18] The emission and capture rates depend on the barrier height (i.e., localization energy and capture barrier height), the temperature, and the electric field. To write a logic "1" [Fig. 2(b)] a negative bias is applied to the gate. This completely eliminates the capture barrier formed by the band-bending and fast write times down to nanoseconds can be realized.[11] Thus, the QD-Flash concept solves the drawbacks of Flash's SiO_2 barriers by using a large barrier height which can, however, almost be decreased to zero during write operation. Write times similar to those of DRAMs or even shorter are possible. To erase the information [Fig. 2(c)] the electric field at the position of the QDs is increased by applying a positive bias such that tunnel emission occurs. The read-out of the stored information is done via the 2DHG below the QD layer. Carriers stored in the QDs reduce the charge density and the mobility in the 2DHG resulting in a lower conductance of the 2DHG when the QDs are occupied.

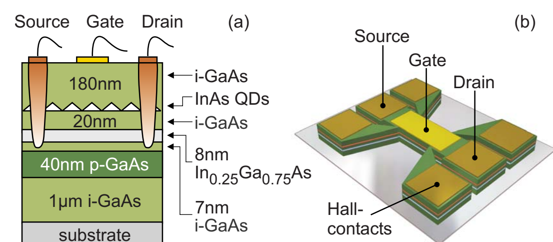

FIG. 1. (Color online) (a) Schematic cross section of the layer structure. (b) Sketch of the QD-Flash prototype. Hall-contacts are used for transport measurements of the 2DHG.

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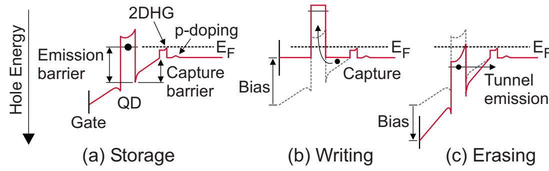

FIG. 2. (Color online) Schematic illustration of the storage (a), write (b), and erase (c) operations in the QD-Flash prototype.

To investigate the influence of holes stored in the QDs on the conductance of the 2DHG, the drain current I_D versus gate voltage V_G was measured in the dark with a fixed drain-source voltage of 100 mV. Figure 3(a) shows the measured hysteresis at a temperature of 50 K. The measurement cycle starts with a 10 ms long charging pulse ($V_G = -1$ V), which shifts the QD states below the Fermi level, charging them with holes from the 2DHG [see Fig. 2(b)]. When the gate voltage is now swept to 1.5 V, the drain current decreases until the 2DHG is pinched off at about 1.1 V. During the down sweep the QDs remain occupied, if the sweep time is shorter than the hole storage time in the QDs. At $V_G = 1.5$ V the QD states are far above the Fermi level [see Fig. 2(c)] and tunnel emission discharges the QDs. When the gate voltage is swept back to -1 V a larger current is observed leading to a distinct hysteresis opening. The hysteresis originates from the influence of holes stored in the QDs on the conductance of the 2DHG during the down sweep. The charged QDs act as Coulomb scattering centers, reducing the mobility of the 2DHG.[19,20] In addition, using Gauss' law it was predicted that the transfer of holes in QDs lead to a reduction in the carrier density in the 2DHG.[21–23] Both, the lowered charge carrier density and the decreased mobility reduce the conductance during the down sweep, resulting in a lower current trace compared to the up sweep.

The maximum hysteresis opening (with respect to the up sweep) is shown in Fig. 3(b) as a function of temperature for two different sweep times. Using a sweep time of 1 ms, the hysteresis opening drops from 32% at 20 K to almost zero at 85 K. The descent has its origin in the reduced charge carrier storage time of QDs with increasing temperature, i.e., at higher temperatures more holes are emitted during the down sweep. Balocco *et al.*[7] have previously reported a high-temperature memory effect due to deep levels for a similar InAs QD-structure. Here, the absence of such high-temperature memory effects proves that not deep levels but in fact the QDs act as memory units. This conclusion is confirmed by previous investigations of hole emission from similar InAs/GaAs QDs by deep level transient spectroscopy,[15] which resulted in a thermal emission time constant of 5 ms at 90 K for the QD hole ground state, in agreement with the disappearance of the hysteresis at 85 K

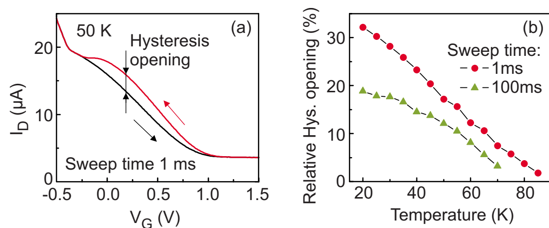

FIG. 3. (Color online) (a) Hysteresis at 50 K. (b) Temperature dependence of the hysteresis opening for a sweep time of 1 and 100 ms, respectively.

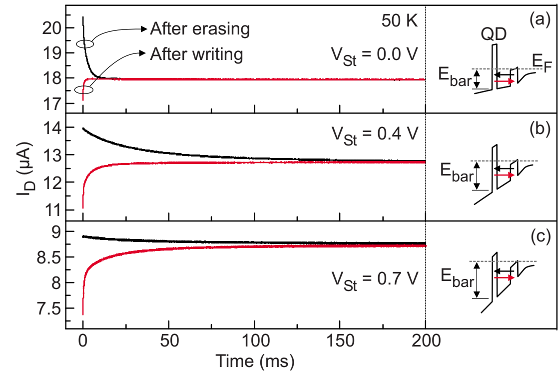

FIG. 4. (Color online) Drain current transients at 50 K at a storage voltage of 0 V (a), 0.4 V (b), and 0.7 V (c). Insets show the valence band profiles at the given voltages.

for a sweep time of 1 ms. A sweep time of 100 ms further reduces the hysteresis opening as compared to 1 ms, since more holes, stored in the QDs, are emitted during the slower down sweep. An increased maximum hysteresis opening is expected using larger QD densities and/or multiple QD layers.

The memory operation of the QD-Flash prototype is studied by time-resolved measurements of the drain current at different storage voltages V_{St}, with either initially occupied or empty QDs. The QDs are charged or discharged by applying a gate voltage of -0.8 or 2 V, respectively. After this initialization of the "1" or "0," the gate voltage was abruptly changed to the storage voltage and the drain current was measured as a function of time. Figure 4 shows the transients at 50 K for three different storage voltages (0, 0.4, and 0.7 V). The upper transients represent hole capture into initially empty QDs, leading to a decrease in the conductance of the 2DHG and, hence, to a decrease in the drain current. The lower transients represent hole emission out of fully occupied QDs and, thus, the drain current increases to the equilibrium state. A change of the storage voltage from 0 to 0.4 V and further to 0.7 V causes multiple effects [Figs. 4(a)–4(c)]; the time constants of both transients increase, the amplitude of the capture transient is reduced, and the amplitude of the emission transient is increased. These effects can be explained by the changes of the capture and emission processes when applying a positive storage voltage to the structure. On the right hand side of Figs. 4(a)–4(c) the valence band profiles for the three storage voltages are shown. The amplitudes of the transients represent the amount of transferred holes and are correlated with the number of levels which are below the Fermi level (for capture) and above the Fermi level (for emission). A larger positive storage voltage shifts the Fermi level toward the QD ground state and, hence, more holes are emitted, less holes are captured, and thus the amplitudes vary. The prolongation of the time constants is also related to the Fermi level shift as it leads to an increased capture and emission barrier height (E_{bar} in Fig. 4).

Finally, we measured the write and erase times of the memory structure. To determine write and erase times, we used a method which allowed to study emission from or capture into QDs across an enlarged span of time constants (described in detail in Ref. 24). The hysteresis opening at a storage position of 0.4 V was measured after applying write/erase pulses with successively reduced pulse widths down to 10 ns. When the pulse width was too short for any charging/

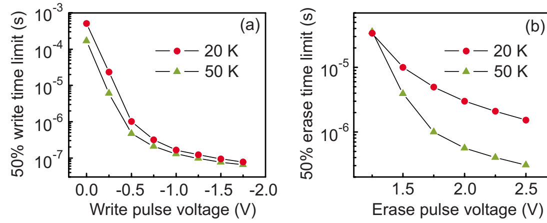

FIG. 5. (Color online) Write times (a) and erase times (b) in dependence on the pulse voltage.

discharging of the QDs, the hysteresis opening vanished. We defined the write/erase time as the pulse width, at which the hysteresis opening drops to 50% of the maximum value. Figure 5(a) shows the write time in dependence on the write pulse voltage at 20 and 50 K. A more negative write pulse leads to a reduction in the capture barrier during writing and, hence, the write time decreases exponentially. For write pulses larger than $|0.5|$ V the write time starts to saturate and reaches a minimum at 80 ns for a write pulse of -1.75 V. This saturation has presently its origin in a parasitic cutoff frequency of about 2 MHz of the *RC* low pass of our present devices. Much faster write times are expected for smaller devices having larger parasitic cut-off frequencies. The erase times are shown in Fig. 5(b). A minimum erase time of 350 ns at 50 K was obtained for an erase pulse of 2.5 V. The temperature dependence of the write and erase times reflects again the increased thermal capture and emission rates at higher temperatures.

In conclusion, we presented the prototype of a hole-based memory device using InAs/GaAs QDs for charge carrier storage. Charging and discharging of the QDs are clearly controlled by a gate voltage. We demonstrated read-out of the stored information using a 2DHG, with a relative hysteresis opening up to 32%. Write and erase times were studied. Write times down to 80 ns only a factor of 8 larger than for a typical DRAM[25] and erase times of 350 ns four orders faster than for a typical Flash[1] were demonstrated. The results support our assumption that the QDs act as memory units and confirm the feasibility of our hole-based memory concept.

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