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Soft-switching non-isolated high step-up three-level boost converter using single magnetic element

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Abstract

Here, a soft switched three-level boost converter with high voltage gain is proposed which is suitable for high step-up applications with wide output power range. In this converter, a ZVT auxiliary circuit is used which provides soft switching in a wide range of output power independent of load variation. Utilizing coupled-inductors with one magnetic core removes extra auxiliary core in the soft switching circuit and provides high voltage gain in conjunction with size reduction. Also, the secondary and tertiary leakage inductances of the coupled-inductors minimize the reverse recovery problem of the output diodes. Due to its three-level structure, it has very low voltage stress over semiconductor elements in comparison to the existing interleaved structures, resulting in using MOSFETs with low on-resistance and thus lower conduction losses and cost. Operating modes as well as analytical analysis of the proposed converter are discussed. Finally, in order to validate the proposed converter performance, experimental results from a 200-W laboratory prototype are presented.

1 | INTRODUCTION

Nowadays, global warming and its impact on environment are turned into a major concern for human beings. Burning fossil fuels to generate energy is known as the main reason for global warming issue. On the other hand, fossil fuel resources are finite, which should be saved for the next generations. Therefore, using renewable energy sources such as photovoltaic (PV) energy is exigent. However, the output voltage of PV panels is relatively low, which cannot satisfy the high voltage DC-link requirements for grid-connected inverters. Connecting several PV panels in series is one solution, which has a number of problems such as module mismatch and shading effect especially for low and medium power applications [1, 2]. The alternative solution is using high step-up DC-DC converters to increase the low output voltage of PV panels. Other applications of high step-up DC–DC converters are fuel cells, batteries, ultra-capacitors used in motor drives, uninterruptible power supplies (UPS), and electric vehicles (EV) [3–5]. A diagram illustrating the usage of high step-up dc-dc converters in renewable-energy-based applications can be observed in Figure 1.

The conventional boost converter is a basic step-up structure, which cannot be employed in high voltage applications because of its low voltage gain, low efficiency, and high switch voltage stress [4]. One solution to reduce the voltage stress of the boost converter is using a three-level boost structure using two switches. The schematic of the conventional three-level boost converter is presented in Figure 2. The voltage stress is halved over each switch, enabling the usage of MOSFETs with lower drain-to-source on-resistance ($R_{ds(on)}$) and lower

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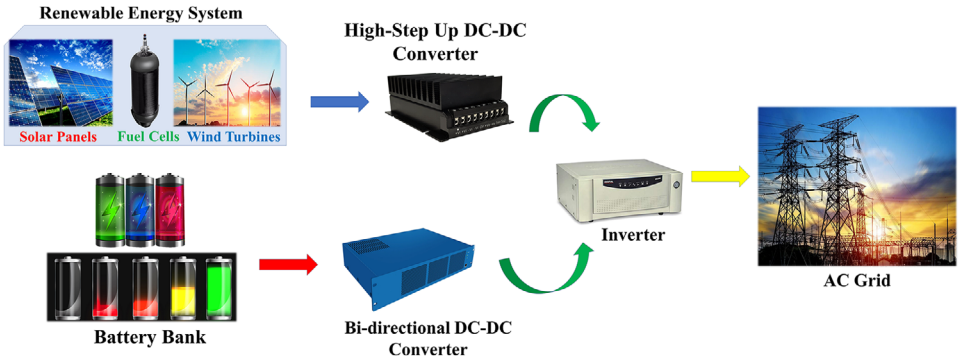

FIGURE 1 Diagram of a grid connected renewable energy system

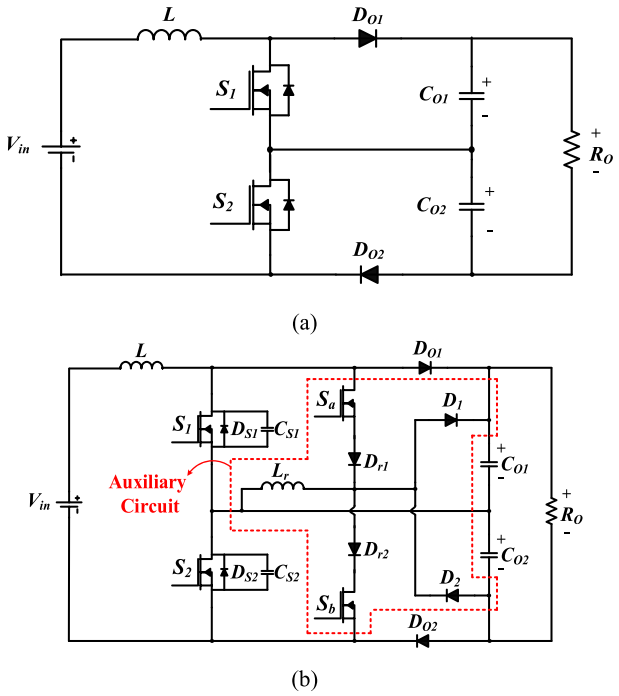

FIGURE 2 Conventional three level boost structure. (a) Hard switching (b) soft switched with ZVT circuit in [10]

conduction loss of the converter. Another two-switch structure based on a boost converter is interleaved boost using two switches and two extra input inductors. In this structure, the input current is divided between switches and thus the current stress of switches is halved [3, 6]. The voltage stress of switches in the interleaved boost structure is two times its three-level counterpart just like the conventional boost converter. The main issue for both three-level boost converter and interleaved boost circuit is that their voltage gain is equal to the conventional boost converter and they still cannot be used for high step-up applications. Additionally, their hard switching operation reduces their usage in high-frequency applications due to high switching loss.

To increase the voltage gain of the boost converter and their derivatives, different methods like coupled-inductors and voltage multiplying cells are presented which can prevent converters from operating with high duty cycles [7]. In [8–10], different three-level high step-up boost converters and in [11–15], interleaved high step-up boost structures based on the abovementioned step-up methods are introduced. In [9], a coupled-inductor based three-level converter is introduced, the voltage gain is a bit higher than the conventional three-level and both switches have low voltage stress, however, diode reverse recovery losses considerably degrade the efficiency. Same problems exist in [8] along with using four power switches which degrades the power density and cost. In [11, 12] interleaved high step-up converters using coupled inductors and voltage multiplying cells are introduced. Although in these converters the voltage gain is high, hard switching operation degrades the efficiency.

To improve the efficiency of DC–DC converters and reduce switching losses, different soft-switching methods are introduced including lossless snubbers [17–19], active clamp circuits [20–23], zero voltage/zero current transition (ZVT/ZCT) methods [10, 13–15] and resonant converters [24, 25]. Among these methods, ZVT converters benefit from load-independent soft-switching condition. Likewise, unlike resonant converters, the ZVT converters operate with constant frequency and optimum design of the magnetic components of LC filter is achieved, which is the benefit of pulse width modulation (PWM) converters [24].

In [16–19], interleaved converters employing lossless snubbers are proposed. In the lossless snubbers-based structures, the main switches turn on under ZCS condition, which has high capacitive turn-on loss (E_{oss}). For the interleaved structure in [16] which uses lossless passive snubber, the voltage gain is increased by diode-capacitor voltage multiplying cells. However, it suffers from reverse recovery losses and a complex structure with the large number of components. In [23, 26], high voltage gain three-level boost converters with active clamp soft switching circuits are proposed. The main limitation of these converters is that they cannot provide soft-switching condition at the wide range of output load. Also, the converter in [26] uses four active switches and a complex control circuit. In [23], an active clamp interleaved converter is proposed which suffers from the high number of components including four power switches and three magnetic cores, plus losing soft switching at light loads.

By using ZVT cells, load-independent soft-switching condition is achieved in [10] for the conventional three-level boost converter (Figure 2) and its conventional interleaved counterpart in [6], which both have a voltage gain equal to the conventional boost converter. In the ZVT interleaved converter in [14], the voltage gain is improved by employing coupled inductors. However, three magnetic cores are required and the structure is complex due to the larger number of elements used. In [15], the presented ZVT interleaved converter employs two coupled inductors and voltage multiplying cells to increase the voltage gain. Nevertheless, the required four power switches and two magnetic cores complicate the structure. In the interleaved topology in [13], two extra ZVT cells are employed which have lots of components including two extra inductors, four capacitors, and two extra switches which results in a high amount of conduction losses and low power density. Note that, the only three-level boost converter which is proposed based on ZVT soft-switching structure is the converter in [10] and as mentioned earlier it has voltage gain equal to the conventional boost converter and cannot be used for high step-up applications. More importantly, the employed ZVT auxiliary cell in this converter has a very high number of components composed of two extra switches, four diodes, and an extra auxiliary magnetic element Figure 2.

Here, a new soft-switching three-level boost converter for high voltage gain applications is proposed, which can provide soft-switching conditions in a wide range of output power, independent of load variations for all semiconductor elements. The three-level structure, which provides converter's switches with low voltage stress, enables using MOSFETs having low $R_{ds(on)}$ and thus low conduction losses. Unlike soft switched three-level converter in [10] and also ZVT interleaved converters in [6, 13–15], the proposed converter uses only one magnetic core by removing the extra core of the resonant inductor in the ZVT cell. This results in reducing the converter size and cost. In this structure, most of the diodes conduct very low current and their losses are not so high to degrade the total efficiency. By providing soft-switching conditions for all semiconductor devices, the reverse recovery and switching losses are alleviated and high efficiency is achieved. Also, the output diode benefits from very low voltage stress which allows using a diode with low reverse recovery and low forward voltage.

Features of the proposed converter can be highlighted as below:

- Very low voltage stress across semiconductor elements
- ZVS soft switching condition for the main and auxiliary switch
- Using coupled inductor and switched capacitor to increase the voltage conversion ratio
- Recycling the leakage inductance energy to the output
- Using only a single magnetic core and reduced size and volume
- Alleviating the reverse recovery losses of the output diodes and efficiency improvement

The paper organization is as follows. In Section 2, the proposed converter topology along with operational principles are discussed. In Section 3, design considerations such as voltage gain expression, selection of elements, and the soft-switching condition are presented. Finally, experimental results of the implemented laboratory prototype and conclusion are provided in Sections 4 and 5, respectively.

2 | OPERATING PRINCIPLES OF THE PROPOSED CONVERTER

The circuit diagram of the proposed high step-up three-level boost converter is shown in Figure 3. The proposed converter consists of three active switches S_1, S_2, and S_A, seven diodes D_1 to D_6 and D_A, and four inductors L_1, L_2, L_3, and L_A which are coupled together with one magnetic core. The proposed circuit also has two snubber capacitors C_{S1} and C_{S2}, two passive clamp capacitors C_1 and C_2, two switched capacitors C_3 and C_4, and two output capacitors C_{O1} and C_{O2}. As illustrated in Figure 3, coupled inductors are modelled by a magnetizing inductance L_m and leakage inductances L_{lk1}, L_{lk2}, L_{lk3}, and L_{lkA} plus an ideal transformer with turns-ratio n_1, n_2, n_3, and n_A. The magnetizing inductance current is assumed to be constant current I_{Lm}.

There are sixteen operation modes in one switching cycle; however, since circuit operation for both main switches S_1 and S_2 is symmetrical, only the first eight modes related to S_1 are examined. The key waveforms of the proposed converter are shown in Figure 4 and the equivalent circuit for each operating interval is illustrated in Figure 5. For simplifying the circuit analysis, the following assumptions are made:

Gating pulses of the main switches S_1 and S_2 are the same as the conventional three-level boost converter with duty cycles > 0.5.

- All the semiconductor devices and passive elements are ideal
- The magnetizing inductance is large enough so its current ripple can be ignored
- The output capacitors C_{O1} and C_{O2}, snubber capacitors C_{S1} and C_{S2}, and the magnetizing inductance L_m are large enough such that their voltage and current ripples can be neglected.
- The output capacitors C_{O1} and C_{O2} are equal.
- Capacitors C_{S1} and C_{S2} are equal
- The two leakage inductances L_{lk2} and L_{lk3} are integrated into L_{lk1}.

Mode 1 [t_0–t_1] (Figure 5): In this mode, both main switches S_1 and S_2 are conducting and energy is stored in magnetizing inductance of the coupled-inductors. Simultaneously, capacitor C_1 is discharged through diode D_6 and its energy is transferred to C_4. All other diodes plus axillary switch S_A are off and C_{O1} and C_{O2} supply the output energy. The current equations of

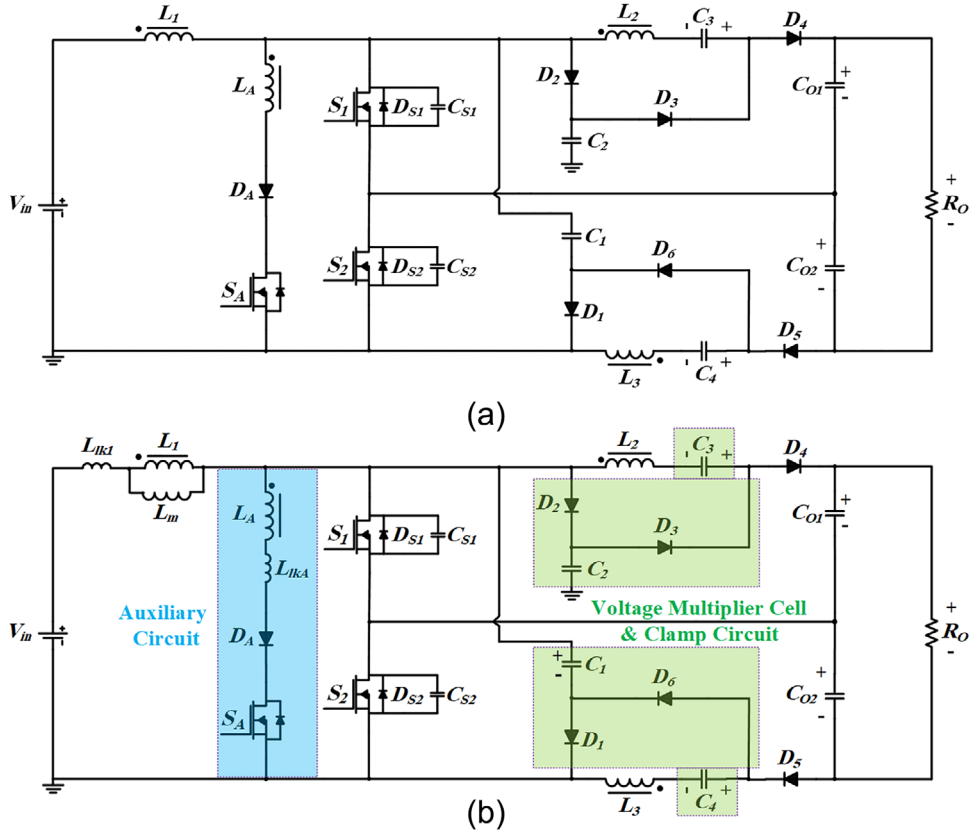

FIGURE 3 The proposed soft-switched three-level boost converter. (a) Schematic (b) equivalent circuit

the leakage inductance L_{lk1} and magnetizing inductance Lm are calculated by:

$$i_{Llk1}\ (t) = i_{Llk1}\ (t_0) + \frac{V_{in} - \frac{V_{C4}-V_{C1}}{n}}{L_{lk1}}\ (t - t_0) \tag{1}$$

$$i_{Lm}\ (t) = i_{Lm}\ (t_0) + \frac{V_{C4} - V_{C1}}{n.L_m}\ (t - t_0) \tag{2}$$

The time duration of this mode is expressed by:

$$\Delta t_1 = t_1\ -\ t_0 = \frac{(2D-1)\ T}{2} \tag{3}$$

Where T is the switching period and D is the duty cycle of the main switches S_1 and S_2.

Mode 2 [t_1–t_2] (Figure 5): At t_1, switch S_1 is turned off while switch S_2 and diode D_6 are still conducting. There is a resonance between L_{lk1}, L_m, and C_{S1}. Since C_{S1} is small, the voltage increment of C_{S1} can be considered linear. As a result, S_1 is turned off under zero voltage condition (ZVS). This mode ends when the voltage of C_{S1} reaches V_{C1}. The voltage across C_{S1} and time interval of this mode are achieved as:

$$V_{CS1}\ (t) = \frac{i_{Llk1}\ (t_1)}{C_{S1}}\ (t - t_1) \tag{4}$$

$$\Delta t_2 = t_2\ -\ t_1 = \frac{V_{C1}.C_{S1}}{i_{Llk1}\ (t_1)} \tag{5}$$

Mode 3 [t_2–t_3] (Figure 5): When the voltage across S_1 reaches V_{C1}, diode D_1 is turned on and the voltage across S_1 is clamped to V_{C1} level. Therefore, the energy of the leakage inductance L_{lk1} is absorbed by the clamp capacitor C_1 and voltage spikes across the main switch S_1 are eliminated. Simultaneously, by decreasing the current of leakage inductance L_{lk1}, diode D_4 starts to conduct and energy of the magnetizing inductance is transferred to the output. The current of L_{lk1} decreases linearly and this mode ends when diode D_6 turns off.

$$i_{Llk1}\ (t) = i_{Llk1}\ (t_2) + \frac{V_{in} - V_{C1} + \frac{n_1}{n_2}V_{L2}}{L_{lk1}}\ (t - t_2) \tag{6}$$

$$V_{L2} = V_{C1}\ + V_{C3} - \frac{V_O}{2} \tag{7}$$

$$\Delta t_3 = t_3\ -\ t_2 = \frac{L_{lk1}\ (i_{Lm} - i_{Llk1}\ (t_2))}{V_{in} - V_{C1} + \frac{n_1}{n_2}V_{L2}} \tag{8}$$

Mode 4 [t_3–t_4] (Figure 5): In this mode, D_6 is off and input energy is transferred to the output. Also, D_1 current reduces linearly to reach zero at t_4. At the end of this, I_{Lk1}

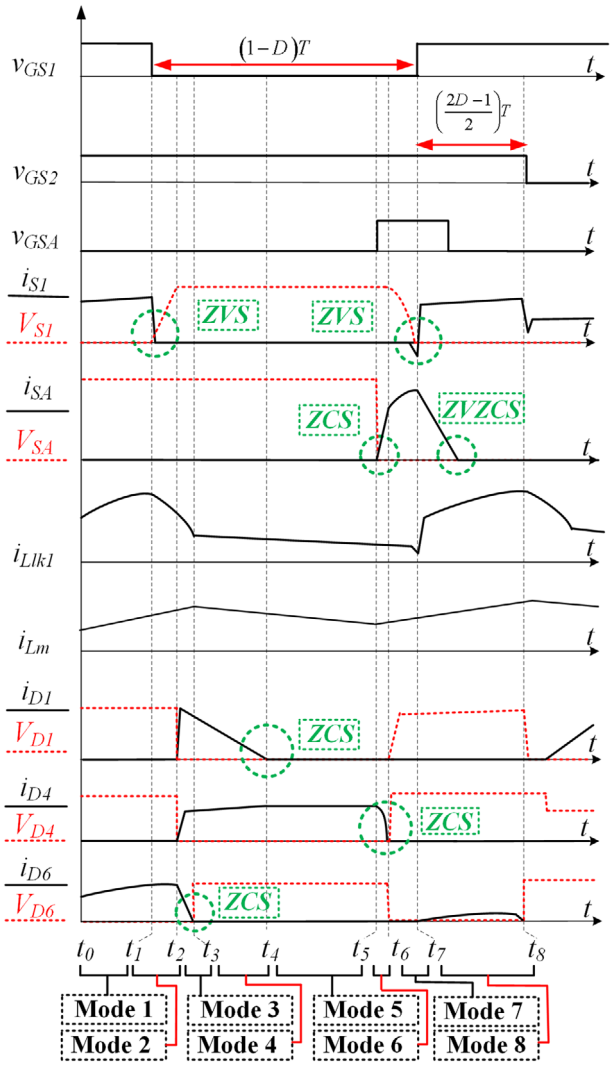

FIGURE 4 The key waveforms of the proposed converter

reaches $(\frac{n_1}{n_1+n_2})I_{Lm}$.

$$i_{Llk1}\ (t) = i_{Llk1}\ (t_3) - \frac{\frac{n_1}{n_2}(V_{L2}) + V_{C1} - V_{in}}{L_{lk1}}(t - t_3) \quad (9)$$

$$V_{C1}\ (t) = V_{C1}\ (t_3) + \frac{\left(L_{lk1} + I_{L1}\left(\frac{n_1}{n_2}\right)\right)\Delta_{t4}}{C_1} \quad (10)$$

$$\Delta t_4 = t_4 - t_3 = \frac{C_1\left[\frac{V_{in}}{1-D} - V_{C1}\ (t_3)\right]}{I_{Llk1} + I_{L1}\left(\frac{n_1}{n_2}\right)} \quad (11)$$

Mode 5 [t_4–t_5] (Figure 5): In this mode, D_1 is off and the input energy is still transferred to the output through D_4. The current of L_{lk1} is equal to the secondary side current of coupled inductor L_2 which can be calculated as Equation (9) by using Kirchhoff's Current Law (KCL).

$$i_{Llk1}\ (t) = \left(\frac{n_1}{n_1+n_2}\right) I_{Lm} \quad (12)$$

$$\Delta t_5 = t_5 - t_4 = (1-D)\ T - (\Delta t_4 + \Delta t_3 + \Delta t_2 + t_d) \quad (13)$$

In which t_d is the delay between switch S_1 and the auxiliary switch.

Mode 6 [t_5–t_6] (Figure 5): This mode starts when the axillary switch S_A is turned on under ZCS due to the series leakage inductance L_{lkA}. As the current in the axillary branch increases, the current through D_4 decreases. In this mode, C_{S1} voltage is considered almost constant. This mode ends when the current through D_4 reaches zero.

$$n_A i_A + n_2\ i_{L2} = n_1\ (I_{Lm} - i_{Llk1}) \quad (14)$$

$$i_{Llk1}\ (t) = i_{Llk1}\ (t_5) + \frac{V_{in} - \left(\frac{1+n_A}{1+n_2}\right)(V_X)}{L_{lk1}}(t - t_5) \quad (15)$$

$$i_{LlkA}\ (t) = \frac{\frac{V_O}{2} - V_{C3} + \left(\frac{n_2}{n_1} - \frac{n_A}{n_2}\right)\left(\frac{V_X}{1+\frac{n_2}{n_1}}\right)}{L_{lkA}}(t - t_5) \quad (16)$$

$$\Delta t_6 = t_6 - t_5 = \frac{V_{CS1}.C_{S1}}{i_{LlkA}\ (t_5)} \quad (17)$$

In which, V_X is: $V_{in} + V_{C3} - \frac{V_O}{2}$

Mode 7 [t_6–t_7] (Figure 5): In this mode, C_{S1} starts to discharge through L_{lkA}. To simplify the analysis, it is assumed that L_{lkA} current is almost constant, so the voltage of C_{S1} decreases linearly. At the end of this mode, C_{S1} reaches zero and D_{S1} starts to conduct. The time duration of this mode is:

$$V_{CS1}\ (t) = -\frac{i_{Llk1}\ (t_5)}{C_{S1}}(t - t_6) \quad (18)$$

$$\Delta t_7 = t_7 - t_6 = \frac{L_{lkA}.I_{Lm}}{\frac{V_{in}}{1-D}} \quad (19)$$

$$i_{SA}\ (t) = i_{SA}\ (t_0) - \left(\frac{nV_{in}}{L_{lkA}}\right).\left(\frac{L_m}{L_m + L_{lk1}}\right)(t - t_7) \quad (20)$$

Mode 8 [t_7–t_8] (Figure 4): At the beginning of this mode, S_1 turns on under ZVS condition. In this mode, the axillary switch current i_{SA} reaches zero. Consequently, switch S_A and diode D_A are turned off under ZCS and the input current flows through S_1 and S_2. As the time duration of mode 8 is too short, it can be neglected.

By the end of this mode, the circuit enters the next eight modes which are complementary with the eight abovementioned modes. In the description of the next eight modes, diodes D_1, D_4, D_6 and the switch S_1 should be replaced by

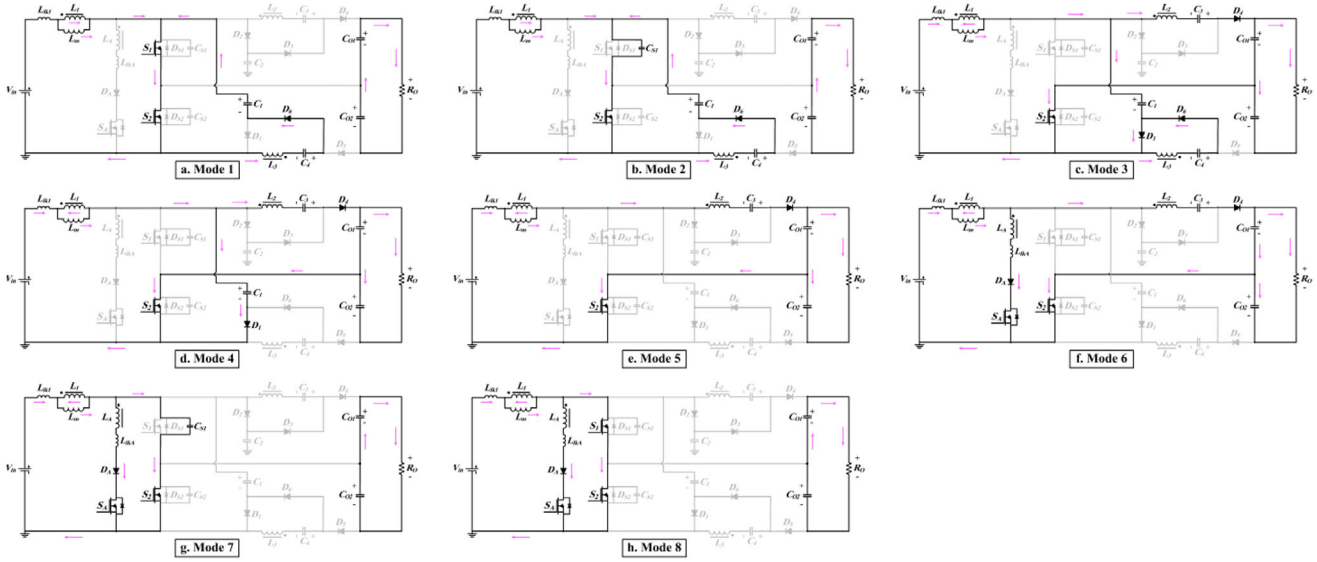

FIGURE 5 Correspondent circuit of the proposed converter associated with switch S

D_2, D_5, D_3, and switch S_2, respectively and the same operating modes will occur.

3 | ANALYSIS OF THE PROPOSED CONVERTER

In this section, design considerations of the proposed converter such as voltage gain, voltage stress of the semiconductor elements, and ZVS range of switches are discussed. Additionally, the performance of the proposed converter is compared with other three-level high step-up converters. Since the duration of modes 2 and 7 are too short in comparison to the other operating modes, these two modes can be neglected.

3.1 | Conversion ratio

The proposed converter stores energy in the magnetizing inductance of the coupled inductors and switched capacitors when both main switches S_1 and S_2 are on and then transfers the energy to the output when one of the switches is turned off. Therefore, the operating duty cycle of the converter should be higher than 0.5. Since the circuit is symmetrical, we have:

$$V_C = V_{C1} = V_{C2} \tag{21}$$

$$V_{C3} = V_{C4} \tag{22}$$

$$n = \frac{n_2}{n_1} = \frac{n_3}{n_1} \tag{23}$$

By using the volt-second balance law for L_{lk1} and L_m and calculating V_{C3} with writing Kirchhoff's Voltage Law (KVL) for mode 8, main equations of the proposed converter are achieved as:

$$KV_{in}\left(D-\frac{1}{2}\right) = (1-D)\left[V_C - \frac{V_A}{n}\right] \tag{24}$$

$$(1-KV_{in})\left(D-\frac{1}{2}\right) = (1-D)\left[V_C - \frac{V_A}{n} - V_{in}\right] \tag{25}$$

$$V_{C3} = V_C + nKV_{in} \tag{26}$$

In which V_A is: $\frac{V_O}{2} - V_{C3} - V_C$

And K is: $\frac{L_m}{L_m + L_{lk1}}$

After some math works and simplification, the expressions for V_C, V_{C3}, and voltage gain ($G = \frac{V_o}{V_{in}}$) are as:

$$V_C = \frac{V_{in}}{2(1-D)} \tag{27}$$

$$V_{C3} = V_{in}\left[\frac{1}{2(1-D)} + nK\right] \tag{28}$$

$$G = \frac{nK+2}{1-D} \tag{29}$$

As it is seen, the voltage gain provided by Equation (29) is sufficiently high that the proposed converter can be used in high step-up applications even without high turns-ratio of the coupled inductors. Figure 6 shows the voltage gain comparison of the proposed converter with converters presented in [6, 14, 15, 20, 27]. As it is clear, the proposed converter provides higher voltage gain than the other three references in [6, 20, 27] while presenting soft switching performance, low voltage stress and a single magnetic core. Although the

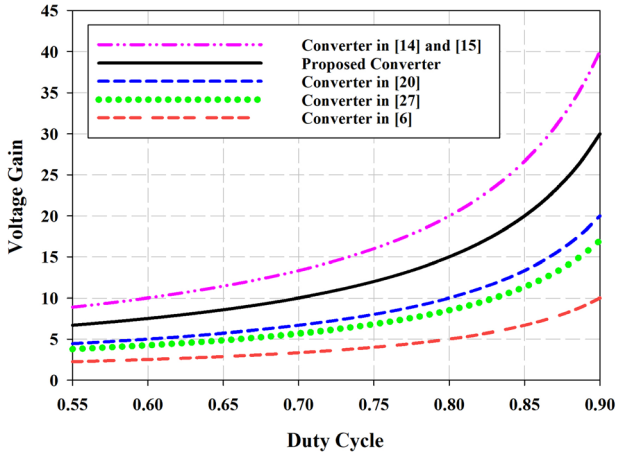

FIGURE 6 Voltage gain comparison of the proposed converter with other converters in [6, 14, 15, 20, 27] ($n = 1$ and $k = 1$)

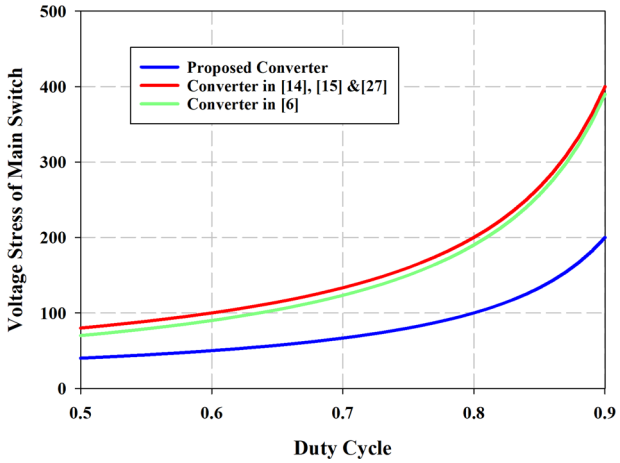

FIGURE 7 Voltage stress of the main switch in the proposed converter compared with converters in [6, 14, 15, 27]

proposed converter has a lower voltage gain than the converters in [14, 15], it has lower components in comparison to its counterparts.

Figure 7 illustrates the voltage stress curve of the main switches versus the duty cycle. With $n = 1$, the voltage stress across the main switches is one-sixth of the output voltage which is very low. In the proposed converter, the voltage stress of the main switches is halved in comparison to converters in [6, 14, 15, 27]. This allows using low voltage power switches with small on-resistance that reduces conduction losses.

In Figure 8 the main switches' voltage stress is plotted versus the voltage gain, and also it is compared with that of converters in [6, 14, 15, 20, 27]. As can be shown, even in higher voltage conversion ratios, the voltage stress across the power switches of the proposed converter is lower than the compared converters. This lets using low-voltage low-priced MOSFETs with small on-resistance that reduce conduction losses and the overall circuit price.

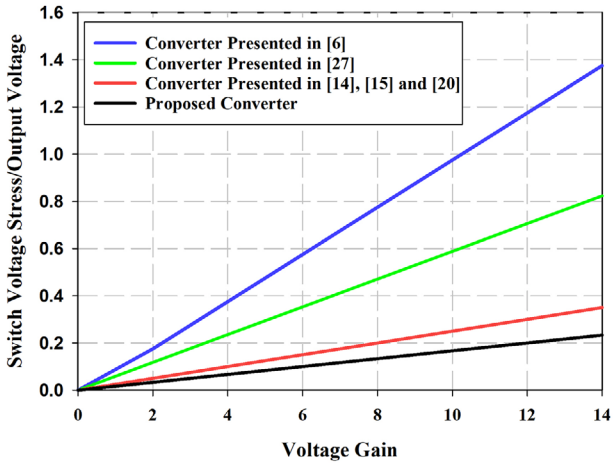

FIGURE 8 Voltage stress of the switch versus the voltage gain of the proposed converter compared with other converters in [6, 14, 15, 20, 27] ($n = 1$ and $k = 1$)

3.2 | Voltage stress of the semiconductor elements

As a result of utilizing a passive clamp circuit, the voltage stress of the main switches S_1 and S_2 when one of them is off (mode 3) is equal to V_C, which is using in Equation (27). This voltage stress is sufficiently low and allows us to employ high-quality MOSFETs with lower on-resistance to reduce conduction losses in the circuit.

By considering the circuit in mode 5, the voltage stress of switches S_1 and S_2, as well as diodes D_2 and D_4, is achieved as follows.

$$V_{S1,2} = V_{D2} = V_C = \frac{V_{in}}{2(1-D)} = \frac{V_O}{2(nK+2)} \tag{30}$$

Similarly, by doing the KVL and substituting Equation (29) in it, one can calculate the voltage stress of D_4 as:

$$\begin{aligned} -V_C + V_{D4} + \frac{V_O}{2} &= 0 \\ V_{D4} = \frac{V_{in}(nK+1)}{2(1-D)} &= \frac{V_O(nK+1)}{2(nK+2)} \end{aligned} \tag{31}$$

Since the circuit is symmetrical, the voltage stress of diodes D_1 and D_5 are the same as Equations (30) and (31) respectively.

Considering mode 4, the voltage stress of diodes D_3 and D_6 are the same and equal to:

$$V_{D3} = V_{D6} = \frac{V_O}{2} - \frac{V_{in}}{2(1-D)} \tag{32}$$

For the axillary switch S_A, we have:

$$V_{SA} = \frac{V_O(n_A - 1 + 2D)}{2(nK+2)n_A} \tag{33}$$

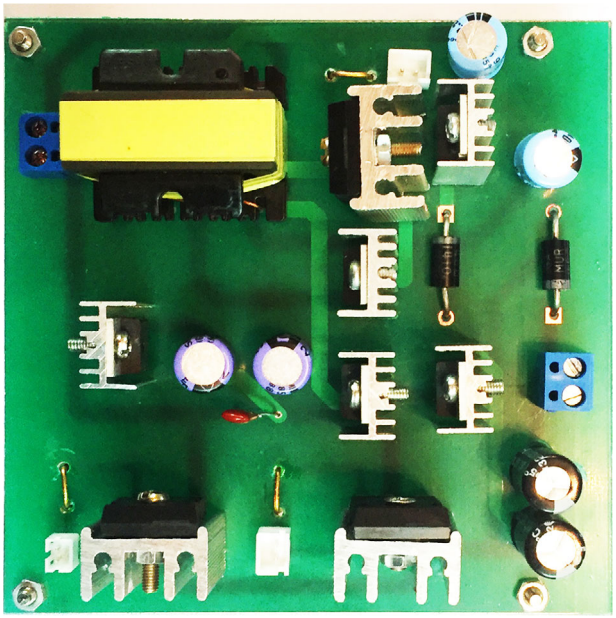

FIGURE 9 Prototype of the implemented circuit

3.3 | Design of magnetic inductance

The magnetizing inductance can be calculated as below.

The voltage across L_m is:

$$V = L\frac{\Delta I}{\Delta t} \tag{34}$$

In which the conduction time is:

$$ton = \frac{(2D-1)}{2}\,T \tag{35}$$

V_{in} is applied across L_m, so:

$$L = \frac{V_{in} * (2D-1)}{2\,\Delta I.f} \tag{36}$$

Therefore, $V_C = V_{C1} = V_{C2} = \frac{1}{2(1-D)}\,V_{in}$, the above equation can be rearranged as below:

$$L = \frac{(V_{in-Vc2}) * (1-D)}{2\Delta I.f} \tag{37}$$

3.4 | Design of capacitors

In this section, the design equations for the capacitors are provided. The output capacitors, clamp capacitors and the multiplier capacitors can be designed by considering the desired ripple voltage as following.

$$C_{o1} = C_{o2} = \frac{\left(D-\frac{1}{2}\right) I_o}{f * \Delta V_o} \tag{38}$$

$$C_1 = C_2 = \frac{\Delta t_4 (I_{Lm} + (n+1)\, I_{L2})}{f\,(n+1) * \Delta V_o} \tag{39}$$

$$C_3 = C_4 = \frac{(1-D)\, I_{Lm}}{f\,(n+1) * \Delta V_o} \tag{40}$$

Where Δt_4 is achieved by Equation (11). Also, the snubber capacitors are obtained by Equation (41).

$$C_{s1}, C_{s2} > \frac{i_{sw} * t_f}{2V_{sw}} \tag{41}$$

Where V_{sw}, i_{sw}, t_r, and t_f are the maximum switch voltage and current and the switch current rise and fall times, respectively.

3.5 | Performance comparison

The proposed converter is compared with other high step-up counterparts and the results are reported in Table 1. Converters in [8, 9] need only one magnetic core and have the lowest component count. However, they suffer from higher switch voltage stress, severe reverse recovery losses, and hard switching performance. The active clamp converters in [20–23] are load-dependent and cannot provide soft-switching condition at specific light loads. Also, although the converter in [20] has a low number of diodes and use only one magnetic core, it suffers from low voltage gain, high switch voltage stress, and does not provide soft-switching condition at light loads. As can be seen, most of the compared converters utilize more than one magnetic core, especially converters in [6, 14–16, 18, 21, 22] that need three or more. In contrast, the proposed converter employs only one magnetic element, which is an important feature for the proposed converter. From the component count point of view, the proposed converter needs relatively fewer elements, however, converters [14, 15, 18] utilize a large number of components and have a complex structure. Also, converters [6, 10, 20] are made up of fewer elements, but their voltage gain is low, and [6] suffers from a very high switch voltage stress and reverse recovery losses. Looking at the switch voltage stress, it can be seen that the proposed converter endures the lowest voltage stress across its switches, while, converters [6, 8, 9, 13, 16] face a considerably high switch voltage stress. With a closer look at [10], though it has a fewer number of elements and a switch voltage stress equal to the proposed converter, it requires two magnetic cores, has a very low voltage gain, and suffers from reverse recovery losses. In terms of the converter cost, it can be observed that the proposed converter is cheaper than its counterparts. Although the converters in [10, 20–22] are cheaper than the proposed converter, they all have a lower voltage gain than the proposed converter. In addition, the converters in [20–22] endure a higher voltage stress across their power switches and the reverse recovery losses is major in

TABLE 1 Comparison of the proposed converter with other high step-up DC–DC converters

Topology	Soft switching cell	Voltage gain	Switch voltage stress	Voltage stress ($n = 1$, $D = 0.7$, $V_O = 400$)	Number of components						V_{DO}/V_o	Input current	No R.R*	Cost ($)
					MOS*	D*	Cap*	Win*	Core	Total				
Ref. [8]	Hard switching	$\frac{1}{1-D_1+D_2}$	$\frac{V_o}{2}$	200	4	8	2	1	1	16	1	C*	✗	39.41
Ref. [9]		$\frac{2(1+nD)}{1-D}$	$\frac{V_o}{2}$	200	2	4	2	2	1	11	$\frac{1}{2}$	D*	✗	36.24
PCWZ*		$\frac{2+n}{1-D}$	$\frac{V_o}{2(n+2)}$	66.6	2	6	6	3	1	18	$\frac{1}{2}$	D	✓	15.84
Ref. [16]	Lossless Snubber-ZCS (on) (LI*)	$\frac{2n_m}{(1-D)}^1$	$\frac{V_o}{2n_m}$	200 n_m	2	$5+2n_m$	$2+2n_m$	4	4	$11+4n_m$	—	C	✗	26.84
Ref. [17]		$\frac{2n+2}{1-D}$	$\frac{V_o}{2n+2}$	100	2	8	5	6	2	23	$\frac{1}{2}$	D	✓	28.08
Ref. [18]		$\frac{2n_2(1+n_1)+1}{3n_2(1+n_1)+2}$	$\frac{V_o}{3n_2(1+n_1)+2}$	–	2	8	7	7	3	27	$\frac{2n_2(1+n_1)+1}{(1+n_1)+2}$	D	✓	39
Ref. [19]		$\frac{2+nD}{1-D}$	$\frac{V_o}{2+nD}$	148	2	8	5	4	2	21	1	D	✗	28.84
Ref. [20]	Active clamp (LD*)	$\frac{1+n}{1-D}$	$\frac{V_o}{2(1+n)}$	100	3	4	8	3	1	19	$\frac{1}{2}$	D	✓	17.73
Ref. [21]		$\frac{n(1+D)}{1-D}$	$\frac{V_o}{n(1+D)}$	235	3	7	7	5	3	25	$\frac{1}{2}$	D	✗	17.62
Ref. [22]		$\frac{2}{1-D}$	V_o	400	3	6	4	4	4	23	1	C	✓	18.14
Ref. [23]		$\frac{2(n+1)}{1-D}$	$\frac{V_o}{2(1+n)}$	80	4	4	5	5	3	21	1	C	✓	37.64
Ref. [6]	ZVT (LI*)	$\frac{1}{1-D}$	$V_o - V_{Ca}$	390	3	4	4	4	3	18	1	C	✗	28
Ref. [10]		$\frac{1}{1-D}$	$\frac{V_o}{2(n+2)}$	66.6	4	6	2	2	2	14	$\frac{1}{2}$	C	✗	14.5
Ref. [13]		$\frac{2n+1}{1-D}$	V_o	400	4	8	7	4	2	25	$(1+\frac{2(1-D)}{2n+1})$	D	✗	42.31
Ref. [14]		$\frac{1+3n}{(1-D)}$	$\frac{V_o}{1+3n}$	100	3	10	6	8	3	30	—	D	✓	29.31
Ref. [15]		$\frac{2(1+n)}{1-D}$	$\frac{V_o}{2(1+n)}$	100	4	6	7	8	4	29	$\frac{(1+2n)}{2(1+n)}$	D	✓	36.5
Proposed		$\frac{2+n}{1-D}$	$\frac{V_o}{2(n+2)}$	66.6	3	7	6	4	1	21	$\frac{1}{2}$	D	✓	20.29

MOS, MOSFET; D, Diode; Cap, Capacitor; Win, Winding, LD, Load-dependent, LI, Load-independent, RR, Reverse recovery, C, Continuous, D, Discontinuous, PCWZ*, Proposed converter without ZVT.

[21]. It should be mentioned that the power switches, especially the high-voltage ones, are of the pricier elements in power converters, hence, converters with higher number of power switches are usually more expensive, as can be seen in [8, 13, 23]. In terms of the input current, the ZVT converters in [13–15] as well as the proposed converter have discontinued input current unlike the converters in [6, 10] which increases the size of the input filter. Although converters in [6, 10] benefit from continues input current, their voltage gain is equal to the boost converter. To sum up, although some counterparts have higher voltage gain or fewer elements, the proposed converter has established a reasonable compromise between the desired parameters. Using only one magnetic core, a simple soft-switching scheme with the least number of components, a wide range of soft-switching performance, ultra-low switch voltage stress, reduced reverse recovery losses, and high voltage gain are the remarkable advantages of the proposed converter. More importantly, because of the three-level structure and minimized voltage stress across the circuit elements, low-priced low-voltage power switches, diodes, and capacitors are employed in the proposed converter which makes it a cost-effective option for high voltage gain applications. Also, reducing the number of power switches, magnetic cores, and windings helps to cut the price and size. The proposed converter is amongst the ones that use the highest number of diodes, but it should be noted that only two of these diodes, D_4 and D_5, are in the main power path. In addition, compared with power switches, the cost of diodes is much cheaper because the average current of diodes is very low. All these advantages make the proposed converter a suitable option for applications that need a high voltage conversion ratio and high efficiency like PV panels and fuel cells.

3.6 | Control circuit performance

The control circuit which is shown in Figure 12 is composed of four main sections. The first section is a feedback isolator which is implemented by isolating the output voltage via TL431 and an optocoupler. The second one is a pulse width modulation (PWM) controller that adjusts the duty cycle according to the output voltage based on traditional voltage control. This stage is implemented using a PWM controller (SG3527 IC) and produces two pulses with 180 degrees phase shift. The fourth stage is a monostable IC with the pulse delay circuit to produce the gate-source voltage of the auxiliary switch with

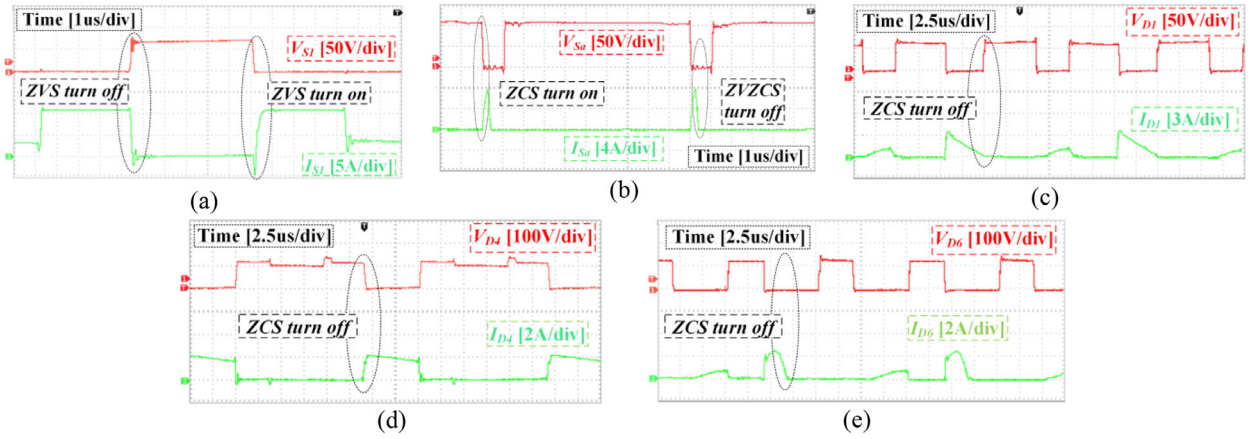

FIGURE 10 Experimental waveforms of the implemented prototype at full load. (a) Main switch S_1 (b) auxiliary switch S_a (c) diode D_1 (d) diode D_4 (e) diode D_6

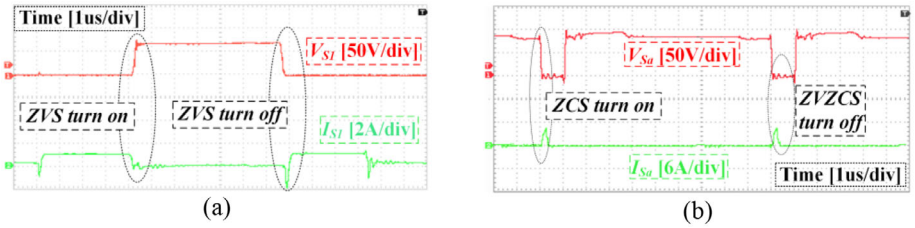

FIGURE 11 Experimental waveforms of the switches at light loads. (a) Main switch S_1 (b) auxiliary switch S_a

the desired duty cycle and delay. According to the operating principles, before turning each of the main switches on, the auxiliary switch should be turned on with an appropriate time delay and duty cycle. The gate-source voltage of the switches is applied by a gate-driver circuit with isolation and amplification.

4 | EXPERIMENTAL RESULTS

To validate the performance of the proposed converter, a laboratory prototype with input voltage 40 V, the output voltage of 400 V, and rated power 200 W has been implemented. Figure 9 and Table 2 provide the photograph and important parameters of the implemented prototype, respectively. Experimental results of the proposed converter are illustrated in Figure 10. Current and voltage waveforms of the main and auxiliary switches in light load are shown in Figure 11b. As can be seen in Figure 10, the drain-source voltage of S_1 is about 70 V which is less than a quarter of the output voltage. It allows choosing low-voltage switches with small on-resistance that leads to efficiency improvement. Moreover, at the turn-on instant of S_1, the switch current i_{ds1} is negative which shows ZVS performance of S_1 that removes switching losses. Also, ZVS turn-off of S_1 can

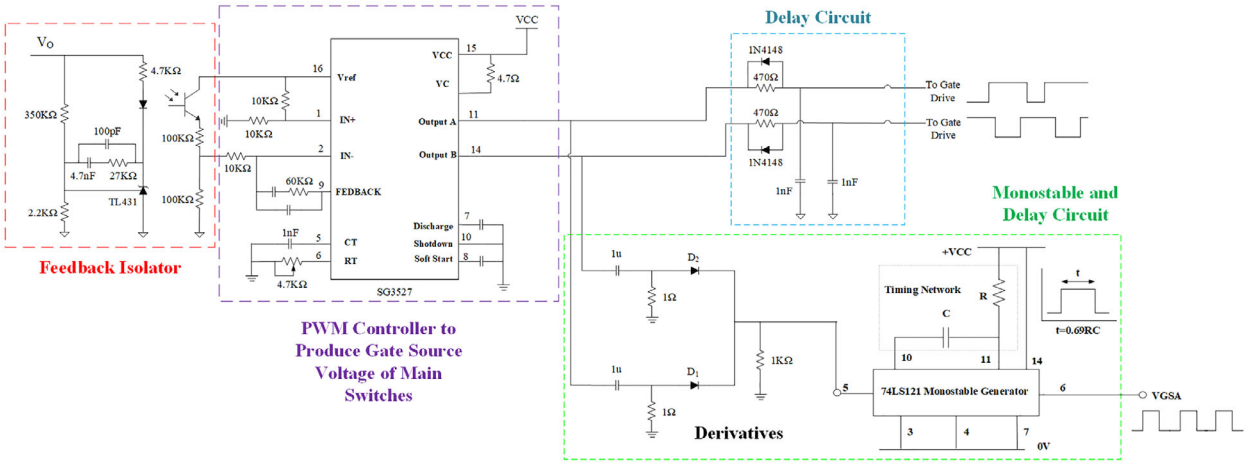

FIGURE 12 Experimental Control circuit of the proposed converter

TABLE 2 Parameters of the implemented prototype

Parameter	value
Input voltage V_{in}	40 V
Output voltage V_o	400 V
Output power P_o	200 W
Switching frequency f_s	50 kHz
Main switches S_1 and S_2	IRF3710
Auxiliary switch S_A	IRF3710
Diodes D_1, D_2, D_3, D_6 and D_A	BYV32
Diodes D_4 and D_5	MUR460
Magnetizing inductance L_m	200 μH
Primary-side leakage inductance L_{lk1}	3 μH
Turns ratios of n_2/n_1 and n_3/n_1	1
Turns ratios of n_A/n_1	0.4
Clamp capacitors C_1 and C_2	4.7 μF/100 V
Snubber capacitors C_{s1} and C_{s2}	2 nF/100 V
Switched capacitors C_3 and C_4	4.7 μF/250 V
Output capacitors C_{O1} and C_{O2}	22 μF/250 V

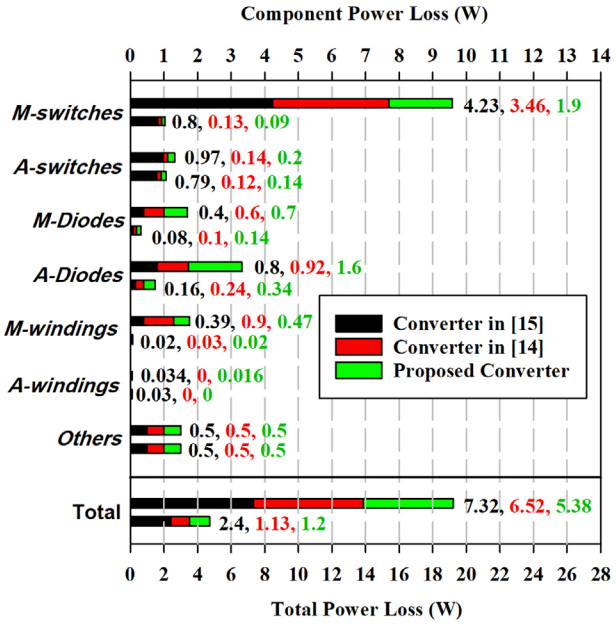

FIGURE 13 Loss distribution of the proposed converter in comparison with converters in [14, 15] at full-load (first rows) and light-load (second rows)

be observed which is due to Cs_1. S_2 has an identical condition as S_1. As shown in Figure 10, the maximum voltage across S_a is about 90 V which is much lower than the 400 V output voltage. Besides, as it is observed in Figure 10, S_a turns on under ZCS because of the series leakage inductance and turns off under ZVZCS condition. The voltage and current waveforms of D_1 is shown in Figure 10. The maximum reverse voltage across D_1 is about 120 V. As can be seen through i_{D1}, D_1 turns on and off under ZCS condition. In Figure 10, the maximum voltage across D_3 is about 50 V which is much lower than the output voltage. The ZCS turn-on and turn-off performance of D_3 can be observed in this figure. The current and voltage waveforms of D_4 can be observed in Figure 10. The maximum voltage across D_4 is about 140 V and D_4 turns on and off in a ZCS manner. As it is observed, all diodes endure low voltage stress and have ZCS turn-off performance. These two factors both help decrease their associated reverse recovery losses dramatically and improve efficiency. The low voltage stress across diodes also makes it able to choose low-voltage high-quality diodes with lower recovery times. As illustrated, not only the voltage stress of the switches is limited, but also their operation is under zero voltage condition. To show the soft-switching operation of the converter at light loads, the voltage and current of switches at 40 W output power are illustrated in Figure 11. Just like the full-load condition, the soft-switching is achieved for all switches at light loads. Since the operation of switch S_2 is the same as S_1, it is not shown in the figures.

The circuit components are analysed separately in terms of power loss at both full load and light load (%20 of the nominal load) condition for the proposed converter and converters in [14, 15] (Figure 13). Only the important components including the power switches, diodes, and inductors are considered and the rest of the losses associated with the gate driver and capacitors are aggregated in the chart bar named "Others". A-Diodes for the proposed converter stands for Auxiliary diodes which are D_1, D_2, D_3, D_6, and D_A, and M-Diodes denote the main diodes which are D_4 and D_5. As Figure 13 shows, the conduction losses of the main switches and diodes have the highest share of total losses. Besides, though there are seven diodes used in the proposed converter, only two of them, D_4, and D_5, are within the main power path, and as the chart shows, the total power dissipations of all the auxiliary diodes are a little higher than the main diodes. The main advantage of the proposed converter is that the voltage stress of the switches is half of the other converters in [14, 15], which results in lower conduction losses and higher total efficiency. In Table 3 the conduction losses of components in the nominal load are calculated. As expected, the conduction losses of the main switches are dominant, and apart from the main switches, more power is dissipated by the main diodes D_4 and D_5 than the other elements. It should also be noted that the reason for the difference between S_A loss values reported in Figure 13 and Table 3 is that E_{oss} loss associated with S_A is not calculated in Table 3 and it is included in power loss analysis reported in Figure 13.

The efficiency of the proposed converter shown in Figure 14 is achieved using PSpice simulation software along with the experimental measurement and is compared to some of its counterparts. Note that, *IRF3710* (V_{DS} = 100 V, $R_{ds(on)}$ = 23 mΩ) is utilized for the main and the auxiliary switch of the proposed converter. Also, for switches of converters in [14, 15], *IRL640A* (V_{DS} = 200 V, $R_{ds(on)}$ = 180 mΩ) is used, due to having higher voltage stress. The results are illustrated in Figure 14. As can be seen the proposed converter has the highest full-load efficiency which is %97.4 for the simulation and %97.2 for the experimental measurement at 200 W output

TABLE 3 Conduction losses of the components used in the proposed converter

Component	Resistance [Ω]	RMS current [A]	Power loss [W]
Main switches $S_{1,2}$	0.023	6.44	2×0.95
Auxiliary switch S_A	0.023	1.29	0.038
Inductor L_A	0.01	1.29	0.016
Inductor L_1	0.012	5.6	0.37
Inductors L_2 and L_3	0.024	1.38	2×0.045
Component	**Voltage drop [V]**	**Average current [A]**	**Power loss [W]**
Diode $D_{1,2}$	0.71	0.5	2×0.35
Diode $D_{3,6}$	0.71	0.5	2×0.35
Diode $D_{4,5}$	0.71	0.5	2×0.35
Diode D_A	0.71	0.3	0.21
Total			4.7

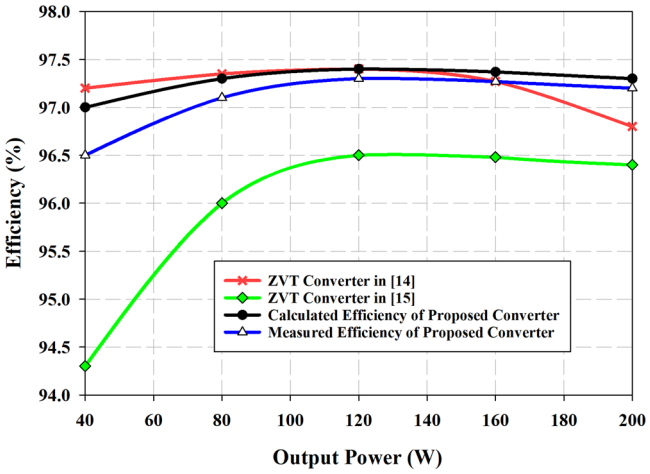

FIGURE 14 Efficiency of the proposed converter in comparison with other converters in [14, 15]

power. In addition, there is no considerable efficiency drop at light loads thanks to its ZVT soft-switching circuit, which are %97 and %96.5 for the simulation and experimental measurements, respectively. Although the converter presented in [14] has also a high efficiency at a wide range of output loads, its efficiency is lower than the proposed converter at full loads due to higher conduction loss of the main switches and large number of semiconductor elements. The converter in [15] not only have a remarkably lower full-load efficiency but also its efficiency dramatically drops at light loads. Another disadvantage of the converter in [15] is that it needs two auxiliary power MOSFET to achieve soft switching which more degrades the efficiency.

5 | CONCLUSION

Here, a new single-core soft-switching high step-up three-level converter with a passive clamp circuit was introduced. All semiconductor elements have soft switching performance. The voltage stress across the main switches S_1 and S_2 along with the auxiliary switch S_A is less than a quarter of 400 V output voltage. The proposed circuit topology is suitable for high step-up applications and has some advantages such as reduced size because of using only one magnetic core, high efficiency as a result of utilizing soft-switching techniques, low voltage stresses across the semiconductor elements, absorption and recycling of leakage inductance energy, and low conduction loss since three-level structure enables using MOSFETs with low drain-to-source on-resistance. The coupled inductors and switched capacitors are integrated to achieve high step-up voltage gain. The secondary and tertiary leakage inductances of the coupled inductors also reduce the reverse recovery problem of the output diodes which improves the circuit performance.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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