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# BPF-Based Thermal Sensor Circuit for On-Chip Testing of RF Circuits

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**Abstract:** A new sensor topology meant to extract figures of merit of radio-frequency analog integrated circuits (RF-ICs) was experimentally validated. Implemented in a standard 0.35 µm complementary metal-oxide-semiconductor (CMOS) technology, it comprised two blocks: a single metal-oxide-semiconductor (MOS) transistor acting as temperature transducer, which was placed near the circuit to monitor, and an active band-pass filter amplifier. For validation purposes, the temperature sensor was integrated with a tuned radio-frequency power amplifier (420 MHz) and MOS transistors acting as controllable dissipating devices. First, using the MOS dissipating devices, the performance and limitations of the different blocks that constitute the temperature sensor were characterized. Second, by using the heterodyne technique (applying two nearby tones) to the power amplifier (PA) and connecting the sensor output voltage to a low-cost AC voltmeter, the PA's output power and its central frequency were monitored. As a result, this topology resulted in a low-cost approach, with high linearity and sensitivity, for RF-IC testing and variability monitoring.

**Keywords:** CMOS thermal sensor; CMOS built-in sensor; CMOS integrated circuits; measurement of RF CMOS circuits; built-in test and measurement



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## 1. Introduction

The temperature in a surface point of an integrated circuit (IC) depends on the power dissipated by the devices placed nearby (so-called self-heating and thermal coupling), the structure and materials that constitute the packaging (which determine the thermal impedances of the different devices) and the ambient temperature [1]. Traditionally, off-chip temperature measurement set-ups have been used to detect unexpected hot spots within digital circuits [2–5]. Hot spots might appear either due to the presence of a defect in the circuit structure [6–9] or by a nonuniform power dissipation on the die surface, which is a common situation in microprocessors [4,10]. In complex digital systems, such as microprocessors, temperature sensors are built-in within the same silicon die in order to ensure reliable system performance, i.e., they perform power-temperature monitoring to control the activation of cooling systems, to modulate microprocessor supply voltage or clock frequency, or to assert if the workload of a specific microprocessor block can be increased or should be reduced to avoid nonuniform power distributions [11–18]. Nevertheless, thermal monitoring is not restricted to digital circuits, but used as well in analog circuits. Most commonly, thermal measurements of analog circuits are usually performed to extract the thermal resistance of devices [19,20], especially in power devices. More recently, temperature measurements are done in high frequency analog circuits to perform testing applications. The test of high frequency analog circuits is a challenging task, as the presence of a defect or the effects of process-voltage-temperature variations

and device aging, does not usually produce a catastrophic circuit failure, but a degradation of circuit performance and specifications [21–25], which compromises yield. A strategy to compensate these performance degradations is to build in monitor circuits with the analog circuit (called hereafter the circuit under test (CUT)) to track variations in their performance [26–30] and, in the eventual case of detecting a circuit degradation, to activate a feedback in the CUT bias to compensate for them. Recently, several studies have proved that by measuring the temperature in a surface point near the CUT, it is feasible to monitor the performances of radio frequency (RF) and millimeter wave (mmW) circuits [30–37] or the presence of structural defects [38,39]. The use of built-in temperature sensors to monitor high-frequency analog circuits is attractive. On the one hand, the sensor does not load any node of the CUT, avoiding the need of a CUT-sensor codesign. On the other hand, thanks to the Joule effect, there is a frequency down-conversion of the high-frequency information in the electrical domain to low frequency in the thermal domain in such a way that the same temperature sensor can be used to monitor different CUTs working at different frequency bands.

In this scenario, the goal of temperature measurements is to get solely a signature of the power dissipated by the CUT, as this power carries information of the high frequency electrical signals while rejecting any temperature variation due to changes in the ambient temperature or the case-to-ambient thermal resistance (e.g., the activation of a cooling system). To this end, one strategy is the use of differential temperature sensors embedded in the same silicon die [37–41]. Such sensors possess two sensing devices (temperature transducers T1 and T2). Whereas T1 is placed close to the CUT, T2 is placed far from it. This placement ensures that only T1 measures the temperature changes caused by the power dissipation of the CUT, but both T1 and T2 detect common-mode temperature changes, being eventually rejected. Generally, the two sensing devices form the differential pair of an operational transconductance amplifier (OTA), which operates in open-loop to have a high sensitivity [38–40]. Although these sensors have been proved useful to perform the test of analog high-frequency CUTs, they have several limitations. Firstly, the OTA output can be easily saturated by mismatches produced because of manufacturing variability and the DC temperature gradients generated by the DC CUT bias [36,38]. Secondly, since the OTA operates in open loop, the gain (and hence the sensitivity to temperature) is quite sensitive to integrated circuit (IC) manufacturing process variations [37]. Thirdly, mismatches, circuit topology and device limitations reduce the rejection to common mode temperature changes.

These limitations have motivated the design of a novel circuit topology that we presented in [42] (Figure 1). One sensing device ($T_1$ placed near the CUT) is connected to an active band-pass filter (BPF). The filter's band-pass is centered at $\Delta f$ so that the bandwidth (and hence the noise) is limited around the frequency of interest. The BPF's zero at the origin rejects slow temperature variations (provoked by either ambient temperature changes or the DC CUT power dissipation). To achieve a CUT thermal signature within the frequency band of the sensor, we propose to excite the CUT with a heterodyne technique [41,43]. The technique consists of applying two tones, whose frequencies are $f_1$ and $f_2 = f_1 + \Delta f$, to the CUT input. This driving strategy generates a spectral component of power dissipated by the CUT devices (and hence of temperature) at $\Delta f$, whose magnitude depends on the CUT figures of merit at $f_1$. For $\Delta f$ values higher than a certain threshold (fixed by both the die thickness and semiconductor thermal properties [40]), the amplitude of this temperature component is no longer dependent on the package materials and package mounting thermal properties, i.e., the silicon die is seen by the CUT, from a thermal point of view, as a semi-infinite medium, independent of the thermal boundary conditions (including ambient temperature). This heterodyne technique is not new: it has been already used with differential temperature sensors connecting the sensor's output node to a lock-in amplifier (LIA) locked at $\Delta f$ [33,35]. To reduce costs, the BPF output signal is proposed to be measured using a low-cost digital multimeter (DMM), off-chip in this work, but that allows an easier integration than the LIA if a complete built-in test approach is required.

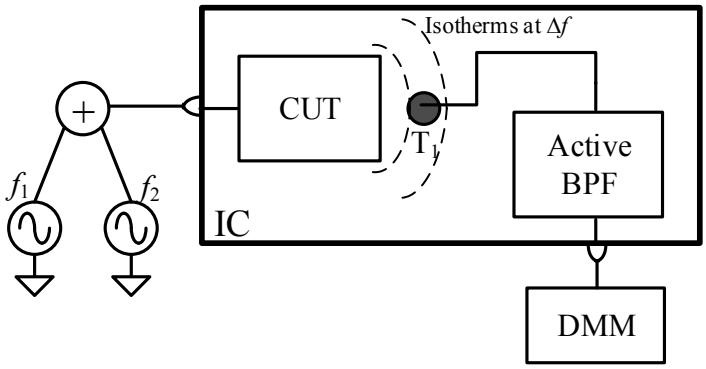


**Figure 1.** Circuit under test (CUT) with heterodyne driving. Temperature sensor made of a single metal -oxide semiconductor (MOS), transistor temperature transducer ($T_1$), an active Band Pass Filter (BPF), and a Digital Multimeter (DMM). Temperature variations at $\Delta f$ carry information about the CUT figures of merit at $f_1$.

The main novelty and first goal of this paper is to present the first experimental characterization of this sensor topology, focusing on its sensitivity, noise and linearity. To this end, we implemented a realization of this sensor topology in a standard 0.35 µm CMOS technology (VDD = 3.3 V) together with MOS transistors acting as controllable dissipating devices. The second goal is to assess the temperature sensor for RF CUT monitoring. For that purpose, a tuned (420 MHz) class-A radio-frequency power amplifier (PA) is built-in together with the sensor, which shows its capability to monitor the PA central frequency and the output power delivered to the load (antenna).

Taking this into account, the paper is organized as follows: the sensor topology and design are described in Section 2. The sensor's block characterization and full sensor validation are carried out in Section 3. Section 4 presents the PA used as CUT, the placement of the transducer within the PA layout and two application cases for this temperature sensor as a built-in RF monitor. Finally, Section 5 draws the main conclusions.

## 2. Sensor Description and Design

Figure 2 shows the proposed sensor schematic. It was made of two blocks: (a) the temperature transducer and (b) the active BPF. The goal of the temperature transducer is to generate a voltage at the node $V_{ot}$ proportional to the working temperature of the transistor $T_1$, which is placed in the silicon die at the proximity of the CUT. On the other hand, the aim of the active BPF is to provide signal amplification at the output node $V_o$ if the input signal $V_{if}$ has its frequency within the passing band. The main figures of merit of the BPF frequency response are represented in Figure 2c: the low-frequency ($f_{p1}$) and high-frequency ($f_{p2}$) poles, which determine the pass-band, and the band-pass gain $A_v$. Three different circuits were implemented in the IC: only (a) with $V_{ot}$ connected to an output pad; only (b) with $V_{if}$ connected to an input pad and (a) and (b) with $V_{ot}$ internally shorted to $V_{if}$. A detailed description and theoretical analysis of each block is in the following two subsections, with emphasis on sensitivity, noise and linearity.

### *2.1. Temperature Transducer Description*

The temperature transducer $T_1$ was an nMOS transistor (dimensions: $W$ = 24 µm, $L$ = 1.5 µm) connected in diode configuration and biased with a DC constant current ($I_B$ in Figure 2). A small bias current placed the transistor in the weak inversion region, having an expected sensitivity of −1.5 mV/K at $I_B$ = 20 nA. With other dimensions and bias, transducer sensitivities in the range [−1.6 mV/K, 5 mV/K] can be achieved, as reported in [44,45]. To create such a small bias current, a current mirror with a ratio $I_B/I_{ext}$ = 1/1000 was implemented. The internal current mirror in conjunction with an operational amplifier (OA) in voltage follower configuration ensures a low parasitic capacitance at node $N_1$ and a low output impedance, enhancing the dynamic transducer behavior.

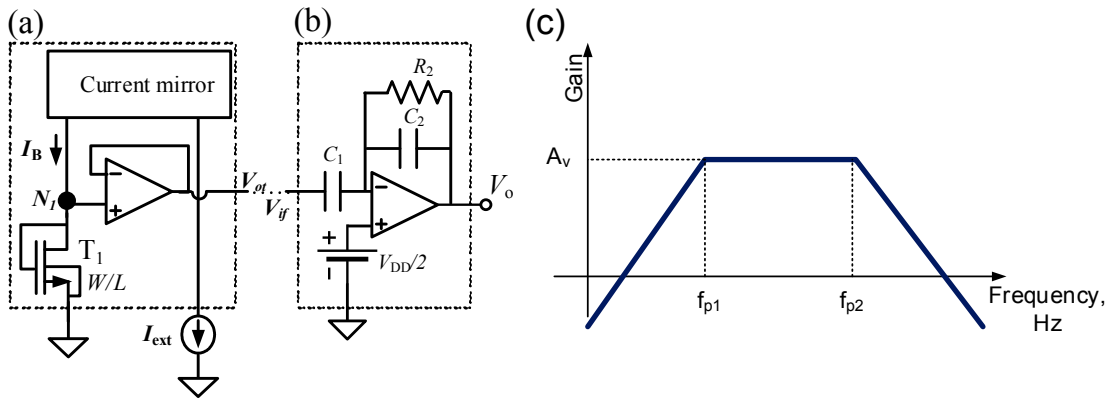


**Figure 2.** Temperature sensor schematic. (**a**) Temperature transducer based on an nMOS transistor ($T_1$). (**b**) Active band pass filter (BPF). In our design: $I_{ext}$ is off-chip. (**c**) Typical BPF frequency response of the circuit in (**b**), characterized by the low-frequency ($f_{p1}$) pole, the high-frequency ($f_{p2}$) pole and the band-pass gain $A_v$.

### *2.2. Band Pass Filter Amplifier: Noise and Linearity Analysis*

The output of the temperature transducer was connected to an active BPF. The transducer signal is AC-coupled, amplified and filtered, and appeared at the output superposed on a DC level of $V_{DD}/2$. Capacitors $C_1$ = 50 pF and $C_2$ = 100 fF set the band-pass gain $A_v$ which was designed to be:

$$|A_v| \cong \frac{C_1}{C_2} = 500\ (54\ \text{dB}). \tag{1}$$

Having a zero at the origin, the pass-band is determined by the low ($f_{p1}$) and high ($f_{p2}$) poles (cut-off frequencies), which are respectively:

$$f_{p1} = \frac{1}{2 \cdot \pi \cdot R_2 C_2} \tag{2}$$

$$f_{p2} = \frac{GBW}{|A_v|} \tag{3}$$

Since the OA gain-bandwidth (GBW) product is 2.4 MHz, this results in a theoretical value for $f_{p2}$ of 4.8 kHz. To have a low $f_{p1}$, resistor values in the order of GΩ are required, thus $R_2$ was implemented with two subthreshold biased pMOS, as shown in Figure 3 [46–49]. These MOS had $W$ = 2 µm and $L$ = 10 µm, and the external voltage $V_{BIAS}$ applied to their gate allows tuning to its equivalent resistance. From Equations (1) and (3), in a first order analysis, $f_{p2}$ and $A_v$ should be independent from $V_{BIAS}$.

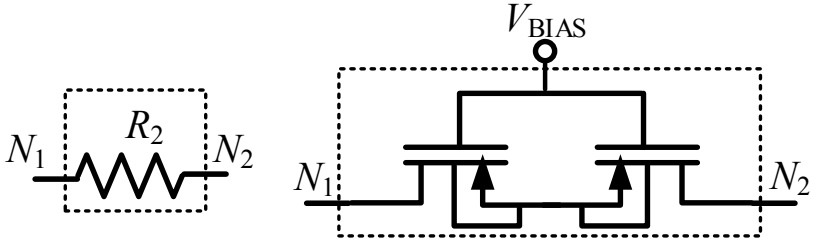


**Figure 3.** $R_2$ implemented with two pMOS transistors biased in subthreshold.

Table 1 shows the values, obtained from simulations, of the $R_2$ incremental resistance as a function of $V_{BIAS}$ (assuming both $R_2$ terminals, $N_1$ and $N_2$, at $V_{DD}/2$) as well as the BPF's low and high cut-off frequencies. Note how $f_{p1}$ is highly sensitive to $V_{BIAS}$, which opens a discussion on its optimum value. As explained above, transducer signal consisted of a tone at a frequency $\Delta f$, which should fall within the filter passband. From the values in

Table 1, $\Delta f$ around 1–2 kHz are reasonable choices. The filter output would be measured with a DMM that evaluates the total RMS voltage. Then, a narrow band-pass (high $f_{p1}$) seems desirable in order to filter out as much noise as possible and reduce the measurement noise level. But, on the other hand, the amplified signal at the output node modulates the $R_2$ value, thus producing distortion. The effect of this $R_2$ nonlinearity on the overall sensor nonlinearity is relevant whenever $R_2$ has a significant contribution to the signal path, i.e., when $\Delta f$ is around $f_{p1}$ or lower. On the contrary, at $\Delta f$ values well above $f_{p1}$, the effects of $R_2$, including its nonlinearity, become negligible on the output linearity and gain. From this point of view, a low $f_{p1}$ is desirable.

**Table 1.** Active band pass filter (BPF) simulated characteristics.

| $V_{BIAS}$ (V) | $R_2$ (GΩ) | $f_{p1}$ (Hz) | $f_{p2}$ (kHz) | $A_{v\_max}$ (dB) | Noise ($\mu V^2_{RMS}$) | $THD_{max}$ (dB) |
|---|---|---|---|---|---|---|
| 1.15 | 1.47 | 973 | 5.5 | 54.8 | 2.04 | −15.7 |
| 1.2 | 6.42 | 248 | 4.6 | 54.7 | 2.22 | −29.9 |
| 1.25 | 28.5 | 55 | 4.6 | 54.5 | 2.46 | −52.7 |

In order to assess the effect of the different $f_{p1}$ choices on the sensor noise and linearity, Table 1 shows simulation results of the filter alone (no transducer included). Noise was evaluated after integrating the power spectral density at the filter output up to 100 kHz, while the maximum harmonic distortion ($THD_{MAX}$) was also evaluated at the filter output obtained for a 1 kHz input sinusoid just before output clipping. Simulations show how linearity was dramatically degraded as $f_{p1}$ was set near the signal frequency, while could be improved as $f_{p1}$ is moved away from the signal. The price to pay was a moderate noise degradation. In view of these simulation results, $V_{BIAS}$ = 1.2 V ($f_{p1}$ = 248 Hz) was selected as a good default setting, which can be increased ($f_{p1}$ decreased) to produce a more linear response.

## 3. Sensor Implementation and Validation

The sensor was designed and manufactured in the CMOS 0.35 µm process. This microelectronic process provides four metal layers and two polysilicon layers. Capacitances $C_1$ and $C_2$ were implemented with polysilicon capacitors. The supply voltage ($V_{DD}$) was 3.3 V (unipolar), and the IC was packaged in a QFN56. Its validation was performed first by each block standing alone and finally both connected, as detailed below.

### *3.1. Temperature Transducer*

To characterize its frequency response, the circuit in Figure 2a was implemented as stand-alone, with the node $V_{ot}$ connected to an output pad. Besides, a large diode-connected nMOS transistor acting as a heater ($W$ = 450 µm, $L$ = 1 µm and 15 fingers) was placed at a 5 µm distance from the transducer (Figure 4). The heater was biased with a gate (drain) voltage, $v_{in}(t)$:

$$V_{in}(t) = V_{DCh} + A \cdot \cos(2\pi \cdot f_i \cdot t), \quad (4)$$

where $V_{DCh}$ is the heater bias voltage, $A$ is the AC amplitude, and $f_i$ is its frequency. Assuming a linear response, the current flowing through the heater is:

$$I_{in}(t) = I_{DCh} + g_m A \cdot \cos(2\pi \cdot f_i \cdot t), \quad (5)$$

where $g_m$ is the heater AC transconductance at $V_{in} = V_{DCh}$, and $I_{DCh}$ is the DC drain to source current when $V_{in} = V_{DCh}$.

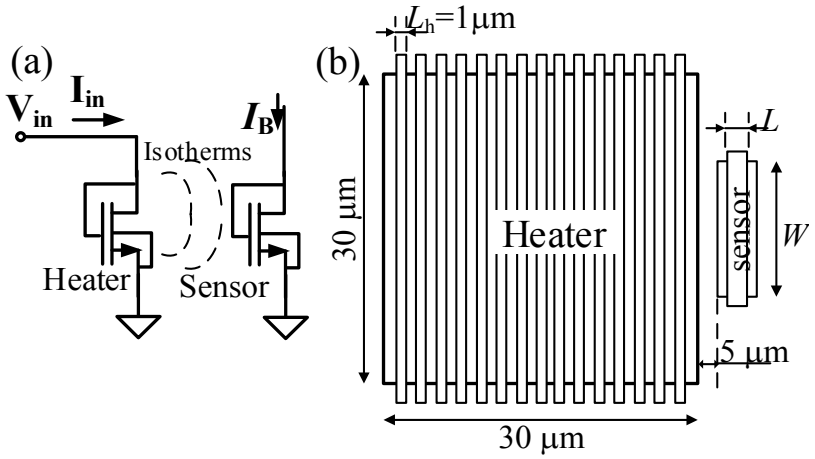


**Figure 4.** (**a**) Schematic of the nMOS heater and the temperature transducer $T_1$. (**b**) Layout floorplan.

Multiplying Equations (4) and (5), the power dissipated by the heater in the frequency domain can be described as the sum of different spectral components. If we focus on the spectral component at the frequency $f_i$ (called $p_{fi}$), it can be written as:

$$p_{fi}(t) = P_A \cdot \cos(2\pi \cdot f_i \cdot t), \tag{6}$$

where $P_A$ is the power dissipation amplitude at the frequency $f_i$. The above-mentioned heater dimensions enabled us to easily have $P_A$ in the mW range while applying a low input voltage. $p_{fi}(t)$ causes a temperature oscillation $t_S(t)$ at the temperature transducer with the same frequency $f_i$:

$$t_S(t) = T_A \cdot \cos(2\pi \cdot f_i \cdot t + \Phi_A), \tag{7}$$

where $T_A$ is the temperature amplitude and $\varphi_A$ is the phase shift between $t_s$ and $p_{fi}$. Both thermal amplitude and phase shift depend on the silicon physical properties (thermal conductivity and specific heat), the input frequency $f_i$ and the distance between the heater and the transducer [40]. The close proximity between the heater and the transducer ensures a good thermal coupling even in the MHz frequency range [32,40,50,51]. Then, the transducer output voltage can be written as:

$$V_{ot}(t) = V_{GST1} + V_A \cdot \cos(2\pi \cdot f_i \cdot t + \Phi_A), \tag{8}$$

where $V_{GST1}$ is the DC gate-to-source voltage in $T_1$, needed to sustain the drain current $I_B$, and $V_A$ is the voltage amplitude generated by the oscillating temperature of amplitude $T_A$. Here we assume that there is no phase shift between the transducer temperature and the output voltage, i.e., the pole induced by the node $N_1$ in Figure 2b is at a frequency much higher than $f_i$. Being a temperature-to-voltage transducer, its sensitivity is defined as $V_A/T_A$. However, as the goal of the sensor was to monitor the CUT characteristics through its power dissipation, the sensitivity expressed as $V_A/P_A$ had a greater interest, and will be evaluated in this work.

In order to characterize the transducer response, the heater has was excited with the different input voltage levels (VL) reported in Table 2. $P_A$ values in this table were calculated from the experimental I-V characteristics of the heater. Figure 5 shows the measured transducer sensitivity as a function of the frequency (transducer biased with $I_B$ = 20 nA). Here, the amplitude $V_A$ was measured with an LIA (Signal Recovery 7265DSP) locked at $f_i$ with a constant time of 1 s.

**Table 2.** Excitation applied to the heater.

| VL | $V_{DCh}$ (V) | $A$ ($mV_{RMS}$) | $P_A$ (mW) |
|---|---|---|---|
| 1 | 1.67 | 7.8 | 0.44 |
| 2 | 1.67 | 15 | 0.84 |
| 3 | 1.67 | 23 | 1.29 |
| 4 | 1.67 | 31 | 1.75 |

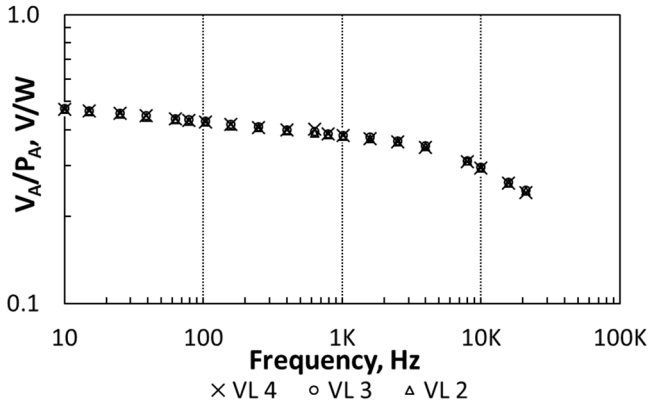


**Figure 5.** Measurements of transducer sensitivity as a function of the frequency. Three different voltage levels (VL) for the heating device are considered.

The frequency response in Figure 5 shows a low-pass behavior corresponding to the thermal coupling from the heater to the transducer, which agrees with the theoretical, simulations and experimental data previously reported in [52]. In this particular set-up, the coupling attenuation increased for frequencies higher than 3 kHz. Besides that, the independence of the transducer's sensitivity on the amplitude $P_A$ proves the transducer linear behavior.

### *3.2. Band Pass Filter Amplifier*

The circuit in Figure 2b was also implemented as stand-alone, with input ($V_{if}$) and output nodes ($V_o$) connected, respectively, to input and output pads.

Figure 6 shows the measured frequency response of the BPF voltage gain. Input $V_{if}(t)$ is a sinusoidal voltage of 20 $mV_{RMS}$ attenuated by a factor of 100 with an off-chip resistive voltage divider. Filter characterizations were done for the three $V_{BIAS}$ values reported in Table 1. For each $V_{BIAS}$, the output voltage amplitude was measured using either the LIA or a DMM (HP 33401A) AC-coupled. The LIA was set with a time constant of 1 s, which implied that the measure was integrating the signal (and noise) in a bandwidth of 1 Hz. On the other hand, the DMM was integrating the signal and noise along all the filter bandwidth (i.e., the output harmonics were integrated as well).

Table 3 summarizes the BPF characteristics extracted from the responses in Figure 6, considering LIA measurements. Comparing Tables 1 and 3, measured characteristics show a reasonable agreement to the simulation predictions.

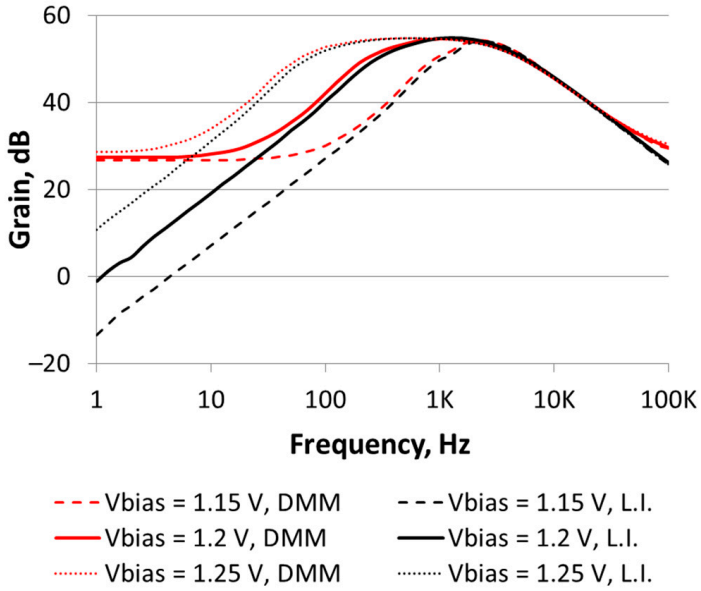


**Figure 6.** Frequency response of the amplifier BPF's voltage gain, plot for three different $V_{BIAS}$ values: 1.15, 1.2 and 1.25 V. For each $V_{BIAS}$, measurements are taken either with a digital multimeter (DMM) or with a lock-in amplifier (LIA).

**Table 3.** Active BPF measured characteristics.

| $V_{BIAS}$ (V) | $f_{p1}$ (Hz) | $f_{p2}$ (kHz) | $A_{v\_max}$ (dB) |
|---|---|---|---|
| 1.15 | 1258 | 5.1 | 54.1 |
| 1.2 | 350 | 3.9 | 54.9 |
| 1.25 | 79 | 3.9 | 54.6 |

More importantly, measurements done with a simple DMM had very good agreement with those made with the LIA for frequencies equal and higher than the BPF central frequency. However, DMM results were higher than the LIA ones when the input signal frequency was equal or smaller than $f_{p1}$. As predicted by simulations, output-voltage nonlinearities became relevant when the input frequency was equal or smaller than $f_{p1}$, due to the $R_2$ modulation. Those nonlinearities produced significant harmonics, which were captured with the DMM, thus producing a slightly higher gain measurement. Finally, DMM results showed an equivalent noise at the filter output of 4 $mV_{RMS}$, which, according to Section 2, translated into an equivalent noise at the temperature sensor's input of 7.54 mK (@ $I_B$ = 20 nA). As predicted by simulations, the noise level at the output was almost independent from $V_{BIAS}$: $f_{p1}$ may change over one order of magnitude, but its values were in the range of tens-hundreds of Hz, with small effect after integrating over the whole bandwidth.

The effects of the manufacturing variability on $R_2$ were also evaluated. Figure 7 shows the effect of $R_2$ sample-to-sample variability on the measured $f_{p1}$ values, as a function of $V_{BIAS}$ in three different IC samples. In all these situations, the maximum gain measured was 54.5 ± 0.43 dB, in agreement with the expected gain independence with $V_{BIAS}$.

### *3.3. Overall Sensor Characterization*

Besides the stand-alone temperature transducer (Figure 2a) and the stand-alone BPF (Figure 2b), the complete circuit in Figure 2 was also implemented with the transducer's output connected to the input of the BPF, and with a nMOS transistor such as that depicted in Figure 4 as a controllable heater. Then, when the dissipating device is biased with $v_{in}(t)$ as in Equation (4), the sensor's output voltage can be written as:

$$V_O(t) = \frac{V_{DD}}{2} + A_O \cdot \cos(2\pi \cdot f_i \cdot t + \Phi_O), \quad (9)$$

where $A_O$ is the amplitude of the sinusoidal component of $V_O(t)$ at the frequency $f_i$. The filter introduces a phase shift $(\varphi_O - \varphi_A) - \varphi_A$ is defined in Equations (7) and (8).

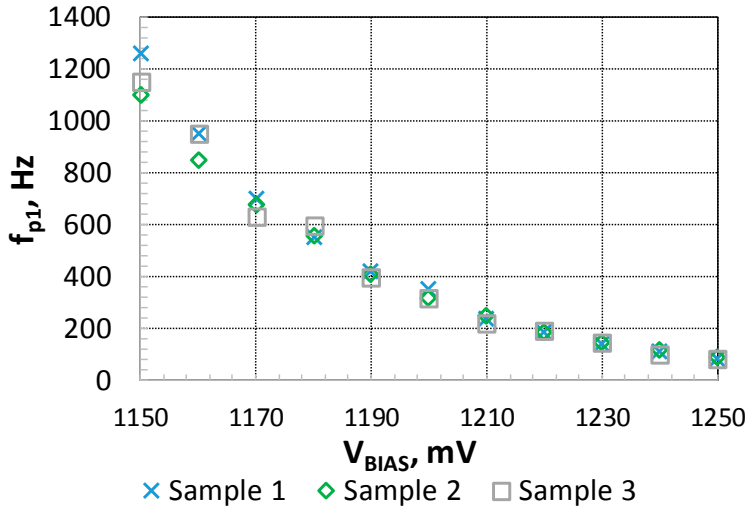


**Figure 7.** $f_{p1}$ as a function of $V_{BIAS}$. Measurements performed in three different samples.

Figure 8 shows $A_{O,RMS}$ (RMS value of $A_O$ from Equation (9)) as a function of the frequency when measured with the DMM (@ $I_B$ = 20 nA, $V_{BIAS}$ = 1.2 V), using the different VLs in Table 2 for the heater excitation. The frequency response reported a central frequency, $f_c$, of about 2 kHz for all the VL. The overall frequency response is the concatenation of the transducers' and BPF frequency responses. For frequencies smaller than 100 Hz or higher than 10 kHz (the exact frequency depends on the particular bias), the sensor's output voltage reached the noise level, which is 40 $mV_{RMS}$. This noise level is higher than that observed in Figure 6, meaning that it was dominated by the heater-transducer circuits. The noise level sets the $P_A$ threshold that the sensor is able to detect. To calculate this threshold, Figure 9 shows the sensor's sensitivity ($A_O/P_A$) as a function of the frequency, when measured with the LIA. The maximum sensitivity was about 140 mV/mW. Therefore, 40 $mV_{RMS}$ corresponded to an equivalent noise floor in $P_A$ of 285 µW.

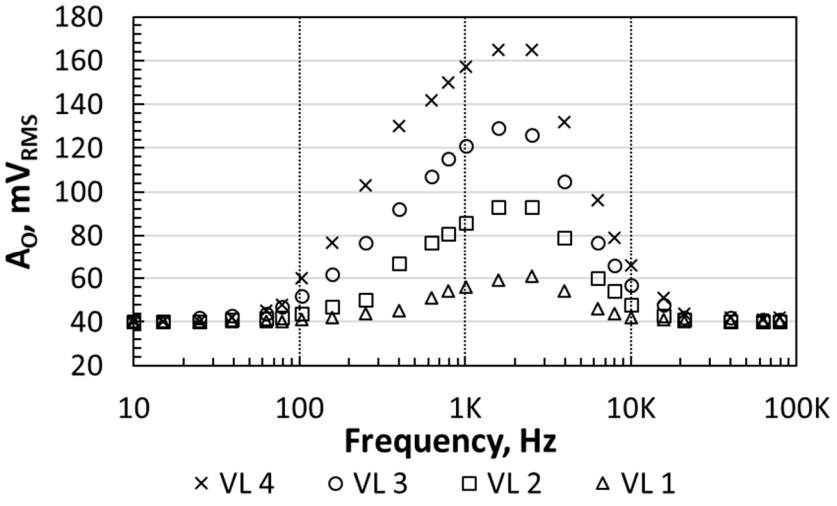


**Figure 8.** Sensor's output voltage as a function of the frequency for four different heater bias. Measurements done with the DMM.

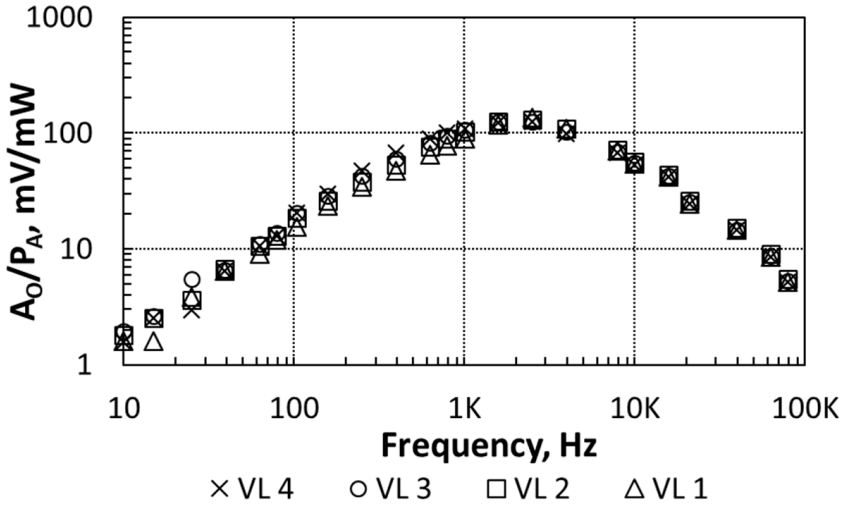


**Figure 9.** Sensor's sensitivity as a function of the frequency. See Table 2 for the VL description and the PA values. Measurements taken with the LIA.

If we now consider the sensor's linearity, the overlapping points in Figure 9 show that the sensor sensitivity was not affected by the $P_A$ level when $f_i$ was equal or higher than $f_c$. On the other hand, the sensitivity depended on the amplitude $P_A$ dissipated by the heater when $f_i$ was smaller than $f_c$: The $R_2$ nonlinear behavior affected the sensor linearity. These results have implications in the way the CUT must be driven when a test is done using a heterodyne excitation (Figure 1): $\Delta f$ should be higher than $f_{p1}$. The exact value of $\Delta f$ is determined by the expected range of values of the amplitude $P_A$ dissipated by the CUT, which determines the required sensor sensitivity and the noise level. For instance, from Figures 8 and 9, if $\Delta f$ = 2.5 kHz the sensor's sensitivity is 134 mW/mV. This sensitivity allows the sensor to detect the $P_A$ dissipated by the heater when driven by the VL 1. On the other hand, if $\Delta f$ = 10 kHz the sensor's sensitivity is 54 mW/mV, and the amplitude $P_A$ dissipated by the heater when driven by the VL 1 is below the noise level, whereas the sensor can barely detect the amplitude PA when driven by the VL 2. This indicates that $\Delta f$ higher than the sensor's central frequency can be a good choice to sense large $P_A$ levels. On the other hand, if $\Delta f = f_c$, high values of $P_A$ might drive the sensor to saturation.

## 4. Use Case: RF Tuned Class-A Power Amplifier Monitoring

### *4.1. Circuit and Experimental Set Up Description*

The BPF temperature sensor was integrated with a narrowband RF power amplifier (PA) used as a CUT. The schematic of the RF PA is shown in Figure 10. It is a class-A cascode amplifier with off-chip load, fully described in [32]. The cascode transistor $M_2$ was made of three transistors in parallel connection (inset in Figure 10). The overall $M_2$ dimensions were W = 1173 µm (implemented with 51 fingers), and L = 0.5 µm. The MOS temperature transducer was placed in the free space existing between two of these transistors. When the DC bias of the PA was $V_{DD}$ = 3.3 V and $V_{cnt}$ = 3 V, it had a current consumption of 22 mA. Experimental characterization of the PA reported a central frequency of 420 MHz, a maximum gain of 12 dB and a 1 dB compression point referred to the input of −4 dBm. To minimize parasitics in the RF measurements, the chip was directly soldered to the board (chip on board).

In order to demonstrate the sensor monitoring capability, the PA was AC driven with a heterodyne approach: two sinusoidal signals of input power $P_i$ and frequencies $(f_{RF} - \Delta f/2)$ and $(f_{RF} + \Delta f/2)$. This driving generated power dissipation in transistor $M_2$, with a spectral component at $\Delta f$ and an amplitude $P_{\Delta f}$. Previous work [32,33] indicated that $P_{\Delta f}$ depended on both the voltage gain of the amplifier at $f_{RF}$ and on the input-output matching at the same frequency. As elaborated in Section 3, this power dissipation

generated an AC sensor output voltage superimposed to $V_{DD}/2$, whose content at $\Delta f$ can be written as:

$$v_O(t) = A_O \cdot \cos(2\pi \cdot f_i \cdot t + \Phi_O). \quad (10)$$

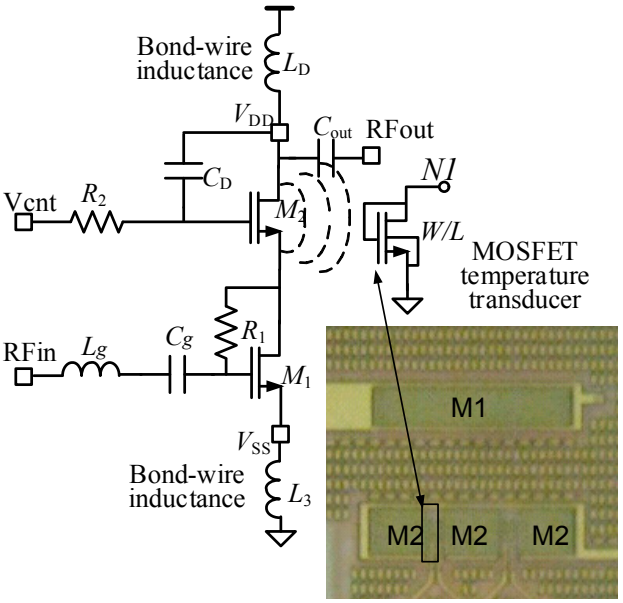


**Figure 10.** Schematic of the RF power amplifier used as CUT. The temperature transducer is placed close the cascode transistor M2. Inset shows a photo of the IC layout, with the placement of the active transistor M1, cascode transistor M2 (formed with three equal transistors connected in parallel), and the MOS acting as temperature transducer.

### *4.2. Output Power Monitoring*

Figure 11 shows the sensor's output voltage amplitude $A_O$ as a function of the total output power delivered by the PA to a 50 Ω load. The temperature transducer was biased with a current $I_B$ = 20 nA and the sensor's filter with $V_{BIAS}$ = 1.2 V. The PA was driven with two tones with $f_{RF}$ = 420 MHz (its central frequency) and $\Delta f$ = 1 kHz. $P_i$ was swept to get a total output power delivered to the load ranging from −40 dBm to 0 dBm. This output power range was below the 1 dB compression point, ensuring constant PA gain for all the cases. The PA output power was measured with the Agilent E4443A spectrum analyzer. The sensor output voltage was measured with both the DMM in AC mode, and the LIA locked at $\Delta f$.

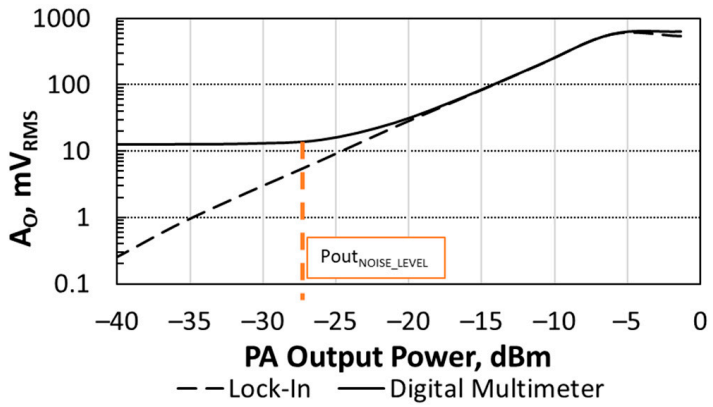


**Figure 11.** Sensors output voltage amplitude as a function of the output power delivered by the CUT to the load. Measurements obtained with a LIA and a DMM in AC mode. Label indicates at which $P_{OUT}$ the DMM readings reach the noise level.

Focusing on DMM measurements, the sensor tracked the power delivered to the load when it was in the range [−25 dBm, −6 dBm] Below this range (−27 dBm, as labelled in Figure 11), DMM readings reached the noise level (which was 12 $mV_{RMS}$,). At the other end of the sensor's linear range above −6 dBm, the sensor output signal became clipped. LIA measurements show that the sensor was able to track the output power delivered to the load for values lower than −6 dBm, with very good agreement with DMM measurements in the range [−19 dBm, −6 dBm]. When the sensor output voltage became clipped, DMM measurements were slightly higher than LIA ones as DMM AC measurements take into account both the sensor's output fundamental and the harmonics generated by the clipping.

If the sensor must track the PA output power for values higher than −6 dBm, the sensor sensitivity ($A_O/P_A$) should be reduced. For example, reducing $A_O/P_A$ by a factor of ten would enable us to measure up to 4 dBm instead of −6 dBm. This would allow, for example, extending the sensor linear response up to the PA compression, and thus be able to monitor its 1-dB compression point.

Several strategies can be followed to reduce the sensor sensitivity: (i) increasing the distance between the CUT and the temperature transducer $T_1$ in the IC layout [40]; (ii) decreasing the BPF gain below the current $A_v$ = 500, which opens the possibility to implement BPF amplifiers with tunable gain for dynamic range extension and (iii) changing the transducer's $T_1$ dimensions or bias [43,44]. All these strategies require either a custom layout depending on the target measurements or the design of additional complex circuits, such as tunable gain networks or a programmable transducer bias. Nevertheless, there is another strategy that can be used without redesigning the sensor or the sensor placement. As pointed out by Figure 9 and discussed in Section 3, the sensor sensitivity can be reduced by choosing a $\Delta f$ value higher than $f_c$. To illustrate this sensitivity reduction, Figure 12 shows the $A_{O,RMS}$ measured with the DMM when increasing $\Delta f$ above 1 kHz, for three constant PA output power values. Focusing on Pout = −6 dBm, with $\Delta f$ = 1 kHz the sensor output had already reached the saturation level observed in Figure 11. As $\Delta f$ was increased, the measured output amplitude decreased (i.e., the sensor enters in the linear range), thus enabling the possibility to monitor higher output powers. Finally, when $\Delta f$ = 200 kHz, the DMM output reached the noise level, and $P_{out}$ = −6 dBm became the $Pout_{NOISE\_LEVEL}$. From Figure 12, $Pout_{NOISE\_LEVEL}$ was −21 dBm when $\Delta f$ = 10 kHz, and −11 dBm when $\Delta f$ = 100 kHz. Therefore, $\Delta f$ selection allowed us to easily adjust the linear response of the sensor to different ranges of dissipated power.

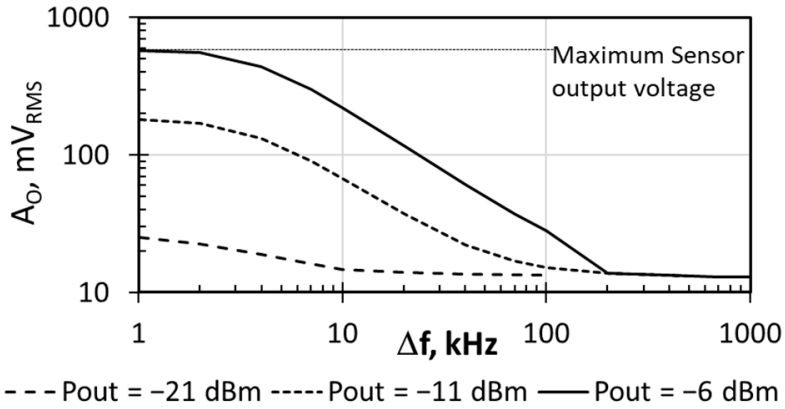


**Figure 12.** Sensor output voltage amplitude as a function of $\Delta f$ for three different output power levels. DMM measurements.

### *4.3. Central Frequency Monitoring*

Figure 13 shows the RF power delivered to the load at the frequency $(f_{RF} + \Delta f/2)$, measured with the RF spectrum analyzer connected to the PA's output; and the sensor's output voltage measured with the DMM in AC mode; both as a function of $f_{RF}$.

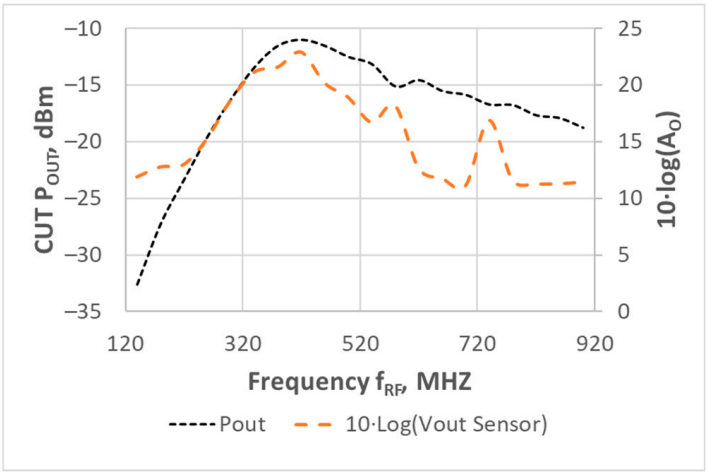


**Figure 13.** Sensor's output measured with the DMM, superposed to power delivered to the load at the frequency $(f_{RF} + \Delta f/2)$ as a function of $f_{RF}$. $\Delta f$ = 1 kHz, and total PA input power = −20 dBm (−23 dBm/tone). Sensor output voltage represented as in [33].

Sensor and PA had the same bias than the one reported in the previous section. In this experiment, the only swept input variable was the frequency $f_{RF}$ (from 120 to 920 MHz). In all the measurements, $\Delta f$ = 1 kHz, and the total PA input power was −20 dBm (−23 dBm each tone), i.e., the PA had a linear behavior. The spectrum analyzer measurements indicated that the PA central frequency was 420 MHz, which agreed with the frequency $f_{RF}$ where the sensor's output amplitude at $\Delta f$ was maximum [31].

## 5. Conclusions

A single MOS transistor used as a temperature transducer connected to a BPF amplifier was presented, characterized and assessed for IC testing applications. The overall sensor circuit was implemented in a standard 0.35 µm CMOS technology, and was built-in with devices acting as controlled heat sources, and an RF power amplifier was used as a CUT. As strong points, heterodyne measurements could be done with a simple DMM, allowing a simplification of the measurement set-up. As the LIA was not required, there was no need for locking the frequencies of all the generators involved in the set-up measurements. Moreover, the task of the DMM could be easily integrated with the CUT, allowing a complete built-in self-test (BIST) solution. As weak point, as DMM integrated noise on a wider bandwidth, DMM readings did not reach the sensitivity levels achieved with an LIA. The sensor characterization showed that the nonlinear $R_2$ behavior did not affect the sensor's linearity as long as $\Delta f$ was higher than the first BPF's cut-off frequency. Moreover, the sensor sensitivity could be reduced by selecting a $\Delta f$ higher than the BPF's central frequency, allowing extension of the sensor's dynamic range. As a proof of concept, we showed the feasibility of the circuit to track the output power delivered to the load and the central frequency of a RF class-A power amplifier.

Future directions of our research are the usage of temperature sensors as monitors in circuits used to compensate the effects of time-variability (e.g., aging) in RF circuits.

## 6. Patents

PCT/ES2013/070095: Sensor Circuit for Obtaining small-signal temperature measurements in integrated circuits.

**Author Contributions:** Conceptualization, F.R., E.B. and J.A.; methodology, F.R., D.M., X.P., and J.A.; circuit simulation, X.A.; circuit design, F.R., E.B., J.A.; board design, E.B. and F.R.; experimental validation, A.B., X.P., D.M., E.B. and J.A.; writing—original draft preparation, J.A., F.R., X.P., X.A. and D.M.; funding acquisition, D.M. and X.A. All authors have read and agreed to the published version of the manuscript.

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