Electrical Power and Energy Systems 133 (2021) 107247

Contents lists available at ScienceDirect

International Journal of Electrical Power and Energy Systems

journal homepage: www.elsevier.com/locate/ijepes

A robust islanding detection method with zero-non-detection zone for distribution systems with DG

Alexandre Serrano-Fontova [a,*], Juan A. Martinez [b], Pau Casals-Torrens [a], Ricard Bosch [a]

[a] Department of Electrical Engineering, Technical University of Catalunya (UPC), Barcelona, Spain
[b] Formerly with Department of Electrical Engineering, Technical University of Catalunya (UPC), Barcelona, Spain

ARTICLE INFO

Keywords:
Distribution networks
Distributed generation
Islanding detection
Smart grids

ABSTRACT

This paper proposes a strategy for detecting unintentional islanding operations (IOs) in distribution networks (DNs) with distributed generation (DG), which eliminating the non-detection zone (NDZ). This hybrid method achieves a zero-NDZ by taking advantage of both passive and active methodologies for an inverter-based DG scenario. The passive-based part of the proposed method considers settings with low thresholds and is activated whenever they are surpassed. The following step uses a three-phase static RC load. This load is connected to intentionally force the frequency and its derivative to exceed the established thresholds. Thus, the events with zero power imbalance can be identified. Unlike other existing methods, this technique does not degrade the power quality (PQ) and does not require DG output power curtailment. The evaluation of the proposed strategy has been carried out through an extensive set of scenarios considering both islanding and non-islanding events. The islanding detection capabilities of the proposed method have been explored considering a custom-made DN test system and the test system recommended by the IEEE 929-2000 standard. The proposed method has a simple implementation, requires a low level of computational complexity, provides a high degree of reliability, and assures fast islanding detection.

1. Introduction

The growing interest in renewable energy resources (RESs) has increased during recent years due to the need to stop global warming and prevent its hazardous effects. Thus, RESs are gaining prominence in the electric power systems, whereas the traditional resources based on fossil fuels are losing interest and being gradually dismantled. Nevertheless, unlike the traditional sources, these RESs may pose several issues for the electrical power systems, undermining their competitiveness. Particularly, given its inherent intermittency due to the energy conversion process, the reliability and the overall system inertia is being jeopardized [1]. In particular, the latter aspect is one of the major concerns for transmission operators (TSOs).

These RESs are being connected to both transmission and distribution networks. Those generation units located at distribution levels are the object of this article. In addition to the aspects mentioned above, one of the issues that DGs are causing to the DNs are the so-called IOs.

Conceptually, an IO occurs when a portion of the network that has been isolated from the main grid remains energized. This scenario has been thoroughly analyzed; see [2]. A distinction between intentional and unintentional is usually considered to classify islanding scenarios. The present study falls within the second type. An essential aspect of any IO study is the capability of the protective devices to detect the island quickly; commonly, within 200-400 ms after the loss of mains have occurred [2]. The list of hurdles in case of failure to trip may include PQ disturbances [3] (e.g., frequency and voltage out of range), a safety hazard for the network personnel, or a damaging effect due to the out-of-phase reclosing. The IEEE Std. 1547 proposes a procedure to follow in these situations and suggests a maximum disconnection time of 2 s [4]. Therefore, the need to detect these unintentional IOs has lead to the implementation of the commonly known islanding detection (ID) methods. Generally, these ID methods can be classified into three main groups: (i) communication-based methods, (ii) passive-based methods, and (iii) active-based methods.

The first group uses several technologies (e.g., optic-fibre, power line communications, etc.) in an attempt to establish direct communications between the circuit breaker (CB) of the substation-feeder with the CB located at the DG interconnection bus. If communication facilities are feasible, it is an excellent option to consider. Indeed, it is widely extended in industry applications [5]. Nevertheless, this strategy has a high economic cost of implementation.

The second group is based on local measurements and are classified

* Corresponding author.

https://doi.org/10.1016/j.ijepes.2021.107247
Received 14 December 2020; Received in revised form 12 April 2021; Accepted 8 May 2021
Available online 11 June 2021

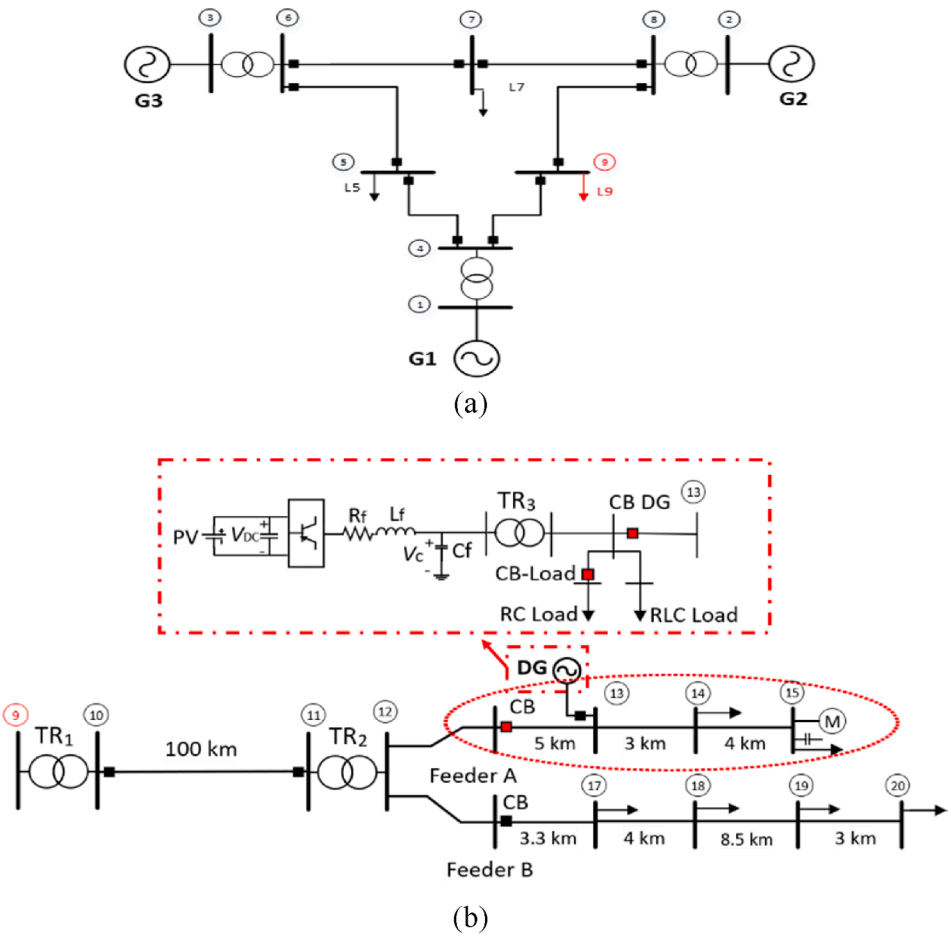

Fig. 1. Custom-made test system. (a) A modified version of the 9-Bus IEEE Test system, (b) DN object of study where islanding occurs.

into three main typologies according to the type of selected variables: time-domain, frequency-domain or pattern recognition strategies. The principal time-domain protective functions are the rate-of-change of frequency protection (ROCOF), the rate-of-change of voltage protection (ROCOV), the under/over voltage protection (UVP/OVP), the under/over frequency protection (UFP/OFP), the rate-of-change of active/reactive power protection (ROCOP/ROCOQ), the rate-of-change of the phase angle difference (ROCPAD) and the vector surge relay; see, for instance, [2,6,7]. An example of a methodology that uses frequency-domain variables can be found in [8]. In general, the low cost and easy implementation are the main advantages of these methods. However, although recent studies have significantly reduced NDZ, these techniques still have large NDZs. Some of them have been conducted taking advantage of decision trees [9], a combination of several passive variables [10], or using algorithms with a large number of datasets obtained through pattern recognition [11]. A common weakness of these methods is the untimely tripping for non-islanding events when their thresholds are set very low to identify near-balanced IOs.

The third group aims to detect IOs by injecting signals into the system to identify either voltage or frequency deviations. Although these techniques have notably reduced the NDZs, the complexity of the required equipment and their negative impact on the PQ are its main disadvantages [12,14]. It is worth mentioning that successful results are achieved when combining these two methodologies in the so-called hybrid methods, see [15,16]. Nonetheless, the bottleneck of these hybrid methods lies in setting the optimal threshold of the required passive-based part to initiate the subsequent active-based one. Crucially, the optimization of this threshold will determine the NDZ of these hybrid methods. A recent review of the currently available ID methodologies can be found in [17].

In this paper, a hybrid methodology is proposed to achieve a zero-NDZ. For this purpose, if any of the time-domain state variables are surpassed, the algorithm orders a three-phase static load connection, causing an under-frequency scenario to identify cases with zero and positive imbalances. If this under-frequency event is not identified, the three-phase load is disconnected so as to identify the negative power imbalances and non-islanding events. Regarding the non-islanding events, a special mention is due to the frequency deviations caused by large-scale imbalances between generation and load, which have not yet been considered in ID studies. Indeed, these type of non-islanding events may be misinterpreted by some ROCOF-based methods or frequency relays as islanding events.

Presently, some grid codes require increasing the ROCOF threshold settings (e.g., above 1 Hz/s) to avoid the disconnection of the DG units during these events. In fact, the effects that this large-scale DG tripping would cause is still under debate and is a serious concern for the TSOs [18].

The remarkable advantages of the proposed method are listed as follows:

- Zero-NDZ.
- Fast tripping time.
- No adverse effects on PQ.
- No need to curtail the DG power.
- High dependability, low cost of implementation and a small degree of computational complexity.

The rest of the paper is organized as follows; Section 2 briefly

introduces the NDZ concept basics used in ID studies. Section 3 details the structure of the custom-made DN test system. Section 4 describes the features of the proposed ID method. Section 5 provides a detailed explanation regarding the adopted criteria to select the threshold settings of the algorithm. Moreover, these theoretical criteria are also used to justify the optimal design of this static load. Section 6 shows and discusses the simulation results obtained from the simulated case scenarios for both islanding and non-islanding events. Section 7 provides an in-depth comparison with some existing ID techniques in order to highlight the contribution of the proposed methodology. Lastly, Section 8 summarizes the principal conclusions of the paper.

2. Basics of the NDZ in ID studies

The concept of the NDZ is referred to a specific region defined by both active and reactive-power imbalances (i.e., right and left, up and down boundaries) where the ID methods are incapable of identifying the islanding condition. The NDZ can be computed for each type of relay or ID method, where its shape depends on the threshold settings, the type of network, and the load model; see the discussion in Section 5. Thence, the boundary of an NDZ for a particular method can be either determined by extensive simulation tests or computed through analytical calculation. A useful study where the NDZ is analytically determined can be found in [19]. The NDZ is a valuable index to predict the possible missoperations of some relays in certain conditions. In addition to the type of relay and its settings, the NDZ also depends on the type of DG and its implemented control (e.g., machine-based or inverter-based) as well as on the particular network under study, see [20]. The NDZ boundaries for the voltage and frequency relays (i.e., either over and under) considering an inverter-based DG scenario with a composite RLC load model are defined in [21]:

$$\left(\frac{V}{V_{max}}\right)^2 - 1 \leqslant \frac{\Delta P}{P} \leqslant \left(\frac{V}{V_{min}}\right)^2 - 1 \tag{1}$$

$$Q_f\left(1 - \left(\frac{f}{f_{min}}\right)^2\right) \leqslant \frac{\Delta Q}{P} \leqslant Q_f\left(1 - \left(\frac{f}{f_{max}}\right)^2\right) \tag{2}$$

where V_{min} and V_{max} are the upper and lower limits for voltage relays, whereas f_{min} and f_{max} are the limits for the frequency relay, ΔP and ΔQ are respectively the active and reactive power imbalances, P is the active power output of the DG and Q_f is the load quality factor. Note that the previous equations are considered for a constant impedance load model.

3. Test system

In order to test the proposed ID method during frequency events (i.e., those events caused by large-scale load-generation imbalances), the DN object of study hangs from a modified version of the 9-Bus IEEE test system. The 9th bus of this test system is connected to a step-down 230/120 kV transformer named TR1, see Fig. 1(a). This transformer is connected with the subsequent 120/25 kV transformer named TR2 through the 100-km subtransmission line (i.e., the line between buses 10 and 11). As shown in that figure, the step-down transformer supplies two medium voltage (MV) feeders, named Feeder A and B. The MV grid is grounded through a zig-zag transformer for fault current limiting. The single-line diagram of the whole system is displayed in Fig. 1(b), where Feeder A is represented as a red dotted circle. The DG object of study is located at this 25-kV MV Feeder, where the IO occurs. The implemented DG is a voltage source converter (VSC)-based photovoltaic (PV) power plant. The DG comprises an aggregate model of the PV arrays equipped with a DC/DC buck-boost converter for the maximum power point tracking. The DC/AC conversion and control is carried out with a three-bridge VSC-based averaged model where the d-axis component I_d depends on the DC bus voltage error, and the q-axis component Iq is set to zero. Therefore, the DG operates at a unity power factor, a commonly adopted DGs solution in grid-connected applications [26]. The DG is connected at the MV bus 13 of the Feeder A through an LC filter plus a step-up 0.26/25 kV 400 kVA transformer named TR3 (see Fig. 1(b)). The three-phase RC 50/40 kW/kVAr load required to identify the IO is switched through the CB-Load (see Fig. 1(b). The system parameters and the DG data are detailed in the Appendix.

Table 1
State Variables.

Symbol	Variable
x_1	ΔV Voltage deviation (pu)
x_2	Δf Frequency deviation (Hz)
x_3	df/dt ROCOF (Hz/s)
x_4	dV/dt ROCOV (pu/s)

4. Description of the proposed method

4.1. Overview

This section is aimed at detailing the main characteristics of the proposed ID method. The first part briefly describes the data mining process, which belongs to the first step of the method (i.e., the passive-based part). Afterwards, the algorithm and its main features are thoroughly detailed. The rest of this section is dedicated to describe the selected settings, their thresholds, and the architecture of the implemented method.

4.2. Data mining of the method

Since the first stage of the proposed algorithm relies on a passive-based methodology, accurate classification of the local measurements becomes an essential task. The time-domain vectors of the four-state variables are as follows:

$$[X_1^j(t)]^T = [x_1^j(t_1), x_1^j(t_2), x_1^j(t_3), \cdots, x_1^j(t_n)] \tag{3a}$$

$$[X_2^j(t)]^T = [x_2^j(t_1), x_2^j(t_2), x_2^j(t_3), \cdots, x_2^j(t_n)] \tag{3b}$$

$$[X_3^j(t)]^T = [x_3^j(t_1), x_3^j(t_2), x_3^j(t_3), \cdots, x_3^j(t_n)] \tag{3c}$$

$$[X_4^j(t)]^T = [x_4^j(t_1), x_4^j(t_2), x_4^j(t_3), \cdots, x_4^j(t_n)] \tag{3d}$$

where $X_m^j(t)$is the *mth* state vector for a particular *jth* event. These vectors can also be expressed using the following transposed 4-dimension vector expression:

$$X_m^j(t)^T = \begin{bmatrix} X_1^j(t_i) \\ \vdots \\ X_4^j(t_i) \end{bmatrix};\ X_m^j(t_i) \in\ 1x4 \tag{4}$$

As mentioned earlier, this vector captures the time-domain variables during the desired period t_n. The state variables for every *jth* event are defined in Table 1. Considering N events, the matrix expression of the whole range of events can be expressed as an N × 4 matrix:

$$X(t_i) = \begin{bmatrix} x_1^1(t_i) & \cdots & x_4^1(t_i) \\ \vdots & \ddots & \vdots \\ x_1^N(t_i) & \cdots & x_4^N(t_i) \end{bmatrix}; X(t_i) \in N\ x\ 4 \tag{5}$$

The state vector X_k expressed in (5) is obtained from the measurements of the three-phase voltages (V_a, V_b, V_c), see the first block of the flowchart in Fig. 2.

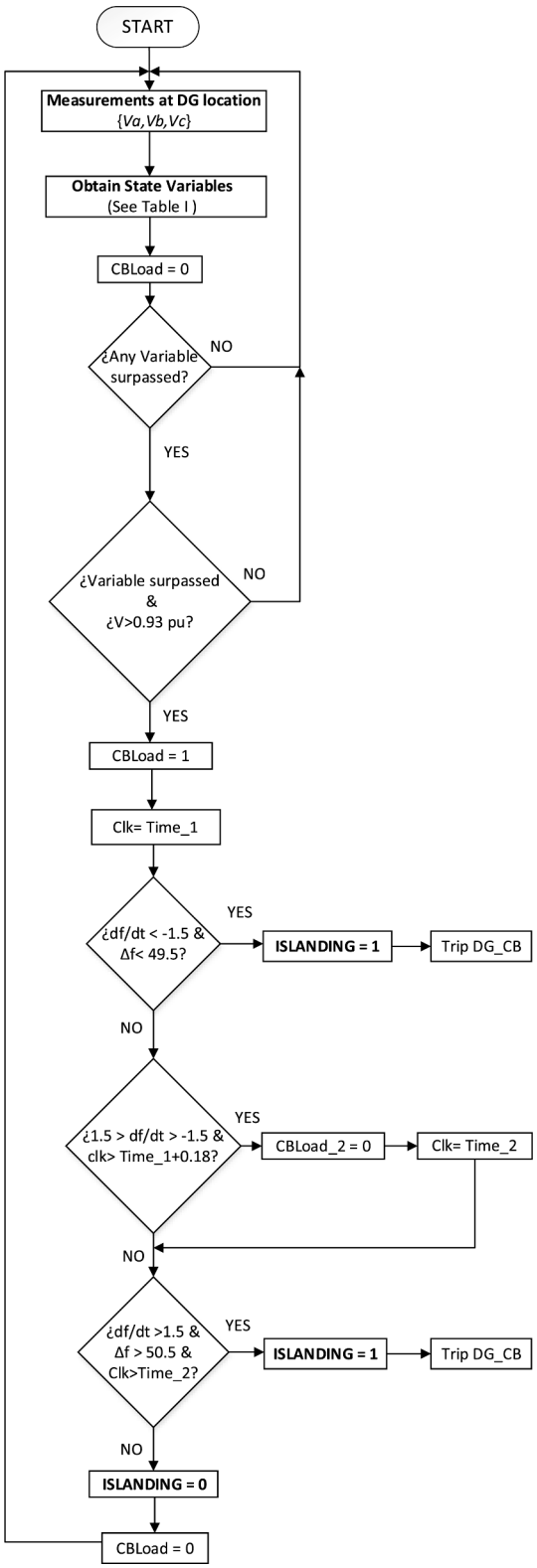

Fig. 2. Flowchart of the algorithm implemented in the proposed ID method.

4.3. Description of the algorithm

The architecture of the proposed ID method is based on the algorithm displayed in the flowchart of Fig. 2. For the sake of clarity, the explanation of this algorithm is divided into four major stages as follows:

The first stage of the algorithm focuses on data mining, which involves two steps (see the first two blocks of the flowchart in Fig. 2). The first step is used for obtaining the local measurements at the DG interconnection bus (i.e., bus 13 of Fig. 1(b)), and the second one computes the four state variables listed in Table 1. Initially, the state the CB of the static load is set to 0, which means that initially this load is disconnected.

Table 2
Settings of the first stage of the method.

Principle of the protection	Setting	Time delay (ms)
Under/Over Frequency supervision	49.7 Hz/50.3 Hz	100
Under/Over Voltage supervision	0.9 pu/1.1 pu	100
ROCOF with 0.85 pu voltage supervision	$2{\cdot}10^{-3}$ Hz/s	20
ROCOV supervision	$2{\cdot}10^{-3}$ pu/s	20

The second stage of the algorithm is aimed at detecting if any state variable is out of range; this is supervised by the first decision block of the flowchart displayed in Fig. 2. Thus, if any state variable exceeds the established thresholds and its delays (i.e., those summarized in Table 2), this block outputs a true signal. Afterwards, to avoid maloperations during faults with a lengthy clearing time, minimum voltage supervision is required (see the second decision block of Fig. 2).

The third stage begins when the three-phase RC load is switched on, and the first-timer is activated (see blocks CB-Load and Time_1 of Fig. 2). Following this switching, if the frequency falls below 49.5 Hz and its derivative below −1.5 Hz/s, islanding is then detected (i.e., see the third decision block of Fig. 2). In this stage, the islanding events with a positive imbalance and those with zero power imbalances are identified, and, as a consequence, the CB of the DG is tripped. The fourth stage begins in case the output of the third decision blocks is negative. In such a case, if the *df/ft* remains between −1.5 and 1.5 Hz/s during 180 ms (see the fourth decision block of Fig. 2), the static load is switched off, and the second timer is activated (see blocks CB-Load and Time_2 in Fig. 2). This step is intended to detect those islanding scenarios with an initial slight negative imbalance that have been compensated due to the load switching. Hence, if

the output of the fourth decision block becomes negative, and another block is required to identify islanding scenarios with larger negative imbalances. To achieve such a goal, the frequency and its derivative have to be positive and above 50.5 Hz and 1.5 Hz/s, respectively (see the fifth decision block of Fig. 2). If the previous constraints are accomplished, the islanding is identified, and the CB of the DG is tripped. On the contrary, if none of the abovementioned steps of the flowchart occurs, the CB state of the static load is returned to its initial value, that is, disconnected.

5. Selection of the optimal threshold settings and the static load size

5.1. Introduction

As shown in the flowchart of the proposed ID method, the connection of the static load occurs if any of the variables summarized in Table 2 are surpassed. Moreover, after the load connection, other thresholds are also considered for ID (see the third and fifth decision blocks in the flowchart of Fig. 2). Therefore, selecting the optimal thresholds for all stages and their delays becomes crucial to avoid undetectable ID regions. The relationship between the active and reactive power and the voltage and frequency for a PV unit with a parallel RLC load in grid-connected mode is defined as follows [21,40]:

$$P_{DG} + \Delta P = \frac{V^2}{R} \tag{6}$$

$$Q_{DG} + \Delta Q = \frac{V^2}{2\pi f L} \tag{7}$$

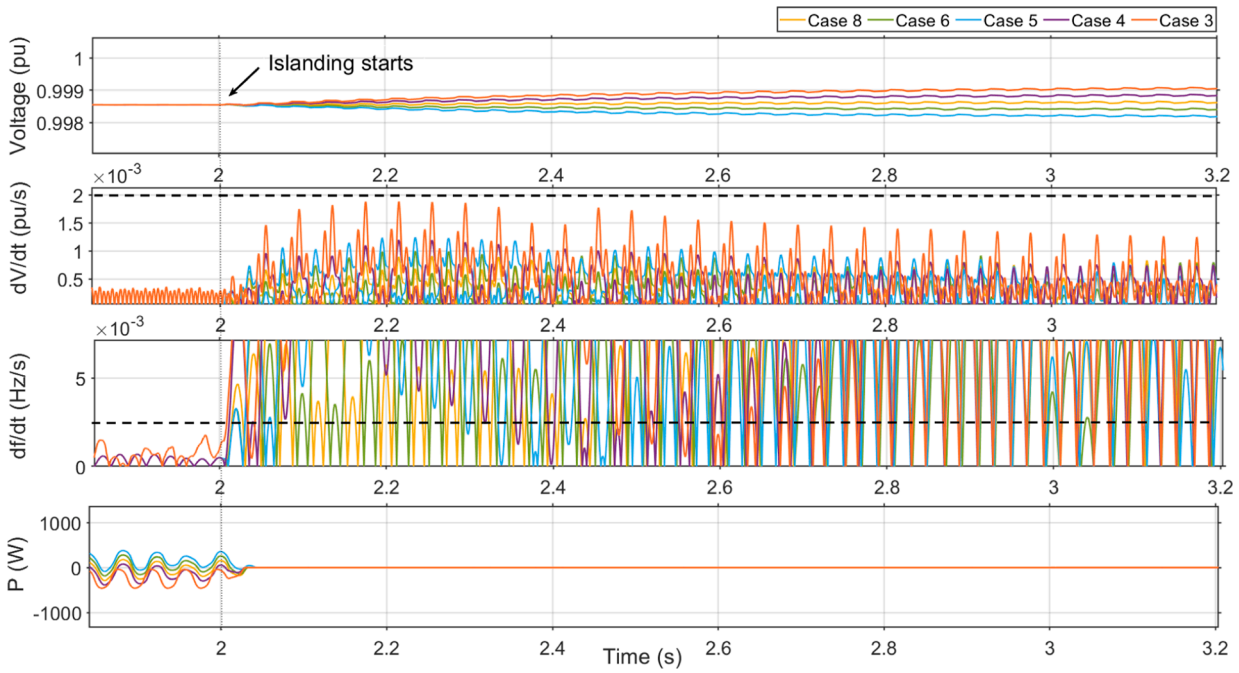

Fig. 3. Sensitivity analysis for the custom-made DN test system of Fig. 1(b) (Mainly Cnt. Z loads).

where P_{DG} and Q_{DG} are the active and reactive powers supplied by the DG unit, ΔP and ΔQ are the active and reactive powers provided by the grid, R is the resistive value of the parallel RLC load, and V is the voltage at the PCC. Once the system is islanded, the terms ΔP and ΔQ become zero, and the mismatch between generation and load dictates the voltage and frequency of the island as

$$V_{island} = \sqrt{R(P_{DG})} \tag{8}$$

$$f_{island} = \frac{V_{island}^2}{2\pi L Q_{DG}} \tag{9}$$

where V_{island} and f_{island} are the voltage and frequency during islanding. Given a change in the voltage due to an active-power mismatch, its derivative with respect to time is obtained as

$$\frac{dV_{island}}{dt} = \frac{\Delta V_{island}}{t} = \frac{\sqrt{R(P_{DG})} - \sqrt{R(\Delta P + P_{DG})}}{t} \tag{10}$$

where $\Delta Visland$ is the voltage variation during islanding.

If a DN is considered instead of the reduced test system with a parallel RLC load, the computed analytical values of both active and reactive imbalances may not coincide with the measured ones due to the voltage drops across the distribution lines. In this sense, if a DN such as

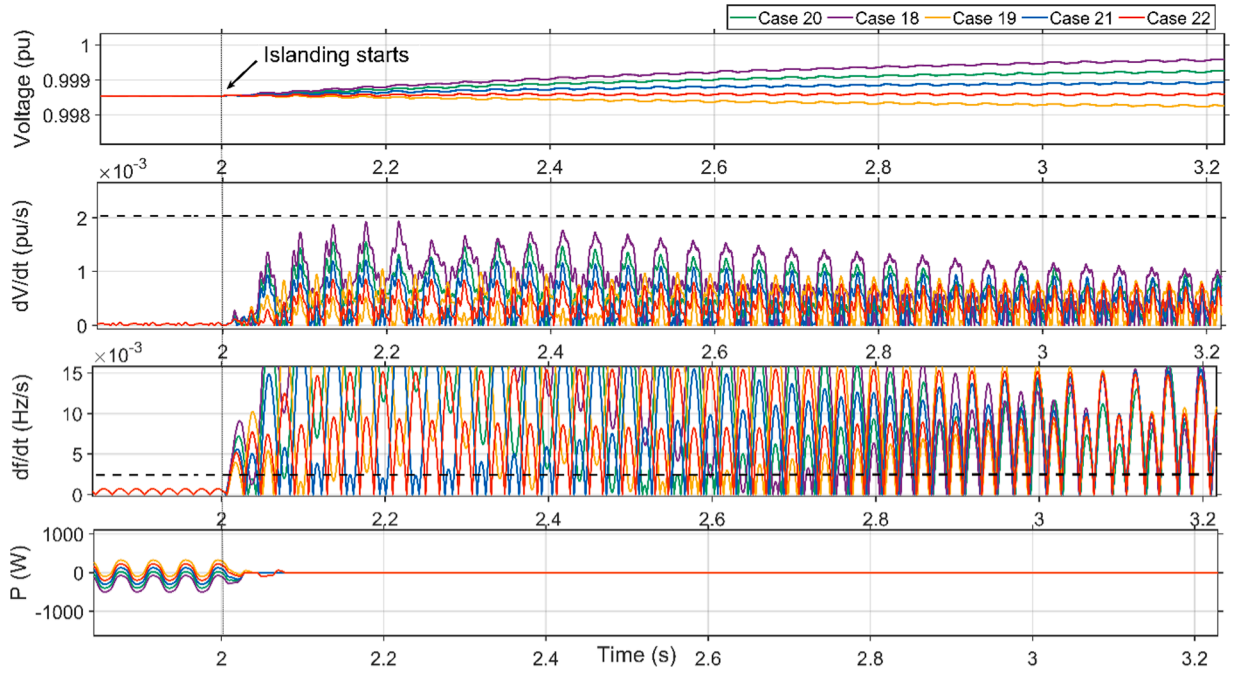

Fig. 4. Sensitivity analysis for the custom-made DN test system of Fig. 1(b) (Mainly Cnt. P loads).

Table 3
Islanding Events with the Custom-made DN Test System.

Case no.	ΔP*(%)	ΔQ*(%)	ΔP_{rated} (%)	ΔQ_{rated} (%)	Load composition*(% Cnt. Z, % Cnt. P, % IM)	Event description	Fault location	TT*(ms)
1	2.57	$-6.6{\cdot}10^{-3}$	1.77	−0.55	(70%,0%,30%)	CB opening	–	82
2	−13	10.6	−14	10	(70%,0%,30%)	CB opening	–	260
3	$-8{\cdot}10^{-2}$	$-6.6{\cdot}10^{-3}$	−0.92	−0.55	(70%,0%,30%)	CB opening	–	97
4	$-2.9{\cdot}10^{-2}$	$-6.6{\cdot}10^{-3}$	−0.9	−0.55	(70%,0%,30%)	CB opening	–	137
5	$5.1{\cdot}10^{-2}$	$-6.6{\cdot}10^{-3}$	−0.82	−0.55	(60%,0%,40%)	CB opening	–	118
6	$2.3{\cdot}10^{-2}$	$-6.6{\cdot}10^{-3}$	−0.84	−0.55	(60%,0%,40%)	CB opening	–	118
7	0.92	0.51	$5.3{\cdot}10^{-2}$	$-5.3{\cdot}10^{-2}$	(60%,0%,40%)	CB opening	–	91
8	$-1.4{\cdot}10^{-2}$	$-6.6{\cdot}10^{-3}$	−0.87	−0.55	(60%,0%,40%)	CB opening	–	141
9	$9{\cdot}10^{-3}$	−0.29	−0.79	0.84	(24%,35%,41%)	CB opening	–	99
10	$9{\cdot}10^{-3}$	−0.55	−0.79	1.1	(18%,38%,44%)	CB opening	–	98
11	$9{\cdot}10^{-3}$	0.22	−0.79	0.3	(22%,38%,40%)	CB opening	–	147
12	$9{\cdot}10^{-3}$	0.47	−0.79	0.005	(22%,38%,40%)	CB opening	–	99
13	0.84	$1.4{\cdot}10^{-2}$	$5.3{\cdot}10^{-2}$	0.55	(21.5%,38.5%,40%)	CB opening	–	91
14	0.36	$1.4{\cdot}10^{-2}$	−0.47	0.55	(21.5%,38.5%,40%)	CB opening	–	96
15	0.24	$1.4{\cdot}10^{-2}$	−0.5	0.55	(21.9%,38%,40.1%)	CB opening	–	96
16	0.16	$1.4{\cdot}10^{-2}$	−0.63	0.55	(21.9%,38%,40.1%)	CB opening	–	96
17	0.14	$1.4{\cdot}10^{-2}$	−0.66	0.55	(22%,38%,40%)	CB opening	–	97
18	0.11	$1.4{\cdot}10^{-2}$	−0.69	0.55	(22%,38%,40%)	CB opening	–	100
19	$-1.7{\cdot}10^{-2}$	$1.4{\cdot}10^{-2}$	−0.71	0.55	(22%,38%,40%)	CB opening	–	101
20	$6.1{\cdot}10^{-2}$	$1.4{\cdot}10^{-2}$	−0.74	0.55	(25%,35%,40%)	CB opening	–	117
21	$3.5{\cdot}10^{-2}$	$1.4{\cdot}10^{-2}$	−0.76	0.55	(25%,35%,40%)	CB opening	–	125
22	$9{\cdot}10^{-3}$	$1.4{\cdot}10^{-2}$	−0.79	0.55	(25.1%,34.9%,40%)	CB opening	–	160
23	−13.4	$1.4{\cdot}10^{-2}$	−14	0.55	(30.9%,20%,49.1%)	CB opening	–	260
24	$9{\cdot}10^{-3}$	$1.4{\cdot}10^{-2}$	−0.79	0.55	(25.1%,34.9%,40%)	SLG Fault with CB opening ($R_f = 0\ \Omega$)	Bus 14	147
25	$9{\cdot}10^{-3}$	$1.4{\cdot}10^{-2}$	−0.79	0.55	(25.1%,34.9%,40%)	LLLG Fault with CB opening ($R_f = 0\ \Omega$)	Bus 14	24
26	$9{\cdot}10^{-3}$	$1.4{\cdot}10^{-2}$	−0.79	0.55	(25.1%,34.9%,40%)	LL Fault with CB opening ($R_f = 0\ \Omega$)	Bus 14	87
27	$9{\cdot}10^{-3}$	$1.4{\cdot}10^{-2}$	−0.79	0.55	(25.1%,34.9%,40%)	LLG Fault with CB opening ($R_f = 0\ \Omega$)	Bus 13	70

* ΔP: Active power imbalance measured at Feeder A expressed in %; ΔQ: Reactive power imbalance measured at Feeder A expressed in %; IM: Induction motors (4x160 kW); TT: Tripping time; Load composition: It represents the % of each type of load according to the voltage-dependence load modelling.

the one displayed in Fig. 1 (b) with different load models is considered, even for a perfect balance between generation and load, a certain power mismatch will occur due to these voltage drops. In particular, DNs with large percentages of constant-impedance loads and induction motors are those scenarios where voltage drops have more influence on these imbalances. The effects of this factor on both the active and reactive power imbalances are detailed in the subsequent Section 6. The sensitivity analysis has been performed separately for the two tested systems.

The first one considers that the whole DN is islanded due to the operation of the CB of feeder A. In contrast, the second one is created by the operation of the CB placed at the DG interconnection bus (i.e., bus 13). For these two major test systems, the zero-power imbalance scenario has been selected as the base case. The subsequent simulations are performed by increasing the active power imbalance by stages of $3{\cdot}10^{-2}$%, where the reactive power imbalance is set to zero.

5.2. Sensitivity analysis for the custom-made DN test system

Since the DN test system object of study considers a composite load model including voltage-dependent loads and induction motors, the sensitivity analysis has been conducted considering two main load modelling scenarios. The first considers a large percentage of constant impedance loads, whereas the second considers a large part of constant power loads. The results of these two sets of simulations are displayed in Figs. 3 and 4. Note that the features of the cases illustrated in Figs. 3 and 4 are also included in Table 3.

The fourth plot of both Figs. 3 and 4 display the active power measured at Feeder A, where the negligible power mismatch is observed. As can be deduced from the second plot of both Figs. 3 and 4, by setting the *df/dt* to $2{\cdot}10^{-3}$ Hz/s, all simulated islanding events would be identified.

Table 4
Islanding Events with the IEEE 929-2000 Test System.

Case no.	ΔP (%)	ΔQ (%)	Q_f	TT (ms)
1	$8{\cdot}10^{-2}$	0	2.5	89
2	$5.8{\cdot}10^{-2}$	0	2.5	90
3	$3.45{\cdot}10^{-2}$	0	2.5	89
4	$3.45{\cdot}10^{-3}$	0	2.5	580
5	$-2.9{\cdot}10^{-2}$	0	2.5	66
6	$-7.7{\cdot}10^{-2}$	0	2.5	65
7	−0.1	0	2.5	62
8	$3.45{\cdot}10^{-2}$	0	1.5	260
9	$3.24{\cdot}10^{-2}$	0	1.5	54
10	$3.45{\cdot}10^{-2}$	0	1.5	95
11	$3.45{\cdot}10^{-2}$	0	1	57
12	$3.45{\cdot}10^{-2}$	0	0.5	61
13	−60	4.2	2.5	28
14	60	0	2.5	28

5.3. Sensitivity analysis for a parallel RLC load

In this subsection, the sensitivity analysis required to set the optimal threshold settings considering the test system recommended by the IEEE 929-2000 standard is detailed. If both active and reactive power imbalances are zero in a PV-based DG scenario, the voltage and frequency do not significantly deviate. However, it has been observed that even for very low power imbalances, the frequency and voltage derivatives with respect to time are non-zero.

In order to carry out an accurate selection of the threshold settings, the zero-power imbalance has been selected as the base case, and further simulations are performed by increasing the active power imbalance by stages of $3{\cdot}10^{-2}$%. The reactive power imbalance is set to zero for all events. The load quality factor of these four simulated cases is set to 2.5

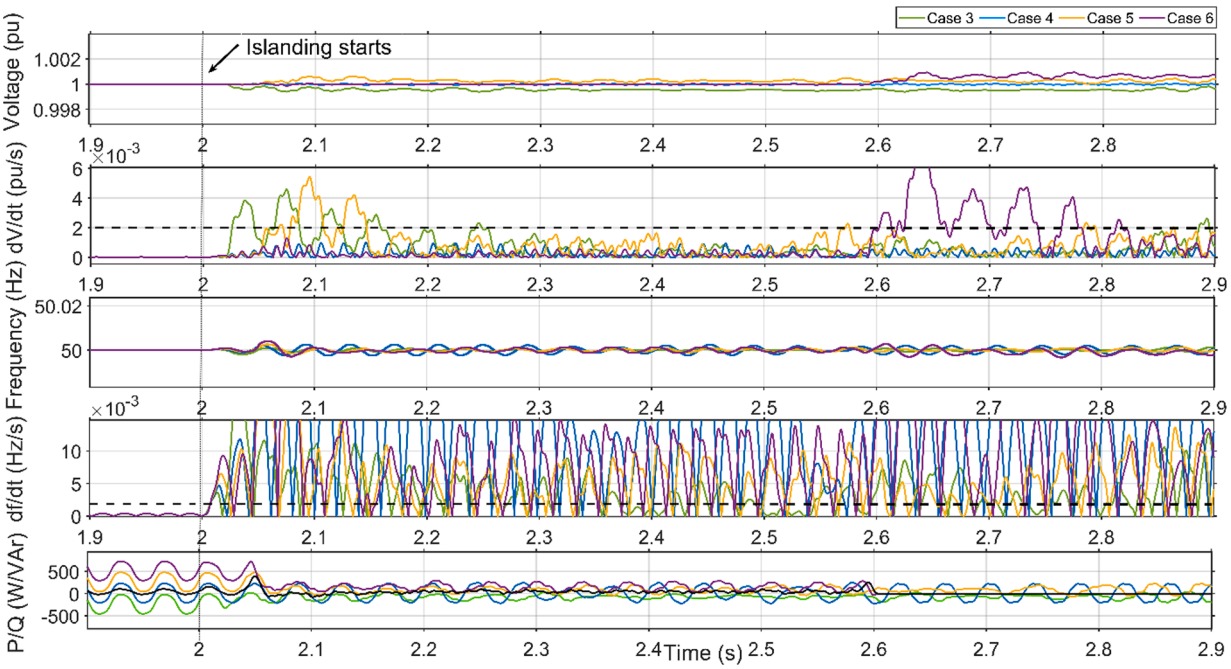

Fig. 5. Sensitivity analysis for the test system recommended by the IEEE 929-2000 standard.

(i.e., cases 3–6 of Table 4). The results of this analysis are displayed in Fig. 5.

By observing the second and fourth plots of Fig. 5, it can be seen that all tested events exhibit *df/dt* and *dV/dt* values higher than $2{\cdot}10^{-2}$ Hz/s and $2{\cdot}10^{-2}$ pu/s respectively. Moreover, in the fifth plot of Fig. 5, the active and reactive powers measured at the CB DG are displayed. The black line in the fifth plot represents the reactive power, which is only shown once because it is equal for all events.

5.4. Optimal design of the RC load

Since the proposed method considers a set of thresholds settings to verify the islanding condition after the load connection, a proper selection of the composition and size of this load is essential. As shown in the third and fifth decision blocks of the flowchart illustrated in Fig. 2, both the frequency deviation and its derivative with respect to time are used to identify the islanding condition. In order to set the optimal parameters, the expected values of both voltage and frequency during the island have to be derived.

Given a PV-based DG scenario with a parallel RLC load, the total resistance in the island after the connection of the static RC load can be computed as

$$R_{total} = \frac{V^2}{(P_{load} + P_{RLC})} \tag{11}$$

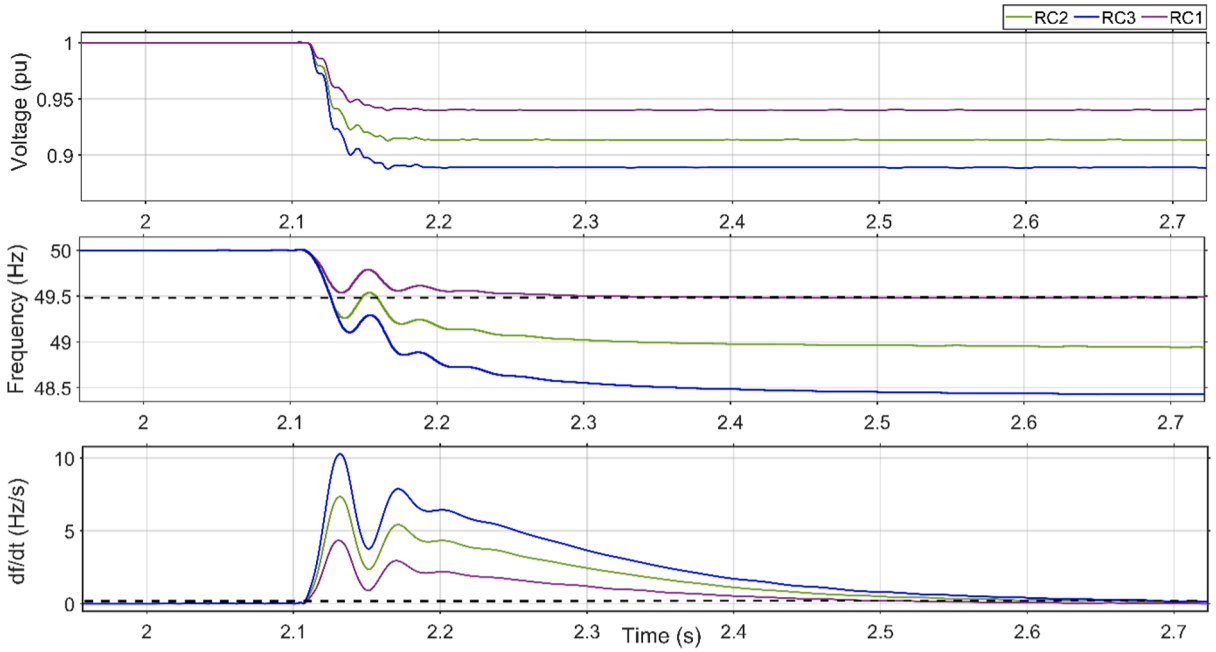

Fig. 6. Sensitivity analysis for the optimal design of the static RC load.

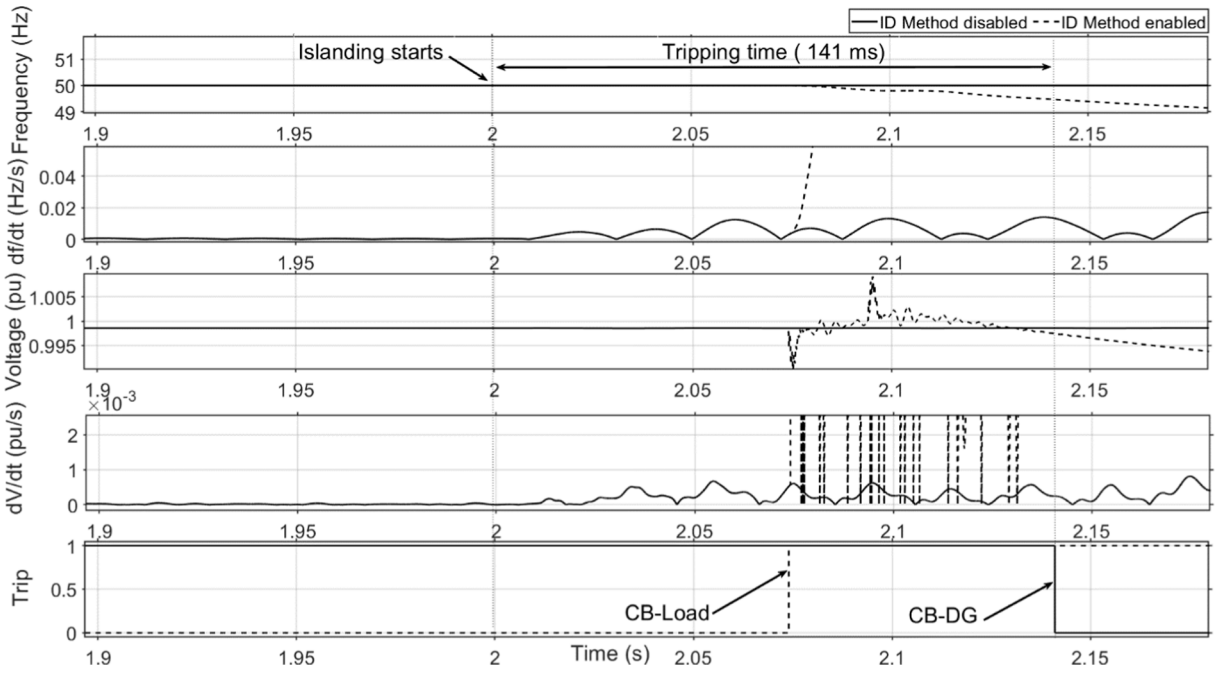

Fig. 7. Results obtained in case 8 of Table 3.

where R_{total} is the total resistance in the island once the RC load has been switched on, P_{load} is the active power of the static RC load, whilst P_{RLC} is the active power drawn by the parallel RLC load. Thereby, if the active power delivered by the DG is kept constant, the voltage deviation introduced by this RC load can be expressed as

$$\Delta V = \sqrt{\Delta R\, P_{DG}} \tag{12}$$

where ΔR is the variation between the initial resistance value and the R_{total} after the RC load has been switched on.

The load quality factor of a parallel RLC load is expressed as

$$Q_f = R\sqrt{\frac{C}{L}} \tag{13}$$

where R, L and C are respectively the resistance, inductance and capacitance of the parallel RLC load.

The frequency of the island is dictated by the resonance frequency of the parallel RLC load as follows

$$\omega_o = 2\pi f_o = \frac{1}{\sqrt{LC}} \tag{14}$$

where ω_o is the angular frequency of the island and f_o the natural frequency of the island. Given an initial quality factor, once the static RC load is switched on, the change in the capacitance produces a variation in the frequency such that

$$\Delta f_o = \frac{1}{2\pi\sqrt{L\,\Delta C}} \tag{15}$$

where ΔC is the variation between the initial and the total capacitance after the RC load switching.

Since the ΔC introduced by the RC load is known, the under-frequency scenario following the load connection can be determined.

Evidence of the abovementioned explanation is displayed in Fig. 6 for three different load compositions (i.e., RC1-50/20 kW/kVAr, RC2-75/40 kW/kVAr, RC3-100/60 kW/kVAr). The first plot of Fig. 6 shows the voltage after the load connection, where the effects of the ΔR are observed, whereas the second and third plot of Fig. 6 shows the effects of the introduced ΔC in both the frequency and its derivative. From the frequency drop following the load connection, the sensitivity analysis of the frequency derivative can be obtained

$$\frac{df}{dt} = \frac{\Delta f}{t} = \frac{f_{initial} - f_o}{t} \tag{16}$$

where $f_{initial}$ and f_o are the frequency before and after the load switching. As can be seen in the flowchart of Fig. 2, the under and over frequency thresholds are set to 49.5 and 50.5 Hz, whilst the frequency derivative is set to ±1.5 Hz/s.

6. Simulation results

6.1. Introduction

This section presents a summary of the study carried out to assess the effectiveness of the proposed ID methodology with the two considered test systems. The first one considers the DN described in Section 3, where the whole DN is islanded after opening the CB of Feeder A. The second test has been carried out according to the IEEE 929-2000 standard [41], which considers a static RLC load with different load quality factors.

As stated earlier, the power imbalance between the DG and loads play a pivotal role in ID studies. Thus, the active and reactive power imbalances are computed through

$$\Delta P_{RATED}(\%) = \frac{(\sum P_{Cnt.Z} + P_{Cnt.I} + P_{Cnt.P} + P_{IM}) - P_{DG}}{P_{DG}} \cdot 100 \tag{17}$$

$$\Delta Q_{RATED}(\%) = \frac{\Delta Q}{P_{DG}} \cdot 100 \tag{18}$$

where ΔP_{RATED} and ΔQ_{RATED} are the rated active and reactive power imbalances, both expressed as a percentage. The first term of the numerator in (17) comprises the four types of loads according to the voltage-dependency load models, plus the induction motors. As stated above, the computed analytical values of the power imbalances may slightly differ from the measured ones at the MV feeder A due to the voltage drops across the DN. Note that both lines and transformers losses (i.e., either active and reactive) are not considered in (17) and (18). Therefore, this paper defines the actual active and reactive power

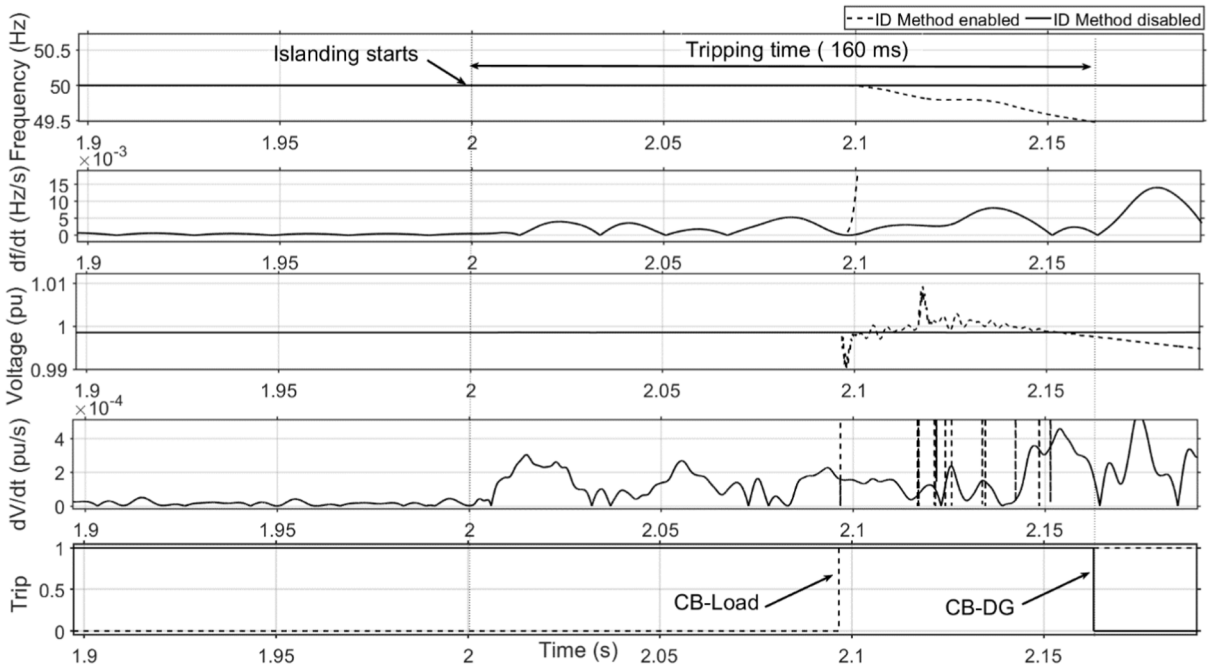

Fig. 8. Results obtained in case 22 of Table 3.

imbalances in the DN once it is islanded with the following expressions

$$\Delta P\,(\%) = \frac{P_{FEEDER\_A}}{P_{DG}} \cdot 100 \tag{19}$$

$$\Delta Q\,(\%) = \frac{Q_{FEEDER\_A}}{P_{DG}} \cdot 100 \tag{20}$$

where ΔP and ΔQ are the actual active and reactive-power imbalances, whereas P_{FEEDER_A} and Q_{FEEDER_B} of (19) and (20) are the active and reactive powers measured at Feeder A. The reactive power imbalances computed in equations (18) and (20) are calculated as a percentage of the DG active power (P_{DG}), which is very common in ID studies where the DG operates at unity power factor [15,20].

As expected, in the simulated cases based on the IEEE 929-2000 Std. test system, the computed analytical power imbalances coincide with those measured in the DG interconnection bus.

The following subsections describe the main characteristics of the simulated case scenarios and depict the obtained results for both islanding and non-islanding events. Additionally, a thorough discussion of the results is presented in Section 6.4.

6.2. *Islanding events*

As stated previously, two major islanding test systems have been

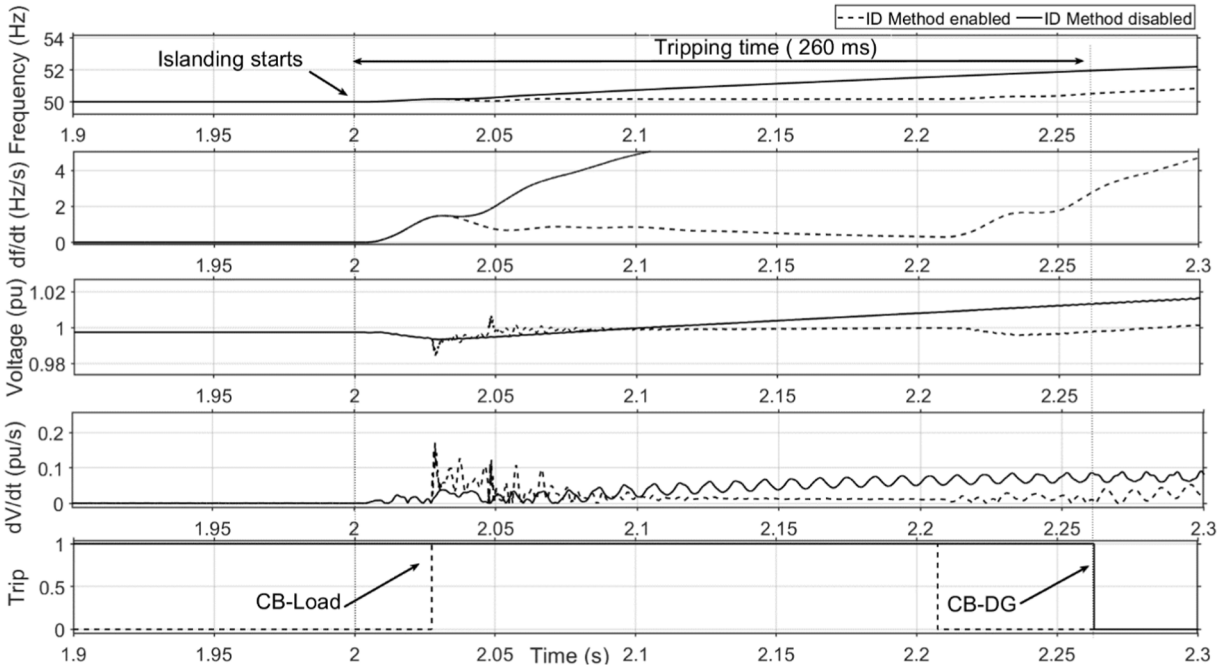

Fig. 9. Results obtained in case 23 of Table 3.

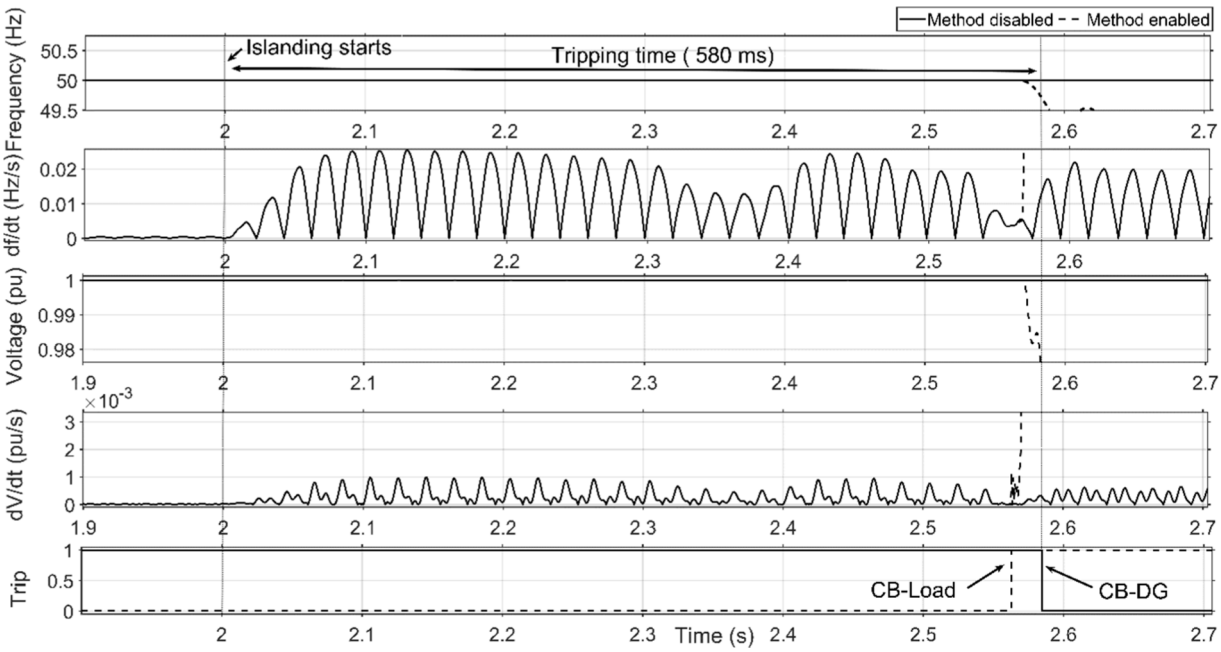

Fig. 10. Results obtained in case 4 of Table 4.

considered for evaluating the present ID methodology. Note that a fault or a smooth switching can cause an islanding event (e.g., due to maintenance, network reconfigurations or false CB operations). Thereby, the islanding condition can occur due to the opening of either the CB of Feeder A or the DG interconnection CB. In the seventh column of Table 3, the origin of this islanding operation is provided. Although many scenarios have been simulated, only a representative sample is shown for the sake of brevity.

6.2.1. *Islanding events with the custom-made DN test system*

In this section, the simulation results with the DN test system displayed in Fig. 1 (b) are provided. The main features of those events are summarized in Table 3. However, the most relevant events in terms of power imbalance are displayed in separate figures where a comparison between the obtained results with and without the method are illustrated. These events belong to cases 8, 22 and 23 of Table 3, displayed in Figs. 7–9. The plotted variables are as follows; *f* (first plot), *df/dt* (second plot), *V* (third plot), *dV/dt* (fourth plot) and the tripping signals (fifth plot). For all events, the islanding begins at t = 2 s. Each case scenario introduces a slight change in the power imbalance for a particular composite load model; see the sixth column of Table 3. By observing that column, two general types of scenarios can be observed, those with and without constant power loads. The percentages provided in the sixth column of Table 3 belong to the active power imbalance. Nevertheless, it is worth pointing out that the reactive power load composition is also divided into constant impedance and constant power loads, plus the

Table 5
Non-islanding Events Description.

Case no.	Event description	Fault Type	Event location	FCT*(ms)	Δf_{Max}*(Hz)	$\lvert df/dt_{Max}\rvert$*(Hz/s)	Duration(s)	Tripping Signal
1	Fault	LLL Fault with (R_f = 0 Ω)	Bus 12	100	3	7.9	0.1	No Trip
2	Fault	LLL Fault with (R_f = 10 Ω)	Bus 12	100	2	5.8	0.1	No Trip
3	Fault	LLG Fault with (R_f = 0 Ω)	Bus 12	100	1.36	4.6	0.1	No Trip
4	Fault	LLG Fault with (R_f = 10 Ω)	Bus 12	100	0.43	1.2	0.1	No Trip
5	Fault	LL Fault with (R_f = 0 Ω)	Bus 12	100	1.36	4.6	0.1	No Trip
6	Fault	LL Fault with (R_f = 10 Ω)	Bus 12	100	0.43	1.2	0.1	No Trip
7	Fault	SLG Fault with (R_f = 0 Ω)	Bus 12	100	0.4	2.1	0.1	No Trip
8	Fault	SLG Fault with(R_f = 10 Ω)	Bus 12	100	0.2	1.5	0.1	No Trip
9	Fault	SLG Fault with (R_f = 200 Ω)	Bus 12	350	0.2	1.5	0.35	No Trip
10	IM starting 4x160 kW	–	Bus 15	–	–	–	0.4	No Trip
11	Capacitor bank switching (150 kVAr)	–	Bus 15	–	–	–	0.1	No Trip
12	Load connection (1 MW)	–	Bus 15	–	–	–	0.25	No Trip
13	Transformer energization (10 MVA)	–	Buses 11–12	–	–	–	0.4	No Trip
14	Frequency event*	–	–	–	0.145	0.1	60	No Trip
15	Frequency event*	–	–	–	0.31	0.14	60	No Trip
16	Frequency event*	–	–	–	0.6	0.4	60	No Trip
17	Frequency event*	–	–	–	0.89	0.6	60	No Trip
18	Frequency event*	–	–	–	1.2	0.83	60	No Trip

* R_f: Fault resistance; SLG = Single-line to ground Fault, LL = Line-to-line fault; LLL Fault = Three-phase Fault; LLG = Two-phase to ground Fault; LLLG: Three-phase to ground Fault; FCT: Fault clearing time; Frequency event: A large-scale imbalance between generation and load; Δf_{Max}: Maximum frequency deviation during the event; $\lvert df/dt_{Max}\rvert$; Maximum frequency derivative during the event.

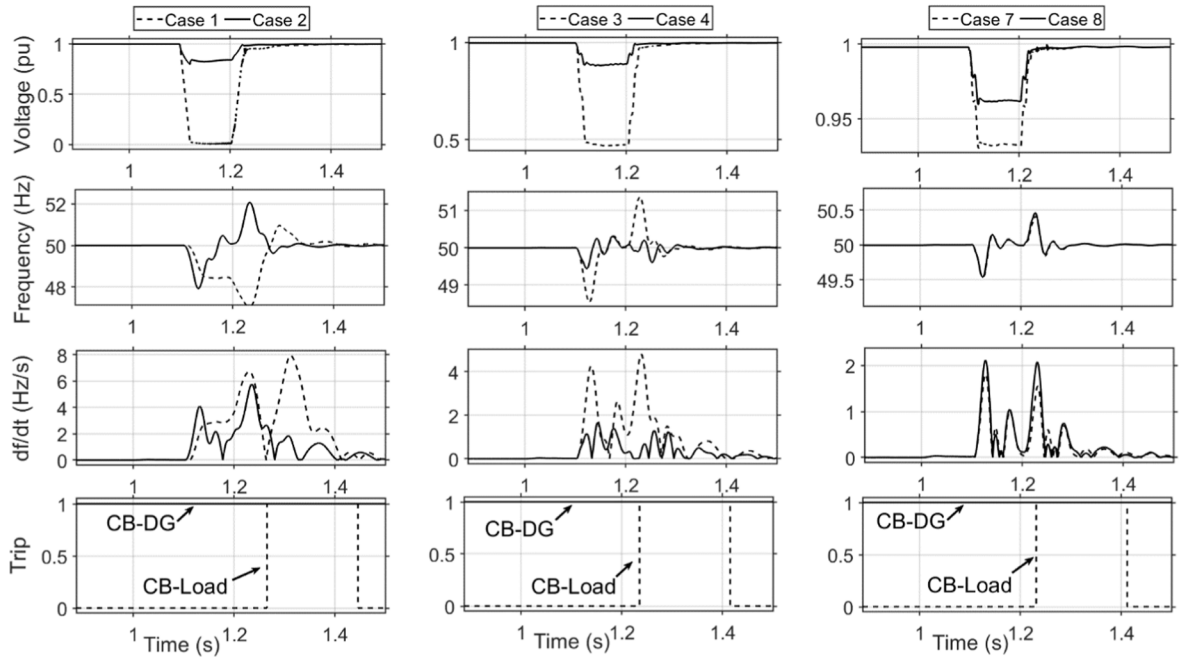

Fig. 11. Results of the non-islanding events of cases 1–8 in Table 5.

induction motors.

As previously stated, if the DG output active power is larger than the load active power, an over-voltage event occurs. On the contrary, an under-voltage will occur. Furthermore, the voltage drop between the DN buses, implies a reactive power imbalance, traduced into a frequency deviation once the static load is connected. This phenomenon is observed in Figs. 7 and 8, which belong to cases 8 and 22 of Table 3.

As shown in the sixth column of Table 3, simulated cases 1–8 are only composed of static loads modelled as constant impedance and a set of induction motors. Whereas cases 9–27 are formed by the same set of induction motors, plus a composite load model based on constant impedance and constant power loads. The details of the dynamic load model used in this paper can be found in [15].

As expected, cases with negative imbalances are easily identified due to the frequency and voltage increase during the island. However, there is the risk of being compensated by the initial RC load connection. Therefore, these negative imbalance scenarios are of particular interest. This casuistry is considered in cases 2 and 23 of Table 3. Even though the load connection has compensated the initial negative imbalance, when the RC load is disconnected, the islanding is correctly identified by the algorithm, see the plots of Fig. 9. Indeed, these cases are the ones that have larger detection times.

6.2.2. *Islanding events considering the IEEE 929-2000 standard*

According to the procedure defined in the IEEE 929-2000 standard for integrating the PV systems into the grid [41], the proposed ID

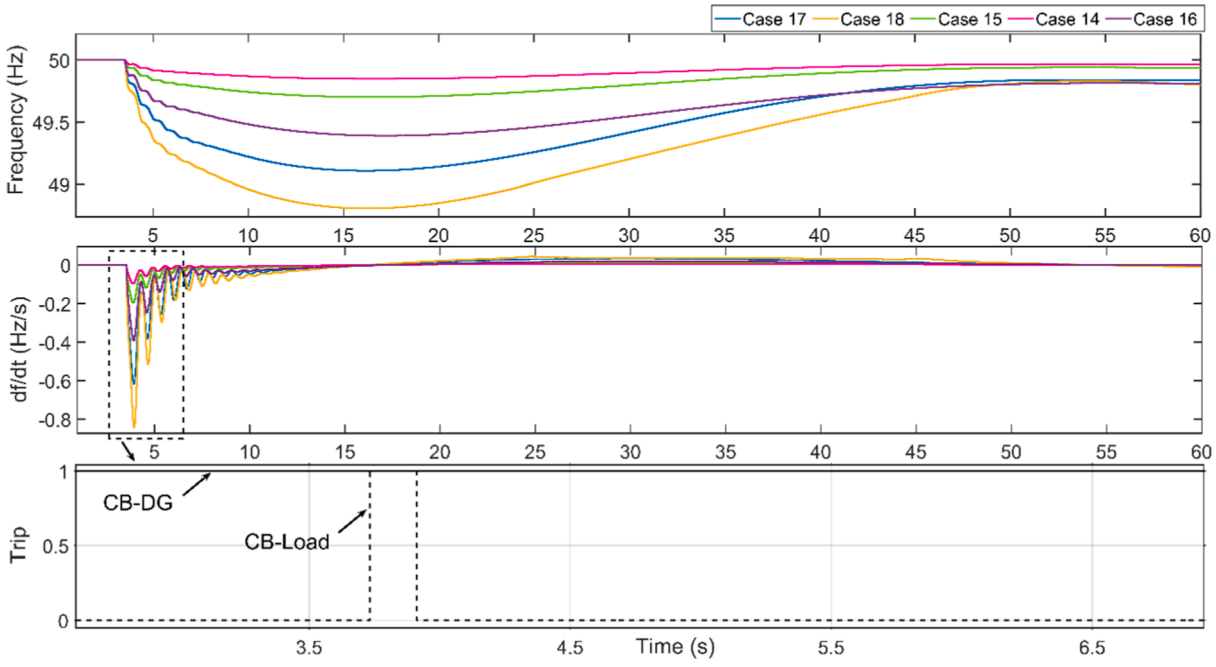

Fig. 12. Results of the non-islanding events of cases 14–18 in Table 5.

Table 6
Comparison with some existing ID Techniques.

Case no.	Proposed method	Method [27]	Method [26]	Method [13]	Method [15]	Method [30]	Method [31]	Method [29]	Method [16]	Method [9]
1	Trip	No Trip	Trip	Trip	Trip	Trip	Trip	No Trip	Trip	No Trip
2	Trip	No Trip	Trip	Trip	Trip	Trip	Trip	No Trip	Trip	No Trip
3	Trip	No Trip	Trip	Trip	Trip	No Trip	Trip	No Trip	Trip	No Trip
4	Trip	No Trip	Trip	Trip	Trip	No Trip	Trip	No Trip	Trip	No Trip
5	Trip	No Trip	Trip	Trip	No Trip	No Trip	Trip	Trip	Trip	No Trip
6	Trip	No Trip	Trip	Trip	No Trip	Trip	Trip	No Trip	Trip	No Trip
7	Trip	No Trip	Trip	Trip	No Trip	No Trip	Trip	No Trip	Trip	No Trip
8	Trip	No Trip	Trip	Trip	No Trip	No Trip	Trip	No Trip	Trip	No Trip
9	Trip	No Trip	Trip	Trip	No Trip	Trip	Trip	No Trip	Trip	No Trip
10	Trip	No Trip	Trip	Trip	No Trip	Trip	Trip	No Trip	Trip	No Trip
11	Trip	No Trip	Trip	Trip	No Trip	Trip	Trip	No Trip	Trip	No Trip
12	Trip	No Trip	Trip	No Trip	No Trip	Trip	Trip	No Trip	Trip	No Trip
13	Trip	No Trip	Trip	No Trip	No Trip	Trip	Trip	No Trip	Trip	No Trip
14	Trip	No Trip	Trip	No Trip	No Trip	Trip	Trip	No Trip	Trip	No Trip
15	Trip	No Trip	Trip	No Trip	No Trip	No Trip	Trip	No Trip	Trip	No Trip
16	Trip	No Trip	Trip	No Trip	No Trip	No Trip	No Trip	No Trip	Trip	No Trip
17	Trip	No Trip	Trip	No Trip	No Trip	No Trip	No Trip	No Trip	Trip	No Trip
18	Trip	No Trip	Trip	No Trip	No Trip	No Trip	Trip	No Trip	Trip	No Trip
19	Trip	No Trip	Trip	No Trip	No Trip	No Trip	Trip	No Trip	Trip	No Trip
20	Trip	No Trip	Trip	No Trip	No Trip	No Trip	No Trip	No Trip	No Trip	No Trip
21	Trip	No Trip	Trip	No Trip	No Trip	No Trip	No Trip	No Trip	No Trip	No Trip
22	Trip	No Trip	Trip	No Trip	No Trip	No Trip	No Trip	No Trip	No Trip	No Trip
23	Trip	Trip	Trip	Trip	Trip	Trip	Trip	Trip	Trip	Trip
24	Trip	No Trip	NC*	NC*	No Trip	Trip	No Trip	No Trip	No Trip	Trip
25	Trip	No Trip	NC*	NC*	No Trip	Trip	No Trip	No Trip	No Trip	Trip
26	Trip	No Trip	NC*	NC*	No Trip	Trip	No Trip	No Trip	No Trip	Trip
27	Trip	No Trip	NC*	NC*	No Trip	Trip	No Trip	No Trip	No Trip	Trip

* NC: Not considered event.

method has been tested with a parallel RLC load under several load quality factors. For that purpose, the DG is islanded with a parallel RLC load plus the static RC load through the CB-DG operation (see Fig. 1(b)). The results of these simulations are summarized in Table 4. Additionally, case 4 is depicted in Fig. 10.

6.3. Non-Islanding events

This section is focused on testing the proposed algorithm for those scenarios that cause voltage drops and frequency oscillations but are not islanding events. To test the reliability of an ID method, these types of events are essential. As for the previous study, although a large number of cases have been simulated, only the most relevant non-islanding events are summarised in Table 5. These 18 events can, in turn, be divided into five major groups as follows:

1. Faults upstream the Feeder A (Cases 1–9).
2. Induction motors starting. (Case no. 10).
3. Capacitor bank switching. (Case no. 11).
4. Transformer energization and load connection. (Cases 12 and 13)
5. Frequency events occurred due to large-scale generation-load imbalances. (see cases 14–18).

Among all the summarised non-islanding events in Table 5, a representative sample of these non-islanding events is shown in separate figures. The first group results (i.e., the faults) are displayed in Fig. 11, while the results of all events of the fifth group (i.e., frequency events) are shown in Fig. 12.

The fault cases have been simulated at bus 12 considering four different types (i.e., SLG, LL, LLG and LLL) with two resistance fault values; $R_f = 0\ \Omega$ and $R_f = 10\ \Omega$, respectively.

Considering the fact that the voltage sag that occurs at the DG terminals is the same for LL and LLG faults due to the grounding in the MV system, only SLG, LLG, and LLL faults are displayed in Fig. 11. The plotted variables in Fig. 11 are as follows: f (first plot), V (second plot), df/dt (third plot) and, tripping signals (fourth plot).

The last set of non-islanding events of Table 5 have been simulated by reducing the mechanical power of the second generator of the modified 9 Bus IEEE test system (see Fig. 1(a)). Therefore, the system experiences a Δf and a df/dt according to these imbalances between generation and load. Thence, Fig. 12 plots the frequency, the df/dt and the tripping signals, respectively.

6.4. Discussion

The main goal of this section is to provide a detailed discussion about the obtained results. Since this paper is focused on ID, only the islanding events will be considered in this discussion.

Firstly, from Figs. 7 to 9, it can be seen that the algorithm is capable of identifying islanding scenarios with insignificant power mismatches when the DN test system is considered. Notably, these figures have proven that, as expected, when the ID method is disabled, both f and V deviations are negligible. Thence, even for negligible imbalances, the islanding condition is identified following the static RC load connection. For instance, for a derisory ΔP and ΔQ of $9{\cdot}10^{-3}$% and $1.4{\cdot}10^{-2}$% respectively (see case 22 in Table 3), the method trips within 160 ms. However, for larger power imbalances, the TT is around five cycles. From the illustrated comparison in Figs. 7–9, it is evident that it would have been very difficult to identify these events with the existing methods. The average tripping time considering the DN test system proved to be 107 ms.

To test the compensation effects of the RC load for initial negative power imbalances, events 2 and 23 have been explored. The simulation results of case 23 are displayed in Fig. 9. As shown in Fig. 9, the RC load connection (at t = 2.025 s) compensates the initial negative power imbalance; therefore, the load disconnection (at t = 2.21 s) is required to identify the islanding condition. The islanding events that caused the opening of the CB in feeder A due to a fault (i.e., cases 24–28 of Table 3) are the easiest to be identified due to the frequency oscillation following the fault.

Secondly, from the results provided in Table 4, it has been demonstrated that all islanding events are correctly identified by the proposed

Table 7
Overall Comparison with other existing ID methods.

Method	NDZ [ΔP]/[ΔQ] (%)	¿Degrade PQ?	¿Considers frequency events? *	¿Considers non-islanding events? *	Degree of practical relevance (H/M/L)	Computational complexity (H/M/L)	Degree of dependability (H/M/L)	TT (s)
Proposed method	**Zero**	**No**	**Yes**	**Yes**	**High**	**Low**	**High**	**0.12**
Ref. [2]	[±2.9]/[±2.9]	No	No	Yes	High	Medium	Medium	0.425
Ref. [9]	[0.17,−0.05]/[0.1,−0.04]	No	No	Yes	High	Medium	Medium	NP*
Ref. [11]	NP*	No	No	Yes	Low	High	High	0.048
Ref. [13]	Nearly Zero	No	No	Yes	High	Low	High	0.366
Ref. [15]	[0.795, −0.85]/[NP]*	No	No	Yes	High	Medium	High	0.46
Ref. [16]	[±0.05]/[±0.15]	Yes	No	Yes	Medium	Medium	High	0.175
Ref. [25]	Nearly Zero	No	No	Yes	High	Low	Medium	0.23
Ref. [26]	Zero	No	No	No	Medium	Low	High	0.03–0.52
Ref. [27]	[8, −10]/[22,−10]	No	No	Yes	High	Low	Medium	0.3
Ref. [28]	[±1.7]/[±1.7]	No	No	Yes	High	Low	Medium	–
Ref. [29]	NP*	No	No	Yes	Medium	Medium	Medium	NP*
Ref. [30]	[±1]/ [±1]	No	No	Yes	Medium	Medium	High	0.1–0.154
Ref. [31]	[±0.4]/ [±1.2]	No	No	Yes	Low	High	High	0.3–0.67
Ref. [32]	NP*	No	No	Yes	Low	High	High	0.04
Ref. [33]	Zero	Yes	No	Yes	Low	High	High	<2
Ref. [34]	[±1]/[±4]	No	No	Yes	Low	High	High	NP*
Ref. [35]	[±0.2]/[±0.2]	No	No	Yes	Medium	Medium	High	0.2
Ref. [36]	[±2.5]/[±2.5]	No	No	Yes	Medium	High	Medium	0.08–0.2
Ref. [37]	NP	No	No	Yes	Medium	Medium	High	NP*
Ref. [38]	NP*	No	No	Yes	Medium	Medium	High	0.12
Ref. [39]	NP*	No	No	Yes	Medium	Medium	High	NP*
Ref. [40]	NP*	No	No	Yes	High	Medium	High	0.2
Ref. [42]	[±0.5]/[±0.5]	No	No	Yes	Medium	Medium	High	0.149
Ref. [43]	[±0.047]/[+0.5]	No	No	Yes	High	Medium	High	0.1
Ref. [44]	[±0.4]/[±0.4]	No	No	Yes	High	Medium	High	0.51

* NP: Not Provided.

ID method if the test system recommended by the IEEE 929-2000 is considered. It is also observed that the higher the load quality factors, the higher the tripping time. The average tripping time for the simulated cases when considering this reduced test system is 120 ms. As suggested by this standard, islanding should be identified with less than ten cycles for events with a power mismatch larger than 50% with a power factor of more than 0.95. The latter casuistry has been considered in cases 13 and 14 of Table 4, where the method trips in 28 ms.

7. Comparison with other existing ID methods

The principal purpose of this section is to compare this method with other recently published ID techniques. Thence, Table 6 compares the ID capabilities between the proposed method and other nine methods. Every method is tested for each case scenario according to those summarized in Table 3. On the other hand, Table 7 provides an overall comparison of the performance, detection time, and other general aspects of interest in ID studies. Note that in Table 7, the comparison methodology has been extended to 22 ID techniques.

Firstly, by analyzing the results in Table 6, it follows that only the present ID method and the one proposed in [26] can identify all tested events with zero-NDZ. However, the method proposed in [26] has not considered non-islanding events and islanding events caused by faults (i.e., see cases 24–27 in Table 3).

Secondly, the benefits and improvements of the proposed ID method are summarized in Table 7.

Besides, in order to provide clear evidence about the novelty of the proposed method and highlight its merits, an individualized discussion is provided below.

References [13,27,28] consider the insertion of several types of impedances whenever islanding is suspected. Particularly, the capacitor-based insertion method in [13] proved very effective for ID. However,

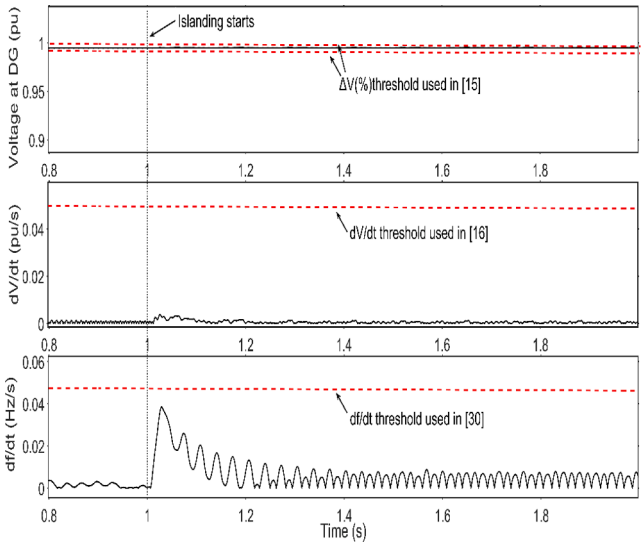

Fig. 13. Voltage, *dV/dt* and *df/dt* obtained for the additional islanding scenario of Section 7.

it would have mistakenly tripped during non-islanding events caused by large-scale frequency deviations, such as those illustrated in Fig. 12. In [27], a pure inductance is proposed where the *dV/dt* threshold is set to 0.1 pu/s, which, as seen, could miss a noticeable amount of islanding scenarios with low power imbalances. An MPPT reduction aimed at causing an additional imbalance is proposed in [15], which implies an undesired DG power curtailment every time an islanding condition is suspected. Furthermore, due to the selected voltage deviation threshold setting in [15] (i.e., ΔV of 0.4%), the method fails to detect some

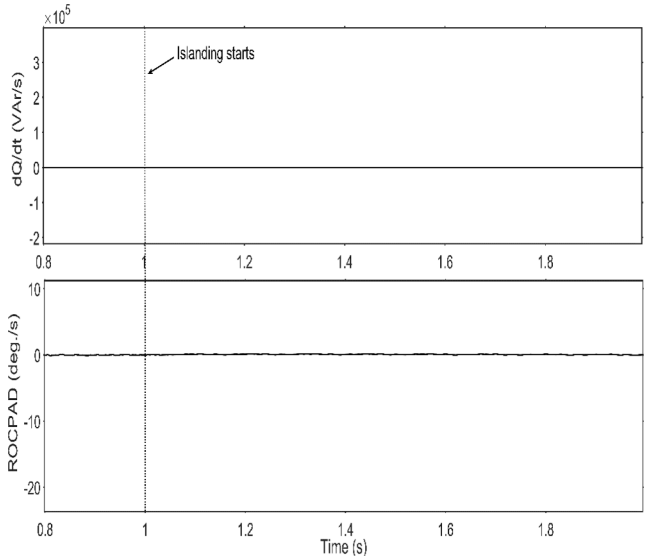

Fig. 14. *dQ/dt* and ROCPAD values obtained for the additional islanding scenario of Section 7.

islanding scenarios.

Additionally, another islanding scenario has been simulated with a 0.12% active power imbalance for comparison purposes. This scenario has considered a static RLC load with a load quality factor of 2.5. Thus, the first and second plots of Fig. 13 show that this particular event is not identified with the selected thresholds in methods [15,16].

Similarly, the flowchart in [30] reveals that this method is only initiated if the *df/dt* exceeds 0.05 Hz/s. Therefore, the third plot of Fig. 13 evidences that with this threshold, this event is misidentified. Moreover, this ID technique has not considered non-islanding frequency events and fail to detect islanding scenarios with significant penetration of constant impedance loads.

On the other hand, the first plot of Fig. 14 shows that the *dQ/dt* threshold used in [28] would have resulted in some undetected islanding scenarios. The second plot of Fig. 14 highlights that the ROCPAD indicator implemented in [29] is ineffective in scenarios with inverter-based DG operating at unity power factor.

Techniques [31,32] demonstrate a high degree of reliability but still have NDZs. Reference [33] holds a zero-NDZ. Nevertheless, it uses a complex active-based method with a synchronized GPS that limits its practicality. Besides, it injects a signal to the grid and degrades the PQ.

In methods [34] and [38], a zero-NDZ is claimed. However, by investigating their settings and results, they seem to have undetectable regions. For example, [34] refers to a zero-NDZ, but a great contradiction appears within the text, where a particular NDZ is revealed (e.g., see the NDZ value in Table 7 of [34]). Similarly, the zero-power imbalance test carried out in [38] proved to have an imbalance of 5.9%, where the DG active power exceeds the load by 0.4 MW.

Some studies have suggested advanced tools and provided satisfactory results, but it has been demonstrated that they still have undetectable regions and drawbacks, see [35–39]. In particular, in references [35,36], only synchronous-based DG scenarios have been considered. In [37], a wavelet-based hybrid ID method is proposed. Even though it has claimed no PQ degradation, it certainly injects an inter-harmonic signal whenever islanding is suspected. Moreover, it has shown only one islanding scenario with a large power imbalance, which leads us to believe that it has a certain NDZ. The modified reactive power control strategy suggested in [39] proved useful. However, in some applications where the inverter-based DG operates at unity power factor and the maximum available active power is delivered to the grid, an additional inverter oversizing would be required to identify IOs.

It is worth mentioning that most of the previously discussed ID methods with low Δf and df/dt thresholds, although proved to be reliable for some islanding scenarios, would probably have misoperated for non-islanding events such as those displayed in Fig. 12, see for instance [22–25]. In particular, the k_v indicator proposed in [25] is computed based on the rated frequency, which could cause undesired tripping during non-islanding frequency events.

Lastly, as stated in [21], the most challenging islanding events to be identified occur when a reduced test system with a parallel RCL load and high load quality factors are considered. Thereby, it has to be noted that the following techniques [9,13,25,27–29,36,39,42] have only considered DNs as a test system to evaluate the ID, and there is no mention of the IEEE 929-2000 standard. Meanwhile, the proposed ID method has been investigated in a custom-made DN test system and considering the IEEE standard procedure.

8. Conclusion

This paper has presented an ID method for DNs with a PV-based DG scenario. This approach overcomes the major drawback of the ID methods by eliminating the NDZ. It uses a static RC load that is switched in case any state variable threshold is surpassed. Although the optimal selection of these settings and their thresholds is the bottleneck of most hybrid ID techniques, this method has successfully dealt with such issue. Furthermore, this paper has provided a sensitivity analysis to justify the selection of the optimal threshold settings and the most appropriate RC load composition and size.

The proposed approach has been tested for a large set of scenarios considering both islanding and non-islanding events. The islanding events have been simulated in two different test systems. The first one is a custom-made DN test system, and the second is the test system recommended by the IEEE 929-2000 standard. Concerning the non-islanding events, this paper has simulated frequency deviations due to large-scale load generation imbalances, which have not yet been considered in ID studies.

In light of the obtained results from the two considered test systems with negligible imbalance scenarios (i.e., in the order of $3.4{\cdot}10^{-3}$%), the zero-NDZ capability of this technique has been undeniably demonstrated. The average tripping time for the events tested with the DN proved to be 107 ms, whereas, with the reduced test system, it is 120 ms. Moreover, all tested islanding events are far below the 2 s disconnection time recommended by the Std. IEEE 1547-2018. Crucially, this method requires very low thresholds to achieve zero-NDZ during islanding events, implying a high risk of misidentification during non-islanding events. Nonetheless, it has to be emphasized that the method has demonstrated high robustness during these events. The most noteworthy characteristics of this method are its simplicity, fast tripping, high dependability, and low computational complexity.

Finally, in order to highlight the novelty of the presented method, an in-depth comparison with some of the recent and relevant published ID techniques has been carried out. Thus, by observing the comparison in Section 7, there is ample evidence of the high profits provided by this method in terms of reliability, practicality and effectiveness.

CRediT authorship contribution statement

Alexandre Serrano-Fontova: Methodology, Software, Conceptualization, Investigation, Writing - original draft. **Juan A. Martinez:** Conceptualization. **Pau Casals-Torrens:** Conceptualization, Investigation. **Ricard Bosch:** Conceptualization, Investigation.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Appendix

This Appendix provides the DG data (see Table 11) as well as the main parameters of the test system displayed in Fig. 1(b), see Tables 8–10. The subtransmission line (named L1) has been modelled as a pi-section, whereas the MV lines, represented by L2, are modelled as series RL impedances. Transformers data can be found in Table 9 and induction motors data in Table 10.

Table 8
Lines Parameters.

Line Type	Z_1(Ω/km)	Z_0(Ω/km)	C/C_0(F/km)
L1 (TN)	0.012 + j0.29	0.38 + j1.17	$12.7e^{-9}$ / $7.7e^{-9}$
L2 (DN)	0.687 + j0.416	3.2 + j1.660	–

Table 9
Transformers Data.

Transformer designation	Power (MVA)	ε (%)	Rated Voltages	Windings Connection
TR1	10	10	230/120 kV	Wye/Delta
TR2	10	10	120/25 kV	Wye/Delta
TR3	0.4	6	0.26/25 kV	Delta/Wye

Table 10
Induction Motors Data.

L_S	0.152 (mH)	P	160 ĸVA (215 HP)
L_R	0.152 (mH)	P	2
R_R	0.0139 (Ω)	F	50 Hz
R_S	0.077(Ω)	V	400 V
L_M	7.9 (mH)	J	2.9 kg.m^2 (0.22 s)

Table 11
DG Data.

Element	Description
PV Array (Model SunPower-315)	Parallel Strings: 230; Series-connected per string: 5; Voc = 64.6 V; Isc = 6.14 A P_{DG} = 400 kW; Q_{DG} = 0 kVAr; V_{DC} = 500 V (rated DC link voltage)
AC/DC converter (controller features)	V_{DC} regulator gains [Kp = 7; Ki = 800] Current regulator gains [Kp = 0.3; Ki = 20]; R_f = 2 mΩ; L_f = 6 mH (RL filter); C_{DC} = 0.1 mF; V_{AC} = 260 V (rated AC phase-to-phase voltage)

References

[1] Ackermann T, Prevost T, Vittal V, Roscoe AJ, Matevosyan J, Miller N. Paving the Way: A Future without inertia is closer than you think. IEEE Power Energy Mag 2017. https://doi.org/10.1109/MPE.2017.2729138.

[2] Cui Q, El-Arroudi K, Joós G. Real-time hardware-in-the-loop simulation for islanding detection schemes in hybrid distributed generation systems. IET Gener Transm Distrib 2017;11(12):3050–6. https://doi.org/10.1049/iet-gtd.2016.1562.

[3] A. Serrano-Fontova, P. C. Torrens, and R. Bosch, "Power Quality disturbances assessment during unintentional islanding scenarios. A contribution to voltage sag studies," Energies 2019, Vol. 12, Page 3198, vol. 12, no. 16, p. 3198, Aug. 2019, doi: 10.3390/EN12163198.

[4] Basso T, Chakraborty S, Hoke A, Coddington M. "IEEE 1547 Standards advancing grid modernization," in *2015 IEEE 42nd Photovoltaic Specialist Conference*. PVSC 2015;2015. https://doi.org/10.1109/PVSC.2015.7356267.

[5] Angrisani L, Bonavolontà F, Liccardo A, Lo Moriello RS. On the use of LORA technology for logic selectivity in MV distribution networks. *Energies* 2018;11(11). https://doi.org/10.3390/en11113079.

[6] Freitas W, Xu W. False operation of vector surge relays. IEEE Trans Power Deliv 2004;19(1):436–8. https://doi.org/10.1109/TPWRD.2003.820412.

[7] Vieira JCM, Freitas W, Xu W, Morelato A. Efficient coordination of ROCOF and frequency relays for distributed generation protection by using the application region. IEEE Trans Power Deliv 2006;21(4):1878–84. https://doi.org/10.1109/TPWRD.2006.881588.

[8] Colombage K, Wang J, Gould C, Liu C. PWM harmonic signature-based islanding detection for a single-phase inverter with PWM frequency hopping. IEEE Trans Ind Appl 2017;53(1). https://doi.org/10.1109/TIA.2016.2611671.

[9] Cui Q, El-Arroudi K, Joos G. Islanding detection of hybrid distributed generation under reduced nondetection zone. IEEE Trans Smart Grid 2018. https://doi.org/10.1109/TSG.2017.2679101.

[10] Khamis A, Xu Y, Dong ZY, Zhang R. Faster detection of microgrid islanding events using an adaptive ensemble classifier. IEEE Trans SmartGrid 2018. https://doi.org/10.1109/TSG.2016.2601656.

[11] Lidula NWA, Rajapakse AD. A pattern recognition approach for detecting power islands using transient signals-Part I: Design and implementation. IEEE Trans Power Deliv 2010. https://doi.org/10.1109/TPWRD.2010.2053724.

[12] Dhar S, Dash PK. Harmonic profile injection-based hybrid active islanding detection technique for PV-VSC-based microgrid system. IEEE TransSustain Energy 2016. https://doi.org/10.1109/TSTE.2016.2515158.

[13] Bejmert D, Sidhu TS. Investigation into islanding detection with capacitor insertion-based method. IEEE Trans Power Deliv 2014. https://doi.org/10.1109/TPWRD.2014.2347032.

[14] Abbey C, Brissette Y, Venne P. An autoground system for anti-islanding protection of distributed generation. IEEE Trans Power Syst 2014. https://doi.org/10.1109/TPWRS.2013.2284670.

[15] Bakhshi-Jafarabadi R, Sadeh J, Popov M. Maximum power point tracking injection method for islanding detection of grid-connected photovoltaic systems in microgrid. IEEE Trans Power Deliv 2020. https://doi.org/10.1109/tpwrd.2020.2976739.

[16] Gupta OH, Tripathy M, Sood VK. Islanding detection scheme for converter-based DGs with nearly zero non-detectable zone. IET Gener Transm Distrib 2019. https://doi.org/10.1049/iet-gtd.2018.5168.

[17] Kim MS, Haider R, Cho GJ, Kim CH, Won CY, Chai JS. Comprehensive review of islanding detection methods for distributed generation systems. Energies 2019. https://doi.org/10.3390/en12050837.

[18] ENTSO-e. Dispersed generation impact on CE region security; 2014. p. 11.

[19] Salles D, Freitas W, Vieira JCM, Venkatesh B. A Practical method for nondetection zone estimation of passive Anti-islanding schemes applied to synchronous distributed generators. IEEE Trans Power Deliv 2015;30(5):2066–76. https://doi.org/10.1109/TPWRD.2014.2360299.

[20] Li Y, et al. Nondetection zone analytics for unintentional islanding in a distribution grid integrated with distributed energy resources. IEEE Trans Sustain Energy 2019. https://doi.org/10.1109/TSTE.2018.2830748.

[21] Ye Z, Kolwalkar A, Zhang Y, Du P, Walling R. Evaluation of anti-islanding schemes based on nondetection zone concept. IEEE Trans Power Electron 2004. https://doi.org/10.1109/TPEL.2004.833436.

[22] Vieira JCM, Freitas W, Xu W, Morelato A. Performance of frequency relays for distributed generation protection. IEEE Trans Power Deliv 2006. https://doi.org/10.1109/TPWRD.2005.858751.

[23] Motter D, Vieira JCM. Improving the islanding detection performance of passive protection by using the undervoltage block function. Electr Power Syst Res 2020. https://doi.org/10.1016/j.epsr.2020.106293.

[24] Grebla M, Yellajosula J, Hoidalen HC. Adaptive frequency estimation method for ROCOF islanding detection relay. IEEE Trans Power Deliv 2019. https://doi.org/10.1109/tpwrd.2019.2956200.

[25] Abd-Elkader AG, Saleh SM, Magdi Eiteba MB. A passive islanding detection strategy for multi-distributed generations. Int J Electr Power Energy Syst 2018. https://doi.org/10.1016/j.ijepes.2018.01.005.

[26] Papadimitriou CN, Kleftakis VA, Hatziargyriou ND. A novel islanding detection method for microgrids based on variable impedance insertion. Electr Power Syst Res 2015;121:58–66. https://doi.org/10.1016/j.epsr.2014.12.004.

[27] Rostami A, Jalilian A, Zabihi S, Olamaei J, Pouresmaeil E. Islanding detection of distributed generation based on parallel inductive impedance switching. IEEE Syst J 2020. https://doi.org/10.1109/JSYST.2019.2923289.

[28] Laghari JA, Mokhlis H, Bakar AHA, Karimi M. A new islanding detection technique for multiple mini-hydro based on rate of change of reactive power and load connecting strategy. Energy Convers Manage 2013. https://doi.org/10.1016/j.enconman.2013.07.033.

[29] Abyaz A, et al. An effective passive islanding detection algorithm for distributed generations. Energies 2019. https://doi.org/10.3390/en12163160.

[30] Xie X, Huang C, Li D. A new passive islanding detection approach considering the dynamic behavior of load in microgrid. Int J Electr PowerEnergy Syst 2020. https://doi.org/10.1016/j.ijepes.2019.105619.

[31] Bakhshi M, Noroozian R, Gharehpetian GB. Novel islanding detection method for multiple DGs based on forced helmholtz oscillator. IEEE Trans Smart Grid 2018. https://doi.org/10.1109/TSG.2017.2712768.

[32] Mlakic D, Baghaee HR, Nikolovski S. A novel ANFIS-based islanding detection for inverter-interfaced microgrids. IEEE Trans Smart Grid 2019. https://doi.org/10.1109/TSG.2018.2859360.

[33] Sivadas D, Vasudevan K. An active islanding detection strategy with zero nondetection zone for operation in single and multiple inverter mode sing GPS synchronized pattern. IEEE Trans Ind Electron 2020. https://doi.org/10.1109/TIE.2019.2931231.

[34] Shayeghi H, Sobhani B. Zero NDZ assessment for anti-islanding protection using wavelet analysis and neuro-fuzzy system in inverter-based distributed generation. Energy Convers Manag 2014. https://doi.org/10.1016/j.enconman.2013.12.062.

[35] Bekhradian R, Davarpanah M, Sanaye-Pasand M. Novel approach for secure islanding detection in synchronous generator based microgrids. IEEE Trans Power Deliv 2019. https://doi.org/10.1109/TPWRD.2018.2869300.
[36] Alam MR, Begum MTA, Mather B. Islanding Detection of distributed generation using electrical variables in space vector domain. IEEE Trans Power Deliv 2020. https://doi.org/10.1109/TPWRD.2019.2929784.
[37] Paiva SC, Ribeiro RL de A, Alves DK, Costa FB, Rocha T de OA. A wavelet-based hybrid islanding detection system applied for distributed generators interconnected to AC microgrids. *Int J Electr Power Energy Syst* 2020. https://doi.org/10.1016/j.ijepes.2020.106032.
[38] Gupta OH, Tripathy M, Sood CK. FPGA implementation of an islanding detection technique for microgrid using periodic maxima of superimposed voltage components. IET Gener Transm Distrib 2020. https://doi.org/10.1049/iet-gtd.2018.5914.
[39] Prajna P Mishra, Chandrashekhar N Bhende. Islanding detection scheme for distributed generation systems using modified reactive power control. IET Gener Transm Distrib 2010. https://doi.org/10.1049/iet-gtd.2017.1777.
[40] Samet H, Hashemi F, Ghanbari T. Islanding detection method for inverter-based distributed generation with negligible nondetection zone using energy of rate of change of voltage phase angle. IET Gener Transm Distrib 2015. https://doi.org/10.1049/iet-gtd.2015.0638.
[41] IEEE recommended practice for utility interface of photovoltaic (pv) systems. IEEE Std 929-2000. doi:10.1109/IEEESTD.2000.91304.
[42] Karimi M, Farshad M, Hong Q, Laaksonen H, Kauhaniemi K. An islanding detection technique for inverter-based distributed generation in microgrids. Energies 2021. https://doi.org/10.3390/en14010130.
[43] Xie X, Xu W, Huang C, Fan X. New islanding detection method with adaptively threshold for microgrid. Electr Power Syst Res 2021;195:58–66. https://doi.org/10.1016/j.epsr.2021.107167.
[44] Bakhshi-Jafarabadi R, Sadeh J, Chavez J, Popov M. Two-level islanding detection method for grid-connected photovoltaic system-based microgrid with small nondetection zone. IEEE Trans Smart Grid 2021. https://doi.org/10.1109/TSG.2020.3035126.