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Enhanced performance controller for high power wind converters connected to weak grids

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Abstract: This study proposes a control scheme for high power grid-connected wind power converters, which is oriented to enhance their performance when connected to weak grids with low short circuit ratio. The proposed controller consists of an outer current reference generation loop and an inner current loop, working in stationary reference frame. In the outer loop, the current reference is calculated to comply simultaneously with the grid code requirements, the control of the DC link, and the operational safety margins of the converter during faulty conditions. On the other hand, the proposed inner current loop consists of a proportional resonant controller, a capacitor voltage feedforward and a phase shifter. Moreover, simulation results considering different weak grid conditions, as well as experimental results of a full-scale 4 MW converter test-bench are presented to validate the good performance of the proposed method.

Nomenclature

<i>i</i> , <i>i</i> _g	current of the converter and the grid		
$i_{p\pm}, i_{q\pm}$	active and reactive components of converter		
	current in positive and negative sequences		
I_{p+}^{*}, I_{q+}^{*}	command of reactive current in positive sequence		
f	fundamental frequency in Hz		
FLL	frequency locked loop		
HV	voltage voltage of transformer in high voltage		
	side		
k _f	feedforward gain		
<i>k</i> _p	proportional gain		
k _i	resonant gain		
$k_{\nu\pm}$	droop coefficient		
LC filter	inductor-capacitor filter		
LPF	low-pass filter		
LVRT	low voltage ride through		
$L_{\rm f}$	inductor of LC filter		
т	modulation index		
PCC	point of common coupling		
P, Q	exchanged active and reactive power with the grid		
SCR	short circuit ratio		
SVPWM	space vector pulse width modulation		
V _{dc}	DC bus voltage		
V_i	output voltage of converter		
V_{g}	grid voltage		
V	PCC voltage		
$ V_{+} , V_{-} $	PCC voltage amplitudes in positive and negative		
	sequences		
Zg	equivalent grid impedance		
$Z_f = X_f = 2\pi f L_f$	impedance of L_f		
ω_o, ω_c	resonant frequency and bandwidth of PR		
0 0	controller in rad/s		
$\theta_{+,} \theta_{-}$	phase of PCC voltage in positive and negative sequences		

Subscripts and superscripts

a, b, c phase

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1	fundamental component
i	converter
in	energy source
dc	DC link
g	grid
max	maximum
+,_	positive sequence and negative sequence, respectively
α, β	Stationary reference frame components
p, q	active and the reactive current components
*	reference
1 In	troduction

Nowadays, high power photovoltaic and wind generation power plants play an important role in the electric power system, covering a significant percentage of the power demand [1, 2]. Although these green energies have a beneficial environmental impact, the particular dynamics, their lack of inertia and the variability of such plants hinders the stability of the network [3]. As a consequence, the transmission system operators (TSOs) have updated their grid codes and standards setting new and demanding requirements for renewable energy-based power plants under steady-state and transient conditions [4, 5] to guarantee a harmonic integration of these plants, whose installation is prone to increase exponentially in the next years. These grid code requirements (GCRs) demand renewable energy source (RES) based power plants to support the network actively during grid faults, injecting positive and negative sequence active and reactive currents during grid faults [6]. These requirements are reflected in the low-voltage ride through (LVRT) requirements issued by the TSOs all over the world [7].

The use of grid feeding voltage source converters is a widespread solution for connecting high power RES-based plants to the grid, due to the good trade-off that such system offers between cost, safe-operation, controllability and dynamic behaviour [8, 9]. Since these plants are often located in remote areas, where the grid has low short circuit ratio (SCR), the control of the power conversion systems has a significant influence on the performance of the grid at the point of common coupling (PCC), especially under fault conditions [10, 11]. In this regard, two main points should be considered in the design of the control scheme





Fig. 1 Single line diagram of the three-phase grid side converter

[12]: (i) To define a suitable current reference considering GCR and the converter operation boundaries; (ii) To design an inner current loop able to track the current reference under all grid conditions.

Concerning the first point, several proposals for generating the operation setpoint have been presented based on the development of power control strategies, especially under faulty grid conditions [13, 14]. For instance, the works presented in [15, 16] proposed different schemes for controlling STATCOMs such as the average active reactive control, the balanced positive sequence control, or the positive negative sequence control (PNSC). Likewise, the flexible positive and negative sequence power control (FPNSC) [17], went one step forward, synthesising current references able to improve the positive sequence voltage profile while minimising the unbalanced voltages produced by the fault. The FPNSC is improved in [18] to avoid using phase locked loop, and it is upgraded in [19] to uniquely determine the current reference by the fault condition and predefined constants from the grid code. The flexible strategy was modified by [20, 21] to limit the current reference during severe conditions; however, the proposed solution gives rise to a complex final implementation. The main reason behind this complexity lays on the fact that these methods convert active/reactive power references to current references, which leads to mismatches and complex calculations to define the grid voltage module in faulty conditions.

The defined current reference in the outer loop should be tracked by the inner current loop [22, 23], which is the second controller indicated previously. These controllers can be referred to natural *abc*, synchronous *dq*0, or stationary $\alpha\beta0$ reference frame components, as finally, all methodologies are mathematically equivalent [24, 25]. However, the development and implementation of controllers in the $\alpha\beta0$ reference frame is currently becoming more popular, as the transformations are simple and less costly from a computational point of view [26]. Besides, this reference frame is itself orthogonal and the cross-coupling terms between control axes are cancelled, while these features cannot be found in implementations based on the *dq*0 axis [27, 28].

In addition to control, hardware plays a significant role, even more in high power systems. In most high power grid-connected power converters, LCL filters are considered the preferred interface with the network [27, 29]. These filters are designed by choosing the resonance frequency value far from the fundamental frequency. However, in high power converters with low switching frequencies, this value is relatively close to the fundamental frequency, which may lead to instability issues in the inner current loop [30]. To overcome this drawback, two methods are broadly extended for damping the resonance peak: introducing physical passive damping by adding some passive elements to the LCL filter or introducing active damping by changing the structure of the controller to increase the magnitude and phase margins (PMs) around the resonance frequency [31]. However, the implementation of effective active damping is not straightforward [32], and different proposals have been presented in [33, 34].

According to the latest changes in the grid codes, during grid faults power plants must inject positive and negative sequence reactive currents based on the voltage profile at the PCC [5, 35]. Based on the literature review of authors, a dual control scheme in dq0 was presented in [21] to cover new grid codes; however, this

study only presented simulation results and did not consider the practical constraints and resonance issues in real high power converter. Other researches in [7–20] have mainly used power references as interface variable to find out the current references in dq0 and $\alpha\beta0$, but there is a lack of research about implementing the new grid code precisely in $\alpha\beta0$. Moreover, the specific issues associated with the implementation and performance of the control scheme when applied to high power converters have not been carefully addressed yet. In a real case, practical issues such as the delay in the measurement systems, the appearance of resonances in weak grids or the reduced controllability due to the use of low switching frequencies have a significant influence in the control of such converters, especially under faulty and transient conditions.

In this paper, an enhanced control scheme, consisting of an outer current reference generator loop and an inner current loop, both working in the $\alpha\beta0$ domain is proposed for a real 4 MVA high power converter. In the outer loop, instantaneous active and reactive current references are generated. These references are calculated and tailored to fulfil the GCRs. To work in a wellreferenced scenario, the current references will be found considering the constraints of the German grid code VDE-AR-N-4120, which is oriented to set the operation boundaries of gridconnected converters under grid fault conditions. In this controller, the proposed inner loop is based on a proportional resonant (PR) controller combined with a voltage feedforward and a new phase shifter for tracking the current reference. This paper intends to deal with practical issues, the proposed solution will integrate as well an active damping system using a voltage feedforward, which will be proven to be a robust method in case of having grid impedance variations. In addition, the implementation of a phase shifter, able to compensate the delay of measurement transducers, and the improvement of the phase lag related to the voltage feedforward will also be contributions linked to this work.

This paper is organised as follows. In Sections 2 and 3, the study case and the description of the proposed control scheme are presented, respectively. In Section 4 the simulation results that permit to analyse the performance of the proposed controller under steady-state and faulty conditions are presented. Likewise, the experimental performance is analysed in Section 5, where results collected in a full-scale 4 MW three-phase wind power converter test-bench are shown. Finally, the conclusions and final discussions that arise from this work are presented in Section 6.

2 System under study

The schematic diagram depicted in Fig. 1 shows the layout of a typical high power grid side converter (GSC) of a generation system, where the energy source is modelled as an ideal current source.

The grid connection filter of the GSC is designed to limit the harmonic injection, limited by the standards. In many applications, this filter is a low-pass filter implemented following an LC or an LCL structure [33]. In this case, L_f and C_f are inductance and capacitance of the LC filter, also Z_g ($r_g + sL_g$) is equivalent grid impedance. The input of energy at the DC side is modelled as a current source i_{in} , which is variable and unpredictable. The braking resistance *R* in series with a chopper is used to keep the DC bus voltage below the safety limits. The parameters of the 4 MVA study case are listed in Table 1.

3 Proposed control strategy

The outline of the proposed control strategy is shown in Fig. 2.

In a nutshell, as the system should be responsive to all kinds of voltage sags, the voltage at the capacitors and the converter's current are measured and considered in the current reference generator, where other elements such as the DC voltage regulation and other references are added. This current reference is generated in the outer loop and then tracked by a PR controller in the inner loop, where a phase shifter and active damping blocks are included.

Table 1 GSC parameters				
Symbol	Description	Value		
V, V _{rms}	nominal line voltage	690		
S _{NOM} , MVA	rated power	4		
V _{dc} , V	dc-link voltage	1150		
L _f , μH	filter inductor	65		
C _f , μF	filter capacitor	1000		
f _O , Hz	rated frequency	50		
f _S , kHz	switching frequency	2		
C, mF	dc-link capacitor	60		



Fig. 2 Modular framework for controlling the high power grid side converter

3.1 Outer loop: reference generation

The schematic diagram of the proposed outer loop is shown in Fig. 2. In this scheme, it can be seen that the current reference in the stationary reference frame (SRF) is obtained based on the voltage conditions at the PCC and the DC side. In this loop, a current limiter and anti-saturation blocks are included to guarantee that the operation boundaries of the converter do not affect the stability and performance of the control stage. In the figure, the signals $i_{p\pm}^*$ and $i_{q\pm}^*$ are the positive & negative active and the reactive current set-points for the converter, which are converted to the $\alpha\beta$ domain to be used as the inputs to the inner loop.

The value of i_{p+}^* is produced by the DC bus controller, and it is focused on maintaining the voltage at the DC side. According to the standards, the converter should inject reactive currents to support the grid during faults. In Fig. 2, it is shown how the reactive current reference i_{q+} is defined based on the voltage drop/ rise at the PCC multiplied by the droop coefficient k_{v+} [33, 35]. The dead-band is implemented according to the requirement of each country, which determines different bandwidths. The value of i_{q+}^* is obtained from the addition between the reactive current command I_{q+}^* plus i_{q+} . The i_{p-}^* is equal to zero according to the VDE-AR-N 4120.

A similar control characteristic can be adopted for the negative sequence. In this case, the t_{q-}^* is determined based on the droop function that is applied to the negative sequence voltage at the PCC.

$$\begin{cases} i_{q+} = 0 & |\Delta|V_+|| < V_{\text{band}+} \\ i_{q+} = k_{v+}(\Delta|V_+| - V_{\text{band}+}) & \Delta|V_+| > V_{\text{band}+} \\ i_{q+} = k_{v+}(\Delta|V_+| + V_{\text{band}+}) & \Delta|V_+| < -V_{\text{band}+} \end{cases}$$
(1)

$$\begin{cases} i_{q_{-}} = 0 & |V_{-}| < V_{\text{band}} \\ i_{q_{-}} = k_{v_{-}}(|V_{-}| - V_{\text{band}}) & |V_{-}| > V_{\text{band}} \end{cases}$$
(2)

where $V_{\text{band}\pm}$ is the threshold voltage in which the GSC has to work in voltage supporting mode injecting reactive current to the PCC. Also, $\Delta |V_+|$ and $|V_-|$ are equal to $1 - |V_+|$ and $|V_-|$, in per unit, respectively.



Fig. 3 DC link voltage control loop



Fig. 4 Vector representation of positive and negative components

It is worth mentioning that the rate limiter in Fig. 2 is used to reduce the change rate of the active current reference in case of grid faults when the reactive current is increased to support the grid voltage. Depending on the application, the country and the technology this rate limiter may be different.

3.1.1 DC bus controller: The dynamic model of the DC side is shown in Fig. 3, where P_0 , P_{loss} , and P_{in} are the output active power of the converter, the power losses and the power input, respectively. V_{dc0} is the nominal value of DC bus voltage and T_v is the delay of the voltage transducer.

In the outer loop, the i_{p+}^* is generated by the DC bus controller. The structure of the dc-link voltage controller and the associated power loop is shown in Fig. 3.

In Fig. 3, the control strategy is implemented in per-unit system. P_{base} and I_{in} are the nominal power and the active feedforward current, respectively. The open-loop transfer function of the DC link loop ($GHdc_{\text{ol}}$) is equal to:

$$GHdc_{ol} = \left(K_{pdc} + \frac{K_{idc}}{s}\right) \frac{P_{base}}{sV_{dc0}^2C} \frac{1}{1 + sT_v},$$
(3)

where K_{pdc} and K_{idc} are the proportional coefficient and the integral coefficients of the PI controller, respectively.

Considering the relatively slow dynamics of the DC link, it is possible to ignore the effect of the transducer in the design of the proportional–integral (PI) controller. Therefore, the open-loop transfer function of the DC link loop can be written as:

$$GHdc_{\rm ol} = \underbrace{\frac{P_{\rm base}}{V_{\rm dc0}^2 C}}_{K} \frac{1}{s} \left(K_{\rm pdc} + \frac{K_{\rm idc}}{s} \right) = \frac{K}{s} \left(K_{\rm pdc} + \frac{K_{\rm idc}}{s} \right), \tag{4}$$

Then, the closed-loop transfer function of the DC control loop $(GHdc_{cl})$ is equal to:

$$GHdc_{cl} = \frac{sKK_{pdc} + KK_{idc}}{s^2 + sKK_{pdc} + KK_{idc}} = \frac{2\zeta\omega s + \omega^2}{s^2 + 2\zeta\omega s + \omega^2},$$
 (5)

The above transfer function reveals that the DC link loop presents a low-pass filtering characteristic, which is an interesting feature for

IET Renew. Power Gener., 2020, Vol. 14 Iss. 12, pp. 2058-2067 © The Institution of Engineering and Technology 2020 attenuating noisy and high-frequency signals. By choosing $K_{pdc} = 4$ and $K_{idc} = 100$, the system becomes stable with a PM of 103°, significantly higher than the 60° considered typically. Likewise, the settling time (t_s) can be found from (6):

$$t_{\rm s} = \frac{4}{\zeta \omega} = \frac{8}{KK_{\rm pdc}} = 0.04 \,\rm s, \tag{6}$$

3.1.2 Anti-saturation: The GSC needs a minimum voltage in the DC link for injecting reactive power to the PCC. If the value of the DC link voltage reduces below a certain level, the current controllers can get saturated and over modulation may occur giving rise to harmonic currents. An anti-saturation scheme based on a PI controller was proposed by Neumann *et al.* [35] to modify the reactive power setpoint and prevent uncontrollability. However, this method is slow and cannot avoid the saturation in transient conditions. In this paper, a new analytical anti-saturation scheme is proposed, based on a reference modifier. The proposed method by authors in [36] can adjust the reactive current reference, according to (7), taking into account the grid conditions and the operation points, with no need to know the grid impedance or the voltage

$$i_{q+\max}^{*} = \frac{\sqrt{\left(V_{i\max} - V_{-} + X_{f} | i_{q-}^{*} | \right)^{2} - \left(X_{f} i_{p+}^{*}\right)^{2} - V_{+}}}{X_{f}}$$
(7)

where the maximum phase voltage V_{imax} is equal to $V_{\text{dc}}/\sqrt{3}$.

3.1.3 *Current limitation:* During faults, the converter should remain connected to the grid, and its current is not allowed to exceed its maximum value set by the semiconductors. On the other hand, according to the standards, the converter must inject reactive current in the positive and the negative sequences with a pattern like Fig. 2 for voltage support. Therefore, the active component of the positive sequence has to be reduced to limit the converter current. Considering the time domain diagram for the positive and negative sequence of the currents, depicted in Fig. 4, the phasor representation for both can be found as shown in (20) and (21)

$$i_{+} = \underbrace{\sqrt{(i_{p+}^{*})^{2} + (i_{q+}^{*})^{2}}}_{|i_{+}|} \angle \underbrace{\left(\theta_{+} - \tan^{-1}\left(\frac{i_{q+}^{*}}{i_{p+}^{*}}\right)\right)}_{\theta_{i+}} = |i_{+}| \angle \theta_{i+},$$
(8)

$$i_{-} = \underbrace{\sqrt{(i_{p-}^{*})^{2} + (i_{q-}^{*})^{2}}}_{|i_{-}|} \angle \underbrace{\left(\theta_{-} - \tan^{-1} \left(\frac{i_{q-}^{*}}{i_{p-}^{*}}\right)\right)}_{\theta_{i-}} = |i_{-}| \angle \theta_{i-} .$$
(9)

where θ_+ and θ_- are the phase of positive and negative sequences, respectively.

Then the amplitude of converter current can be found as:

$$i^{2} = |i_{+}|^{2} + |i_{-}|^{2} + 2|i_{+}||i_{-}|\cos\theta$$
(10)

$$\begin{cases} \theta = \theta_{+} - \tan^{-1} \left(\frac{i_{q}^{*}}{i_{p}^{*}} \right) + \theta_{-} - \tan^{-1} \left(\frac{i_{q}^{*}}{i_{p}^{*}} \right) \\ \theta_{+} = \omega t + \theta_{+0} \\ \theta_{-} = -\omega t - \theta_{-0} \\ \to \theta = 2\omega t + \theta_{+0} + \theta_{-0} - \tan^{-1} \left(\frac{i_{q}^{*}}{i_{p}^{*}} \right) + \tan^{-1} \left(\frac{i_{q}^{*}}{i_{p}^{*}} \right) \end{cases}$$
(11)

where θ_{+0} and θ_{-0} are the initial phases. Therefore, in (10) by setting $\cos\theta = 1$ the maximum converter current I_{max} can be expressed as follows:

$$I_{\max}^{2} = |i_{+}|^{2} + |i_{-}|^{2} + 2|i_{+}||i_{-}|$$

$$\rightarrow |i_{+}|^{2} + 2|i_{-}||i_{+}| + |i_{-}|^{2} - I_{\max}^{2} = 0$$

$$\rightarrow x^{2} + 2bx + c = 0, \quad x = -b \pm \sqrt{b^{2} - c}$$
(12)

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Fig. 5 Inner loop block diagram

As a result, the maximum available active current can be found from (13):

$$\rightarrow |i_{+}| = -|i_{-}| \pm I_{\max} = I_{\max} - |i_{-}|$$

$$\rightarrow \sqrt{(i_{p+}^{*})^{2} + (i_{q+}^{*})^{2}} = I_{\max} - |i_{-}|$$

$$\rightarrow i_{p+\max}^{*} = \sqrt{(I_{\max} - |i_{-}|)^{2} - (i_{q+}^{*})^{2}}$$

$$(13)$$

3.1.4 Current reference generation in SRF: There are different methods to obtain the current reference in the SRF from the active and the reactive components: $i_{p\pm}^*$ and $i_{q\pm}^*$. These strategies require the estimation of the negative- and positive-sequence components of the grid voltage under generic conditions. In this regard, some advanced and robust techniques were suggested to detect grid voltage components, which they can work perfectly under unbalanced and distorted grid voltages. In this paper, a dual second order generalised integrator frequency locked loop (DSOGI-FLL), due to its accuracy and fast response, is used for estimating the magnitude of the symmetrical components of the voltage at the PCC [37].

The following method is based on the instantaneous power theory and FPC [15], where the current set-points in the SRF are found from the active and reactive power set-points based on the following relationship:

$$\begin{bmatrix} i_{\alpha_{+}}^{*} \\ i_{\beta_{+}}^{*} \end{bmatrix} = \frac{1.5V_{\text{base}}}{v_{\alpha_{1}+}^{2} + v_{\beta_{1}+}^{2}} \begin{bmatrix} v_{\alpha_{1}+} & v_{\beta_{1}+} \\ v_{\beta_{1}+} & -v_{\alpha_{1}+} \end{bmatrix} \begin{bmatrix} i_{p+1}^{*} \\ i_{q+1}^{*} \end{bmatrix},$$
(14)

$$\begin{bmatrix} i_{\alpha}^{*} \\ i_{\beta}^{*} \end{bmatrix} = \frac{1.5V_{\text{base}}}{v_{\alpha1-}^{2} + v_{\beta1-}^{2}} \begin{bmatrix} v_{\alpha1-} & v_{\beta1-} \\ v_{\beta1-} & -v_{\alpha1-} \end{bmatrix} \begin{bmatrix} i_{p-1}^{*} \\ i_{q-1}^{*} \end{bmatrix}.$$
 (15)

In these equations, $v_{\alpha\beta1}$ is the fundamental component of the grid voltage. The subscript + and - indicate positive and negative sequences, respectively.

Equations (14) and (15) work correct in ideal systems; however, in faulty situations, the amplitude of the voltage, which is at the denominator, can be very small. Therefore, (14) and (15) do not work well in fault situations due to the generation of current references with undesirable high amplitudes. [20, 38] tried to solve this drawback by modifying denominator but the solutions are complex to practical implementation. In this paper, the following relationship is proposed to determine the current reference in the SRF:

$$\begin{bmatrix} i_{\alpha_{+}}^{*} \\ i_{\beta_{+}}^{*} \end{bmatrix} = \begin{bmatrix} \cos \theta_{+} & \sin \theta_{+} \\ \sin \theta_{+} & -\cos \theta_{+} \end{bmatrix} \begin{bmatrix} i_{p_{+}}^{*} \\ i_{q_{+}}^{*} \end{bmatrix}$$
$$= \underbrace{\frac{1}{\sqrt{(v_{\alpha_{1}+})^{2} + (v_{\beta_{1}+})^{2}}} \begin{bmatrix} v_{\alpha_{1}} & v_{\beta_{1}+} \\ v_{\beta_{1}+} & -v_{\alpha_{1}+} \end{bmatrix}}_{T^{+}} \begin{bmatrix} i_{p_{+}}^{*} \\ i_{q_{+}}^{*} \end{bmatrix},$$
(16)

$$\begin{split} & \begin{bmatrix} i_{\alpha_{-}}^{*} \\ i_{\beta_{-}}^{*} \end{bmatrix} = \begin{bmatrix} \cos \theta_{-} & \sin \theta_{-} \\ \sin \theta_{-} & -\cos \theta_{-} \end{bmatrix} \begin{bmatrix} i_{p_{-}}^{*} \\ i_{q_{-}}^{*} \end{bmatrix} \\ &= \underbrace{\frac{1}{\sqrt{(v_{\alpha_{1-}})^{2} + (v_{\beta_{1-}})^{2}} \begin{bmatrix} v_{\alpha_{1-}} & v_{\beta_{1-}} \\ v_{\beta_{1-}} & -v_{\alpha_{1-}} \end{bmatrix}}_{T^{-}} \begin{bmatrix} i_{p_{-}}^{*} \\ i_{q_{-}}^{*} \end{bmatrix},$$
(17)

In this method, according to (16) and (17), the current reference is built by using the outputs of a DSOGI-FLL. The main advantage of the proposed method is that the current reference in SRF is directly calculated from active/reactive current set-points without converting to power references, which causes matching with grid codes as much as possible.

3.2 Inner current loop

The AC model of the GSC is shown in Fig. 5 where $V_i(s)$, $V_g(s)$, g_i and i(s) are the converter output voltage, the grid voltage, the converter gain $(0.5V_{dc})$, and the converter output current, respectively. The delay of computation is modelled by e^{-sT_d} , where T_d is related to the sampling time. The resistor in series with C_f is modelled as r_d . In this system, V_i and V_g are accounted as a control input and a disturbance, respectively. The converter current *i* is the output of this system. In this converter, the current and the PCC voltage are measured where the delay of the transducers are modelled as first-order low-pass filters. $T_i = 280 \,\mu s$ and $T_v = 310 \,\mu s$ are the delay of voltage and current transducers, respectively.

In the inner current loop, two functions are performed in addition to the implementation of a PR controller: active resonance damping and system stabilisation by using voltage feedforward and phase shifting.

According to Fig. 5, a PR controller with the following relationship operates as the current controller in the inner loop:

$$PR = k_p + \frac{2\omega_c k_i s}{s^2 + 2\omega_c s + \omega_0^2},$$
(18)

where k_p , k_i , and ω_c are the proportional gain, the resonant gain and the resonance bandwidth, respectively. The PR controller is proposed to ensure the steady-state reference tracking performance and the fast dynamic response. A non-pure resonant term with resonance bandwidth $\omega_c = 2$ rad/s is used in the PR controller to avoid stability problems that can be associated with the infinite gain at the resonance frequency. Also, the voltage feedforward with coefficient k_f is used to improve transient response and to damp unstable dynamics related to the resonances.

To set the parameters of the controller, a set of simplification are performed first. Hence, the system model with voltage feedforward can be simplified as shown in the following:

$$i(s) = Y'_{i}(s)V'_{i}(s) + Y'_{g}(s)V'_{g}(s),$$
(19)

$$Y'_{i}(s) = \frac{e^{j\phi_{c}} e^{-sT_{d}} (s^{2}L_{g}C_{f} + C_{f}(r_{g} + r_{d}) + 1)}{\Delta(s)},$$
(20)

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$$Y'_{g}(s) = \frac{(1 + sr_{d}C_{f})((1 - k_{f}e^{j\phi_{c}}e^{-sT_{d}}) + sT_{v})}{\Delta(s)},$$
 (21)

$$\begin{split} \Delta(s) &= s^{4}L_{\rm f}C_{\rm f}L_{\rm g}T_{\rm v} \\ &+ s^{3}(L_{\rm f}C_{\rm f}L_{\rm g} + T_{\rm v}C_{\rm f}(r_{\rm g}L_{\rm f} + r_{\rm d}(L_{\rm f} + L_{\rm g}))) \\ &+ s^{2} \begin{pmatrix} C_{\rm f}(r_{\rm g}L_{\rm f} + r_{\rm d}L_{\rm f} + r_{\rm d}L_{\rm g}) + T_{\rm v}(r_{\rm g}r_{\rm d}C_{\rm f} + L_{\rm f} + L_{\rm g}) \\ &- k_{\rm f}\,{\rm e}^{{\rm j}\phi_{\rm c}}\,{\rm e}^{-sT_{\rm d}}r_{\rm d}C_{\rm f}L_{\rm g} \end{pmatrix} \right) (22) \\ &+ s((1 - k_{\rm f}\,{\rm e}^{{\rm j}\phi_{\rm c}}\,{\rm e}^{-sT_{\rm d}})(r_{\rm g}r_{\rm d}C_{\rm f} + L_{\rm g}) + r_{\rm g}T_{\rm v} + L_{\rm f}) \\ &+ r_{\rm g}(1 - k_{\rm f}\,{\rm e}^{{\rm j}\phi_{\rm c}}\,{\rm e}^{-sT_{\rm d}}), \end{split}$$

where V'_i is the output of the current controller. According to the Routh-Hurwitz stability criterion, if any coefficient of the characteristic equation is zero or negative, the system has at least one root with a non-negative real part and it is unstable. Based on (22) and the Routh-Hurwitz criterion, the voltage feedforward (k_f) gain must be lower than one. However, the exact value for this gain should be determined. To find the proportional coefficient (k_p) of the PR controller, the PM and bandwidth criteria will be used. The crossover frequency f_c is set usually to be lower than the 10% of the equivalent switching frequency, considering the effect of highfrequency noise. In turn, the cutoff frequency filter f_r is usually designed in the region from 25 to 50% of the equivalent switching frequency to ensure an effective harmonic suppression and an excellent dynamic response. The resonant coefficient (k_i) of the PR controller is selected based on the steady-state error at the fundamental frequency.

In Figs. 6–8, the open-loop response, the closed-loop response, and the effect of the grid voltage on the converter's current are shown for $k_p = 1.5$, $k_i = 80$ and an SCR = 5. From the steady-state error and the resonant coefficient point of view, the magnitude of the open-loop response in fundamental frequency $f_0 = 50$ Hz is bigger than 50 dB; thus, the steady-state error of tracking in $f_0 = 50$ Hz is lower than 1%.

By selecting a proportional coefficient and a feedforward gain, the following features would be covered: fast dynamic response, high stability margin and resonance elimination. It can be seen from Fig. 6, in open-loop response, that increasing feedforward gain leads to an increase of bandwidth, but to decrease the PM and the attenuation of the resonance.

The reduction in the PM leads to the creation of a peak around the cutoff frequency in the closed-loop response, as shown in Fig. 7. By increasing the feedforward gain, the magnitude around the cutoff frequency and the resonance frequencies get amplified and dropped off, respectively.

In Fig. 8, the effect of the grid voltage on the converter's current is shown. Therefore, the voltage feedforward can be used to reject disturbances around the fundamental and resonance frequencies. As it is proven in the plot, by increasing the feedforward gain, the grid voltage will have a significant impact on the converter current. The cutoff frequency is within 200–250 Hz. As a result, the effect of the grid voltage harmonics in the converter's current will be higher in this area.

Therefore, it can be concluded from Figs. 6–8 that the voltage feedforward has a dual behaviour, and it must be selected based on a compromise between stability and resonance elimination. The main constraints for setting the feedforward gain selection are: (i) the system becomes unstable without voltage feedforward due to the occurrence of resonance in locations with low SCRs; (ii) when feedforward gain increases, the peak amplitude of the resonance will be declined. However, by increasing the feedforward gain, some peaks appear around the cutoff frequency in the closed-loop response, due to the reduction of the PM in the open-loop response. Therefore, the best value for the feedforward gain is around 0.5, by taking into account the constraints in the open-loop response, the closed-loop response and the effect of the grid voltage in the current bode diagrams.

To enhance stability, a new phase shifter is proposed in (23) to increase PM and to improve stability:

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Fig. 6 *Bode diagram for SCR = 5: open-loop response*



Fig. 7 Bode diagram for SCR = 5: closed-loop response



Fig. 8 Bode diagram for SCR = 5: effect of the grid voltage in the converter's current



Fig. 9 Bode diagram for SCR = 5 with phase shifter: open-loop response

$$1 e^{j\phi} = \begin{bmatrix} \cos\phi & -\sin\phi \\ \sin\phi & \cos\phi \end{bmatrix},$$
 (23)

This phase shifter is used between the current controller and the SVPWM module to improve the PM of the system and to damp unstable dynamics. Besides, this phase shifter can be used to compensate for the delays of feedback signals to improve the performance of the overall system. In such a way, the delays of transducers are mitigated by adding a phase shifter to the feedback currents and voltages in Fig. 5. The effect of using phase shifters on the bode diagrams are shown in Figs. 9–11.

In the open-loop response, shown in Fig. 9, it can be seen that the phase shifter leads to a small increase of the bandwidth, but the improvement in the PM is significant. It should be mentioned that it does not have any effect on the resonance location. According to Fig. 10, using phase shifter smoothes the magnitude of the closedloop response, removes undesired peaks and improves stability. Also, in Fig. 11, the results display that phase shifter works well and decreases the effect of the grid on converter current around the bandwidth frequency (200 Hz).



Fig. 10 Bode diagram for SCR = 5 with phase shifter: closed-loop response



Fig. 11 Bode diagram for SCR = 5 with phase shifter: effect of grid voltage on converter current



Fig. 12 Simulation results under normal grid situations for SCR = 4(a) The voltage of the high voltage side of the transformer, (b) Actual and reference currents in the stationary reference frame, (c) PCC voltage, (d) Converter current, (e) Grid current, (f) Active and reactive powers, (g) DC link voltage, (h) The amplitude of positive and negative sequence voltages for PCC

4 Simulation results

This section presents the simulation results derived from four different case studies carried out to evaluate the performance of the proposed control scheme with a weak grid (SCR = 4). The parameters of 4 MVA GSC are listed in Table 1. The nominal dc-link voltage of the converter is 1150 VDC. The GSC is connected to the grid through a Dyn1 30/0.69 kV three-phase transformer with a 6% impedance. The maximum acceptable converter current I_{max} is 7200 A (1.5211 p.u.) and $V_{i\text{max}}$ is considered $V_{dc}/\sqrt{3}$ (1.1785 p.u.). The SCR of the grid from the high voltage side of the transformer and X/R of grid impedance are chosen to be 4 and 7, respectively. The active reference power is increased by 160 MW/s rate, and it is decreased immediately by step function due to the limitation of the input power source. The droop coefficients $k_{\nu\pm}$ set 2 and $V_{\text{band}\pm}$ is considered to be 0.1 p.u in (1) and (2) according to VDE-AR-N 4120. According to Fig. 1, dynamic braking resistors

and a dc chopper installed on the dc bus to help regulate the dc bus voltage during transients and grid faults.

- Start-up and power reference change at normal grid conditions: The simulation results considering a weak grid with SCR = 4 are shown in Fig. 12. The simulation has three stages: first, start-up until t = 0.1 s; then, increase input power to 4 MW from t = 0.1 s until t = 0.2 s by 160 MW/s rate; finally, the input power decreases to 2 MW immediately at t =0.3 s. Results presented in Fig. 12g prove that DC bus voltage is regulated around 1150 V during the power variation and also, according to Fig. 12b the current references in $\alpha\beta$ reference frame increase and decrease proportionally to input power and they are tracked by the current controller without any overshoot and with zero steady-state error. Figs. 12c and d show the converter current and the grid current are sinusoidal with no dc component. Also, it should be noted from Fig. 12a that increasing the active power with a smooth rate does not affect the PCC voltage, but the PCC voltage changes a little at the time of reducing the active power. THD of HV voltage and grid current are 4.5 and 1.61%, respectively. All these measurements fulfil what is required by the standards. Also, there is not any resonance phenomena in the voltage or the current.
- ii. An 80% deep balanced voltage sag ($V_{g+} = 0.2 p.u.$, $V_{g-} = 0$ p.u.) in the amplitude of the grid voltage: This voltage sag occurs between 0.25 and 0.4 s. The results obtained in this test are shown in Fig. 13. When the voltage fault occurs at t = 0.25s, the following actions are performed: (i) Positive sequence reactive current reference becomes negative value 0.84 p.u. according to the VDE-AR-N 4120 for grid support. (ii) The negative sequence reactive current setpoint is increased from zero because the fault is balanced. (iii) The positive sequence of active current setpoint is reduced to 0.545 to limit the converter's current.

In this case, a severe fault has occurred at the high voltage side of the transformer; as a result, the voltage of the three phases voltages decrease to 0.2 p.u.. The proposed scheme forces GSC to inject a suitable current to support the grid voltage. Therefore, the voltage at the PCC is compensated to 0.48 p.u. compared to the one measured at the high voltage side of the transformer (see Fig. 13h). According to Fig. 13b, the outer loop generates the current reference in the SRF (two sinusoidal current references) based on the positive and negative sequence of the PCC voltage and the active and reactive current references. The resulting current reference is followed with a zero-steady state error and a suitable transient response. It is worth to remark that the current of the converter has always been below the maximum value, hence within safety margins (see Fig. 13d). DC bus voltage is around 1150 V when the grid is normal, and it is clamped to 1230 V by DC chopper during the fault.

iii. Two-phase unbalanced 100% voltage sag for type E ($V_{g+} =$ 0.33 p.u., $V_{g^-} = 0.33$ p.u.): The grid voltages in phases b and c reduce to zero between 0.25 and 0.4 s. During the fault the value of the positive and negative sequence reactive current references i_{q+} and i_{q-} are set around 0.71 and 0.36 p.u., respectively. Therefore, i_{p+} is cropped by the current limiter part to zero to prevent the converter overcurrent trip. The voltage and current waveforms of the grid and the PCC, in this case, are shown in Fig. 14. In the high voltage side of the transformer, the voltages of a and b phases are reduced. Likewise, the voltage of the PCC is unbalanced and distorted similar to the high side of the transformer. As can be seen from Fig. 14b, despite the voltage at the PCC, the proposed outer loop generates the reference currents correctly. The PR controller later tracks this current reference without giving rise to any overshoot or steady-state error, endorsing thus the good performance of the proposed control scheme. It is clear from the current waveforms in Fig. 14d that the peak value 6000 A is below the maximum nominal value. In addition, the grid and the converter currents have satisfactory performance. As can



Fig. 13 Simulation results of fault situations for SCR = 4 in three-phase voltage sag (80%)

(a) The voltage of the high voltage side of the transformer, (b) Actual and reference currents in the stationary reference frame, (c) PCC voltage, (d) Converter current, (e) Grid current, (f) Active and reactive powers, (g) DC link voltage, (h) The amplitude of positive and negative sequence voltages for PCC



Fig. 14 Simulation results of two-phase-to-ground fault for SCR = 4(a) The voltage of the high voltage side of the transformer, (b) Actual and reference currents in the stationary reference frame, (c) PCC voltage, (d) Converter current, (e) Grid current, (f) Active and reactive powers, (g) DC link voltage, (h) The amplitude of positive and negative sequence voltages for PCC

be seen from Figs. 14*c* and *h* that the GSC helps to restore the PCC voltage and the amplitude of positive and negative sequence voltages in the PCC are $V_+ = 0.54$ p.u. and $V_- = 0.23$ p.u., respectively. The dc bus voltage during fault is kept under its maximum value 1230 V by DC chopper and after fault is regulated around 1150 V in Fig. 14g.

iv. One-phase unbalanced 100% voltage sag for type B ($V_{g+} = 0.66 \text{ p.u.}, V_{g-} = 0.33 \text{ p.u.}$): Only the grid voltage in phase a reduces to zero. The obtained results are shown in Fig. 15 where the voltage fault happens from t = 0.25 s until t = 0.4 s. The positive and negative reactive set-points are set 0.25 and 0.36 p.u., respectively. Then, positive sequence active current set point is declined to 0.59 p.u. to keep converter current

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Fig. 15 Simulation results of fault situations for SCR = 4 in one-phase voltage sag (100%)

(a) The voltage of the high voltage side of the transformer, (b) Actual and reference currents in the stationary reference frame, (c) PCC voltage, (d) Converter current, (e) Grid current, (f) Active and reactive powers, (g) DC link voltage, (h) The amplitude of positive and negative sequence voltages for PCC

under the safe zone. Both sides of transformer experience a voltage sag according to Figs. 15*a* and *c*, but voltage of low voltage side are improved by the converter and the amplitude of positive and negative sequences are $V_+ = 0.78$ p.u. and $V_- = 0.23$ p.u., respectively (Fig. 15*h*). Fig. 15*b* shows that the currents in $\alpha\beta$ are successively matched to the reference current with minimum distortions and spikes at the PCC voltage. In Fig. 15*d*, the converter current is sinusoidal without any dc component and its maximum is 5500 A when the voltage sags occur.

The obtained results demonstrate that control scheme can control converter according to recently issued standard especially VDE-AR-N 4120 in normal and faulty situations.

5 Experimental results

To validate the proposed control strategy and observe its behaviour under different real grid conditions, it was implemented in an experimental setup and tested in the lab. The experimental tests have been carried out in a test-bench built by Ingeteam Power Technology S.A. The test-bench allows testing full converter topology in low voltage (LV, 400 V_{rms}). The parameters and other hardware data are the same as the ones used in throughout the paper, listed also in Table 1. Two experimental cases have been selected in this validation stage, a non-distorted scenario, where a sudden active power step of 1 MW is performed and a faulty situation consisting of severe three-phase voltage sag. The experimental results obtained in these tests are presented in the following figures that show the transient performances of the two cases under weak grid conditions (SCR = 4). The PR regulator is tuned to provide a fast dynamic response, high stability margin and resonance elimination, as in the simulation study case. In the first test, an active power step of 1 MW is performed and the reactive power reference is set to zero. The phase to phase grid voltages and the currents delivered to the grid, both oscilloscope registers, are shown in Fig. 16. As it can be seen in the figure, the proposed PR controller offers a good response in front of sudden active power step, with minimal overshoot in current and short rise time, about 20-25 ms. There are not any resonance phenomena in voltage and current. The registers captured by the converter control unit are processed and shown in Fig. 17. The results shown in Figs. 17a and b present the current reference and the real measured current in the



Fig. 16 *Experimental evaluation in case of active power step* (*a*) *i_{abc}*injected currents to the grid: (500 A/division, 20 ms/division), (*b*) *V_{ab}* and *V_{bc}* PCC voltages: (200 V/division, 20 ms/division)



Fig. 17 *Experimental evaluation in case of active power step* (*a*), (*b*) Current reference and actual current in α and β axes, (*c*) Detected positive and negative sequence voltage amplitudes, (*d*) Converter output power

 α and β axes. As can be concluded from the plots, these references are tracked with the good transient response and zero steady-state error. Fig. 17*c* illustrates the minimal effect on PCC voltage and Fig. 17*d* confirms the good behaviour with the converter output.

In the second experimental case, a 100% balanced voltage sag in the amplitude of the grid voltage during 0.5 s is emulated. The response of the system in terms of grid voltages and injected currents, depicted in Fig. 18, also includes zoomed captures, Figs. 18*c* and *d*, centred around the appearance of the fault.

It can be concluded from the figure when the fault appears, the system has an acceptable transient response with respect to the expected line current overshoot and resonance phenomena.

Figs. 19*a* and *b* confirm that the reference current is properly followed. As shown in Fig. 19*c*, the amplitude of the positive sequence in the PCC is reinforced to 0.25 p.u. The power converter by injecting the positive sequence reactive current works supporting the voltage. From Fig. 19*d*, it can be noted that during the voltage sag, the active power is reduced according to the grid code and, during voltage sag recovery, this output power has a satisfactory response despite being a severe sag. According to the results shown in all the experiments, the good performance of the proposed control strategy has been experimentally validated.

6 Conclusions

This paper proposes a new control strategy, working in a SRF, to control high power three-phase grid-connected inverter based on two embedded loops: an outer current reference generation loop Pre fault Voltage sag type A Post fault Post fault

Fig. 18 Experimental evaluation in case of voltage sag type A

(a) i_{abc} injected currents to the grid: (700 A/division, 100 ms/division), (b) V_{ac} and V_{bc} PCC voltages: (200 V/division, 100 ms/division), (c) Detailed injected currents: (700 A/division, 20 ms/division) (A), (d) Detailed grid voltages: (200 V/division, 20 ms/division)



Fig. 19 *Experimental evaluation in case of voltage sag type A* (*a*), (*b*)Current reference and actual current in α and β axes, (*c*) Detected positive and negative sequence voltage amplitudes, (*d*) Converter output power

and an inner current loop. The proposed outer loop generates the current references that comply efficiently with the LVRT requirement of the grid codes, meanwhile protects the converter from operating points that could be harmful for its integrity. The developed inner loop of this paper has proposed a structure that combines PR controllers working in the stationary domain with a phase shifter and active damping blocks. By proposing the voltage feedforward and phase shifter in the control strategy, it can damp the unstable dynamics and improve PM, respectively. Moreover, realistic constraints such as communication delays and signal mismatching have been considered to issue a robust proposal.

The overall structure has been proven to be analytically feasible and effective in the simulation and experimental tests made. In a nutshell, the proposed control permits to generate positive and negative current references that comply with the codes protects the

IET Renew. Power Gener., 2020, Vol. 14 Iss. 12, pp. 2058-2067 © The Institution of Engineering and Technology 2020 converter and avoids reaching uncontrollability limits by controlling the reactive currents.

The simulation and experimental results, obtained using realistic data and parameters, as well as the possibility of testing the proposed system in a real 4 MVA test-bench has permitted to make the most realistic approach, endorsing the validity of the work presented.

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