Multibattery Charger System Based on a Three-Level Dual-Active-Bridge Power Converter

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***Abstract*—A charger for two batteries connected in series is presented in this work. From the three-phase grid, the batteries are charged through a three-level neutral-point-clamped ac-dc converter in cascade with a three-level dual active bridge converter. The system provides galvanic isolation and allows bidirectional power flow. A simple control strategy to charge the batteries is presented, based on the regulation of the common- and differential-mode components of the batteries' charging currents. With this control approach, each battery bank can be charged independently, allowing it to reach full battery bank capacity, even under different battery initial state-of-charge values or different battery nominal capacities. Moreover, the proposed control system also regulates the total dc-link voltage and the dc-link voltage balance in both dc-links of the system. The simulation results verify the feasibility of the proposed implementation and control system approach.**

Keywords*—Battery charger, current control, common-mode, differential-mode, dual-active-bridge, multilevel converter, voltage balance.

I. Introduction

Battery chargers (BCs) are required in many applications, from cell phones to industrial systems. At present, among these applications, it is worth highlight the importance of the BCs for electric vehicles.

BCs are typically classified into different categories [1], [2]: supplied from a single- or a three-phase power grid; on- or off-board; with or without galvanic isolation (GI); uni- or bidirectional power flow (BPF) capacity; and with two-level or multilevel (ML) technology. From the topological point of view, BCs are usually implemented with an ac-dc stage connected in cascade with a dc-dc stage [1], [2].

In comparison to the conventional two-level technology, the advantages of ML converters are well-known [3], even for low and medium power applications [4], despite the greater number of power devices required. However, in the literature, the ML technology is applied to BCs only in a reduced number of works. Furthermore, within these works, it is difficult to find a complete description of the BC topology and control, including the battery current control, the dc-link voltage balance control, and the dc-link control. For instance, in [5], a BC is implemented with an ac-dc ML converter in cascade with a dc-dc stage based on a hybrid NPC dual-active-bridge converter (DAB) and flying capacitor converter. However, no information about the ac-dc converter topology and control is reported. The dc-dc converter keeps the output voltage constant and the charging currents of the batteries are not directly controlled. In [6], the dc-dc converter of the BC is based on an asymmetric DAB, where an ML half-bridge is used in the primary side of the transformer but a conventional two-level full-bridge is used on the secondary side, not taking full advantage of the ML technology. Also, in the ac-dc stage, the dc-link voltage balance control strategy is not reported. In [7], a BC is implemented with ML ac-dc and dc-dc stages, where the dc-dc converter includes GI. However, the ac-dc converter is based on a Vienna rectifier, without BPF capacity. In the dc-dc stage, a half-bridge is used in the primary side of the transformer, with higher current ratings for the power devices than in a full-bridge, for the same given voltage level.

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This paper proposes a BC implemented with a three-level neutral point clamped ac-dc converter in cascade with a three-level DAB dc-dc converter, with GI and BPF capacity. A control approach is presented for the complete system, which requires coordination between the specific control strategy of each converter. The control of the total voltage and the voltage balance are carried out for the two dc-links present in the proposed implementation. Additionally, the charging current of each battery bank can be regulated independently, based on the regulation of the differential- and common-mode components of the charging currents. Therefore, each battery bank can reach full battery bank capacity, even under different battery initial state-of-charge values or different battery nominal capacities. Although this work is presented for three levels, it can be extended to *n*-levels, taking advantage of the ML technology and also increasing the number of battery banks to be charged independently, enhancing the overall capacity of the system.

II. Battery Charger Topology and Model

The topology and the switching model of the proposed BC are shown in Fig. 1. From the three-phase grid, an ac-dc stage is implemented with an inductive filter and a three-level neutral-point-clamped (NPC) converter [8] and, connected to the dc-link (A-Side dc-Link). This converter is labeled as the 3L-3P-NPC converter. Following the ac-dc stage, the dc-dc stage is connected in cascade, implemented with a three-level DAB topology [9], including a high-frequency transformer (HFT), resulting in another dc-link (B-Side dc-Link). This converter is labeled as the 3L-1P-DAB converter. Finally, two battery packs are connected. These battery packs build a battery bank. In the following, the models for the different parts of the proposed topology are described. Both dc-links are built with capacitors (C_{a1}, C_{a2}, C_{b1}, and C_{b2}), with their corresponding bleeding resistors (R_{Ca1}, R_{Ca2}, R_{Cb1}, and R_{Cb2}) in parallel, connected for safety reasons.

A. 3L-3P-NPC Converter Model

This model includes the equations of the ac-grid side and the 3L-3P-NPC converter. The equations of the ac side and the converter are shown in (1) and (2), and the A-Side dc-Link model in (3). The equations are expressed in the rotative

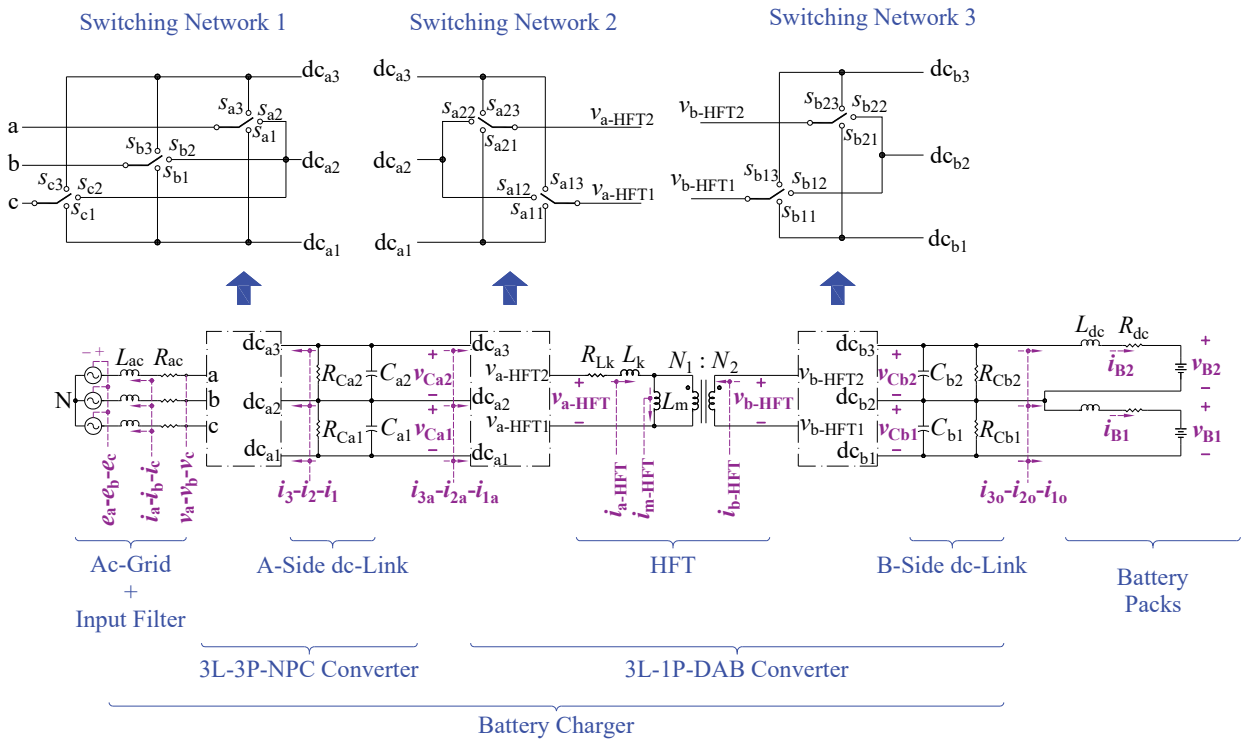

Fig.1. Proposed battery charger system. Topology and switching model.

dq frame, where the d axis is aligned with phase a of the grid.

$$\frac{\mathrm{d}i_\mathrm{d}}{\mathrm{d}t} = \frac{1}{L_\mathrm{ac}} \cdot \left\{-R_\mathrm{ac} \cdot i_\mathrm{d} + L_\mathrm{ac} \cdot \omega \cdot i_\mathrm{q} + v_\mathrm{d} - E_\mathrm{L}\right\} \quad (1)$$

$$\frac{\mathrm{d}i_\mathrm{q}}{\mathrm{d}t} = \frac{1}{L_\mathrm{ac}} \cdot \left\{-R_\mathrm{ac} \cdot i_\mathrm{q} - L_\mathrm{ac} \cdot \omega \cdot i_\mathrm{d} + v_\mathrm{q}\right\} \quad (2)$$

$$\frac{\mathrm{d}v_{\mathrm{DC_a}}}{\mathrm{d}t} = -\frac{2}{C_\mathrm{a}} \cdot \left\{\frac{1}{2} \cdot \frac{1}{R_{\mathrm{C_a}}} \cdot v_{\mathrm{DC_a}} + i_{3\mathrm{a}} + \frac{v_\mathrm{d} \cdot i_\mathrm{d} + v_\mathrm{q} \cdot i_\mathrm{q}}{v_{\mathrm{DC_a}}}\right\}, \quad (3)$$

where (v_d, v_q, i_d, i_q) correspond to the voltages (v_a, v_b, v_c) and currents (i_a, i_b, i_c) of the converter in dq frame respectively; E_L is the rms line-to-line voltage of the grid; ω represents the angular frequency line; $v_{\mathrm{DCa}} = v_{\mathrm{Ca1}} + v_{\mathrm{Ca2}}$ is the total voltage of the A-Side dc-Link; $i_{3\mathrm{a}}$ is the A-Side dc-Link current; (R_ac, L_ac) are the resistor and inductor of the input filter, respectively. To simplify the analysis, the equalities described in (4) and (5) have been assumed.

$$\begin{aligned} C_{\mathrm{a_1}} &= C_{\mathrm{a_2}} = C_\mathrm{a} \\ C_{\mathrm{b_1}} &= C_{\mathrm{b_2}} = C_\mathrm{b} \\ R_{\mathrm{C_{a_1}}} &= R_{\mathrm{C_{a_2}}} = R_{\mathrm{C_a}} \\ R_{\mathrm{C_{b_1}}} &= R_{\mathrm{C_{b_2}}} = R_{\mathrm{C_b}} \end{aligned} \quad (4)$$

$$\begin{aligned} v_{\mathrm{C_{a_1}}} &= v_{\mathrm{C_{a_2}}} = 0.5 \cdot v_{\mathrm{DC_a}} \\ v_{\mathrm{C_{b_1}}} &= v_{\mathrm{C_{b_2}}} = 0.5 \cdot v_{\mathrm{DC_b}}. \end{aligned} \quad (5)$$

B. 3L-1P-DAB Converter Model

Equations (6)–(10) represent the switching model of the 3L-1P-DAB converter. Expressions (6)–(8) are related to the dynamics of the HFT, while (9) corresponds to the model of the B-Side dc-Link. The switching functions f_{a2}, f_{b2}, f_{a3}, and f_{b3} are present in (6)–(9) and described in (10)

Here ($i_{\mathrm{a\text{-}HFT}}$, $i_{\mathrm{b\text{-}HFT}}$, $i_{\mathrm{m\text{-}HFT}}$, t_r) are the input current of the primary and secondary side of the HFT, the magnetizing

$$\frac{\mathrm{d}i_{\mathrm{a-HFT}}}{\mathrm{d}t} = \frac{1}{2} \cdot \frac{1}{L_\mathrm{k}} \cdot \left\{-2 \cdot R_{\mathrm{L_k}} \cdot i_{\mathrm{a-HFT}} - \right. \\ \left. -\left(f_{\mathrm{a_2}} + 2 \cdot f_{\mathrm{a_3}}\right) \cdot v_{\mathrm{DC_a}} + \left(f_{\mathrm{b_2}} + 2 \cdot f_{\mathrm{b_3}}\right) \cdot v_{\mathrm{DC_b}}\right\} \quad (6)$$

$$\frac{\mathrm{d}i_{\mathrm{b-HFT}}}{\mathrm{d}t} = \frac{1}{2} \cdot \frac{t_\mathrm{r}}{L_\mathrm{k}} \cdot \left\{2 \cdot R_{\mathrm{L_k}} \cdot i_{\mathrm{a-HFT}} + \right. \\ + \left(f_{\mathrm{a_2}} + 2 \cdot f_{\mathrm{a_3}}\right) \cdot v_{\mathrm{DC_a}} - \\ \left. - \frac{t_\mathrm{r} \cdot L_\mathrm{k}}{L_\mathrm{eq}} \cdot \left(f_{\mathrm{b_2}} + 2 \cdot f_{\mathrm{b_3}}\right) \cdot v_{\mathrm{DC_b}}\right\} \quad (7)$$

$$\frac{\mathrm{d}i_{\mathrm{m-HFT}}}{\mathrm{d}t} = -\frac{1}{2} \cdot \frac{t_\mathrm{r}}{L_\mathrm{m}} \cdot \left\{\left(f_{\mathrm{b_2}} + 2 \cdot f_{\mathrm{b_3}}\right) \cdot v_{\mathrm{DC_b}}\right\} \quad (8)$$

$$\frac{\mathrm{d}v_{\mathrm{DC_b}}}{\mathrm{d}t} = -\frac{2}{C_\mathrm{b}} \cdot \left\{-\frac{1}{2} \cdot \frac{1}{R_{\mathrm{C_b}}} \cdot v_{\mathrm{DC_b}} + f_{\mathrm{b_3}} \cdot i_{\mathrm{b-HFT}} - \right. \\ \left. -i_{3\mathrm{o}}\right\} \quad (9)$$

$$\begin{aligned} f_{\mathrm{a_2}} &= s_{\mathrm{a_{12}}} - s_{\mathrm{a_{22}}} \\ f_{\mathrm{a_3}} &= s_{\mathrm{a_{13}}} - s_{\mathrm{a_{23}}} \\ f_{\mathrm{b_2}} &= s_{\mathrm{b_{12}}} - s_{\mathrm{b_{22}}} \\ f_{\mathrm{b_3}} &= s_{\mathrm{b_{13}}} - s_{\mathrm{b_{23}}}. \end{aligned} \quad (10)$$

current, and the transformer turns ratio respectively; $i_{3\mathrm{o}}$ is the B-Side dc-Link current; (R_{Lk}, L_k) are the resistance and the leakage inductance of the HFT windings, and $L_{\mathrm{eq}} = L_\mathrm{k} \,//\, L_\mathrm{m}$; ($i_{\mathrm{B1}}$, i_{B2}) are the charging currents of each battery pack.

C. Battery Bank Model

The battery bank of the BC is represented by wires and battery packs. Expressions (11)–(15) correspond to the model of battery packs, as a function of their common-mode (CM) and differential-mode (DM) components [10].

Here (i_{DM}, i_{CM}) are the DM and CM components of i_{B1} and i_{B2}; (v_{B1}, v_{B2}) are the voltages of each battery pack; (R_{dc},

L_{dc}) are the resistance and inductance of the wires connecting the battery packs. The battery model used in this work is based on [10].

$$\frac{di_{DM}}{dt} = -\frac{1}{L_{dc}} \cdot \left\{ R_{dc} \cdot i_{DM} - v_{C_{b_{DM}}} + v_{DM} \right\} \quad (11)$$

$$\frac{di_{CM}}{dt} = -\frac{1}{L_{dc}} \cdot \left\{ R_{dc} \cdot i_{CM} - v_{C_{b_{CM}}} + v_{CM} \right\} \quad (12)$$

$$i_{CM} = \frac{1}{2} \cdot \left(i_{B_1} + i_{B_2} \right), i_{DM} = i_{B_1} - i_{B_2} \quad (13)$$

$$v_{CM} = \frac{1}{2} \cdot \left(v_{B_1} + v_{B_2} \right), v_{DM} = v_{B_1} - v_{B_2} \quad (14)$$

$$v_{C_{b_{CM}}} = \frac{1}{2} \cdot \left(v_{C_{b_1}} + v_{C_{b_2}} \right), v_{C_{b_{DM}}} = v_{C_{b_1}} - v_{C_{b_2}}. \quad (15)$$

III. Control System Description

The complete scheme of the proposed control system for the BC is shown in Fig. 3(a). The control goals are to regulate the charging currents of the batteries by controlling the B-Side dc-Link voltages, to regulate the A-Side dc-Link (total voltage and balance), and to regulate the power factor of the grid connection.

The controller of the 3L-3P-NPC converter is in charge of regulating the total A-Side dc-Link voltage (v_{DCa}) and to regulate the reactive power exchange with the grid (power factor control) and can be also in charge of keeping balanced the A-Side dc-Link capacitor voltages (v_{Ca1}, v_{Ca2}). The controller of the 3L-1P-DAB converter is in charge of regulating the charging currents of the batteries (i_{B1}, i_{B2}) and can be also in charge of keeping balanced the A-Side dc-Link capacitor voltages (v_{Ca1}, v_{Ca2}). Therefore, the A-Side dc-Link capacitor voltage balancing can be carried out only by the 3L-3P-NPC converter, only by the 3L-1P-DAB converter, or concurrently by both converters. The user can decide which option to choose to keep this voltage balance.

A. 3L-3P-NPC Converter Control Description

A conventional voltage-oriented control in the dq frame is used in the 3L-3P-NPC converter, as shown in Fig. 2(b), which is implemented according to (1)–(3) [11], [12]. The total A-Side dc-Link voltage (v_{DCa}) is regulated by a PI controller which provides the reference for the d-component of the grid current (i_d), also regulated by a PI controller. The q-component of the grid current (i_q) is regulated by a PI controller to control the reactive power flow and, hence, the grid power factor, typically unity power factor. The current controllers provide the v_d and v_q, which are then converted into α-β variables to obtain the modulation index m = sqrt(v_α+v_β) and the reference angle θ = atan(v_β/v_α) through a calculation function block (Calc. Function) [11].

The A-Side dc-Link voltage balance compensator [13] depicted in Fig. 2(c) is also implemented. This PI controller generates a signal that represents the control effort (k_2) required to reduce to zero the dc-link unbalance $v_{Caimb} = v_{Ca1} - v_{Ca2}$.

The switching strategy of the converter is a virtual space vector modulation [11]. As shown in Fig. 2(a), the signals m, θ, and k_2 enter the modulator block to generate the duty cycles of each leg of the converter. Finally, a distributor block produces the switching signals for switches.

B. 3L-1P-DAB Converter Control Description

The control scheme for this converter is shown in Fig. 2(d) and 2(e) [9], [10]. The switching strategy for this converter is shown in Fig. 3 and is based on the modification of switching angles for the shape of the voltages on the primary and secondary sides of the HFT proposed in [9].

In Fig. 3 the switching strategy proposed in [9] is presented, where the waveforms of the voltages on the primary and secondary side of the HFT ($v_{a\text{-HFT}}$, $v_{b\text{-HFT}}$) are shown; the voltage of the inductance L_k (v_{LK}) and the current $i_{a\text{-HFT}}$. With this switching strategy, five levels are produced in the voltages $v_{a\text{-HFT}}$ and $v_{b\text{-HFT}}$. Then, employing the control strategies shown in Fig. 2(d) and 2(e), the values of the switching angles α_{ao1}, α_{ao2}, α_{ai1}, α_{ai2}, α_{bo1}, α_{bo2}, α_{bi1}, and α_{bi2} are modified in order to regulate the voltages v_{Ca1}, v_{Ca2}, v_{Cb1}, v_{Cb2}, and the power transfer between A- and B-side of this converter by means of the phase shift angle ϕ regulation.

The control scheme in Fig 2(e) is the specific control of the charging currents i_{B1} and i_{B2} of the batteries. These currents are converted into DM and CM components (13), which are regulated by the i_{DM} and i_{CM} PI compensators.

The i_{CM} compensator provides the reference of the CM voltage v_{CM}, i.e., the total B-Side dc-Link voltage (12). Then, to control this CM voltage v_{CM}, the power transfer is regulated through the control of the DAB phase shift angle ϕ, by means of a PI compensator (ϕ-Compensator). That is, the CM current i_{CM} is controlled by regulating the total B-Side dc-link voltage through the phase shift angle ϕ regulation.

As the proposed controller provides the option of having different charging currents for each battery pack, there is a need to regulate the DM current component (14).

The i_{DM} compensator provides the reference of the DM voltage, i.e., the B-Side dc-Link voltage unbalances, which is regulated by means of a PI compensator (α_b-Compensator). The output of this controller generates the modification of the switching angles α_{bo1}, α_{bi1}, α_{bo2}, α_{bi2} to

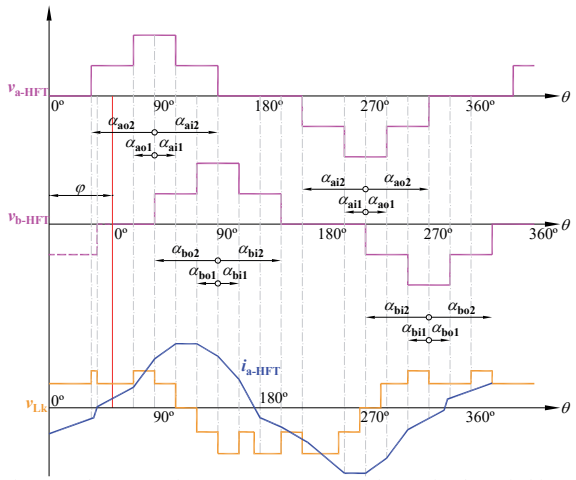

Fig. 3. Voltage waveform $v_{a\text{-HFT}}$, $v_{b\text{-HFT}}$, v_{Lk}, and $i_{a\text{-HFT}}$ for the switching strategy in [9].

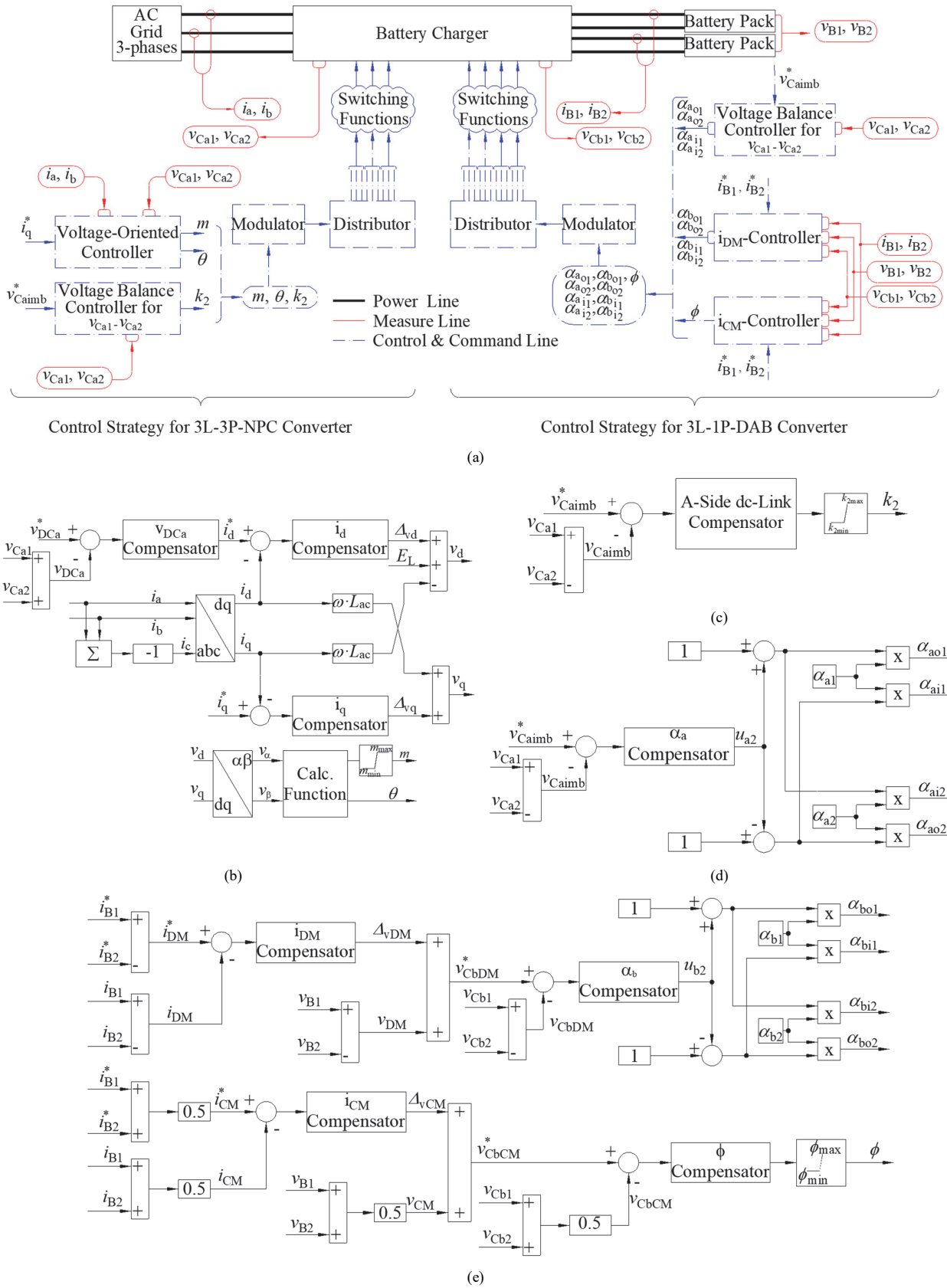

Fig. 2. Control system diagrams. (a) General battery charger control diagram. (b) Voltage-oriented controller for the 3L-3P-NPC converter. (c) A-Side dc-Link voltage balancing control of the 3L-3P-NPC converter. (d) A-Side dc-Link voltage balancing control of 3L-1P-DAB converter. (e) Control scheme of the 3L-1P-DAB converter for i_{DM} and i_{CM}, regulation.

TABLE I. SIMULATION VALUES

Parameters	Value
R_{ac}	10 mΩ
L_{ac}	1 mH
$R_{Ca} = R_{Cb}$	10 kΩ
$C_a = C_b$	800 μF
L_k	300 μH
L_m	10 H
R_{Lk}	50 mΩ
t_r	1
R_{dc}	20 mΩ
L_{dc}	2 μH

properly inject or extract electric charge towards or from the neutral point dc_{b2} (see Fig. 1) over a switching period, to lead the system to the reference v_{DM}, i.e. the reference B-Side dc-Link voltage unbalance that provides the desired DM current component.

IV. SIMULATION RESULTS

The simulation tests have been carried out with the lossless model shown in Fig. 1, using MATLAB-Simulink.

The proposed BC is connected to a three-phase AC grid with 400 Vrms line-to-line and f = 50 Hz. Both converters in the BC operate with a switching frequency f_s = 10 kHz. The simulation values are listed in Table I.

The voltage of each battery pack is 400 V. The parameters of the battery packs have been obtained experimentally [10].

The simulation results of the proposed BC and control are shown in Fig. 4. The initial condition for the BC is the following: The A-Side dc-Link voltage is unbalanced, v_{Ca1} = 480 V and v_{Ca2} = 320 V; The total A-Side dc-Link voltage reference is set at v^*_{DCa} = 800 V. The initial charge currents are zero $i_{B1} = i_{B2} = 0$ A and the reference charge currents are $i^*_{B1} = i^*_{B2} = 5$ A. The initial voltages of the B-Side dc-Link (v_{Cb1}, v_{Cb2}) are imposed by the voltages of each battery pack (v_{B1}, v_{B2}). Finally, it has been set that both converters are in charge of the A-Side dc-Link voltage balancing.

During the start-up, the charging currents of the batteries (i_{B1}, i_{B2}), shown in Fig. 4(a), present a good dynamic response, with an overshoot of 12.8% and 13.7% respectively and an equal settling time of 50 ms, with zero steady-state error. Fig. 4(b) shows the response of the CM and DM currents (i_{CM}, i_{DM}), presenting an overshoot of 13.2% and 18% and settling times of 30 ms and 45 ms respectively. The values achieved by i_{CM} and i_{DM} are 5 A and 0 A respectively. The total A-Side dc-Link voltage (v_{DCa}), shown in Fig. 4(c), exhibits an overshoot of 15% and a settling time of 25 ms. Furthermore, Fig. 4(c) also shows that the A-Side dc-Link voltage reaches the voltage balance at approximately 140 ms, where the A-Side dc-Link voltages (v_{Ca1}, v_{Ca2}) reach 400 V each. The overshoots presented by v_{Ca1} and v_{Ca2} are 15.7% and 20% respectively with an equal settling time of 120 ms. Finally, the B-Side dc-Link voltages (v_{Cb1}, v_{Cb2}) start balanced reaching both, a voltage of approximately 440 V. Also, v_{Cb1}, v_{Cb2} present a small ripple about 0.1 V and 0.2 V respectively, at switching frequency.

At 200 ms there is a step-change in the battery charging currents references (i^*_{B1}, i^*_{B2}). The new values are i^*_{B1} = 1.1 A and i^*_{B2} = 3 A. The dynamic responses of i_{B1} and i_{B2} show an overshoot of 2.8% and 25.3% with settling times of 20 ms and 10 ms respectively, see Fig. 4(a), with zero steady-state error. The currents i_{CM} and i_{DM}, see Fig. 4(b), reach the new values of 2.05 A and −1.9 A respectively. i_{CM} and i_{DM} show overshoots of 15.4% and 7.9% respectively and an equal settling time of 10 ms. Fig. 4(c) shows that v_{DCa} suffers a small disturbance with an overshoot of around 3.1% and a settling time of 30 ms, remaining its value at 800 V. The voltages v_{Ca1} and v_{Ca2} are kept balanced at 400 V each, presenting overshoots of 2.5% and 3.6% respectively and the settling time of 140 ms. For the case of v_{Cb1} and v_{Cb2}, see Fig. 4(d), present overshoots of 1.1% and 1.6% respectively, and the equal settling time of 60 ms. Moreover, a slight unbalance appears in v_{Cb1} and v_{Cb2} of 3 V and 2 V respectively, to provide the required DM current. v_{Cb1}, v_{Cb2} keep the small ripple about 0.1 V and 0.2 V respectively.

Finally, at 400 ms the reference of the total A-Side dc-Link voltage v^*_{DCa} is changed from an initial 800 V to 950 V. Fig. 4(c) shows that the transient response of v_{DCa} features an overshoot of 18% and a settling time of 30 ms. The voltages v_{Ca1} and v_{Ca2} keep the balance and reach a new value of 475 V, presenting the same overshoot and settling time of 18% and 20 ms. The voltages v_{Cb1} and v_{Cb2} keep their slight unbalance of around 3 V and 2 V respectively, no presenting overshoots, and settling times, and keeping their ripple (see Fig. 4(d)).

In summary, the simulation results show that more significant transient disturbances appear when the reference of the battery charging currents i^*_{B1} and i^*_{B2} are changed rather than when the reference v^*_{DCa} is changed. All overshoots and settling times present reasonable values according to the system under study. On other hand, when the references of the battery charging currents i^*_{B1} and i^*_{B2} are changed, the controller of the 3L-1P-DAB converter is able to manage it and its propagation to the A-Side dc-Link is very small. In addition, when the reference of the A-Side dc-Link total voltage v^*_{DCa} is changed, the controller of the 3L-3P-NPC converter is slower and the propagation of the transient to the B-Side dc-Link generates very small transients in the battery charging currents. Finally, it can be noted that the voltages v_{Cb1} and v_{Cb2} show small values of ripple that do not present problems to the converter. Therefore, it can be stated that the simulation results demonstrate both good transient and steady-state operation of the proposed BC and control scheme.

V. CONCLUSION

This paper presented a BC built by a three-level NPC and a three-level DAB connected in cascade. A control scheme has been proposed for the complete system, including the dc-link voltage control and dc-link voltage balance control for both the dc-links in the proposed BC. Also, the proposed control allows the independent regulation of the charging current of each battery bank, based on the regulation of the differential- and common-mode components of the charging currents. This feature allows using the full battery bank capacity, even under different battery initial state-of-charge values or different battery nominal capacities, without the need to add additional balancing circuits. It is expected that the proposed system can be extended to n-levels.

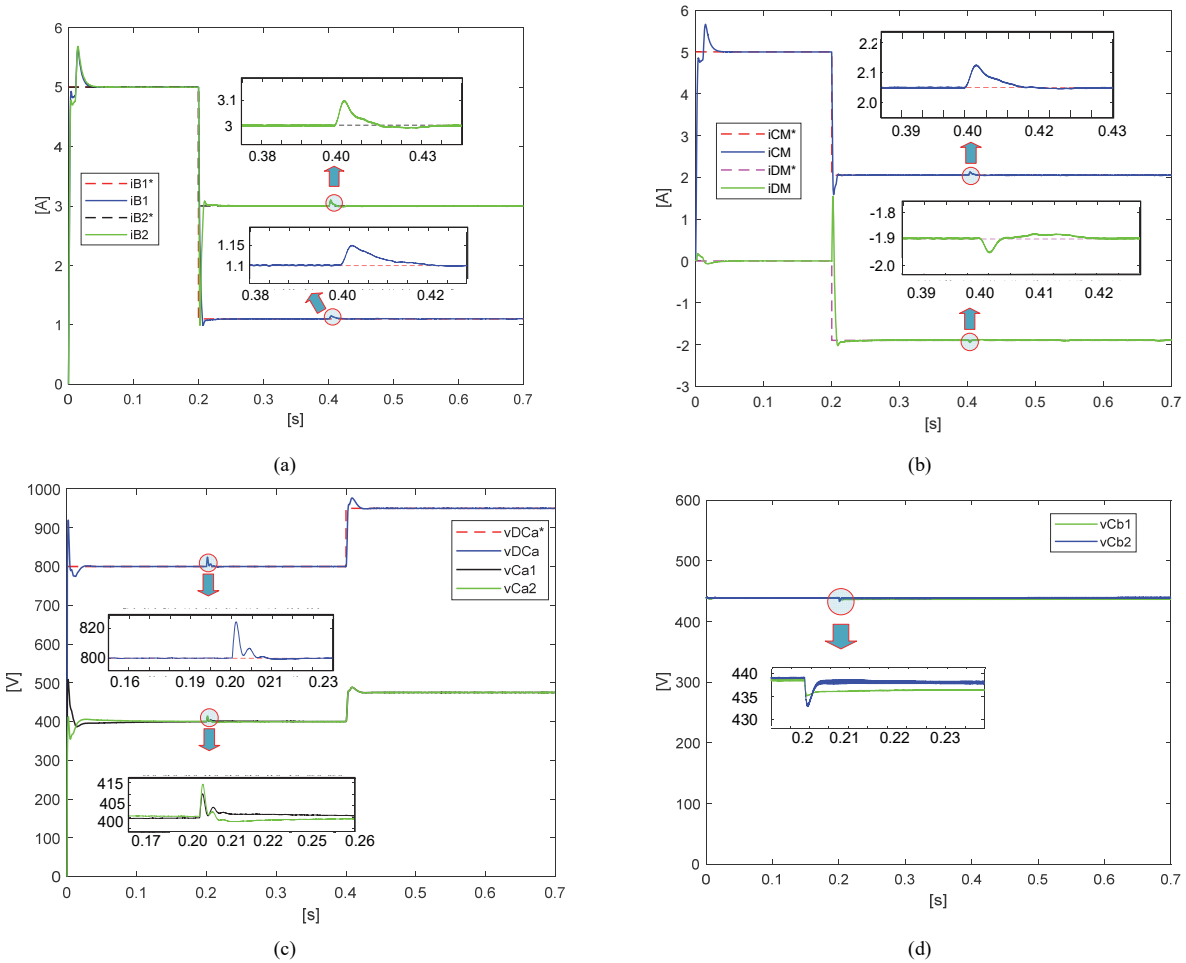

Fig. 4. Simulation of the BC under transient operation. Start-up, step change in i^*_{B1} and i^*_{B2} at $t = 200$ ms, and step change in v^*_{DCa} at $t = 400$ ms. (a) Charging currents of the batteries (i_{B1}, i_{B2}). (b) CM and DM currents (i_{CM}, i_{DM}). (c) A-Side dc-Link total voltage (v_{DCa}) and capacitor voltages (v_{Ca1}, v_{Ca2}). (d) B-Side dc-Link capacitor voltages (v_{Cb1}, v_{Cb2}).

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