An Improved Hybrid DC Circuit Breaker with Self-Adaptive Fault Current Limiting Capability

Huijie Lyu, Jiawei He*, Bin Li*, *Member, IEEE*, Ye Li, Daniel Westerman Spier, *Graduate Student Member*, *IEEE*, Eduardo Prieto-Araujo, *Senior Member*, *IEEE*, and Oriol Gomis-Bellmunt, *Fellow*, *IEEE*

Abstract—**The effective fault current limiting is very significant for the dc distribution system. However, the traditional dc fault current limiting method, i.e., directly installing dc reactor, may trigger negative impacts the system normal operation and fast isolation of the circuit breaker. Therefore, an improved hybrid dc circuit breaker with self-adaptive fault current limiting capability is proposed in this paper. Not only can it realize fault current limitation in a quick and efficient manner, but also ensures the continuous operation of the converter and the fault ride-through of the healthy network after the dc fault. In this sense, the requirements on the protection and arrester capacity are reduced. Compared with other types of fault current limiting methods, the proposed topology has the merit of few negative effects on system stability and transient response. It can effectively perform fault current limiting and fault isolation, with low conduction loss and low implementation difficulty. The working principle and advantages of the proposed topology are verified by experimental tests and simulation cases.**

Index Terms—**dc distribution system, fault current limitation, operation stability, isolation speed.**

I. INTRODUCTION

With the development of voltage source converter (VSC) technology, the dc distribution grid are getting ever-important with the modern drive towards the environment-friendly and sustainable power generations for flexible control, large-scale power supply capacity, high power quality, low power loss and no need for reactive power compensation [1] [2]. Existing researches show that dc distribution network can effectively coordinate the power grids and distributed generation thus giving full play to the value and benefits of distributed energy [3]. However, the engineering application of dc distribution network still suffers from several technical problems, including lower system damping, faster fault development speed and greater damage [4] [5], which put forward strict requirements for protection and fault isolation. To ensure validate fault ride-through of the remaining grid, it is required to detect, identify and isolate the fault line within hundreds of microseconds after the fault [6].

According to different working principles, DCCBs are mainly divided into three categories, i.e., mechanical circuit breakers, solid state circuit breakers (SSCBs) and hybrid circuit breakers. Mechanical circuit breakers have the lowest operation loss, but their operating speed cannot achieve the required specifications [7]. SSCBs are promising solutions in the distribution grid because of its simple control strategy and high operating speed, but the steady-state loss cannot be overlooked. Whereas, hybrid circuit breakers match the distributed grid better for the high operation speed [8-10].

To properly cut off the fault line, it is not enough to rely on the fast tripping of the circuit breaker itself. It is also vital for the protection system to distinguish the fault cable with selectivity before isolating the fault. Currently, the fastest operation speed of dc protection is within 2~3ms, making the selective fault isolation speed far from matching the fault development speed.

Valid dc fault current restricting technology can restrict the rapid rise of fault current and lower the requirements on protection and fault isolation operating speed, which is the key technology of a safe and reliable dc distribution system. The fault current limitation must satisfy the following requirements. 1) Sufficient fault current limitation capacity: the dc current shoots up after the fault, thus the fault current limitation should have a quick response to the event, while keeping the fault current beneath the threshold value until the DCCBs are tripped. 2) Little impact on normal dc grid operations: the fault current limitation should not present undesired impacts during normal dc network conditions. However, the dc system stability and its dynamic response speed have a poor performance when large dc reactors are installed (especially under power flow shifting). 3) Coordination with DCCB: DCCB is supposed to eliminate the fault current rapidly after it is tripped, but only installing a large dc reactor drastically prolongs fault current clearing period and increases the requirement on the metal oxide varistor (MOV) capacity.

Direct installation of dc reactor is one of the effective ways to restrict the fault current in dc distribution system [11], [12]. However, it suppresses the dynamic characteristics and operation stability of the dc system, as well as the fast fault current clearing [13], [14]. Therefore, the dc fault current limiters (FCL) suitable for dc distribution network are widely discussed, which could be classified into superconducting fault current limiters (SFCL) and FCL based on power electronic devices [15]. The SFCLs, including both the resistive and inductive SFCLs, have presented promising results in flexible dc grids due to their minor influence on the system normal operation [16] [17]. But, further research is required to ameliorate the fault current restricting speed and its recovery time once the fault is isolated. Besides SFCLs, FCLs based on power electronic switches are also another potential field of research for dc systems. To solve the problem of current limiting reactor restraining fault current clearing, reference [18] proposed a bridge-type fault current limiter topology, as shown in Fig. 1 (a). It is composed of an H-bridge with four series diode groups, a branch of series-connected dc reactor and dc-biased voltage source. This topology can avert negative impacts on system normal operation aroused by the dc reactor and speed up the fault current clearing. However, after the faulty cable is cut off, the bridge-type FCL needs a long time to absorb the fault energy preserved in the dc reactor, which

means that the recovery of the bridge-type FCL is very slow [19]. The authors of [20] introduced a hybrid current-limiting circuit (HCLC), which consists of an energy dissipation circuit (EDC) in parallel with the dc reactor, as shown in Fig. 1 (b). The EDC are made up with antiparallel thyristors abutted with a resistor in series. The semiconducting devices don't conduct unless the DCCB is tripped. Thus, the resistor R_r dissipates the fault current along with the DCCB's MOV, as a result the isolation speed of the failure can be improved by a large margin. Nevertheless, it does not consider the negative impact of dc reactor on the dc system normal operation. In the distribution network, the change of power flow becomes much more frequent, which further highlights this problem.
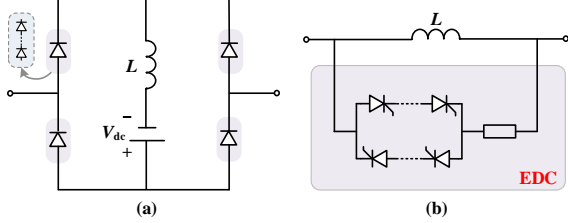

Fig. 1 Different kinds of existing fault current limiters for flexible dc grid: (a) bridge-type fault current limiter, (b) hybrid current-limiting circuit (HCLC).

To sum up, the direct installation of dc reactor deteriorates the dynamic response characteristic and system stability, the fast fault current clearing and the system recovery. The SFCLs needs to work in low temperature. The bridge-type FCL needs to work together with DCCB which increase the loss and cost in the industry. The HCLC needs additional operation during the power step which increases the complexity when used in the distributed grid where the change of power flow becomes much more frequent. Thus the SSCB with self-adapt fault current limiting capability (S-SSCB) becomes a technical proposal [5]. Furthermore, an improved hybrid dc circuit breaker with self-adaptive fault current limiting capability is proposed in this paper. It can limit the dc fault current effectively and quickly, and ensure the continuous operation of the converter and the fault ride-through of the healthy network after dc faults. The proposed topology has the merits of few negative impacts on the system transient response and operation stability, lower power loss, and easier engineering implementation. The paper is organized as: In Section II, the topology and control strategy of the proposed method is given. Then the parameter design principle and comparison analysis are provided in Section III. The scaled-down circuits are built and experimental tests are carried out to validate the operating principle and superiority of the proposed topology, in Section IV. Furthermore, in Section V, the supremacy of the proposed topology for utilization in the multi-terminal dc distributed grid is proved by the simulation cases. In the end, the conclusions are stated in Section VI.

II. THE SELF-ADAPTIVE SSCB AND ITS IMPROVED TOPOLOGY

A. Operating principle of the existing S-SSCB

The topology of S-SSCB [5] is shown in Fig. 2, which is composed of an H-bridge, a dc biased power supply and a dc reactor in series. During normal operation, the dc reactor is bypassed from the dc line, so the negative impact on the operation stability of the dc system is avoided. Under the fault condition, the dc reactor can be connected to the faulted circuit automatically and instantaneously to limit the fault current. It

can achieve the fast fault current limiting response, as well as the effective combination of fault current limiting and fault isolation, thus ensuring reliable fault ride-through of the remaining healthy system. It completely avoids the dc reactor's passive impacts on the transient response speed and operating steadiness of the distributed system. However, it requires a biased power supply, which greatly increases manufacturing difficulty, including the design of the dc biased power source, the protection of the power supply and so on. In addition, the existing topology triggers large conduction loss of electronic devices during normal operation, which makes it necessary to continue further improvements.

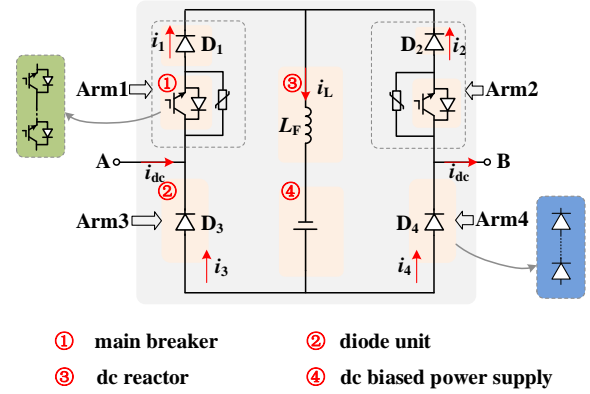| ① | main breaker | ② | diode unit |
| ③ | dc reactor | ④ | dc biased power supply |

Fig. 2 The topology of the S-SSCB.

B. The improved hybrid dc circuit breaker

To reduce the investment cost, manufacturing difficulty and operation power loss, an improved hybrid dc circuit breaker is presented in this paper, as shown in Fig. 3. Different from S-SSCB, a load branch made up with a series-connected fast mechanical switch, a diode and a load commutation switch (LCS), is added in Arm1 and Arm2 respectively. The LCS is built by the parallel-connected IGBT and a diode highlighted with blue color in Fig. 3. The biased power source is replaced with a resistor R parallel to the dc reactor L. It should be pointed out that, in Arm1, the load branch is directly installed in parallel with the diode group and the main breaker (formed by IGBTs) to reduce the conduction loss while the load branch of Arm2 is in parallel with the main breaker.

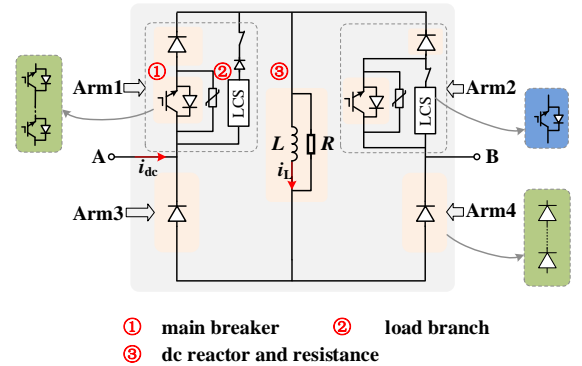| ① | main breaker | ② | load branch |
| ③ | dc reactor and resistance | | |

Fig. 3 The proposed topology.

The operation of proposed topology can be classified into four states, i.e., normal operation state, fault current limiting state, fault current clearing state and recovery state.

1) Normal operation state: The load branches of Arm1 and Arm2 are applied by conducting signals, while the IGBTs in the two main breakers are blocked. When i_{dc} flows from terminal A

to B, it covers the load branch of Arm1, dc reactor L and Arm4. The resistor R is bypassed by the dc reactor L. Arm2 and Arm3 are blocked due to the unidirectional conductivity of the diodes. Similarly, when the current flows from B to A, i_{dc} flows through load branch of Arm2, dc reactor and Arm3. Because there are only several semiconducting switches in the load branch, the conducting loss of proposed topology is much smaller than S-SSCB. Although the biased power source is removed, the application of R//L can also significantly minimize the negative impacts of the dc reactor on the stability during normal operation, which is analyzed in Section III.C.

2) Fault current limiting state: Under the condition of dc fault, the amplitude of dc current increases significantly. The dc reactor provides a reverse voltage Ldi/dt and the resistor limits the amplitude of the fault current, which function together to prevent the fault current from ruining the system.

The main factor limiting the isolation speed of the proposed topology is the switching speed of the fast mechanical switch. 'Pre-action strategy' is adopted to faster the fault current clearing stage. Generally, when a fault is detected, The IGBT in LCS is used to switch off the circuit and realize current commutation. The IGBTs of the main breaker are gated on, the LCS is blocked immediately and the open signal is applied on the fast mechanical switch. And the fault current is commutated from load branch to main breaker, as shown in Fig. 4 (b). If the protection has identified the fault properties as permanent and the DCCB needs to be tripped, the tripping signal is applied to the IGBTs in the main breaker. While the fault is just transient, the DCCB doesn't need to trip, then the current can be commutated back to the LCS by sending controlling signals, which faster the fault clearing speed of the proposed topology.
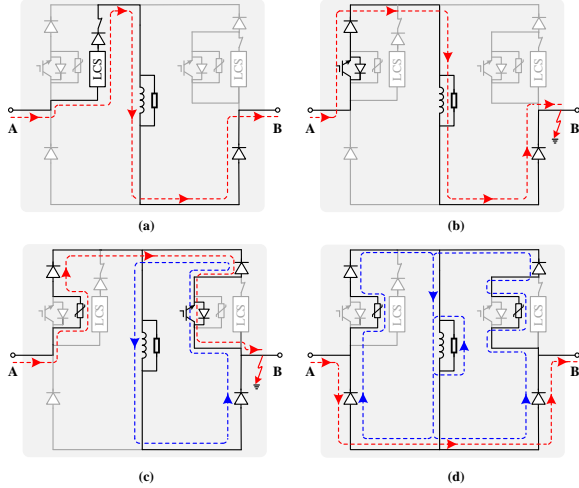

Fig. 4 Working principle of the proposed topology: (a) normal operation state, (b) fault current limiting state, (c) fault current clearing state, (d) recovery state.

3) Fault current clearing state: After the fault is detected and identified by the protection, the corresponding main breaker is tripped to cut off the fault. As shown in Fig. 4 (c), if the fault is on side B, the main breaker in Arm1 is tripped, yet the main breaker in Arm2 conducts (i.e., proposed topology installed on positive output). In contrast, if the fault point is located in side A, the main breaker in Arm2 is gated off while the main breaker in Arm1 still conducts.

To be specific, during forward fault (namely side A), the induction voltage of the reactor is directly exerted on Arm2, which the diodes unit of Arm2 should withstand. In engineering

practice, one diode and one IGBT are configured in the load branch of Arm1, because their voltage rating is the conducting voltage drop of the main breaker, which appears when LCS of Arm1 is turned off, the mechanical switch has not been totally opened, and the IGBTs of the main branch have been turned on. After the current is commutated from load branch to main breaker, the mechanical switch is opened. And the series-connected IGBTs are turned off only when the mechanical switch is opened completely. This means the alone IGBT in LCS only needs to withstand the conducting voltage of the IGBTs and diodes in main breaker. The opened mechanical switch bears the turned-off voltage of the IGBTs. During backward fault (namely side B, i.e., the outlet fault of the converter), the diode of load branch in Arm1 bears the voltage drop of the current limiting reactor. Due to the small capacity of MOV, the fault current limiting capability is limited. Nevertheless, the corresponding converter must be blocked right away when there is outlet fault, thus providing zero fault current to the system, and there is no need for current limiting for this converter. The fault current is mainly supplied by other converters in the system, which can be effectively suppressed by the proposed topologies at the outlets of those converters.

As Fig. 4 (c) shows, the current through dc reactor i_L circulates in $L//R$, Arm2 and Arm4. Meanwhile, i_{dc} flows through Arm1 and Arm2. This means that the dc reactor is bypassed from the fault circuit and the fault energy of the dc line is disconnected from the fault energy stored in the reactor. The connected-in MOV only needs to dissipate the former to clear i_{dc}. Therefore, the MOV capacity can be effectively reduced. T_{clear} of the dc reactor directly installed system, is

$$T_{clear}=I_{trip} \cdot \left(L_l+L \right) / \left(U_A - U_{dc}/2 \right) \tag{1}$$

where I_{trip} is the fault current at the tripping time, L_l the equivalent inductance of the fault line, L is the inductance of the dc reactor, U_A the clamping voltage of the MOV, and U_{dc} is the dc voltage of the system [5]. Generally, L_l is much smaller than L. With the proposed topology installed, the fault current clearing time T_{clear} is computed as

$$T_{clear}=I_{trip} \cdot L_l / \left(U_A - U_{dc}/2 \right) \tag{2}$$

Obviously, T_{clear} of the dc reactor directly installed system is much larger than T_{clear} with the proposed topology being installed. Therefore, the fault current clearing speed of the proposed topology is much faster than that of the DCCB combined with dc reactor only, which is very important for ensuring the normal operation of healthy grid and rapid insulation recovery performance of fault cable.

4) Recovery state: Since the dc fault is removed, the fault cable needs to be reconnected to the healthy grid. At the same time, the freewheeling current in the dc reactor needs to recover to I_{dcN}. It should be noted that I_{dcN} and i_L are dissimilar concepts. I_{dcN} is rated dc line current under normal operation, while i_L is the current flowing through L. Under normal operation and current limiting state, $I_{dcN} = i_L$. In the fault clearing period, the MOV is connected to the fault circuit, so i_{dc} drops rapidly while i_L decreases slowly because there is no MOV in the circuit of Arm2, L and Arm4. Therefore, before fault recovery, i_L is larger than i_{dc}.

During recovery state, the other main breaker needs to be gated off first. The fault energy stored in dc reactor is absorbed

by R and MOVs, and i_L decreases rapidly. When i_L approaches i_{dc}, Arm1 and Arm2 are turned on at the same time, that is, the proposed topology recovers completely, preparing for the next fault. It should be noted that in practical engineering, IGBTs are usually equipped with snubber circuits. When Arm1 and Arm2 need to be turned on, if the IGBT in load branch is directly turned on and the fast mechanical switch is reclosed, the snubber circuit capacitors of the IGBTs in the main breaker can only discharge through the MOV which leads to large time constant and difficult recovery of proposed topology. Therefore, when Arm1 and Arm2 need to be turned on, the IGBTs of main breaker should be turned on first, then the load branch is connected in, finally the main breaker is turned off again to complete the recovery process of proposed topology.

According to the above analysis, the recovery process can be divided into two states:

$i_{dc}<i_L/2$: Before recovery state, $i_{dc}=0$, because the fault line has been cut off by proposed DCCB. When it starts to recover, i_L is equally distributed in Arm1 and Arm2, as well as in Arm3 and Arm4. When $i_{dc}<i_L/2$, i_{dc} flows through Arm3 and Arm4 directly, as Fig. 4 (d) shows, so i_{dc} begins to increase rapidly. During this period, the polarities of the MOV's clamping voltages in Arm1 and Arm2 respectively are opposite, thus the voltage across the proposed DCCB $u \approx u_A - u_A = 0$. Therefore, it can be considered that the MOV has no impacts on the dc system. That is to say, as soon as the proposed topology enters the recovery state, the fault line is reconnected with the healthy grid. So the faulty grid can be recovered soon, and the recovery process of proposed DCCB has no effect on dc grid recovery.

$i_{dc} \geq i_L/2$: In the recovery state, i_L decreases rapidly and i_{dc} rises. When i_{dc} exceeds $i_L/2$, Arm3 is no longer on, and i_L can only flow through Arm2 and Arm4. The voltage over the proposed topology still meets $u \approx u_A - u_A = 0$. Therefore, its recovery process is still regarded having no effect on dc system.

Compared with the existing DCCBs, the proposed topology can quickly and automatically limit the dc fault current to an acceptable level before the protection tripping signal is received. The self-adaptive fault current limiting capability is manifested that the dc reactor bypasses the resistor under normal operation, leaving no impacts on the steady-state characteristics of the system (discussed in Section III.C). When a fault occurs, the dc reactor and resistor are automatically connected to the fault circuit, which can reduce the action speed requirements. In addition, compared with S-SSCB, the biased power supply is not necessary anymore, which significantly reduces the implementation difficulty.

III. PARAMETER DESIGN AND COMPARISON ANALYSIS

In this section, the design principle of the key parameters, such as the values of L and R, the number of the power electronic switches, are researched in depth. The power loss of proposed topology is analyzed and compared with three types of existing methods from the scale of the whole system. Furthermore, small signal analysis is carried out to give an insight of the proposed topology influence on system stability.

A. Parameter design

For parameters design, the voltage and current rating of the semiconducting switches and the capacity of MOVs are

thoroughly discussed in [5]. Therefore, the design values of current limiting L and R are mainly discussed in this section.
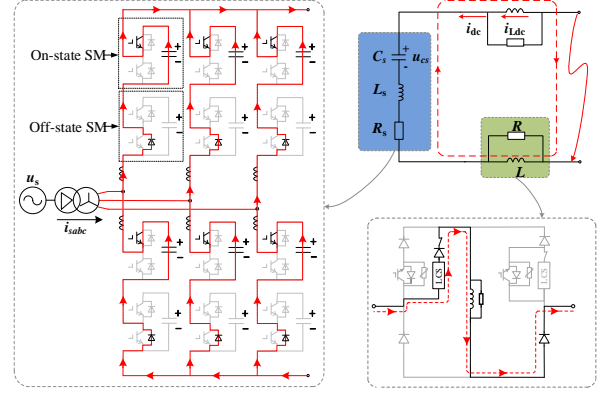

Fig. 5 Equivalent circuit of the MMC system with proposed topology installed.

In the proposed topology, the main function of L and R is to suppress the fault current after dc faults, so the values of L and R should be determined according to the fault current limiting requirement. Before it is tripped, the parallel connected L and R are always connected to the dc line. The equivalent circuit of MMC and proposed topology equals to the dc side of MMC connected in series with the parallel-connected L and R directly, as shown in Fig. 5 (omitting the equivalent resistance of L and all power electronic devices). The core destination of fault current limiting in dc system is to keep the continuous operation of the converter after the fault [18]. The arm current i_{arm} (instantaneous value) should be limited below the threshold value of the IGBT self-protection, namely $k_1 I_{IGBTN}$ (I_{IGBTN} is the rated current of the IGBT in the MMC; k_1 is defined as the overload coefficient, and $k_1 > 1$). So it should satisfy that $i_{arm} \leq k_1 I_{IGBTN}$, to realize the converter continuous operation after dc faults. In practice, the rated current I_{IGBTN} of the selected IGBT is a little larger than the rated arm current I_{armN} for security reasons, which means $I_{IGBTN}=k_2 I_{armN}$, where $k_2>1$. Considering that the arm current during the initial stage of a dc fault increases mainly due to the dc fault current, according to the relation of i_{arm} and i_{dc} proposed in [18], the dc current i_{dc} should be limited below the permitted level,

$$i_{dc} \leq 3\left(k_1 k_2 \sqrt{\frac{1}{9} + \frac{2}{9}\frac{1}{M^2\cos^2\varphi}} - \frac{2}{3}\frac{1}{M\cos\varphi} \right) i_{dcN} \qquad (3)$$

where i_{dcN} is the rated dc current of the converter station. M is modulation ratio while $\cos\varphi$ is the power factor [18]. That is to say, before the protection acts to trip the related proposed topology, the largest fault current the system can bear, namely I_{set}, which equals to the right part of equation (3). According to the equivalent circuit shown in Fig. 5, the transient characteristics with proposed topology can be equivalent to

$$\begin{cases} \dfrac{du_{cs}}{dt} = \dfrac{1}{C_s} i_{dc} \\[2mm] \dfrac{di_{dc}}{dt} = -\dfrac{R_s}{L_s} i_{dc} - \dfrac{1}{L_s} u_{cs} - \dfrac{R}{L_s} i_{dc} + \dfrac{R}{L_s} i_{Ldc} \\[2mm] \dfrac{di_{Ldc}}{dt} = \dfrac{R}{L} i_{dc} - \dfrac{R}{L} i_{Ldc} \end{cases} \qquad (4)$$

where u_{cs} is the voltage over the equivalent capacitor, and C_s, L_s, R_s are the equivalent capacitor, reactor and resistance of the converter where $C_s = 6C_{SM}/N$, $L_s = 2L_{arm}/3$, $R_s = 2R_{arm}/3$. i_{Ldc}

represents the current of L, while C_{SM} denotes the sub-module capacitor, L_{arm} is the value of arm reactor and R_{arm} is the equivalent resistance of each arm.

To further specify the design of R and L, the largest dc fault current I_{set} is calculated as the max current that the power electronic devices can tolerate in (4), which is also the max current level to which R and L together should limit. Since (4) is transcendental, Runge Kutta method is used to calculate the numerical value of instantaneous i_{dc} with different combination of R and L, since other parameters are known once the system is set. Then the values of i_{dc} are extracted at t_{trip} and plotted in a 3D-figure of i_{dc}, R and L. The red region refers to the R and L whose absolute value of i_{dc} are smaller than I_{set}. It means i_{arm} is limited below the upper limit before the DCCBs are tripped. That is to say, no power electronic devices are blocked by self-protection and the dc system can keep the continuous operation of the converter after the fault.
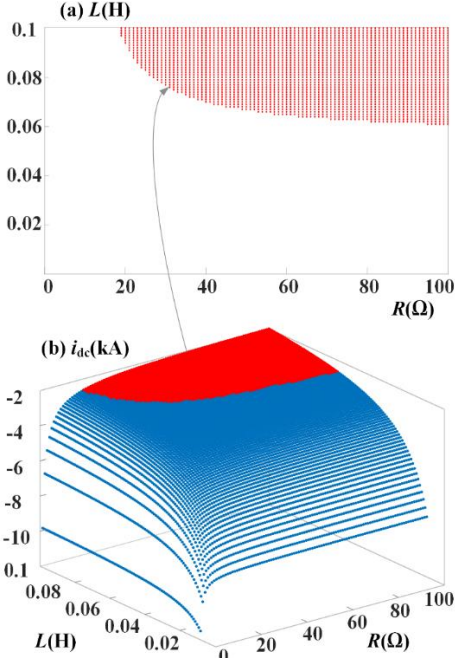

Fig. 6 Selection of the values of L and R in the proposed topology: (a) i_{dc}(kA) with different L(H) and R(Ω), (b) R and L meeting the requirement $i_{dc} \leq I_{set}$.

The following is an example of parameter design for a station (rated dc voltage ± 10 kV, 25 submodules, SM capacitor 16000 μF, arm reactor 43 mH, rated capacity 15 MW). Generally, the DCCBs are supposed to trip at 6ms after the dc fault, taking the fault identification and the protection operation time into consideration, so t_{trip} is set 6ms. The red area is the $L//R$ value combination which meets the current limiting requirement, shown in Fig. 6(a). I_{dc} (fed by S_1) corresponding to different $L//R$ at $t=t_{trip}$, is shown in Fig. 6(b). Considering that the cost of inductor is higher than the resistance, the smallest value of dc reactor is chosen, 0.06 H and then the resistance is chosen correspondingly, being equal to 100 Ω.

B. Loss analysis

The conducting loss of the bridge-type FCL, typical SSCB [8], shown in Fig.7, S-SSCB and proposed topology are analyzed in this section. The conduction losses of IGBT, diode and inductor are dominant in basic component losses [23], while the fast mechanical switch loss, the IGBT switching loss and the diode reverse recovery loss are ignored. The inductor

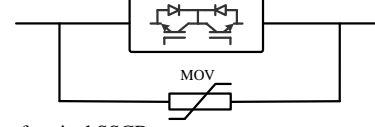losses of the above topologies equal to each other with the same i_{dc}, so the inductor loss is not discussed.

Fig. 7 The topology of typical SSCB

1) Loss of proposed topology:

There are m IGBTs and n diodes in each arm. When the power flows from A to B, Arm1 has 1 IGBT and 1 diode, and Arm4 has n diodes conducting, so $P_{loss} = P_{v1}+(n+1) P_{v2}$, where, IGBT loss: $P_{v1}=U_{0T}i_{dc}$, diode loss: $P_{v2}=U_{0D}i_{dc}$.

When the power flows from side B to side A, Arm2 has 1 IGBT and $(n+1)$ diodes conducting, and Arm3 has n diodes in on-state, so $P_{loss} = P_{v1}+(2n+1) P_{v2}$. It is worth mentioning that when installed in the rectifier outlet, loss is smaller. n diodes' conduction loss is saved compared with the inverter side.

2) Loss of S-SSCB: The dc biased power source is normally rooted in semiconducting devices, while the rated voltage of the switches is far less than that in the arms, which means that the conduction losses of the arm switches is much larger than that of the biased dc power source. Arm1 has m IGBTs and n diodes, and Arm4 has n diodes in on-state, so the conduction losses of S-SSCB are calculated as $P_{loss\_S-SSCB}=mP_{v1}+nP_{v2}$, where, $P_{v1}=U_{0T}i_1+U_{0T}i_2$, $P_{v2}=U_{0D}i_1+U_{0D}i_2+U_{0D}i_3+U_{0D}i_4$. Under normal operation, the current flowing path in the S-SSCB is Arm1, L and Arm 4 under the largest load current which equals to I_b. At this time, $i_1=i_4=I_b$, while $i_2=i_3=0$ [5].

3) Loss of T-SSCB: Under normal operation, the conduction loss is $P_{loss\_T-SSCB}= nP_{v1}$, where $P_{v1}=U_{0T}i_1$.

4) Loss of T-SSCB: Since bridge-type FCL cannot realize fault current clearing by itself, the conducting loss is calculated together with T-SSCB, which equals to $P_{loss\_bridge}= mP_{v2}+ P_{loss\_T-SSCB}$, where $P_{v2}=U_{0D}i_1+U_{0D}i_2+U_{0D}i_3+U_{0D}i_4$.

Taking the dc system shown in Section III.A for example, the fault current reaches 2666 A at t_{trip}=6ms. Taking 1.2 as the reliability factor, the IGBT's rated current should be larger than 3.2 kA which the main breaker needs to withstand. The blocking voltage U_A of the MOV should be greater than 1.5~2 times of system voltage (15 kV). Infineon IGBT FZ3600R12HP4 (rated 1.2 kV, 3.6 kA) is chosen. For the proposed topology, the rated voltage of LCS is the conducting voltage drop of all IGBTs and diodes in main breaker. The main breaker is equipped with 15 IGBTs, and the conduction voltage is 15*1.7= 25.5 V<1.2 kV, so 1 IGBT is used for LCS to meet the withstanding voltage. According to the datasheet, V_{CE} is about 1.7 V and V_F is about 1.8 V, when I_{dcN} = 0.75 kA. Therefore, the number of conducting electronic devices and the power losses of different SSCBs are listed in TABLE I.

TABLE I CONDUCTION LOSSES COMPARISON FOR DIFFERENT SSCB STRUCTURES

	Bridge-type FCL	T-SSCB	S-SSCB	Proposed method
IGBTs	30	30	15	1
Diodes	30	0	30	16
Loss(kW)	78.75	38.25	59.625	22.875

Compared with bridge-type FCL, S-SSCB and T-SSCB, the conduction losses of proposed topology are reduced by 55.875 kW, 36.75 kW and 15.375 kW respectively. With the

expansion of the system scale, the number of circuit breakers increases, and this advantage are more prominent.

C. Stability analysis

The operation stability of MMC with directly installed L, R and $L//R$ is analyzed and compared in this section based on small signal model theory.

1) Small signal model of MMC and control system: The small signal model includes the modeling of MMC circuit and control system, which has been researched in detail in [24] [25]. The dynamic model of MMC circuit can be expressed as

$$\dot{\Delta x} = A\Delta x + B\Delta u \tag{7}$$

where $x=[u_c, i_{dc}, I_{sd}, I_{sq}]^T$ represents the state variables, which are, submodule capacitance voltage, dc current, and dq axis components of ac current. $u=[U_{cd}, U_{cq}, \omega, U_{sd}, U_{sq}, U_{dc}]^T$ represents input variables, which are, dq-axis component of valve outlet voltage, ac frequency, dq-axis component of PCC point voltage, and dc voltage.

To analyze the small signal stability of the whole system, the MMC system and control models should be integrated into one state space equation, which can be written as

$$\begin{bmatrix} \dot{\Delta x} \\ \dot{\Delta x_c} \end{bmatrix} = \begin{bmatrix} A+B_1D_{c1}E & B_1C_c \\ B_{c1}E & A_c \end{bmatrix} \begin{bmatrix} \Delta x \\ \Delta x_c \end{bmatrix} + \begin{bmatrix} B_2 & B_1D_{c2} \\ 0 & B_{c2} \end{bmatrix} \begin{bmatrix} \Delta u_2 \\ \Delta u_{c2} \end{bmatrix} \tag{8}$$

where, $x_c=[x_1, x_2, x_3, x_4, x_5, x_{pll}]^T$ and $u_c=[I_{sd}, I_{sq}, U_{sd}, U_{sq}, P_{ref}, Q_{ref}]^T$. In x_c, $x_1 \sim x_4$ are the integrations of error quantities of the four PI regulators in the MMC controller, x_5 is the integration of U_{sq}, and x_{pll} is the output phase of the PLL. P_{ref}, Q_{ref} are the reference values of active power and reactive power. In addition, B_1 and B_2 are the first three columns and the last three columns of matrix B. B_{c1}, B_{c2} are the first two columns and the last four columns of matrix B_c. D_{c1}, D_{c2} are the first two columns and the last four columns of D_C matrix. Δu_1 and Δu_2 are the first three and the last three variables of Δu. Δu_{c1} and Δu_{c2} are the first two and last four variables of Δu_c. The detailed calculation methods of the state matrices can be found in [26].

2) Case study: According to the aforementioned analysis, the stability of the system can be evaluated by discussing the eigenvalues of the state matrix in small signal model (8). Based on Lyapunov's first rule, the whole system is stable only when all eigenvalues of the state matrix are negative.

Taking MMC parameters in Section III.A as example, $\Delta x_0=[\Delta u_{c0}, \Delta I_{dc0}, \Delta I_{Ldc0}, \Delta I_{sd0}, \Delta I_{sq0}]^T=[0.8, -0.75, -0.75, 1.22, 0]^T$; $\Delta u_0=[U_{cd0}, U_{cq0}, \omega_0, U_{sd0}, U_{sq0}, U_{dc0}]^T=[8.164, 0, 2pi*50, 8.164, 0, 20]^T$. Therefore, the root locus of MMC small signal model can be obtained, shown as Fig. 8.

Fig. 8 (a) shows the root locus under the condition only the reactor is installed, when the inductance varying from 10 mH to 200 mH. With the gradual increase of inductance, the real part of eigenvalue gradually approaches zero, and finally enters the positive axis. It means that with the increase of dc reactor, the stability of the system gradually becomes worse and the system finally loses stability.

Fig. 8 (b) shows the root locus under the condition that a resistor is fixed at the dc side of MMC, when the resistance changing from 1 Ω to 100 Ω. The eigenvalue always stays negative with resistance increasing, which means the system always keeps stable. It shows that the resistor has no impact on the stability of MMC-based dc system.
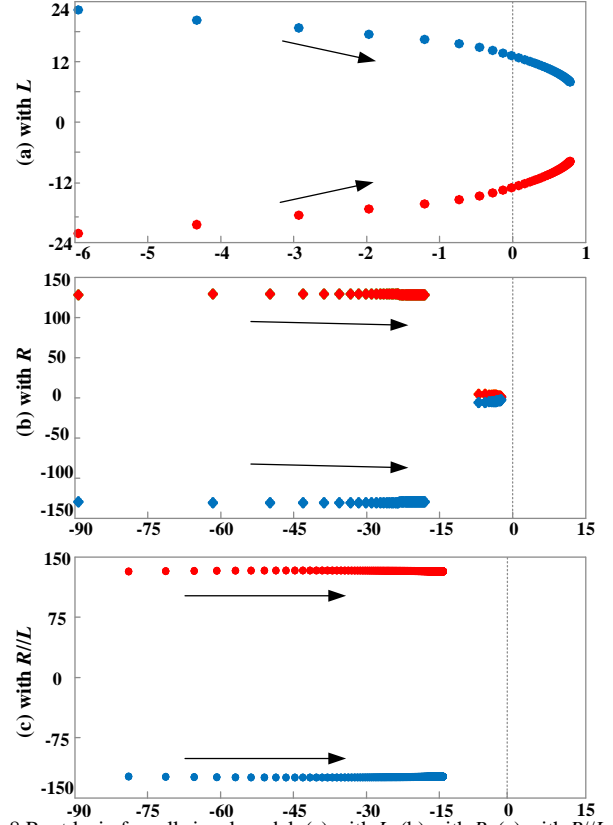

Fig. 8 Root loci of small signal model: (a) with L, (b) with R, (c) with $R//L$.

Fig. 8 (c) shows the root locus under the condition that parallel-connected dc reactor and resistor are installed at dc side of MMC. The inductance value of L is 200 mH, which is big enough to cause system imbalance when directly connected to the system. When the resistance value changes from 1 Ω to 100 Ω, the real part of the eigenvalue always remains negative. This means that the shunt resistor can significantly eliminate the adverse effect of dc reactor on the stability of MMC-based dc system. As analyzed above, during normal operation, the proposed topology eliminates the dc reactor's passive impacts on stability of dc system effectually.

IV. EXPERIMENT TEST

The proposed prototype and the scale-down test circuit, displayed in Fig. 9 are established to support the operating theory and advantages of the proposed topology in this section. The specific parameters of the experimental network are shown in Table II. Two capacitors in series are connected in parallel with a rectifier to establish the required dc voltage. The dc cable is emulated by series-connected resistors and reactors. Taking that the maximum heat dissipated by the MOV has the possibility of going beyond the allowable capability of a single MYG20D241K into consideration, two MOVs are paralleled. The dc load shift and dc fault are preset to come about separately, to validate the working principle and highlight the advantages of the proposed topology.

A. DC Load shifting

For this case study, the load resistance is set to change from 40 Ω to 20 Ω at t=0 s.
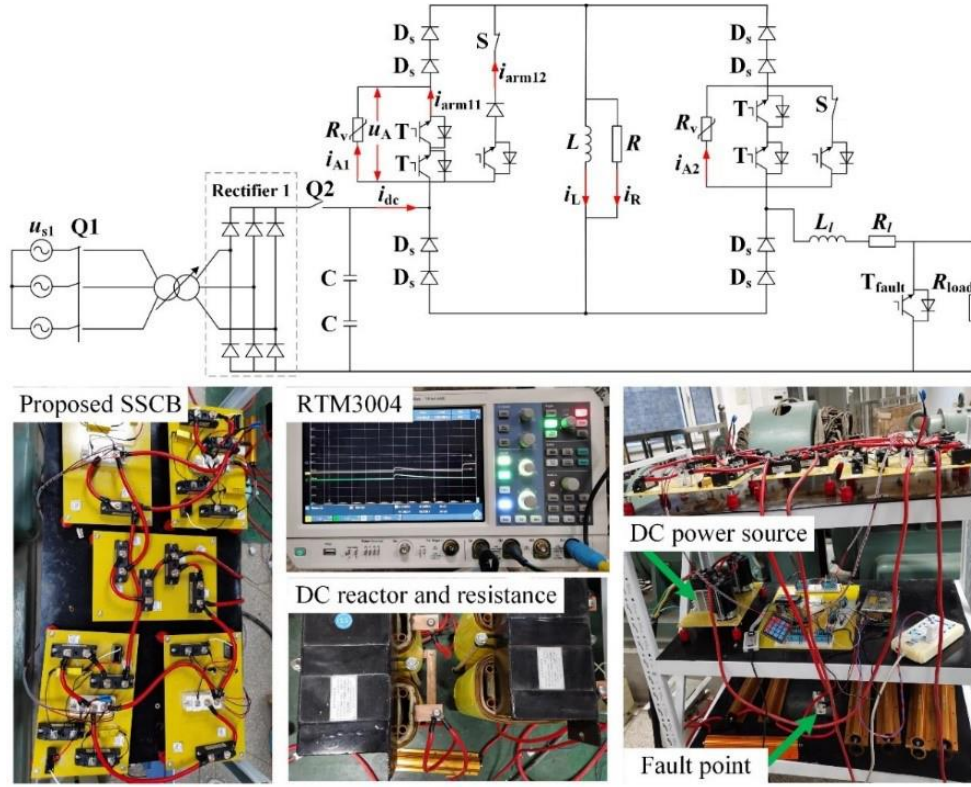
Fig. 9 Experimental circuit of the proposed topology.

TABLE II
PARAMETERS OF THE EXPERIMENTAL CIRCUIT

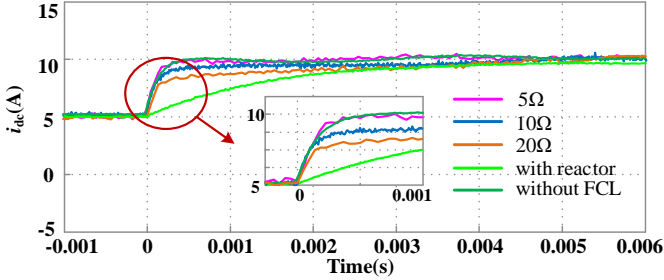| U_{dc} (V)	C (μF)	L (mH)	L_l (mH)	R_l (Ω)	R_{load} (Ω)	IGBT	Diode	MOV
200	4700	40	3	0.3	20	FF200R12KS4	MD200A1600V	MYG 20D241K

Fig. 10 Experiment outcomes of transient current process after the power step.

The outcomes of no fault current limitation experiment, directly installed dc reactor experiment and proposed topology with different shunt resistances (5 Ω, 10 Ω, 20 Ω) experiment are shown in Fig. 10. When no fault current limiter is installed, i_{dc} reaches the new steady state (i_{dc}=10 A) very quickly (in 0.5 ms). Nevertheless, the fault current rising rate as well as the steady-state value are limited effectively when the proposed topology is adopted. And the larger parallel resistance, the smaller the initial amplitude of dc current. When only the dc reactor is directly installed, the change rate of i_{dc} is very slow, and it takes about 5 ms to switch to the new steady state. Actually in the dc distributed grid, this phenomenon goes so far as to trigger grid collapse. Moreover, the limitation effect of dc reactor on the dc current fast changing is the essential reason why the dc reactor reduces the flexible dc grid transient response speed, and deteriorate the operation stability.

Therefore, the above case can indirectly verify that, in the flexible dc grid, the negative influence of the dc reactor on the system transient response speed, and then on the operation stability, can be avoided by the parallel structure of R//L of the proposed topology after the power step.

B. DC Failure

1) DC fault without FCL or with directly installed reactor:
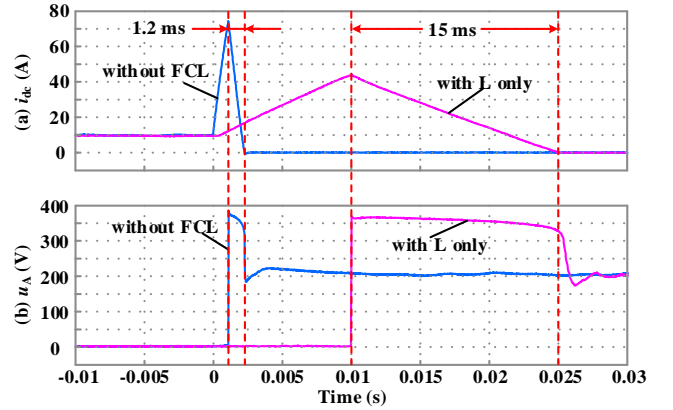

Fig. 11 Outcomes of bipolar fault experiment: (a) dc current i_{dc} (A), (b) T-SSCB MOV voltage u_A (V).

The bipolar dc fault is preset to occur at t=0 s. As shown in Fig.11 (a), the blue line stands for the case that no fault current limiter is installed and the fault current is cleared by a T-SSCB at t=0.001 s. And the pink line represents that a reactor (40 mH)

is configured and the related T-SSCB is set to trip at t=0.01 s. Although the tripping time of the second instance is deferred to t=0.01 s, the amplitude of the dc current is still much lower than that without FCL, which validates that the dc reactor has good current limiting performance. However, the clearing time of the second case (15 ms) is much longer than that without FCL (1.2 ms). Because the MOV of T-SSCB absorbs additional energy in the inductance during fault current limiting stage, it is much greater than the fault energy of the dc line. The rated capacity of MOV bears a dramatic rise (about 110 J).

2) Performance of the proposed topology:

As shown in Fig. 12(a), the proposed topology can also limit the fault current to an acceptable level after a dc fault. In the initial stage after the fault, the fault current limiting effect is closely related to the chosen value of the resistance because the current of the dc inductance cannot change immediately. The larger the resistance is, the better the fault current limiting effect performs. After the initial stage after the fault, the current limiting is functioned by the resistance and inductance together before the proposed topology is tripped.
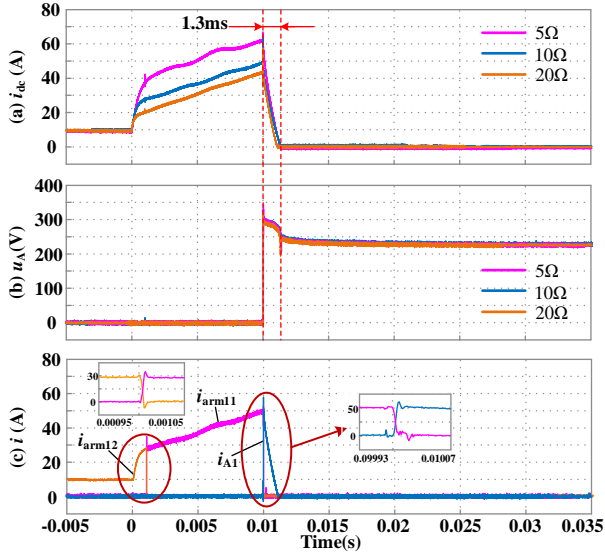

Fig. 12 Experimental outcomes of the dc bipolar failure with proposed topology (t_{trip}=0.01 s): (a) dc current i_{dc} (A), (b) proposed topology MOV voltage u_A (V), (c) dc current of main breaker i_{arm11} (A), dc current of LCS i_{arm12} (A), current of MOV in Arm1 i_{A1} (A).

After the proposed method is tripped, the fault current is quickly cleared (1.3 ms). This is because the dc reactor is bypassed from the fault circuit. And the fault energy of the dc line is separated from the fault energy stored in the reactor. The connected-in MOV only needs to dissipate the former to clear i_{dc}. Therefore, the proposed topology dissipates the negative impact of dc reactor on the fault current clearing. And the MOV capacity is effectively reduced, shown in Fig. 12 (b), where the energy dissipated by the MOV is merely around 9 J. Fig. 12 (c) shows the detailed current commutation process of 'pre-action strategy', fault current limiting period and fault clearance.

C. System Recovery

The faulty cable is supposed to be reconnected after the faulty point vanishes. Assuming the time to evaluate the faulty property is t_{pro}, the time to trip the DCCB is t_{int}, the period to clear the fault current is t_{clear}, the time to recover the insulation of the faulty line is t_{rec} and the period for the system to return to

stability is t_{res}. The T-SSCB strategy can reclose $t_{pro}+t_{int}+t_{clear}+t_{rec}+t_{res}$ after the failure, where t_{pro} is 1 ms, t_{int} is preset 10 ms, t_{clear} is 15 ms, t_{rec} is 80 ms. Considering that t_{res} is about 15 ms for i_{dc} to return to the load current level after T-SSCB is reclosed, presented in Fig. 13 (a), 121 ms is required from the fault moment to the grid recovery. Differently, i_{dc} can be quickly restored (in 1 ms) to the load current, when proposed topology is applied, using the afore-mentioned recovery strategy, as presented in Fig. 13. Therefore, compared with T-SSCB, proposed topology can save 20 ms~30 ms. After the main breaker of Arm2 is tripped at t=0.091s, the fault energy stored in dc reactor is absorbed by R and MOVs. Since the equivalent resistance of the MOVs is much larger than R, the fault energy stored in dc reactor is mainly dissipated by R, and the MOV only shares a small part, shown in Fig. 13 (b). At t=0.101s, the main breakers of Arm1 and Arm2 are turned on, i_{arm11} rises. At t=0.102s, the LCS of Arm1 and Arm2 are turned on while the main breakers are turned off at the same time. Fig. 13 (c) gives the detailed current commutation process between the main breaker and LCS of Arm1 during recovery state.
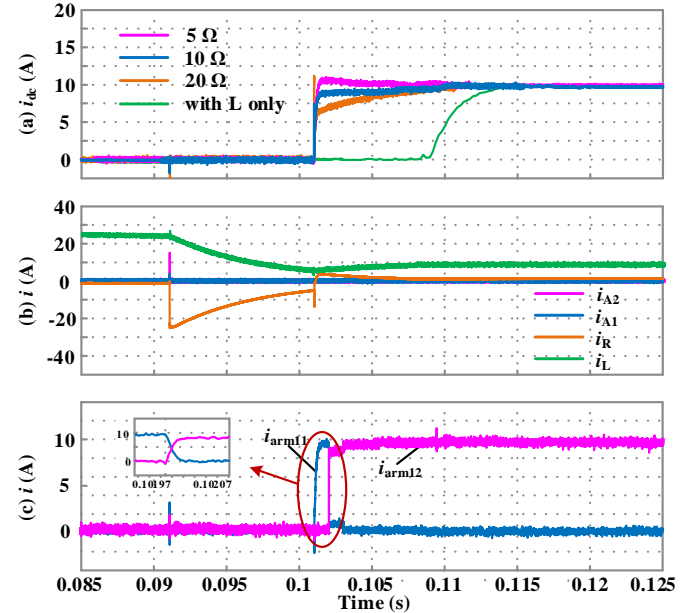

Fig. 13 Experimental outcomes of the bipolar failure recovery with the proposed topology: (a) dc current i_{dc} (A), (b) current through different elements (A), (c) current in main breaker and load branch (A).

The experimental results support that the proposed topology suppresses the amplitude of fault current effectually, so lowering the requirements on fault current clearing speed and dc protection speed. Moreover, the dc fault current clearing and recovery speed is much faster, with the proposed topology being installed and the MOV capacity can be much smaller, compared with the directly installed dc reactor.

V. LARGE NETWORK SIMULATION CASE STUDY

In Section IV, the effective dc fault current limiting capability, its advantages on speeding up the dc fault current clearing, minimizing the proposed topology's MOV capacity are proved. In order to further validate its supremacy of the dc distribution system application, a meshed dc distribution system based on three-terminal MMC, demonstrated in Fig. 14 is modeled in PSCAD/EMTDC. The parameters are shown in

TABLE III. According to (4), the dc reactor of S_1 is set 60 mH, and the dc reactors of S_2 and S_3 are set 90 mH. The resistance of S_1 proposed topology is set 100 Ω and the resistance of S_2 and S_3 proposed topology are set 200Ω. The dc failure and power flow shifting are preset to observe the effectiveness of the proposed topology respectively.
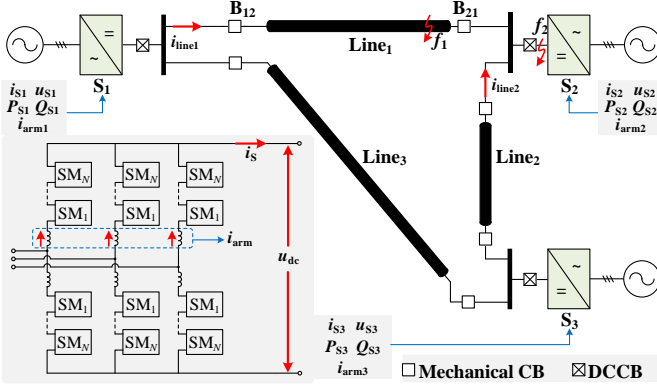

Fig. 14 Topology of the meshed dc system based on three-terminal MMC.

TABLE III PARAMETERS OF THE MMC-BASED THREE-TERMINAL MESHED DC SYSTEM

Parameter	Value
Rated dc voltage (kV)	±10
Rated ac voltage (kV)	10
Rated capacity of S_1~S_3 (MW)	15, 10, 10
Number of SMs per Arm	25
SM capacitors of S_1~S_3 (μF)	16000, 16000, 16000
Arm reactors of S_1~S_3 (mH)	43, 64, 64
Resistance of the dc lines (ohm/km)	0.032
Inductance of the dc lines (mH/km)	1.29
Length of the dc lines (km)	15, 10, 10

A. Healthy Grid Ride-through after DC Failure

In order to confirm the credible fault ride-through capacity of the healthy system with the proposed topology installed, the hybrid configuration strategy presented in [5] is adopted. The proposed methods are configured at the outlets of every converter station. The mechanical DCCBs are fixed on every terminal of dc cables.

The bipolar failure f_1 presented in Fig. 14 is preset to occur at t=2 s. As displayed in Fig. 15 (a), the faulty cable is isolated approximately 15 ms after the failure, where 15 ms is used for protection and mechanical DCCB to act on line$_1$. Since the active reference values of each station are 5MW, 5MW, 10MW respectively, the power flow in the system is S_1 and S_2 feeding S_3 together. This is why the steady current from S_1 to S_2 is almost zero in Fig. 15(a). S_2 is the nearest converter to f_1, so its dc current and voltage are observed. Presented in Fig. 15 (b) and (c), during the operation of protection and mechanical DCCB, the converters' output currents are restricted within the high threshold (2 kA), and the output voltage is maintained higher than the low threshold (16 kV) [5]. Since the faulty cable is segregated, the voltage of dc grid, normal cable current and MMC station current could recover to steady values one and all. The active power, reactive power of each converter, and arm currents keep constant with acceptable fluctuation during the

whole period, illustrated in Fig. 15 (d) and (e). This signifies proposed topology is able to effectively restrict the fault current and enable the remaining grid to ride through the failure.
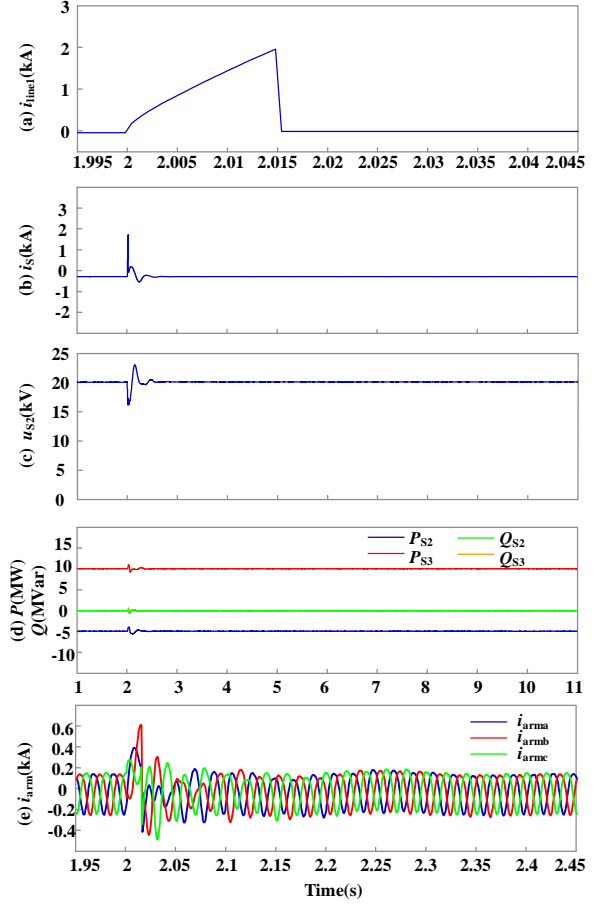

Fig. 15 Simulation results after the forward fault: (a) fault cable current i_{line1} (kA), (b) dc current of S_2 (kA), (c) dc voltage of S_2 (kV), (d) active power and reactive power of S_2, S_3 (MW/MVar), (e) arm currents of S_2 (kA).

The backward failure f_2 (the outlet fault of S_2) in Fig. 14 is preset to occur at t=2 s. S_2 is blocked at t=2.001 s and the proposed topology installed in the outlet of S_2 is tripped to isolate the fault.
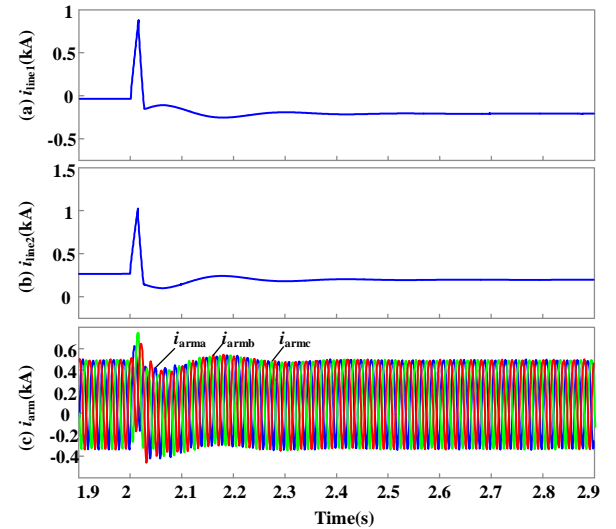

Fig. 16 Simulation results after the backward fault: (a) dc current i_{line1} (kA), (b) dc current i_{line2} (kA), (c) arm currents of S_3 (kA).

Shown in Fig. 16 (a) and (b), though f_2 is a backward fault,

the proposed topology of S_2 can still cut off the fault current. It provides little fault current limiting capability, but the dc current of $line_1$ and $line_2$ can be restricted within the high threshold (2 kA) by other FCLs installed on the outlets of the other converters. Moreover, the arm currents is kept constant with acceptable fluctuation during the whole period, illustrated in Fig. 16 (c).

B. Power Flow Shifting with Various FCLs

Above experimental results show that the transient response is decelerated under the condition that only the reactor is configured. In this case, a further impact of the steadiness of the dc grid is watched, and the reference of active power of S_3 shifts from 10 MW to -10 MW at t=2.2 s.

As presented in Fig. 17 (a), after the active power reference shifts, the dc current changes rapidly from 0.5 kA to -0.5 kA when no dc reactor is installed. After an acceptable fluctuation, the dc voltage quickly returns to the rated value 20 kV, shown in Fig. 17 (b). However, when two reactors of 90 mH are assembled at both poles of S_3 output position respectively, the oscillation happens during power flow shifting, and eventually triggers the grid instability. This is why big dc reactors are not recommended to be directly configured in the distributed grid. While proposed topology is adopted, the dc current and voltage quickly return to stable values after an acceptable transient process, which is close to the transient response characteristics without fault current limiters. This means that proposed topology can eliminate the dc reactor's passive impacts on the system transient response and operating steadiness.
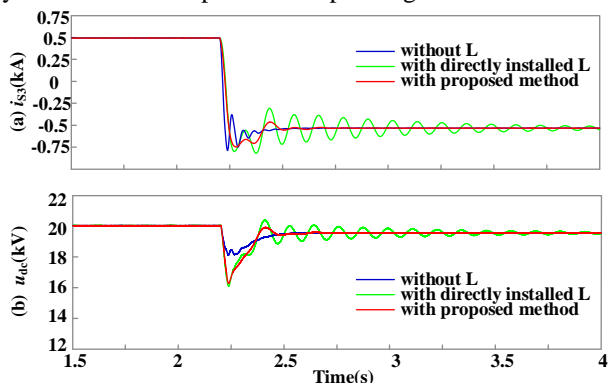

Fig. 17 Simulation results after power flow shifting without fault current limiting, with directly installed dc reactors or with proposed topology: (a) dc current of S_3 i_{S3} (kA), (b) dc voltage u_{dc} (kV).

VI. CONCLUSIONS

Effective fault current limitation is instrumental in reducing the requirement on fault protection and isolation operation speed in dc distribution network. The proposed topology is able to restrict the fault current quickly and automatically before receiving tripping signals from the protection. Compared with the fault current restricting technique by installing dc reactors, the method presented in this paper enjoys two main merits: 1) During normal operation, proposed topology has no impact on the system operation stability. The transient response speed and operation steadiness of the distributed grid are not deteriorated during power shifting. 2) After the proposed topology is tripped, the reactor is automatically and instantaneously bypassed from the faulty branch again to ensure the fast clearance of the fault current. In addition, compared with S-SSCB, the biased power

supply is not used anymore, which greatly reduces the implementation difficulty. Moreover, the operation power loss is also reduced significantly.

REFERENCES

[1] N. Flourentzou, V. G. Agelidis, G. Demetriades, et al. "VSC-Based HVDC Power Transmission Systems: An Overview," IEEE Tran on Power Electron., 2009, vol.24(3): 592-602.
[2] Q Song, B Zhao, W. H. ZHAO, et al. An Overview of Research on Smart DC Distribution Power Network[J]. Proceedings of the CSEE, 2013, 33(25):9-19.
[3] JIANG Daozhuo, ZHENG Huan. Research status and developing prospect of DC distribution network[J]. Automation of Electric Power Systems，2012, 36(8): 98-104．
[4] ZHANG Zhaoyun, LIN Pu1, WANG Xinghua. Review on relay protection of AC/DC hybrid distribution grids[J]. Power System Protection and Control, 2019,47(05):179-187. DOI: 10.7667/PSPC180561
[5] Bin Li, Jiawei He, et al. A novel solid-state circuit breaker with self-adapt fault current limiting capability for LVDC distribution network [J]. IEEE Transactions on Power Electronics, 2019, 34(4): 3516-3529.
[6] Emhemed A, Fong K, Fletcher S, et al. Validation of Fast and Selective Protection Scheme for an LVDC Distribution Network[J]. IEEE Transactions on Power Delivery, 2017, 32(3): 1-8. DOI: 10.1109/TPWRD.2016.2593941
[7] ABB Technical Application Papers No. 5, ABB circuit-breakers for direct current applications. [Online]. Available: http://www.abb.com.
[8] Feng L, Gou R, Zhuo F, et al. Development of a 10kV solid-state DC circuit breaker based on press-pack IGBT for VSC-HVDC system[C]. international power electronics and motion control conference, 2016: 2371-2377. DOI: 10.1109/IPEMC.2016.7512668
[9] Liu F, Liu W, Zha X, et al. Solid-State Circuit Breaker Snubber Design for Transient Overvoltage Suppression at Bus Fault Interruption in Low-Voltage DC Microgrid[J]. IEEE Transactions on Power Electronics, 2017, 32(4): 3007-3021. DOI: 10.1109/TPEL.2016.2574751
[10] Hassanpoor A, Hafner J, Jacobson B, et al. Technical Assessment of Load Commutation Switch in Hybrid HVDC Breaker[J]. IEEE Transactions on Power Electronics, 2015, 30(10): 5393-5400. DOI: 10.1109/TPEL.2014.2372815
[11] GUAN Eryong, DONG Xinzhou, WANG Hao. Study of Combined F ault Current Limiting Equipment and Operation Strategy for DC G rid[J]. Proceedings of the CSEE, 2019, 39(11):3222-3232. D OI:10.13334/j.0258-8013.pcsee.181335
[12] Li R, Xu L, Holliday D, et al. Continuous Operation of Radial Multiterminal HVDC Systems Under DC Fault[J]. IEEE Transactions on Power Delivery, 2016, 31(1): 351-361. DOI: 10.1109/TPWRD.2015.2471089
[13] Khan U A, Lee J, Amir F, et al. A Novel Model of HVDC Hybrid-Type Superconducting Circuit Breaker and Its Performance Analysis for Limiting and Breaking DC Fault Currents[J]. IEEE Transactions on Applied Superconductivity, 2015, 25(6): 1-9. DOI: 10.1109/TASC.2015.2477373
[14] Rui Li, Lie Xu, Derrick Holliday, Frederick Page, Stephen J. Finney, and Barry W. Williams, "Continuous operation of radial multiterminal HVDC systems under dc fault," IEEE Trans. Power Del., vol. 31, no. 1, pp. 351-361, Feb. 2016.
[15] HAN Naizheng, JIA Xiuxiu, ZHAO Xibei, et al．A Novel Hybrid DC Fault Current Limiter Topology[J]. Proceedings of the CSEE,2019, 3 9(6).
[16] Bin Li and Jiawei He, "Studies on the application of R-Sfault current limiting in the VSC-based DC distribution system," IEEE Trans. Appl. Superconduct., vol. 26, no. 3, pp. 5601005, Apr. 2016.
[17] J. Shi, Y. J. Tang, L. Chen, J. Wang, L. Ren, J. D. Li, L. Li, T. Peng, S. J. Cheng, "The application of active superconducting DC fault current limiter in hybrid AC/DC power supply systems," IEEE Trans. Appl. Superconduct., vol. 18, no. 2, pp. 672-675, Jun. 2008.
[18] Jiawei He, Bin Li, and Ye Li, "Analysis of the fault current limiting requirement and design of the bridge-type fault current limiting in the multi-terminal DC grid," IET Power Electron., vol. 11, no. 6, pp. 968-976, May. 2018.
[19] Jian Liu, Nengling Tai, Chunju Fan, and Shi Chen, "A hybrid current-limiting circuit for DC line fault in multiterminal VSC-HVDC

system," *IEEE Trans. Indus. Electron.*, vol. 64, no. 7, pp. 5595-5607, Jul. 2017.

[20] Bin. Li, Jiawei. He, Ye. Li, Weijie. Wen and Botong. Li, "A Novel Current-Commutation-Based fault current limiting for the Flexible DC Grid," in IEEE Transactions on Power Electronics, vol. 35, no. 1, pp. 591-606, Jan. 2020, doi: 10.1109/TPEL.2019.2924024.

[21] Z. Nie, Z. Yu, Z. Gan, L. Qu, Y. Huang and B. Zhao, "Topology Modelling and Design of a Novel Magnetic Coupling Fault Current Limiter for VSC DC Grids," in IEEE Transactions on Power Electronics, doi: 10.1109/TPEL.2020.3025461.

[22] Jin Yang, John E. Fletcher, and John O'Reilly, "Short-circuit and ground fault analyses and location in VSC-based DC network cables," IEEE Trans. Ind. Electron., vol. 59, no. 10, pp. 3827-3837, Oct. 2012.

[23] Jones, P., Davidson, C.: 'Calculation of power losses for MMC-based VSC HVDC stations'. 2013 15th European Conference on Power Electronics and Applications(EPE), Lille, France, September 2013, pp. 1–10.

[24] K Vinothkumar, Inger Segerqvist, Niclas Johannesson, and Arman Hassanpoor, "Sequential auto-reclosing method for hybrid HVDC breaker in VSC HVDC links," in Proc. SPEC, Auckland, New Zealand, 2016, pp. 1–6.

[25] T. Li, A. M. Gole, and C. Zhao, "HArmonic instability in MMC-HVDC converters resulting from internal dynamics," IEEE Trans. Power Del., vol. 31, no. 4, pp. 1738–1747, Aug. 2016.

[26] Bin Li, Jiawei He, Ye Li, et al. The improved topology and control strategy for the HCLC in multi-terminal flexible DC grid [J]. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2021, 9(2):1795-1807.