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Effect of the Heat Dissipation System on Hard-Switching GaN-Based Power Converters for Energy Conversion

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Abstract: The design of a cooling system is critical in power converters based on wide-bandgap (WBG) semiconductors. The use of gallium nitride enhancement-mode high-electron-mobility transistors (GaN e-HEMTs) is particularly challenging due to their small size and high power capability. In this paper, we model, study and compare the different heat dissipation systems proposed for high power density GaN-based power converters. Two dissipation systems are analysed in detail: bottom-side dissipation using thermal vias and top-side dissipation using different thermal interface materials. The effectiveness of both dissipation techniques is analysed using MATLAB/Simulink and PLECS. Furthermore, the impact of the dissipation system on the parasitic elements of the converter is studied using advanced design systems (ADS). The experimental results of the GaN-based converters show the effectiveness of the analysed heat dissipation systems and how top-side cooled converters have the lowest parasitic inductance among the studied power converters.

Keywords: dissipation systems; gallium nitride (GaN); hard-switching; parasitic inductance; power electronics; thermal modelling; thermal interface materials

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1. Introduction

Power converters based on wide-bandgap (WBG) semiconductors offer many advantages over silicon-based converters. These new semiconductors withstand high voltages and temperatures and allow switching at high frequencies with low losses [1,2]. Currently, the two most mature WBG semiconductors are composed of silicon carbide (SiC) and gallium nitride (GaN). In general, GaN offers more benefits than SiC, but its use is currently limited to voltages below 650 V [2]. GaN technology has already been successfully used in many power electronics applications, such as microgrids [3,4], wireless chargers [5], electric vehicle (EV) battery chargers [6], on-board chargers [7], AC electric drives [8,9], electric vehicles [10], and resonant converters [11].

GaN enhancement-mode high-electron-mobility transistors (e-HEMTs) are high power density devices. They can operate at high voltages and currents despite their small size. However, GaN has poor thermal conductivity, lower than that of SiC and silicon [1,2,12,13]. The high power density of GaN e-HEMTs, combined with their low thermal conductivity and small size, makes thermal dissipation extremely difficult in GaN-based power converters. Inadequate thermal management can increase the junction temperature and, thus, reduce efficiency and even cause device destruction. Figure 1 compares the thermal pad size of a SiC MOSFET and a GaN e-HEMT.

Researchers have proposed several methods to improve heat dissipation in GaN-based converters. An interesting proposal is integrating materials with high thermal conductivity within the transistor package, such as graphite and diamond [14,15]. Another proposal to improve dissipation is to modify the packs to dissipate heat on both sides,

top and bottom. This proposal has been made for power converters based on silicon [16] and SiC devices [17–19]. This dissipation method improves the dissipation of the converter but significantly increases its volume, so it is not a valuable proposal for the small GaN-based converters. Liquid cooling is another effective method for improving heat dissipation. In [20], an extensive review of the different liquid cooling solutions is provided. Radio-frequency GaN transistors are directly cooled using the microjet impingement technique [21]. Moreover, the authors improved the GaN packaging using diamond, which further enhanced the heat dissipation. Liquid cooling was also proposed for high power switching applications, such as wind power applications. In [22], a high power three-phase SiC converter was cooled using a liquid-cooled plate. Despite the liquid cooling excellent results, the liquid cycling system (i.e., pumps, compressor, chiller, and radiator) requires a lot of space. Therefore, air cooling is preferred for manufacturing high power density converters [23], especially GaN-based power converters, due to the small size of GaN e-HEMTs. Some researchers investigate alternative thermal interface materials (TIMs) and how to characterise them. Different methods to characterise solid TIMs were analysed by [24]. Finally, in [25,26], the effect of a graphene TIM on the dissipation of GaN transistors and converters was briefly studied. In industry, most power converters use commercial GaN e-HEMTs designed for forced-convection cooling. Usually, GaN transistors are top- or bottom-cooled, but none of the previous articles compared these standard heat dissipation systems. There are some short comparisons, usually between bottom-side cooled converters, in application notes [27,28].

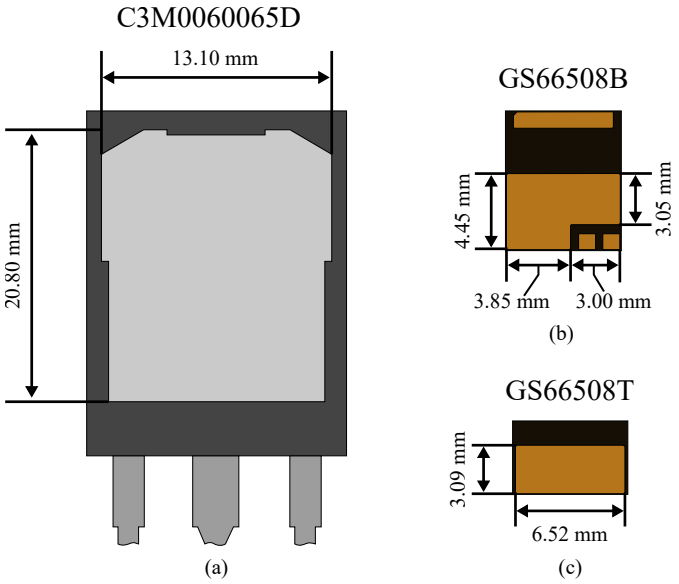

Figure 1. Size comparison between: (**a**) SiC MOSFET; (**b**) bottom-side cooled GaN e-HEMT; and (**c**) top-side cooled GaN e-HEMT. Thermal pad measurements are shown. The transistors are drawn to scale with each other.

It is common practice to simulate the designed power converters before prototyping. Using simulation models to estimate GaN losses, which will be converted to heat, is crucial to ensure a good design. Some popular programs for simulating converters are Matlab-Simulink, PLECS and PSIM [29,30]. A model of GaN in Pspice, which includes the behaviour in the 3rd quadrant, has been developed in [31]. The accuracy of the PLECS models provided by GaN manufacturers is demonstrated in [32]. Additionally, in the same article, different methods to experimentally measure GaN losses are detailed. An analytical model to compute the switching losses is introduced in [33]. Moreover, the accuracy of this model is compared with that of the LTspice simulation tool. Some authors propose new methods to estimate GaN losses. In [34], a model is proposed and validated to quantify the losses caused by the dynamic ON-state resistance of GaN. In [35], two models are

compared to determine the efficiency and temperature of GaN: a basic one and a detailed one that considers parasitic elements. Finally, Catalano et al. propose and experimentally validate an analytical thermal model for thermal vias and heatsinks [36,37]. Nevertheless, none of the previous articles analyses in detail how to simulate the dissipation of GaN losses, nor the effect of dissipation on parasitic elements and losses.

The heat dissipation system affects the PCB layout of the converter, and thus its parasitic elements [38–40]. Parasitic elements of the PCB, i.e., capacitances and inductances, may increase the converter losses and electromagnetic interferences. These elements must be minimised using good PCB design [38–42], so it is essential to analyse the influence of the dissipation system on them.

In this study, we analysed the effect of different dissipation systems in high voltage GaN-based power converters, such as grid-connected converters. These converters must comply with the applicable harmonised standards, so their design has certain constraints which limit the dissipation solutions [43,44]. The two most common dissipation strategies were analysed: top-side cooled GaN e-HEMTs and bottom-side cooled GaN e-HEMTs and thermal vias. Top-side cooled GaN e-HEMTs have the thermal pad on its top side, while bottom-side cooled GaN e-HEMTs have the thermal pad on its bottom side. This article presents the following novelties:

1. A study of the different dissipation strategies and a comparison in terms of thermal efficiency;
2. An analysis of the relationship between the TIM and the effectiveness of the dissipation system;
3. A detailed discussion on how to model GaN converters, including their dissipation system and the parameters that affect losses and junction temperature;
4. A quantification of the impact of the dissipation system on the parasitic inductance of the power converter.

Moreover, we reviewed the different dissipation systems proposed in industry. The review encompassed the PCB structures recommended for thermal dissipation and a summary of the different types of TIMs. In addition, we discussed the modelling of the different dissipation strategies, including a detailed analysis of GaN e-HEMT loss mechanisms and power loop parasitic inductances. The effectiveness of the dissipation techniques was evaluated on the basis of simulation studies using MATLAB/Simulink software and PLECS. The impact of the dissipation system on the parasitic inductances was determined using advanced design system (ADS) software. Finally, the results were experimentally validated by implementing the analysed dissipation strategies on different GaN-based power converters.

The rest of this article is organised as follows: Section 2 reviews different heat dissipation systems, including the PCB structure and the thermal interface materials. Section 3 introduces the models used to simulate the power converters and their dissipation, analyse their basis, and compare the efficiency of the dissipation systems and their effect on the parasitic inductances. Section 4 validates the above results that show the impact of the dissipation strategy on real GaN-based power converters. Finally, Section 5 summarises the conclusions of this study.

2. Thermal Dissipation

The heat dissipation system can be divided into two parts. The first is the PCB structure. The PCB design must be adapted to the heat dissipation method, i.e., top- or bottom-cooling. The second includes the thermal interface materials and the heatsink. The TIM transports heat from the transistor or printed circuit board to the heatsink. Moreover, the TIM adapts surface roughness between surfaces and thus ensure the best possible contact. Some TIMs present additional properties such as electrical isolation.

2.1. PCB Structure

The PCB structure is crucial when designing power converters based on WBG semiconductors. An inadequately designed PCB can increase parasitic elements, i.e., capacitances and inductances. These elements may increase losses, cause electromagnetic interference (EMI), and even destroy the semiconductors. Hence, it is essential to minimise these parasitic elements using a good PCB design [38–42]. In general, four types of PCBs have been proposed (Figure 2): top-cooled PCBs, bottom-cooled with vias, bottom-cooled with a copper inlay, and PCBs with an insulated metal substrate (IMS) [27,28,45].

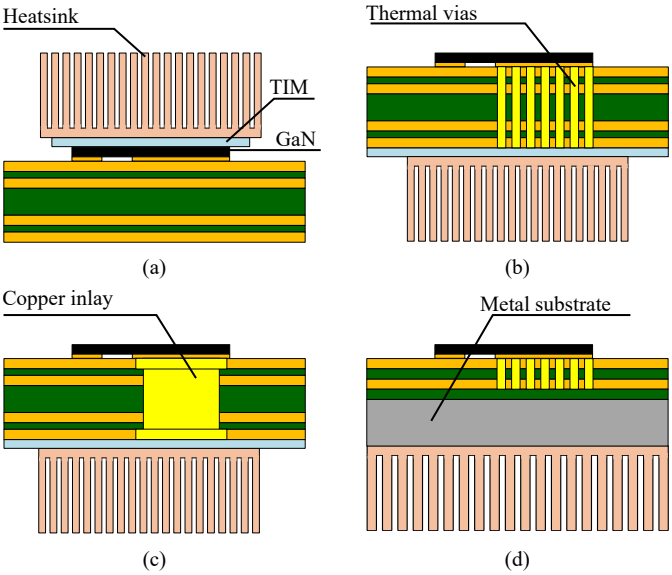

Figure 2. Heat dissipation methods: (**a**) top-side cooled, (**b**) bottom-side cooled with vias, (**c**) bottom-side cooled with copper inlay, and (**d**) insulated metal substrate.

Figure 2a displays a top-side cooled PCB, which is the easiest to manufacture. This structure uses top-side cooled transistors and a heatsink placed on top of these transistors. A TIM must be placed between the transistors and the heatsink to ensure electrical isolation. This type of PCB does not need thermal vias, as heat does not flow through it. Therefore, the return current can flow directly under the GaN, which minimises the power loop parasitic inductance and EMI [27,46,47]. However, this PCB structure has certain drawbacks. Firstly, the heatsink must maintain clearance and creepage distances as defined in the applicable standards [48]. There are several methods available to comply with this requirement, such as using pedestal heatsinks or employing solid insulation [28,48]. Secondly, the thermal pad of GaN is extremely small. It may be necessary to use a TIM with excellent planar thermal conductivity to increase the heat dissipation area. Finally, this dissipation has the highest parasitic capacity. The parasitic capacitance is calculated using

$$C_{par} = \frac{\epsilon_0 \epsilon_r A}{d} \tag{1}$$

where ϵ_0 and ϵ_r are the relative permeability of the air and dielectric, respectively; A is the overlapping area; and d is the distance between the transistor and heatsink.

According to Equation (1), using larger heatsinks to improve dissipation leads to an increase in the parasitic capacitance [27,49].

Figure 2b shows a PCB dissipating through its bottom layer. The thermal resistance of PCBs is high [50]. Consequently, it is necessary to use thermal vias to transfer heat through the PCB [27]. The process of manufacturing this PCB structure is standard and well-known. Furthermore, using this topology easily complies with clearance and creepage distances. However, the presence of vias forces the power loop to be closed over a longer path, which increases the parasitic inductance [39,41,47]. Some manufacturers propose using

electrically insulated thermal vias [51]. Hence, the current may flow directly below the GaN, which minimises parasitic loop inductance. This solution is viable in low voltage power converters but not in high voltage power converters. In these converters, the insulation of the thermal vias must be very thick to comply with the applicable standards, which limits the feasibility of this solution [48].

A manufacturer of GaN e-HEMTs proposed a variation of PCBs that dissipates heat through thermal vias. The manufacturer proposed replacing the vias with a copper inlay, as represented in Figure 2c [45]. This structure has lower thermal resistance than a PCB with thermal vias. However, these PCBs are difficult to manufacture, and their cost may be high. Furthermore, this PCB design increases the power loop parasitic inductance, as do all the topologies with thermal vias. Despite the advantages of this design, the GaN manufacturer did not discuss them in more recent application notes [28].

The last proposed dissipation method is to use IMS PCBs. The thermal conductivity of standard PCBs is very low (<1 W/mK for FR4 material), so some PCBs use alternative materials with better thermal characteristics. PCBs with ceramic materials, such as alumina (Al_2O_3), have been proposed in academia [50]. Alumina has better thermal conductivity than FR4 (from 24 to 33 W/mK) but has low dielectric strength [52]. For this latter reason, PCBs using these materials must be thicker [50]. It was also proposed in industry to mix FR4 with metal substrates. In this topology, a highly conductive metal (i.e., aluminium or copper) replaces the bottom layers of the PCB. The heat flow passes through thermal vias to the layer closest to the metal. The PCB dielectric ensures electrical isolation between the metal and the transistors. Therefore, it is not mandatory to use a TIM [28,45], but it is recommended to ensure uniform contact between the heatsink and metal [27]. Figure 2d illustrates this PCB structure. IMS technology allows manufacturing PCBs with low thermal resistance, much lower than those achieved using thermal vias or copper substrate [27,28,45]. Nevertheless, this type of PCB presents some shortcomings. The metal substrate occupies one side of the PCB. Hence, the component placement is limited to the opposite side [27,28,45]. Thus, larger and more expensive PCBs are needed. The small size of GaN transistors makes it possible to build small converters with high power density. Using large IMS PCBs implies designing larger power converters and, therefore, not taking advantage of the small size of GaN e-HEMTs. To overcome this problem, some manufacturers propose to use two PCBs: one for the power part (i.e., transistors and dc bus) and the other for the signal part (i.e., drivers) [45]. This solution complicates the design of the converter. In addition, placing the drivers and transistors on different PCBs increases the gate loop inductance of the system. Another option is to use custom-made mixed PCBs. These PCBs include IMS on the power part, but the rest of the PCB is standard. This solution is the easiest to design but is extremely expensive. Moreover, the presence of the metal substrate restricts the number of PCB layers [27,28]. Finally, as with other bottom-side cooled topologies, the presence of thermal vias increases the power loop inductance.

Table 1 summarises the main characteristics of the analysed PCB topologies.

Table 1. Comparison of different PCB structures.

	Top Side	**Bottom Side with Thermal Vias**	**Bottom Side with Cu-Inlay**	**IMS**
Figure	Figure 2a	Figure 2b	Figure 2c	Figure 2d
Thermal resistance [a]	**/***	*	**	***
Cost	Low	Low	High	Medium
Parasitic inductance	Low	High	High	High
Parasitic capacitance	High	Low	Low	Low
References	[28,53]	[27,28,45,54]	[45]	[27,28,45,55]

[a] A high number of asterisks is preferred.

2.2. Thermal Interface Materials

Thermal interface materials are elements that are inserted between two components to improve their thermal coupling. Usually, these materials are good thermal conductors and should have good gap filling properties. Electrical isolation is necessary for AC/DC converters in which several transistors share a single heatsink. However, other converter types do not require dielectric TIMs [56].

Many properties of TIMs must be considered when designing the dissipation of a GaN-based power converter. The most significant characteristics are described below:

- **Thermal conductivity:** determines the capacity to conduct heat. Materials with a high thermal conductivity easily transfer heat;
- **Thermal resistance:** measures the difficulty with which heat flows through a component. It should be as low as possible to ensure good dissipation. Thermal resistance is defined as

$$R_{th} = \frac{e}{A \times \lambda} + R_{c1} + R_{c2} \quad (2)$$

  where e is the thickness, A is the cross-sectional area perpendicular to the heat flow path, λ is the thermal conductivity, and R_{c1} and R_{c2} are the contact resistances of the TIM with adjacent surfaces;
- **Mounting pressure:** directly influences the thermal resistance of the TIM (see Equation (2)). Each material requires a different pressure to minimise contact resistance [57,58]. Inadequate pressure can increase the thermal resistance and cause GaN e-HEMTs to overheat [27]. Importantly, some GaN e-HEMTs only tolerate pressures below 690 kPa (100 psi) [28];
- **Dielectric breakdown voltage:** is the maximum voltage that a dielectric can withstand without becoming electrically conductive. This voltage depends, amongst others, on the size, shape, and material of the TIM [59].

Apart from the above properties, others may be important depending on the application, such as the thermal expansion coefficient, operating temperature range, and viscosity [57,59].

Among the TIM types, polymeric ones are widely used due to their excellent dielectric properties, low cost, and ease of handling [57,59]. However, their thermal conductivity is very low (from 0.1 to 0.5 W/mK). It is common to fill the polymers using high-thermal-conductivity materials, such as aluminium oxide, graphite, or diamond, to improve their thermal conductivity [56,59,60].

Thermal conductivity in the through-plane direction is a critical parameter when designing GaN e-HEMT heat dissipation. High in-plane conductivity expands the heat flow area and decreases the thermal resistance of the TIM. The thermal pad of GaN e-HEMTs is small, so it is strongly recommended to enlarge the heat flux area with TIMs with high conductivity in the through-plane direction. Most commercially available polymeric TIMs have conductivities of less than 10 W/mK [58]. Nevertheless, in many cases, the in-plane conductivity ranges from 4 to 5 W/mK [58].

Graphite-enhanced TIMs can solve this problem. These materials have an extremely high thermal conductivity in all directions [56,61]. Additionally, graphite is affordable, abundant, and allows for the production of TIMs with improved physical properties. For example, graphite-enhanced TIMs are flexible and require low assembly pressures [61,62]. However, graphite has low electrical resistance, so these TIMs may include an isolation layer on the surface to ensure electrical isolation [58,59].

Table 2 summarises the characteristics of the two groups of commercially available TIMs analysed in this article. The first group consists of filled-polymer TIMs known as gap pads. The second comprises different graphite-enhanced TIMs. Graphite-based TIMs have higher thermal conductivities and lower thicknesses than those of filled polymers. Hence, graphite-enhanced TIMs may have lower thermal resistance and are more suitable for working with GaN e-HEMTs. Figure 3 represents the heat flow through the two analysed TIMs.

Table 2. Properties of common thermal interface materials [58,63].

	Filled-Polymer TIM (Gap Pad)	Graphite-Enhanced TIM
Thermal conductivity (W/mK)	Z: 0.8–5 X–Y: 4–5	Z: 8–13 X–Y: 350–1750
Thickness (mm)	0.5–6.35	0.017–0.8
Electrical isolation	1–2 sides	0–1 sides
Adhesive	1–2 sides	0–1 sides
Temperature range (ºC)	From –60 to 200	From –55 to 400

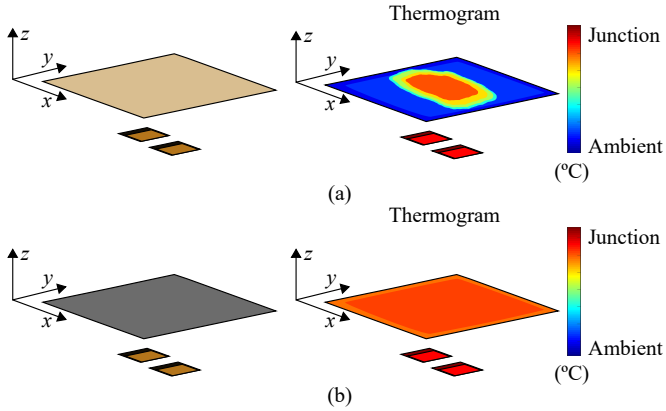

Figure 3. Representation of heat flow through: (**a**) a polymetric TIM; and (**b**) a graphite-enhanced TIM.

3. Power Converter Modelling and Simulation Results

This section describes the GaN-based power converter parameters that influence losses, temperature, and parasitic inductance. In addition, the section details how to include these parameters in the simulation model.

The proposed model uses the following assumptions:

- The heatsink does not affect the parasitic capacitance;
- The temperature inside the GaN e-HEMT is homogeneous;
- There is no gate driver loss.

Additionally, this section describes the evaluation of the effectiveness of the dissipation strategies and their effect on parasitic inductance. The dissipation system effectiveness and the power converter losses were computed using the MATLAB/Simulink (version 2018a) and PLECS software (version 4.5.3). The parasitic inductances were determined using ADS software (version 2021 update 2).

3.1. Thermal Modelling

The objective of the thermal model is to validate the heat dissipation system. The proposed thermal model allows estimating the temperature of the GaN e-HEMTs and, thus, determining if the converter will function.

The first step was simulating the GaN transistors. Internally, these devices are composed of layers of different materials. Consequently, the temperature inside the transistors is not homogeneous [64,65]. However, to simplify the model, the junction temperature was assumed to be constant throughout the interior of the device. The thermal behaviour of GaN e-HEMTs was simulated using their equivalent thermal model. This thermal model represents the physical structure of GaN, i.e., its different internal layers [28,66]. Each inner layer was modelled using a thermal resistor and a capacitor. The manufacturer of the used GaN e-HEMTs provides these thermal parameters in the datasheets [67,68]. Figure 4 shows the equivalent Cauer thermal model of a GaN e-HEMT.

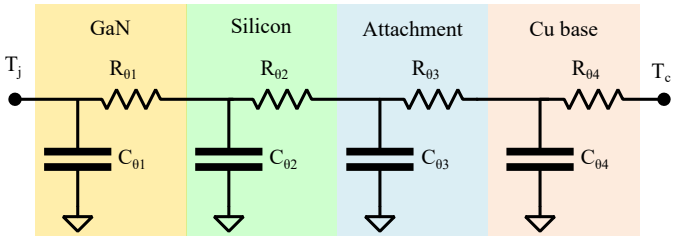

Figure 4. Equivalent thermal model of a GaN e-HEMT.

For bottom-side cooled PCBs, the next step was to calculate the equivalent thermal resistance of the thermal vias. This parameter was calculated using

$$R_{Vias} = \frac{1}{n} \times \frac{e}{\pi \times \lambda_{CU}(R^2 - (R-r)^2)} \tag{3}$$

where e is the thickness, n is the number of thermal vias, λ_{CU} is the thermal conductivity of copper (401 W/mK [69]), R is the radius of the drill hole, and r is the plating thickness.

The thermal resistance of the TIM was then estimated. If the contact between the TIM and adjacent surfaces is ideal, contact resistances are negligible. Then, Equation (2) becomes

$$R_{TIM} = \frac{e}{A \times \lambda_{TIM}}. \tag{4}$$

The heat spreads out in the XY plane as it flows through the TIM. Therefore, area A is not constant but increases as the heat moves away from the GaN e-HEMT. It is usual to consider the smallest contact area to simplify the calculation of this thermal resistance. Furthermore, considering the smallest area is the most critical case. As a general rule, when several transistors share a TIM, the TIM should be modelled as multiple thermal resistors in parallel. The value of each of these resistors is calculated using the contact area between the TIM and the transistor. Sometimes there is an element on the other side of the TIM, such as a second TIM. The thermal resistance of this second element considers the whole area of the first TIM. Moreover, this element dissipates all heat flowing through the first TIM.

Finally, there is the heatsink. The thermal resistance of heatsinks is usually provided in their data sheets. The thermal resistance of the heatsink considers that the heat flows uniformly through the base of the heatsink. Data sheets often include the effect of forced cooling on thermal resistance: the higher the airspeed, the lower the thermal resistance. Another significant parameter is the thermal capacity of the heatsink. This parameter determines the dynamics of the heatsink and was modelled using a thermal capacitor. The thermal capacity was calculated by

$$C_{heatsink} = m \times c_p \tag{5}$$

where m is the mass of the heatsink and c_p is its specific heat capacity. The latter depends on the material of the heatsink, usually aluminium (0.897 J/gK) or copper (0.385 J/gK).

The system thermal model was obtained using all the previous thermal resistances and capacitances. Figure 5 shows the thermal model of top- and a bottom-side cooled converters in which several transistors share a single heatsink.

3.2. Electrical Modelling

GaN transistor losses are one of three different types: gate losses, switching losses, and conduction losses. This subsection discusses these losses and explains how to include them in a PLECS model. Figure 6 outlines the different types of losses.

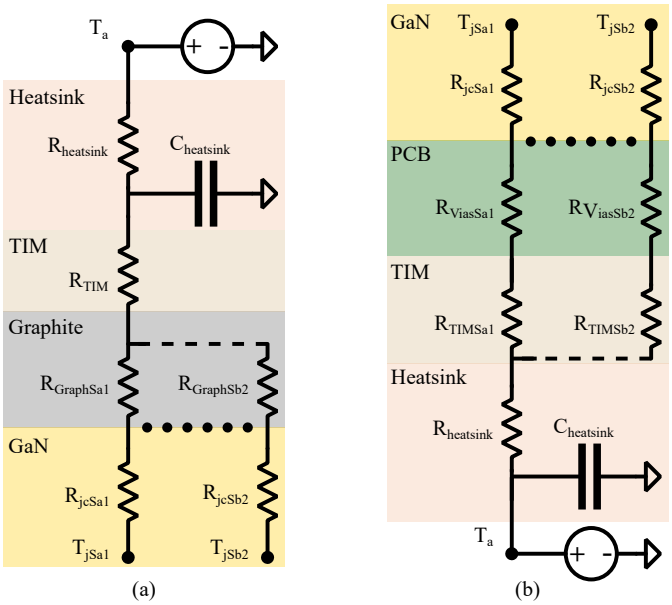

Figure 5. Thermal model of a converter with: (**a**) top-side cooled GaN-eHEMTs; and (**b**) bottom-side cooled GaN e-HEMTs.

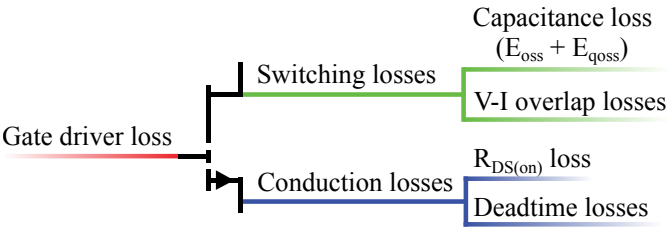

Figure 6. Major sources of losses in GaN e-HEMTs.

3.2.1. Gate Driver Loss

GaN e-HEMTs, like Si transistors, experience gate driver losses, but GaN devices have a small gate charge, so they have fewer gate driver losses Si devices. Moreover, the activation voltage of GaN is usually low, around 5 V, so losses are further reduced. The gate driver loss can be calculated by applying

$$P_{driver} = V_{gs(on)} \times Q_G \times f_{sw} \quad (6)$$

where $V_{gs(on)}$ is the turn-on gate-source voltage, Q_G is the total gate charge, and f_{sw} is the switching frequency.

3.2.2. Switching Losses

In hard-switched GaN converters, the switching losses include turn-ON/turn-OFF VI overlap loss (E_{VI}), E_{oss} and E_{qoss} losses. Voltage and current overlap losses occur only in hard-switching. These losses are defined as the area of overlap between the voltage and current waveforms. Hence, these losses appear during transistor turn-on and also during turn-off.

The drain-source capacitances (C_{oss}) of GaN e-HEMTs produce E_{oss} and E_{qoss} losses. Both losses occur only during the turn-on process [70,71]. E_{oss} is caused by the capacitance C_{oss} of the transistor. During turn-on, the transistor is closed, and its drain-source voltage decreases. The capacitance C_{oss} is discharged through the transistor. E_{oss} is calculated by

$$E_{oss} = \int_0^{V_{dc}} V_{ds} \times C_{oss(V_{ds})} dV_{ds} \quad (7)$$

where V_{dc} is the DC bus voltage and V_{ds} is the drain-source voltage.

The C_{oss} capacitor of the complementary transistor produces E_{qoss}. The transistor is off, so the C_{oss} capacitor needs to be charged. The charging current I_{qoss} passes through the complementary transistor, which is on, causing additional losses. The expression of E_{qoss} is

$$E_{qoss} = \int_0^{V_{dc}} (V_{dc} - V_{ds}) \times C_{oss(V_{ds})} dV_{ds}. \quad (8)$$

Figure 7 depicts the turn-on process in a half-bridge electrical circuit. In this figure, transistor S2 is turned on, so the capacitance C_{oss2} is discharged and produces E_{oss} losses. In contrast, S1 is off, so C_{oss1} is charged through S2, generating E_{qoss} losses.

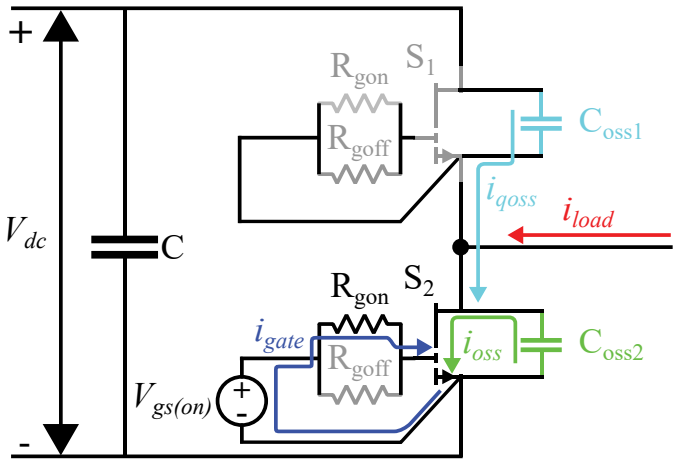

Figure 7. Half-bridge electrical circuit the turn-on process.

The PCB also introduces additional parasitic capacitance between the drain and source. This parasitic capacitance increases the E_{oss} and E_{qoss} losses. Consequently, Equations (7) and (8) are rewritten as

$$E_{oss} = \int_0^{V_{dc}} V_{ds} \times C_{oss(V_{ds})} dV_{ds} + \frac{C_{pcb} \times V_{dc}^2}{2}, \text{ and} \quad (9)$$

$$E_{qoss} = \int_0^{V_{dc}} (V_{dc} - V_{ds}) \times C_{oss(V_{ds})} dV_{ds} + \frac{C_{pcb} \times V_{dc}^2}{2} \quad (10)$$

where C_{pcb} is the parasitic capacitance introduced by the PCB.

The total transistor turn-on and turn-off losses are calculated by

$$E_{on} = E_{VIon} + E_{qoss} + E_{Eoss} \quad (11)$$

and

$$E_{off} = E_{VIoff}. \quad (12)$$

The calculation of losses was simplified using PLECS software. This software employs thermal data sheets to calculate device losses, depending on several parameters such as the junction temperature, the device current, or the device voltage. These data sheets can be created manually, but many manufacturers provide them for their devices.

Thermal data sheets consist of look-up tables and equations. Look-up tables are similar to the loss tables provided on component data sheets. The look-up tables define loss values for certain current, voltage, and temperature values. If the transistor is working between two defined points, PLECS approximates the losses by linear interpolation. Figure 8 illustrates the look-up tables of the studied GaN e-HEMTs. The look-up table illustrated in Figure 8a includes the turn-on caused by E_{oss} and E_{qoss}. When I_{ds} is equal to zero, there are losses proportional to the voltage V_{ds}. At these operating points, there are no losses due to E_{VIon} since the current is zero. Therefore, the losses that appear are produced by the parasitic capacitors of GaN, i.e., they are the sum of E_{oss} and E_{qoss}.

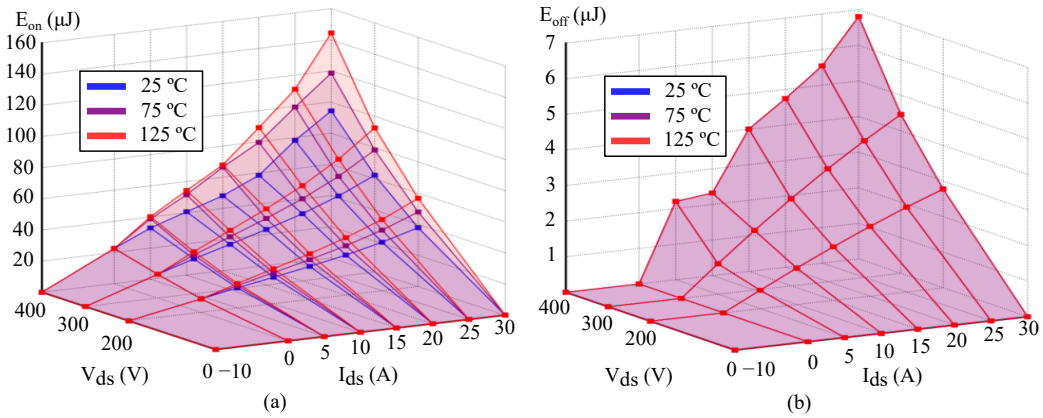

Figure 8. GaN e-HEMTs look-up tables: (**a**) turn-on and (**b**) turn-off losses.

Equations allow direct calculation of losses using parameters, such as device voltage, current, junction temperature, gate voltages, and external gate resistances. Moreover, the output of a look-up table can be a variable of an equation. This last operation allows obtaining a more accurate loss value. Some manufacturers provide these equations in the thermal model of their transistors. The manufacturer details that the turn-on losses of the modelled GaN e-HEMTs (GS66508B and GS66508T) are defined as

$$E_{on} = (-8.990 \times 10^{-12} + 1.788 \times 10^{-10} \times I_{ds}) \times \\ \times (R_{gon} - 10) \times V_{ds} + E_{on} \tag{13}$$

where I_{ds} is the drain current in A and R_{gon} is the external turn-on gate resistance in Ω. The voltage V_{ds} is in V. Notice that this expression uses the turn-on energy losses in µJ obtained by applying the look-up table as a variable.

The expression for the turn-off losses provided by the manufacturer is

$$E_{off} = \frac{(-8.718 \times 10^{-10} + 2.103 \times 10^{-8} \times I_{ds})}{(|V_{gs(off)}| + 1.3 + 0.041 \times I_{ds}) T_j} \times \\ \times (R_{goff} - 2) \times V_{ds} + E_{off} \tag{14}$$

where R_{goff} is the external turn-off resistance in Ω, $V_{gs(off)}$ is the turn-off gate-source voltage in V, and T_j is the junction temperature in ºC. In this equation, the current I_{ds} is expressed in A, the voltage V_{ds} is in V, and the energy E_{off} is in µJ.

Finally, the power loss in a switching period is estimated using

$$P_{sl} = \frac{1}{nT_{sw}} \sum_{j=1}^{j=nT_{sw}} \left(E_{on_j} + E_{off_j} \right) \tag{15}$$

where nT_{sw} is the number of transitions in one fundamental period.

3.2.3. Conduction Losses

Two mechanisms contribute to GaN conduction losses. The first is the on-state resistance ($R_{DS(on)}$). When a GaN e-HEMT is turned on, it has an internal resistance that causes a voltage drop across the device. This voltage drop, together with the current, generates some conduction losses. $R_{DS(on)}$ is not constant but depends on two physical effects: the heating effect and the charge-trapping effect of electrons [34]. In general, an increase in the temperature results in higher on-resistance and, thus, more conduction losses. The resistance also increases due to electrons trapped inside the GaN e-HEMT, i.e.,

the charge-trapping effect. Material defects in the transistor cause electron trapping and an additional increase in on-resistance [32]. The expression that describes the on-resistance is

$$R_{DS(on)} = R_{DS(on)(25\,^{\circ}\mathrm{C})} \times (1 + k_{Tj} + k_{dr}) \tag{16}$$

where $R_{DS(on)(25\,^{\circ}\mathrm{C})}$ is the static on-resistance at 25 °C, k_{Tj} is the increased normalised $R_{DS(on)}$ portion from the heating effect, and k_{dr} is the increased portion due to the trapping effect. Notice that k_{Tj} and k_{dr} are normalised to $R_{DS(on)(25\,^{\circ}\mathrm{C})}$.

Dynamic on-resistance is complex to measure and model, mainly due to the charge-trapping effect [34]. This effect makes the on-resistance dependent on several parameters, such as switching frequency, duty cycle, and drain-source voltage [32]. Furthermore, the transistor device used also changes the behaviour of $R_{DS(on)}$ [72–74]. However, the on-resistance increase is mainly due to the heating effect, especially as the junction temperature increases [34].

The deadtime contributes significantly to the conduction losses of GaN e-HEMTs [34]. GaN e-HEMTs do not have an intrinsic body diode, but they are capable of reverse conduction [67,68]. In this operation mode, the transistor starts to conduct when the gate-drain voltage exceeds the gate threshold voltage. Nevertheless, the voltage drop is higher than those of diodes, so the reverse conduction losses are significant [55]. The voltage drop during deadtime is calculated using

$$V_{deadtime} = V_{th} + |V_{gs\_off}| + V_{on} \tag{17}$$

where V_{th} is the the threshold voltage and V_{on} is the on-state drain-source voltage.

There are mainly two methods used to minimise reverse conduction losses. The first is to reduce deadtime. Reverse conduction losses occur during deadtime, so losses decrease if deadtime is minimised. The second method is to adjust the turn-off gate-source voltage. $V_{gs(off)}$ affects reverse conduction and switching losses. Negative turn-off voltages increase the voltage drop across the transistor (see Equation (17)) and, therefore, raise the reverse conduction losses. However, negative voltages decrease the turn-off losses, as detailed in Equation (14). Hence, the optimum voltage value depends on the converter application and parameters [55].

PLECS software calculates conduction losses using look-up tables and equations, using the same procedure as for switching losses. Figure 9 depicts the look-up table used to calculate the conduction losses. Notice that the absolute value of the on-state voltage V_{on} increases with temperature. Therefore, the look-up table considers the heating effect in $R_{DS(on)}$. Deadtime must be included in the electrical model of the converter. The negative voltages and currents in the look-up table correspond to reverse conduction. PLECS calculates the voltage drop with the look-up table and then adjusts it employing

$$V_{deadtime} = V_{on} - (1.3 - V_{gs\_off}). \tag{18}$$

Equation (18) is provided by the manufacturer in the GaN e-HEMTs thermal models. This expression is a particular case of Equation (17), where V_{th} is 1.3 V.

Finally, conduction losses are calculated as

$$P_{cl} = \frac{1}{T_{sw}} \left(\int_0^{T_{dead}} (V_{deadtime} \times I_{ds}) dt + \int_{T_{dead}}^{T_{sw}} (V_{on} \times I_{ds}) dt \right) \tag{19}$$

where T_{sw} is the switching period and T_{dead} is the deadtime.

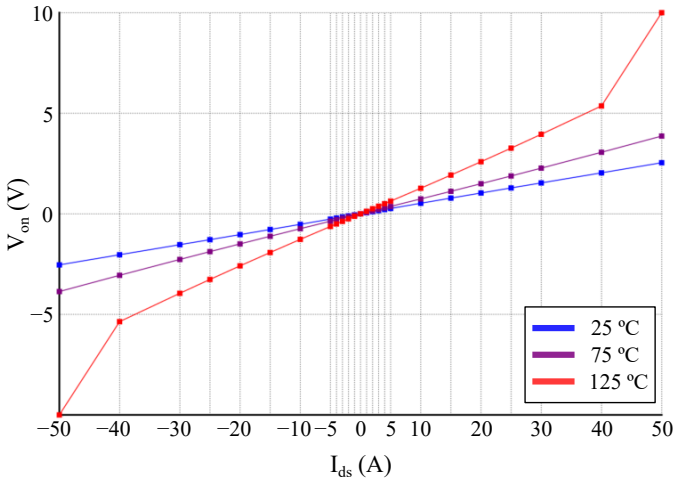

Figure 9. GaN e-HEMT conduction losses look-up table.

3.3. Temperature Analysis

We also analysed the efficiency of the proposed heat dissipation systems and power converters. We compared two types of GaN-based power converters: a bottom-side cooled converter using thermal vias (Figure 5b) and a top-side cooled converter. Additionally, the simulations considered three different top-side cooled converters to study the effect of TIM on heat dissipation. The first used a graphite-enhanced TIM to expand the heat flow area and a polymeric TIM to fix the heatsink (Figure 5a). The second used a single layer of graphite-enhanced TIM, so the heatsink may be attached using screws. The last used a single layer of polymeric TIM to increase the heat flow area and stick the heatsink.

The effectiveness of the different dissipation strategies was evaluated in the power converter shown in Figure 10. This converter consisted of a GaN single-phase inverter, a step-down transformer, and a rectifier formed by SiC diodes. The simulations only studied the losses and dissipation of the GaN inverter, as this is the critical point of the system.

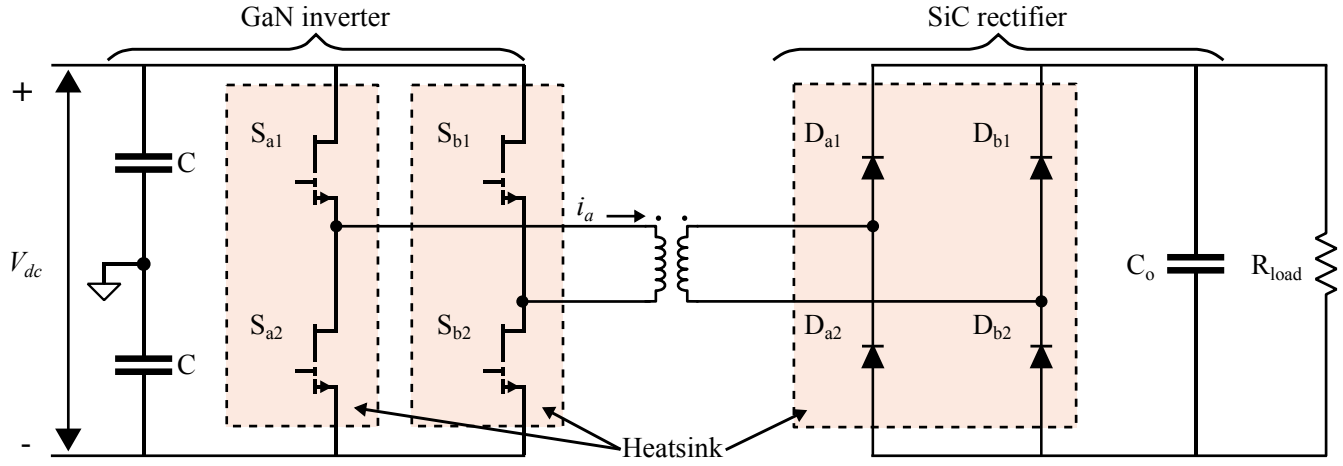

Figure 10. Schematic of the power converter. The heatsinks are drawn with dashed lines.

The DC bus voltage was 300 V, and the transformer turn ratio was 2. The GaN e-HEMT GS66508B/T was used to simulate the converter switches. This device, manufactured by GaN Systems, features a maximum drain-source voltage (V_{ds}) of 650 V and a continuous drain current (I_{ds}) of 30 A. Each device had an external turn-on gate resistance of 10 Ω. The deadtime was 40 ns, and the turn-off gate-source voltage was 0 V. SiC C4D10120D diodes from CREE were used to model the rectifier. These diodes allowed a maximum current of 38 A, and their forward voltage was 1.4 V. The ambient temperature was equal

to 25 ºC. Table 3 details the thermal resistances included in the model. Each half-bridge had its heatsink, so the equivalent thermal resistances in a half-bridge are detailed.

Table 3. Thermal resistances included in the simulation model.

Equivalent Thermal Resistance	Bottom-Side with Thermal Vias (°C/W)	Top-Side with Graphite and Polymer (°C/W)	Top-Side with Graphite (°C/W)	Top-Side with Polymer (°C/W)
GaN e-HEMTs (R_{jc})	0.25	0.25	0.25	0.25
Thermal vias (R_{Vias})	0.30	—	—	—
Graphite-enhanced TIM (R_{Graph})	—	0.04	0.04	—
Filled-polymer TIM (R_{TIM})	0.26	0.41	—	7.76
Heatsink ($R_{heatsink}$)	0.80	0.80	0.80	0.80
Total thermal resistance	1.61	1.5	1.09	8.81

We used the junction temperature safety factor as a comparison parameter. The safety factor is defined as follows

$$\gamma_{^oC} = \frac{T_{jMAX}}{T_j} \tag{20}$$

where T_{jMAX} is the maximum operating junction temperature and T_j is the junction temperature in steady-state.

Figure 11 plots the junction temperature safety factor of the studied converters. Only the junction temperature of a single transistor is shown, as it is the same for all four transistors of the converter due to the implemented modulation. When the safety factor is higher than one, the junction temperature is below the maximum operating temperature, so the converter works safely. A safety factor equal to or less than one implies that the GaN e-HEMTs are overheated and may be destroyed. Figure 11a shows the temperatures obtained for the bottom-side cooled power converter. The safety factor decreases as the output power and switching frequency increase. As the switching frequency increases, the losses also grow, so the junction temperature of the GaN device increases, and the safety factor diminishes. The same applies to output power. The DC bus voltage is constant, so more power means more current, and, therefore, additional losses and higher temperature. The safety factor is equal to or higher than one for most operating points but at maximum output power and switching frequency. At this operating point, the safety factor is slightly less than one, so the GaN device would overheat. Figure 11b illustrates the junction temperature of the top-side cooled power converter with graphite-enhanced and polymeric TIMs. The safety factor of this converter is always slightly higher than that of the bottom-side cooled converter. This coincidence in temperatures is due to the similar thermal resistance of the converters (Table 3). As with the bottom-side cooled converter, the safety factor is always equal to or greater than one except at maximum output power and switching frequency. Figure 11c depicts the junction temperature of the top-side cooled power converter with a graphite-enhanced TIM. This dissipation method has the lowest thermal resistance, so the safety factor is higher than one for all the operating points. Hence, the analysed top-side cooled converter can safely operate at high switching frequencies and powers. Finally, Figure 11d shows the temperatures of a top-side cooled converter with a polymeric TIM. The conductivity of the TIM in the in-plane direction is very low, so the thermal resistance of the system is the highest among the studied converters. Hence, the values of $\gamma_{^oC}$ are inferior to those of the other converters. This converter can only switch at frequencies of up to 250 kHz when operating at low power; otherwise, the junction temperature may surpass the maximum operating temperature. As the output power increases, the maximum switching frequency must decrease to guarantee the correct operation of the converter. From 2 kW upwards, overheating occurs using this dissipation system for all the switching frequencies.

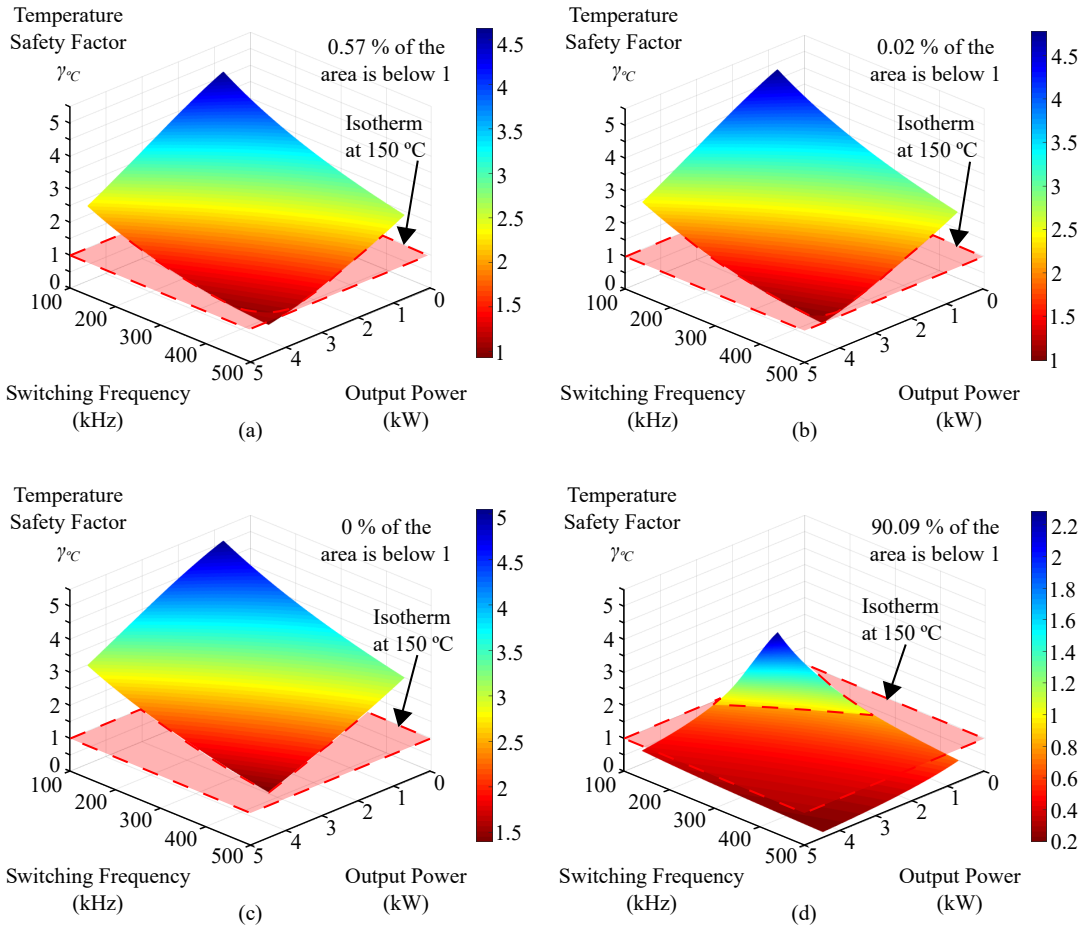

Figure 11. Junction temperature safety factor: (**a**) bottom-side cooled converter; (**b**) top-side cooled converter with graphite-enhanced and polymeric TIMs; (**c**) top-side cooled converter with a graphite-enhanced TIM; and (**d**) top-side cooled converter with a polymeric TIM.

The former simulation results depend on the deadtime used. As explained above, the deadtime value influences the GaN losses. The losses of a GaN e-HEMT were obtained using different deadtimes to study this effect. Figure 12 illustrates the losses of a transistor as a function of deadtime and output power. Losses rise as output power and deadtime increase, but the influence of deadtime varies with output power. At low power, the deadtime has little impact on losses. A deadtime of 100 ns produces 0.7 W more losses than a deadtime of 40 ns. However, deadtime losses significantly increase as the output power grows. At high power, a deadtime of 100 ns generates 6.65 W additional losses in each transistor than a deadtime of 40 ns. Therefore, in hard-switching high-power converters, it is critical to minimise the deadtime to optimise efficiency.

3.4. Parasitic Inductance Modelling

The dissipation system influences the PCB layout and thus its parasitic inductance. It is essential to estimate the parasitic inductance to verify the converter design before manufacturing. Quantifying the parasitic inductance allows knowing the voltage ringing of the converter. It is crucial to limit this ringing to avoid the destruction of the converter [39]. The parasitic inductance can be determined analytically, employing simulations, and through experiments.

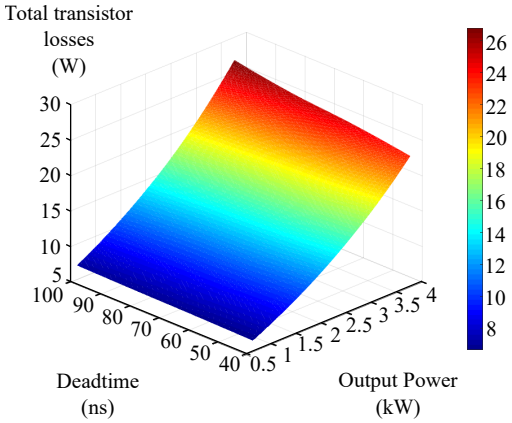

Figure 12. Total transistor losses as a function of deadtime and output power.

The fastest method for estimating the parasitic inductance is through calculation. In a power loop in which the forward and reverse current flow through different layers, the parasitic inductance is determined with

$$L_{pcb} = \mu_r \mu_0 \frac{h}{w} l \tag{21}$$

where μ_0 and μ_r are the vacuum and PCB permeabilities, respectively; h is the distance between the layers; w is the width of the power loop; and l is the length of the loop.

However, Equation (21) is not accurate enough for the small power loops that are frequently used in GaN converters [39]. Hence, the following correction is proposed:

$$L_{pcb} = \mu_r \mu_0 \frac{h}{w} l \left(\frac{1}{1 + h/w} + 0.024 \right). \tag{22}$$

The above expression is only valid when 0.25 mm $< w <$ 50 mm and 100 µm $< h <$ 2 mm [39]. In addition, both Equations (21) and (22) assume that the return current path is entirely below the forward current path. However, in bottom-side cooled converters, the presence of thermal vias prevent this, so the former equations are not adequate.

Simulating PCBs allows the estimation of the parasitic inductance for all types of power loops. We used ADS software to determine the effect of the constraints inherent to each dissipation system on parasitic inductance. This software allows importing PCB designs for further electromagnetic analysis. ADS uses scatting parameters (S parameters) to accurately extract the low parasitic inductances present in the GaN power loops. There are three methods to measure the loop impedance (Z_{pcb}) using S parameters: one-port reflection, two-port shunt-thru, and two-port series-thru [42]. Figure 13 illustrates the different measurement procedures.

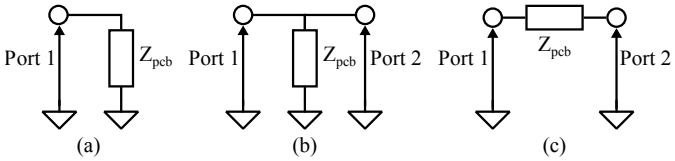

Figure 13. Techniques for measuring S parameters: (**a**) 1-port reflection; (**b**) 2-port shunt-thru; and (**c**) 2-port series-thru.

Figure 13a shows the one-port reflection technique. This method connects the PCB, which is the device under test, in parallel with the port. ADS transmits a sinusoidal signal through the port and measures the reflection coefficient S_{11}. This measurement system is accurate for high impedances. However, the error is significant for impedances below 0.1 Ω. Therefore, two-port S-parameter methods are more suitable to measure very low impedances.

Figure 13b illustrates the shunt-thru method. This technique is the most accurate when measuring low inductances, less than 10 nH [42]. Therefore, it was the method used in this study. In this two-port method, the S parameters S_{11} and S_{22} contain the impedance of the PCB and their internal impedances. As in the one-port reflection method, each port sends an electrical signal and measures its reflection to determine the impedance of the PCB. However, the ports also measure the reflection of the signal transmitted by the other ports. Therefore, the S parameters determined by a port are

$$S_{11} = \frac{-Z_0/2}{Z_{pcb} + Z_0/2}, \text{ and} \tag{23}$$

$$S_{21} = \frac{Z_{pcb}}{Z_{pcb} + Z_0/2}. \tag{24}$$

where Z_0 is the impedance of the port, whose value is 50 Ω.

Both S parameters work to obtain the PCB impedance, but S_{21} is more sensitive to slight voltage variations [75]. Therefore, Equation (24) is preferred to estimate very low impedances.

Figure 13c displays the two-port series-thru measurement method. This procedure achieves the highest accuracy in measuring high impedances [42]. In this technique, the PCB is connected between the two ports, so the S parameters contain the PCB impedance and the internal impedances of the two ports.

Once Z_{pcb} is obtained, the calculation of the parasitic inductance (L_{pcb}) is straightforward. Usually, the parasitic capacitance is negligible at low frequencies (<100 MHz) and can, therefore, be neglected. If the capacitive part of the impedance is neglected, the PCB impedance is

$$Z_{pcb}(\omega) = \sqrt{R_{pcb}^2 + (\omega L_{pcb})^2} \tag{25}$$

where R_{pcb} is the parasitic resistance of the PCB and ω is the pulse signal.

ADS software can determine the modulus of the impedance, so neither R_{pcb} nor L_{pcb} is known. However, the parasitic inductance is minimal at low frequencies. Consequently, at these frequencies, the impedance is essentially resistive. Once R_{pcb} is known, the parasitic inductance can be calculated using Equation (25).

3.5. Parasitic Elements Analysis

The PCBs of the analysed converters are imported into ADS to estimate their parasitic inductances. The GS66508B-EVBDB1 daughter board was used as a model for the bottom-cooled power converter. The model of the top-side cooled converter was based on a prototype that we designed. Figure 14 illustrates the studied PCBs and their power loops.

Figure 14a shows the power loop of the bottom-side cooled converter. Due to the presence of thermal vias, the power loop cannot be closed just below the GaN. Therefore, this PCB uses two different strategies to close the loop. Firstly, there is a lateral loop. In this loop, forward and reverse currents flow through the same PCB layer. This loop partially cancels the electromagnetic flux and, thus, has the highest parasitic inductance [38,39]. Secondly, there is a mixed loop. This loop is like a lateral loop where the current returns through inner layers. This additional loop may be helpful if the GaN thermal vias occupy a small surface area. In this scenario, the return currents can flow near the GaN e-HEMTs, which would reduce the parasitic inductance.

Figure 14b illustrates the PCB of the top-cooled power converter. This converter has no thermal vias. Thus, the power loop can be minimal. In this case, the return currents flow through the inner layer immediately below the GaN e-HEMTs. Hence, the electromagnetic fluxes are cancelled, and the parasitic inductance is minimised. This hybrid loop has the lowest parasitic inductance among the power loops [38,39].

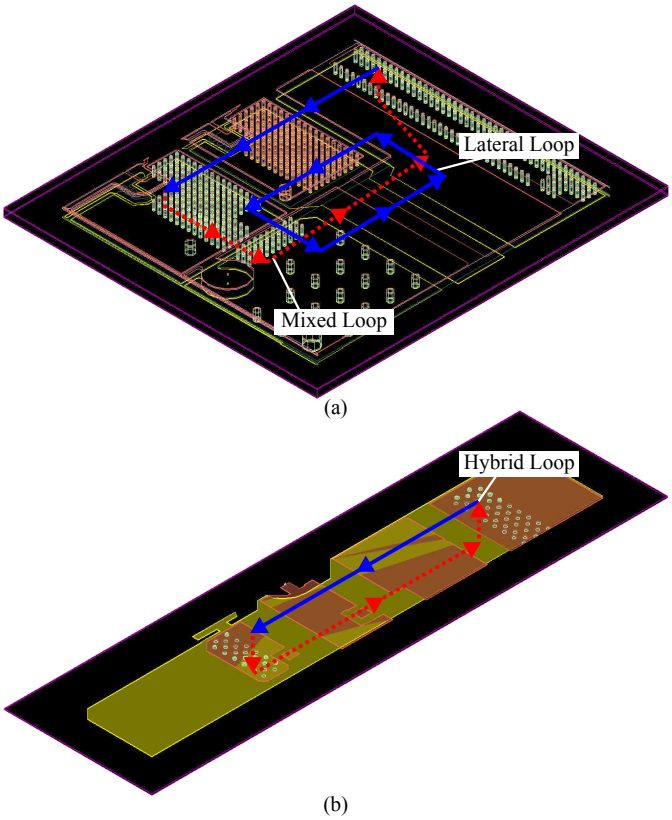

Figure 14. Power converters modelled in ADS: (**a**) bottom-side cooled converter; and (**b**) top-side cooled converter. The top-side currents are drawn using blue lines. The currents that flow through inner layers are drawn using red dashed lines.

The two PCBs had the same electrical and physical parameters. Both PCBs consisted of 4 layers. All copper layers had a thickness of 35 µm. The dielectric was FR4 material. The distance between the top layer and the nearest inner layer was 0.11 mm. The distance between the bottom layer and the closest inner layer was also 0.11 mm. The distance between the inner layers was 0.8 mm. The diameter of the vias was 0.3 mm.

Figure 15 shows the results of the electromagnetic simulations. Specifically, the impedance modulus of the two PCBs is shown. The impedance of both boards is similar at low frequencies, but its value increases along with the frequency. From 200 kHz onward, the impedance of the bottom-side cooled converter starts to grow significantly. However, the impedance of the top-cooled converter is more stable since it begins to grow at 10 MHz. The parasitic inductance values were calculated using these impedances and Equation (25). The resistance of the PCBs is equal to the impedance at low frequencies. Therefore, the bottom-side cooled converter exhibits a parasitic resistance of 1.3 mΩ, whereas the top-side cooled converter presents a resistance of 3.7 mΩ. The parasitic inductances at different frequencies can be determined once the parasitic resistances are known. At 1 MHz, the bottom-side cooled converter has an inductance of 5.5 nH, whereas the top-side cooled converter exhibits an inductance equal to 0.85 nH. The bottom-side cooled converter features a parasitic inductance 6.47 times larger than the top-side cooled converter due to its non-optimal power loop.

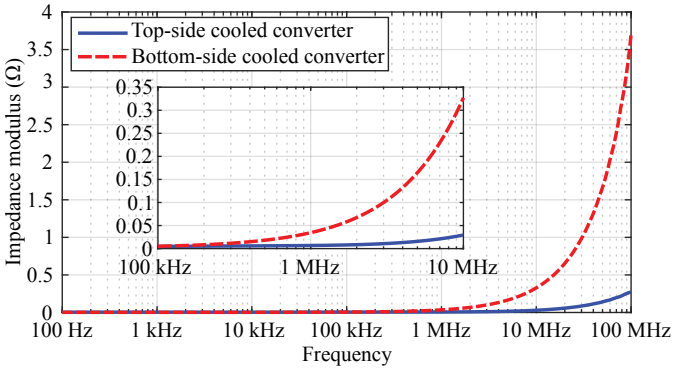

Figure 15. PCB impedances obtained from an electromagnetic simulation.

4. Experimental Results

To experimentally evaluate the analysed power converters, we used prototypes that incorporated the previously simulated GaN e-HEMTs (GS66508B and GS66508T). The prototype that dissipates heat using thermal vias uses the GS66508B-EVBDB1 daughter boards, marketed by GaN Systems. The top-side cooled power converter is a proprietary design and uses the transistors GS66508T. Figure 16 shows the studied converters.

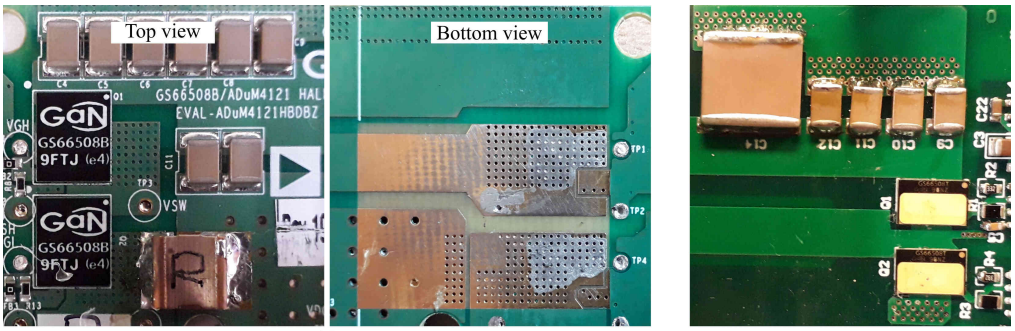

Figure 16. View of the GaN-based power converters: (**a**) bottom-side cooled converter; and (**b**) top-side cooled converter.

The prototypes consisted of a GaN single-phase inverter, a step-down transformer, and a rectifier formed by SiC diodes, as shown in Figure 10. The DC side of the GaN inverter was supplied by a constant DC source. On the DC side of the SiC rectifier, there was a single-phase series-connected R load. Bipolar pulse width modulation was implemented on a dSPACE DS1006 platform and a DS5203 FPGA board. Voltages were measured with a high-resolution oscilloscope (Agilent InfiniiVision MSO7104A: 1 GHz bandwidth and 4 GS/s sample rate), and voltage passive probes (Agilent 10073D: 500 MHz bandwidth). Thermograms were obtained using a thermal camera (Fluke Ti480 PRO). The obtained thermograms were processed with Fluke Connect software to more accurately determine the converter temperatures. The ambient temperature was controlled and equal to 25 ºC. Table 4 summarises the performed experiments.

The first experiment was conducted to analyse the parasitic inductance of the converters. Figure 17 illustrates the method used to measure the voltage ringing, while Figure 18 shows the drain-source voltages obtained. There is no significant difference between the rise times of the converters. The bottom-side cooled converter exhibited significantly more ringing than the top-side cooled converter. In the first converter, the ringing frequency was 133 MHz. However, there was practically no ringing in the last converter. The measured drain-source voltages showed that both transistors behaved as a second-order system. Therefore, the natural frequencies of both systems were determined using the measured voltages. The relationship between natural frequency and parasitic inductance is defined using

$$L_{pcb} = \frac{1}{C_{oss} \times \omega_n^2} \tag{26}$$

where ω_n is the natural frequency.

Table 4. Summary of the performed experiments.

Experiment	Bus Voltage (V)	Switching Frequency (kHz)	Deadtime (ns)	Output Power (W)	Figures
Parasitic inductance	100	100	40	108.1	Figure 18
Deadtime effect	280	100	40/100	432.4	Figure 19
No heatsink	140	400	40	108.1	Figures 20 and 21
With heatsink	250	400	40	574.5	Figures 22 and 23

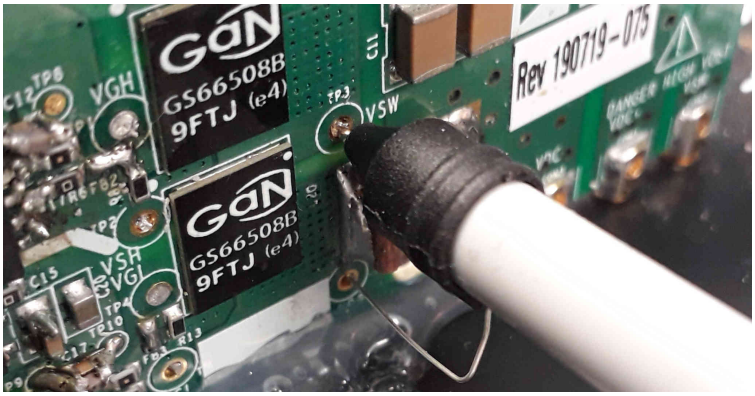

Figure 17. Drain-source voltage measurement technique.

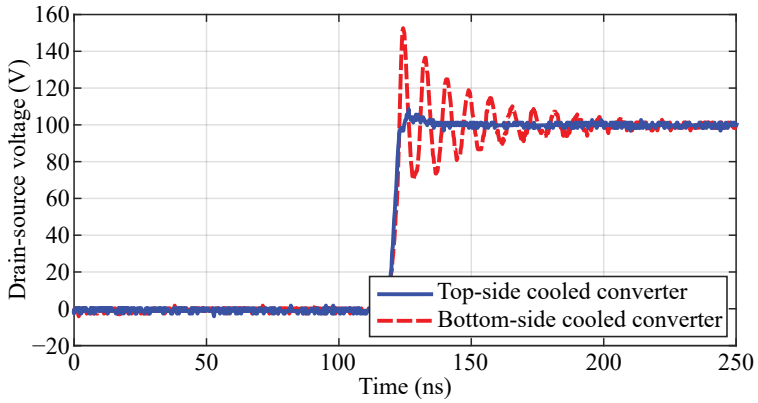

Figure 18. Comparison between the experimental drain-source voltages of the studied converters.

The parasitic inductances of the studied converters were determined using Equation (26). The bottom-side cooled converter featured a parasitic inductance equal to 4.84 nH, a value close to the one obtained by simulations. The top-side cooled converter exhibited an inductance of 0.57 nH, a value similar to that obtained analytically. Hence, the bottom-side cooled converter has a parasitic inductance 8.49 times higher than the top-dissipated converter. Table 5 summarises and compares all the obtained parasitic inductances.

Table 5. Power loop inductance comparison.

Dissipation System	Top-Side	Bottom-Side
Loop dimensions (mm) ($l \times w \times h$)	23.19 × 7.92 × 0.11	—
L_{pcb} with Equation (22) (analytical)	0.48 nH	—
L_{pcb} with Equation (24) (simulated)	0.85 nH	5.5 nH
L_{pcb} with Equation (26) (experimental)	0.57 nH	4.84 nH

To evaluate the deadtime effect on the temperature of GaN-based converters and, hence, on power losses, we implemented different deadtimes on the top-side cooled converter. The implemented deadtimes were 40 and 100 ns, while the switching frequency was 100 kHz.

Figure 19 shows the converter temperatures when using different deadtimes. Figure 19a shows the thermogram obtained using a deadtime of 40 ns. Heat flowed through the GaN e-HEMT to the PCB, so the space between the two GaNs had a high temperature. The hottest point of the GaN e-HEMTs was the thermal pad. The upper GaN pad had a temperature of 78.01 ºC, while the lower GaN pad was 82.46 ºC. Figure 19b illustrates the results obtained with a deadtime of 100 ns. This image displays higher temperatures than the previous thermogram because a high deadtime increases the losses and the temperature of the semiconductors. The warmest areas of the converter were again the thermal pads and the space between the GaN e-HEMTs. Since the temperature of the transistors was higher than at 40 ns, the heat spread further through the PCB. The upper GaN thermal pad was 84.73 °C, while the lower GaN pad was 89.41 °C. Hence, the thermal pads of the GaNs were at a temperature about 7 °C higher than at 40 ns. In both thermograms, the lower GaN e-HEMT is slightly hotter than the upper one due to the PCB layout. In this converter, there is an overlap between the phase and the ground plane. This overlap increases the C_{oss} capacity of the lower GaN and thus its losses.

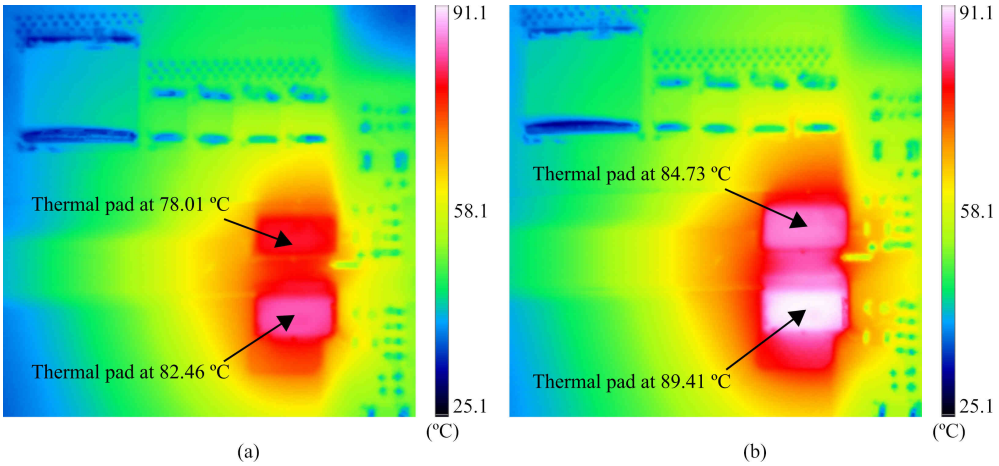

Figure 19. Thermal images of the GaN-based converter using different deadtimes: (**a**) 40 ns and (**b**) 100 ns.

With the following experiment, we analysed the behaviour of converters switching at high frequency and without a heatsink. In this scenario, the deadtime was 40 ns and the switching frequency was 400 kHz. Figures 20 and 21 display the thermograms of the studied converters.

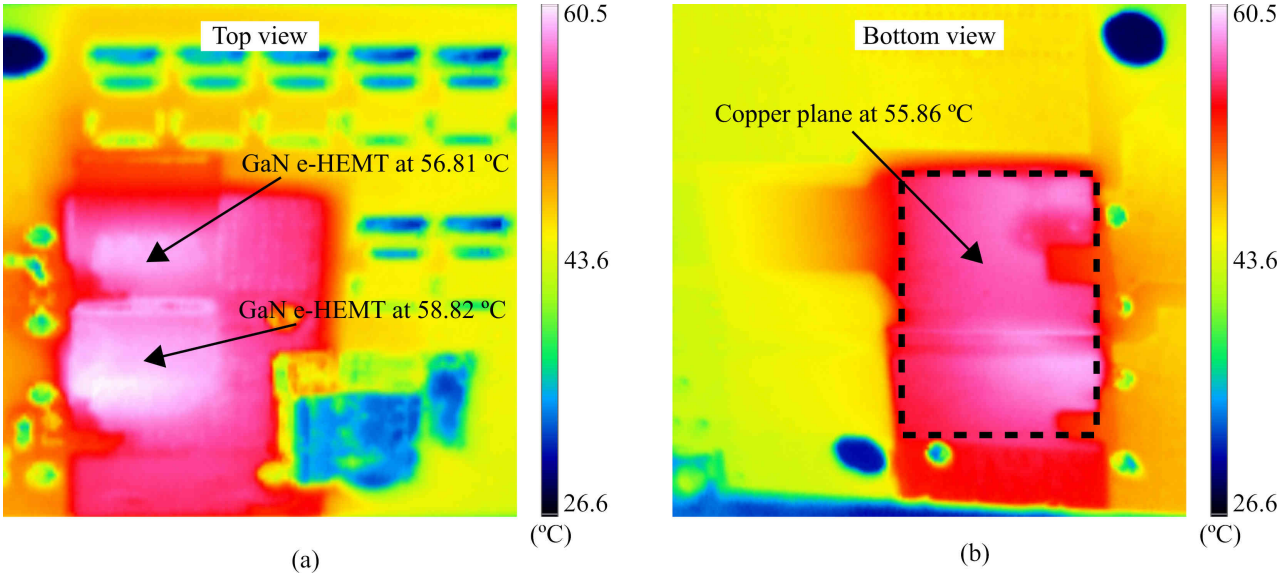

Figure 20. Thermogram of the bottom-side cooled converter without heatsink: (**a**) bottom view; and (**b**) top view.

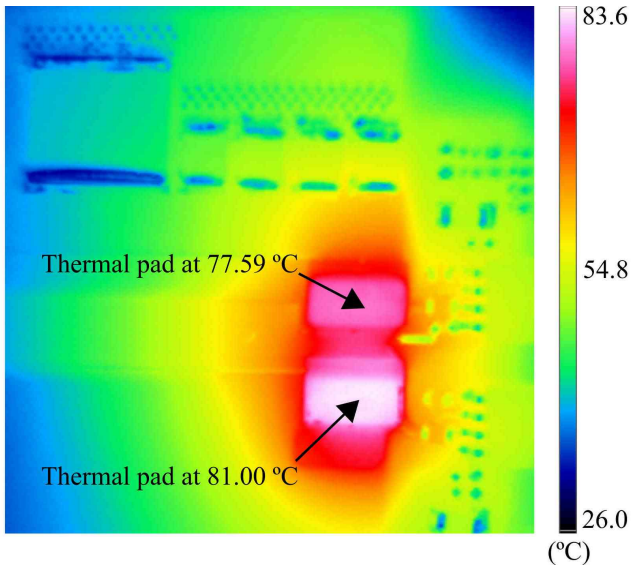

Figure 21. Thermogram of the top-side cooled converter without heatsink.

Figure 20 shows a thermogram of the bottom-side cooled converter. This converter had a thermal copper plane under each GaN to dissipate heat. The heat circulated across the plane and flowed through the thermal vias to the bottom layer. Figure 20a shows the thermogram from the top view. The GaN e-HEMTs were the hottest elements; the upper GaN was 56.81 ºC and the lower was 58.82 ºC. In this converter, there was also an overlap between the phase and the ground plane. Hence, the lower GaN e-HEMT exhibited additional losses and a slightly higher temperature than the upper transistor. In this thermogram, there is a well-defined hot zone around the GaN transistors. This zone is the thermal copper plane. Figure 20b shows a bottom view of the converter. On the bottom layer, there are other two copper thermal planes. These planes distribute the heat to facilitate its transmission to the TIM and the heatsink. The planes were 55.86 °C, slightly lower than at the GaN package. However, the temperature was not uniform within the copper. The thermal planes were hotter just below the GaNs, and the temperature was lower in the areas distant from the heat source.

Figure 21 depicts the thermogram of the top-side cooled converter. The thermal pads of the transistors were the warmest elements. The upper GaN pad was 77.59 ºC, while the

lower GaN pad was 81 ºC. The temperatures of this converter are higher than those of the bottom-side cooled converter since there is no heatsink. In the bottom-side cooled converter, the heat flows from the GaN e-HEMTs to the copper plane. Hence, the temperature of the GaN transistors is lower. Nevertheless, in the top-side cooled converter, the heat is dissipated essentially by convection. This dissipation is inefficient due to the small area of the GaN thermal pads.

With the last experiment, we studied the power converters operating with a heatsink. The switching frequency and deadtime were maintained at 400 kHz and 40 ns, respectively. The bottom-side cooled converter used a polymeric TIM (L37-5 Interface Material) with a thickness of 0.5 mm and a conductivity of 1.6 W/mK. The top-dissipated converter used different TIMs. The polymeric TIM mentioned before was tested, as well as a graphite-enhanced TIM (GCS-017). This last TIM featured a thickness of 0.017 mm and exhibited a conductivity of 11 W/mK. All converters used the same model of an aluminium heatsink without a fan.

Figure 22 illustrates the thermogram of the bottom-side cooled converter with a heatsink. Figure 22a is a top view of the PCB. As in the previous experiments, the transistors were the hottest elements of the converter. The upper GaN was 56.93 ºC, while the lower GaN was 59.14 ºC. The image also shows how the heat from the transistors flows through the copper thermal plane. Figure 22b is a bottom view of the converter. This thermogram shows the heatsink and its temperature. The average temperature of the heatsink was 41.63 °C at steady state.

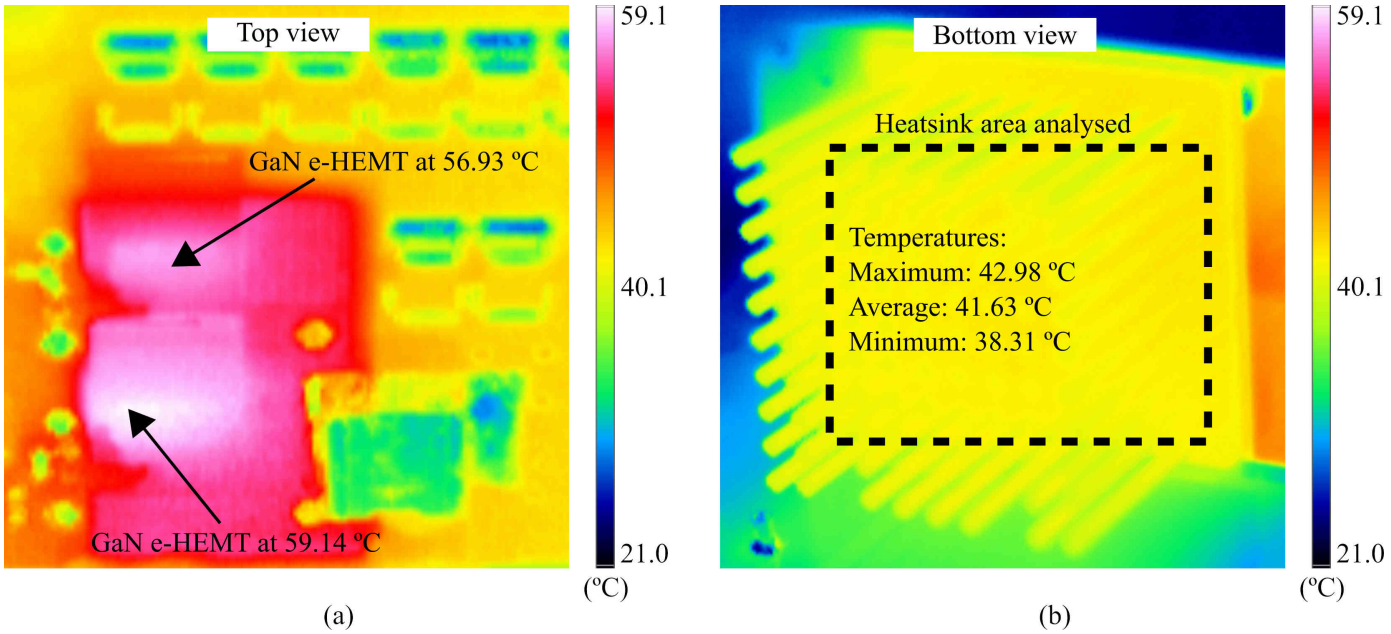

Figure 22. Thermal images of the bottom-side cooled converter: (**a**) bottom view and (**b**) top view.

Figure 23 depicts the temperatures of the top-side cooled converters with heatsinks. The PCB on the left dissipates heat using a graphite-enhanced TIM, whereas the PCB on the right uses a polymeric TIM. The converter with the graphite-enhanced TIM transmits heat better, so its heatsink is the warmest. This TIM is very thin and has an extremely high thermal conductivity in the plane. These two properties minimise the thermal resistance of the system and, therefore, improve heat dissipation. The converter with the polymeric TIM has a higher thermal resistance. This polymer TIM presents lower thermal conductivity, and it is also thicker. Consequently, the heat dissipation is worse, and the heatsink is slightly cooler.

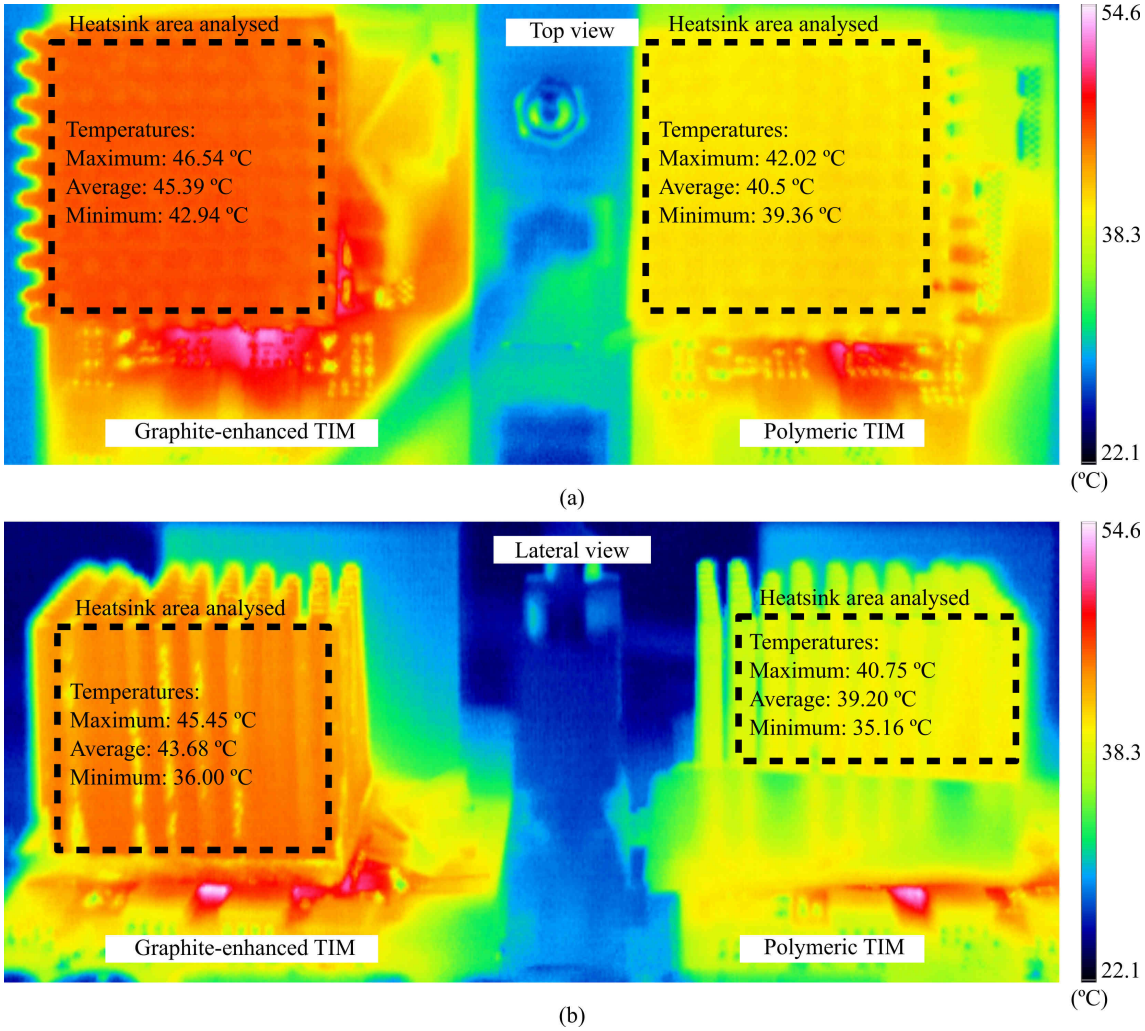

Figure 23. Thermal images of the top-side cooled converter: (**a**) top view and (**b**) lateral view.

5. Conclusions

In this study, we had evaluated different dissipation systems for GaN-based power converters. The dissipation and parasitic inductance of a top-cooled power converter and a bottom-cooled power converter had been analysed. We present a comprehensive model for GaN-based power converters to analyse the losses, the dissipation system and also the parasitic inductance. The dissipation strategies had been analysed by simulation and experimentation. The results had revealed the following:

1. Deadtime has a significant influence on losses, especially when working with high power;
2. Bottom-cooled power converters exhibit significant parasitic inductance and, therefore, high voltage ringing. This behaviour is due to the presence of thermal vias. The vias prevent the current from flowing directly below the transistors, so the power loop has to be closed over a longer path, which increases the parasitic inductance;
3. Top-cooled power converters allow for a more optimised layout than bottom-cooled converters since the former do not require thermal vias. Thus, the parasitic inductance may be minimal. However, due to the small size of GaN e-HEMTs, these converters require TIMs with high thermal conductivity to properly extract heat from the transistors.

Author Contributions: D.L. was mainly responsible for preparing the review paper and simulated the studied dissipation systems. J.J. and A.C. reviewed the different dissipation methods proposed in the industry. N.B. analysed the parasitic inductances through simulations. D.L. and M.V. performed the presented experiments. J.Z. revised and corrected the initial manuscript. All the authors performed the final check of the review. All authors have read and agreed to the published version of the manuscript.

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Abbreviations

The following abbreviations are used in this manuscript:

ADS	Advanced design system
EV	Electric vehicle
EMI	Electromagnetic interference
e-HEMT	Enhancement-mode high-electron-mobility transistors
IMS	Insultaded metal substrate
GaN	Gallium nitride
PLECS	Piecewise linear electrical circuit simulation
SiC	Silicon carbide
TIM	Thermal interface material
WBG	Wide-bandgap

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