Towards Efficient and Reconfigurable Next-generation Optical Fronthaul Networks for Massive MIMO

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ABSTRACT

This paper summaries our recent research on digital radio over fibre (DRoF) based optical fronthaul links and experimentally demonstrates a novel last-mile wireless coverage system incorporating data compression, time-division multiplexing (TDM) based packetization, and wavelength division multiplexing (WDM) based optical transmission. Compression reduces the fronthaul data rate required per service by a factor of 3 when compared with the common public radio interface (CPRI) standard, enabling efficient radio resource distribution over optical fibre infrastructure. The new packetization mechanism and WDM architecture enable fully reconfigurable resource allocation in a fronthaul network for 20MHz-bandwidth RF inputs with 64x64 MIMO carried over an aggregated compressed optical data rate of 32Gbps using 4 wavelengths. The experimental results show over 40dB RF dynamic range with < 8% error value magnitude (EVM) for the 64 quadrature amplitude modulation (64-QAM) input signals across all the WDM channels while the lowest EVM is less than 2%. Meanwhile, this field-programmable gate array (FPGA) based DRoF system allows flexible, software definable and easy-scalable dynamic antenna resource allocation.

Keywords: Digital Radio over Fibre (DRoF), 5G, massive MIMO, Fronthaul, WDM, Data Compression

1. INTRODUCTION

The growing demand for wireless capacity in the 5G radio access network (RAN) has driven the development of new designs and architectures for optical fronthaul links connecting centralised baseband units (BBUs) and remote radio units (RRUs). Common public radio interface (CPRI) based digital radio over fibre (DRoF) scheme for centralised RAN (C-RAN), which has been widely deployed for the 4G network, is facing a backlash for dealing with the high capacity demand in 5G over the concerns of the excessive overheads and stringent latency requirement [1]. Recent advancement in massive multiple input and multiple output (mMIMO) technology defined in the 5G NR standard poses new challenges for the fronthaul links in terms of bandwidth efficiency requirements [2]. In CPRI, carrying a single 20MHz bandwidth RF input requires a link capacity of 1.2288Gbps and the number will easily become hundreds of Gbps for a single 100MHz 5G input with mMIMO (e.g. 32x32 or 64x64) [3]. To resolve this issue, the emerging Evolved CPRI (eCPRI) based distributed RAN (D-RAN) is introduced and has become the predominant mobile access architecture in the current 5G rollout [4]. The advantage of D-RAN is that a new set of functional splits allows low bandwidth data transmission between central unit (CU) and distributed unit (DU) while high-speed CPRI transmission is only needed at the final drop.

However, the trade-off is the increased complexity in the DU and the remote units (RUs), which might drive the aggregated deployment and maintenance costs even higher in certain scenarios. Another hurdle is the difficulty of multi-vendor multi-operator interoperability using these protocols in a neutral host scenario as eCPRI/CPRI are mostly vendor-specific. The open RAN (O-RAN) alliance is formed attempting to promote the virtualised, interoperable and standardised RAN elements allowing seamless operation from discrete equipment vendors [5]. The three RAN architectures are shown in Figure 1. Although the open RAN is still under development and there is an ongoing debate of its efficiency due to the difficulties of building interoperable software platforms and the reluctance of participation from some major vendors, the cost reduction as a result of neutral hosting and the virtualisation of RAN components is foreseeable and generally agreed.

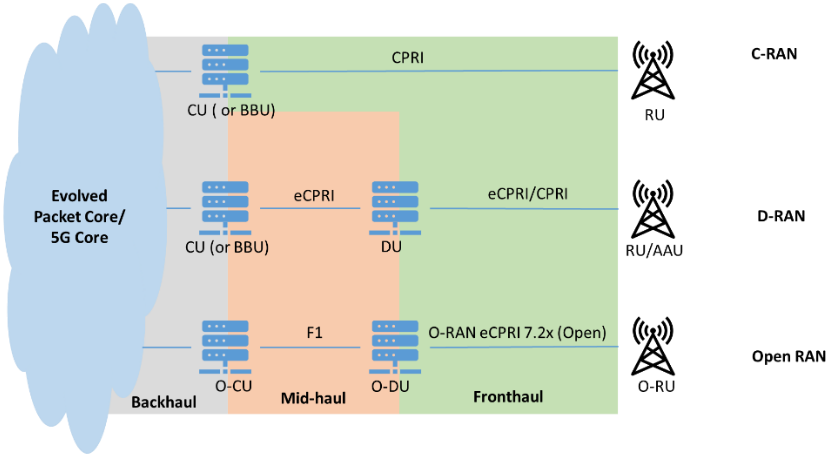

Figure 1. RAN Architectures

In this paper, we review our recent works on efficient and reconfigurable DRoF based fronthaul systems and propose a new fronthaul gateway for implementing mMIMO inputs using real-time FPGAs and wavelength division multiplexing (WDM) transmission. The system can support neutral hosting and virtualised RAN at the same time. The experimental results show proof of feasibility for implementing 64x64 MIMO 20MHz RF input and realising dynamic antenna resource allocation and distribution. To our knowledge, this is the first demonstration of its kind and could offer a promising solution for next-generation fronthaul networks.

2. REVIEW OF OUR RECENT WORKS ON DROF FRONTHAUL

Several previous studies have investigated data compression techniques over CPRI to reduce the link capacity requirement [6][7]. An alternative approach is applying compression for the raw digitised signals to improve the transmission efficiency without affecting the openness of the fronthaul interface and therefore allow neutral hosting. Our team previously demonstrated a data compression technique [8] and a neutral-host DRoF system [9] showing up to 3-times higher bandwidth efficiency than CPRI. 14 RF bands including MIMO channels are transported simultaneously over a single optical fronthaul link in a digital distributed antenna system (DAS). This efficient aggregation of services also enables flexible and cost-effective multi-service RF transportation over integrated microwave links using photonically-generated millimetre wave (mmW) or terahertz (THz) carriers to deal with the issue that installation of new fibres may be prohibitive [10][11]. Saving fibre consumption using multiplexing techniques are also studied in our past research works. A time-division multiplexing (TDM) based fronthaul protocol [9] and a space-division multiplexing (SDM) solution for integrated backhaul and fronthaul data using multicore fibres [12] are demonstrated.

On the virtualisation of RAN, given the surging of densified 5G cells, moving software-definable RAN control functionalities towards the mobile edge has recently become attractive for easing the traffic burden at the mobile core. Despite that softwarization has been recommended for the mobile edge networks in 5G, the fronthaul is mostly static to date with fixed links between BBUs and RRUs. Therefore, it is desirable to build a reconfigurable fronthaul architecture to perform dynamic edge traffic orchestration and coordination, and in the meantime, advanced functions such as coordinated multipoint (CoMP) and distributed MIMO can be made possible in such implementation. The reconfigurability can be achieved by either a packet-switched or a circuit-switched system. For packet switching, the IEEE 1914.3 working group has developed the radio over Ethernet (RoE) standard to implement CPRI/eCPRI over standard Ethernet [13]. The convergence of fronthaul and Ethernet allows statistical multiplexing operation for radio frames[14]. Nevertheless, the major drawbacks of this approach are the excessive Ethernet overheads and timing/latency issues introduced. We demonstrated a low-latency neutral-host RoE system incorporating data compression and time-stamped packetisation based on the real-time NetFPGA platform to improve the feasibility of the real-life deployment[15].

To achieve deterministic data transport, the time-sensitive network (TSN) with smart scheduling is recommended by IEEE 802.1CM for fronthualing when the traffic grows. To achieve this, a significant amount of development efforts is required on both RAN and Ethernet. Another option is to use circuit switching under the circumstances that real-time statistical multiplexing is not yet imperative because that the requirement of fast traffic shaping is still moderate to date. In this case, deployment of a circuit switching network is a sensible alternative for a reconfigurable fronthaul to completely avoid the latency caused by the store-and-forward operation for the Ethernet packets, although there is a setup time (typically millisecond/microsecond) before links are established. In [16][17], we use a silicon photonic (SiP) based micro-ring resonator (MRR) switch to optically re-route the unshaped fronthaul traffic in the electro-optical switch-and-select topology. The system is scalable and can potentially support >100 port counts, which means over 100 RU sites can be addressed simultaneously by a single photonic integrated chip (PIC). However, until now, these demonstrations are lab-based and there is still a product development cycle before large-scale industry-level SiP switches become available.

With regards to mMIMO, large antenna array-based mMIMO macrocells with beamforming have been deployed. Even so, the short transmission distance of 5G carriers is still a major obstacle for efficient usage of the mMIMO cells (i.e. capacity cannot reach users). The problem will be exacerbated for future millimetre wave (mmW) deployment. Smart relaying and distribution of the capacity produced from the mMIMO cells to the users is essential for the practical implementation of mMIMO cells. The WDM-PON based fronthaul has recently been widely studied and it offers a converged transport solution for mMIMO fronthauling with the existing fibre to the home (FTTH) infrastructure by virtually creating point-to-point links with independent wavelengths[18]. The main challenges of this approach are the loss and crosstalk introduced in PON which limits the number of channels supported, as well as the misalignment of RAN and PON standardisation roadmaps, especially for high data rates (>10Gbps) [19].

An evolution towards an overlaid reconfigurable RAN and WDM-PON architecture might overcome the issues. By leveraging the processing power in the RAN components and channel aggregation capability using WDM, in the following sections, we propose and demonstrate a reconfigurable DRoF fronthaul system incorporating commercially-off-the-shelf (COTS) FPGAs and CWDM devices to achieve high-efficiency and cost-effective mMIMO switching and distribution for next-generation fronthaul networks which creates a new paradigm for fronthaul network convergence and transportation with reconfigurability.

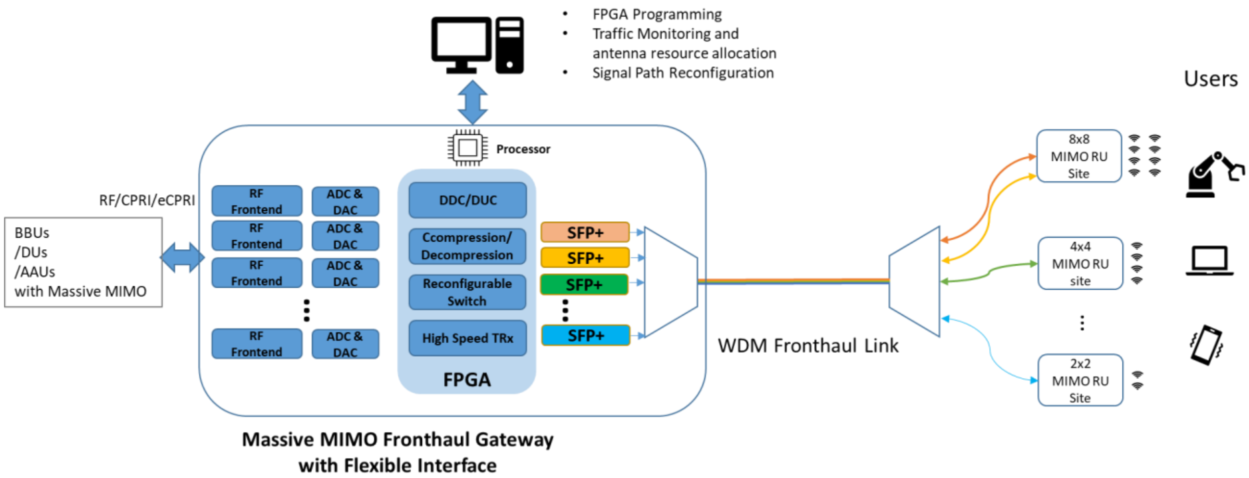

Figure 2. Reconfigurable Fronthaul Proposal for mMIMO

3. MASSIVE MIMO RECONFIGURABLE FRONTHAUL PROPOSAL

The concept of mMIMO fronthaul gateway is introduced as shown in the system proposal in Figure 2. The gateway can flexibly interface with CPRI, eCPRI, or direct RF inputs generated from BBUs, DUs, and active antenna units (AAUs). For the direct RF inputs, the RF frontend processing chains convert the signals to an intermediate frequency (IF), typically located at the centre of the first or second Nyquist Zone of the following high-resolution analogue-to-digital converters (ADCs). After digitisation, the raw digitised IF signals are digitally downconverted (DDC) to baseband and compressed to a low bit rate using our unique compression algorithm (as described in section 3.1) on an FPGA [8]. The resultant data are subsequently switched (as described in section 3.2) to the ports of high-speed FPGA transceivers where line coding and parallel to serial (P/S) conversion take place. An embedded system and FPGA programming software are used collaboratively to monitor the network traffic and thus configure the FPGA accordingly. Small form-factor pluggable plus (SFP+) modules with distributed feedback (DFB) lasers for coarse wavelength division multiplexing (CWDM) are employed to transport the data carried over optical carriers at specific wavelengths. The CWDM module aggregates the multiple wavelengths with 20nm separation onto a single fibre for fronthaul transmission.

At the remote end, the optical carriers at different wavelengths are firstly separated and then fed to the destination RU sites with variable capacity requirements. The numbers of MIMO antennas supported by the RU sites can be flexibly configured according to the user requirement. In a single RU site, multiple distributed RUs in a conventional distributed antenna system (DAS) can be deployed for extensive coverage. The RUs process the received signals in a reverse manner by converting the compressed IQ bitstreams back to the RF format before feeding into the corresponding MIMO antennas.

It is notable that, in respect of the input mMIMO channels, the fronthaul gateway is transparent except routing the MIMO antenna resource to the allocated destination for capacity distribution. And, for the CPRI/eCPRI inputs, FPGA-based intellectual property (IP) cores are available to process the frames allowing the following compression, switching, and transceiver operation to take place. The experiment in the next section mainly focuses on the direct RF inputs for neutral-host applications.

3.1. DRoF Data Compression Chain

Figure 3 shows the two-stage data compression processing chain aiming to reduce the data rate of the raw digital IF signal [9]. At the first stage, a digital automatic gain control (DAGC) module with fast settling time is introduced [20]. The module automatically adjusts the amplification gain to maintain signal power within a certain range. The signal is then rescaled to match the ADC full-scale range in order to maximise the quantisation compression ratio. The least significant bits (LSBs) are truncated to reduce the input bit width before the following DDC where the digital IF signal is downconverted to the baseband. In the case of 14/16-bit ADC quantisation, each IQ component is compressed to 8 bits. A carefully designed raise root cosine (RRC) filtering module with a steep cut-off is used within the DDC to remove the spectral redundancy of the signals so that a second compression stage narrows down the IQ baseband sampling window. For example, the filtering process allows a >6x decimation in the case of a 20MHz bandwidth input with a 150Msamples/s sampling clock.

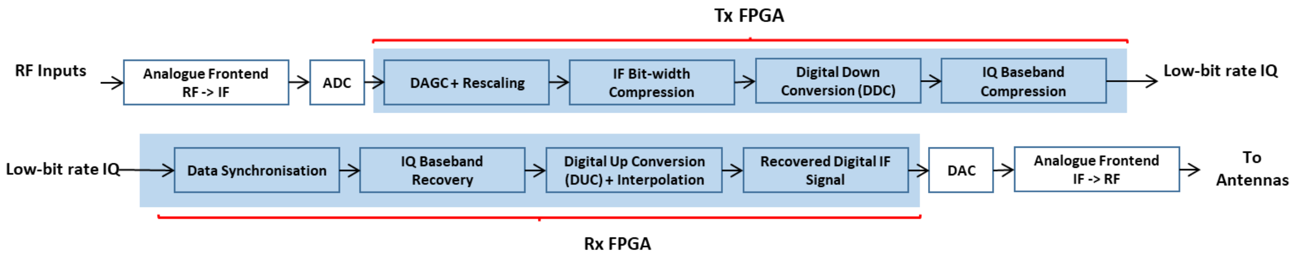

Figure 3. The Data Compression Chain

After transmission, the low-bit-rate baseband signal is recovered in a reverse manner at the receiver side. Compared with the raw input, this technique can achieve over 5x overall compression ratio and shows that a 20MHz-bandwidth RF input only requires 400Mbps in the experimental demonstration. A higher compression ratio is also possible by trading off RF performance and dynamic range.

3.2. The FPGA Switching and Transmission Architecture

As shown in Figure 4, the compressed IQ data each with 8-bit quantisation width are passed to a channel switching module programmed on the FPGA fabric. This module can be reconfigured by programming the FPGA in a software platform to route the baseband signals to the desired destinations. By doing this, mMIMO resources are switched to dedicated ports before a TDM module aggregates the IQ data to a 32 bits stream allowing a 32-bit FPGA transceiver to perform P/S conversion, synchronisation and line coding (8B/10B or 64B/66B). In the case shown in Figure 4, each 8Gbps stream at the transceiver output can accommodate 16 20MHz RF streams or 320MHz spectral bandwidth.

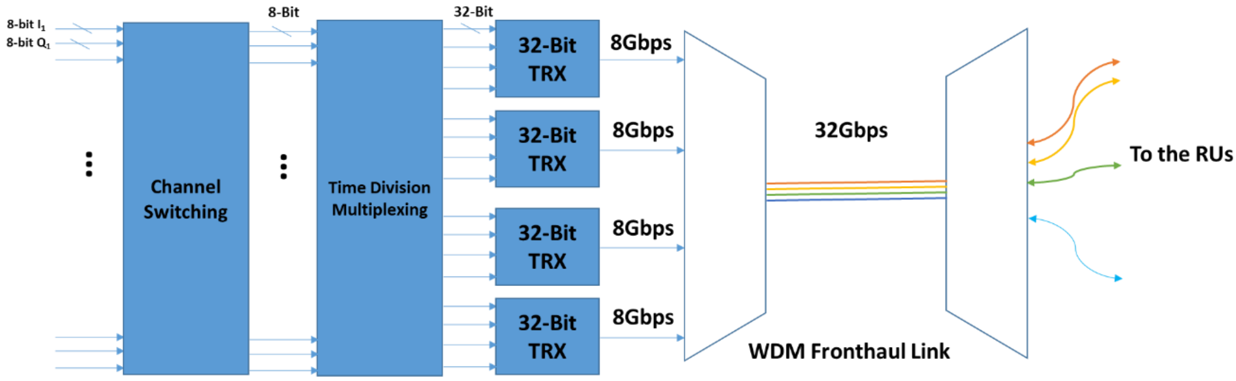

Figure 4. The FPGA Switching and Transmission Architecture

Four transceivers blocks are activated in this paper to demonstrate the transmission of 64 streams of 20MHz RF inputs (i.e. 64x64 MIMO or 1.28GHz spectrum w/o MIMO). The four channels are E/O converted with dedicated CWDM wavelengths in the SFP+ modules for multiplexing over a single fibre. This new way of channel aggregation saves the number of wavelengths needed for the WDM transmission and enables software-defined resource allocation on the FPGA.

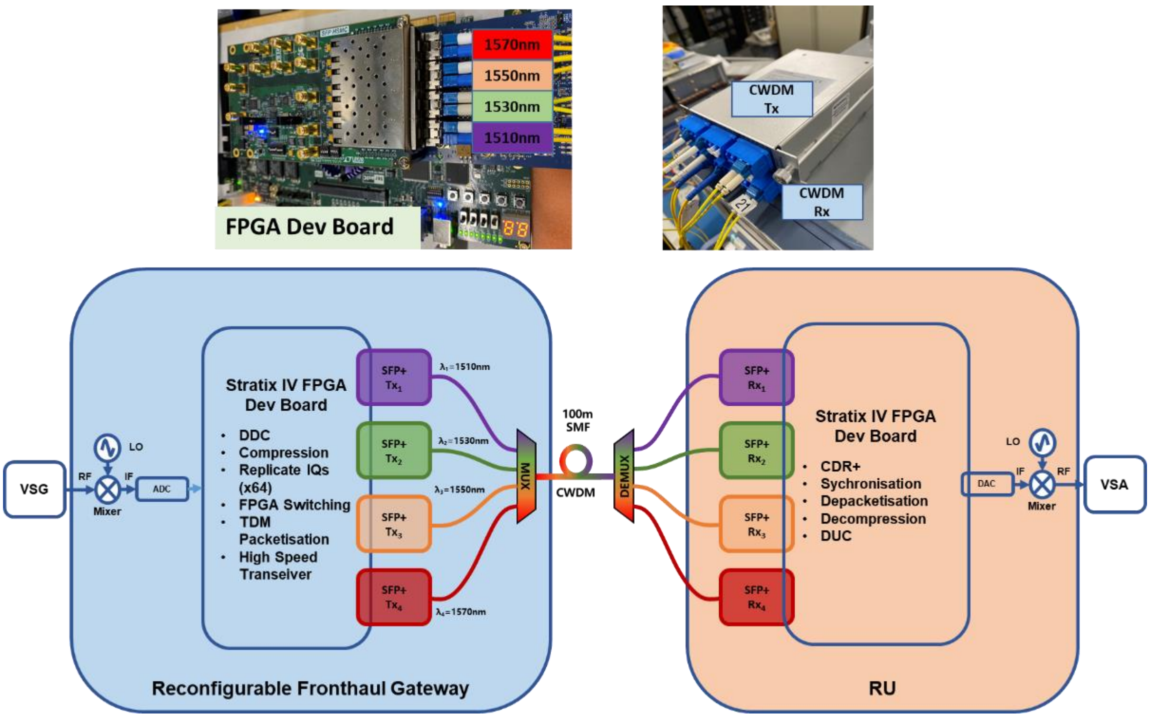

Figure 5. The Experimental Setup

4. EXPERIMENTAL SETUP AND RESULTS

An experiment is carried out to provide a feasibility study and evaluate the performance of the proposed mMIMO fronthaul gateway and CWDM fronthaul link mentioned in Section 3. Figure 5 depicts the experimental setup with the details of the processing modules in the optical and electrical domain. A single 20MHz 4G-LTE stream with 64 quadrature amplitude modulation (64-QAM) and a carrier frequency at 1.8GHz is generated by the Rhode & Schwarz (R&S) SMW200A vector signal generator (VSG). At the reconfigurable fronthaul gateway, the signal is then down-converted to a 37.5MHz intermediate frequency (IF) using an RF mixer. A pair of 14-bit 150Msamples/s ADC and DAC is implemented for mutual digital and analogue format conversions while the digitised RF signals are processed by Intel's Stratix IV FPGA development board for data compression, channel switching and packetization before optical transmission. With compression, each LTE stream is compressed by 5.25x to an 8-bit IQ baseband signal with a 25MHz sampling frequency (i.e. 400Mbps per channel).

On the FPGA, the data streams are replicated 64 times to emulate the 64x64 MIMO scenario and then switched and multiplexed to the desired destinations by establishing software programmable connections among dedicated registers using Intel's Quartus Prime FPGA software platform where all the 64 channels can be flexibly switched to the target transceiver channels. In the high-speed FPGA transceiver module, the data streams are firstly P/S converted and a synchronisation code (K28.5) is added at each channel. For better transmission efficiency, the code is added for every 1000 IQ samples to create a synchronizable TDM frame before 8B/10B coding takes place. Four 32-bit FPGA embedded transceivers are used to transport the 64 8-bit IQ channels. The resultant data rate at the output of each FPGA transceiver is 8Gbps carrying 16 channels of the original LTE inputs.

By using 10G CWDM SPF+ modules for the E/O conversions, four dedicated CWDM wavelengths are applied for optical transmission at 1510nm, 1530nm, 1550nm and 1570nm respectively. The signals are then fed to a pair of 8+1ch CWDM modules for (de-)multiplexing, which is connected via a 100m single-mode fibre (SMF), creating a 32Gbps converged optical fronthaul link.

At the RU side, the receiver FPGA performs clock data recovery (CDR), synchronisation, depacketisation, decompression, and digital up-conversion (DUC) to recover the signal back to the original IF format which is subsequently upconverted to an RF at 1.8GHz by an analogue mixer, followed by the performance measurement using the R&S FSQ vector signal analyser (VSA).

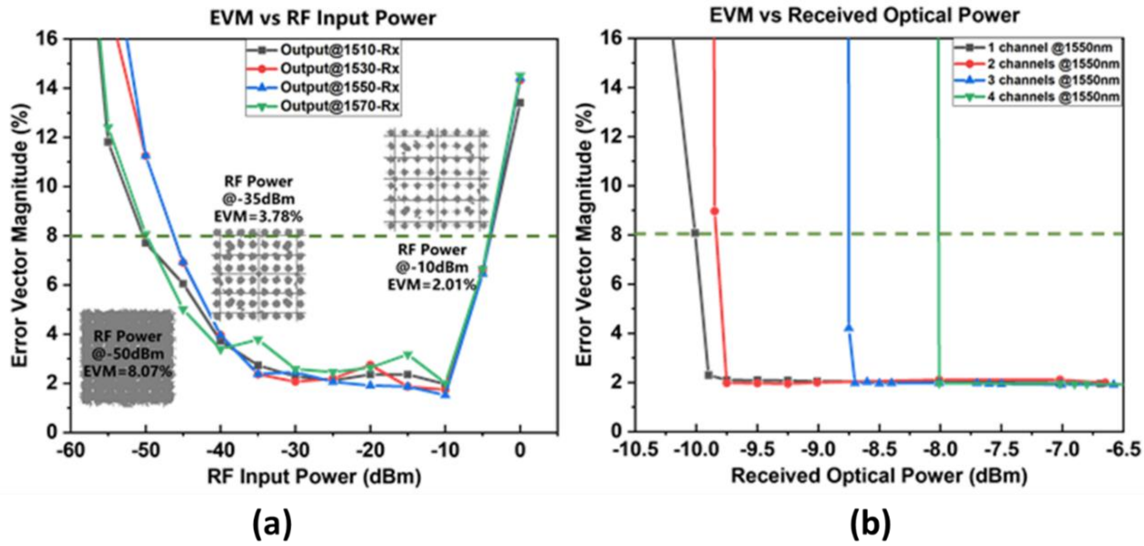

Figure 6. The Experimental Results (a) EVM vs RF Input Power (b) EVM vs Receiver Optical Power

Fig 6(a) illustrates the error vector magnitude (EVM) curves and constellation diagrams of a single replicated MIMO channel recovered at the receiver RU while all four CWDM wavelengths are employed. Dynamic range is a crucial figure which repeatedly emphasised by mobile network operators (MNOs) during the conformance testing. Typically frontend automatic gain control (AGC) unit is employed to improve the dynamic range. However, it is still essential for the digital processing units and optical transportation to maintain a high level of performance in a dynamic environment. The experimental results show that the RF input power dynamic range is >40dB with a minimum EVM floor of ~1.8% for <8% EVM requirement specified by 3GPP for the 64QAM scenario, without an external AGC [21].

To evaluate the dynamic range in the optical domain and the impacts induced by the crosstalk in the WDM system, the optical power dynamic range under different WDM scenarios are also measured in respect of the 1550nm channel as shown in Figure 6(b). Without optical amplification, the received optical power is around -6.5dBm before the SFP+ Rx module. We gradually reduce the power using a variable optical attenuator (VOA) to measure the optical dynamic range. For a single 1550nm transmission, the rapid increase of EVM occurs below -10dBm showing a 4dB optical link budget available for additional optical transmission system and processing using the given SFP+ transceiver. When 1530nm, 1550nm, 1570nm are consecutively added into the CWDM system, the sharp increase shifts to -9.8dBm, -8.7dBm, -8dBm respectively due to the interchannel crosstalk. A total 2dB power budget is observed for simultaneous transmission of all four wavelength channels. Notably, the sensitivity performance is mainly limited by the CWDM SFP+ transceiver used in this experiment and using SFP+ transceiver modules with higher sensitivity will further extend the optical power dynamic range and thus the scalability of the system.

5. CONCLUSION

In 5G and beyond, the existing fixed fronthaul links are not able to meet the growing last-mile traffic shaping requirement. In this case, reconfigurable fronthaul links are required to enable robust edge-based capacity manipulation and traffic management. This paper reviews our recent research on the DRoF based fronthaul systems and experimentally demonstrates a novel reconfigurable FPGA-based fronthaul system for mMIMO services with COTS components. By incorporating FPGA-based data compression, channel switching and multiplexing as well as CWDM operations in an integrated fronthaul gateway, high-capacity mMIMO antennas can be efficiently delivered to the end-users with variable capacity requirements through a software defined network at the mobile edge.

The experimental results show simultaneous transmission of 64 streams of 20MHz-bandwidth RF service with low crosstalk, over 40dB RF dynamic range and lowest EVM <2%. With the optical power budget demonstrated, which can be further improved by using transceivers with better sensitivities, long-distance transmission and additional optical processing are made possible. The system is also scalable by using concatenated FPGAs connected through high-speed interfaces or high-port count photonic switches to further enhance the overall capacity that the system can handle. Future work will investigate the capacity enhancement schemes as well perform performance evaluation of edge-based CoMP and distributed MIMO scenarios in such implementation.

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