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IEEE Transactions on Energy Conversion

DOI:
https://doi.org/10.1109/TEC.2021.3130492

E-pub ahead of print: 24/11/2021

Peer reviewed version

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Quasi Type-1 PLL With Tunable Phase Detector for Unbalanced and Distorted Three-Phase Grid

Hafiz Ahmed, *Senior Member, IEEE*, Zoheir Tir, *Senior Member, IEEE*, Anant Kumar Verma, *Member, IEEE*, Seifeddine Ben Elghali, and Mohamed Benbouzid, *Fellow, IEEE*

***Abstract*—Out of various moving average filter (MAF)-based phase-locked-loop (PLL), quasi type-1 PLL (QT1-PLL) is widely adopted due to its fast dynamic performance, implementation simplicity, and harmonics rejection abilities. However, the performance of QT1-PLL deteriorates in the presence of an off-nominal frequency unbalanced grid voltage component. Moreover, the sensitivity towards the fundamental frequency negative sequence (FFNS) component is high. Hence, this paper proposes a novel enhanced QT1-PLL solution that is insensitive to unbalance in the grid voltage signal during off-nominal frequency conditions. The proposed adaptive phase detector makes it possible to estimate both the fundamental frequency positive sequence (FFPS) and FFNS components with a high degree of immunity against harmonics. Notably, the pre-loop separation of the FFPS and the FFNS components helps suppress the second harmonic oscillations for improving the parameter estimation accuracy. The loop-filter design of QT1-PLL remains unaffected and requires a proportional gain to estimate the fundamental phase and frequency information. To address the DC offset issue, a modified delayed signal cancellation method is also proposed, which can theoretically eliminate the DC offset for any arbitrary delay length. A small-signal model of the proposed PLL is developed for the sake of stability analysis. Comparative numerical simulation and experimental results are provided with various variants of QT1-PLLs to demonstrate the performance improvement achieved with the proposed technique.**

***Index Terms*—Phase locked-loop, delayed signal cancellation, moving average filter.**

Manuscript received June 15, 2021; revised October 9, 2021; accepted November 20, 2021. The work of H. Ahmed was supported through the Sêr Cymru Programme by Welsh European Funding Office (WEFO) under European Regional Development Fund (ERDF). The experimental part of the present work was supported by the General Directorate of Scientific Research and Technological Development through the Ministry of Higher Education and Scientific Research of Algeria under Grant A01L07UN390120180001. Paper no. TEC-00636-2021.

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Digital Object Identifier 10.1109/TEC.2021.3130492

I. Introduction

THE penetration of grid-interfaced power electronic converters into traditional electric power grid is increasing day-by-day. They are used for various purposes such as grid-integration of distributed energy resources [1]–[5], power quality improvement [6], supplying domestic and industrial loads [7], charging electric vehicles [8], to name a few. These applications require grid-synchronous operation of the converter with the grid. This process is commonly known as grid-synchronization in the literature. Grid-synchronization necessitates the real-time extraction of unknown grid voltage parameters. As a result, a significant research attention has been given to this problem in the last few decades.

Many fast, efficient, and accurate techniques are already reported in the literature. Out of them, phase-locked loop (PLL) [9]–[13] and it's various variants are particularly popular. Traditional synchronous reference frame-PLL (SRF-PLL) uses Park's transformation as the phase detector and uses a proportional-integral low-pass filter to estimate the unknown grid frequency and phase. The SRF-PLL has fast convergence speed and good disturbance rejection capability. However, this PLL is designed for a balanced grid i.e. only the fundamental frequency positive sequence (FFPS) component is present. In practice, especially at the distribution network level, the grid often has a level of phase unbalance, e.g., more than 50% of the 800 low voltage substations in Cardiff, U.K. have serious phase unbalance [14]. So, enhanced filtering capability is essential to ensure efficient operation of PLL under the presence of phase unbalance i.e. both FFPS and fundamental frequency negative sequence (FFNS) components exist simultaneously.

In the presence of phase unbalance, the phase detector of SRF-PLL generates an undesirable double frequency components. To eliminate the undesirable components, several solutions propose the application of additional filtering stage(s) through pre-loop, in-loop and a combination of both. In the case of pre-loop, filters are applied in the stationary reference frame, i.e., $\alpha\beta-$frame where as in-loop filters are applied in the synchronous reference frame, i.e., $dq-$frame. In the case of hybrid filtering, filters are applied at both stationary and synchronous reference frames.

Some popular filters proposed in the literature are: delayed signal cancellation (DSC) [15]–[17], complex coefficient filter (CCF) [18], [19], moving average filter [20]–[24], orthogonal signal generator (OSG) filter such as second-order generalized integrator (SOGI) [25], adaptive notch filter (ANF) [26], to

name a few. In addition to the filter-based SRF-PLLs, multiple reference frame-based SRF-PLLs such as double decoupled SRF-PLL [27] are also popular in the literature.

Delayed signal cancellation (DSC) [15]–[17], [28] is a popular technique to eliminate the FFNS from the measured grid voltages at the point of common coupling. In order to make DSC-PLL immune to harmonics, multiple DSC operators are used in cascade. So, prior information about the grid harmonics is needed.. Moreover, in the case of off-nominal frequency operation, frequency-adaptive DSCs are proposed [29]. This can potentially increase the computational complexity. By using cross-coupling between two CCF, CCF-PLL [18], [19] can extract grid-synchronized FFPS and FFNS components. CCF is very suitable for selective harmonic elimination. However, multiple CCFs are required to eliminate the effect of harmonics which causes additional computational burden.

OSG-PLLs operate in the stationary reference frame, i.e., $\alpha\beta-$frame and uses OSGs to separate the FFPS and FFNS components followed by traditional SRF-PLL. OSGs typically have band-pass (*cf.* SOGI [25]) or notch (*cf.* ANF [26]) characteristics. To enhance the harmonic robustness of OSG-PLLs, multiple parallel OSGs are often recommended in the literature [30]. This can be computationally complex. Moreover, discretization of parallel OSGs is not straightforward, specially for high-order harmonics. Multiple reference frame PLLs use multiple SRFs to separate the FFPS and FFNS components. In the case of DDSRF-PLL, two cross-coupled reference frames operating at opposite instantaneous phases are used. This helps to make the PLL insensitive to FFNS components. However, the presence of harmonics and/or DC-offset deteriorates the performance. This necessitates the application of several reference frames where each operates at the relevant instantaneous phases. This kind of structure is complex and not suitable for low-cost embedded devices-based real-time implementation.

MAF-PLLs [20]–[24] provides an interesting solution to eliminate the effect of harmonics and/or DC offset. Here, MAF is used to eliminate the effect of FFNS component. Depending on the MAF window length, MAF-PLL can be very effective to block all harmonics and DC offset. However, this comes at the cost of slow dynamic response [20]. To enhance the convergence speed of MAF-PLL, quasi type-1-PLL (QT1-PLL) is proposed in [21]. The QT1-PLL uses the idea of frequency-adaptive demodulation [31]. An advantage of this approach is that only a proportional loop-filter can estimate the unknown grid-frequency whereas proportional-integral loop filter is required for conventional MAF-PLL. However, QT1-PLL is sensitive to off-nominal FFNS component. Since, fundamental frequency tuned MAFs are used in QT1-PLL, it cannot completely block the FFNS component if they appear at off-nominal frequency condition. To speed-up the convergence speed of QT1-PLL, hybrid QT1-PLL (HQT1-PLL) [22] is proposed. In this case, DSC operators are applied in the $\alpha\beta-$frame whereas MAF is applied in the $dq-$frame. However, fast dynamic response comes at the cost of sacrificing the high phase margin. Moreover, HQT1-PLL is also sensitive to off-nominal FFNS component. To reduce the effect of off-nominal frequency FFNS component sensitivity of QT1-PLL, total QT1-PLL (TQT1-PLL) is proposed in [24].

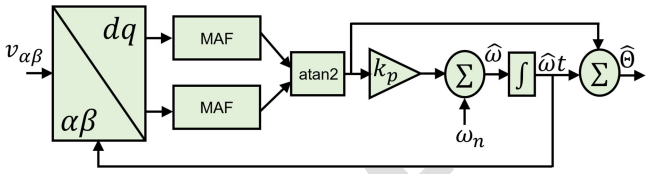


Fig. 1. Overview of QT1-PLL [21].

In this case, a third-order non-adaptive MAF is proposed. This MAF has same window length as QT1-PLL but has significantly lower steady-state errors in the presence of off-nominal FFNS component. However, this comes at the cost of high sensitivity to sub- and inter-harmonics. In [32], the authors have proposed the application of all-pass filter (APF) [33] as the sequence components separator for HQT1-PLL. Although this technique can reduce the sensitivity, however, APF on its own has limited filtering capability. This can be a limiting factor when the grid voltage has inter- and/or sub-harmonics components. Similar line of investigation is considered in [34] where third-order generalized integrator is considered as the pre-loop filter. It is to be noted here that none of the QT1-PLL techniques discussed in this section can extract the FFNS component with high degree of harmonic immunity. This limits their application where sequence extraction is important [35].

Comparative analysis in [23] shows that out of various MAF-PLLs, QT1-PLL is very suitable for grid-connected converters. This motivates the current work of improving the performance of QT1-PLL. Our main objective is to use QT1-PLL for FFPS and FFNS sequence extraction. For this purpose, an enhanced phase detector is constructed in this work. This phase detector can separate the FFPS and FFNS initial phase-angle and amplitudes. Output of the phase detectors are passed through a proportional loop-filter to estimate the unknown frequency and instantaneous phase of the grid voltage. A small-signal model is derived through analytical calculations and constructive gain tuning procedures are developed for the proposed enhanced QT1-PLL. Finally, the performance of the proposed technique is verified through simulation and experiments on a PWM-controlled voltage source inverter. In contrast to the conventional QT1-PLLs, the proposed approach is insensitive to off-nominal FFNS component. Moreover, it can extract FFPS and FFNS components unlike conventional QT1-PLLs. These are the main contributions of this work.

The rest of this paper is organized as follows: Section II summarizes the conventional QT1-PLL. Development of the proposed enhanced QT1-PLL is given in Section III. Results and discussions are given in Section IV. Finally, concluding remarks are given in Section V.

II. Quasi Type-1 PLL: Brief Overview

This section summarizes the basic idea of the conventional QT1-PLL as proposed in [21]. Block diagram of the QT1-PLL is given in Fig. 1. To analyze the phase detector of the QT1-PLL, let us consider the three-phase grid voltages in $\alpha,\beta-$frame as:

$$v_\alpha(t) = V\cos\left(\omega t + \phi\right), \tag{1}$$

$$v_\beta(t) = V \sin(\omega t + \phi), \tag{2}$$

where the amplitude, angular frequency, and the initial phase-angle are given by V, ω, and ϕ, respectively. The instantaneous phase of the signals (1) and (2) is given by $\Theta = \omega t + \phi \in [0, 2\pi)$. The voltages in (1) and (2) are converted into the synchronous reference frame (d, q) by applying the Park-type transformation and given by:

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\hat{\omega}t) & \sin(\hat{\omega}t) \\ -\sin(\hat{\omega}t) & \cos(\hat{\omega}t) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}. \tag{3}$$

From (3), the direct and quadrature-axis voltages can be rewritten as:

$$\begin{aligned} v_d &= v_\alpha \cos(\hat{\omega}t) + v_\beta \sin(\hat{\omega}t), \\ &= \frac{V}{2}\left[\cos\{(\omega - \hat{\omega})t + \phi\} + \cos\{(\omega + \hat{\omega})t + \phi\}\right] \\ &\quad + \frac{V}{2}\left[\cos\{(\omega - \hat{\omega})t + \phi\} - \cos\{(\omega - \hat{\omega})t + \phi\}\right]. \end{aligned} \tag{4}$$

$$\begin{aligned} v_q &= v_\beta \cos(\hat{\omega}t) - v_\alpha \sin(\hat{\omega}t), \\ &= \frac{V}{2}\left[\sin\{(\omega + \hat{\omega})t + \phi\} + \sin\{(\omega - \hat{\omega})t + \phi\}\right] \\ &\quad - \frac{V}{2}\left[\sin\{(\omega + \hat{\omega})t + \phi\} - \sin\{(\omega - \hat{\omega})t + \phi\}\right]. \end{aligned} \tag{5}$$

In the quasi-locked condition i.e. $\hat{\omega} \approx \omega$, it can be assumed that $\omega - \hat{\omega} \approx 0$. Then, (4) and (5) can be simplified as:

$$v_d \approx V \cos(\phi). \tag{6}$$

$$v_q \approx V \sin(\phi). \tag{7}$$

It is to be noted here that only when $\phi = \pm n\pi, n = 0, 1, 2, \ldots$, $v_d \approx V$ and $v_q \approx 0$ which is the same as the output of the phase detector of SRF-PLL [9]. From (6) and (7), the initial phase-angle can be estimated as:

$$\hat{\phi} = \text{atan2}(v_q, v_d), \tag{8}$$

where atan2 is the double quadrant arctangent function. In the above analysis, it is assumed that the grid is balanced and does not contain any harmonics. In practice, the grid is unbalanced, then, the FFNS component will appear as a double the fundamental frequency component in (6) and (7). Similarly, odd-order harmonics in the grid voltage will also appear as even-order harmonics in (6) and (7). These high frequency components will introduce ripple in the estimated phase-angle. Hence, the frequency even-order AC components can be filtered out by using a moving average filter (MAF) of window length, $T_w = T/2$, where T is the period of the fundamental component. The transfer function of the MAF in continuous and discrete-time are given by

$$G_{MAF}(s) = \left(1 - e^{-T_w s}\right)/T_w s. \tag{9}$$

$$G_{MAF}(z) = \frac{1}{N}\frac{1 - z^{-N}}{1 - z^{-1}}, \tag{10}$$

where $N = T/T_s$ with T_s being the sampling period. There are three major issues that affect the performance of the standard QT1-PLL. Firstly, the phase detector part does not use any gain i.e. no design freedom. Secondly, off-nominal frequency negative-sequence component will introduce high frequency ripple in the estimated phase. Finally, it is not capable of extracting the FFNS component. These issues will be addressed in the next section.

III. Enhanced QT1-PLL

In this section, the proposed modifications are detailed. First, the development of the proposed modified delayed signal cancellation (DSC) is detailed. Then, tunbale phase detector is given followed by the small-signal model-based stability analysis and tuning of the proposed PLL. For the remainder of this Section, let us consider the unbalanced grid voltages in the $\alpha\beta-$frame as:

$$v_\alpha = V_\alpha^0 + V^+ \cos\left(\omega t + \phi^+\right) + V^- \cos\left(\omega t + \phi^-\right), \tag{11}$$

$$v_\beta = V_\beta^0 + V^+ \sin\left(\omega t + \phi^+\right) - V^- \sin\left(\omega t + \phi^-\right), \tag{12}$$

where DC offsets are denoted by V_α^0 and V_β^0, the superscript $+$ and $-$ indicate the positive- and negative-sequence component and the remaining variables retain the same meaning as defined in Section II.

A. DC Offset Rejection

To reject DC offset, half-cycle DSC is a popular solution in the literature [22], [24], [28], [32]. In this work, we are considering a modified version of the DSC method for DC offset rejection. For this purpose, let us consider the delayed versions of the signals (11) and (12) as given below:

$$v_l^{nt_d} = v_\alpha(t - nt_d), \tag{13}$$

for $l \in \{\alpha, \beta\}$, $n = 1, 2$ with t_d being the basic time delay. Let us denote the DC offset-free version of the signals (11) and (12) as $v_\alpha^\emptyset$ and $v_\beta^\emptyset$. Then, these signals can be estimated using (11), (12), and (13) as given below:

$$v_l^\emptyset = v_l + \frac{0.5}{\cos(\omega t_d) - 1}\left(v_l - 2\cos(\omega t_d)\, v_l^{t_d} + v_l^{2t_d}\right). \tag{14}$$

Using (14), DC offset-free signals can be estimated using any arbitrary amount of time-delay as opposed to the half-cycle delay requirement of traditional DSC method. To implement (14), real-time information of the grid frequency ω is required. However, real-time frequency adaptation can complicate the modeling and tuning process. As such, frequency-fixed version of (14) is considered similar to [22], [24], [32] where the frequency ω is substituted by its nominal value. However, this will introduce amplitude and phase attenuation in the off-nominal frequency condition. So, compensation of these deviations need to be considered. For this purpose, transfer function of the filter (14) needs to be considered. Then, based on the developed transfer function, quantification of the amplitude and phase attenuation need to be studied. Filter (14) has the same transfer function of convention half-cycle DSC if $t_d = T/4$ is considered. For this value of t_d, the total delay of the proposed DSC filter (14) is the same as the standard DSC, i.e., $T/2$. As such, this value of t_d is selected. For this value, transfer function of (14) in the

phasor-form is given by:

$$G_{DSC}^{\alpha\beta}(s) = \left(1 - e^{-2t_d s}\right)/2. \tag{15}$$

Let us consider that $\omega = \omega_n + \Delta\omega$, where ω_n is the nominal value and $\Delta\omega$ is the deviation. Then, the amplitude and phase of transfer function (15) can be found as [36]:

$$\left|G_{DSC}^{\alpha\beta}(s)\right| \approx 1 - k_v \left(\Delta\omega\right)^2, \tag{16}$$

$$\angle G_{DSC}^{\alpha\beta}(s) = -k_\phi \Delta\omega, \tag{17}$$

where $k_v = T^2/32$ and $k_\phi = T/4$. From (16) and (17), it is clear that in the off-nominal frequency case, amplitude and phase attenuation are characterized by k_v and k_ϕ. As such, compensation of these pre-loop filter induced attenuation need to be considered in the in-loop of the PLL. It is to pointed out here that as a particular case of (14), convention half-cycle DSC filter can be be obtained. However, unlike conventional DSC, (14) can eliminates DC offset for any value of t_d. Moreover, despite the transfer functions being equal for $t_d = T/4$, the dynamic response is not the same for our DSC and the conventional counterpart.

Transfer function (15) in the dq-frame is given by:

$$G_{DSC}^{dq}(s) = \left(1 + e^{-2t_d s}\right)/2. \tag{18}$$

Transfer function (18) will be used for small-signal modeling purpose later in Section III-C.

B. Tunable Phase Detector

To develop the phase detector with tunable gain, let us consider the offset-free signal in (11) and (12), i.e., $v_\alpha^{\emptyset}$ and $v_\beta^{\emptyset}$. By applying basic trigonometric identities, expressions of $v_\alpha^{\emptyset}$ and $v_\beta^{\emptyset}$ can be expanded and rewritten into the parametric form as [37], [38]:

$$v_\alpha^{\emptyset} = \Omega_\alpha^T \theta_\alpha, \tag{19}$$

$$v_\beta^{\emptyset} = \Omega_\beta^T \theta_\beta, \tag{20}$$

where

$$\Omega_\alpha = \Omega_\beta = \left[\cos\left(\omega t\right)\ \sin\left(\omega t\right)\right]^T,$$

$$\theta_\alpha = \begin{bmatrix}\theta_{\alpha 1}\\ \theta_{\alpha 2}\end{bmatrix} = \begin{bmatrix} V^+\cos\left(\phi^+\right) + V^-\cos\left(\phi^-\right)\\ -V^+\sin\left(\phi^+\right) - V^-\sin\left(\phi^-\right)\end{bmatrix},$$

$$\theta_\beta = \begin{bmatrix}\theta_{\beta 1}\\ \theta_{\beta 2}\end{bmatrix} = \begin{bmatrix} V^+\sin\left(\phi^+\right) - V^-\sin\left(\phi^-\right)\\ V^+\cos\left(\phi^+\right) - V^-\cos\left(\phi^-\right)\end{bmatrix},$$

with the unknown parameter vectors being denoted by θ_α, θ_β while Ω_α and Ω_β denote the known information vector. To estimate the unknown parameter vectors θ_α and θ_β from the measured voltages v_α and v_β, let us consider the estimated voltages as $\hat{v}_\alpha^{\emptyset} = \Omega_\alpha^T \hat{\theta}_\alpha$and $\hat{v}_\beta^{\emptyset} = \Omega_\beta^T \hat{\theta}_\beta$. Let us define the parameter vector estimation error as $\tilde{\theta}_\alpha = \theta_\alpha - \hat{\theta}_\alpha$ and $\tilde{\theta}_\beta = \theta_\beta - \hat{\theta}_\beta$. Then, the output estimation error can be written as:

$$\tilde{v}_\alpha^{\emptyset} = v_\alpha^{\emptyset} - \hat{v}_\alpha^{\emptyset} = \Omega_\alpha^T \tilde{\theta}_\alpha. \tag{21}$$

$$\tilde{v}_\beta^{\emptyset} = v_\beta^{\emptyset} - \hat{v}_\beta^{\emptyset} = \Omega_\beta^T \tilde{\theta}_\beta. \tag{22}$$

Let us consider the following Lyapunov-like function with $k_e > 0$:

$$V\left(\tilde{\theta}_\alpha, \tilde{\theta}_\beta\right) = \frac{1}{2}\left(\tilde{\theta}_\alpha^T k_e^{-1} \tilde{\theta}_\alpha + \tilde{\theta}_\beta^T k_e^{-1} \tilde{\theta}_\beta\right). \tag{23}$$

Time-derivative of (23) leads,

$$\dot{V} = -\tilde{\theta}_\alpha^T k_e^{-1} \dot{\hat{\theta}}_\alpha - \tilde{\theta}_\beta^T k_e^{-1} \dot{\hat{\theta}}_\beta. \tag{24}$$

Let us select the parameter vector update laws as:

$$\dot{\hat{\theta}}_\alpha = k_e \Omega_\alpha \tilde{v}_\alpha^{\emptyset}. \tag{25}$$

$$\dot{\hat{\theta}}_\beta = k_e \Omega_\beta \tilde{v}_\beta^{\emptyset}. \tag{26}$$

By plugging in the update laws (25) and (26) into (24), one can get that:

$$\dot{V} = -\left(\tilde{v}_\alpha^{\emptyset}\right)^2 - \left(\tilde{v}_\beta^{\emptyset}\right) \leq 0.$$

This proves the boundedness of the parameter vector estimation error. Parameter update laws (25) and (26) can be used to extract the amplitude and phase angles. In obtaining the update laws, it is assumed that the information vectors Ω_α and Ω_β are known *a priori*. In practice, the grid frequency is unknown. In this case, an estimate of the grid frequency has to be used. By considering the estimated grid frequency, the unknown parameter estimation laws can be written in the scaler form as:

$$\dot{\hat{\theta}}_{\alpha 1} = k_e \cos\left(\hat{\omega} t\right) \tilde{v}_\alpha^{\emptyset}. \tag{27}$$

$$\dot{\hat{\theta}}_{\alpha 2} = k_e \sin\left(\hat{\omega} t\right) \tilde{v}_\alpha^{\emptyset}. \tag{28}$$

$$\dot{\hat{\theta}}_{\beta 1} = k_e \cos\left(\hat{\omega} t\right) \tilde{v}_\beta^{\emptyset}. \tag{29}$$

$$\dot{\hat{\theta}}_{\beta 2} = k_e \sin\left(\hat{\omega} t\right) \tilde{v}_\beta^{\emptyset}. \tag{30}$$

From the estimated parameters, direct- and quadrature-axis positive- and negative-sequence voltages can be obtained as:

$$v_d^+ = \frac{\hat{\theta}_{\alpha 1} + \hat{\theta}_{\beta 2}}{2}. \tag{31}$$

$$v_q^+ = \frac{\hat{\theta}_{\beta 1} - \hat{\theta}_{\alpha 2}}{2}. \tag{32}$$

$$v_d^- = \frac{\hat{\theta}_{\alpha 1} - \hat{\theta}_{\beta 2}}{2}. \tag{33}$$

$$v_q^- = \frac{-\hat{\theta}_{\alpha 2} - \hat{\theta}_{\beta 1}}{2}. \tag{34}$$

Similar to QT1-PLL, estimated direct and quadrature-axis positive- and negative-sequence voltages will also be passed through MAF to enhance the harmonic robustness. Then, the amplitude and phase-angle of the positive- and negative-sequence voltages can be obtained as:

$$\hat{V}^+ = \sqrt{\left(v_d^+\right)^2 + \left(v_q^+\right)^2}. \tag{35}$$

$$\hat{V}^- = \sqrt{\left(v_d^-\right)^2 + \left(v_q^-\right)^2}. \tag{36}$$

$$\hat{\phi}^+ = \text{atan2}\left(v_q^+, v_d^+\right). \tag{37}$$

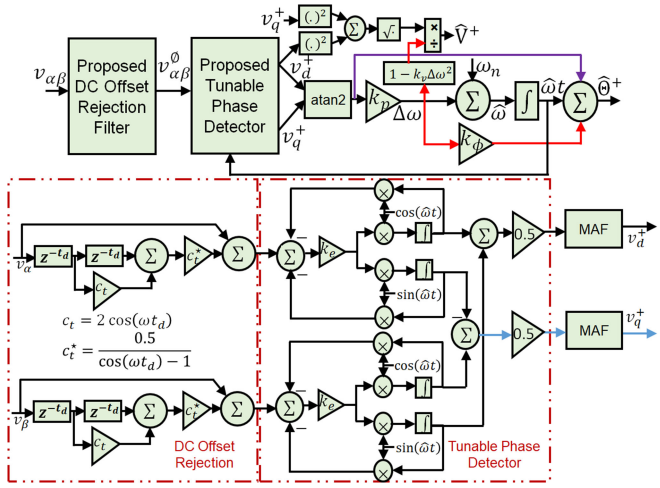


Fig. 2. Block diagram of the proposed enhanced QT1-PLL.

$$\hat{\phi}^- = \text{atan2}\left(v_q^-, v_d^-\right). \tag{38}$$

Using (35)–(38) and the estimated $\hat{\omega t}$, FFPS and FFNS can easily be obtained. Block diagram of the proposed tunable phase detector based enhanced QT1-PLL for the FFPS case is given in Fig. 2.

C. Small-Signal Modeling and Tuning

1) Small-Signal Modeling: The considered parameter estimation technique described by (27)–(30) is nonlinear in nature and not very suitable to find an analytical formula to tune the phase detector gain k_e. To find an explicit gain tuning formula, let us consider the FFPS phase-angle dynamics by using (37):

$$\dot{\hat{\phi}}^+ = \frac{\dot{v}_d^+ v_q^+ - v_d^+ \dot{v}_q^+}{\left(v_d^+\right)^2 + \left(v_q^+\right)^2}. \tag{39}$$

By substituting (27)–(32) into (39), it can be found that:

$$\begin{aligned}\dot{\hat{\phi}}^+ &= \frac{\hat{V}^+ \sin(\hat{\phi}^+)(\dot{\hat{\theta}}_{\alpha 1} + \dot{\hat{\theta}}_{\beta 2}) - V^+ \cos(\hat{\phi}^+)(\dot{\hat{\theta}}_{\beta 1} - \dot{\hat{\theta}}_{\alpha 2})}{2\left(\hat{V}^+\right)^2}, \\ &= \frac{k_e \sin(\hat{\Theta}^+)\tilde{v}_\alpha^{\emptyset} - k_e \cos(\hat{\Theta}^+)\tilde{v}_\beta^{\emptyset}}{2\hat{V}^+}, \\ &= \frac{k_e V^+ \sin(\Theta^+ - \hat{\Theta}^+)}{2\hat{V}^+} \\ &\quad + \frac{k_e\{\hat{V}^- \sin(\hat{\Theta}^+ + \hat{\Theta}^-) - V^- \sin(\Theta^- + \hat{\Theta}^+)\}}{2\hat{V}^+}. \end{aligned} \tag{40}$$

In the quasi-locked condition, $V^+ \approx \hat{V}^+$, $V^- \approx \hat{V}^-$, $\Theta^+ \approx \hat{\Theta}^+$, and $\Theta^- \approx \hat{\Theta}^-$. In this case, $\hat{V}^- \sin(\hat{\Theta}^+ + \hat{\Theta}^-) - V^- \sin(\hat{\Theta}^- + \hat{\Theta}^+) \approx 0$. Moreover, by applying small-angle approximation formula, one can obtain that $\sin(\Theta^+ - \hat{\Theta}^+) \approx (\Theta^+ - \hat{\Theta}^+) \approx \phi^+ - \hat{\phi}^+$. Then, (40) can be simplified as:

$$\dot{\hat{\phi}}^+ \approx \frac{k_e}{2}(\Theta^+ - \hat{\Theta}^+),$$

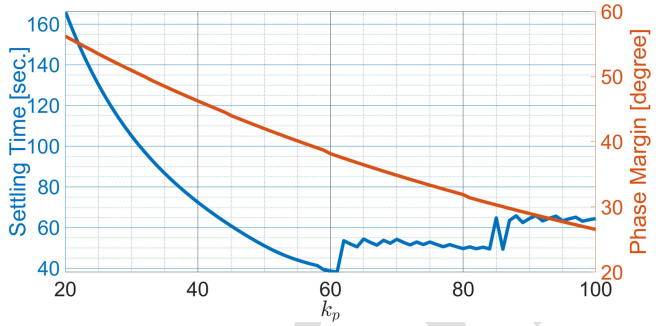


Fig. 3. Gain tuning results for +2 Hz step test.

$$\approx (k_e/2)(\phi^+ - \hat{\phi}^+). \tag{41}$$

From (41), the phase-angle transfer function can be obtained as:

$$G_{PD}(s) = \hat{\phi}^+(s)/\phi^+(s) = 1/\tau_e s + 1, \tag{42}$$

where $\tau_e = 2/k_e$. From the transfer function (42), it is clear that the considered phase detector has a first-order dynamics. As such, the gain k_e can be tuned by using the formula:

$$k_e = 8\tau_s^{-1}, \tag{43}$$

where τ_s is the desired settling time. Using the transfer function (42) and the block diagram of the proposed enhanced QT1-PLL (*cf.* Fig. 2), the small-signal model can be obtained as shown in Fig. 4.

2) Tuning: The proposed technique has three tuning parameters. They are: phase detector gain k_e and the frequency estimator gain k_p. The proposed phase detector can be considered as the observer while the loop-filter can be considered as the controller. In traditional observer-based control system, the observer's convergence speed is typically selected as significantly faster than the controller's convergence speed. Similar idea is considered here also to tune the phase detector gain k_e. To tune this again, we assume a quarter cycle convergence time i.e. $\tau_s = T/4$. With this value of τ_s, the phase detector gain can be found as $k_e = 1600$ from (43).

Finally, to tune the loop-filter parameter k_p, we have considered settling time-based tuning approach similar to [22], [24], [32]. For this purpose, frequency step test of +2 Hz is considered. Then, the settling time (within 2% of the final value) are calculated for different values of k_p. Results of the simulation are given in Fig. 3. The lowest settling time is obtained for $k_p = 61$. As such, this value has been considered. This value corresponds to a phase margin of $\approx 37.8°$ which is within the widely accepted $30° - 60°$ limit.

To validate the developed small-signal model and the tuning procedure, a validation test is performed. In this test, suddenly the grid voltage undergoes a $+15°$ phase-angle step change. Response of the model versus the actual estimator is given in Fig. 5. Result shows that the small-signal model developed in this section is fairly accurate to capture the nonlinear dynamics of the proposed technique.

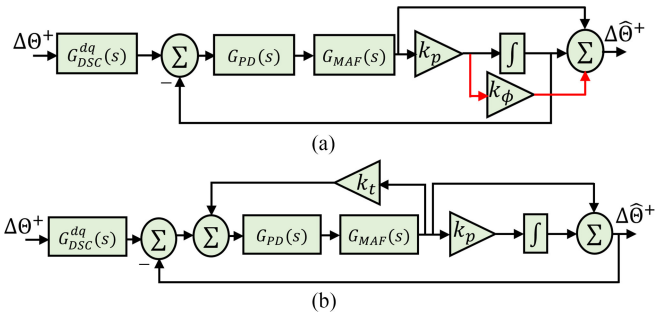


Fig. 4. Small-signal model of the proposed enhanced QT1-PLL: (a) basic model and (b) alternative feedback representation with $k_t = 1 + k_p k_\phi$.

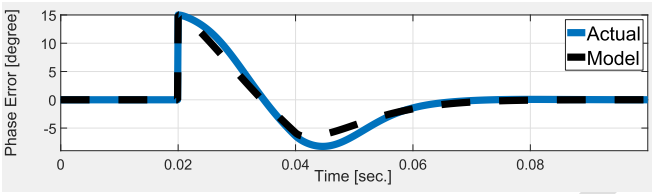


Fig. 5. Small-signal model validation for $+15^\circ$ phase angle step change with $k_e = 1600$, $k_p = 61$, $t_d = 0.005$ and $T_w = 0.01$.

TABLE I
CONTROL PARAMETERS OF THE SELECTED TECHNIQUES.

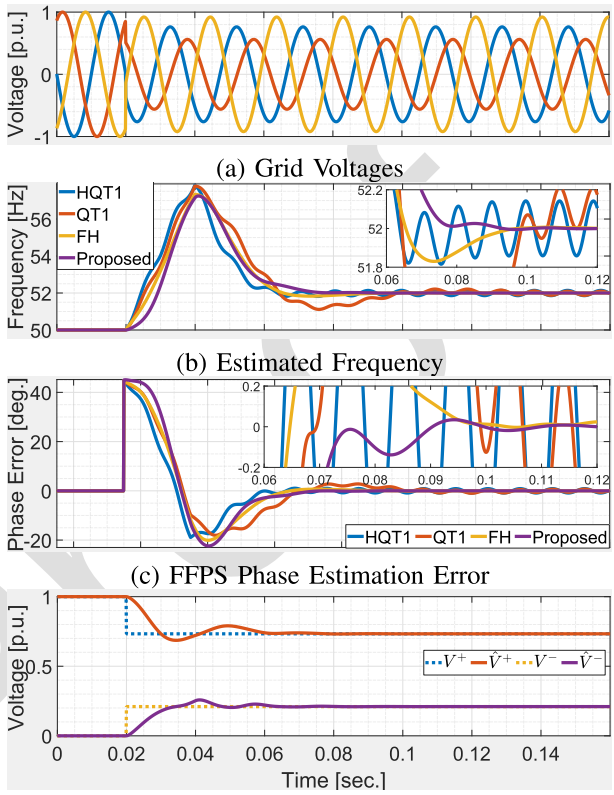
Method	QT1	HQT1	FH	Proposed
k_p	64	81	61	61
MAF Window Length	T	$T/2$	$T/2$	$T/2$
DSC Window Length	–	$T/2$	$T/2$	$T/2$
Phase Margin			$\approx 37.8^\circ$	

IV. RESULTS AND DISCUSSIONS

In this Section, performance of the proposed technique is going to be investigated. Proposed technique is based on the idea of QT1-PLL. As such QT1-PLL [21] and hybrid QT1-PLL (HQT1-PLL) [22], and a recent variant of HQT1-PLL named fast hybrid - PLL (FH-PLL) [32] are considered as comparison techniques. Control parameters are given in Table I. All four techniques are implemented in Matlab/Simulink with a sampling frequency of 10 kHz.

A. Simulation Results

1) Test-I: Balanced to Off-Nominal Frequency Unbalanced Grid: Effectiveness of the comparative techniques under unbalanced fault at off-nominal frequency condition is tested in this test. Pre-fault grid is made of $V^+ = 1\angle 0^\circ$. Post-fault grid is composed of $\overrightarrow{V}^{+1} = 0.733\angle 45^\circ$ [p.u.] and $\overrightarrow{V}^{-1} = 0.211\angle -45^\circ$ [p.u.] at $f = 52$ Hz. Simulation results are given in Fig. 6. Results show that both FH-PLL and the proposed technique have no steady-state oscillation in the steady-state parameters whereas this is not the case for QT1- and HQT1-PLLs. In terms of frequency estimation convergence time, the proposed technique took 55 msec. to converge whereas FH-PLL took 68msec.



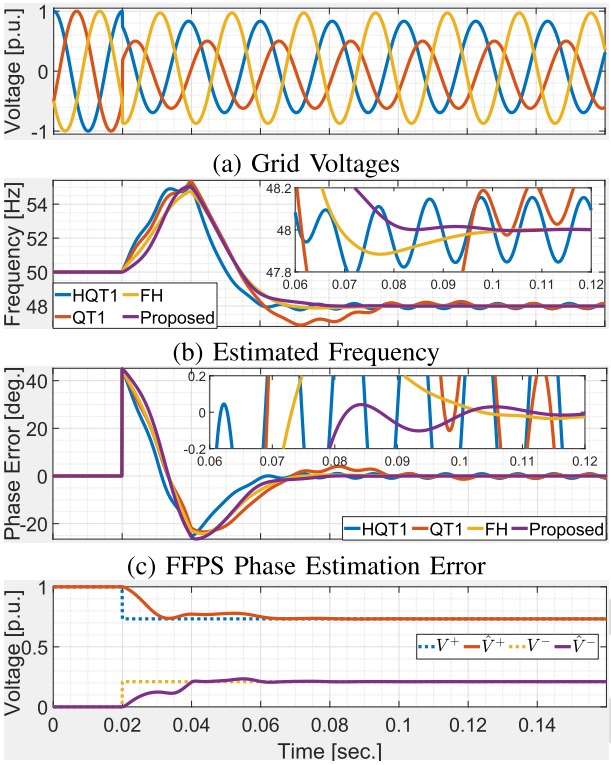
(d) Estimated FFPS and FFNS amplitude by the Proposed Technique

Fig. 6. Test-I: Simulation results.

Similarly, the phase estimation error convergence time of the proposed technique was 6msec. faster compared to FH-PLL.The proposed technique was very rapid to estimate the amplitudes of FFPS and FFNS components as shown in Fig. 6(d). The convergence time is roughly two cycle which shows the effectiveness of the proposed method as a sequence extraction tool.

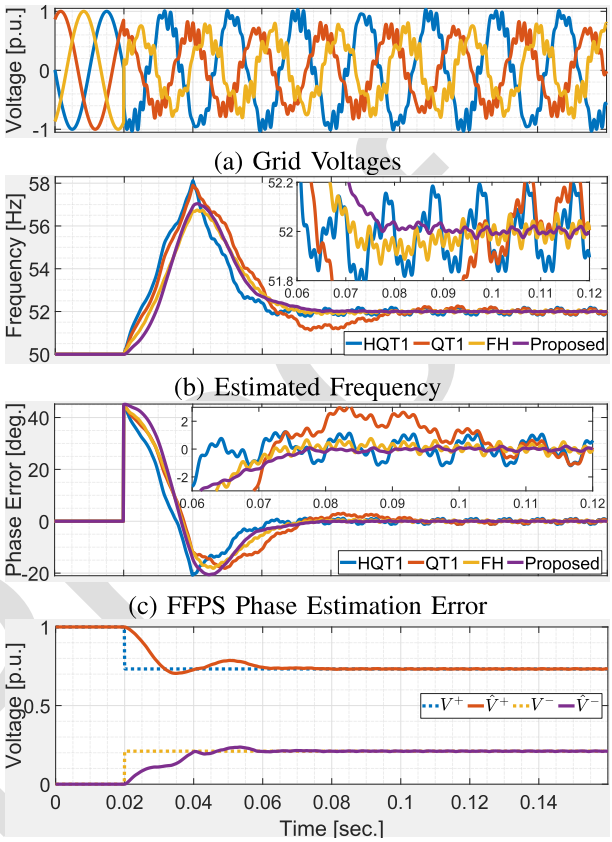
2) Test-II: Balanced to Off-Nominal Frequency Unbalanced and Biased Grid: Here, the post-fault grid is composed of $\overrightarrow{V}^{+1} = 0.733\angle 45^\circ$ [p.u.] and $\overrightarrow{V}^{-1} = 0.211\angle -45^\circ$ [p.u.] at $f = 48$ Hz. Moreover, unequal DC offsets of $0.07, 0.06, 0.05$ p.u. are added in phase a, b, and c, respectively. Simulation results for Test-II are shown in Fig. 7. Similar to Test-I, steady-state values by QT1- and HQT1-PLLs are outside the settling band. In terms of frequency estimation convergence time, the proposed technique took 58msec. to converge whereas FH-PLL took 12msec. more than the proposed technique. Similarly, the phase estimation error convergence time of the proposed technique was 14msec. faster compared to FH-PLL.

3) Test-III: Balanced to Off-Nominal Frequency Unbalanced and Distorted Grid: Here, the post-fault grid is composed of $\overrightarrow{V}^{+1} = 0.733\angle 45^\circ$ [p.u.] and $\overrightarrow{V}^{-1} = 0.211\angle -45^\circ$ [p.u.], $\overrightarrow{V}^{+5} = 0.0625\angle 45^\circ$, $\overrightarrow{V}^{-5} = 0.0625\angle -45^\circ$, $\overrightarrow{V}^{-11} = 0.0625\angle 180^\circ$, $\overrightarrow{V}^{+13} = 0.0625\angle -180^\circ$, and 570 Hz interharmonics of $0.0625\angle 90^\circ$ at $f = 52$ Hz. Simulation results are given in Fig. 8. Results in this test are consistent with the previous two cases. Peak-to-peak oscillation in the estimated frequency



(d) Estimated FFPS and FFNS amplitude by the Proposed Technique

Fig. 7. Test-II: Simulation results.



(d) Estimated FFPS and FFNS amplitude by the Proposed Technique

Fig. 8. Test-III: Simulation results.

by the proposed technique is 6 times higher for QT1-PLL compared to the proposed technique. In case of phase estimation error, the ratio is almost 4 times. Similar performance improvement by the proposed technqiue can also be seen compared to FH-PLL. Total harmonic distortion is also the lowest for the proposed technique. This is due to the fact that the MAFs are used in all the comparative techniques, however, they are tuned at the fundamental frequency. This makes the techniques sensitive to frequency variation. However, the proposed technique is significantly less sensitive to same frequency condition despite having the same fundamental frequency tuned MAFs. This is due to the low-pass filter characteristics of the proposed phase detector. This characteristics also helps to extract the FFPS and FFNS amplitude with extremely low total harmonic distortion (THD) as can be seen in Fig. 8(d). Low THD sequence extraction is very important to satisfy strict grid-integration standards for distributed generation systems.

Comparative time-domain summary of the selected techniques are given in Table II.

B. Experimental Results

The experimental setup, shown in Fig. 9, is used to validate the proposed enhanced QT1-PLL Here, a PWM-controlled three-phase inverter is used to emulate the adverse grid voltage signal. Three GW Instek GDP-100 high voltage differential probe are used to measure the voltages at the load-side. Parameters of the emulator are given in Table III.

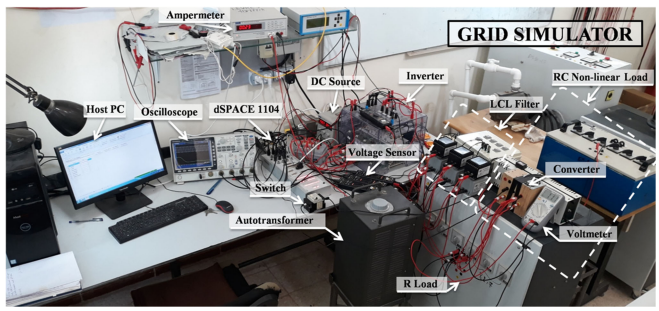
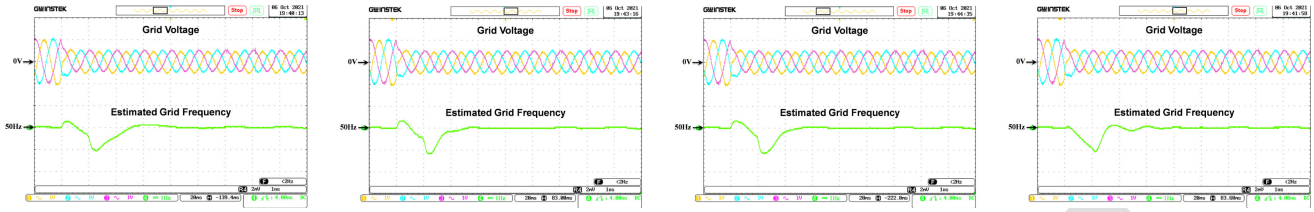


Fig. 9. Test setup.

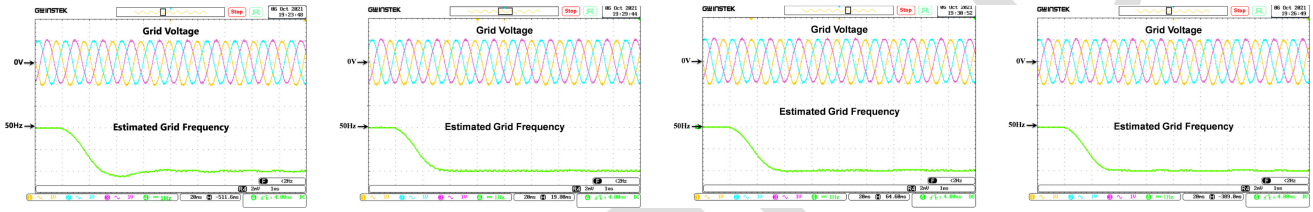
In the first test, a symmetrical voltage sag of 0.5 p.u. is considered. Performances of the comparative techniques are given in Fig. 11. Results show that the proposed technique and QT1-PLL had a peak overshoot of ≈ 1 Hz while it is ≈ 1.15 Hz for HQT1- and FH-PLLs. Frequency estimated by the proposed technique returns back to the nominal value in roughly 2 cycles whereas it is slightly higher for the other techniques.

In the second test, -2 Hz frequency sag is considered. Performance of the comparative techniques are given in Fig. 10. Except QT1-PLL, the other techniques have first-order response. Although the dynamic responses are similar, the proposed technique show less sensitivity to switching and measurement noises



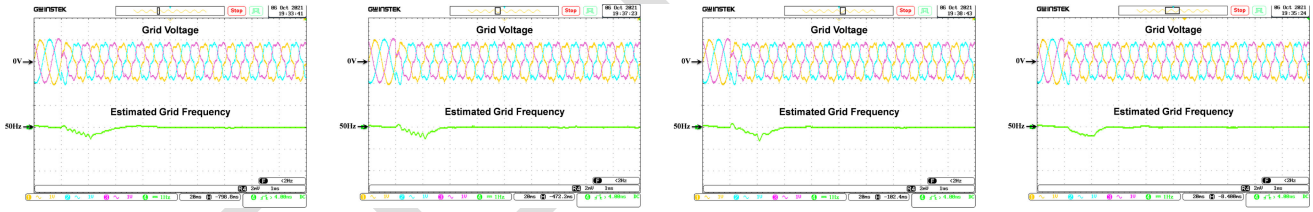
(a) QT1-PLL (b) HQT1-PLL (c) FH-PLL (d) Proposed

Fig. 10. Comparative experimental results for -0.5 p.u. voltage sag.



(a) QT1-PLL (b) HQT1-PLL (c) FH-PLL (d) Proposed

Fig. 11. Comparative experimental results for -2 Hz frequency sag.



(a) QT1-PLL (b) HQT1-PLL (c) FH-PLL (d) Proposed

Fig. 12. Comparative experimental results for distorted grid.

TABLE II
COMPARATIVE SUMMARY OF THE SELECTED TECHNIQUES.

	QT1	HQT1	FH	Proposed
Test-I: Balanced to Unbalanced Grid				
Settl. Time ($\pm$0.04Hz) (msec.)	NA	NA	68	55
Frequency Overshoot	5.78	5.83	5.34	5.25
Settl. Time ($\pm 0.1^\circ$) (msec.)	NA	NA	71	65
Test-II: Balanced to Unbalanced and Biased Grid				
Settl. Time ($\pm$0.04Hz) (msec.)	NA	NA	70	58
Frequency Overshoot (Hz)	7.4	7.15	6.8	7
Settl. Time ($\pm 0.1^\circ$) (msec.)	NWB	NWB	74	60
Test-III: Distorted Grid				
Oscillation (pk-pk) (Hz)	0.27	0.35	0.14	0.04
Oscillation (pk-pk) ($^\circ$)	1.55	2.2	0.96	0.41
THD (%) (Grid - 23.84%)	0.79	1.11	0.37	0.19

NA - Not applicable as the steady-state value is outside of the band

TABLE III
SYSTEM PARAMETERS.

Parameter	Value
DC-Link voltage	$V_{dc} = 310\ V$
Inverter voltage	$110\ V$ (rms)
LCL filter	Inverter and load side $L = 3$ mH, $C = 84\ \mu F$
Inverter rating	20 kVA
Frequency	Sampling and Switching: 10 kHz
Load parameter	$R = 167$ Ohm

compared to the other techniques. As all the techniques are tuned using phase margin, dynamic responses will be similar. However, the presence of low-pass filter-like phase detector makes the proposed technique less sensitive to off-nominal frequency components and/or various noises.

In the final test, suddenly diode rectifier which is a highly nonlinear load is added to generate distorted grid. Performance of the comparative techniques are given in Fig. 12. The proposed technique had a peak overshoot of 0.4 Hz while it is 0.5 Hz, 0.55 Hz and 0.6 Hz for QT1-, HQT1-, and FH-PLL,

respectively. Moreover, the proposed technique's steady-state accuracy is also better than the comparative techniques due to the presence of low-pass filter-like phase detector.

Experimental results in Figs. 10–12 show that the proposed technique has very good dynamic performance and high steady-state accuracy. These results validate the performance of the proposed PLL.

V. Conclusion

This paper proposed an enhanced QT1-PLL that eliminates the limitation of conventional QT1-PLLs. The proposed technique uses a novel enhanced phase detector that can separate the FFPS and FFNS components. This makes the proposed technique insensitive to off-nominal FFNS component. Moreover, a novel DC offset rejection filter is also proposed. A systematic procedure for small-signal modeling and tuning is provided for the proposed PLL. Comparative performance analysis using various challenging test scenarios showed that the proposed technique is very suitable for unbalanced and distorted grid. It has fast convergence speed, high degree of immunity to grid abnormalities and it is easy to tune and implement. Thanks to the FFPS and FFNS extraction capabilities, the proposed PLL is a very suitable candidate to be used as a grid-synchronization tool inside fault-tolerant controller of grid-connected converters.

Acknowledgment

Hafiz Ahmed would like to acknowledge Dr. Denis Efimov and Dr. Rosane Ushirobira from Inria, Lille, France for their helpful comments and discussions on the development of the DC offset rejection filter used in this work.

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Quasi Type-1 PLL With Tunable Phase Detector for Unbalanced and Distorted Three-Phase Grid

Hafiz Ahmed, *Senior Member, IEEE*, Zoheir Tir, *Senior Member, IEEE*, Anant Kumar Verma, *Member, IEEE*, Seifeddine Ben Elghali, and Mohamed Benbouzid, *Fellow, IEEE*

***Abstract*—Out of various moving average filter (MAF)-based phase-locked-loop (PLL), quasi type-1 PLL (QT1-PLL) is widely adopted due to its fast dynamic performance, implementation simplicity, and harmonics rejection abilities. However, the performance of QT1-PLL deteriorates in the presence of an off-nominal frequency unbalanced grid voltage component. Moreover, the sensitivity towards the fundamental frequency negative sequence (FFNS) component is high. Hence, this paper proposes a novel enhanced QT1-PLL solution that is insensitive to unbalance in the grid voltage signal during off-nominal frequency conditions. The proposed adaptive phase detector makes it possible to estimate both the fundamental frequency positive sequence (FFPS) and FFNS components with a high degree of immunity against harmonics. Notably, the pre-loop separation of the FFPS and the FFNS components helps suppress the second harmonic oscillations for improving the parameter estimation accuracy. The loop-filter design of QT1-PLL remains unaffected and requires a proportional gain to estimate the fundamental phase and frequency information. To address the DC offset issue, a modified delayed signal cancellation method is also proposed, which can theoretically eliminate the DC offset for any arbitrary delay length. A small-signal model of the proposed PLL is developed for the sake of stability analysis. Comparative numerical simulation and experimental results are provided with various variants of QT1-PLLs to demonstrate the performance improvement achieved with the proposed technique.**

***Index Terms*—Phase locked-loop, delayed signal cancellation, moving average filter.**

Manuscript received June 15, 2021; revised October 9, 2021; accepted November 20, 2021. The work of H. Ahmed was supported through the Sêr Cymru Programme by Welsh European Funding Office (WEFO) under European Regional Development Fund (ERDF). The experimental part of the present work was supported by the General Directorate of Scientific Research and Technological Development through the Ministry of Higher Education and Scientific Research of Algeria under Grant A01L07UN390120180001. Paper no. TEC-00636-2021.

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TEC.2021.3130492.

Digital Object Identifier 10.1109/TEC.2021.3130492

I. Introduction

THE penetration of grid-interfaced power electronic converters into traditional electric power grid is increasing day-by-day. They are used for various purposes such as grid-integration of distributed energy resources [1]–[5], power quality improvement [6], supplying domestic and industrial loads [7], charging electric vehicles [8], to name a few. These applications require grid-synchronous operation of the converter with the grid. This process is commonly known as grid-synchronization in the literature. Grid-synchronization necessitates the real-time extraction of unknown grid voltage parameters. As a result, a significant research attention has been given to this problem in the last few decades.

Many fast, efficient, and accurate techniques are already reported in the literature. Out of them, phase-locked loop (PLL) [9]–[13] and it's various variants are particularly popular. Traditional synchronous reference frame-PLL (SRF-PLL) uses Park's transformation as the phase detector and uses a proportional-integral low-pass filter to estimate the unknown grid frequency and phase. The SRF-PLL has fast convergence speed and good disturbance rejection capability. However, this PLL is designed for a balanced grid i.e. only the fundamental frequency positive sequence (FFPS) component is present. In practice, especially at the distribution network level, the grid often has a level of phase unbalance, e.g., more than 50% of the 800 low voltage substations in Cardiff, U.K. have serious phase unbalance [14]. So, enhanced filtering capability is essential to ensure efficient operation of PLL under the presence of phase unbalance i.e. both FFPS and fundamental frequency negative sequence (FFNS) components exist simultaneously.

In the presence of phase unbalance, the phase detector of SRF-PLL generates an undesirable double frequency components. To eliminate the undesirable components, several solutions propose the application of additional filtering stage(s) through pre-loop, in-loop and a combination of both. In the case of pre-loop, filters are applied in the stationary reference frame, i.e., $\alpha\beta-$frame where as in-loop filters are applied in the synchronous reference frame, i.e., $dq-$frame. In the case of hybrid filtering, filters are applied at both stationary and synchronous reference frames.

Some popular filters proposed in the literature are: delayed signal cancellation (DSC) [15]–[17], complex coefficient filter (CCF) [18], [19], moving average filter [20]–[24], orthogonal signal generator (OSG) filter such as second-order generalized integrator (SOGI) [25], adaptive notch filter (ANF) [26], to

name a few. In addition to the filter-based SRF-PLLs, multiple reference frame-based SRF-PLLs such as double decoupled SRF-PLL [27] are also popular in the literature.

Delayed signal cancellation (DSC) [15]–[17], [28] is a popular technique to eliminate the FFNS from the measured grid voltages at the point of common coupling. In order to make DSC-PLL immune to harmonics, multiple DSC operators are used in cascade. So, prior information about the grid harmonics is needed.. Moreover, in the case of off-nominal frequency operation, frequency-adaptive DSCs are proposed [29]. This can potentially increase the computational complexity. By using cross-coupling between two CCF, CCF-PLL [18], [19] can extract grid-synchronized FFPS and FFNS components. CCF is very suitable for selective harmonic elimination. However, multiple CCFs are required to eliminate the effect of harmonics which causes additional computational burden.

OSG-PLLs operate in the stationary reference frame, i.e., $\alpha\beta-$frame and uses OSGs to separate the FFPS and FFNS components followed by traditional SRF-PLL. OSGs typically have band-pass (*cf.* SOGI [25]) or notch (*cf.* ANF [26]) characteristics. To enhance the harmonic robustness of OSG-PLLs, multiple parallel OSGs are often recommended in the literature [30]. This can be computationally complex. Moreover, discretization of parallel OSGs is not straightforward, specially for high-order harmonics. Multiple reference frame PLLs use multiple SRFs to separate the FFPS and FFNS components. In the case of DDSRF-PLL, two cross-coupled reference frames operating at opposite instantaneous phases are used. This helps to make the PLL insensitive to FFNS components. However, the presence of harmonics and/or DC-offset deteriorates the performance. This necessitates the application of several reference frames where each operates at the relevant instantaneous phases. This kind of structure is complex and not suitable for low-cost embedded devices-based real-time implementation.

MAF-PLLs [20]–[24] provides an interesting solution to eliminate the effect of harmonics and/or DC offset. Here, MAF is used to eliminate the effect of FFNS component. Depending on the MAF window length, MAF-PLL can be very effective to block all harmonics and DC offset. However, this comes at the cost of slow dynamic response [20]. To enhance the convergence speed of MAF-PLL, quasi type-1-PLL (QT1-PLL) is proposed in [21]. The QT1-PLL uses the idea of frequency-adaptive demodulation [31]. An advantage of this approach is that only a proportional loop-filter can estimate the unknown grid-frequency whereas proportional-integral loop filter is required for conventional MAF-PLL. However, QT1-PLL is sensitive to off-nominal FFNS component. Since, fundamental frequency tuned MAFs are used in QT1-PLL, it cannot completely block the FFNS component if they appear at off-nominal frequency condition. To speed-up the convergence speed of QT1-PLL, hybrid QT1-PLL (HQT1-PLL) [22] is proposed. In this case, DSC operators are applied in the $\alpha\beta-$frame whereas MAF is applied in the $dq-$frame. However, fast dynamic response comes at the cost of sacrificing the high phase margin. Moreover, HQT1-PLL is also sensitive to off-nominal FFNS component. To reduce the effect of off-nominal frequency FFNS component sensitivity of QT1-PLL, total QT1-PLL (TQT1-PLL) is proposed in [24].

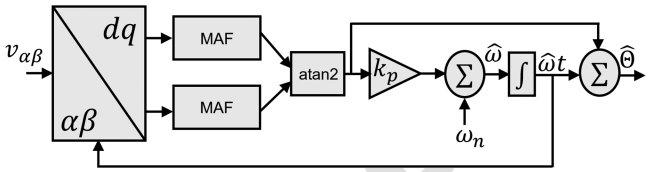


Fig. 1. Overview of QT1-PLL [21].

In this case, a third-order non-adaptive MAF is proposed. This MAF has same window length as QT1-PLL but has significantly lower steady-state errors in the presence of off-nominal FFNS component. However, this comes at the cost of high sensitivity to sub- and inter-harmonics. In [32], the authors have proposed the application of all-pass filter (APF) [33] as the sequence components separator for HQT1-PLL. Although this technique can reduce the sensitivity, however, APF on its own has limited filtering capability. This can be a limiting factor when the grid voltage has inter- and/or sub-harmonics components. Similar line of investigation is considered in [34] where third-order generalized integrator is considered as the pre-loop filter. It is to be noted here that none of the QT1-PLL techniques discussed in this section can extract the FFNS component with high degree of harmonic immunity. This limits their application where sequence extraction is important [35].

Comparative analysis in [23] shows that out of various MAF-PLLs, QT1-PLL is very suitable for grid-connected converters. This motivates the current work of improving the performance of QT1-PLL. Our main objective is to use QT1-PLL for FFPS and FFNS sequence extraction. For this purpose, an enhanced phase detector is constructed in this work. This phase detector can separate the FFPS and FFNS initial phase-angle and amplitudes. Output of the phase detectors are passed through a proportional loop-filter to estimate the unknown frequency and instantaneous phase of the grid voltage. A small-signal model is derived through analytical calculations and constructive gain tuning procedures are developed for the proposed enhanced QT1-PLL. Finally, the performance of the proposed technique is verified through simulation and experiments on a PWM-controlled voltage source inverter. In contrast to the conventional QT1-PLLs, the proposed approach is insensitive to off-nominal FFNS component. Moreover, it can extract FFPS and FFNS components unlike conventional QT1-PLLs. These are the main contributions of this work.

The rest of this paper is organized as follows: Section II summarizes the conventional QT1-PLL. Development of the proposed enhanced QT1-PLL is given in Section III. Results and discussions are given in Section IV. Finally, concluding remarks are given in Section V.

II. Quasi Type-1 PLL: Brief Overview

This section summarizes the basic idea of the conventional QT1-PLL as proposed in [21]. Block diagram of the QT1-PLL is given in Fig. 1. To analyze the phase detector of the QT1-PLL, let us consider the three-phase grid voltages in $\alpha,\beta-$frame as:

$$v_\alpha(t) = V\cos\left(\omega t + \phi\right), \tag{1}$$

$$v_\beta(t) = V \sin(\omega t + \phi), \tag{2}$$

where the amplitude, angular frequency, and the initial phase-angle are given by V, ω, and ϕ, respectively. The instantaneous phase of the signals (1) and (2) is given by $\Theta = \omega t + \phi \in [0, 2\pi)$. The voltages in (1) and (2) are converted into the synchronous reference frame (d, q) by applying the Park-type transformation and given by:

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\hat{\omega}t) & \sin(\hat{\omega}t) \\ -\sin(\hat{\omega}t) & \cos(\hat{\omega}t) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}. \tag{3}$$

From (3), the direct and quadrature-axis voltages can be rewritten as:

$$\begin{aligned} v_d &= v_\alpha \cos(\hat{\omega}t) + v_\beta \sin(\hat{\omega}t), \\ &= \frac{V}{2}\left[\cos\{(\omega - \hat{\omega})t + \phi\} + \cos\{(\omega + \hat{\omega})t + \phi\}\right] \\ &\quad + \frac{V}{2}\left[\cos\{(\omega - \hat{\omega})t + \phi\} - \cos\{(\omega - \hat{\omega})t + \phi\}\right]. \end{aligned} \tag{4}$$

$$\begin{aligned} v_q &= v_\beta \cos(\hat{\omega}t) - v_\alpha \sin(\hat{\omega}t), \\ &= \frac{V}{2}\left[\sin\{(\omega + \hat{\omega})t + \phi\} + \sin\{(\omega - \hat{\omega})t + \phi\}\right] \\ &\quad - \frac{V}{2}\left[\sin\{(\omega + \hat{\omega})t + \phi\} - \sin\{(\omega - \hat{\omega})t + \phi\}\right]. \end{aligned} \tag{5}$$

In the quasi-locked condition i.e. $\hat{\omega} \approx \omega$, it can be assumed that $\omega - \hat{\omega} \approx 0$. Then, (4) and (5) can be simplified as:

$$v_d \approx V \cos(\phi). \tag{6}$$

$$v_q \approx V \sin(\phi). \tag{7}$$

It is to be noted here that only when $\phi = \pm n\pi, n = 0, 1, 2, \ldots$, $v_d \approx V$ and $v_q \approx 0$ which is the same as the output of the phase detector of SRF-PLL [9]. From (6) and (7), the initial phase-angle can be estimated as:

$$\hat{\phi} = \text{atan2}(v_q, v_d), \tag{8}$$

where atan2 is the double quadrant arctangent function. In the above analysis, it is assumed that the grid is balanced and does not contain any harmonics. In practice, the grid is unbalanced, then, the FFNS component will appear as a double the fundamental frequency component in (6) and (7). Similarly, odd-order harmonics in the grid voltage will also appear as even-order harmonics in (6) and (7). These high frequency components will introduce ripple in the estimated phase-angle. Hence, the frequency even-order AC components can be filtered out by using a moving average filter (MAF) of window length, $T_w = T/2$, where T is the period of the fundamental component. The transfer function of the MAF in continuous and discrete-time are given by

$$G_{MAF}(s) = \left(1 - e^{-T_w s}\right)/T_w s. \tag{9}$$

$$G_{MAF}(z) = \frac{1}{N}\frac{1 - z^{-N}}{1 - z^{-1}}, \tag{10}$$

where $N = T/T_s$ with T_s being the sampling period. There are three major issues that affect the performance of the standard QT1-PLL. Firstly, the phase detector part does not use any gain i.e. no design freedom. Secondly, off-nominal frequency negative-sequence component will introduce high frequency ripple in the estimated phase. Finally, it is not capable of extracting the FFNS component. These issues will be addressed in the next section.

III. Enhanced QT1-PLL

In this section, the proposed modifications are detailed. First, the development of the proposed modified delayed signal cancellation (DSC) is detailed. Then, tunbale phase detector is given followed by the small-signal model-based stability analysis and tuning of the proposed PLL. For the remainder of this Section, let us consider the unbalanced grid voltages in the $\alpha\beta-$frame as:

$$v_\alpha = V_\alpha^0 + V^+ \cos\left(\omega t + \phi^+\right) + V^- \cos\left(\omega t + \phi^-\right), \tag{11}$$

$$v_\beta = V_\beta^0 + V^+ \sin\left(\omega t + \phi^+\right) - V^- \sin\left(\omega t + \phi^-\right), \tag{12}$$

where DC offsets are denoted by V_α^0 and V_β^0, the superscript $+$ and $-$ indicate the positive- and negative-sequence component and the remaining variables retain the same meaning as defined in Section II.

A. DC Offset Rejection

To reject DC offset, half-cycle DSC is a popular solution in the literature [22], [24], [28], [32]. In this work, we are considering a modified version of the DSC method for DC offset rejection. For this purpose, let us consider the delayed versions of the signals (11) and (12) as given below:

$$v_l^{nt_d} = v_\alpha(t - nt_d), \tag{13}$$

for $l \in \{\alpha, \beta\}$, $n = 1, 2$ with t_d being the basic time delay. Let us denote the DC offset-free version of the signals (11) and (12) as $v_\alpha^\emptyset$ and $v_\beta^\emptyset$. Then, these signals can be estimated using (11), (12), and (13) as given below:

$$v_l^\emptyset = v_l + \frac{0.5}{\cos(\omega t_d) - 1}\left(v_l - 2\cos(\omega t_d)\, v_l^{t_d} + v_l^{2t_d}\right). \tag{14}$$

Using (14), DC offset-free signals can be estimated using any arbitrary amount of time-delay as opposed to the half-cycle delay requirement of traditional DSC method. To implement (14), real-time information of the grid frequency ω is required. However, real-time frequency adaptation can complicate the modeling and tuning process. As such, frequency-fixed version of (14) is considered similar to [22], [24], [32] where the frequency ω is substituted by its nominal value. However, this will introduce amplitude and phase attenuation in the off-nominal frequency condition. So, compensation of these deviations need to be considered. For this purpose, transfer function of the filter (14) needs to be considered. Then, based on the developed transfer function, quantification of the amplitude and phase attenuation need to be studied. Filter (14) has the same transfer function of convention half-cycle DSC if $t_d = T/4$ is considered. For this value of t_d, the total delay of the proposed DSC filter (14) is the same as the standard DSC, i.e., $T/2$. As such, this value of t_d is selected. For this value, transfer function of (14) in the

phasor-form is given by:

$$G_{DSC}^{\alpha\beta}(s) = \left(1 - e^{-2t_d s}\right)/2. \tag{15}$$

Let us consider that $\omega = \omega_n + \Delta\omega$, where ω_n is the nominal value and $\Delta\omega$ is the deviation. Then, the amplitude and phase of transfer function (15) can be found as [36]:

$$\left|G_{DSC}^{\alpha\beta}(s)\right| \approx 1 - k_v \left(\Delta\omega\right)^2, \tag{16}$$

$$\angle G_{DSC}^{\alpha\beta}(s) = -k_\phi \Delta\omega, \tag{17}$$

where $k_v = T^2/32$ and $k_\phi = T/4$. From (16) and (17), it is clear that in the off-nominal frequency case, amplitude and phase attenuation are characterized by k_v and k_ϕ. As such, compensation of these pre-loop filter induced attenuation need to be considered in the in-loop of the PLL. It is to pointed out here that as a particular case of (14), convention half-cycle DSC filter can be be obtained. However, unlike conventional DSC, (14) can eliminates DC offset for any value of t_d. Moreover, despite the transfer functions being equal for $t_d = T/4$, the dynamic response is not the same for our DSC and the conventional counterpart.

Transfer function (15) in the dq-frame is given by:

$$G_{DSC}^{dq}(s) = \left(1 + e^{-2t_d s}\right)/2. \tag{18}$$

Transfer function (18) will be used for small-signal modeling purpose later in Section III-C.

B. Tunable Phase Detector

To develop the phase detector with tunable gain, let us consider the offset-free signal in (11) and (12), i.e., $v_\alpha^{\emptyset}$ and $v_\beta^{\emptyset}$. By applying basic trigonometric identities, expressions of $v_\alpha^{\emptyset}$ and $v_\beta^{\emptyset}$ can be expanded and rewritten into the parametric form as [37], [38]:

$$v_\alpha^{\emptyset} = \Omega_\alpha^T \theta_\alpha, \tag{19}$$

$$v_\beta^{\emptyset} = \Omega_\beta^T \theta_\beta, \tag{20}$$

where

$$\Omega_\alpha = \Omega_\beta = \begin{bmatrix}\cos(\omega t) & \sin(\omega t)\end{bmatrix}^T,$$

$$\theta_\alpha = \begin{bmatrix}\theta_{\alpha 1} \\ \theta_{\alpha 2}\end{bmatrix} = \begin{bmatrix} V^+\cos(\phi^+) + V^-\cos(\phi^-) \\ -V^+\sin(\phi^+) - V^-\sin(\phi^-)\end{bmatrix},$$

$$\theta_\beta = \begin{bmatrix}\theta_{\beta 1} \\ \theta_{\beta 2}\end{bmatrix} = \begin{bmatrix} V^+\sin(\phi^+) - V^-\sin(\phi^-) \\ V^+\cos(\phi^+) - V^-\cos(\phi^-)\end{bmatrix},$$

with the unknown parameter vectors being denoted by θ_α, θ_β while Ω_α and Ω_β denote the known information vector. To estimate the unknown parameter vectors θ_α and θ_β from the measured voltages v_α and v_β, let us consider the estimated voltages as $\hat{v}_\alpha^{\emptyset} = \Omega_\alpha^T \hat{\theta}_\alpha$and $\hat{v}_\beta^{\emptyset} = \Omega_\beta^T \hat{\theta}_\beta$. Let us define the parameter vector estimation error as $\tilde{\theta}_\alpha = \theta_\alpha - \hat{\theta}_\alpha$ and $\tilde{\theta}_\beta = \theta_\beta - \hat{\theta}_\beta$. Then, the output estimation error can be written as:

$$\tilde{v}_\alpha^{\emptyset} = v_\alpha^{\emptyset} - \hat{v}_\alpha^{\emptyset} = \Omega_\alpha^T \tilde{\theta}_\alpha. \tag{21}$$

$$\tilde{v}_\beta^{\emptyset} = v_\beta^{\emptyset} - \hat{v}_\beta^{\emptyset} = \Omega_\beta^T \tilde{\theta}_\beta. \tag{22}$$

Let us consider the following Lyapunov-like function with $k_e > 0$:

$$V\left(\tilde{\theta}_\alpha, \tilde{\theta}_\beta\right) = \frac{1}{2}\left(\tilde{\theta}_\alpha^T k_e^{-1} \tilde{\theta}_\alpha + \tilde{\theta}_\beta^T k_e^{-1} \tilde{\theta}_\beta\right). \tag{23}$$

Time-derivative of (23) leads,

$$\dot{V} = -\tilde{\theta}_\alpha^T k_e^{-1} \dot{\hat{\theta}}_\alpha - \tilde{\theta}_\beta^T k_e^{-1} \dot{\hat{\theta}}_\beta. \tag{24}$$

Let us select the parameter vector update laws as:

$$\dot{\hat{\theta}}_\alpha = k_e \Omega_\alpha \tilde{v}_\alpha^{\emptyset}. \tag{25}$$

$$\dot{\hat{\theta}}_\beta = k_e \Omega_\beta \tilde{v}_\beta^{\emptyset}. \tag{26}$$

By plugging in the update laws (25) and (26) into (24), one can get that:

$$\dot{V} = -\left(\tilde{v}_\alpha^{\emptyset}\right)^2 - \left(\tilde{v}_\beta^{\emptyset}\right) \leq 0.$$

This proves the boundedness of the parameter vector estimation error. Parameter update laws (25) and (26) can be used to extract the amplitude and phase angles. In obtaining the update laws, it is assumed that the information vectors Ω_α and Ω_β are known *a priori*. In practice, the grid frequency is unknown. In this case, an estimate of the grid frequency has to be used. By considering the estimated grid frequency, the unknown parameter estimation laws can be written in the scaler form as:

$$\dot{\hat{\theta}}_{\alpha 1} = k_e \cos(\hat{\omega} t)\, \tilde{v}_\alpha^{\emptyset}. \tag{27}$$

$$\dot{\hat{\theta}}_{\alpha 2} = k_e \sin(\hat{\omega} t)\, \tilde{v}_\alpha^{\emptyset}. \tag{28}$$

$$\dot{\hat{\theta}}_{\beta 1} = k_e \cos(\hat{\omega} t)\, \tilde{v}_\beta^{\emptyset}. \tag{29}$$

$$\dot{\hat{\theta}}_{\beta 2} = k_e \sin(\hat{\omega} t)\, \tilde{v}_\beta^{\emptyset}. \tag{30}$$

From the estimated parameters, direct- and quadrature-axis positive- and negative-sequence voltages can be obtained as:

$$v_d^+ = \frac{\hat{\theta}_{\alpha 1} + \hat{\theta}_{\beta 2}}{2}. \tag{31}$$

$$v_q^+ = \frac{\hat{\theta}_{\beta 1} - \hat{\theta}_{\alpha 2}}{2}. \tag{32}$$

$$v_d^- = \frac{\hat{\theta}_{\alpha 1} - \hat{\theta}_{\beta 2}}{2}. \tag{33}$$

$$v_q^- = \frac{-\hat{\theta}_{\alpha 2} - \hat{\theta}_{\beta 1}}{2}. \tag{34}$$

Similar to QT1-PLL, estimated direct and quadrature-axis positive- and negative-sequence voltages will also be passed through MAF to enhance the harmonic robustness. Then, the amplitude and phase-angle of the positive- and negative-sequence voltages can be obtained as:

$$\hat{V}^+ = \sqrt{\left(v_d^+\right)^2 + \left(v_q^+\right)^2}. \tag{35}$$

$$\hat{V}^- = \sqrt{\left(v_d^-\right)^2 + \left(v_q^-\right)^2}. \tag{36}$$

$$\hat{\phi}^+ = \text{atan2}\left(v_q^+, v_d^+\right). \tag{37}$$

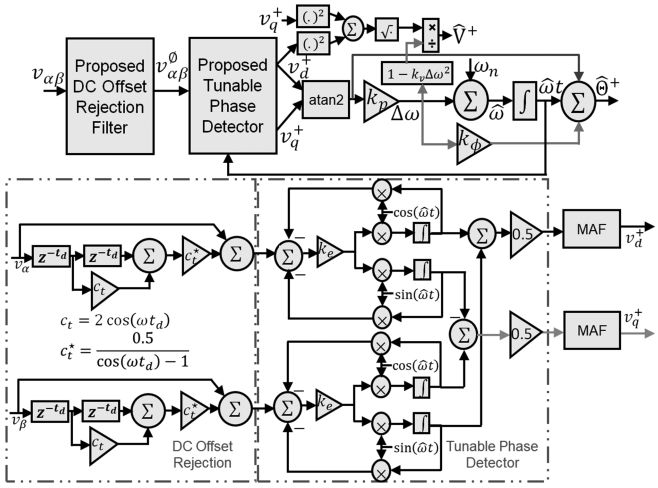


Fig. 2. Block diagram of the proposed enhanced QT1-PLL.

$$\hat{\phi}^- = \text{atan2}\left(v_q^-, v_d^-\right). \tag{38}$$

Using (35)–(38) and the estimated $\hat{\omega t}$, FFPS and FFNS can easily be obtained. Block diagram of the proposed tunable phase detector based enhanced QT1-PLL for the FFPS case is given in Fig. 2.

C. Small-Signal Modeling and Tuning

1) Small-Signal Modeling: The considered parameter estimation technique described by (27)–(30) is nonlinear in nature and not very suitable to find an analytical formula to tune the phase detector gain k_e. To find an explicit gain tuning formula, let us consider the FFPS phase-angle dynamics by using (37):

$$\dot{\hat{\phi}}^+ = \frac{\dot{v}_d^+ v_q^+ - v_d^+ \dot{v}_q^+}{\left(v_d^+\right)^2 + \left(v_q^+\right)^2}. \tag{39}$$

By substituting (27)–(32) into (39), it can be found that:

$$\begin{aligned}\dot{\hat{\phi}}^+ &= \frac{\hat{V}^+ \sin(\hat{\phi}^+)(\dot{\hat{\theta}}_{\alpha 1} + \dot{\hat{\theta}}_{\beta 2}) - V^+ \cos(\hat{\phi}^+)(\dot{\hat{\theta}}_{\beta 1} - \dot{\hat{\theta}}_{\alpha 2})}{2\left(\hat{V}^+\right)^2}, \\ &= \frac{k_e \sin(\hat{\Theta}^+)\tilde{v}_\alpha^{\emptyset} - k_e \cos(\hat{\Theta}^+)\tilde{v}_\beta^{\emptyset}}{2\hat{V}^+}, \\ &= \frac{k_e V^+ \sin(\Theta^+ - \hat{\Theta}^+)}{2\hat{V}^+} \\ &\quad + \frac{k_e\{\hat{V}^- \sin(\hat{\Theta}^+ + \hat{\Theta}^-) - V^- \sin(\Theta^- + \hat{\Theta}^+)\}}{2\hat{V}^+}. \end{aligned} \tag{40}$$

In the quasi-locked condition, $V^+ \approx \hat{V}^+$, $V^- \approx \hat{V}^-$, $\Theta^+ \approx \hat{\Theta}^+$, and $\Theta^- \approx \hat{\Theta}^-$. In this case, $\hat{V}^- \sin(\hat{\Theta}^+ + \hat{\Theta}^-) - V^- \sin(\hat{\Theta}^- + \hat{\Theta}^+) \approx 0$. Moreover, by applying small-angle approximation formula, one can obtain that $\sin(\Theta^+ - \hat{\Theta}^+) \approx (\Theta^+ - \hat{\Theta}^+) \approx \phi^+ - \hat{\phi}^+$. Then, (40) can be simplified as:

$$\dot{\hat{\phi}}^+ \approx \frac{k_e}{2}(\Theta^+ - \hat{\Theta}^+),$$

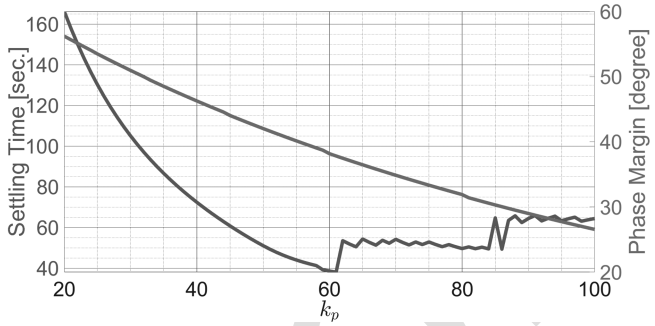


Fig. 3. Gain tuning results for $+2$ Hz step test.

$$\approx (k_e/2)(\phi^+ - \hat{\phi}^+). \tag{41}$$

From (41), the phase-angle transfer function can be obtained as:

$$G_{PD}(s) = \hat{\phi}^+(s)/\phi^+(s) = 1/\tau_e s + 1, \tag{42}$$

where $\tau_e = 2/k_e$. From the transfer function (42), it is clear that the considered phase detector has a first-order dynamics. As such, the gain k_e can be tuned by using the formula:

$$k_e = 8\tau_s^{-1}, \tag{43}$$

where τ_s is the desired settling time. Using the transfer function (42) and the block diagram of the proposed enhanced QT1-PLL (*cf.* Fig. 2), the small-signal model can be obtained as shown in Fig. 4.

2) Tuning: The proposed technique has three tuning parameters. They are: phase detector gain k_e and the frequency estimator gain k_p. The proposed phase detector can be considered as the observer while the loop-filter can be considered as the controller. In traditional observer-based control system, the observer's convergence speed is typically selected as significantly faster than the controller's convergence speed. Similar idea is considered here also to tune the phase detector gain k_e. To tune this again, we assume a quarter cycle convergence time i.e. $\tau_s = T/4$. With this value of τ_s, the phase detector gain can be found as $k_e = 1600$ from (43).

Finally, to tune the loop-filter parameter k_p, we have considered settling time-based tuning approach similar to [22], [24], [32]. For this purpose, frequency step test of $+2$ Hz is considered. Then, the settling time (within 2% of the final value) are calculated for different values of k_p. Results of the simulation are given in Fig. 3. The lowest settling time is obtained for $k_p = 61$. As such, this value has been considered. This value corresponds to a phase margin of $\approx 37.8^\circ$ which is within the widely accepted $30^\circ - 60^\circ$ limit.

To validate the developed small-signal model and the tuning procedure, a validation test is performed. In this test, suddenly the grid voltage undergoes a $+15^\circ$ phase-angle step change. Response of the model versus the actual estimator is given in Fig. 5. Result shows that the small-signal model developed in this section is fairly accurate to capture the nonlinear dynamics of the proposed technique.

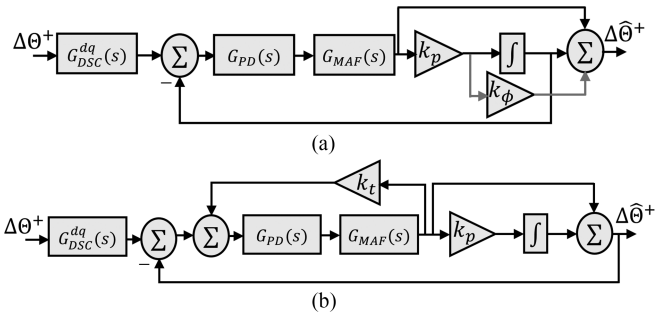


Fig. 4. Small-signal model of the proposed enhanced QT1-PLL: (a) basic model and (b) alternative feedback representation with $k_t = 1 + k_p k_\phi$.

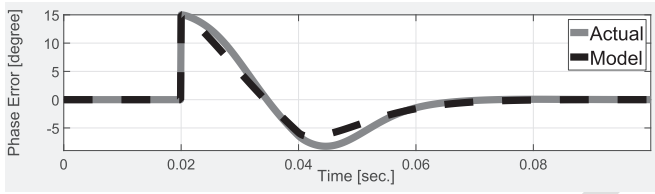


Fig. 5. Small-signal model validation for $+15^\circ$ phase angle step change with $k_e = 1600$, $k_p = 61$, $t_d = 0.005$ and $T_w = 0.01$.

TABLE I
CONTROL PARAMETERS OF THE SELECTED TECHNIQUES.

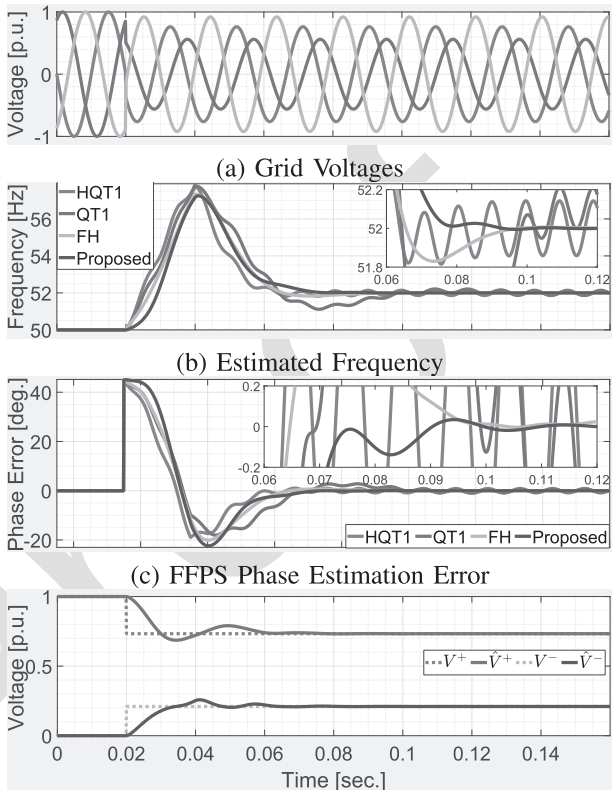
Method	QT1	HQT1	FH	Proposed
k_p	64	81	61	61
MAF Window Length	T	$T/2$	$T/2$	$T/2$
DSC Window Length	–	$T/2$	$T/2$	$T/2$
Phase Margin		$\approx 37.8^\circ$		

IV. RESULTS AND DISCUSSIONS

In this Section, performance of the proposed technique is going to be investigated. Proposed technique is based on the idea of QT1-PLL. As such QT1-PLL [21] and hybrid QT1-PLL (HQT1-PLL) [22], and a recent variant of HQT1-PLL named fast hybrid - PLL (FH-PLL) [32] are considered as comparison techniques. Control parameters are given in Table I. All four techniques are implemented in Matlab/Simulink with a sampling frequency of 10 kHz.

A. Simulation Results

1) Test-I: Balanced to Off-Nominal Frequency Unbalanced Grid: Effectiveness of the comparative techniques under unbalanced fault at off-nominal frequency condition is tested in this test. Pre-fault grid is made of $V^+ = 1\angle 0^\circ$. Post-fault grid is composed of $\overrightarrow{V}^{+1} = 0.733\angle 45^\circ$ [p.u.] and $\overrightarrow{V}^{-1} = 0.211\angle -45^\circ$ [p.u.] at $f = 52$ Hz. Simulation results are given in Fig. 6. Results show that both FH-PLL and the proposed technique have no steady-state oscillation in the steady-state parameters whereas this is not the case for QT1- and HQT1-PLLs. In terms of frequency estimation convergence time, the proposed technique took 55 msec. to converge whereas FH-PLL took 68msec.



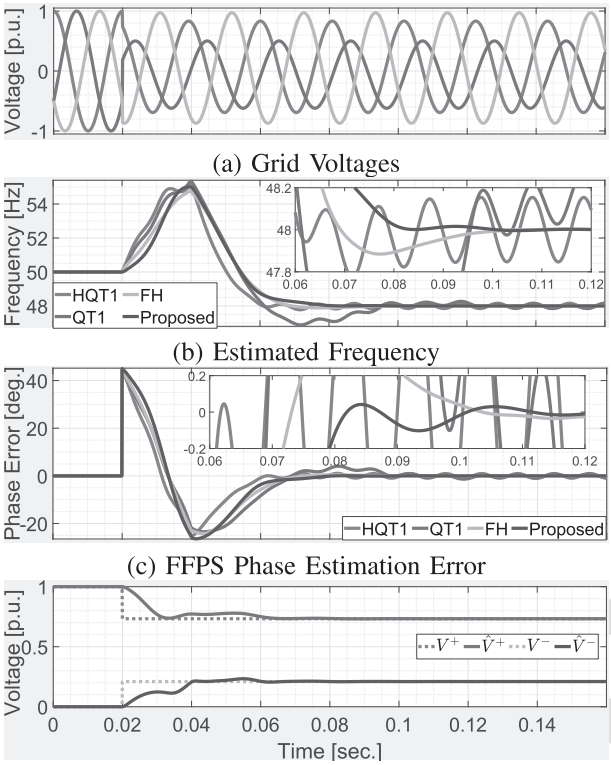
(d) Estimated FFPS and FFNS amplitude by the Proposed Technique

Fig. 6. Test-I: Simulation results.

Similarly, the phase estimation error convergence time of the proposed technique was 6msec. faster compared to FH-PLL.The proposed technique was very rapid to estimate the amplitudes of FFPS and FFNS components as shown in Fig. 6(d). The convergence time is roughly two cycle which shows the effectiveness of the proposed method as a sequence extraction tool.

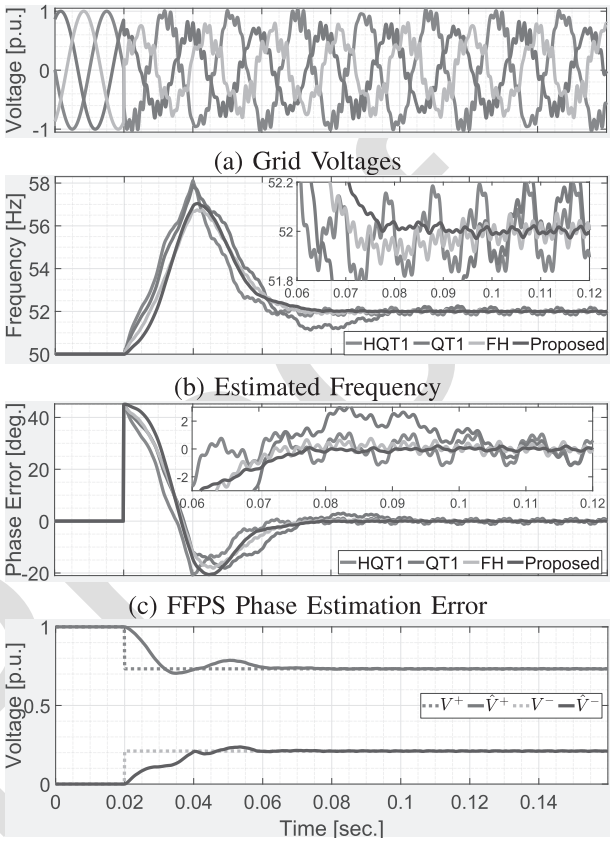
2) Test-II: Balanced to Off-Nominal Frequency Unbalanced and Biased Grid: Here, the post-fault grid is composed of $\overrightarrow{V}^{+1} = 0.733\angle 45^\circ$ [p.u.] and $\overrightarrow{V}^{-1} = 0.211\angle -45^\circ$ [p.u.] at $f = 48$ Hz. Moreover, unequal DC offsets of $0.07, 0.06, 0.05$ p.u. are added in phase a, b, and c, respectively. Simulation results for Test-II are shown in Fig. 7. Similar to Test-I, steady-state values by QT1- and HQT1-PLLs are outside the settling band. In terms of frequency estimation convergence time, the proposed technique took 58msec. to converge whereas FH-PLL took 12msec. more than the proposed technique. Similarly, the phase estimation error convergence time of the proposed technique was 14msec. faster compared to FH-PLL.

3) Test-III: Balanced to Off-Nominal Frequency Unbalanced and Distorted Grid: Here, the post-fault grid is composed of $\overrightarrow{V}^{+1} = 0.733\angle 45^\circ$ [p.u.] and $\overrightarrow{V}^{-1} = 0.211\angle -45^\circ$ [p.u.], $\overrightarrow{V}^{+5} = 0.0625\angle 45^\circ$, $\overrightarrow{V}^{-5} = 0.0625\angle -45^\circ$, $\overrightarrow{V}^{-11} = 0.0625\angle 180^\circ$, $\overrightarrow{V}^{+13} = 0.0625\angle -180^\circ$, and 570 Hz interharmonics of $0.0625\angle 90^\circ$ at $f = 52$ Hz. Simulation results are given in Fig. 8. Results in this test are consistent with the previous two cases. Peak-to-peak oscillation in the estimated frequency



(d) Estimated FFPS and FFNS amplitude by the Proposed Technique

Fig. 7. Test-II: Simulation results.



(d) Estimated FFPS and FFNS amplitude by the Proposed Technique

Fig. 8. Test-III: Simulation results.

by the proposed technique is 6 times higher for QT1-PLL compared to the proposed technique. In case of phase estimation error, the ratio is almost 4 times. Similar performance improvement by the proposed technqiue can also be seen compared to FH-PLL. Total harmonic distortion is also the lowest for the proposed technique. This is due to the fact that the MAFs are used in all the comparative techniques, however, they are tuned at the fundamental frequency. This makes the techniques sensitive to frequency variation. However, the proposed technique is significantly less sensitive to same frequency condition despite having the same fundamental frequency tuned MAFs. This is due to the low-pass filter characteristics of the proposed phase detector. This characteristics also helps to extract the FFPS and FFNS amplitude with extremely low total harmonic distortion (THD) as can be seen in Fig. 8(d). Low THD sequence extraction is very important to satisfy strict grid-integration standards for distributed generation systems.

Comparative time-domain summary of the selected techniques are given in Table II.

B. Experimental Results

The experimental setup, shown in Fig. 9, is used to validate the proposed enhanced QT1-PLL Here, a PWM-controlled three-phase inverter is used to emulate the adverse grid voltage signal. Three GW Instek GDP-100 high voltage differential probe are used to measure the voltages at the load-side. Parameters of the emulator are given in Table III.

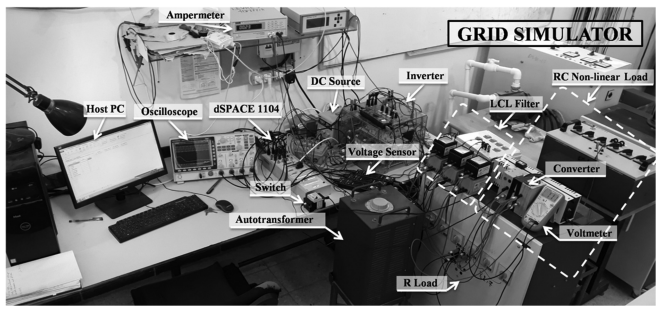
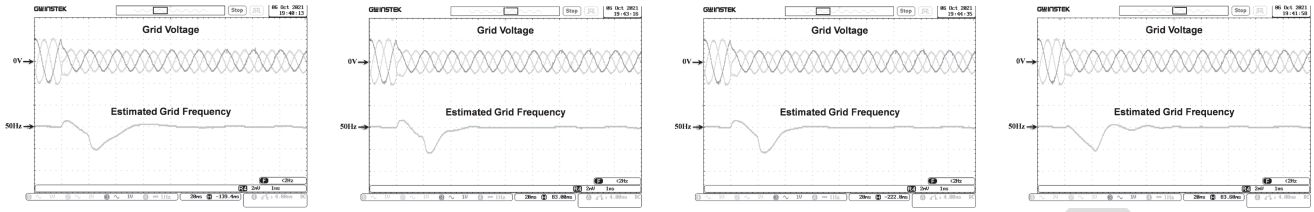


Fig. 9. Test setup.

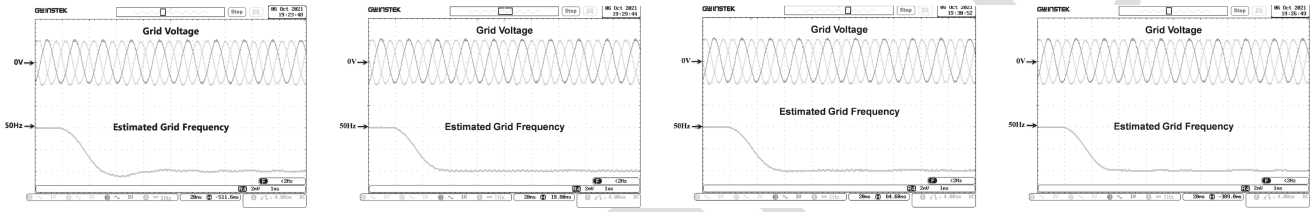
In the first test, a symmetrical voltage sag of 0.5 p.u. is considered. Performances of the comparative techniques are given in Fig. 11. Results show that the proposed technique and QT1-PLL had a peak overshoot of ≈ 1 Hz while it is ≈ 1.15 Hz for HQT1- and FH-PLLs. Frequency estimated by the proposed technique returns back to the nominal value in roughly 2 cycles whereas it is slightly higher for the other techniques.

In the second test, -2 Hz frequency sag is considered. Performance of the comparative techniques are given in Fig. 10. Except QT1-PLL, the other techniques have first-order response. Although the dynamic responses are similar, the proposed technique show less sensitivity to switching and measurement noises



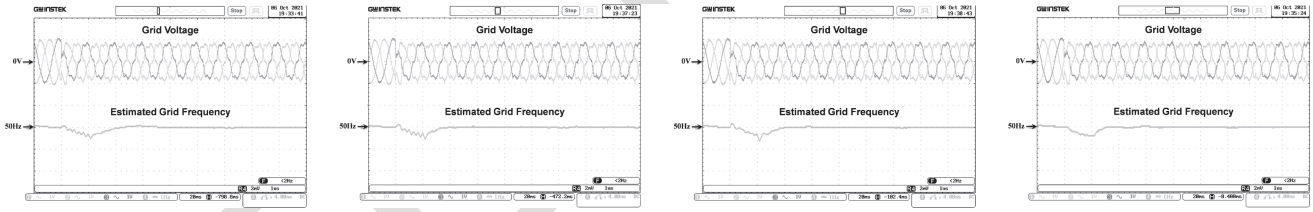
(a) QT1-PLL (b) HQT1-PLL (c) FH-PLL (d) Proposed

Fig. 10. Comparative experimental results for -0.5 p.u. voltage sag.



(a) QT1-PLL (b) HQT1-PLL (c) FH-PLL (d) Proposed

Fig. 11. Comparative experimental results for -2 Hz frequency sag.



(a) QT1-PLL (b) HQT1-PLL (c) FH-PLL (d) Proposed

Fig. 12. Comparative experimental results for distorted grid.

TABLE II
COMPARATIVE SUMMARY OF THE SELECTED TECHNIQUES.

	QT1	HQT1	FH	Proposed
Test-I: Balanced to Unbalanced Grid				
Settl. Time ($\pm$0.04Hz) (msec.)	NA	NA	68	55
Frequency Overshoot	5.78	5.83	5.34	5.25
Settl. Time ($\pm 0.1^\circ$) (msec.)	NA	NA	71	65
Test-II: Balanced to Unbalanced and Biased Grid				
Settl. Time ($\pm$0.04Hz) (msec.)	NA	NA	70	58
Frequency Overshoot (Hz)	7.4	7.15	6.8	7
Settl. Time ($\pm 0.1^\circ$) (msec.)	NWB	NWB	74	60
Test-III: Distorted Grid				
Oscillation (pk-pk) (Hz)	0.27	0.35	0.14	0.04
Oscillation (pk-pk) ($^\circ$)	1.55	2.2	0.96	0.41
THD (%) (Grid - 23.84%)	0.79	1.11	0.37	0.19

NA - Not applicable as the steady-state value is outside of the band

TABLE III
SYSTEM PARAMETERS.

Parameter	Value
DC-Link voltage	$V_{dc} = 310\ V$
Inverter voltage	$110\ V$ (rms)
LCL filter	Inverter and load side $L = 3$ mH, $C = 84\ \mu F$
Inverter rating	20 kVA
Frequency	Sampling and Switching: 10 kHz
Load parameter	$R = 167$ Ohm

compared to the other techniques. As all the techniques are tuned using phase margin, dynamic responses will be similar. However, the presence of low-pass filter-like phase detector makes the proposed technique less sensitive to off-nominal frequency components and/or various noises.

In the final test, suddenly diode rectifier which is a highly nonlinear load is added to generate distorted grid. Performance of the comparative techniques are given in Fig. 12. The proposed technique had a peak overshoot of 0.4 Hz while it is 0.5 Hz, 0.55 Hz and 0.6 Hz for QT1-, HQT1-, and FH-PLL,

respectively. Moreover, the proposed technique's steady-state accuracy is also better than the comparative techniques due to the presence of low-pass filter-like phase detector.

Experimental results in Figs. 10–12 show that the proposed technique has very good dynamic performance and high steady-state accuracy. These results validate the performance of the proposed PLL.

V. Conclusion

This paper proposed an enhanced QT1-PLL that eliminates the limitation of conventional QT1-PLLs. The proposed technique uses a novel enhanced phase detector that can separate the FFPS and FFNS components. This makes the proposed technique insensitive to off-nominal FFNS component. Moreover, a novel DC offset rejection filter is also proposed. A systematic procedure for small-signal modeling and tuning is provided for the proposed PLL. Comparative performance analysis using various challenging test scenarios showed that the proposed technique is very suitable for unbalanced and distorted grid. It has fast convergence speed, high degree of immunity to grid abnormalities and it is easy to tune and implement. Thanks to the FFPS and FFNS extraction capabilities, the proposed PLL is a very suitable candidate to be used as a grid-synchronization tool inside fault-tolerant controller of grid-connected converters.

Acknowledgment

Hafiz Ahmed would like to acknowledge Dr. Denis Efimov and Dr. Rosane Ushirobira from Inria, Lille, France for their helpful comments and discussions on the development of the DC offset rejection filter used in this work.

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