Role of ALD Al_2O_3 surface passivation on the performance of p-type Cu_2O thin film transistors

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Abstract

High-performance p-type oxide thin film transistors (TFTs) have great potential for many semiconductor applications. However, these devices typically suffer from low

hole mobility and high off-state currents. We fabricated p-type TFTs with a phase-pure polycrystalline Cu_2O semiconductor channel grown by atomic layer deposition (ALD). The TFT switching characteristics were improved by applying a thin ALD Al_2O_3 passivation layer on the Cu_2O channel, followed by vacuum annealing at 300 °C. Detailed characterisation by TEM-EDX and XPS shows that the surface of Cu_2O is reduced following Al_2O_3 deposition and indicates the formation of 1–2 nm thick $CuAlO_2$ interfacial layer. This, together with field-effect passivation caused by the high negative fixed charge of the ALD Al_2O_3, leads to an improvement in the TFT performance by reducing the density of deep trap states as well as by reducing the accumulation of electrons in the semiconducting layer in the device off-state.

Keywords: Thin film transistors, oxide thin films, passivation, copper oxide, atomic layer deposition

Introduction

Metal-oxide thin film transistors (TFTs) have attracted increasing interest especially in display technologies owing to their optical transparency and high mobility, low processing temperatures and material costs, and mechanical flexibility.[1] This has led to the development of high-performance n-type semiconducting oxide materials, such as amorphous indium-gallium-zinc-oxide (IGZO) with electron mobility of several tens of $cm^2V^{-1}s^{-1}$.[2] However, the full utilisation of oxides in p-n junction based electronics and complementary metal oxide semiconductor (CMOS) integrated circuits, is still hindered by the lack of high performance p-type oxides. The reason for the challenges in achieving feasible hole conductivity are the differences in the electronic structures of the n- and p-type oxides.[3] The transport path of holes in p-type oxides, valence band maximum (VBM) consists typically of localised anisotropic oxygen 2p orbitals, which results in large hole effective mass and low mobility. In addition, the concentration of holes in oxides is often limited by the high formation energy of the cation vacancies, as well as the annihilation of holes due to the low formation

energy of the oxygen vacancies.[3] In case of cuprous oxide Cu_2O, however, the valence band is formed by the hybridisation of the O 2p and Cu 3d orbitals, resulting in a less localized VBM and pathway for hole transportation for holes formed via copper vacancies (V_{Cu}) as acceptor states.[4] Such special configuration and high hole mobility have made Cu_2O an extensively studied p-type oxide for TFTs,[5] and due to to its other advantageous properties, such as material abundance and solar absorbance, it has also been investigated as a potential candidate for multiple device applications ranging from photovoltaics to sensors.[6]

Cu_2O layers for TFTs are traditionally fabricated by physical vapour deposition (PVD) methods, such as pulsed lased deposition (PLD)[7–9] and sputtering.[10–12] Solution-based processing methods have also been used, such as spin coating,[13,14] electrodeposition[15] and inkjet printing.[16] For scalable device applications it is crucial to be able to deposit films with uniform and controllable thickness and composition over large areas, preferably at low or moderate temperatures. Atomic layer deposition (ALD) has been proven invaluable for the fabrication of modern microelectronics, where it is used to produce ultra-thin high-quality dielectric films for devices including metal-oxide semiconductor field effect transistors (MOSFET) and dynamic random access memories (DRAM). ALD has the potential to be extended in production of active device layers. It has already shown to be capable of depositing n-type semiconducting films, such as IGZO,[17] with properties compatible with what has been achieved by PVD techniques.[2,17] The successful application of ALD grown n-type semiconducting oxides in TFTs has been demonstrated both on rigid and flexible substrates.[18,19] Development of ALD processes for p-type materials (NiO, CuO_x, SnO) has been mostly of interest for photovoltaics, especially in perovskite and tandem solar cells, where they can be used as electron-blocking and hole transport layers.[20] However, some examples of other electronics applications, such as p-type TFTs with ALD grown semiconductor channels have been published.[18,21,22] For example, high performing TFTs with ALD grown CuO_x films (consisting of both Cu_2O and CuO phases) have been reported by Maeng et al.[21] Their devices showed an unusually high field effect mobility of $\mu_{FE} = 5.6$ $cm^2V^{-1}s^{-1}$, which is higher

than the μ_{FE} of any reported CuO_x device in the literature. Unfortunately, to our best knowledge, these results have not yet been consistently reproduced, nor are there other reports of the use of ALD Cu_2O in TFTs. However, ALD was used to demonstrate high-performance p-type TFTs with SnO channel.[22] There it was observed that applying an Al_2O_3 channel passivation significantly improves the TFT performance via the reduction of trap states at the interface.

Here, we investigate the influence of an ALD Al_2O_3 passivation layer on the performance of p-type TFTs with an ALD grown Cu_2O channel. We show that passivation and subsequent vacuum annealing improve the transistor performance metrics. In addition to device measurements, the Al_2O_3/Cu_2O interface was characterised in detail by using x-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM) to obtain more information of the interface modification taking place during the deposition of the Al_2O_3 on the Cu_2O. Furthermore, we discuss the significance of the interface formation and other passivation mechanisms of the ALD Al_2O_3 film, such as the effect of the high fixed charge, on the improved performance of the Cu_2O p-channel TFTs.

Results and discussion

Cu_2O film characterization

The X-ray diffraction pattern of a 40 nm thick Cu_2O film is presented in Fig. 1(a). The GIXRD revealed that the films were polycrystalline Cu_2O, with the most intense reflections associated to the (200), (111), and (220) planes of the cubic Cu_2O. No trace of CuO or Cu were detected, indicating that the films were phase-pure Cu_2O, with crystallite size of ca. 30 nm. The crystalline structure of the films was visible also by AFM (see example Fig. 1(b)) showing the films to have distinct grains in the morphology with a high surface roughness of ca. 4.5 nm (RMS). Despite the high film roughness, we can assume the films to be continuous, based on the detailed growth analysis of corresponding ALD Cu_2O films reported by Iivonen

et al. in Ref.[23] Hall effect measurements confirmed the p-type conductivity of the films, with a resistivity of ρ= 300 Ωcm, hole density of N = 10^{16} cm^{-3} and Hall mobility μ_H = 0.6 $cm^2V^{-1}s^{-1}$. The Hall hole mobility is somewhat lower than what has been reported earlier for Cu_2O films. However, as-deposited films processed at lower temperatures generally pose a lower hole mobility, in the order of few $cm^2V^{-1}s^{-1}$ [5,10,12,24,25] as a maximum, than films deposited and/or treated at high temperatures, in which the mobility can reach tens of $cm^2V^{-1}s^{-1}$ [3,7] but the variation between different reports is vast. In our case the low hole mobility may be due to low film thickness, which, combined with small grain size and high surface roughness, limits the conduction. Han et al. have investigated the role of the Cu_2O film morphology on the charge carrier characteristics, and they concluded that nanocrystalline structure of thin Cu_2O films can suggest the presence of potential energy barriers at grain boundaries, leading to effects such as grain boundary scattering, which hinders the hole transport in the thin films.[26] This is further enhanced by the formation of a conductive CuO layer onto the grain surfaces.[27]

TFT performance

The Cu_2O films were tested as p-channels in simple bottom-gate thin film transistor devices with Au source and drain electrodes and p-Si substrate acting as a common gate (see inset in Fig. 2). The switching characteristics of the as-deposited films without the Al_2O_3 passivation layer were negligible as shown in Fig. 2. With a 10 nm Al_2O_3 layer deposited on the Cu_2O channel the off-state drain current ($|I_{DS}|$) at positive gate voltage V_{GS} decreased by three orders of magnitude and switching with $I_{on}/I_{off}\approx$ 30 was measured. It has been shown that the gap state density in oxide semiconductor TFTs can be affected by the ambient moisture and oxygen adsorption on the top channel surface, which can be suppressed by the passivation layer.[28] However, for this effect the type or fabrication method of the passivation layer seems not to be critical, as improvements in the performance of n- and p-type TFTs have been reported with different ALD and solution-processed oxide films as well as with

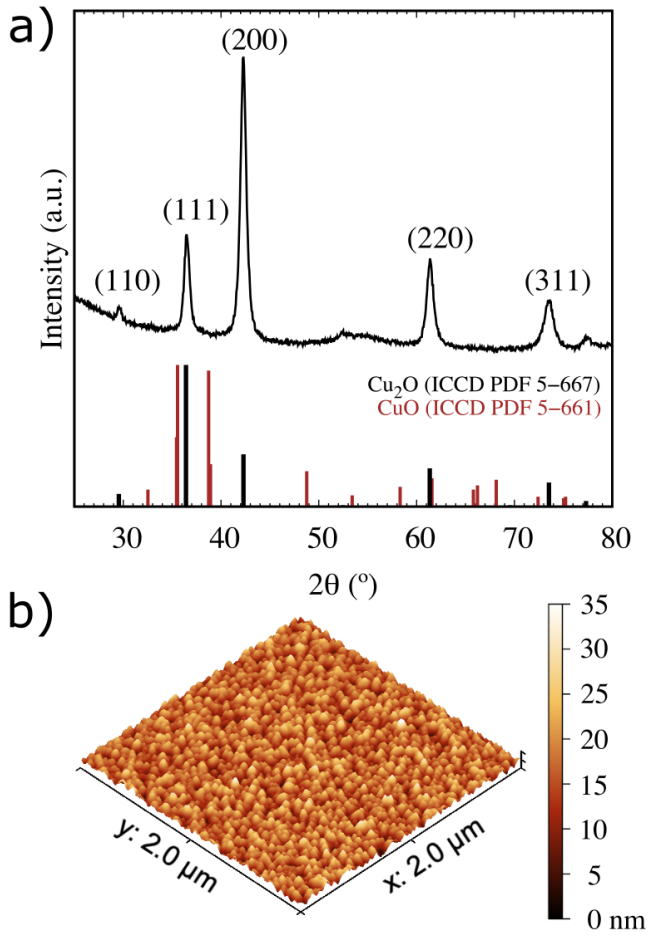

Figure 1: a) XRD pattern of the as-deposited, phase-pure polycrystalline Cu_2O film and the ICCD cards for both Cu_2O and CuO, used for indexing. b) 3D AFM image of 2 µm × 2 µm area of the corresponding film. The film roughness (RMS) is 4.5 nm.

organic passivation layers.[22,29–31]

To further improve TFT performance, the devices were annealed for 10 mins in 1.5 mbar N_2 directly after Al_2O_3 deposition. A low vacuum environment was chosen to prevent phase transitions of the Cu_2O layer into CuO or Cu. As seen in Fig 3(a) the transfer characteristics of the devices started to improve after annealing at 250 °C, but the most significant effect was gained at 300 °C, with output characteristics shown in Fig. 3(b). At higher annealing temperatures transfer characteristics begun to deteriorate. In the devices annealed at 400 °C no switching was observed, and a positive I_{DS} was recorded (data not shown). In the unpatterned Al_2O_3/Cu_2O film reference sample on glasss the 400 °C annealing caused

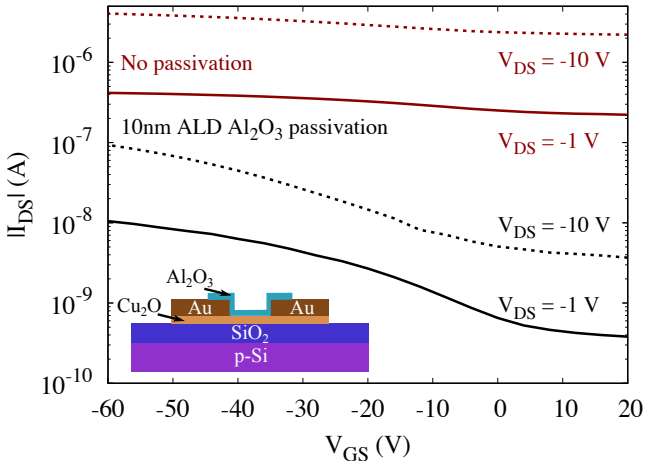

Figure 2: Gate transfer characteristics of a TFT device with 40 nm ALD Cu_2O p-channel, with and without Al_2O_3 passivation, shown as black and dark-red curves, respectively. In both cases the device is measured with drain voltages (V_{DS}) of -10.0 V (dashed lines) and -1.0 V (solid lines). Inset shows the schematic of the TFT device with Al_2O_3 passivation layer.

color changes visible to the naked eye, potentially indicating a partial reduction into metallic Cu. The same effect was observed also when the annealing was performed in 1 atm Ar atmosphere at the same temperature.

Despite the increase in the switching ratio of up to $I_{on}/I_{off} = 5 \cdot 10^3$ in the sample annealed at 300 °C, the carrier mobility remained low, with field-effect mobility for the as-deposited and annealed devices being $\mu_{FE} \approx 1.5 \cdot 10^{-3}$ $cm^2V^{-1}s^{-1}$, which was calculated as $\mu_{FE}=(g_m L)/(WC_{ox}V_{DS})$, where g_m is the transconductance ($g_m=\delta I_{DS}/\delta V_{GS}$), L and W the channel length and width, respectively, (L=50 µm, W=1000 µm), and C_{ox} the gate dielectric capacitance per unit area, calculated using a dielectric constant of 3.9 for SiO_2 gate oxide. Additionally, high operating voltages were required for switching, even for devices with enhanced characteristics, with a threshold voltage V_{TH} and subthreshold swing SS of -19.8 V and 11.5 V dec^{-1}, respectively. The corresponding V_{TH} and SS of the as-deposited device with Al_2O_3 passivation were -13.0 V and 29.2 V dec^{-1}, respectively.

The characteristics of the TFTs without the Al_2O_3 layer were not improved upon annealing, and Hall effect measurements showed there to be no change in the carrier mobility of the annealed Cu_2O samples (Fig. S1 in the Supporting Information). Therefore, it can

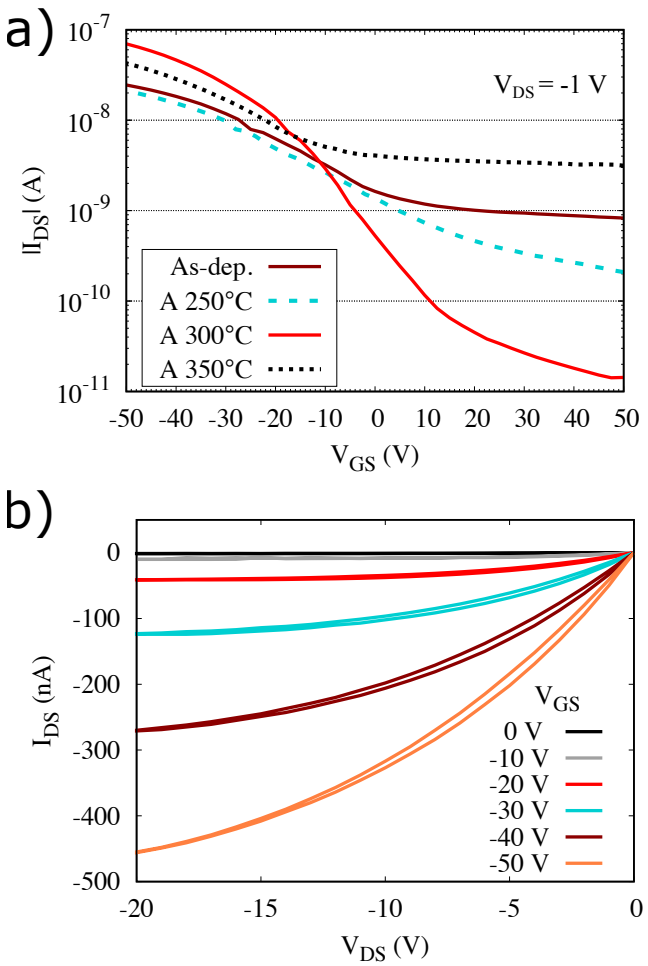

Figure 3: (a) Transfer characteristics of the Cu_2O TFTs with Al_2O_3 passivation, annealed in low-vacuum at different temperatures. Measured with V_{DS}=-1.0 V. (b) Output characteristics of a device annealed at 300 °C.

be concluded that the Al_2O_3 passivation is the reason for the improved performance. Similar effects have been reported for p-type TFTs with passivated SnO channels.[22,32] Kim et al. showed an improvement in devices with ALD SnO channel passivated with ALD Al_2O_3, which was further enhanced by subsequent annealing.[22] Similar observations were made by Qu et al., who passivated sputtered SnO channels by ALD Al_2O_3 as well as with organic coatings.[32] Our results are consistent with these findings, both reporting an increase in the I_{on}/I_{off} ratio and a decrease in SS upon ALD Al_2O_3 passivation. These changes can be associated with a reduction in the trap state density at the channel surface. It seems that the ALD Al_2O_3 passivation has more impact on reducing the deep trap state density, both in

the Cu_2O and SnO, indicated by the reduction in the SS. On the other hand, the shallow traps (tail states near the valence band), are less affected, as the the carrier mobility does not increase significantly.[32] Interestingly, it has been reported[29] that passivation of n-type oxide TFTs by ALD Al_2O_3 increases the mobility and SS which is opposite to what has been observed for the p-type devices.

The low field-effect mobility in the order of $\mu_{FE} = 10^{-3} - 10^{-2}$ $cm^2V^{-1}s^{-1}$ is typical for Cu_2O TFTs processed at low/moderate temperatures and with thin channel layer of few tens of nm, regardless of the deposition technique.[3,10,14] However, there are some reports where orders of magnitude higher μ_{FE} values, up to 6 $cm^2V^{-1}s^{-1}$ have been achieved, even with a room-temperature processing and mixed phase Cu_2O-CuO films.[21,33] The limited mobility in Cu_2O thin films is typically associated with the high density of subgap trap states and grain boundary scattering.[3,26] Additionally, it has been shown that a CuO layer can form at the Cu_2O/SiO_2 interface already at 300 °C, which further increases the trap density and, hence, has a negative impact on the transfer characteristics.[9] Therefore, it has been suggested that replacing SiO_2 with a high-k dielectric may result in better performance.[8,34]

We also tested devices with a 75 nm thick ALD Al_2O_3 gate oxide, and observed switching in the devices with a decreased SS (7.5 V dec^{-1}) and a V_{TH} of 10.6 V (See Fig. S2), indeed indicating a reduction in the trap states at the dielectric/semiconductor interface. However, in this case the Al_2O_3 gate oxide had a lower breakdown voltage than the 100 nm SiO_2, which meant that the channel was not yet fully depleted when the gate modulation was lost, limiting both the I_{on}/I_{off} ratio and the mobility.

To investigate the effect of annealing on the Al_2O_3/Cu_2O stack in detail, a high-temperature GIXRD measurement was performed. 10 nm Al_2O_3 was deposited on a 40 nm Cu_2O sample and the diffraction patterns were collected at 150–600 °C in 20 mbar N_2 (Fig. 4). It was observed that at 250 °C the (111) and (200) reflections shift towards larger 2ϑ angles, indicating a decrease in the unit-cell parameters, possibly due to stress relaxation when the annealing temperature exceeds the deposition temperature. As seen in the samples annealed

earlier, signs of metallic Cu appeared also in the passivated sample. These changes, seen as reflections at ca. 43° and 50.5°, take place just above 300 °C. At 475°C the Cu reflections disappear and features corresponding to formation of CuO become visible. These changes in the film structure upon annealing could explain the observed narrow annealing temperature window for optimal TFT performance.

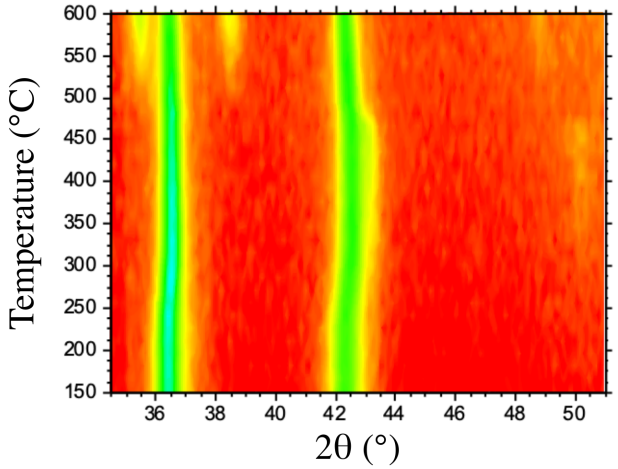

Figure 4: 2D high-temperature GIXRD pattern of the 10 nm Al_2O_3/40 nm Cu_2O stack annealed to 150–600 °C in 20 mbar N_2. High intensity lines correspond to the Cu_2O (111) and (200) reflections. The intensity is plotted in logscale.

Moreover, when annealed under similar conditions, a Cu_2O film without the Al_2O_3 layer undergoes oxidation to CuO already at 300 °C (Fig. S3), showing the importance of the Al_2O_3 layer to the phase-stability of the films during annealing. This behaviour of both the bare ALD Cu_2O and the $Al_2O_3Cu_2O$ film stack differ from what has been shown for Cu_2O films and devices fabricated by physical deposition methods such as PLD and sputtering. There a high temperature deposition or annealing at 500–800 °C, both in vacuum and inert gas atmosphere have shown to improve the device performance significantly by reduction of the CuO phases on the grain boundaries and increase in the Cu_2O crystallite and grain sizes, while the Cu_2O phase remains stable.[3,8,11,26,35,36] Though the film thickness may have an effect on the film behaviour during the annealing, it does not fully explain the observed differences between PVD and ALD deposited Cu_2O. One explanation is that the grain

boundaries of the nanocrystalline ALD Cu_2O contain a higher density of hydroxyl groups, which then accelerate the film reduction, despite the presence of the passivation layer, and the partial oxidation into CuO is later initiated by the oxygen diffusion from both the Al_2O_3 layer as well as the SiO_2 gate oxide. However, this remains inconclusive.

Al_2O_3/Cu_2O interface characterisation

Our results and the previous studies on the passivation of TFTs with oxide semiconductor channels show that quality of the interface between the channel oxide and the passivation layer can have a significant impact on the device performance. Especially, in the case of passivation by chemical routes, such as ALD, it can be assumed that the interface is further modified by the surface chemistry taking place during the layer deposition. It has been shown that exposure to certain ALD metal precursors, namely alkyl compounds, can reduce a surface oxide layer if the reactions are energetically favourable,[37–39] and this is also routinely utilized e.g. in so-called "self-cleaning" process of III-V semiconductor materials.[40] In the case of copper oxide surfaces, for surface reactions of diethylzinc, commonly used as a precursor for ALD ZnO, the Gibbs free energies for reduction reactions of Cu_2O surface into metallic Cu are ΔG_r = (-300)–(-200) kJ mol^{-1} (T = 373 K).[38] The reactions between TMA and Cu_2O can be assumed to be even more favourable due to higher reactivity of the TMA. The reduction of oxidized Cu surface during the first Al_2O_3 cycles has been verified both numerically and experimentally.[39,41]

Gharachorlou et al. investigated the TMA and hydroxyl-free copper surface reactions and presented the mechanism where the Cu_2O surface is reduced by the highly exothermic stepwise dissociative adsorption reactions of the TMA on the surface. This leads to the consumption of the surface oxygen atoms by the Al to form $CuAlO_2$ and the remaining Cu to be in the reduced Cu^0 state during the first Al_2O_3 cycles. This results in island-type growth of $CuAlO_2$ followed by Al_2O_3 film growth when the available Cu_2O sites have been

used. Their proposed overall reaction for the $CuAlO_2$ and Cu formation by TMA is:[39]

$$2Cu_2O + Al(CH_3)_3 \rightarrow CuAlO_2 + 3Cu + 2CH_4(g) + CH_{ads} \ . \quad (1)$$

Using a process with H_2O as a reactant leads to surface hydroxyl groups forming during deposition. However, it can be assumed that the mechanism described above is still valid, because it has been calculated that the hydroxyl coverage does not affect the TMA dissociation on the surface, but only on growth efficiency.[42]

The formation of a $CuAlO_2$ interface could be beneficial to TFT performance, because it is a known p-type material with low V_{Cu} formation energy.[43] In order to investigate in detail the reduction of Cu_2O by TMA, and the formation of the $CuAlO_2$ interface layer, samples were prepared for XPS and TEM. XPS was used to analyse Cu_2O films with and without the Al_2O_3 passivation and subsequent annealing at 300 °C. To minimize the need of Ar^+ etching to reach the Al_2O_3/Cu_2O interface, only 20 cycles i.e. ca. 2 nm of Al_2O_3 was deposited on samples for XPS measurements. The XPS of as-deposited Cu_2O without the Al_2O_3 layer confirmed the films to be phase-pure Cu_2O seen both in the Cu 2p and Cu LMM spectra, with a minor CuO content present at the film surface, as well as a high content of hydroxyl groups, as seen in the measured O 1s spectra (See Fig. S4).

The effect of the annealing on the Cu_2O film was investigated by measuring a sample annealed at 300 °C. No changes to the film composition were observed (Fig. S5). Figure 5 shows the XPS spectra of the Al_2O_3/Cu_2O films, before and after annealing at 300 °C. As seen in Fig. 5(a) the Cu 2p spectra of the both films show the absence of the CuO phase. However, the differentiation of between the Cu^+ and Cu^0 states cannot be done from the Cu 2p spectrum. The complementary Cu LMM spectra of the samples in Fig. 5(b) show the significant broadening of the Auger electron peak compared to the Cu_2O sample without the Al_2O_3 layer. This corresponds to the presence of the metallic Cu^0 at the Al_2O_3/Cu_2O interface, confirming the reduction of the Cu_2O due to TMA exposure.[44] This Cu^0 can remain

metallic even after the subsequent pulsing of H_2O, as the oxidation reactions into Cu_2O or CuO are not thermodynamically favourable (Tab. S1(a) and (b)). However, the oxidation by residual O_2 in the deposition reactor is possible (Tab. S1(b) and (c)). Furthermore, because the TMA adsorption and dissociation is not favourable on Cu sites, it is feasible to assume that the metallic Cu^0 is not consumed to form $CuAlO_2$ or oxidised to copper oxides but will remain at the interface, as shown by our results.

The O 1s spectra were also recorded from both samples. The deconvoluted spectra in Fig. 5(c) and (d) show the oxygen in lattice Cu_2O at 530.2 eV, a minor CuO contribution at 529.8 eV, and Al_2O_3 bound oxygen at 531.6 eV, as well as the presence of high hydroxyl concentration ($\sim$532 eV).[45] This is contributed by both the persistent surface hydroxyl groups on the Cu_2O as well as the remaining -OH species in the Al_2O_3 from the TMA + water process at relatively low deposition temperature of 150 °C. There is a small difference in the O 1s spectra of the as-deposited and annealed samples, namely in the Al_2O_3 related O content, which may indicate a partial diffusion of the Al into the Cu_2O film or a densification of the film upon annealing, which would lead to a slightly different etching rate during the Ar ion sputter cleaning.

However, the measured *ex-situ* XPS data can not be reliably used to confirm the presence of the $CuAlO_2$ phase at the Al_2O_3/Cu_2O interface, as the related changes are too subtle to be distinguished from the Al_2O_3 and Cu_2O signals within the probed volume. Moreover, we measured the valence spectra of the annealed Cu_2O and Al_2O_3/Cu_2O samples. Deuermeier et al. reported a shift in the binding energy of a Cu_2O during the ALD of Al_2O_3. In their *in situ* XPS experiments on ALD Al_2O_3 growth on sputtered Cu_2O surface the position of the valence band edge ($E_F - E_{VB}$) of the Cu_2O increased from original 0.4 eV to 0.6 eV after the first Al_2O_3 ALD cycle indicating a formation of Cu/Cu_2O Schottky junction.[41] Though our core level LMM spectrum showed the formation of the Cu, similar indication of a Schottky junction formation was not observed in the valence spectra and 0.9 eV $E_F - E_{VB}$ was measured for both the original Cu_2O as well as for the Al_2O_3/Cu_2O interface (See Fig.

S6). However, this does not exclude the potential Fermi level pinning at the interface due to the reasons explained above.

To obtain more evidence on the proposed $CuAlO_2$ interface layer formation, a sample with 10 nm Al_2O_3 deposited on Cu_2O, annealed at 300 °C, was imaged with TEM. The TEM and STEM coupled with EDS elemental mapping was recorded from the film interface (Fig. 6) from the very thin edge of the TEM foil. Figure 6(a) shows a low magnification image confirming the film stack, with a Cu_2O film sandwiched between two 10 nm Al_2O_3 films on SiO_2/Si. In Fig. 6(b) the enlarged TEM shows the polycrystalline Cu_2O and with the conformal, amorphous Al_2O_3 on top. The STEM image (6c) along with the EDS mapping results (6d) at the interface region reveals a 1–2 nm region at the interface with a mixed Al and Cu oxide composition (Fig. 6(d)). Though the actual composition of this region cannot be reliably determined from the STEM-EDS data, it is in qualitative agreement with the observations by Gharachorlou et al. of a formation of a $CuAlO_2$ layer during the first Al_2O_3 cycles according to Eq. 1.

The partial reduction of the film surface by the TMA can explain the decreased I_{DS} over the whole gate voltage range when the Al_2O_3 passivation layer is applied, as presented in Fig. 2. It has been shown that the inevitable formation of thin CuO layer on the Cu_2O grain surfaces under ambient conditions increases the conductivity of Cu_2O films, which can affect the device performance.[27] The surface Cu_2O reduction by TMA thus decreases the film conductivity. However, this reduction mechanism and formation of the interfacial $CuAlO_2$ do not fully explain the significant improvement in the TFT performance by the decrease in the device off-state current. We tested the effect of the Al_2O_3 film thickness on the TFT transfer characteristics and observed that when the nominal Al_2O_3 thickness was 2–5 nm the device performance was similar to TFTs without the Al_2O_3 passivation and the improvement in the TFT transfer characteristics was detected only with a thicker, 10 nm Al_2O_3 layers (See Fig. S7). This indicates that the formation of the interface layer by the TMA exposure during the first couple of tens of deposition cycles is not sufficient in improving the device

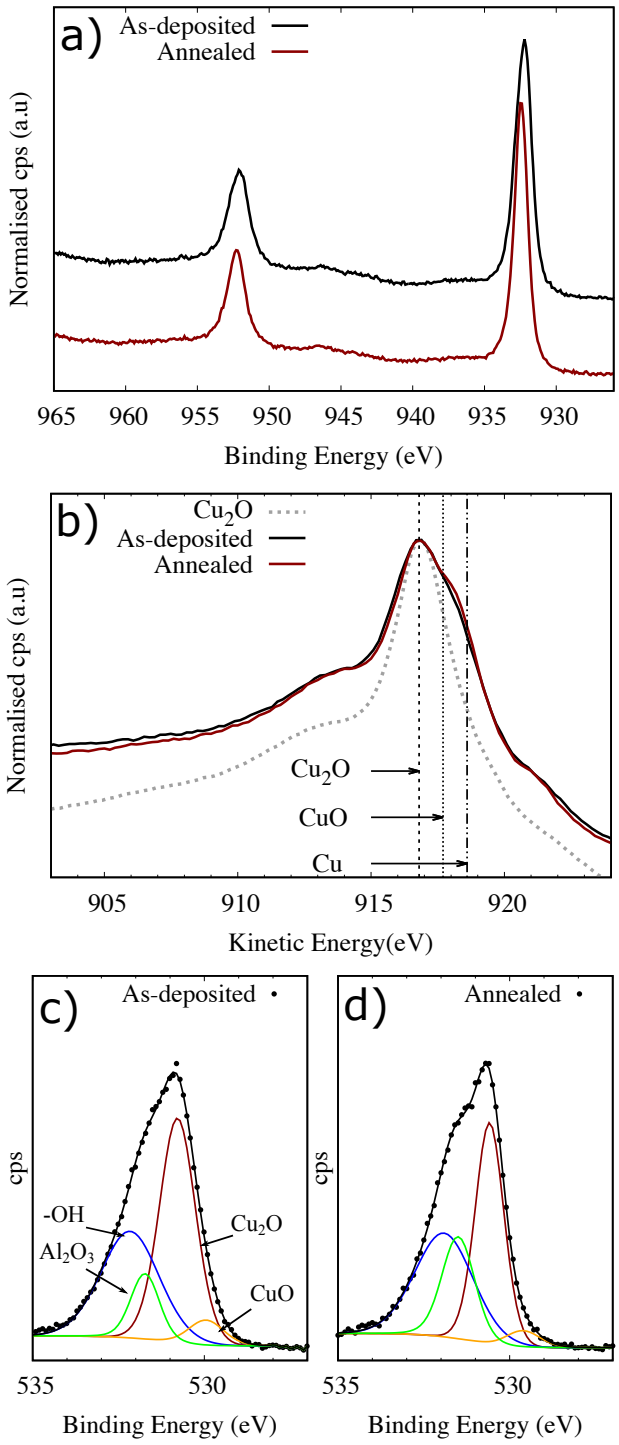

Figure 5: XPS spectra of the Al_2O_3/Cu_2O interface region, measured after 90 s 0.5 keV Ar^+ sputtering, (a) Cu 2p of the as-deposited (black) and annealed (dark red) samples. (b) Cu LMM Auger electron spectra, corresponding spectrum of a Cu_2O film without the Al_2O_3 passivation layer shown by dashed grey line as a reference. The O 1s spectra of the (c) as-deposited and (d) annealed sample. The deconvoluted peaks correspond to oxygen in Cu_2O (dark red), CuO (orange), hydroxyl -OH (blue), and Al_2O_3 (green).

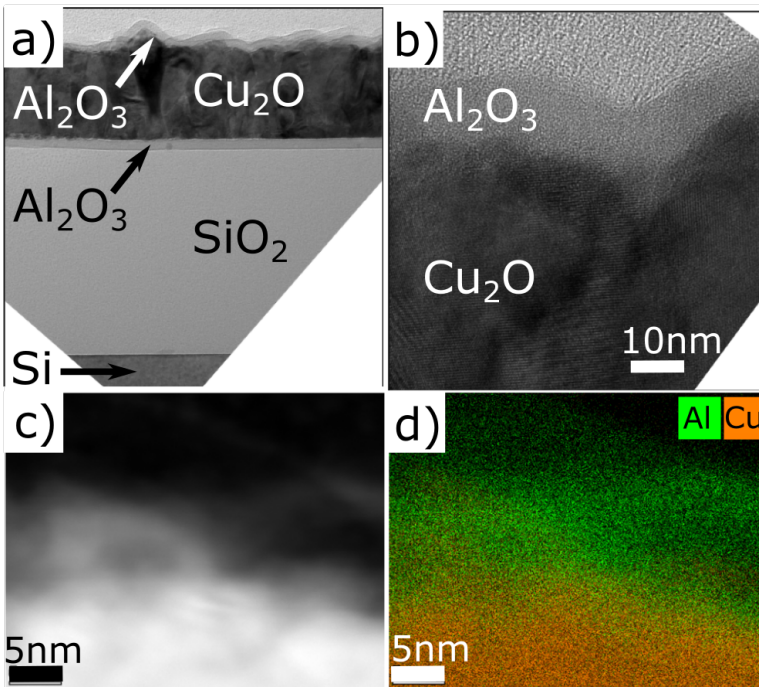

Figure 6: Transmission electron microscopy (TEM) micrographs (a)-(b) of a Cu_2O thin film sample with 10 nm Al_2O_3 passivation layer, annealed in 1.5 mbar N_2 for 10 min. (c) Scanning transmission electron microscope (STEM) image and (d) the corresponding TEM-EDS mapping of Al and Cu at the sample interface.

performance, but thicker coverage with the Al_2O_3 layer is required. The thicker layer can act as an enhanced barrier against oxygen and moisture, but it is unlikely that this is the sole reason for the significant TFT performance improvement. Therefore, the key to the improved characteristics are likely in the properties of the ALD Al_2O_3 film itself.

A plausible reason for the observed behaviour is the high negative fixed charge density ($Q_f = 10^{-13}$ cm^{-2}) of the ALD Al_2O_3, which has traditionally been utilised in c-Si solar cells where it reduces the recombination losses on the Si surface via surface defect density reduction and by field-effect passivation. The field-effect passivation is based on the reduction of electron or hole concentrations on the surface/interface by the means of an intrinsic internal electric field.[46,47] In our measured TFT data the impact of the field-effect passivation is indicated by the negative shift in the V_{TH} and the reduction in the I_{off}. It has previously been reported by Han et al. that the high off-state current in the Cu_2O TFTs is due to accumulation of minority charge carriers (electrons) at positive gate voltage regime.[48] We

also measured the capacitance of the as-deposited and passivated p-channels (See Fig. S8). The results qualitatively show the enhanced hole accumulation in the channel, especially at low frequencies, which supports the hypothesis of the reduced electron accumulation. The application of the field-effect passivation by ALD Al_2O_3 on the Cu_2O channel and subsequent annealing can be an effective way in reducing the accumulation of electrons via electrostatic shielding, which leads to the orders of magnitude lower off-state current and, hence, improves the performance of TFTs with Cu_2O p-channels.

Conclusions

p-Type thin film transistors with ALD grown phase pure polycrystalline Cu_2O channel layer were fabricated. The TFTs with as-deposited films showed only limited switching performance, due to the unoptimised film properties and processing parameters, but the characteristics were improved by depositing an 10 nm ALD Al_2O_3 passivation layer on the Cu_2O channel and by subsequent annealing at 300 °C in low vacuum. The analysis of the transfer characteristics indicates that the improvement is due to the reduced number of trap states at the channel. The detailed investigation of the Al_2O_3/Cu_2O interface by XPS and TEM showed a partial reduction of the Cu_2O and possible formation of a 1-2 nm thick $CuAlO_2$ layer. This presents an example of the importance of understanding the surface reactions and interface modification during the ALD growth on multilayer stacks, as it can significantly impact the performance of thin film devices.Here, the reduced copper oxide surface and the formation of p-type $CuAlO_2$ layer with a low Cu vacancy formation energy can be beneficial to the device operation, but cannot solely explain the better performance of the Al_2O_3 passivated TFTs. Hence, we conclude that the main benefit of the Al_2O_3 passivation comes from its high negative fixed charge density that reduces the accumulation of electrons in the Cu_2O channel when positive gate voltage is applied and, thus, reduces the I_{off} of the devices. While the field-effect passivation may not be applicable to tradition nanoscale

Si-based CMOS devices, as it influences the V_{th} and the transport of charge carriers in ways that can be detrimental to the circuit operation, it can be an useful tool in the development of alternative approaches that utilise p-type oxide semiconductors with moderate charge carrier density.

Experimental

The Cu_2O films were grown on 5 cm × 5 cm substrates of thermally grown SiO_2 on p-Si (resistivity 0.001 Ωcm, Si-Mat) by atomic layer deposition at 200 °C in an ASM F-120 reactor. Copper(II) acetate $Cu(OAc)_2$ with source temperature of 185 °C, and water vapor were used as precursors. Each Cu_2O ALD cycle consisted of 2 s $Cu(OAc)_2$ pulse / 2 s purge / 1.5 s H_2O pulse / 1.5 s purge, which resulted a growth per cycle of 0.011 nm. A fluorine-free precursor was chosen because residual fluorine impurities can affect the electrical properties of the films, F being a known n-type dopant, and, additionally lead to poor adhesion of the films due to the accumulation of the fluorine into the interfaces.[49] Details of the growth chemistry and materials characterisation are published by Iivonen et al. in Ref.[23] No further optimisation of the Cu_2O film processing or thickness was done regarding the device operation. Bottom gate TFT structures, with the Si substrate acting as a common gate and thermally grown 100 nm thick SiO_2 as a gate dielectric, were fabricated with a standard photolithography and nanofabrication methods to test the performance of the Cu_2O films. The 40 nm Cu_2O films were patterned by wet etching using diluted (0.025 M aq.) HCl, and 100 nm thick Au source and drain electrodes were deposited by thermal evaporation (Edwards Coating System E306A), with a base pressure of 10^{-6} mbar. Au was chosen as the electrode material to ensure an ohmic contact was made between the film and the electrodes. That is because of the high work function (WF) of Au 5.1–5.4 eV[50] that matches the ca. 4.9–5.0 eV WF of Cu_2O,[27,51] as well as its high standard reduction potential, which avoids electrode oxidation during annealing. After electrode patterning, the device samples were diced, and the Cu_2O channel

was passivated by a 10 nm Al_2O_3 film grown by ALD (Cambridge Nanotech (Veeco) Savannah S100) at 150 °C with trimethylaluminium (TMA, Sigma Aldrich) and water vapour. Finally, the devices were annealed in 1.5 mbar N_2 at 200–400 °C for 10 minutes.

Film thickness was determined with x-ray reflectivity (XRR) using a PANalytical X'Pert Pro MPD diffractometer, which was also used for x-ray diffraction (XRD) measurements. The measurements were performed in the grazing incidence (GIXRD) geometry at an incidence angle of 1°. The same geometry was used with the high-temperature GIXRD measurements, where Anton-Paar HTK1200N furnace was used for sample heating in 20 mbar N_2 (N_2 flow 40 sccm) and data were collected at 150–600 °C with 15 °C intervals. Atomic force microscopy (AFM) images were taken with Bruker Multimode 8. The electrical properties of the Cu_2O films were characterised by Hall-effect measurements using van der Pauw configuration with a magnetic field of 0.2 T at room temperature (MMR Technologies Hall System). Thin film transistors were measured using a Cascade probe station and Agilent B1500A semiconductor device parameter analyser. The electrical characterisations were performed in dark to suppress the film photoconductivity. In the interface examinations Escalab (Thermo Fisher Scientific) x-ray microprobe was used for x-ray photoelectron spectroscopy (XPS), and the results were analysed using CasaXPS processing software. Transmission electron microscopy (TEM) imaging was done using FEI TALOS T200X operated at 200 kV with EDS for elemental mapping.

Acknowledgement

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work at Purdue University.

Supporting Information Available

More detailed information and experimental data on Hall mobility, thin film transistor characteristics, high-temperature GIXRD, X-ray photoelectron spectroscopy, and Cu and Cu_2O oxidation are available in Supporting Information.

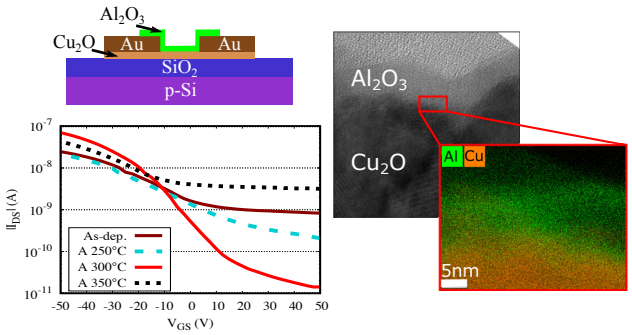

Figure 7: For Table of Contents Only

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Supporting Information

Role of ALD Al_2O_3 surface passivation on the performance of p-type Cu_2O thin film transistors

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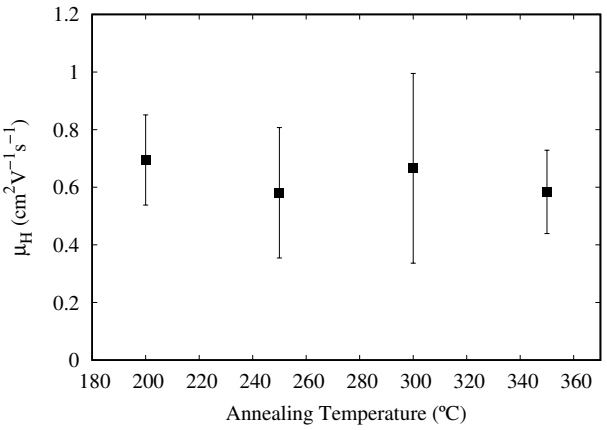

Figure S1: Hall-measured hole mobility μ_H in the annealed Cu_2O films. Data point at 200 °C represents the as-deposited film. The errorbars are the standard deviation of the multiple measurements taken from two samples annealed in same conditions.

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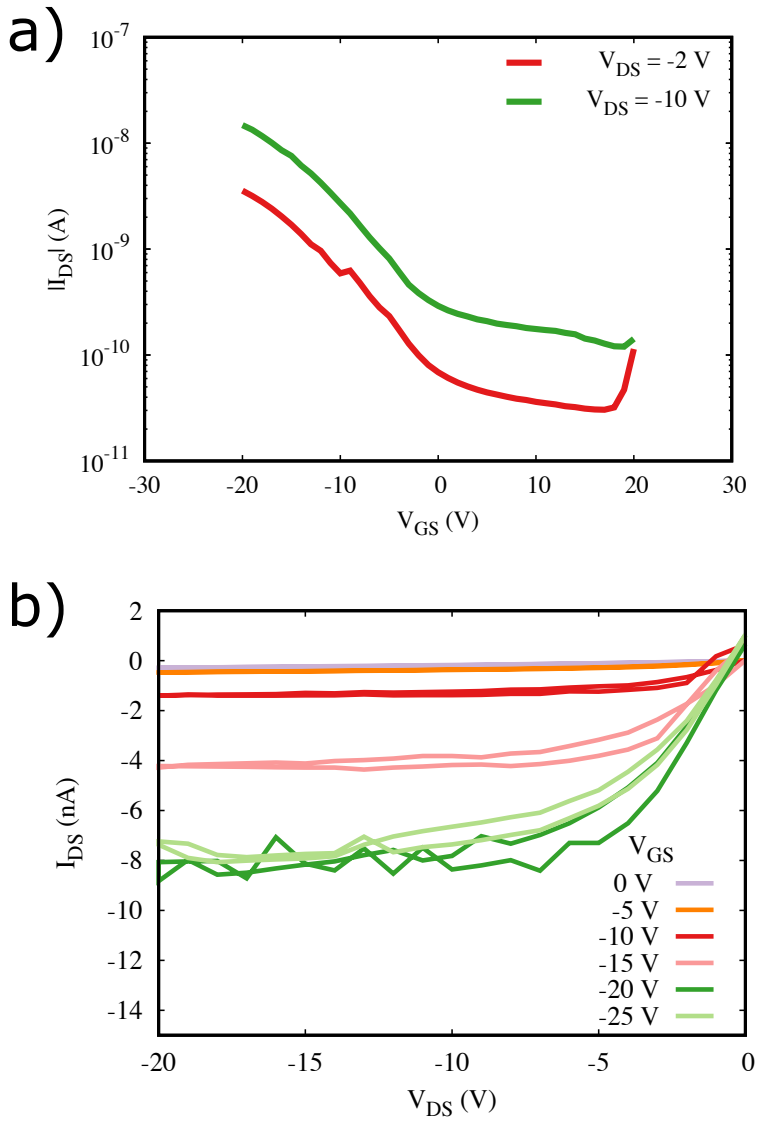

Figure S2: a) Transfer characteristics of a Cu_2O p-channel TFT with 75 nm Al_2O_3 gate oxide, the device is passivated with 10 nm Al_2O_3 and subsequently annealed at 300 °C, W/L = 20. (b) TFT output characteristics measured from the same device.

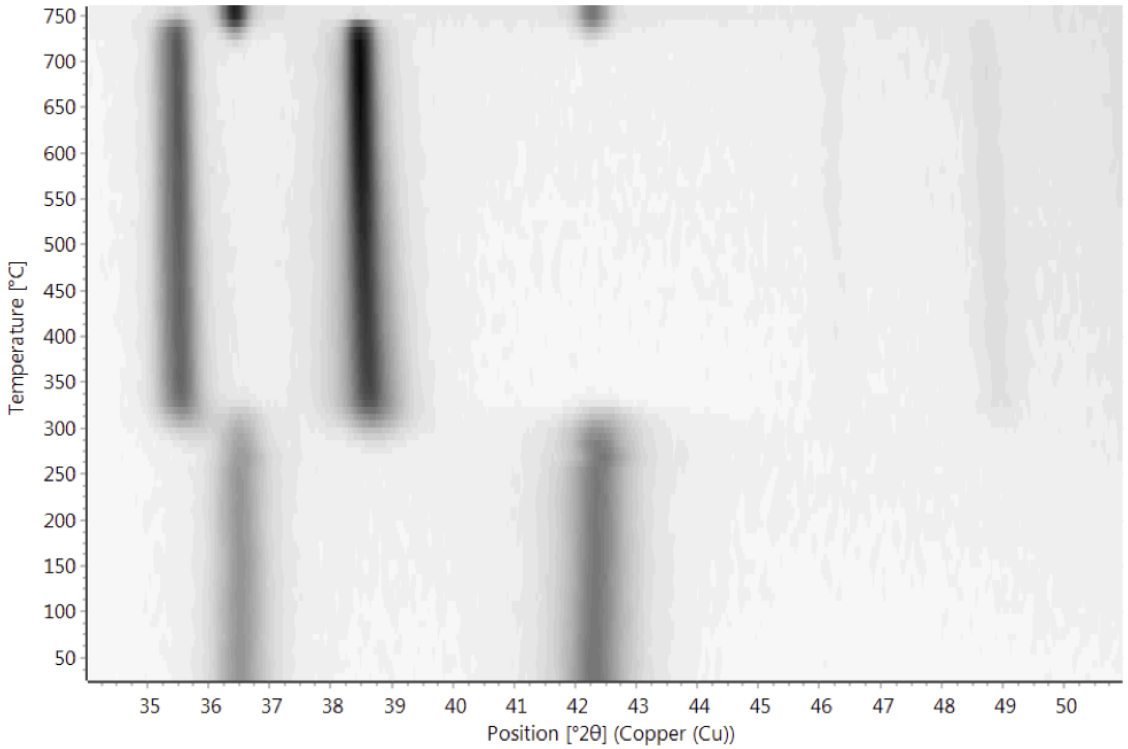

Figure S3: High-temperature GIXRD pattern of an ALD Cu_2O film measured at 20 mbar N2 (flow 40 sccm). The Cu_2O film with most intense reflections (111) at 36.4° and (200) at 42.3°, oxidises into CuO at 300 °C, as seen in appearance of CuO (002) and (111) reflections at 35.4° and 38.6°, respectively.

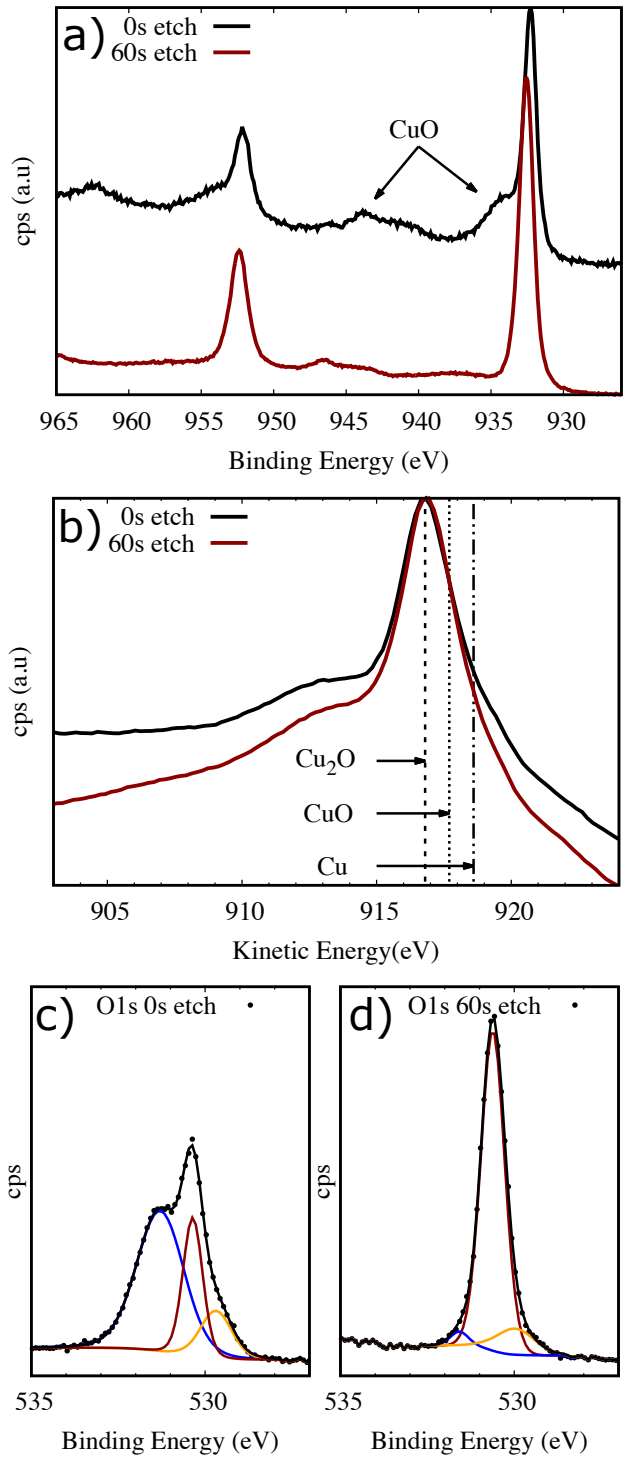

Figure S4: XPS spectra of the as deposited Cu_2O film, (a) Cu 2p, (b) Cu LMM (normalized), (c)&(d) O1s, measured after 0 s and 60 s of 0.5 keV Ar^+ sputter surface cleaning. The deconvoluted peaks in (c) and (d) correspond to Cu_2O lattice oxygen (dark-red), CuO (orange), and hydroxyl groups (-OH, blue)

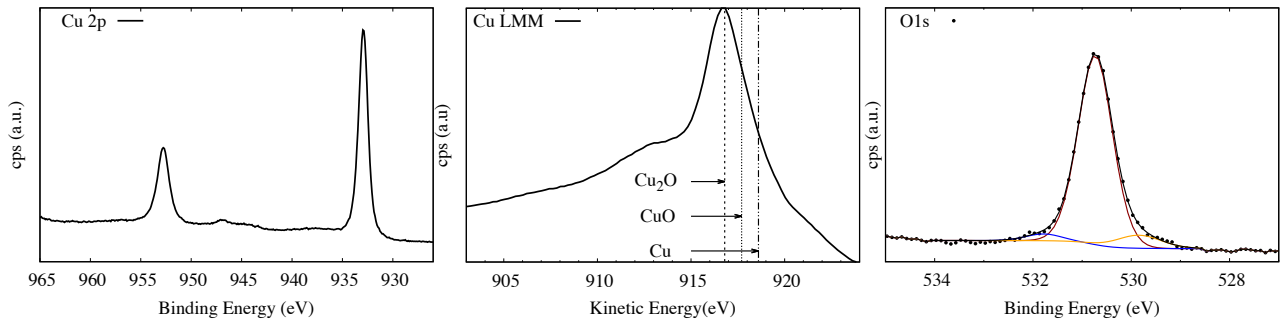

Figure S5: XPS Cu2p, Cu LMM, and O 1s spectra of the Cu_2O film annealed 10 min in 1.5 mbar at 300 °C, measured after 30 s 0.5 keV Ar^+ sputter surface cleaning.

Table S1: Thermodynamics of oxidation reactions of Cu^0 into Cu_2O and CuO by H_2O or O_2

(a) $\mathbf{2Cu + H_2O(g) = Cu_2O + H_2(g)}$

T (°C)	ΔH (kJ)	ΔS (J/K)	ΔG (kJ)
0	73.003	-32.630	81.916
100	73.969	-29.640	85.030
200	75.132	-26.886	87.853
300	76.389	-24.477	90.419
400	77.705	-22.363	92.758
500	79.054	-20.494	94.899
600	80.417	-18.837	96.864
700	81.766	-17.374	98.673
800	83.071	-16.097	100.345
900	84.288	-15.011	101.899
1000	85.372	-14.124	103.354

(b) $\mathbf{Cu + H_2O(g) = CuO + H_2(g)}$

T (°C)	ΔH (kJ)	ΔS (J/K)	ΔG (kJ)
0	84.200	-49.639	97.759
100	85.596	-45.317	102.506
200	87.210	-41.489	106.841
300	88.896	-38.257	110.823
400	90.599	-35.519	114.508
500	92.287	-33.180	117.940
600	93.941	-31.169	121.155
700	95.540	-29.434	124.183
800	97.064	-27.942	127.050
900	98.490	-26.671	129.779
1000	99.792	-25.605	132.391

(c) $\mathbf{2Cu + O_2(g) = 2CuO}$

T (°C)	ΔH (kJ)	ΔS (J/K)	ΔG (kJ)
0	-314.762	-186.407	-263.845
100	-313.941	-183.909	-245.315
200	-312.597	-180.733	-227.083
300	-311.029	-177.732	-209.162
400	-309.350	-175.033	-191.526
500	-307.609	-172.623	-174.146
600	-305.833	-170.463	-156.993
700	-304.045	-168.524	-140.046
800	-302.272	-166.790	-123.282
900	-300.553	-165.258	-106.681
1000	-298.933	-163.932	-90.223

(d) $\mathbf{4Cu + O_2(g) = 2Cu_2O}$

T (°C)	ΔH (kJ)	ΔS (J/K)	ΔG (kJ)
0	-337.156	-152.388	-295.531
100	-337.193	-152.557	-280.266
200	-336.752	-151.526	-265.058
300	-336.043	-150.172	-249.971
400	-335.138	-148.721	-235.026
500	-334.075	-147.251	-220.228
600	-332.881	-145.800	-205.576
700	-331.592	-144.404	-191.066
800	-330.259	-143.099	-176.692
900	-328.956	-141.938	-162.441
1000	-327.773	-140.969	-148.298

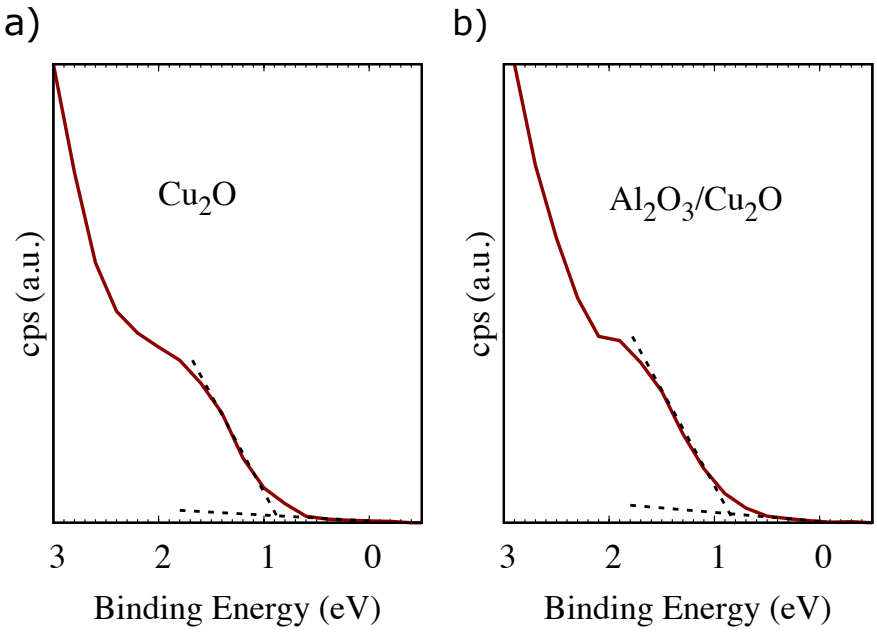

Figure S6: XPS valence edge spectra of a) Cu_2O film ($E_F - E_{VB} = 0.9$ eV), and b) Al_2O_3/Cu_2O interface after a 90 s sputtering with 0.5 keV Ar^+ ($E_F - E_{VB} = 0.9$ eV)

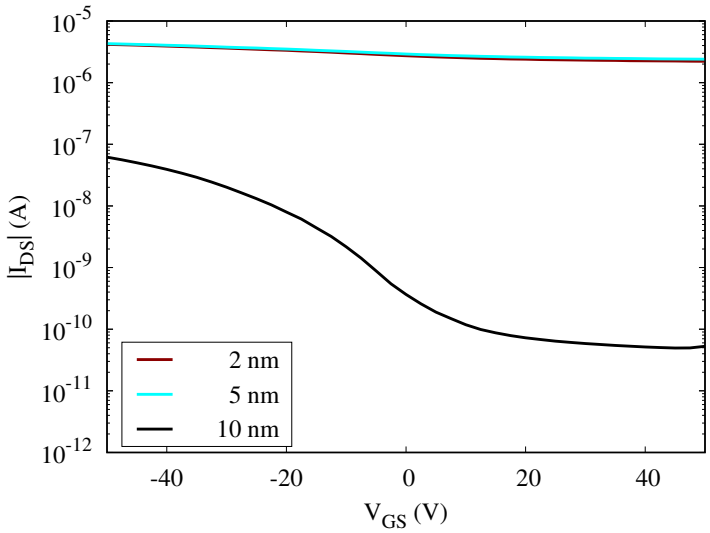

Figure S7: The effect of ALD Al_2O_3 layer thickness on the transfer characteristics of the Cu_2O p-channel TFTs, all samples were annealed for 10 min at 300 °C 1.5 mbar N_2

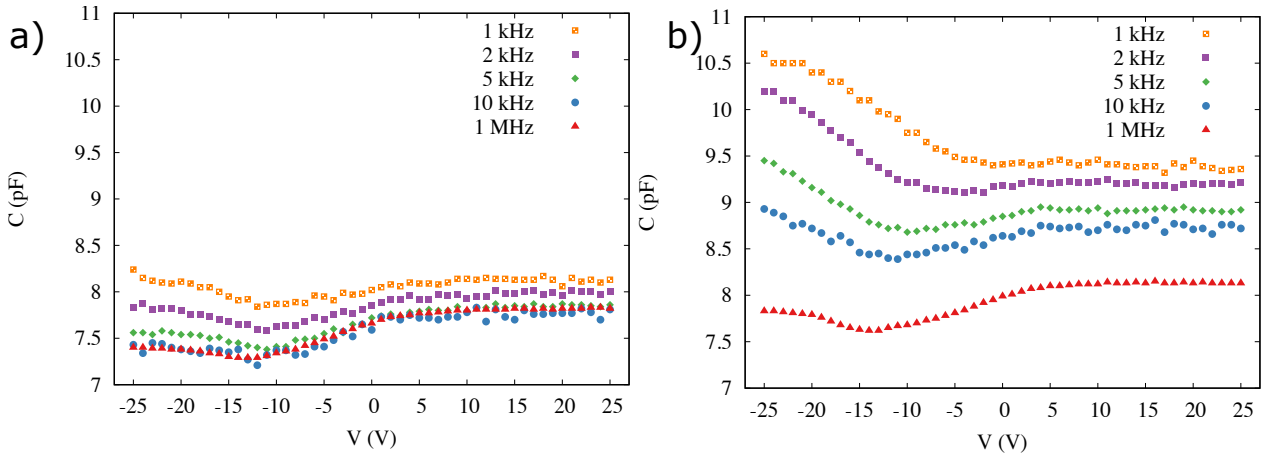

Figure S8: C-V characteristics of the Cu_2O channel (a) as-deposited, and (b) after 10 nm Al_2O_3 passivation and annealing. The effect of passivation is seen as enhanced hole accumulation at low frequencies. Note: Data measured by coupling the S&D electrodes and using the common Si gate as a bottom electrode, which leads to highly asymmetric surface areas, and therefore increases the uncertainty of the measured data.