DESIGN OF LOW-COST ENERGY HARVESTING AND DELIVERY SYSTEMS FOR SELF-POWERED DEVICES: APPLICATION TO AUTHENTICATION IC

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DESIGN OF LOW-COST ENERGY HARVESTING AND DELIVERY SYSTEMS FOR SELF-POWERED DEVICES: APPLICATION TO AUTHENTICATION IC

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A journey of a thousand miles starts with a single step.

Lao-Tzu

To my family.

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SUMMARY

High levels of mobility and accessibility of devices have been made possible through the development of wireless technologies. However, challenges in power delivery and security must also be addressed to realize the Internet of Everything (IoE). This is especially critical for standalone devices such as ultra-low-power sensors and active identification tags. Energy harvesting can be introduced as power links for these systems to address restrictions in cost and footprint. Increased operational lifetime and reduced maintenance cost can be achieved without relying on battery capacity to sustain depleted energy. For the purpose of authentication, wake-on-interrogate with harvesting-based power delivery can further improve security.

This thesis investigates the development of low-cost energy harvesting and delivery systems for low-power low-duty-cycle devices. Initially, we begin by designing a power management scheme for on-demand power delivery. The baseline implementation is also used to identify critical challenges for low-power energy harvesting. We further propose a robust self-powered energy harvesting and delivery system (EHDS) design as a solution to achieve energy autonomy in standalone systems. The design demonstrates a complete ecosystem for low-overhead pulse-frequency modulated (PFM) harvesting while reducing harvesting window confinement and overall implementation footprint. Two transient-based models are developed for improved accuracy during design space exploration and optimization for both PFM power conversion and energy harvesting. Finally, a low-power authentication IC is demonstrated and projected designs for self-powered System-on-Chips (SoCs) are presented. The proposed designs are prototyped in two test-chips in a 65nm CMOS process and measurement data showcase improved performance in terms of battery power, cold-start duration, passives (inductance and capacitance) needed, and end-to-end harvesting/conversion efficiency.

CHAPTER 1
INTRODUCTION

From motion activated lights and health monitoring devices to driver safety precautions and smart cities, the Internet of Everything (IoE), which connects not only networks of items but also users, has emerged as an inevitable outcome of increased expectations of electronic devices in this generation. The immersive user experience deeply integrated into our everyday lives has been enabled by ubiquitous devices that highlight not only machine-to-machine communication but also people-to-machine communication. The endless demand for "smart-er" electronic devices has brought many conveniences, and with them, many challenges that need to be overcome.

IoE edge devices can vary greatly in design and complexity depending on target applications but, fundamentally, a complete solution would contain four functionalities: sensing, computation, communication and power delivery. While all functions are essential to establish a self-sustained system, power delivery is the basis to guaranteeing robustness and integrity of other blocks, and the physical implementation is often the bottleneck of reducing form factor, which are all critical tributes to ensure a friction-less introduction of these devices during deployment.

Devices that can be embedded with existing appliances can conveniently utilize available power resources with proper conversion. However, standalone devices that do not have dedicated power supplies suffer under the restraint of energy storage capacity. Energy harvesting implementation in small-scale can extend lifetimes of battery-powered devices and full autonomy can be made possible by carefully balancing the trade-off between operation duty-cycle and quiescent/active power consumption.

Existing issues in prior approaches can be summarized as such:

- Low-power IoE devices and systems minimize overall power consumption through

reducing IDLE power for "OFF" periods between operations.

- Large storage capacitors/batteries are traditionally required to retain minimal system operation over long intervals (> 10s).

- Cold-start operation with harvesting sources can minimize IDLE power and provide increased robustness for self-powered operation. However, it also suffers from high overhead from additional auxiliary converters or slow boot-strapped operation.

- Energy harvesting from restricted source power (due to: limited form factor $\times$ power density) requires discrete conduction mode (PFM) harvesting systems for high efficiency.

- Compact models for discrete conduction mode power delivery lose accuracy at high conversion ratio and cannot be used for system-level design and analysis.

- Decoupled design of harvesting sources and power management units rely on near-DC fine-grain maximum power point tracking in PFM and results in wasted energy or additional system overhead.

1.1 Thesis Statement

The objective of this thesis is to demonstrate that tracking maximum system power through output regulation metrics, controlling PMU operation based on harvesting capability of input sources and enabling robust cold-configuration of harvesting source networks to produce high voltage allows simultaneous tuning of harvesting efficiency and conversion efficiency, reduced passives, and shorter ACTIVE time and wake-up time, to ultimately achieve a low-cost low-overhead energy harvesting and delivery solution for self powered devices.

1.2 Key Contributions

The key contributions of this thesis can be summarized as:

- **Development of an analytical model and simulator for PFM power conversion and harvesting:** A high accuracy model is developed to quickly explore high-level design of PFM IVRs and enable tailoring the EHDS design depending on the target loading module/input source behavior. The model is verified by both simulation and silicon data. Harvesting voltage tracking is additionally implemented to constitute a semi-simulator for PFM harvesting to model EHDS operation with limited power and is used for design projections for different target specifications where harvesting sources can be integrated on-chip.

- **Demonstrate system-focused solutions for ensuring robust PFM harvesting with reduced resources (capacitance, inductance, footprint):** Critical challenges for PFM harvesting are identified with silicon measurements and used as guidelines to design an all-in-one solution for low-power energy harvesting. The proposed approach "borrows" energy from IDLE states by increasing the input regulation window while controlling thresholds to ensure energy equilibrium. A complete system is developed to adapt to this change including an output-based MPPT tracking algorithm, configurable sampling fraction based harvesting efficiency tuning and switching frequency based conversion efficiency tuning. The approach also reduces the passives needed for the EHDS. Wake-up assist circuitry is designed to accelerate bootstrapped cold-start operation while introducing little area overhead for implementation.

- **Design and testing of a visible-light (VL) centric authentication SoC:** A low-power sensing method with on-chip photo-diodes for visible-light based data receiving is developed to and integrating with a off-chip harvesting power link to

demonstrate full interrogation cycle of a low-power authentication IC. A converter-embedded load-wake-up scheme is created with a pulse frequency modulated (PFM) boost regulator (BR) is designed with input-power based load control. The implementation decouples high-power loads from battery power and uses the PFM-BR for on-demand power delivery from harvesting sources. This approach reduces system IDLE power significantly by ensuring that only the PFM-BR remains ON and "waiting" for on-demand operation and that loads are activated only when input power is adequate. Additional power-gate control with existing PFM BR regulation signals enhances wake-up operation robustness by reducing BR load during system wake-up. Projected self-powered design with prior PFM EHDS is also presented.

1.3 Organization of this thesis

Chapter 2 will present a detailed survey of existing literature to explain and identify critical challenges for low-power self-powered systems. Existing methods that have been commonly implemented and the overhead that they introduce are also outlined.

Chapter 3 will discuss and investigate operation of the PMU scheme that will be implemented for the EHDS in detail: a PFM boost regulator. Detailed steps to develop a high accuracy model are presented and followed by accuracy validation and possible applications.

Chapter 4 demonstrates a power-management scheme that relieves the burden of high-power loading modules on battery power and uses the PMU to determine on-demand activation of loads. Test-chip measurements are provided to demonstrate the operation and are further used to identify and justify challenges in PFM harvesting.

Chapter 5 presents an all-in-one PFM EHDS with fast cold-start, low area, low passives and embedded self-tuning. Design and implementation details are discussed and silicon measurements are presented.

Chapter 6 explores the target application space with a sample design: a visible light

based authentication IC. This chapter will focus on implementation details for developing a low-power on-chip signal sensing scheme. Silicon measurements for characterizing the sensing circuit and demonstrating a full interrogation cycle are discussed.

Chapter 7 presents a design methodology to project fully self-powered SoCs that can be achieved with the designs presented in prior chapters. An EHDS semi-simulator is developed based on the DC-DC conversion model in Chapter 3 and observations in Chapter 5 to evaluate system performance and used for design space exploration.

Chapter 8 summarizes research contributions of this thesis and future research directions.

CHAPTER 2
LITERATURE SURVEY

2.1 Power management for increased lifetime

The deployment of energy-constrained edge devices, such as ultra-low power sensors, is an integral part in the establishment of the Internet-of-Everything. One of the most critical challenges is designing power management solutions for these device platforms. Among the vast field of devices designed for IoE applications, there is a specific subset that can be distinguished by their nature of operation - devices that only operate when interrogated. A representative example of such designs can be explained by investigating the operation of authentication tags [1, 2, 3].

These devices are often required to operate over long periods of time with limited opportunities for battery replacement. Therefore, without additional measures, the system lifetime would be mainly limited by idle power, operation duty cycle and capacity of the storage [4]. Instead of remaining idle yet powered-on by batteries, the discrete and infrequent nature of operation for authentication tags has motivated the design to be normally inaccessible (powered down) to eliminate IDLE power completely and allow indefinite increase in deployment duration. These tags then wake-up only via power transfer from an interrogation probe through energy-harvesting based power links that have been developed for on-demand power delivery [5, 6, 7, 8, 9]. However, compared to typical power conversion from reliable sources, energy harvesting also brings many challenges along with its convenience.

2.2 Energy Harvesting

2.2.1 Harvesting sources

Harvesting energy from surrounding environments, whether in the form of light, heat, or vibration is the key to relieving the usage of large batteries in a wireless application. Integrated harvesting sources such as Photovoltaic (PV) harvesters [10, 11, 12, 13, 6, 14] and Thermoelectric Generators (TEGs) [15, 16, 17, 18, 19] to achieve this goal have been proposed and demonstrated in previous literature. However, as the form factor also limits the power produced from these sources along with storage capacity, the harvested energy is generally low and highly variant. Therefore, maximizing harvested power and designing efficient power conversion with low-power solutions under these conditions are critical requirements to supplying loading modules with transduced ambient energy.

PV modules are DC harvesting sources that have been widely adopted for energy harvesting [11, 20, 14]. Electron-hole pairs are generated when light is applied to PV devices and are separated/collected through the electric field across the depletion region [12]. The biasing voltage directly modulates the depletion region and the generated photo-current (I_{ph}). Fig. 2.1 shows a plot of current-voltage and power-voltage characteristics for PV devices acquired from measurements. An advantage of PV harvesting sources is that they can generate relatively high voltage (> 0.2V) in nominal room-light environments. When properly controlled close to the maximum power point (MPP), PV harvesters can produce $>$1mW/cm^2 power density. When no current is drawn, PV devices enter open-circuit voltage (OCV) conditions, where equilibrium is reached and no photo-current is generated. When higher current is drawn from the harvesting node than what the harvester can produce, PV cells enter short-circuit/reverse-bias conditions. Therefore, a critical challenge for EHDS designs is controlling the PMU at the system level to prevent imposing undesired harvesting conditions on the harvesting source.

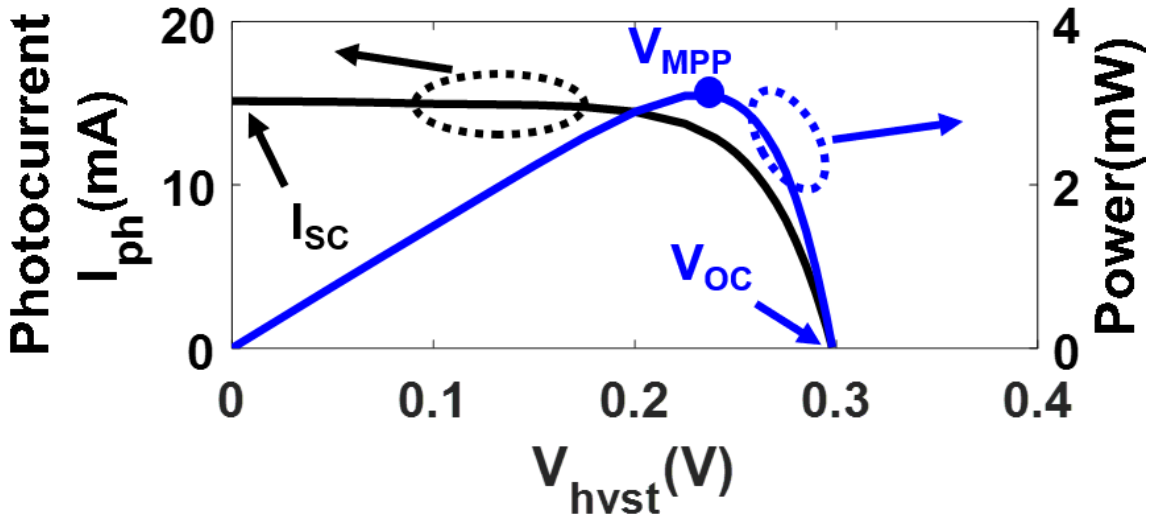


Figure 2.1: I-V and P-V characteristics of PV devices.

2.2.2 Power Management Unit (PMU) Architecture Selection

In most conventional applications, the architecture of the power converter defines the overall power conversion efficiency at given target load. However, when interfaced with non-ideal harvesting sources that have supply limited power, peak efficiency is no longer the highest priority when deciding which architecture to adopt. Instead, the adaptability to the designated range of operation conditions should be considered. Switch capacitor converters can have high efficiency when the conversion ratio is fixed but often experience efficiency drops outside of these ranges[21]. This makes the topology suitable for initial power conversion in multi-stage power conversion schemes and for applications where the operating condition can be pre-determined. pulse width modulated inductive voltage regulators can have low ripple, fast transient response time if the switching frequency and sampling rate are sufficiently high. In continuous conduction mode (CCM), the more-stable inductor current make impedance matching more controllable. However, the control is more complex and power hungry and the efficiency drop at low loads makes it more often used for high power applications [22]. Though adaptive-on-time (ADM) and PFM-controlled regulators all have lower efficiency at high load [23], they exhibit superior low-power conversion effi-

ciency by allowing idle periods in between active conversion operations. Furthermore, the nature of bang-bang PFM controls make it especially suitable for applications where the idle period is long and duty cycle is determined by the end user and not pre-designed and is the architecture that will be implemented in this thesis.

Conversion efficiency for low power PMUs

Regardless of architecture selected, custom design of the PMU is often required to ensure sufficiently high conversion efficiency based on the operating range of input source and output load. Techniques to improve designs and control methods of power converters have continuously been a celebrated topic of research. For example, control blocks with higher performance to improve efficiency by preventing inter-phase transition losses [24, 25] and designs with multiple control modes implemented to increase efficiency across a wide load range [23, 26] have been proposed over the years. While some methods may not be applicable when designing IVRs with a sub-mW harvested power budget, design of active control blocks in accordance with passive devices is increasingly important in this scenario. For low power operations, the efficiency bottleneck resides in the quiescent power consumed [27, 28]. Methods such as bias gating [29] to turn off certain unused functional blocks can reduce quiescent power to a minimum.

2.3 Full-System Design Challenges

Self-powered devices that operate in standalone environments are critical foundations for Internet of Things applications. One of the key challenges for these end-devices is to provide a robust, yet low-cost, low-overhead system for power management. Scavenging energy from harvesting sources [30, 31] and smart management of power delivery [32, 11, 33] have become integral parts of Energy Harvesting and Delivery Systems (EHDS) for self-powered devices to alleviate the overhead of costly high-capacity batteries and minimize cost for maintenance. A compact EHDS to achieve autonomous devices can be

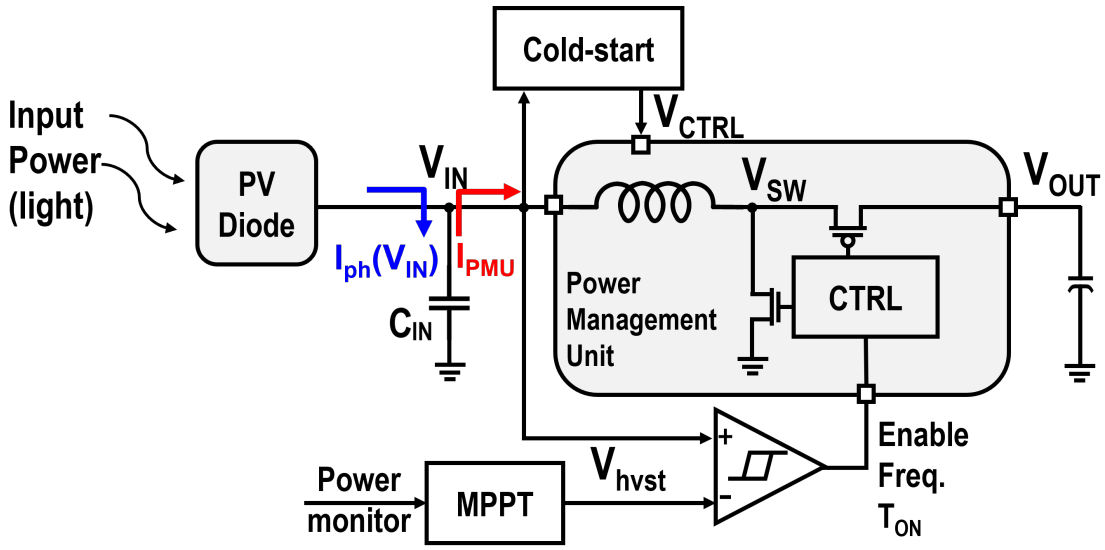


Figure 2.2: Schematic of generic EHDS.

created by integrating harvesting sources with integrated voltage regulators (IVRs). However, compared to power conversion from steady sources, the power that harvesting sources can provide depends on the strength of the input (light, heat, etc.) and biasing conditions of the transducer; which are highly variant and intermittent/unstable [18, 34]. To address this unique concern, additional control circuits for maximum power point tracking (MPPT) methods and cold-start techniques have been proposed and implemented to increase the robustness of EHDSs [35, 36] to support PMU operation.

Fig. 2.2 shows a schematic for a typical EHDS. For MPPT to dynamically adapt to variations in harvesting conditions, it will need to monitor certain metrics such as voltage/current/time for power evaluation. Time-based [37, 38] and indirect MPPT methods such as Fractional Open Circuit Voltage (FOCV) [33, 36] do not require power-hungry sensors that are necessary for direct MPPT [30] and have been implemented widely for light-weight EHDSs. However, regardless of the MPPT method implemented, a common challenge for EHDSs is that large passives are often required to ensure a sufficiently tight tracking window. Cold-start methods allow the power management unit (PMU) to enter typical operating conditions from power-free ("cold") states by generating sufficiently high control voltage (V_{CTRL}) for the PMU to initiate operation in a controlled manner.

2.3.1 Maximum Power Point Tracking

The harvested power from transducer sources is highly dependent on environmental settings and operating conditions. Maximum Power Point Tracking (MPPT) for harvesting sources is essential to achieving self-powered systems and extended lifetime. Without MPPT, the operating condition of the harvesting source will be dominated by the IVR operation and very likely converge close to short-circuit or open-circuit conditions, where little energy is harvested, depending on the target regulator load. Typical MPPT methods performed at the source are designed to determine the point of operation at which maximum power can be extracted from the source[10, 16, 39].

Various methods have been proposed over the years. Direct MPPT utilize voltage and/or current sensors[16] to obtain harvesting power information under different operating condition. One of the most simple and commonly adopted MPPT methods is the Fractional Open Circuit Voltage (FOCV), which is used when the harvesting source characteristics are know in advance. The maximum power point (MPP) is assumed to be at a fraction of the open circuit voltage by investigating the I-V and P-V curves. In implementation, a capacitive sample-and-hold circuits [40] are commonly used. Other methods include, but are not limited to, look-up-tables that are highly application dependent and incremental conductance (IC) and perturb and observe (P&O) methods that can be applied regardless of sensing method used [41].

Lee et.al.[14] has proposed a different viewpoint for MPPT implementation. Instead of adapting converters to adjust to source variations, re-configuration of the source to match converter specifications when operating conditions vary can also be done. Configuration of sources is conventionally used to shift the conversion responsibility to the harvesting sources when overhead of high conversion-ratio becomes large. In this work, reconfiguration of PV cell networks that are directly connected to a battery when exposed light intensity changes is demonstrated. Because the output voltage is fixed by the battery harvesting ability of the photodiodes under illumination variations will change if this voltage is

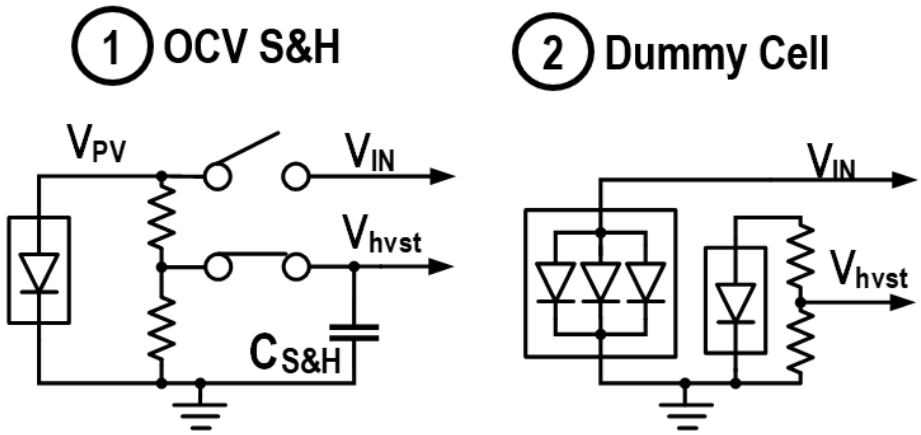


Figure 2.3: Typical FOCV methods.

directly applied to the harvesting node. Instead of decoupling the harvesting voltage from battery voltage with a power converter, configuring the photodiode array to have more diodes in series under low light, low V_{MPP} and vice versa is done to ensure the voltage across each photodiode is closer to its V_{MPP}.

To bypass the use of voltage and current sensors that would consume a substantial amount of power, time-based MPPT has been introduced. Lopez et.al. [38] used the characteristic that increase/decrease in power can be observed at opposite sides of the MPP, which is mapped by the charging time of the input capacitor, along with perturb and observe(P&O) tracking algorithm to implement MPPT. Rawy et. al. [42] moves one step further to normalize the charging time based one DAC values to use as the metric for power estimation. Liu et.al. [20] embeds the MPPT within the power conversion and measures the time and number of steps it takes to charge the output of the converter. However, this scheme requires the overhead of an additional buffer capacitor.

Fractional Open Circuit Voltage MPPT

One of the most prevalent topologies used in small scale harvesting systems is the fractional open circuit voltage (FOCV) method [33, 35]. This method is based on the assumption that the maximum power point is close to a fixed fraction of the OCV (V_{OC}), regardless of variations in input power. Fig. 2.3 shows two common FOCV implementations:

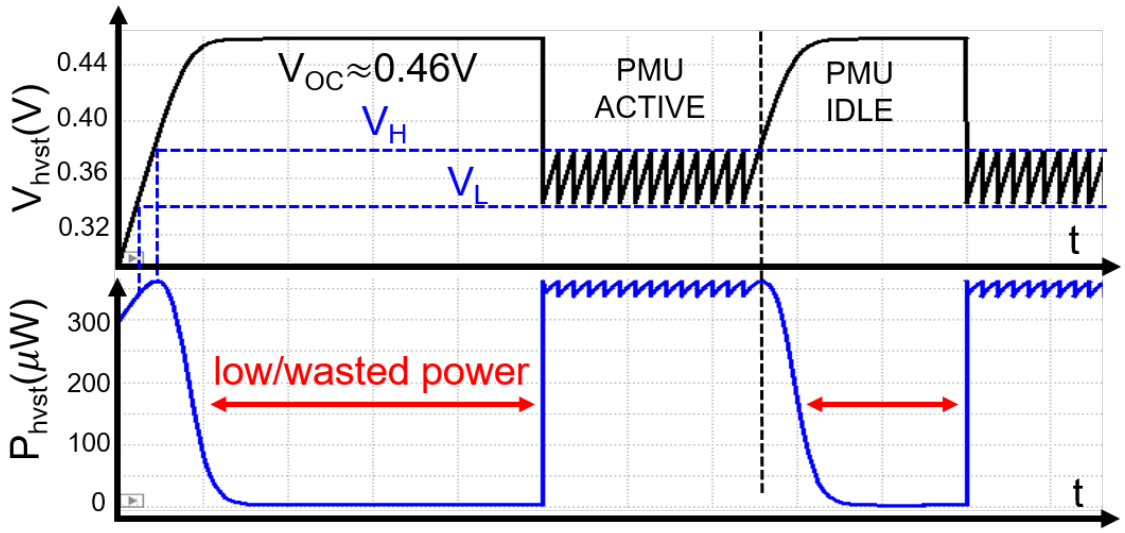


Figure 2.4: Transient of single-input single-output PFM boosting.

1) Sample & Hold through periodic disconnection of the source [40], *2)* Utilizing never-harvesting dummy cells that remain in OCV conditions [11]. Once V_{OC} is obtained, a pre-designed voltage division is sufficient to derive the MPP voltage V_{MPP} ($V_{MPP} \sim 0.78V_{OC}$ in Fig. 2.1), which is used as a reference to control the PMU for impedance matching within the EHDS. **FOCV benefits from its simplicity, but also introduces undesired area/wasted-energy overhead due to the need to obtain V_{OC} [36, 31].**

Impedance Matching Methods

Since the harvesting voltage (V_{hvst}) dynamically varies with both the current generated by the harvesting source and the current drawn by the PMU (Fig. 2.2), one can also indirectly modulate the harvesting voltage by carefully controlling the impedance of the PMU. Several different impedance matching techniques have been devised to bias the harvesting source. For example, impedance matching for MPPT in EHDSs can be performed by controlling the PMU duty cycle to modulate the harvesting voltage [18]. At equilibrium, the net increase in harvesting voltage (charged by the harvester) on the input capacitor will be equal to the net decrease (discharged with current drawn by PMU). To interface with low-power PMUs such as pulse frequency modulation (PFM) integrated voltage regula-

tors (IVRs), input hysteresis comparators [32] and switching frequency modulation [19] have both been implemented in prior works. However, due to burst-harvesting periods, the use of high capacitance ($> 10\mu$F) and high inductance ($> 10\mu$H) is often necessary to filter/dampen harvesting voltage ripple (Fig. 2.4) for MPPT and reduce current ripple for improved conversion efficiency [4, 38, 27, 39, 18, 11, 19].

2.3.2 Challenges for System Start-up with Power Conversion

System start-up is as crucial as its nominal operation. For small analog circuits, this is done by designing extra circuitry (often with capacitors/diode-connected transistors) to ensure initial biasing of critical nodes when supply undergoes a low to high transition. For larger systems, the startup is often built into the regulatory circuits.

Cold-start is a unique operation for EHDSs where the control voltage to the entire system starts from floating/grounded initial conditions and wakes up with harvested power. The ability to support cold-start is critical for self-powered EHDSs as it enables restoration of operation from power-drained conditions.

Prior Cold-start Approaches

Boot-strapped configuration of IVRs [43, 44] is the method of connecting IVR output back to its own voltage supply. When the input source is connected, boosting eventually brings the IVR to its nominal operating point and IVR regulation signifies the end of start-up. This is a commonly used method to allow the boost converters to completely power-down during idle, thus minimizing quiescent power. Kar et.al. [45] has also presented using stacked comparators to ensure initial states of switches can provide protection to circuits when the system is powered up with a voltage ramp. This is especially useful to ensure that output loads remain off to prevent start-up phases from exhausting source energy before control circuits kick in.

Bootstrapped cold-start requires voltage-invariant designs to allow boosting from low

voltages [29]. Before regulation can be reached, the PMU will be always-ON and continuously draws current from the harvesting source to boost the output voltage (which is connected back to the control voltage of the PMU). During this process, power consumption from control blocks (oscillator, analog comparators, power stage, etc.) within the PMU can be considered as increased load of the EHDS. The additional power burdens bootstrap operation and can result in excessive current drawn from the harvesting node. This reduces the harvesting voltage, and further lengthens cold-start periods.

A common approach is to have a secondary converter that is devoted for cold-start [18] to ensure that control power is decoupled from the load through a two-stage cold-start arrangement. This is usually implemented via switch-capacitor converters as they do not need high-performance voltage/current sensors to perform zero-current sensing [46]. Prior work has also demonstrated one-shot cold-start where only the control voltage of the low-side gate and driver needs to be charged [19] with the charge-pump. However, these designs present significant area overhead from large on-chip capacitance and increased transistor sizing to reduce transistor resistance at low voltages.

CHAPTER 3

ENERGY DELIVERY SYSTEM DESIGN AND ANALYSIS

Prior approaches for designing energy harvesting and delivery systems (EHDS) often focus on tailoring the power conversion module to maximize conversion efficiency at typical operating ranges (harvesting voltage) of a target harvesting source. Then, the efficiency is used to determine the size of the input source needed based on the target load demand. By decoupling the design of each stage, integration becomes very straightforward and simple. However, while this approach provides satisfactory results, it also limits space for possible system-level optimizations. Fig. 3.1 shows a diagram of common design dependencies and considerations within an EHDS.

Viewing/co-designing the EHDS at the system level instead of treating harvesting sources and power converters as separate modules can bring many opportunities and challenges. It

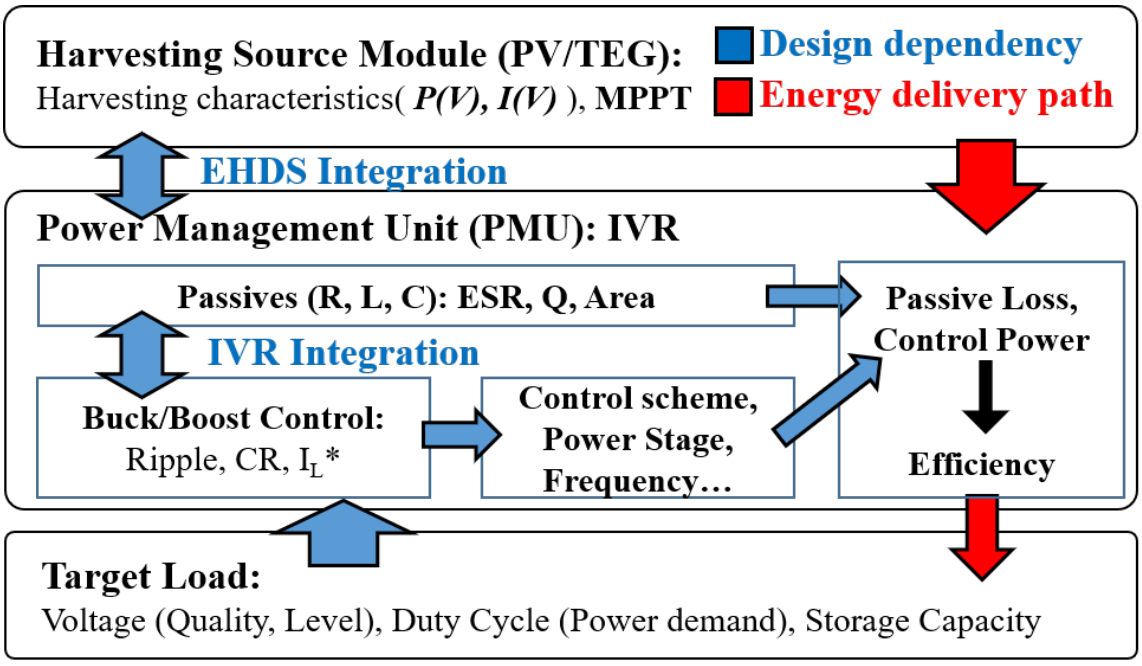


Figure 3.1: EHDS design considerations.

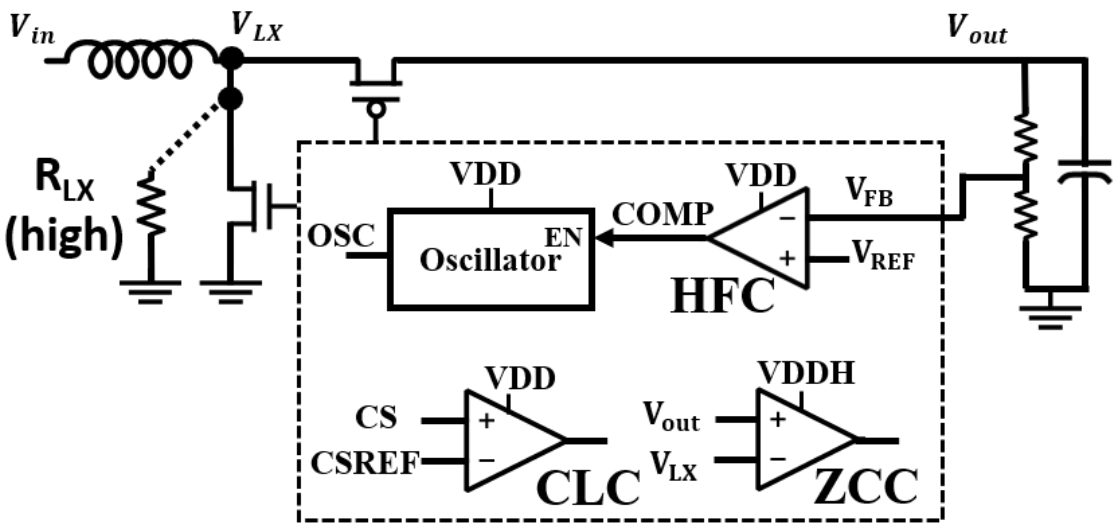


Figure 3.2: Analog PFM-BR schematic. (R_{LX} is only connected in simulations to increase simulation speed.)

also requires fast analytical models for design space exploration. This is mainly because transient simulations of L/C components in the IVR often take long periods of time to converge and complete. To maximize the potential of self-powered devices, we will begin with constructing and analyzing a compact model that can be used for system-level analysis of EHDSs. This chapter presents the steps taken to create a system-level evaluation framework, which is then validated and employed to perform high-level co-design.

3.1 PFM Boost Regulator Operation

For the PMU, we will focus on PFM controlled inductive voltage regulators that have superior efficiency for a wide conversion ratio range at lower loads[26, 25]. This makes them especially suitable for creating boost regulators (PFM-BRs) for up-converting EHDS output voltage from a low harvester output voltage. The PFM boost regulator chosen to be implemented and modeled is adapted from Ahmed et. al. [47]. The regulator design consists of the following major functioning blocks: Current Limit Comparator (CLC), Zero Current Comparator (ZCC), Oscillator (OSC), and Hysteresis Feedback Comparator (HFC).

Fig.3.2 shows a schematic of the PFM boost regulator. While the HFC defines voltage

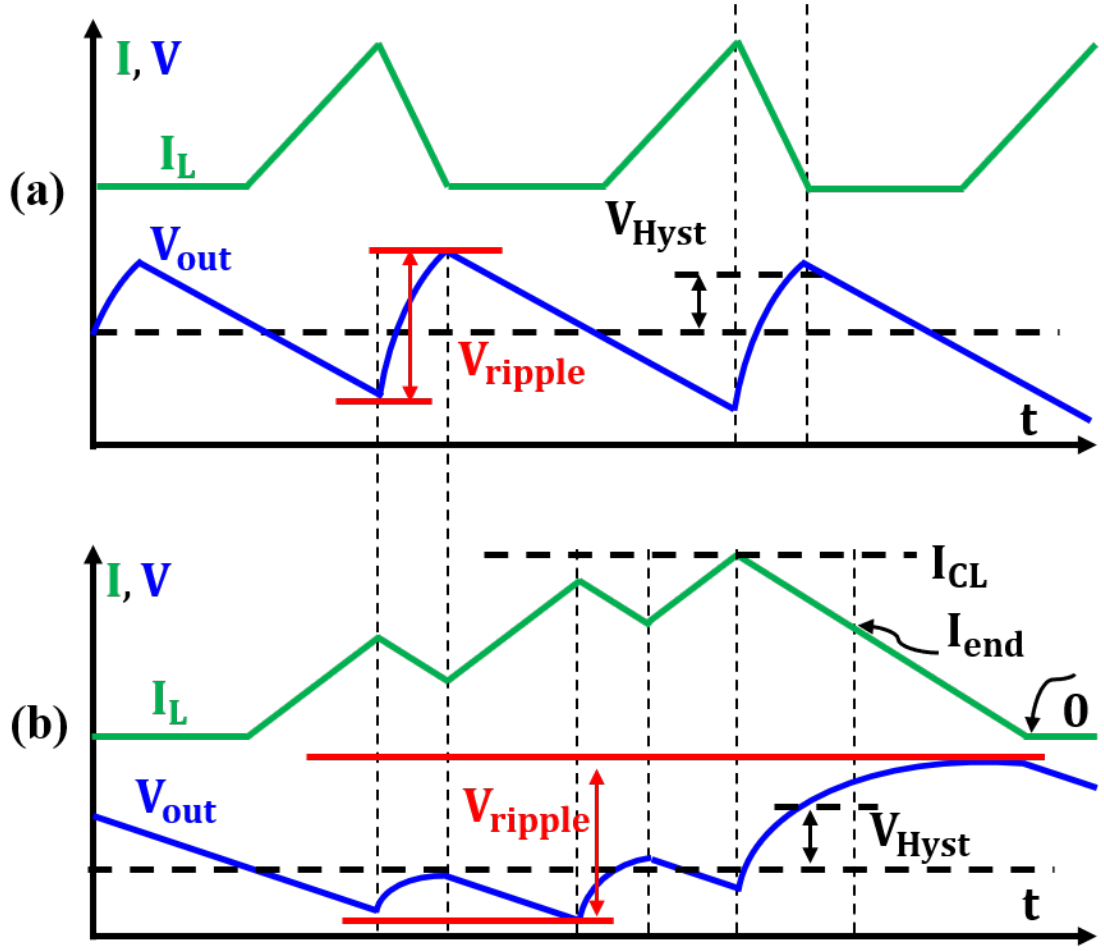


Figure 3.3: (a) Single-pulse operation (b) Multi-pulse operation for PFM-BR

hysteresis and is the main block that controls output regulation, the CLC and ZCC are designed to modulate inductor current behavior to improve conversion efficiency. When the inductor current surpasses a pre-designed current limit (I_{CL}), the CLC turns off the NFET and turns on the PFET to allow the current to decrease while charging the output capacitance. The ZCC is designed to turn off the PFET when the inductor current reaches zero to prevent reverse current flow from the output. The Oscillator (OSC) design defines duty cycle and switching frequency, which plays a critical role in determining power conversion capability and efficiency [43].

The internal operation of PFM BRs depends on the input voltage and the conversion ratio (V_{out}/V_{in}). Fig. 3.3 shows sample inductor current (I_L) and output voltage (V_{out})

waveforms that represent typical PFM operations. If the input voltage is high, the boosted charge in a single pulse is sufficient to increase the output voltage above the set hysteresis level and regulation is reached (Fig. 3.3(a)). We will refer to this mode as the single-pulse mode. Under low conversion ratio and high duty cycle, this control scheme enters multi-pulse operation, with exemplary waveforms shown in Fig.3.3(b).

The criteria to enter multi-pulse operation is decided by whether the inductor current is allowed to build with succeeding oscillator cycles under the condition that V_{hyst} is not reached within a single pulse. This means, net change in inductor current at the end of the OFF time (ΔI) for the oscillator should be higher than zero, as shown in (3.1-3.2). Where m_{pos} and m_{neg} represent the rising/falling slope of inductor current and T_{on}/T_{off} represent active high/low periods.

$$\Delta I = I_{\text{peak}} - I_{\text{drop}} = T_{\text{on}} m_{\text{pos}} - T_{\text{off}} m_{\text{neg}} \geq 0 \tag{3.1}$$

$$m_{\text{pos}} = V_{\text{in}}/L \tag{3.2}$$

$$m_{\text{neg}} = (V_{\text{out}} - V_{\text{in}})/L \tag{3.3}$$

The following derivation can be used to approximate the maximum output voltage ripple. Assuming for both single-pulse and multi-pulse operation, the hysteresis voltage threshold (V_{Hyst}) is a designed parameter of the HFC, the output ripple can be expressed as:

$$V_{\text{out,ripple}} = V_{\text{hyst}} + V_{\text{os}} + V_{\text{droop}} \tag{3.4}$$

Where V_{os} represents the overshoot above the hysteresis voltage can be expressed as:

$$V_{\text{os}} \leq V_{\text{os,max}} = (\frac{I_{\text{CL}}}{2} - I_{\text{load}}) T_{\text{boost}}/C_{\text{out}} \tag{3.5}$$

$$T_{\text{boost}} = \frac{I_{\text{end}} L}{V_{\text{out}} - V_{\text{in}}} \leq \frac{I_{\text{CL}} L}{V_{\text{out}} - V_{\text{in}}} \tag{3.6}$$

Where I_{CL}, C_{out} and I_{load} are the inductor current limit, output capacitance, and load current respectively. T_{boost} is the time it takes for the inductor current to fall to zero after the hysteresis upper limit is reached. L, V_{out}, V_{in}, are the inductance, the output voltage, and the input voltage.

From (eq. 3.5) and (eq. 3.6) it can be concluded that higher ripple occurs with higher input voltage and increase in the current limit, both of which are desired in order to supply higher load currents and higher output voltage. The droop below the lower limit of the hysteresis V_{droop} does not have a concise expression for multi-pulse operation, for single-pulse operation, it is simply $T_{on} I_{load} / C_{out}$.

3.1.1 Fundamental Limitations of PFM control

The linear slope approximations (eq.3.2-eq.3.3) can be used to quickly provide insights of fundamental limitations of the PFM control. An example is the derivation of theoretical maximum conversion ratio and its relationships with other design parameters.

During single pulse operation, the conversion ratio limit is determined by how much charge can be boosted within a single pulse and if it is sufficient to supply the target load. A mathematical expression can be derived by the following equations:

$$I_{\text{load}} \leq \frac{Q_{\text{boost}}}{T_{\text{cycle}}} = \frac{Q_{\text{boost}}}{(T_{\text{on}} + T_{\text{boost}} + T_{\text{idle}})} \tag{3.7}$$

$$Q_{\text{boost}} = \frac{I_{\text{peak}} T_{\text{boost}}}{2} = \frac{(T_{\text{on}} m_{\text{pos}})^2}{2 m_{\text{neg}}} \tag{3.8}$$

Because T_{on} and T_{boost} are both non-zero values, the minimum-period cycle occurs when T_{idle}=0, that is, when the idle time is exhausted by the load current. Thus, the follow-

ing equation can be derived:

$$V_{\text{in}} \geq \sqrt{\frac{2V_{\text{out}}I_{\text{load}}L}{T_{\text{osc}}D}} \tag{3.9}$$

We can observe that the duty cycle poses a lower limit to the input voltage when we wish to supply a load current at a specified output voltage with single pulse operation.

Substituting (eq. 3.2) into (eq. 3.1) we can come to the following equation (eq. 3.10), which poses a second limit to the conversion ratio during multi-pulse operation.

$$D \geq (V_{\text{out}} - V_{\text{in}})/V_{\text{out}} \tag{3.10}$$

In addition to limitations of the duty cycle, the design of the oscillator also includes determining the frequency at which the oscillator would operate. However, the design of the frequency is highly associated with determining the value of the inductance. An implication of the correlation can be observed in (3.9) at fixed input and output conditions. To further explain the relationship, the effect of change in inductance at fixed frequency is shown in Fig.3.4.

Fig.3.4 shows possible outcomes of decreasing inductance in a PFM boost regulator.

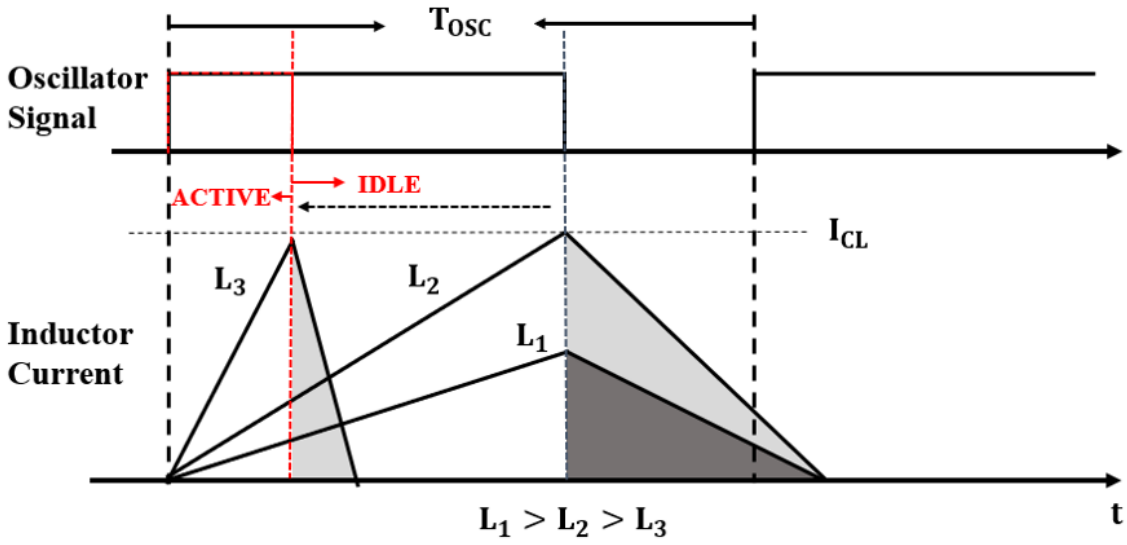


Figure 3.4: Effect of Inductance.

Revisiting equations (3.2) and (3.3), decrease in inductance would increase the slope of the inductor current at fixed input/output voltage. A decrease in inductance will increase the current ripple when all other factors remain constant. The shaded area in Fig.3.4 indicates the charge that can be boosted to the output (Q_{boost}).

For a single pulse, the charge boosted increases with a slight decrease in inductance from L_1 to L_2. For multi-pulse operation, this would result in frequent exceeding of the current limit. In both cases, larger output voltage ripples can be observed due to higher peak current. The functionality of the regulator is maintained with a decrease in supply voltage quality.

Further decrease in inductance from L_2 to L_3 when an inductor current limit is applied will decrease the charge boosted. The current build-up behaviour observed in typical multi-pulse operation becomes restricted and converges to multiple single-pulse current packets. Not only is the benefit of increasing potential to supply higher load with multi-pulse operation lost, the maximum load that can be supplied is also reduced. Under the same conversion ratio and oscillator frequency, the maximum amount of charge that can be supplied to the output is limited by the inductor current pulse. It can thus be derived with the following equations:

$$Q_{\text{boost}} = \frac{I_{\text{peak}} T_{\text{boost}}}{2} = \frac{{I_{\text{CL}}}^2 L}{2(V_{\text{out}} - V_{\text{in}})} \tag{3.11}$$

$$I_{\text{load}} \leq I_{\text{avg}} = \frac{Q_{\text{boost}}}{T_{\text{osc}}} \tag{3.12}$$

This places a theoretical upper limit to the load current at which regulation is feasible. In order to increase the ability to supply higher load currents at a smaller inductance, one can either decrease the IDLE time due to the early reach of the current limit to increase the average current or seek to re-establish multi-pulse operation. In both cases, an increase in oscillator frequency is necessary [4].

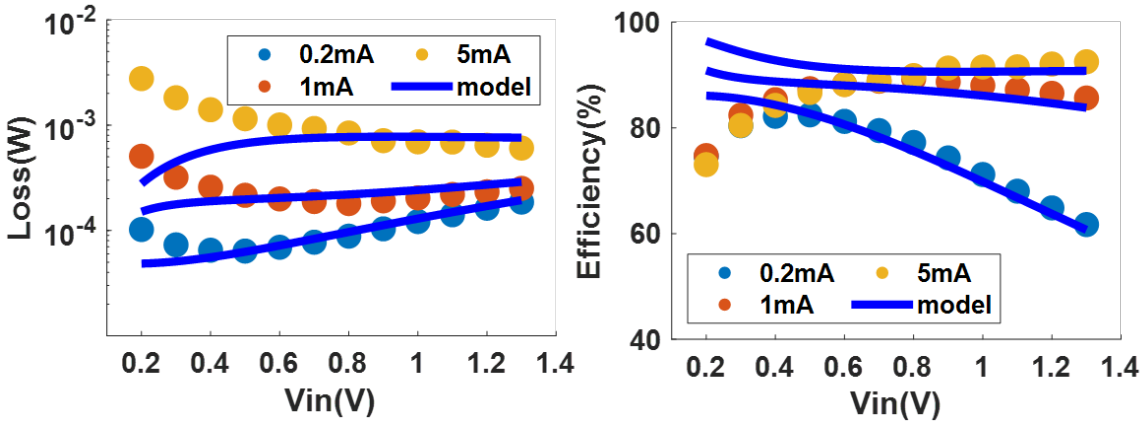


Figure 3.5: Simulated loss and efficiency compared with single pulse model results. Output voltage is set to be 1.5V for different Vin (x-axis) and load current (colored dots) pairs.

3.2 Analytical Model Development

PFM boost regulators use simple, low power control that directly modulates the inductor current based on pre-designed thresholds. However, the modeling of PFM operation is not as straightforward. Depending on operation conditions (input voltage, output voltage, load current, etc.) and design components (inductor value, capacitor value, oscillator frequency, etc.) transient behavior of PFM-BR can vary greatly making compact modeling of power loss challenging. Fortunately, the effect of variations in the design space can be traced by investigating their effect on changing the inductor current waveform and the transient behavior of feedback control loop.

3.2.1 Prior Work - Single-Pulse Model

Analytical loss models for single-pulse operation have been proposed [29]. The model can be used to evaluate conversion efficiency by computing loss factors (conduction loss, switching loss, and bias power) individually based on the derived peak current of the inductor. However, comparison with transistor-level simulations show under-estimation of loss at lower input voltage when multi-pulse operations are entered (Fig. 3.5). This is because the inductor current behaviour for multi-pulse operation is dependent of multiple factors

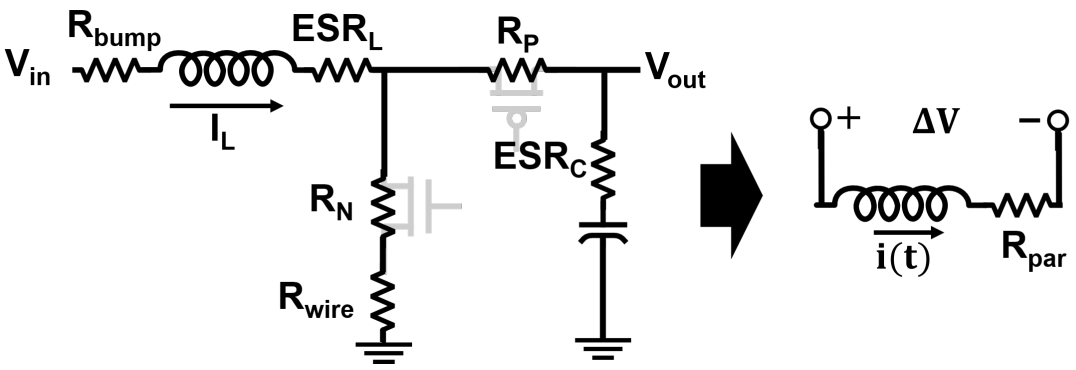


Figure 3.6: Inductor current with parasitic resistance from power stage/wire/bump etc.

and can no longer be approximated with triangular current pulses for single-pulse. Hence, a different approach for modeling loss is necessary to allow wide conversion ranges that cover both single and multi-pulse operations.

3.2.2 Charge-equilibrium Based Model

To address the loss in accuracy in single-pulse models, we have constructed a loss-model framework by computing and tracking inductor current behavior under design parameter variations. The model constructed in this section is based on charge equilibrium equations and includes non-ideal parasitic resistances (Fig. 3.6) when modeling inductor current behavior to increase the accuracy of the model. The effect of parasitic resistance is increasingly critical when the source voltage is low and size of power switches are limited to drive low output load. Switch resistances should be considered depending on the state of the switches as shown in the following equations [48].

When the NFET switch is ON and PFET switch is OFF (Charging phase):

$$V_{\text{in}} - i(t)R_{\text{charge}} = L\frac{di(t)}{dt} \tag{3.13}$$

When the NFET switch is OFF and PFET switch is ON (Boosting phase):

$$V_{\text{in}} - V_{\text{out}} - i(t)R_{\text{boost}} = L\frac{di(t)}{dt} \tag{3.14}$$

R_{charge} and R_{boost} indicate the parasitic resistances along the charging and boosting path, respectively. Assuming the schematic shown in Fig. 3.6, they can be computed as:

$$R_{\text{charge}} = R_{bump} + ESR_L + R_N + R_{wire} \tag{3.15}$$

$$R_{\text{boost}} = R_{bump} + ESR_L + R_P + ESR_C \tag{3.16}$$

These resistances pose an additional limit to the maximum inductor current i_{max} as shown in (3.17), when the voltage across the switch is equal to the input voltage and there can no longer be an increase in inductor current.

$$i_{\text{max}} = \frac{V_{\text{in}}}{R_{\text{charge}}} \tag{3.17}$$

Based on Fig. 3.6 and combining all parasitic resistances, the inductor current can be generalized to:

$$i(t) = \frac{\Delta V}{R_{\text{par}}} + (i_0 - \frac{\Delta V}{R_{\text{par}}})e^{-\frac{t}{\tau}} \tag{3.18}$$

where i_0 is the starting current, which is non-zero during multi-pulse operation; τ is the time constant L/R_{par}; i(t) is the inductor current; ΔV is the voltage across the inductor and the parasitic resistance; and R_{par} represents the sum of all parasitic resistances. As explained previously, the value of R_{par} will need to be replaced when modeling different phases of IVR operation, depending on the state of the power switches (i.e. charging/boosting current path) and different values will need to be applied during transient modeling accordingly.

It can then be derived without loss of generality that the change in inductor current over a time period is:

$$i_{\text{step}}(t) = (\frac{\Delta V}{R_{\text{par}}} - i_0)(1 - e^{-\frac{t}{\tau}}) \tag{3.19}$$

The total charge that flows through the inductor during a specific time period is:

$$Q_{\text{step}}(t) = \frac{\Delta V}{R_{\text{par}}} t - (\frac{\Delta V}{R_{\text{par}}} - i_0)(\frac{L}{R_{\text{par}}})(1 - e^{-\frac{t}{\tau}}) \tag{3.20}$$

The time for the inductor current to reach a certain value can be approximated with:

$$\Delta T(i_0, I_{\text{end}}) = \frac{(I_{\text{end}} - i_0)L}{\Delta V - (I_{\text{end}} + i_0)R_{\text{par}}/2} \tag{3.21}$$

It can be proven that these equations converge to their linear-slope counterparts when R_{par} is negligible. Using these equations, the operation of a PFM boost regulator is simplified into identifying the inductor current behavior in the active and idle phases of one regulation cycle. The active (boosting) phase of the cycle is defined by the period of time for a number of pulses to boost a total amount of charge equal to the hysteresis difference in addition to the charge consumed by load current:

$$\sum_{n=1}^{k} Q_{\text{boost,k}} \geq C_{\text{out}} V_{\text{hyst}} + \int_0^{kT_{\text{osc}}} I_{\text{load}} dt \tag{3.22}$$

This phase can also be segmented into multiple sub-"packets" if the inductor current falls back to zero before the equation 3.22 is met (usually after surpassing I_{CL} early during ON time of OSC):

$$\sum_{n=1}^{m} I_{\text{step,m}} \leq 0, m \leq k \tag{3.23}$$

The idle phase is simply the time taken for the load current to discharge hysteresis voltage in the output capacitor.

With these constraints for identifying high-level cycles and sub-packets of charge boosting known, the remainder of the model is built upon multiple check statements that mimic the operation of the CLC, OSC and ZC. A flow diagram for the model is as shown in Fig. 3.7. The computation begins with an initial current of zero and checks conditions for equation (3.22) and (3.23) while inductor current change is derived and tracked in a

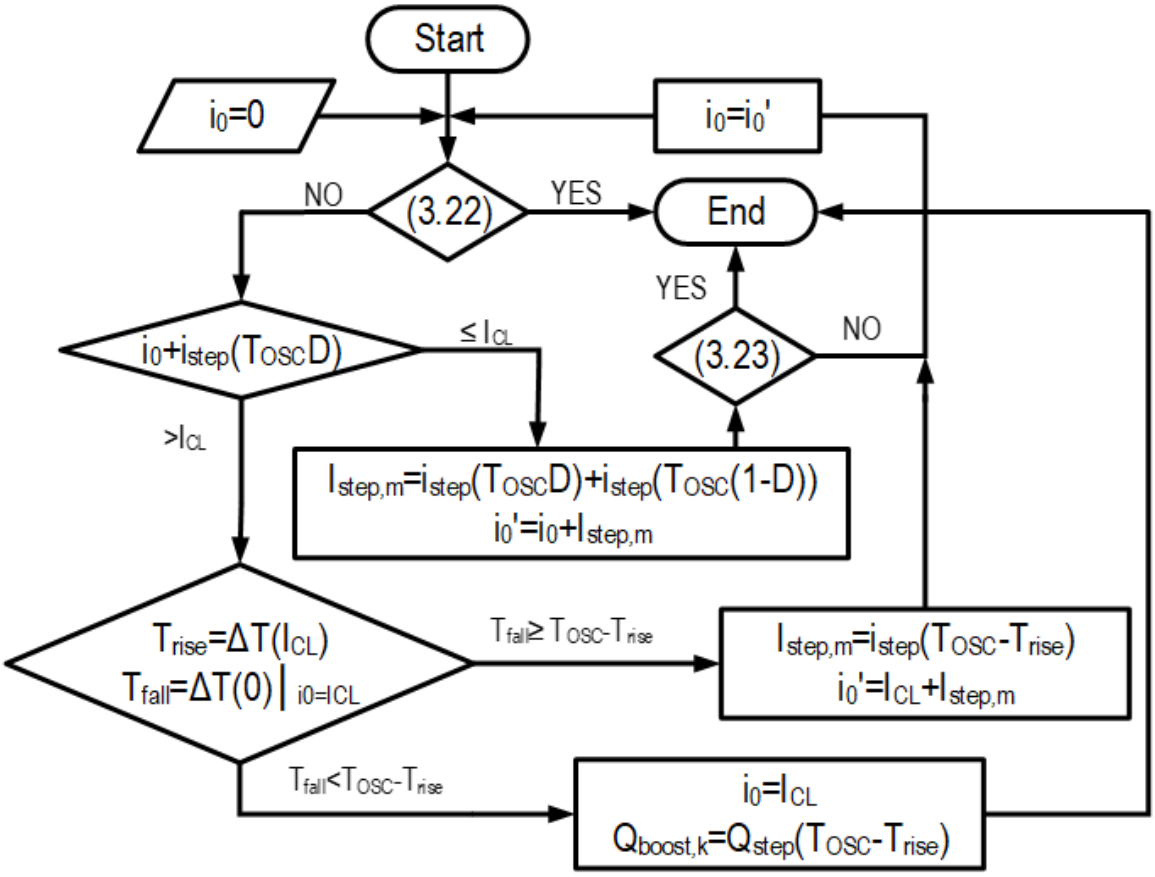


Figure 3.7: Flow diagram for performing inductor current transient modeling.

recursive manner.

For each loop, the step increase in current during the charging phase (low-side NFET ON, high-side PFET OFF) is summed with the initial current and then compared to the current limit (I_{CL}). This criteria models an ideal current limit comparator behavior. If the current limit is reached, the inductor current step in this oscillator cycle is recomputed and checked if a zero current is resulted from the boosting phase (low-side NFET OFF, high-side PFET ON). This models zero current comparator behavior when boosting starts earlier within an OSC period after hitting I_{CL}. The loop continues until the constraints are met. The current behaviour is logged and used for loss computation with the loss model explained in the following subsection.

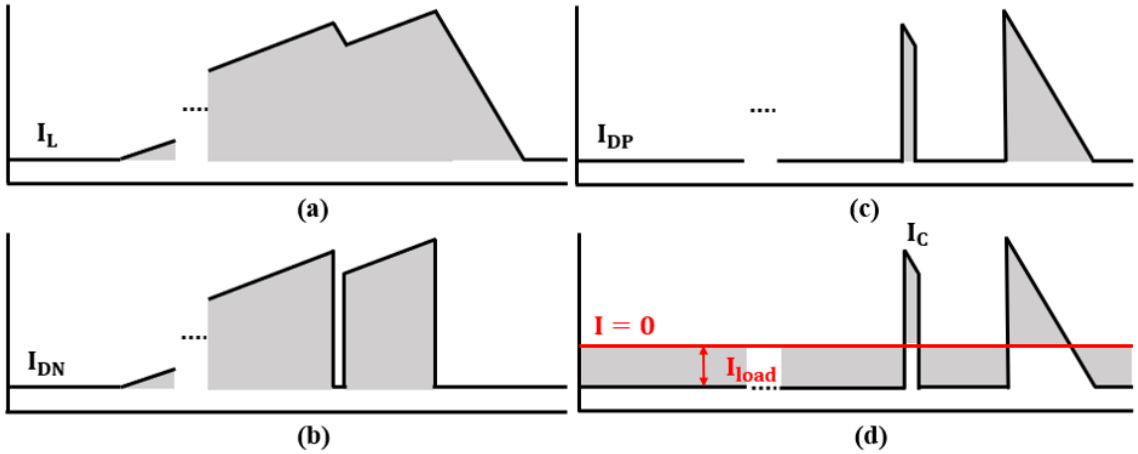


Figure 3.8: Conduction loss from (a) inductor current (b) NFET drain current (c) PFET drain current, (d) current to capacitor.

3.2.3 Loss Components Modeled

The tracked inductor current within a regulation period is used to compute the contribution of the following loss factors: conduction loss, switching loss, and control power [48].

Conduction Loss

Conduction loss is due to resistive loss when current flows through components and is converted into heat dissipation. Therefore, it is also often referred to as I^2R loss. Similar to the phase-dependent computation of inductor current, conduction loss is calculated by first determining the contribution of each component depending on the phase of switching and applying eq. 3.18. The current waveforms of the components that contribute most to conduction loss along the EDS path are shown in Fig. 3.8, where the shaded areas indicate when conduction loss is present. Dead-time designed in driver stages to prevent reverse current can also be modeled as increased resistance in the PFET. Fig. 3.9 shows the voltage and parasitic resistance for power gates used during the boosting phase. Using these parameters, the I^2R loss are estimated using a squared then integrated version of equation

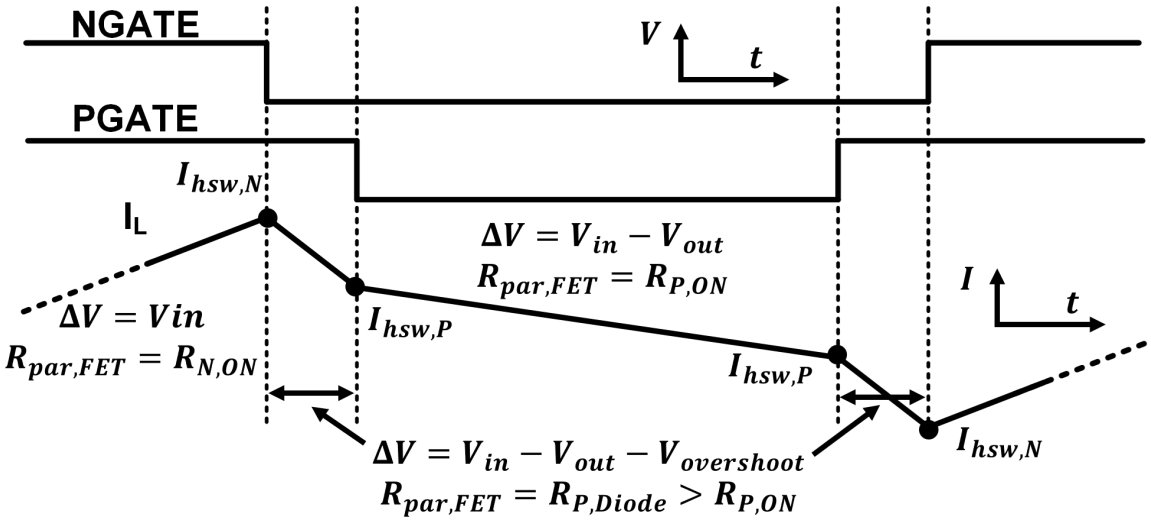


Figure 3.9: Inductor current behavior and parameters used for calculation.

(3.18) and added across loops shown in Fig. 3.7:

$$\int I^2{}_{\text{step}}(t) = (\frac{\Delta V}{R_{\text{par}}})^2 t - (\frac{\Delta V}{R_{\text{par}}} - i_0)(\frac{4\Delta V}{R_{\text{par}}} + (i_0 - \frac{\Delta V}{R_{\text{par}}})(1+e^{-\frac{t}{\tau}}))(\frac{L}{2R_{\text{par}}})(1-e^{-\frac{t}{\tau}}) \quad (3.24)$$

Conduction loss is mostly load dependent, which is quite intuitive as the demanded load should be the average of the current that flows through the PFET power switch. There is also a dependence on conversion ratio. A decrease in input voltage results in a decrease in inductor current rising slope and an increase in the falling slope. This increases the ratio between the charge passed to ground during the inductor charging phase and the charge passed to output during the boosting phase, which essentially represents more energy dissipated while building inductor current for a given output load.

This effect is illustrated in Fig.3.10 (a), where inductor current is plotted with two different input voltages V_1 and V_2 ($V_1 > V_2$) under fixed output voltage and charging time. The shaded area indicates the charge boosted to the output. Model results using eq. 3.18 are plotted in Fig.3.10 (b), where we can observe the dependence on load current and input voltage. The legends indicate the level of load current applied to the model. The output

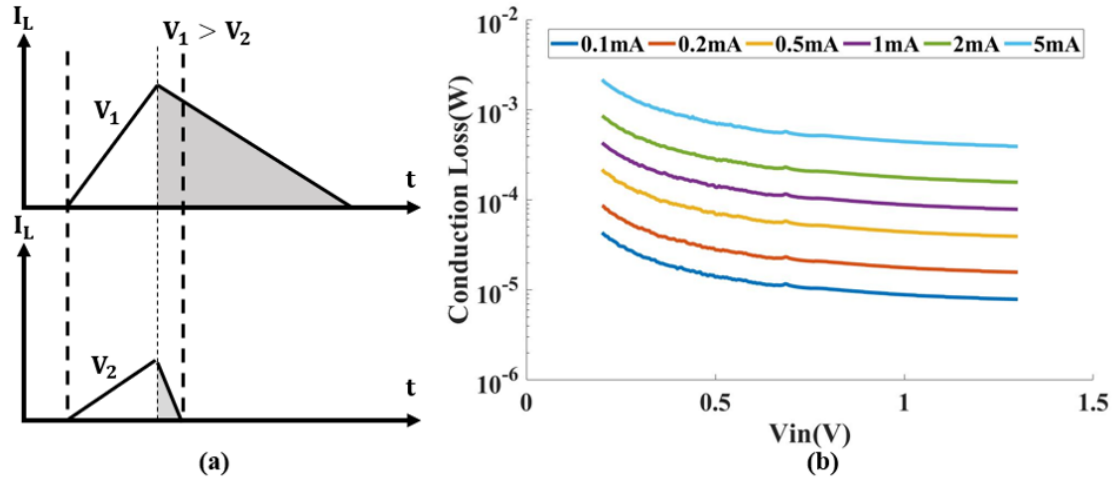


Figure 3.10: (a) Effect of input voltage (b) Conduction loss obtained from model.

voltage is set to be 1.5V.

Switching Loss

Fig. 3.11 shows the components that contribute to switching loss that is considered in the model. We compute switching energy required to drive gates of the power MOSFETS (incurred at the gate drivers, Fig. 3.11(a)) in an occurrence based manner. This allows for a simple method to model variations when changing oscillator frequency. The energy consumed for a single switching event is obtained and the total contribution of switching energy is obtained by tracking the total number of switching incidents during a regulation cycle.

Finite switching time of power MOSFETs also results in loss. Hard switching loss can occur when power switches change states at non-zero current, as shown in Fig. 3.11(b). This scenario occurs much more frequently in the multi-pulse operation compared to the single-pulse operation. The model sums current values across a regulation cycle depending on the direction of switching to take into account multiple switching events with non-zero drain currents to compute switching loss [48]. The currents accounted for NFET and PFET hard switching loss are annotated as $I_{hsw,\,N}$ and $I_{hsw,P}$ in Fig. 3.9. A hard switching

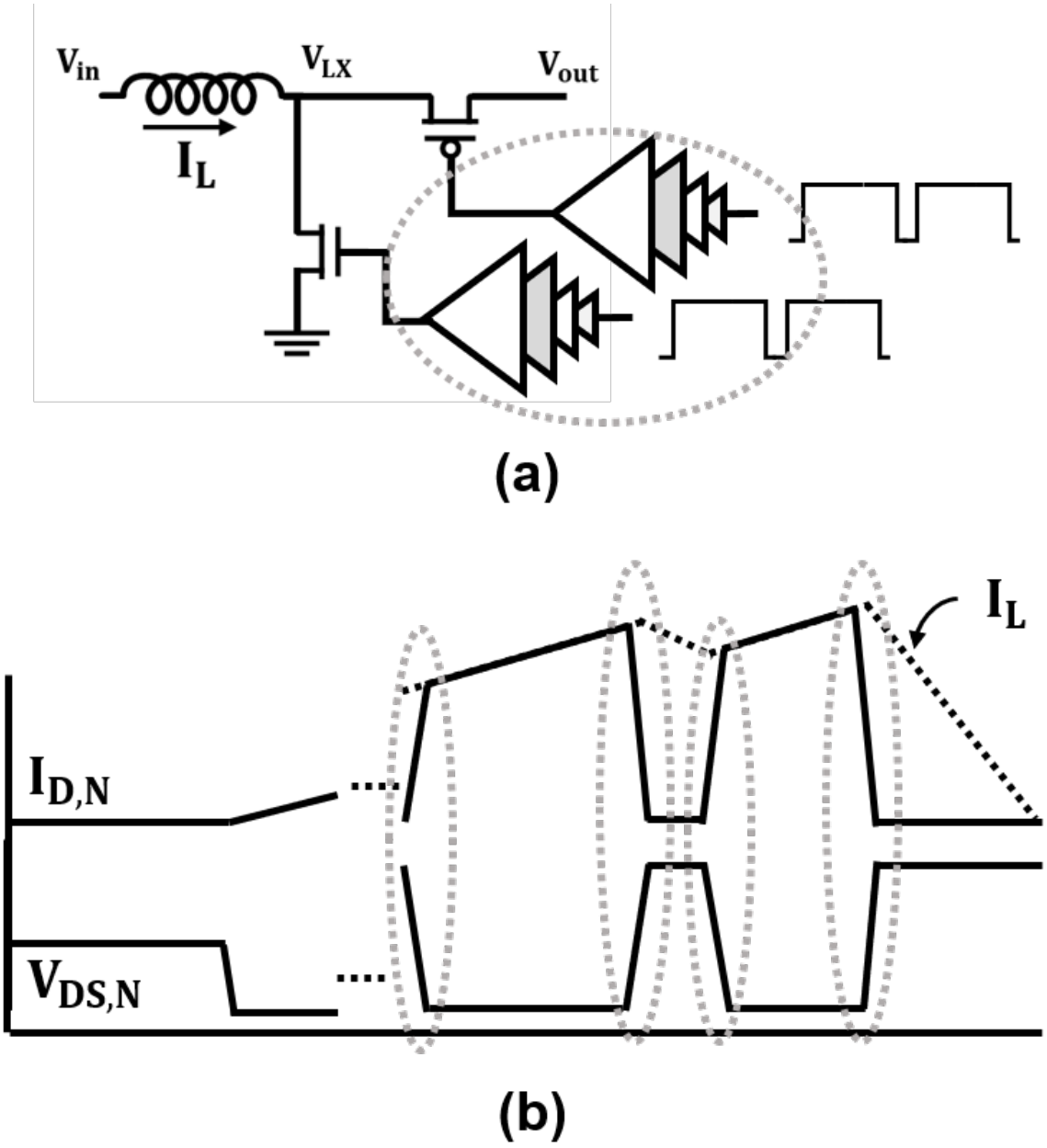


Figure 3.11: Switching loss occurrences included in the loss model (a) gate-drive losses (b) hard-switching loss .

loss model is adapted from [49] to fit the multi-pulse PFM operation with the following equations:

$$P_{\text{sw,off}} = (\Sigma I_{\text{off}})(\frac{V_{\text{os}}}{12} + V_{\text{DS}})\frac{T_{\text{sw}}}{T_{\text{per}}} \tag{3.25}$$

$$P_{\text{sw,on}} = (\Sigma I_{\text{on}}) \frac{V_{\text{DS}} T_{\text{sw}}}{6 T_{\text{per}}} \tag{3.26}$$

The currents are summed across a regulation cycle depending on the direction of switching to take into account multiple switching events with non-zero drain currents in multi-pulse operation.

$$P_{\text{sw,tot}} = \Sigma (P_{\text{sw,on}} + P_{\text{sw,off}})_{\text{N.P}} \tag{3.27}$$

Control Power

Control power is due to the analog comparators and necessary biasing reference circuits that consume static power to operate. Power overhead of the control circuits are also considered in the model by extracting from measurement/simulation data. The active power (P_{active}) and idle power (P_{idle}) are assigned based on the state of functional blocks in each phase.

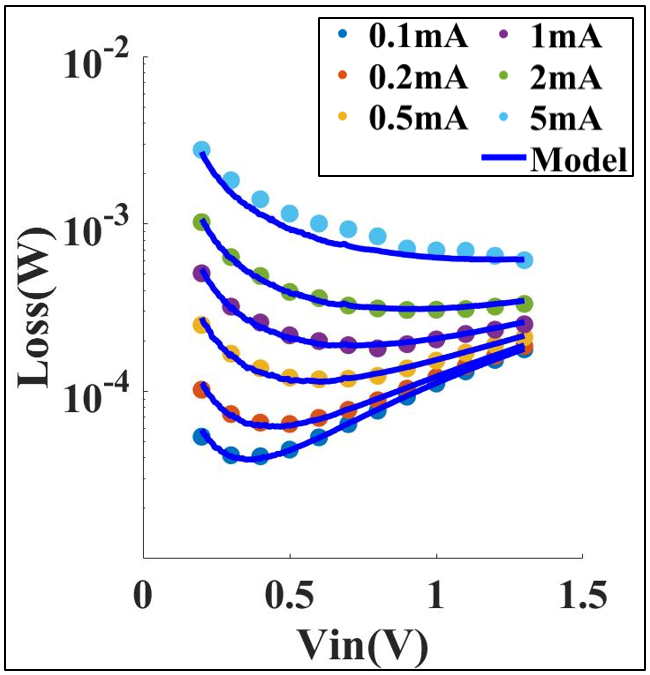
$$P_{\text{bias,tot}} = \Sigma (P_{\text{active}} + P_{\text{idle}})_{\text{blocks}} \tag{3.28}$$

3.3 Model Results and Validation

To verify the accuracy of the model, the model is compared to data acquired from transient simulations for both DC-DC conversion and harvesting scenarios. The first test validates the ability of the model to capture changes in loss under load current and conversion ratio variations and is compared against both simulation and silicon data. The second test serves as a preliminary validation of whether the model can be used for system-level optimization when input power also becomes dependent on the converter operation and involves multiple steps that will be explained in the following.

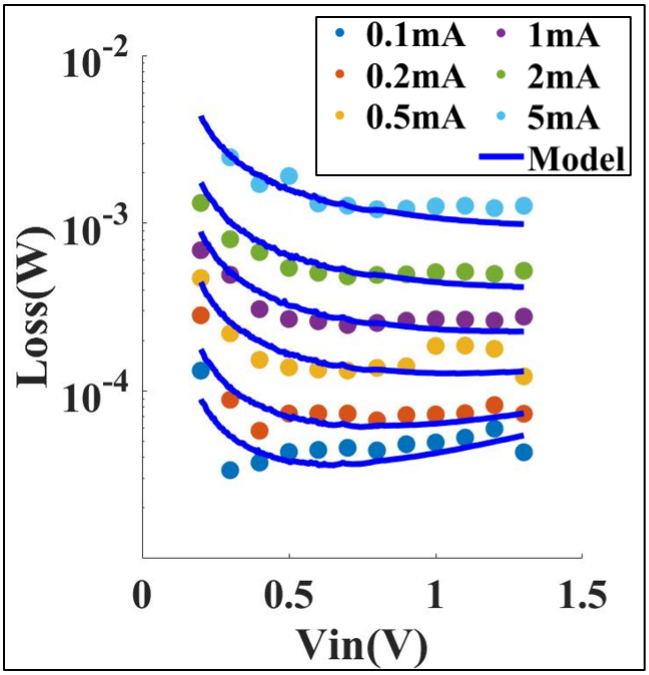
3.3.1 DC-DC conversion

For the first test of comparing DC-DC conversion modeling accuracy, the model is implemented in MATLAB to allow for accelerated result evaluation. Fig. 3.12 shows the model results compared with Spectre simulated data. The effect of the damping resistor (R_{LX} shown in Fig. 3.2) added during Spectre simulations to increase simulation speed is also modeled. Overall, the model results have less than 6% difference in loss estimations when compared to simulation data with load current in the range of 0.1 mA - 2 mA. The loss calculated can then be used to derive the efficiency of power transfer to the load. The difference in loss accounts for less than 1.2% efficiency difference. By using the charge equilibrium model, only one simulation is required for initial calibration of parameters such as current limit (I_{CL}), parasitic resistance ($R_{P,ON}$,$R_{N,ON}$), etc. Because the model run time is negligible compared to circuit simulations, this signifies as 72x reduction in simulation time for this particular experiment. The larger the exploration space, the higher the benefit.



Param.	Value
V_{out}	1.5 V
T_{on}	9.46 µs
T_{off}	0.46 µs
I_{CL}	95 mA
$R_{P,ON}$	0.8 Ω
$R_{N,ON}$	0.35 Ω
R_{LX}	50 kΩ
$R_{esr,Cout}$	0 Ω
$R_{esr,L}$	0 Ω
I_{CL}	95 mA

Figure 3.12: Loss results of PFM regulator obtained from model compared with Spectre simulations



Param.	Value
V_{out}	1.5 V
T_{on}	9.46 µs
T_{off}	0.46 µs
I_{CL}	95 mA
$R_{P,ON}$	0.9 Ω
$R_{N,ON}$	0.4 Ω
R_{LX}	N/A
$R_{esr,Cout}$	0.45 Ω
$R_{esr,L}$	0.24 Ω
I_{CL}	95 mA

Figure 3.13: Loss results of PFM regulator obtained from model compared with silicon measurements

While marginal differences in loss are still existent, the accuracy is sufficient to be used as a fast-exploration tool that provides a practical estimation of the total loss of the PMU during design and analysis.

Fig.3.13 shows the model comparison with measurement data from a 130nm CMOS test-chip with the parameters used as shown in the table. The ESR of the inductor and capacitor are included in this case, and socket/board resistances are included into $R_{N,ON}$ and $R_{P,ON}$. The details of the test-chip have been reported in prior publications[47].

3.3.2 EHDS System-level optimization

The second experiment for EHDS system-level optimization accuracy is organized as explained in the following. A simplified schematic indicating power transfer dependencies for a typical EHDS as illustrated in Fig. 3.1 is shown in Fig.3.14. As the EHDS supply capability directly reflects on the target load operation frequency and duty cycle, the ultimate goal is to minimize EHDS overhead while providing maximum output power. On top of

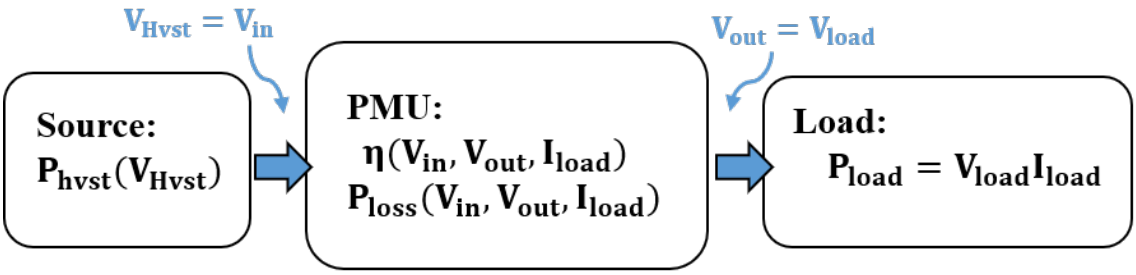


Figure 3.14: Power delivery path and interfaces between each stage for a typical EHDS supplying target load.

conventional approaches to increase power conversion efficiency and/or harvested power, another design objective to increase system output power is to manage the interfacing between harvesting sources and IVR during EHDS integration.

Conventional harvesting source maximum power point (source-MPP) tracking methods focus on the interface between the harvesting source and the PMU. The PMU operation is controlled to ensure its input voltage (which is also the harvesting voltage) is maintained at a point at which maximum power can be harvested by the source. However, because the harvested power from transducer sources is highly dependent on environmental settings and operating conditions, this source-MPP does not often correspond to the input voltage that allows maximum power transfer efficiency for the PMU. during EHDS integration. Arising from this discrepancy is a possible degradation of overall system power transfer from a theoretical maximum.

The following experiment will investigate potential gain in output power that can be obtained by selecting different harvesting voltages as opposed to conventional source-MPP. Experiment results based on the aforementioned model are compared to Spectre simulation data to validate usage of the model for system analysis.

Impact of MPPT

To understand the purpose of the experiment, it is crucial to acknowledge differences in EHDS operation compared to DC-DC conversion first. The addition of an MPPT control

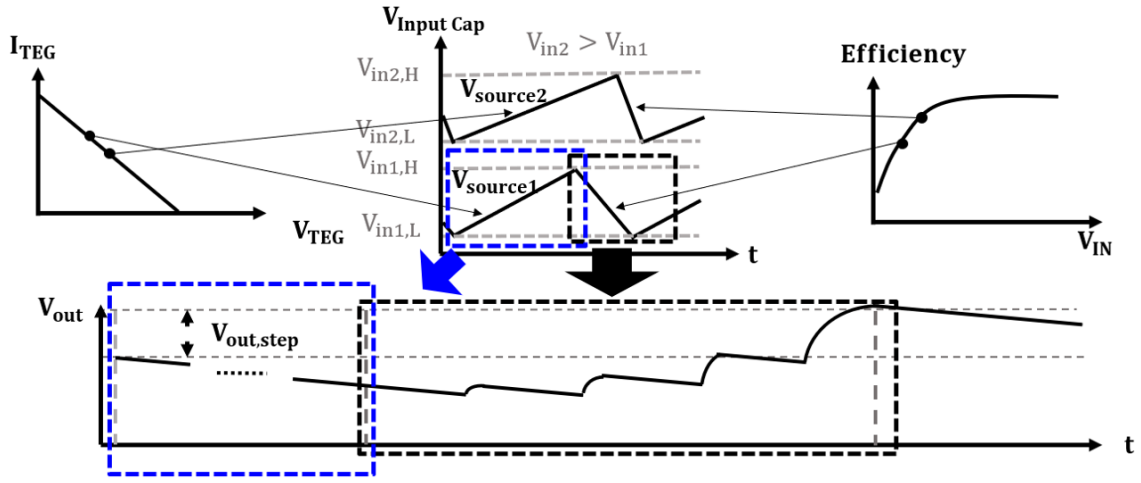


Figure 3.15: Input hysteresis at different voltages and step-wise increase in output due to input hysteresis.

circuit not only modulates harvesting voltage, but the act of shifting regulation priority from the PMU output to its input also changes the behavior of the PMU when input resources (capacitance, transduced power) are limited. A direct change that results from this is that the effect of load current during DC-DC conversion becomes decoupled during EHDS power delivery. For a PFM-BR, increase in load current increases output ripple and active time, but decreases idle periods. However, MPPT does not consider load variations while modulating the PMU to ensure harvesting voltage is controlled for maximum source power.

In an implementation of MPPT, after the MPP is located based on methods explained in Chapter 2, hysteresis voltage control is applied to the harvesting node to ensure that the source is biased at its MPP to maximize the harvesting efficiency. This hysteresis control at the IVR input capacitor will limit the transfer of energy that is supplied to the output and the operation of regulation becomes segmented and the output voltage increases with similar voltage steps for each input hysteresis cycle[20]. A sample waveform of the output voltage is shown at the bottom of Fig.3.15. An overall voltage increase of $V_{out,step}$ can be observed if the power transferred is larger than the load power.

Fig.3.15 also shows how different levels of input hysteresis can affect the process of power transfer. A higher input voltage(indicated by V_{in2}) results in the following variations:

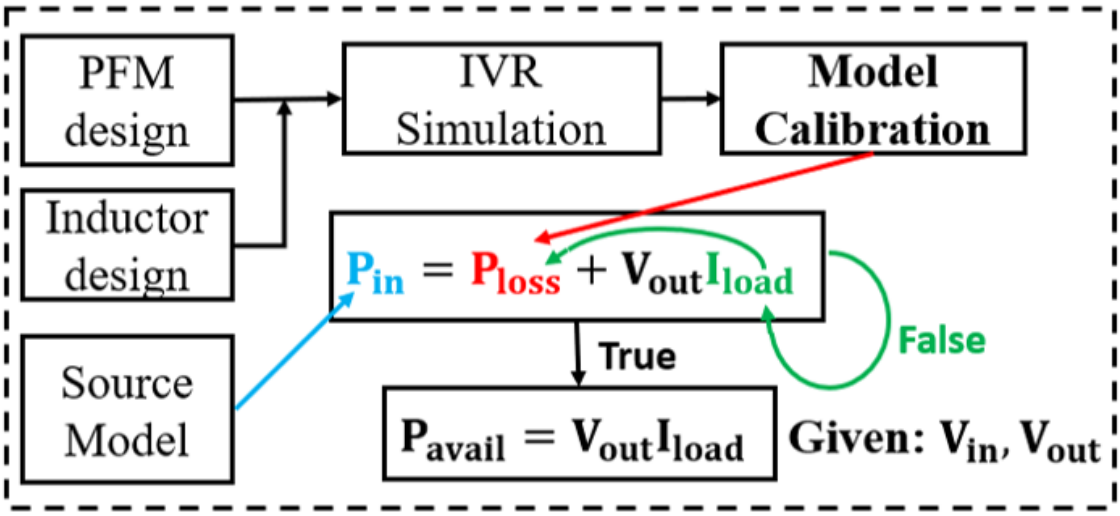


Figure 3.16: Computing available output power

(i) A lower harvesting current, (ii) increase in the efficiency of conversion, (iii) decrease in discharging time of the input capacitor, (iv) higher input hysteresis energy. The input hysteresis energy ($E_{in,hyst}$) can be approximated as in (eq. 3.29). Where $V_{in,H}$, $V_{in,L}$, and C_{in} are input hysteresis higher limit, input hysteresis lower limit and input capacitance:

$$E_{\text{in,hyst}} \approx \frac{(V_{\text{in,H}}{}^2 - V_{\text{in,L}}{}^2)C_{\text{in}}}{2} \tag{3.29}$$

While DC-DC conversion efficiency can be obtained through the aforementioned model, the derived metric from DC-DC conversion can not be directly used to derive maximum output power for EHDSs due to the change in operating characteristics. To resolve this inconsistency, we implement an iterative search with conversion loss estimations at different loads to find the maximum supply-able load possible.

Derivation of Maximum Available Output Power

Knowing that IVR loss increases with load current demand, the available output power at a specific harvesting voltage can be derived to be when the source power equals the sum of the output power and the loss. If a source voltage can provide higher power than the sum

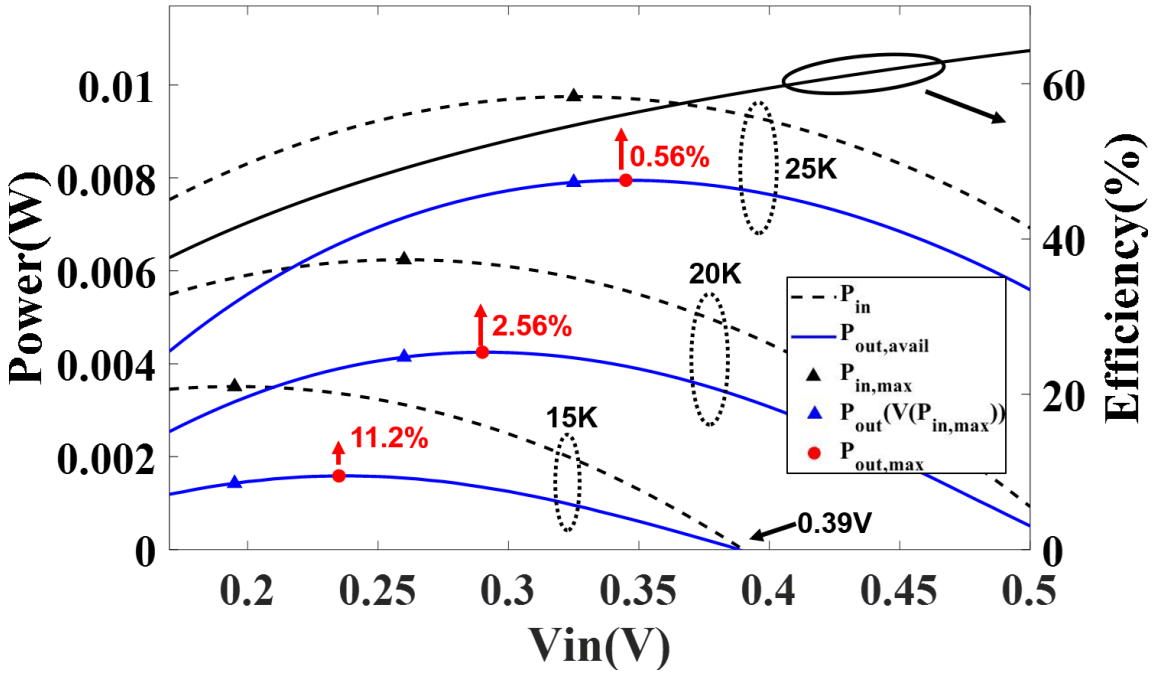


Figure 3.17: TEG source power and available system output power at 15 K, 20 K, 25 K temperature difference. ($V_{\text{OC}} = 0.39V, I_{\text{SC}} = 36mA@\Delta T = 15K$)

of the loss and the output power, we know that higher load can be supplied and available output power has not yet been reached.

This procedure is illustrated in Fig.3.16 and is performed across the range of input voltage to track the maximum available output power. The loss model is calibrated with simulated data and used to monitor load dependence of IVR loss to evaluate maximum available power. Unless the source MPP falls on the point of maximum efficiency for the converter, a shift from the maximum available power can be observed. The difference in output power that can be gained in theory by this shift in harvesting voltage depends on both source and converter characteristics.

TEG Harvesting Model Results

Fig. 3.17 shows simulated results of modeling output power of a EHDS when using a Thermo-electric Generator (TEG) as the harvesting source. The TEG source model param-

Table 3.1: Effect of System-MPPT on Harvesting Voltage and Maximum Output Power

Temperature difference applied to TEG source				
ΔT (K)	15	20	25	30
Harvesting voltage at MPPT point				
Source-MPPT (mV)	195	260	325	390
System-MPPT (mV)	235	285	345	405
ΔV(mV)	40	25	20	15
Potential Output power increase				
Power increase	11.2%	2.56%	0.56%	0.15%

eters are extracted from a commercial product [17]. In Fig. 3.17, the dashed black lines indicate the TEG source power at 5 K, 10 K and 15 K temperature difference. The solid black line shows the IVR efficiency at fixed 2mA load current. The solid blue lines show the available output power from EHDS by applying the proposed approach. The black triangles show the maximum input power drawn from the TEG source ($P_{in,max}$, typically @ $VOC/2$ for TEG sources). The blue triangles show the output power at the point of Source-MPPT ($P_{out}(V(P_{in,max}))$). And the red dots show the maximum available output power.

We can observe a shift between the last two points for all temperature differences. Which indicates that instead of harvesting at the input MPP, a slight increase in harvesting voltage can result in higher output power. Labels indicate power increase from source MPP to maximum available power. As the converter's efficiency is more sensitive to conversion ratio at low input voltages, the maximum advantage of System-MPPT is observed for small temperature differences where the input voltages are low (Table 3.1).

TEG harvesting Transient simulation

Because the harvesting voltage is now a variable that is dependent on MPPT decisions, we can no longer use the $V_{OC}/2$ FOCV method that is commonly implemented for TEG harvesting. Instead, the following experiment implements a time-based MPPT (TB-MPPT)

approach similar to prior work published by Liu et. al. [20] and targets to find a harvesting voltage that minimizes ACTIVE boosting periods, which has been proven to be used as a metric that indicates increase/decrease in output power under fixed load.

Fig. 3.18 shows a schematic of the simulation testbench for testing the TB-MPPT algorithm. Three Verilog-A blocks are added to transistor level designs for a PFM boost regulator to realize the high-level schematic for system-focused MPPT shown in Fig. 2.2. These blocks include an ideal TEG source model with linear I/V characteristics [17], and ideal hysteresis comparator for input (harvesting) voltage control, and a time-based MPPT (TBMPPT) block that attempts to minimize ACTIVE time (T_{ACTIVE}) with a similar approach as [20].

The verilog-A TBMPPT model implements a simple Perturb and Observe (P&O) algorithm that works as such: after a step increase (or decrease) is applied to the reference voltage, compare the current T_{ACTIVE} value to a stored minimum value from previous cycles. If T_{ACTIVE} is lower, then a step in reference voltage in the same direction is taken. Otherwise, a step in the opposite direction is taken. When a local maximum is reached, the reference voltage will oscillate around this MPP.

Two transmission gates are added to direct the harvested energy either through the

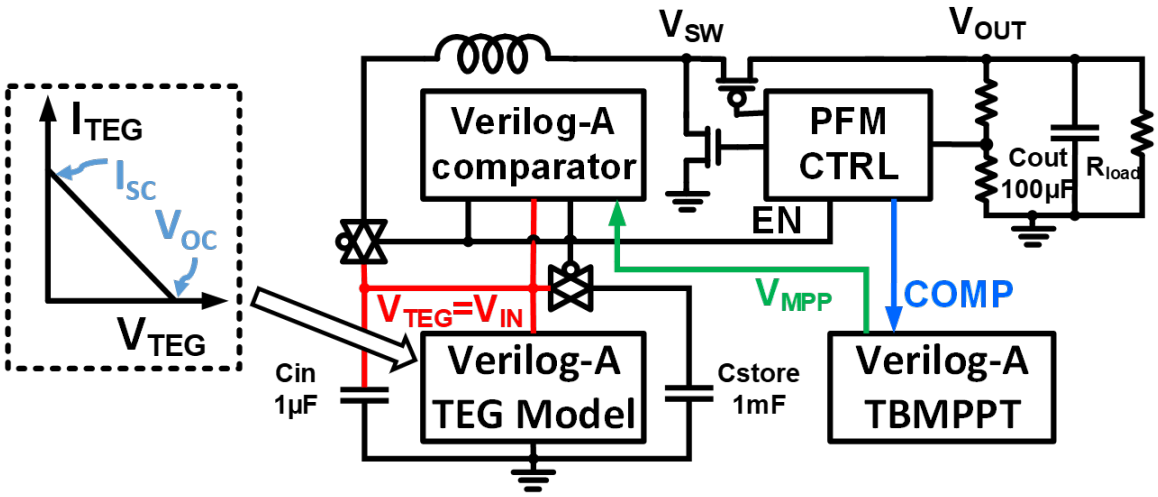


Figure 3.18: Schematic for transient TB-MPPT tracking

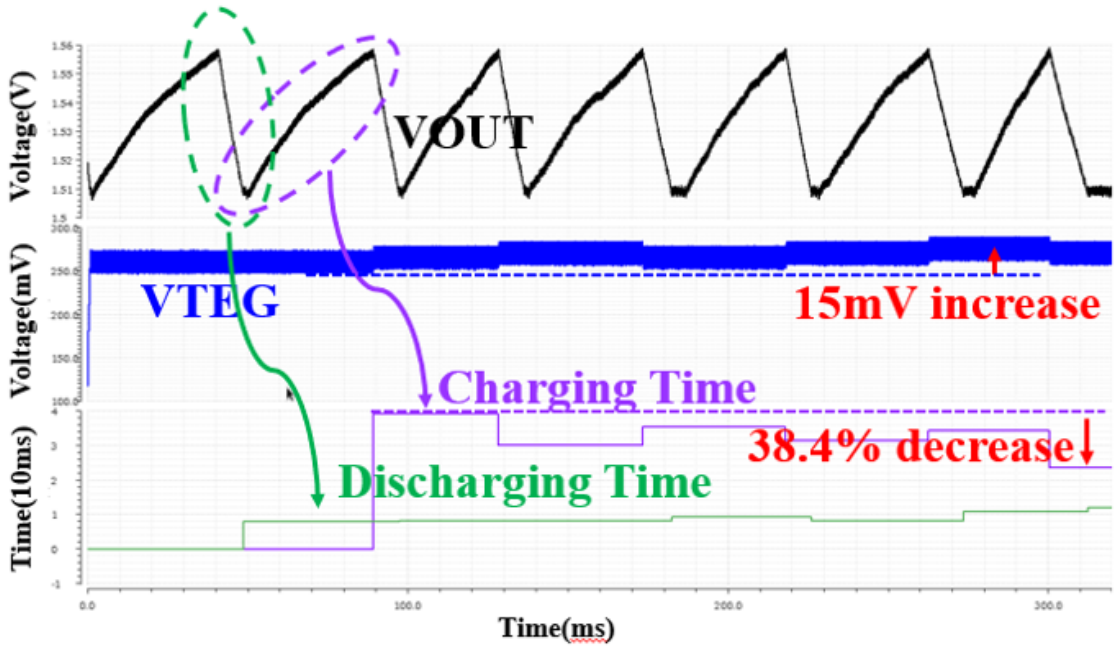


Figure 3.19: Simulation results of Time-based System-MPPT (TEG@ΔT=20)

boosting path or to a temporary storage capacitor (Cstore) during falling periods of the IVR output regulation. The secondary storage uses a large capacitor initially set at low voltage to ensure that the TEG energy can be regulated at V_{MPP} when IVR output is falling. This ensures that SF-MPPT analysis along the single boosting path is unbiased during transient analysis.

Fig. 3.19 shows simulation results of the proposed output-power estimation method and System-MPPT with the testbench. The simulation assumes an input temperature difference of 20 K ($V_{OC} = 0.52V, I_{SC} = 48mA@\Delta T = 20K$), and the simulation starts with an initial $V_{in} = V_{TEG}$ set at the theoretical Source-MPPT level of $0.5 \times (Open-Circuit-Voltage)$ for TEG source at this temperature difference. During the IDLE period indicated by the falling edge of V_{OUT} in Fig. 3.19, the source power is stored in a secondary capacitor to mimic a single-input dual-output IVR topology and to maintain the MPPT level. The step-wise increase in output voltage is observed as a result of input hysteresis. As the MPPT algorithm selects different V_{MPP} levels, the rising time and falling time change accordingly. We can observe that eventually the System-MPPT settles at 15 mV higher V_{MPP} compared

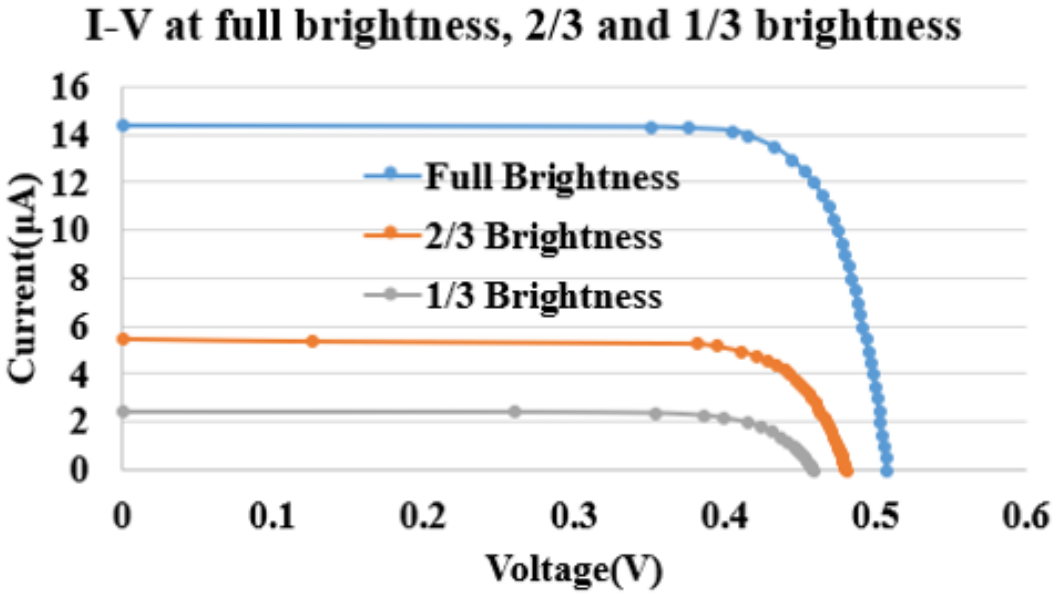


Figure 3.20: I-V measurements of PV cell

to the source MPP starting point. This is similar to the projection from analytical models. However, the transient simulation projects a 13% higher maximum output power, which is higher than the 2.56% predicted by the loss model, indicating that additional measures may be needed to increase the accuracy further.

Application to PV cells

A similar analysis is performed for photovoltaic (PV) considering stacked on-chip photodiodes [50]. In this example, we study the potential of re-configuring harvesting cell networks to maximize output power. The concept of PV cell reconfiguration has been introduced for a regulator-less EHDS to charge a battery [14]. The notion of configuring cell networks can also be used in these cases to shift the conversion responsibility to the harvesting source to prevent a stressed conversion ratio from decreasing efficiency within the PMU. We focus on PV cell reconfiguration for EHDS with a PFM-BR designed to deliver regulated voltages directly to a load.

Power to voltage characteristics are extracted from a PV array from a test-chip that re-

configures a CMOS image sensor array for harvesting [51]. I-V characteristics of the PV array under three different lighting conditions are shown in Fig. 3.20.

This data is scaled, fitted with a third degree polynomial in MATLAB and used as input to the proposed loss model. The results of applying the same analysis for TEG sources are shown in Fig.3.21. It can be observed that the exponential behavior of the photocurrent results in quite different conclusions compared to that for linear-current TEGs. For all three illuminance levels, the operating point that delivers maximum system power converges close to the point of maximum source power for PV sources. Therefore, traditional source-based MPPT techniques are sufficient to guarantee maximum output power for single-cell harvesters.

However, when different source configurations are made possible by a harvesting cell-network, educated configuration selection is necessary to maximize output power. Fig.3.22 demonstrates how source configuration is valuable with three PV array configurations. In this example, a boost regulator to supply 3.3V output voltage has been designed and the

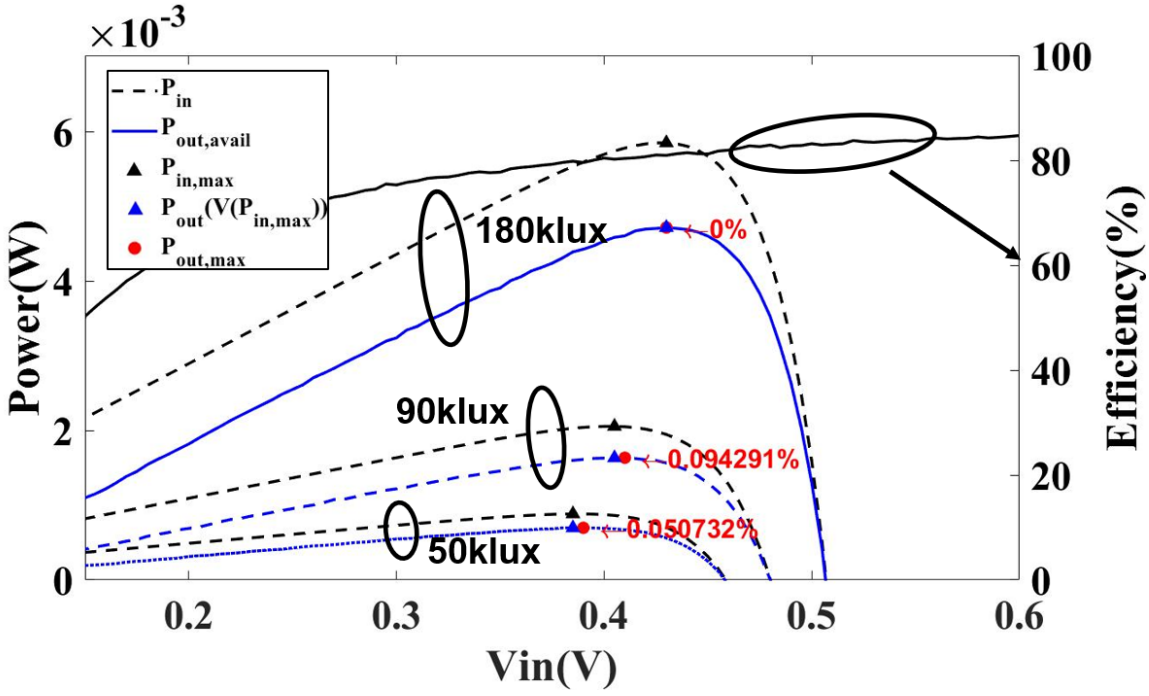


Figure 3.21: PV measurement data power and available output power.

loss model has been calibrated accordingly based on simulated delays/thresholds and active/passive component resistances. Again, the input power data is generated using the measurement data from Fig.3.20 scaled to match the IVR design (∼1mA). A 1Ω resistor is considered as parasitic resistance for each photodiode to establish array connections. The dotted lines indicate source power from each configuration and the solid black line is the conversion efficiency of the IVR.

In the case of PV3, while providing the highest input voltage that allows low conversion ratio and high conversion efficiency in the BR, loss from resistors for stacking is high. Furthermore, the harvested current is relatively low. Without an alternative storage/source, when source MPPT is implemented with input hysteresis control, the low harvesting current

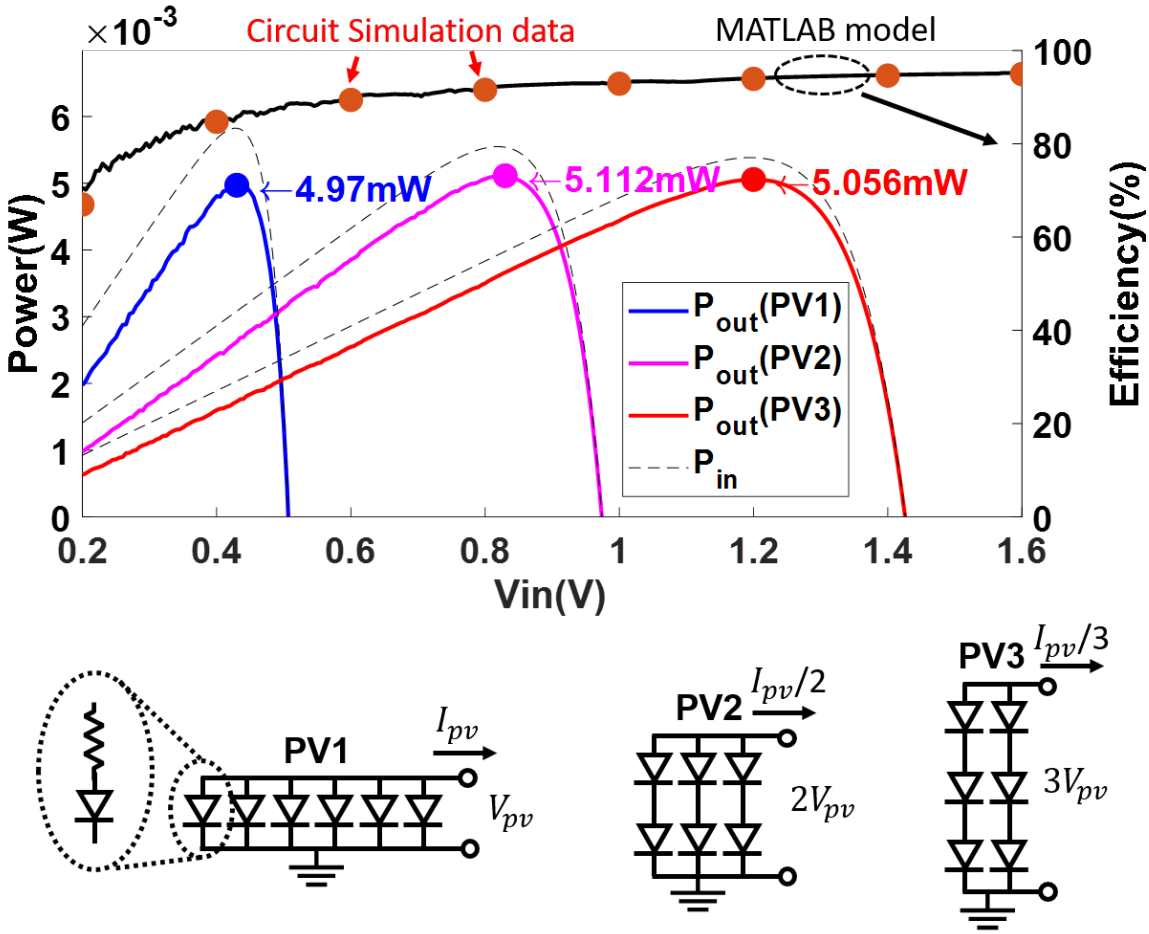


Figure 3.22: PV-IVR output power with three PV configurations.

can result in loss of regulation at the output load due to the extensive time taken to charge the input capacitor. In such cases, a source with slightly lower harvesting voltage but higher current is desired. Looking into configurations PV1 and PV2, the MPP of PV1 is located in a region where the IVR efficiency is experiencing a drop. Though PV2 results in less input power P_{in}, the combined effect results in a 3% increase in output power.

For Single-Inductor-Multi-Output (SIMO) boost regulators which can have very different output voltage domains, this method of adaptively re-configuring harvesting cell networks to distribute up-conversion responsibility depending on the target output voltage level can also be implemented to increase time-division multiplexing efficiency.

3.4 Model Application: Co-design with embedded passives

While a highly integrated system-in-package (SiP) IVRs can be fabricated with low-cost embedded inductors, the higher DC resistance and design correlation between resistance [52] and inductance [53] for embedded passives amplifies its impact on IVR conversion loss. Instead of tailoring the control circuitry of IVRs to pre-determined passives, co-design by including the performance of the embedded passives during the design process of regulator control circuitry can be performed to further increase IVR efficiency.

3.4.1 Co-Design and Results

The analytic model can be used to explore the design space of the PFM IVR and couple that with the inductor design. Fig.3.23 shows modeled maximum efficiency with varying inductance for embedded inductors under fixed oscillator frequency. Embedded inductor ESR dependence is extracted from previous work [52]. Different optimum design points can be observed at different loads. Increase in efficiency with inductance can be observed until these turning points where it is suppressed by increase in ESR and output voltage overshoot. The abrupt stop in the 2mA line indicates the converter is unable to supply the load with a smaller inductance.

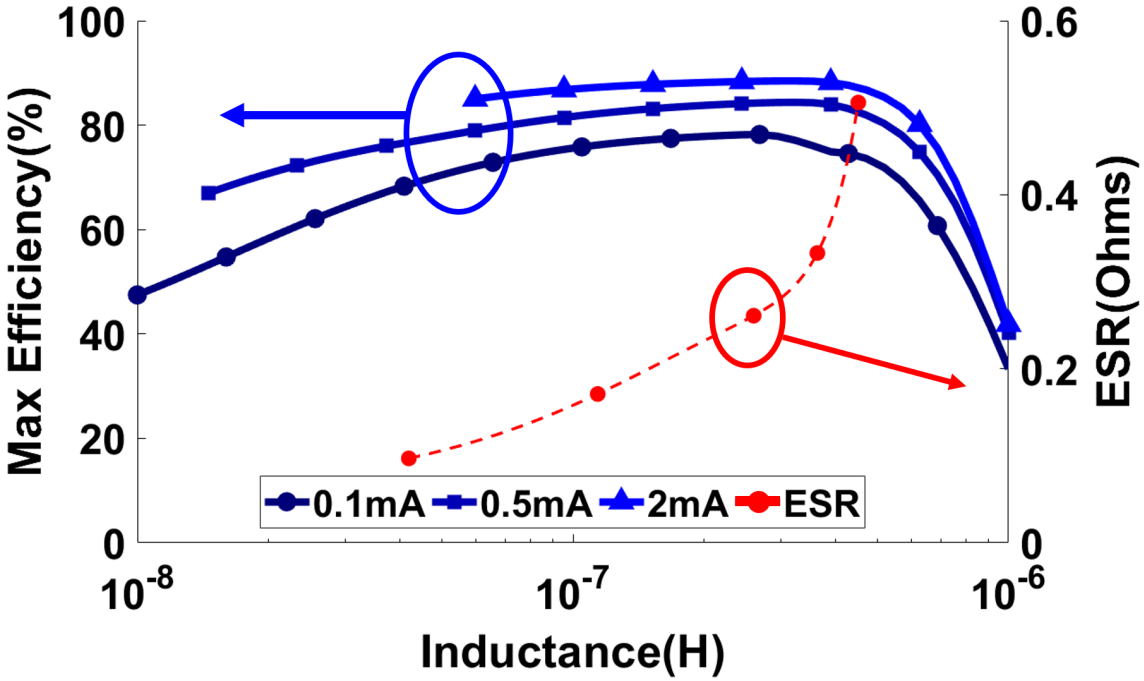


Figure 3.23: Embedded inductor inductance effect on maximum efficiency.

Increase in oscillator frequency segments regulation with finer charging steps, which results in increase in not only switching loss but also a slight rise in conduction loss. This effect is demonstrated in Fig.3.24. We can observe that the conduction loss is less sensitive to frequency variation under the condition that the power stage including power switches and drivers are fixed. Switching loss remains stable at lower frequency until it starts rising proportional to the frequency. The relatively flat region occurs when frequency change is canceled out by idle time.

Co-design analysis is performed with the procedure as shown in Fig. 3.25. In this procedure, an initial design of the inductor is determined and parameters of the inductor are modeled in HFSS and MATLAB. These parameters are included in the PMU design and the combined performance is analyzed and evaluated to determine if a change in inductor design can be beneficial. The goal of the co-design is to achieve maximum efficiency while minimizing area. Co-design to achieve maximum efficiency with embedded inductor designs 3, 5, and 7 from [52] integrated into the PFM boost regulator model is performed.

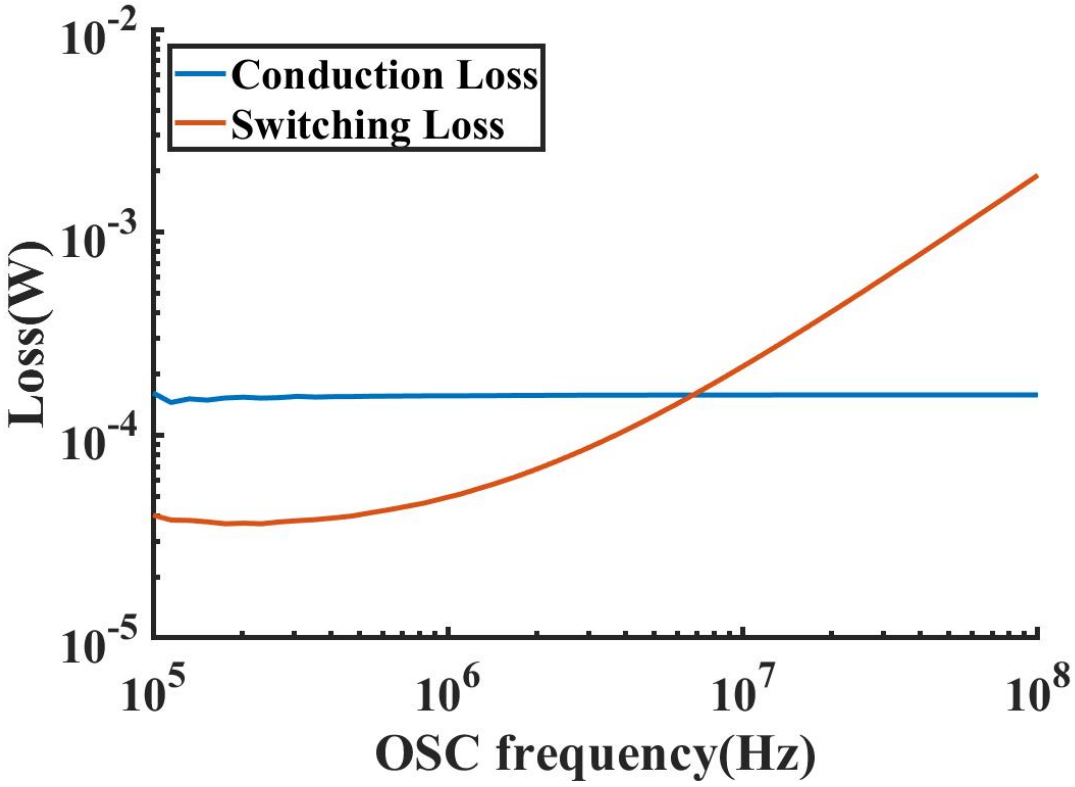


Figure 3.24: Conduction loss and switching loss at different frequencies (Post-silicon optimization: Fixed power stage).

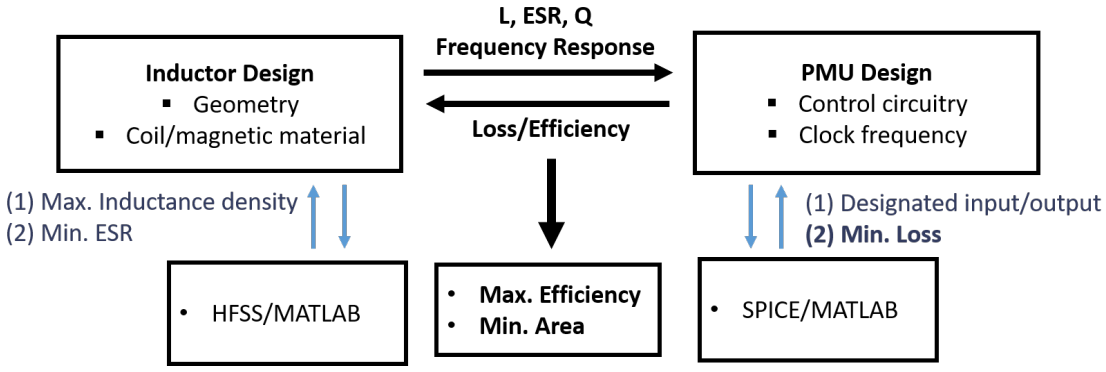


Figure 3.25: Co-design flow for conversion efficiency optimization.

Each inductor design is optimized at their respective inductance level for minimal area and ESR. Their characteristics are incorporated into the loss model and the oscillator frequency to maximize the efficiency for each design is determined. Table I shows resulting operating frequencies and losses that would produce maximum efficiency obtained from the

Table 3.2: Operating Frequency and Loss for Co-design

Inducor Design	3	5	7
Inductance	114 nH	364 nH	452 nH
DC Resistance	0.171 Ω	0.339 Ω	0.506 Ω
Operating Freq.	5.7 MHz	1.6 MHz	1.4 MHz
Conduction Loss	236 µW	270 µW	**306 µW**
Switching Loss	**414 µW**	129 µW	103 µW
Peak Eff. (2mA)	81%	**87%**	86%

model. The target load is 2mA at a regulated output of 1.5V, with target ripple guaranteed for input voltage ranges from 0.2V to 1.0V.

Table 3.2 shows resulting operating frequencies and losses that would produce maximum efficiency obtained from the model. By observing the conduction and switching loss contributions of the design with inductor design 3, the dominance of switching loss would suggest designing with higher inductance and lower frequency. From design 5 to 7, however, the cost of higher conduction loss with inductor design 7 counters the benefit of decrease in switching loss by the lower frequency and further increase in inductance may not be favorable. This is counter-intuitive to the traditional boost regulator design where a larger inductance and hence, lower frequency is preferred to reduce switching loss.

Under these conditions, designing with the 364nH inductor is estimated to show the highest peak efficiency. The results successfully demonstrate an optimal system design point and can be adjusted to support future co-design strategies for SiP IVRs. For example, a post-silicon efficiency optimization strategy would be to tailor the on-board embedded inductor design as the operating frequency undergoes process variations.

CHAPTER 4

EHDS-BASED LOAD CONTROL FOR REDUCED SYSTEM POWER

This chapter presents details of a power management approach to minimize battery power needed to support low duty-cycle operation of high-power loading modules. Measurement data are obtained from a testchip implemented in 65nm CMOS. A chip micrograph of the testchip is shown in Fig. 4.1

4.1 Target Application and Implementation

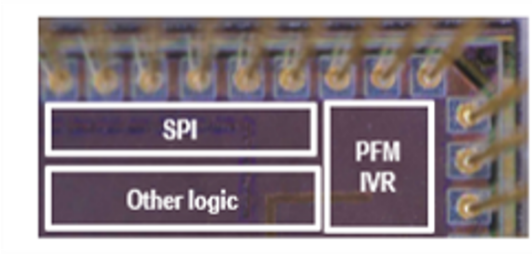
The proposed method has been designed to address the demand for extended lifetime in battery-powered systems. For these systems, a simplified expression of the lifetime (T_{life}) can be expressed as:

$$T_{\text{life}} = \frac{E_{\text{battery}}}{D \times P_{ACTIVE} + (1 - D) \times P_{IDLE}} \tag{4.1}$$

Where $E_{battery}$ is the storage capacity, D is the duty cycle and P_{ACTIVE}, P_{IDLE} are active and idle power of the system. For more accurate computation, P_{active} includes power consumed during system wakeup, data receiving/transmitting, core processing, data logging, and other states, depending on the application. P_{IDLE} can include power from "standby" modules and leakage from "sleeping" modules and within the battery itself. For sake of simplicity, $D \times P_{ACTIVE}$ in eq.4.1 is sometimes expressed in terms of energy with $N \times E_{event,total}$, where N is the number of active events that occur and $E_{event,total}$ represents the total energy consumed during each encounter. The equation then becomes:

$$T_{\text{life}} = \frac{E_{\text{battery}} - N \times E_{event,total}}{P_{IDLE}} \tag{4.2}$$

With the above equations in mind, it is straightforward that for low duty cycle operations,



Technology	65nm CMOS
Package	CLCC44
Area	1mm x 1mm
IVR Area	227µm x 101 µm

Figure 4.1: Chip micrograph and specification of the testchip/package.

the lifetime can be dominated by P_{IDLE}. Methods such as bias gating [29] and clock gating have been used universally to reduce idle power of individual blocks and systems. However, in technology nodes and processes that suffer from leakage, power gating is often required. The following design embeds power gate control with PMU control to create a simple but effective method to only enable loading modules when the PMU output is stabilized with sufficient input power. The design further integrates energy harvesting from DC harvesting sources that are used to supply loading modules (after conversion through the PMU), and also serve as indicators for on-demand system wakeup.

Fig. 4.2 shows a schematic of the proposed architecture during ACTIVE and IDLE states of operation. An IVR with pulse-frequency modulated (PFM) control is designed on chip to regulate and supply loading modules and is the only component that consumes battery power in this design. Energy is harvested from an off-chip photodiode to supply on-chip loads. Off chip passives include the main IVR inductor and input/output capacitors. Co-design of the energy transducer (off-chip photodiode) and IVR impedance is also performed so that the transduced power is insufficient to reach regulation at nominal room light condition (the system stays IDLE).

During an IDLE state, the power gates to loads are closed and the IVR freely draws current from the harvesting source to counter leakage at the output node. When an external light source is applied, the output will boost and allow the HFBC to switch at regulation. After this point, the power gate is enabled and the system wakes up and enters ACTIVE mode.

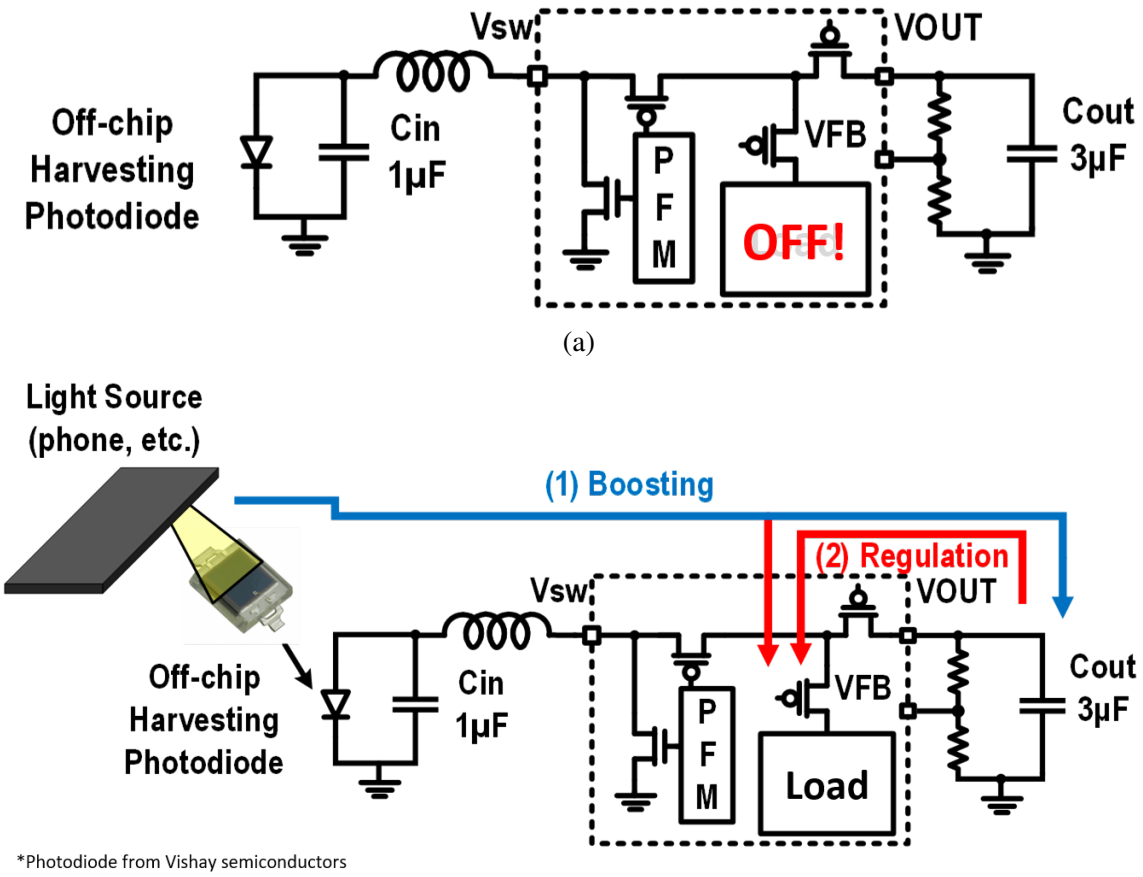


Figure 4.2: Power management during (a)IDLE (b)ACTIVE for proposed EHDS.

4.2 Embedded Wake-up mechanism with PMU control

4.2.1 Wake-up FSM

To implement this functionality, we have adopted an analog bang-bang IVR architecture that consists of a synchronous power stage, a CMOS current-capacitor oscillator with 4-bit configurable frequency and analog PFM control path (Fig. 4.3). The control path has three main comparators, namely, a hysteresis feedback comparator (HFBC), a current limit comparator (CLC) and a zero current comparator (ZCC) [43]. The CLC senses the inductor current through the node voltage Vsw and changes from inductor charging to boosting by switching both NGT and PGT low when the current surpasses a designed threshold. The

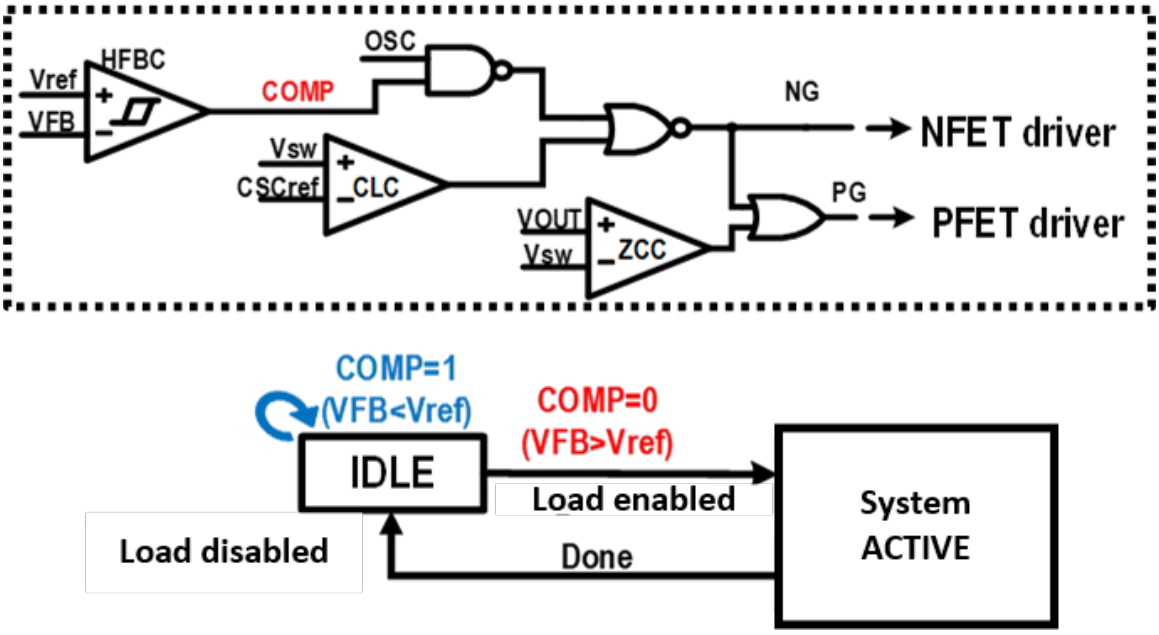


Figure 4.3: PFM control path for IVR including HFBC, CLC, ZCC and on-chip finite state machine.

ZCC prevents current back-flow by comparing voltages across the PFET switch (Vsw and VOUT). The HFBC directly modulates the regulator output by enabling boosting when a divided feedback voltage (VFB) falls below an on-chip reference voltage. The output signal of the HFBC, "COMP", indicates a "ready" (COMP=0) power state during typical regulation and is adopted to serve as a trigger for the on-chip FSM to enable/disable power gates to loading blocks. Measured switching signals of the PFM control are shown in Fig. 4.4.

One of the key design targets of the IVR is that the implementation should ensure that power gates to loads do not open prematurely under fluctuations in input power (which is dependent on illuminance on off chip photodiodes in the described setup). This can cause glitches in system operation and erroneous results to occur. Therefore, the IVR impedance needs to be designed to be low enough to drain the off chip diode close to short-circuit conditions under room light conditions. Furthermore, the conversion efficiency of the IVR will need to be restricted under low input voltage. Under this criteria, the IVR boosted output voltage will also be low, as it will be limited by the duty cycle of OSC and leakage

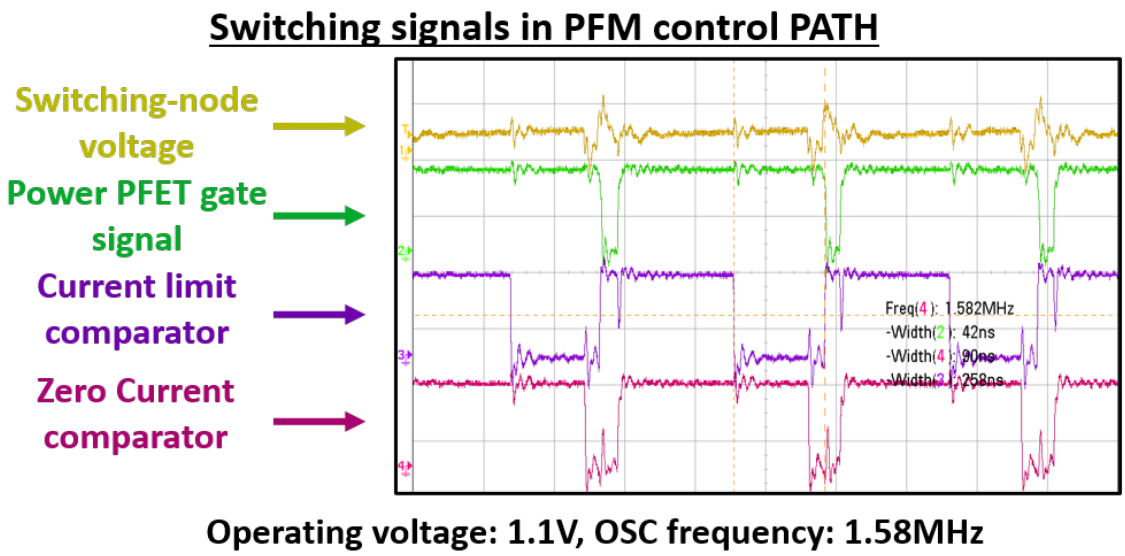


Figure 4.4: Measured PFM control path switching behaviour. Switching node voltage =V_{sw} in Fig. 4.2. Operating voltage increased to 1.1V for undistorted off-chip observation.

from loads.

IVR impedance design and configuration is mainly performed through the design of the oscillator (2.4MHz∼13.4MHz) and the CLC threshold (348mA) which have been measured under typical operating voltage of 0.8V. Additionally, high voltage devices have been used for the low-side branch of the power stage to increase parasitic resistance (due to higher threshold voltage) when the input power is low.

Fig. 4.5 shows a measurement waveform for the three phases of: (1) room light inten-

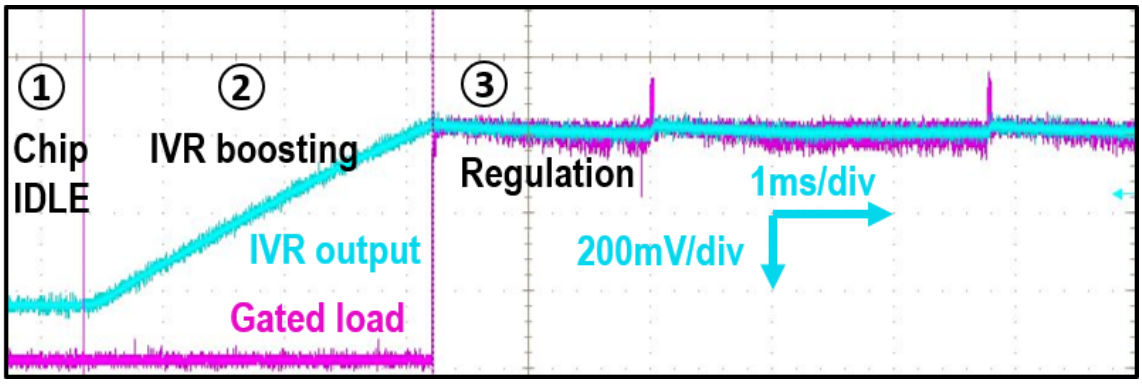


Figure 4.5: Measured Waveform showing three phases of wake-up under low-to-high light intensity step.

sity (∼380lux) during which sensing/encryption is idle, (2) high intensity boost (>5Klux), and (3) high intensity regulation with power gate enabled when a light intensity step is applied. It can be observed that the IVR output remains at ∼200 mV during IDLE and it takes around 2.5ms for the IVR to reach regulation. Also, the 3µF output capacitance can maintain output voltage levels during charge sharing when the power gate is enabled.

4.3 Efficiency Optimizations

This section explores approaches to allow adaptive efficiency optimizations to be performed as an addition to the prior power management scheme. Specifically, we wish to leverage the large difference in load conditions during and after system wake-up to perform PMU system optimizations with two methods: (1) Designing parallel power switches to be enabled (2) Re-configuring IVR switching frequency. The first approach is analyzed with transistor-level simulations and the second is analyzed with silicon measurement data. Both approaches focus on improving power delivery system performance under different phases of operation and require minimal change in system design.

4.3.1 IVR parallel power stages

As mentioned in section 4.2 the usage of high voltage devices to implement power switches and power gates to loading modules in the IC were necessary to prevent system start-up from ambient light sources. The increased threshold voltage for these high voltage devices limits power delivery from low harvesting voltage at typical room-light conditions ($V_{OC} \sim 0.26$V@500lux). However, for the same reasons, power conversion efficiency during high-power conversion is also impacted.

Parallel power switches that can be selectively enabled can be utilized to reduce conduction loss at increased load (Fig. 4.6). An analysis with transistor level simulations has been conducted with a parallel power switch that is $3\times$ larger (equivalently $4\times$ stronger in total when enabled). From transient simulations with 100nF output capacitance, maximum

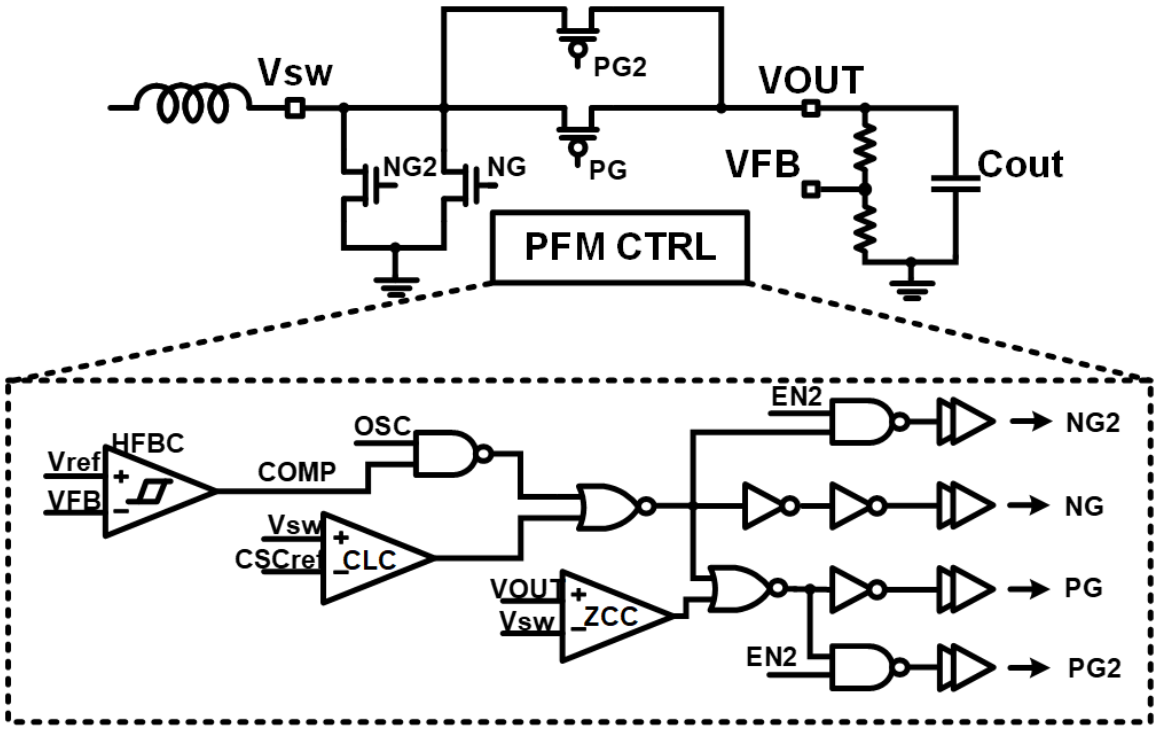


Figure 4.6: PFM boost IVR with parallel power switch enabled.

efficiency observed at 1.2V supply (3MHz OSC frequency), 0.9V input voltage, 1.0V output regulation and 0.5mA is increased from 76.8% to 83.4% by enabling the $3\times$ parallel output stage. Based on the PFM boost regulator model proposed in Chapter 3, the maximum load current can also be increased by $\sim 3.5\times$ ($2mA \rightarrow 7mA$) due to the increased current limit. However, to achieve this increase in conversion efficiency and maximum load current, static leakage current is increased by $7.17\mu A$.

4.3.2 Frequency reconfiguration

An alternative approach to prevent IDLE power overhead from leakage would be to utilize existing blocks for efficiency optimization. As shown in Chapter 3, the oscillator frequency plays a critical role in determining inductor current behaviour and thus, conversion efficiency. The oscillator design implemented in the IC is an analog differential current-capacitance oscillator with additional capability to tune oscillator frequency enabled by implementing configurable current mirror paths control the bias current for the oscillator

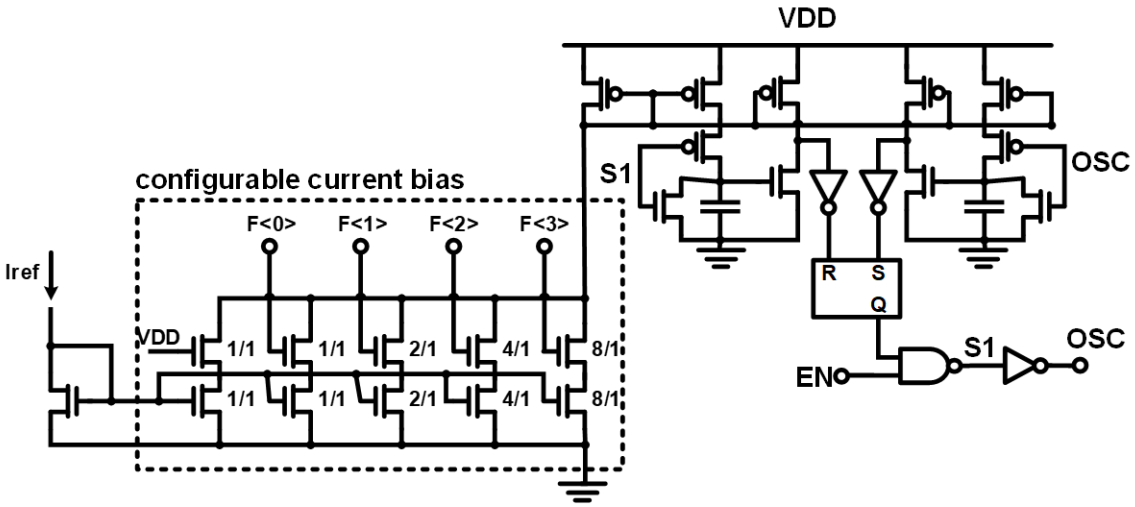


Figure 4.7: Schematic of analog I-C oscillator with frequency configurability.

(Fig. 4.7). A feasible range of 2.4 MHz to 13.4 MHz is observed at nominal 0.8 V.

Efficiency measurement results for different frequency and input voltages are shown in Fig. 4.8. To observe internal switching signals, the IVR control voltage has been increased to 1.2V the conversion efficiency measurements. Using a 1.2V supply, the measured switching frequency of the oscillator ranges from 0.96MHz to 5.26MHz and the measured conversion efficiency (at 500μA load and 1.0V output) increases by 23%. However, as expected, gain in conversion efficiency is only observed for high input voltage conditions because the conversion efficiency at low input voltage is limited by the 2.5V devices. An abrupt drop can be observed at around 0.65V for the [5.26MHz, 150µA] measurement. The measured maximum load current that can be regulated is also increased from 1.3mA to 2.5mA. However, IVR power is increased from 21.7 μW to 56.8 μW.

One can operate the IVR at low frequency in idle mode to save power with similar conversion efficiency and increase the frequency in active mode to improve efficiency when the load demand is high. This allows maximum utilization of the configure-ability to increase overall system efficiency. Moreover, the reconfiguration can be performed by using the same signals and circuitry for waking up loading systems, which adds very little overhead to system design and implementation.

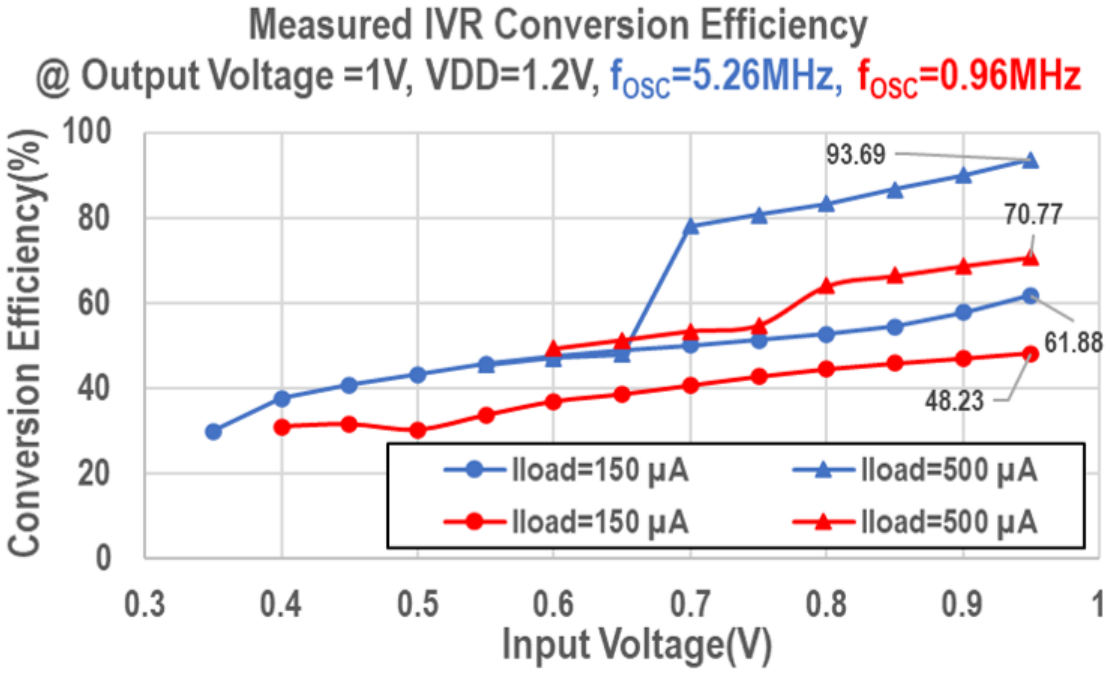


Figure 4.8: Measured Efficiency of IVR configured at two oscillator frequencies (top) 5.26MHz (bot) 0.96 MHz.

4.4 Discussions

4.4.1 Variation Analysis of Oscillator

The process, voltage, and temperature (PVT) variations modulate the frequency and duty-cycle of the oscillator (Fig. 4.9), which in turn can impact power delivery circuits. However, in a PFM voltage regulator, the variation in the oscillator's frequency only changes the efficiency, but the wake-up and regulation properties depend mainly on the duty cycle [43]. Fig. 4.9 shows that the duty cycle of the differential current-capacitance oscillator implemented is largely independent of PVT variation thereby maintaining power delivery quality. Therefore, while conversion efficiency may be impacted by PVT variations, the main functionality critical for the proposed power management scheme remains intact.

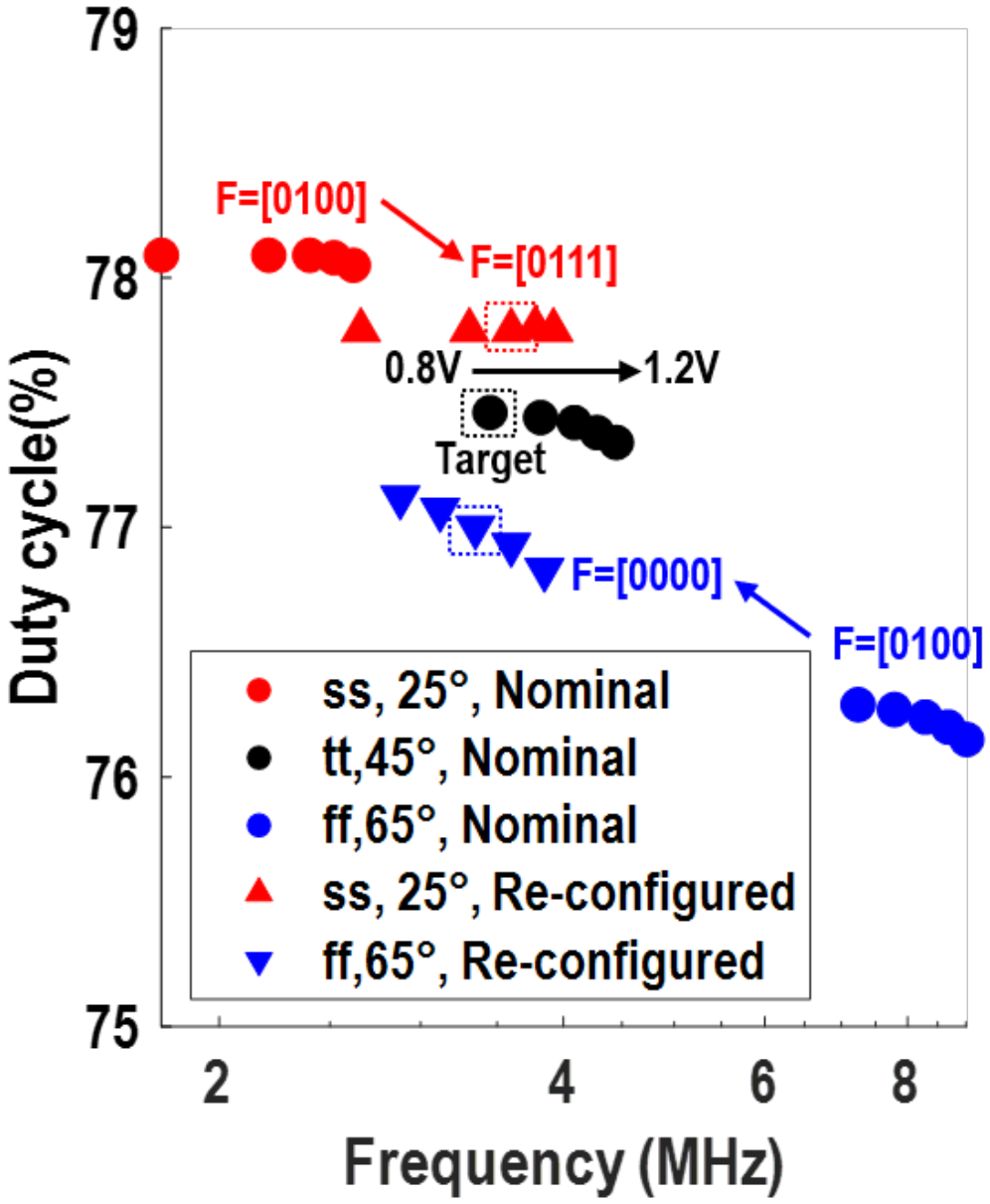


Figure 4.9: Oscillator PVT variation simulation. Due to sub-threshold biasing, slow-slow process at low-temperature and fast-fast process at high-temperature produce maximum variation.

4.4.2 Reducing variation via re-configuration

Utilizing the configure-ability of the designed oscillator, it is possible to reduce the effect variations. For example, consider the baseline design with frequency configuration F=0101 under typical corners (@[1.0V, tt, 45°], marked with dotted box in Fig. 4.9). The worst-

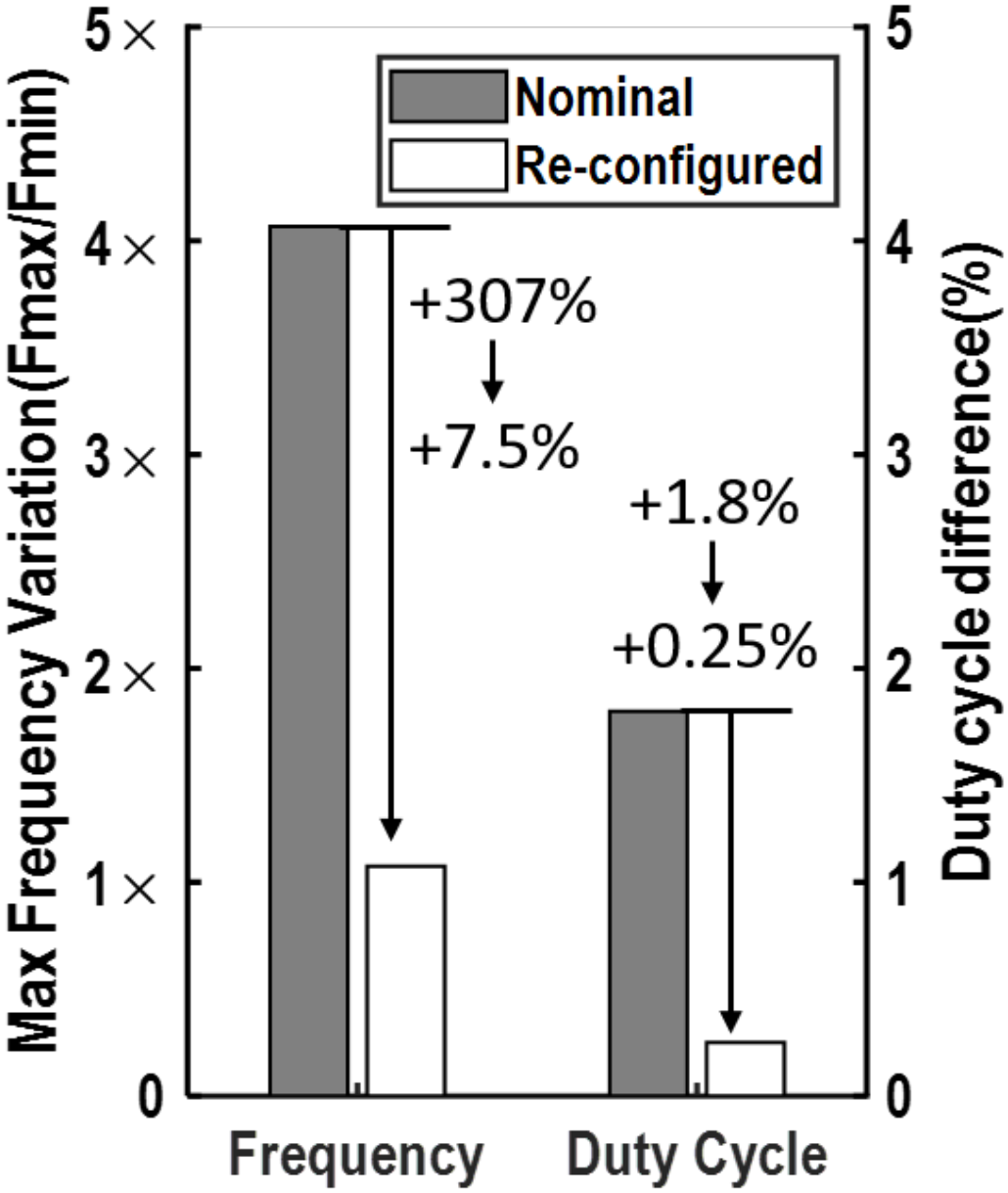


Figure 4.10: Effectiveness of re-configuration.

case PVT variation is observed from [0.8V, ss, 25°] to [1.2V, ff, 65°] and results in 471% and 2.0% difference in frequency and duty-cycle, respectively (Fig. 4.10). Using F=1011 for [ss, 25°] and F=0001 for [ff, 65°] one can reduce frequency and duty-cycle variations to 47% and 1%, respectively, even under $\pm 200mV$ of voltage variation.

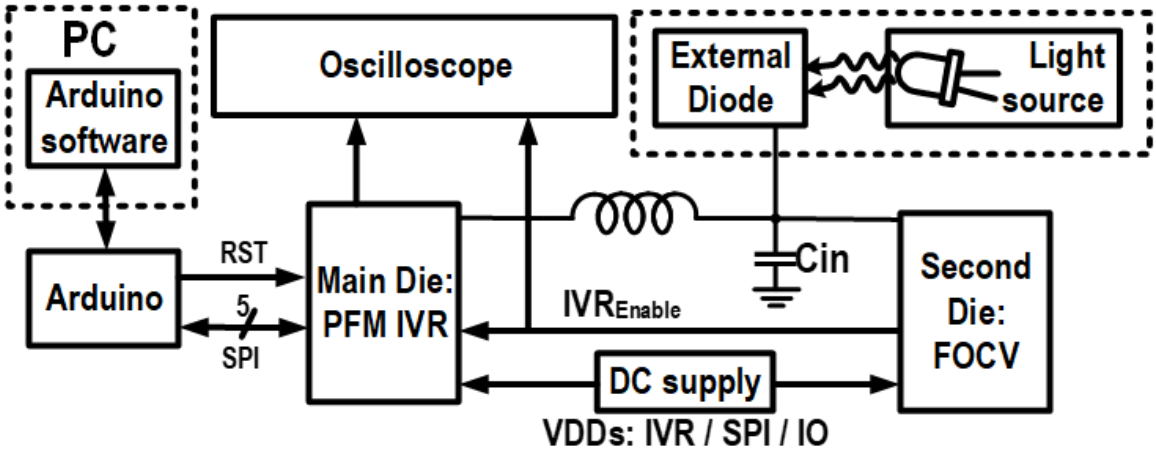
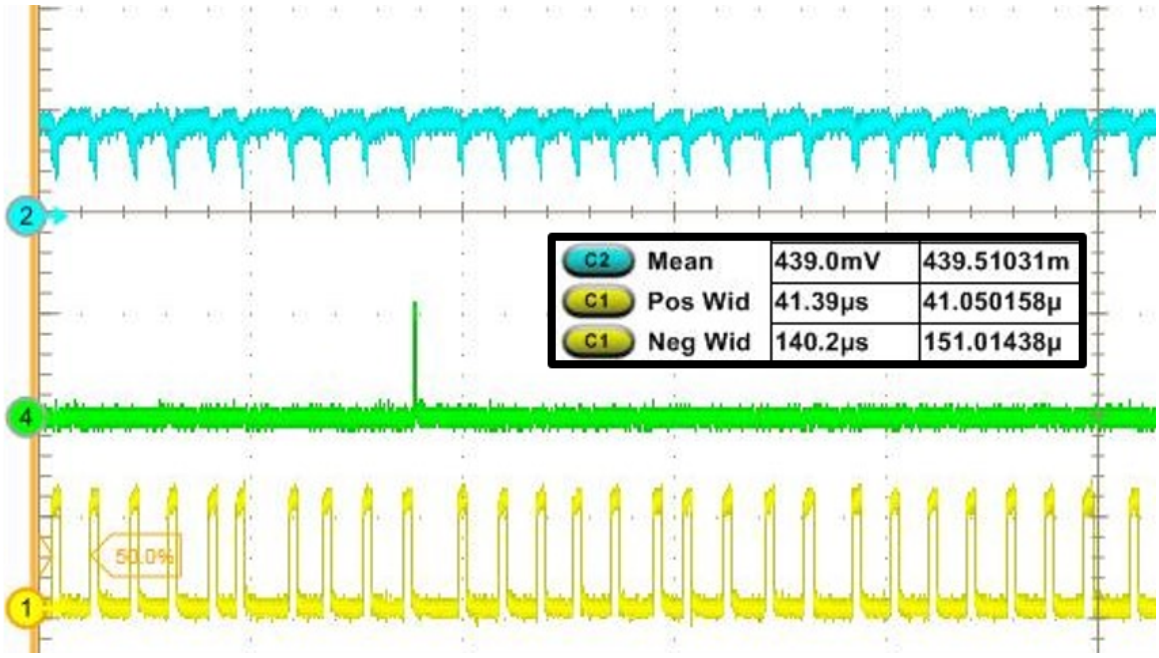


Figure 4.11: Measurement setup with off-chip MPPT.

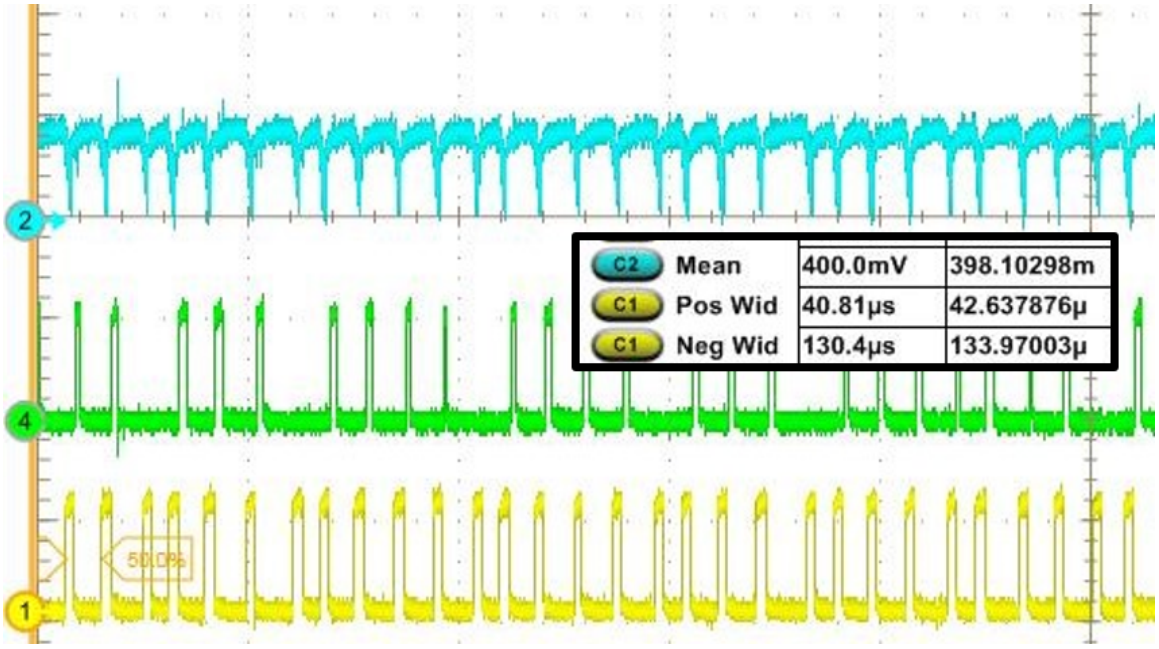
4.5 System Analysis: Discrete conduction maximum power point tracking

As explained in 2.3.1, maximum power point tracking in discrete conduction mode demonstrate very different profiles compared to continuous conduction MPPT for high-power applications. However, it's design is equally, if not more, critical compared to CCM MPPT due to limitations in input power. The following demonstrates key findings from initial test measurements to identify key characteristics and challenges during PFM MPPT.

Fig. 4.11 shows a schematic of the measurement setup. Testing of MPPT is performed with the following setup: A main die with a PFM IVR is configured to perform harvesting/regulation operation in a manner similar to the aforementioned setup. However, instead of allowing the IVR to freely operate, a configurable signal that enables/disables switching activity (IVR_{enable}) is controlled by a second die that contains a Fractional Open-Circuit Voltage (FOCV) sampling circuit. The main purpose of the FOCV control is to disable IVR switching activity when the harvesting voltage drops below the sampled reference voltage to ensure the boosting operation does not draw the input source to short-circuit conditions. In this test, off-chip photodiodes are also used as the harvesting source.



(a) 36 klux



(b) 17 klux

Figure 4.12: measurement of MPPT at 36klux and 17klux. Blue: Input photodiode voltage; Green: FOCV-generated IVR disable signal to prevent voltage drop beyond threshold; Yellow: IVR output hysteresis comparator signal (high=active, low=idle)

4.5.1 MPPT measurement waveforms

Fig. 4.12 shows tracking waveforms under different lighting conditions. The output voltage is set to be 880mV in these measurements.

At 36klux intensity, we can observe that the input voltage (light blue) showcases spurious drops which correspond to pulses of current drawn by the IVR when it is enabled (yellow). However, the harvested power and input capacitance is able to sustain input voltage and prevent it from dropping below the threshold set by the FOCV circuit and the IVR is rarely disabled (green) halfway through a boosting pulse. Although energy is wasted during IDLE periods in the single-input-single-output EHDS, regulation of the load is sustained while supply quality is guaranteed.

Under this illuminance, the majority of the harvesting behaviour is not different from typical DC-DC conversion scenarios. The IVR is allowed to complete a boosting cycle that is sufficient to reach the higher hysteresis threshold of the HFC and maintain output regulation without being restricted by input regulation requirements. We can observe from the measurements acquired by the oscillator that output regulation for the IVR shows a mean ACTIVE period of 41.39 µs and an IDLE period of 140.2 µs.

As the illuminance on off chip diodes is reduced to 17klux, however, the input power also reduces and the harvesting behaviour is also impacted. Under this condition, we can observe the following changes in the measured waveforms:

1. deeper dip in input voltage (light blue)
2. frequent IVR disable. (green)
3. reduced IDLE periods. ("Neg Wid" of yellow waveform)

From these findings, we can conclude that input power generated by the photodiodes can no longer support instantaneous current drawn from the input capacitor (Cin). The ACTIVE period is reduced to 40.81 µs because boosting is cut short by the FOCV circuit when it

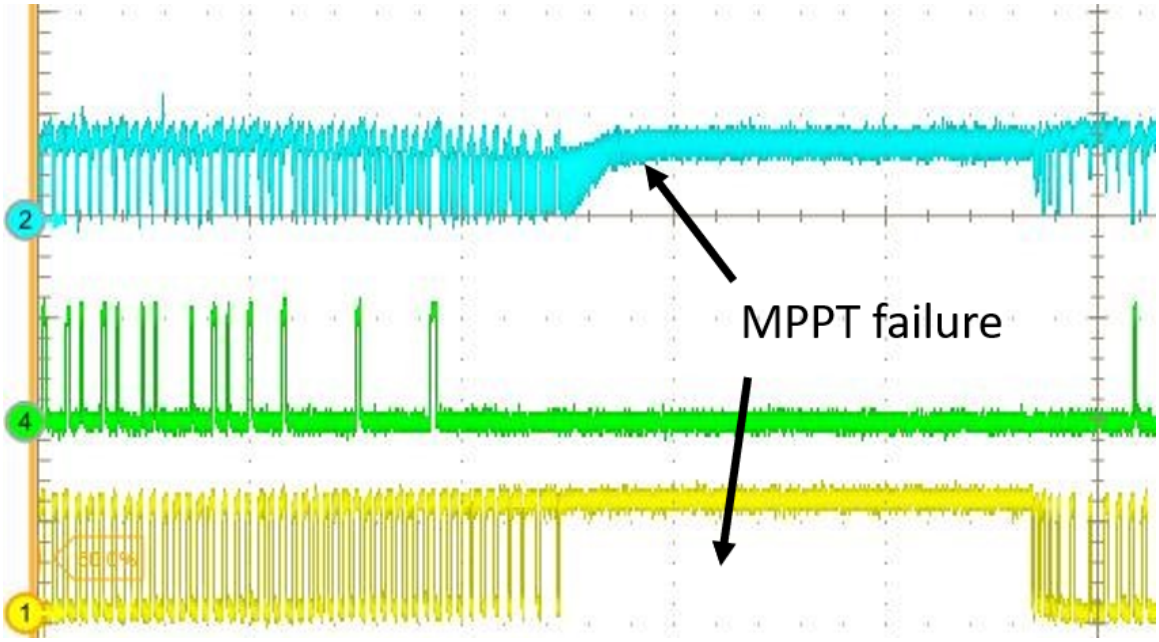


Figure 4.13: Occasional MPPT failures at illuminance <17klux.

senses that the input voltage has dropped. However, although the IVR is turned off by the FOCV circuit, residue energy in the inductor still draws current from the input node while it is released, and a higher dip in the input voltage is observed. Furthermore, the IDLE period is also reduced because the charge boosted to the output is also reduced due to the shorter ACTIVE period:

$$T_{\text{IDLE}} = \frac{Q_{\text{boost}}}{I_{load}} \tag{4.3}$$

Further reducing the input power results in glitching behavior and occasional MPPT failure during measurements. A sample failure is captured in Fig. 4.13. It can be seen that spurious pulses when the IVR is ACTIVE frequently drain the input voltage, even when the FOCV circuit tries to disable the IVR switching activity. As shown in Fig. 4.13, although a weak point of stability can be maintained initially, fluctuations in input power can cause the input voltage to be drained to a point that it cannot restore itself before the next pulse arrives. The low-voltage also results in low-efficiency boosting and escalates the need for longer ACTIVE periods before the output can reach regulation. This is marked as "MPPT failure" in the figure.

4.5.2 Limitations

From the aforementioned off-chip PFM MPPT test measurements, we can conclude the following limitations that need to be addressed to realize a robust EHDS for low-power harvesting in self-powered devices.

1. Static battery power: As explained in 2.3.2, cold-start is a critical function needed in battery-less systems to allow restoring of system operation under input power variations. However, prior cold start approaches suffer from slow wake-up (simple bootstrapped mode) or high area overhead (auxiliary converters). Furthermore, prior approaches do not incorporate undesired-wake-up prevention. A different approach will need to be designed to eliminate battery power consumption of the prior system.

2. Drop in harvesting voltage (low input power): For EHDS designs where harvesting sources are directly connected to the IVR, the harvesting voltage is also the input voltage that the IVR sees. This node voltage increases/decreases based on the relative strength of the source current compared to the inductor current. For systems where the source power is abundant (i.e. harvested current can fully supply inductor current) harvesting can almost be viewed as DC-DC conversion. However, When the source power is low, harvesting voltage can drop when the IVR is ACTIVE. To prevent failures caused by extensive harvesting voltage drop, higher capacitance/inductance can be deployed to dampen voltage ripple and higher frequency can be utilized to reduce current ripple. This approach is commonly implemented in prior literature shown in 2.3.1. However, higher cost and form factor is often associated with the use of increased passives when trying to maintain similar quality (e.g. total ESR along power delivery path).

3. Wasted IDLE energy during MPPT (high input power): Another concern that adds unnecessary overhead to the system is that the energy stored in the input capacitor saturates when the harvesting voltage reaches its open-circuit voltage (V_{OC}) when

input power is high. Prior designs often integrate secondary backup storage units to store energy for later re-use [32]. However, it also induces increased area and design complexity of the EHDS.

4. Slow response: The current test setup with on-board integration of two dies suffers from slow response due to high-latency off-chip signals used to enable/disable the IVR. Furthermore, the asynchronous sampling/IVR switching across two dies is also a reason for glitching behaviour during MPPT when the voltage sampled is not at V_{OC}.

The following chapter will explain a compact EHDS implementation that targets to address these concerns.

CHAPTER 5

DESIGN AND MEASUREMENT OF A LOW-OVERHEAD EHDS

This chapter presents a compact, low-cost energy harvesting and delivery system (EHDS) with pulse frequency modulated (PFM) integrated voltage regulator (IVR) power conversion and self-tuned maximization of system output power. A novel load-inclusive time-based maximum power point tracking (LI-TB-MPPT) is developed to provide centralized tuning of PFM-IVR operation based on both source capabilities and load demand on-the-fly, and a configurable fractional sample & hold (FSH) circuit provides adaptive harvesting window control. The EHDS enables robust harvesting while relieving the use of high passives, with over 2 orders of magnitude reduction, at the cost of only slight decrease in end-to-end efficiency compared to prior works. Furthermore, a low-overhead wake-up assist circuit utilizes cold-configuration of harvesting sources for efficient and accelerated cold-start.

Altogether, the presented design resolves several drawbacks that limit deployment of self-sustained energy harvesting in small-scale systems. *1) large overhead:* devoted auxiliary converters and/or larger harvesting sources are needed to address low-efficiency power conversion during cold-start, *2) large, high-cost passives:* high passives (L/C) are needed to provide input voltage filtering/regulation and to increase conversion efficiency of the PMU, and *3) load decoupling:* source-oriented MPPT prioritizes regulation of harvesting voltage and does not consider change in the conversion efficiency of the power management unit (PMU) under variations in load and input power. A detailed survey and discussion can be found in Chapter 2 and Chapter 4.

The proposed EHDS is demonstrated in a 65nm CMOS process with commercial Photovoltaic (PV) energy harvesting modules. Using only 1.2µF and 1 µH of passives, measured results show a peak 74.9% end-to-end efficiency (simulated upto 85% at 47µH) and

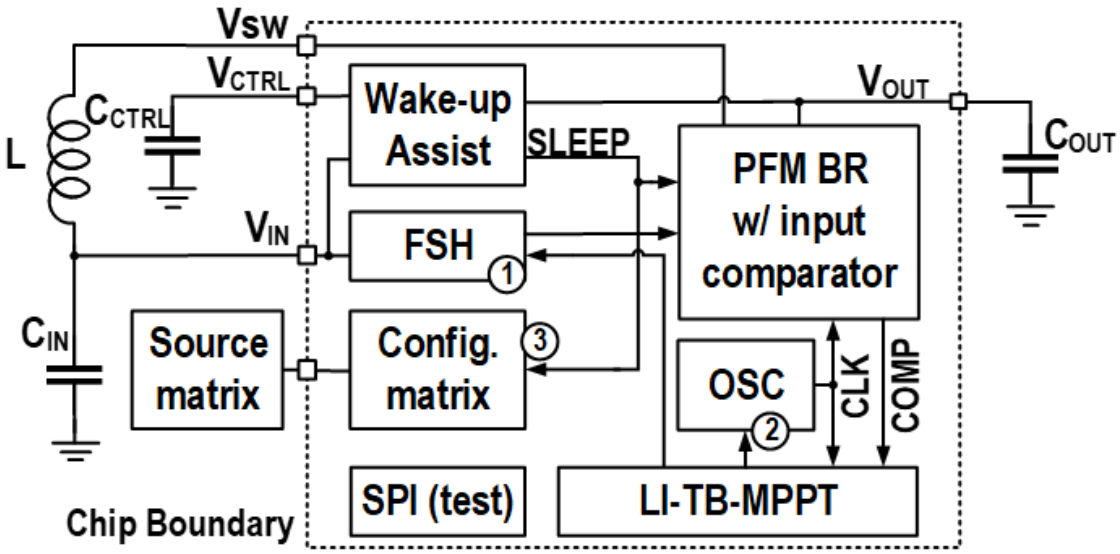


Figure 5.1: Schematic of proposed system components.

a fast startup time of 3.8ms. Up to 15% increase in conversion efficiency against load and input voltage variations is achieved with LI-TB-MPPT. The results demonstrate a compact solution for self-sustained cost-restricted standalone systems.

5.1 Proposed Approach and System Components

The high-level schematic of the proposed system is presented in Fig. 5.1. An input comparator for harvesting voltage regulation is integrated with a typical PFM boost regulator (BR) architecture [43] to form the main PMU of the proposed system. The LI-TB-MPPT circuit, which represents our proposed load-inclusive time-based MPPT approach, takes the output comparator signal (COMP) along with the oscillator clock as inputs to perform fully-digitized power estimation and internally uses a perturb and observe algorithm to control configurations in ① the fractional sample & hold (FSH) block and ② the oscillator to maximize output power. The mutual dependence of the LI-TB-MPPT and FSH blocks is especially important and is a key innovation in this work. FSH supports the system-output-optimization of LI-TB-MPPT by allowing flexibility in controlling the harvesting window. LI-TB-MPPT performs the load-sensing required for open-circuit-free sampling

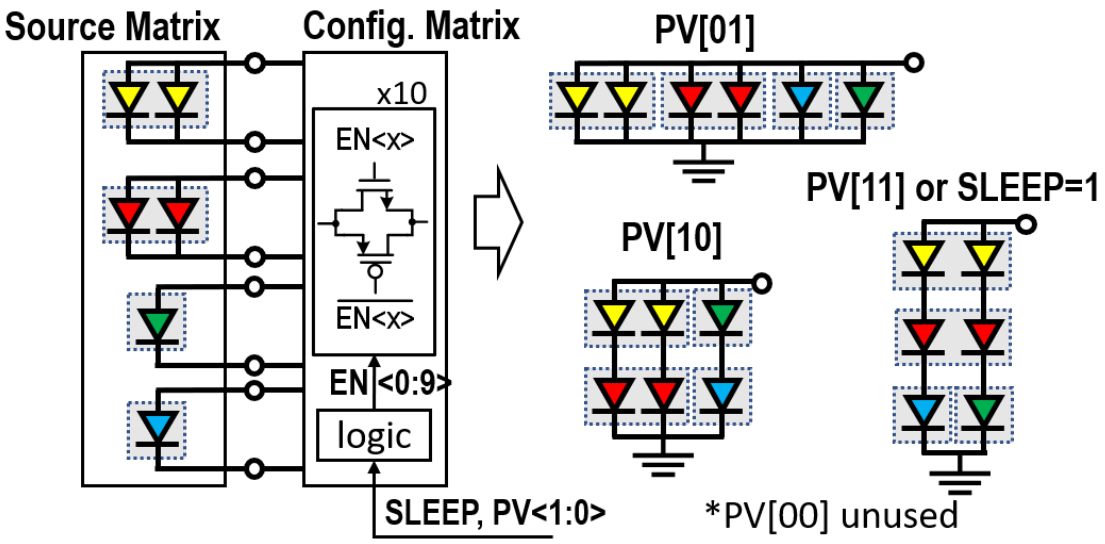


Figure 5.2: Possible source configurations.

in the FSH circuit. These points will be explained in detail later in this section. Together, LI-TB-MPPT and FSH provide the foundations for a robust EHDS with reduced inductance and capacitance. ③ The analog wake-up assist circuit creates a "SLEEP" signal for initial cold-configuration across the system and manages connections between the output voltage (V_{OUT}), the input voltage (V_{IN}), and the control voltage (V_{CTRL}) to enable controlled transition from efficient $V_{IN} \rightarrow V_{CTRL}$ charging for accelerated cold-start to bootstrapped $V_{OUT} \rightarrow V_{CTRL}$ self-powered operation.

5.1.1 Cold-start: Wake-up Assist

An advantage of PV harvesting sources is that they can generate relatively high voltage (> 0.2V) in nominal room-light environments. The high V_{OC} from PV modules gives opportunity for using self-powered source configurations to create the necessary kick-start voltage for the main PMU, and eliminate the large area overhead associated with the prior need for auxiliary cold-start converters. A critical challenge for realizing cold-configuration functionality is that the state of digital logic can be hard to determine without explicit RESET triggers. Incorrect cold-configuration of the EHDS can result in system

failure. To realize low-overhead cold-start, we propose a wake-up assist (WUA) circuit that creates a robust "SLEEP" signal even in sub-threshold voltages (<0.4V) to guarantee correct initialization of the EHDS during cold-start. This signal is used universally across the EHDS to "assist wake-up operation". For example, the EHDS bypasses low-efficiency switching activity at low voltages completely (PMU is turned OFF) by using the SLEEP signal to bias-gate all analog comparators until the system is ready to enter boot-strapped operation. To still be able to create sufficient wake-up voltage of the system (without switching the PMU), one of the most important purposes of the SLEEP signal is to control harvesting source configurations (Fig. 5.2) during cold-start. Before cold-start is complete, the WUA ensures harvesting sources are always configured in series (with SLEEP$= 1$) to create a high voltage. After the control voltage is sufficient for typical operation, the WUA re-configures the source to its programmed state for higher efficiency.

In this test-chip, the on-chip source configuration matrix enables three combinations (stack of 3, 2 and all parallel, Fig. 5.2) of off-chip photodiodes to allow exploration of trading-off PV voltage and current during testing and evaluation of the prototype EHDS. To ensure a comparable harvested power across configurations, a total of 6 on-board photodiodes are integrated. Source-configuration can also be embedded into diode-pixels in a similar manner as CMOS active pixel sensor circuits [51] if on-chip harvesting sources are used.

5.1.2 LI-TB-MPPT: Boosted Power Estimation

The load-inclusive time-based MPPT (LI-TB-MPPT) block is developed based on a fully-digital boosted-power estimation metric to evaluate the total output power of the EHDS. The derivation of the metric is illustrated in Fig. 5.3. The ACTIVE periods (indicated by the switching NGT signal) and IDLE periods are marked as the first and second phases (T_1 and T_2), respectively. During the ACTIVE phase, the net flow of energy (E_1) comes solely from PMU boosted power (P_{boost}). This power is used to supply the load power (P_{load}) and

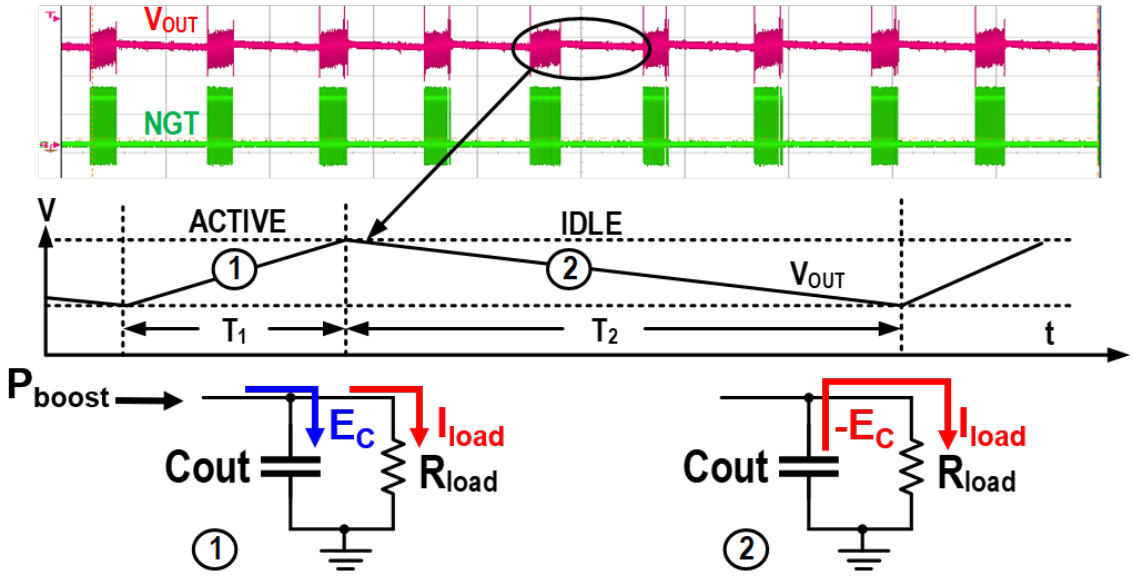


Figure 5.3: Boosted-power estimation metric derivation.

charge the output capacitor with enough energy to reach upper hysteresis (E_C). Assuming that the load current is consistent across this regulation cycle, the energy consumed by the load during the IDLE period (T_2) will be equivalent to the difference in capacitor-stored energy ($E_C = \frac{1}{2}C(V_{OUT,max}^2 - V_{OUT,min}^2)$) at the output. It can then be derived that the boosted power is proportional to $1/T_1 + 1/T_2$ when the hysteresis energy is stable:

$$E_1 = P_{boost}T_1 = E_C + P_{load}T_1 \tag{5.1}$$

$$E_2 = E_C = P_{load}T_2 \tag{5.2}$$

$$P_{boost} = E_C(\frac{1}{T_1} + \frac{1}{T_2}) \propto (\frac{1}{T_1} + \frac{1}{T_2}) \tag{5.3}$$

A shorter ACTIVE period means higher power is boosted to the output under the same load. Higher loads will decrease T_2 and increase T_1 under the same boosted power conditions. This metric is used as a reference when performing perturb and observe searching [46]

to tune aforementioned FSH fractions and oscillator frequency. Performing MPPT with a metric derived from the system output not only ensures maximum power delivered, but it also abides with the objective of relieving the need for high passives needed for source-based MPPT.

With MPPT performed at the system output, the EHDS no longer needs to maintain a strict confinement on the input voltage (as opposed to source-based MPPT). This allows us to co-design input capacitance along with inductance and frequency of the EHDS to reduce overall cost. Nevertheless, because the input voltage is no longer strictly confined, the proposed system also necessitates a different harvesting-window control compared to conventional EHDSs. Our proposed approach is explained in the following.

5.1.3 Fractional Sample & Hold: Harvesting-window Control

Passive filter dependence in prior approaches

Assuming an ideal boost regulator inductor current behavior (no parasitic resistance). It can be derived (with linear approximations for inductor current increase/decrease [29]) that the

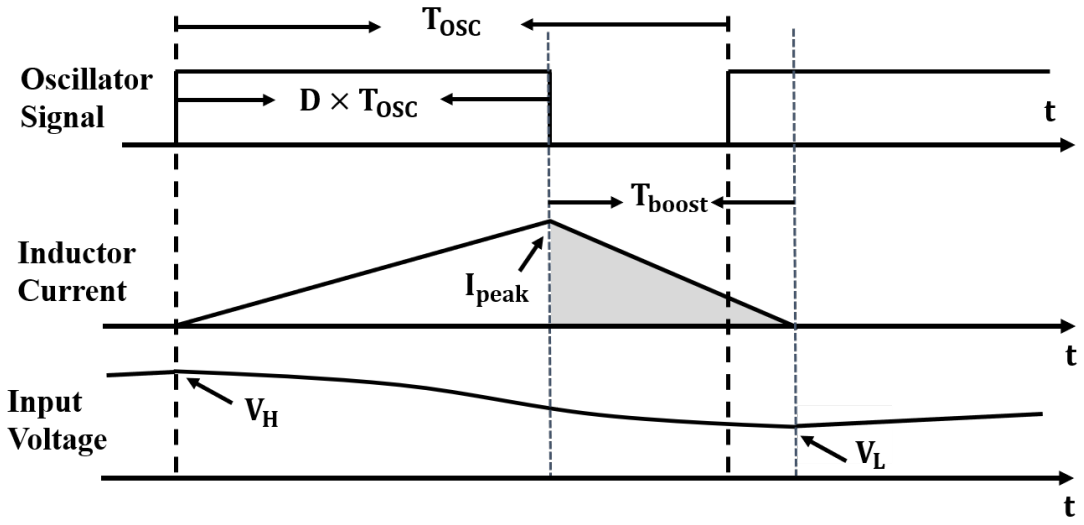


Figure 5.4: Current drawn from a single inductor pulse and drop in voltage.

charge drawn from a single inductor current pulse (Q_{pulse}) as shown in Fig. 5.4 is:

$$I_{peak} \approx \frac{V_H}{L} \times D \times T_{OSC} \tag{5.4}$$

$$Q_{pulse} = \frac{I_{peak}(D \times T_{OSC} + T_{boost})}{2} \tag{5.5}$$

$$T_{boost} \approx \frac{I_{peak} L}{V_{OUT} - V_H} \tag{5.6}$$

$$Q_{pulse} \approx \frac{V_H T_{OSC}^2 D^2}{2L}(1 + \frac{V_H}{V_{OUT} - V_H}) \tag{5.7}$$

Where V_H is the higher threshold of the input hysteresis (Fig. 2.4), L is the inductance, T_{OSC} is the clock period, D is the duty cycle and V_{OUT} is the output voltage of the PMU. To maintain input regulation within a fixed window, Q_{pulse} has to be less than the net input of charge from the source and the input capacitor hysteresis charge.

$$Q_{pulse} \leq I_{ph}(V_H) T_{OSC}(1 + \frac{V_H}{V_{OUT} - V_H}) + C_{IN}(V_H - V_L) \tag{5.8}$$

When the PV module strength is limited (by form factor, illumination, etc.), I_{ph} is low. Therefore, high inductance, input capacitance and/or fast clocks are required to maintain the above inequality. For example, with an input hysteresis of 20 mV from $V_H = 0.48$V to $V_L = 0.46$V, output voltage of 0.8V, I_{ph} of 1mA, and an 80% duty cycled clock at 100KHz, it can be approximated that $LC \geq 3.8 \times 10^{-9}$, and therefore $> 10\mu$ of capacitance and inductance are required.

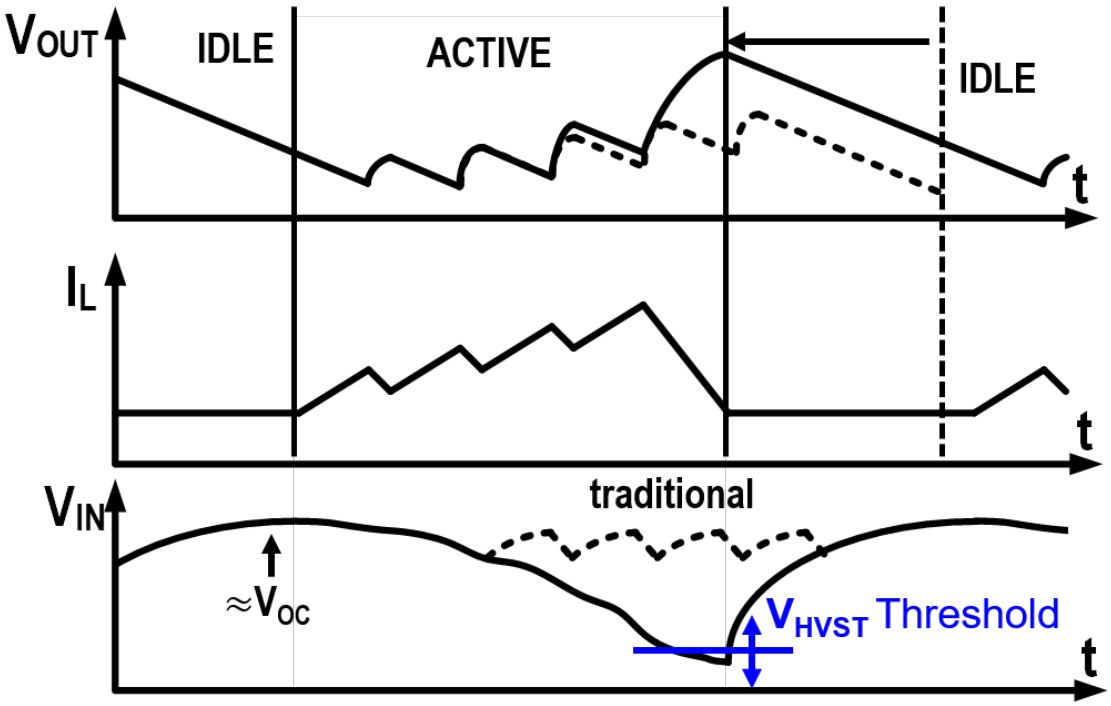


Figure 5.5: PFM inductor current and input/output voltage.

Proposed approach

The proposed EHDS increases the harvesting window and allows the PMU to continue drawing current until the harvesting voltage falls below a minimum threshold. This threshold is carefully controlled to ensure that the harvesting voltage can restore itself with harvested power when the PMU is IDLE. Fig. 5.5 shows an illustration of current and voltage waveforms during PFM boosting for the proposed system. The EHDS essentially "borrows" energy from IDLE periods to improve ACTIVE performance. The reduced ACTIVE time can be utilized with bias-gating techniques to reduce PMU power consumption [29]. Additionally, multi-pulse PFM operation (consecutive non-interrupted inductor-current build-up) can benefit conversion efficiency at increased load. Furthermore, lower C_{IN} and inductance are required because the system can tolerate a higher input voltage ripple and allows higher hysteresis charge eq. (5.7)-(5.8).

The waveform in Fig. 5.5 begins with the PMU in an IDLE state. During this phase,

V_{OUT} reduces with leakage and/or active current of loading modules and because the inductor current is close to zero, the harvesting node voltage (V_{IN}) increases with harvested power. For low load conditions (and/or high output capacitance), the idle period is long and V_{IN} can be restored back to V_{OC} with the harvested energy during PMU IDLE. However, as load increases, $max(V_{IN})$ drops as its charging is cut short by the following PMU ACTIVE period. This also affects the harvesting window applied to the source. Assuming an ideal PV harvesting source (zero series resistance), the harvested current can be expressed as [54]:

$$I_{hvst}(t) = I_{SC} + I_{pv0}(1 - e^{KV_{hvst}(t)}) \tag{5.9}$$

Where I_{SC} is the short-circuit current of the harvesting device and I_{pv0}, K are device and harvesting condition dependent constants that result in $I_{hvst} = 0$ @ $V_{hvst} = V_{OC}$. It can then be derived (by solving for $\partial V_{hvst}(t)/\partial t = I_{hvst}(t)/C_{IN}$) that the input voltage follows the following curve when the IVR is IDLE:

$$V_{hvst}(t) = \frac{-1}{K} ln(\frac{1}{I_{SC}}(I_{pv0} + (I_{SC} - I_{pv0})e^{\frac{-I_{SC}K(t+t_0)}{C_{IN}}})) \tag{5.10}$$

$$t_0 = (\frac{-C_{IN}}{I_{SC}K})(\ln(\frac{I_{SC}e^{KV_{min}} - Ipv0}{I_{SC} - I_{pv0}})) \tag{5.11}$$

Second, based on charge equilibrium at the harvesting node, the integrated value of $I_{hvst}(t)$ is equal to charge drawn by the inductor current summed with the hysteresis of stored charge in the input capacitor. We can thus derive the maximum input voltage as:

$$V_{max} = V_{OC} - \frac{1}{K}\ln(1 + (\frac{I_{SC}}{I_{pv0}}e^{KV_{min}} - 1)e^{\frac{I_{SC}KT_{IDLE}}{C_{IN}}}) \tag{5.12}$$

The same derivation can be done for TEG sources that present a linear I-V relationship

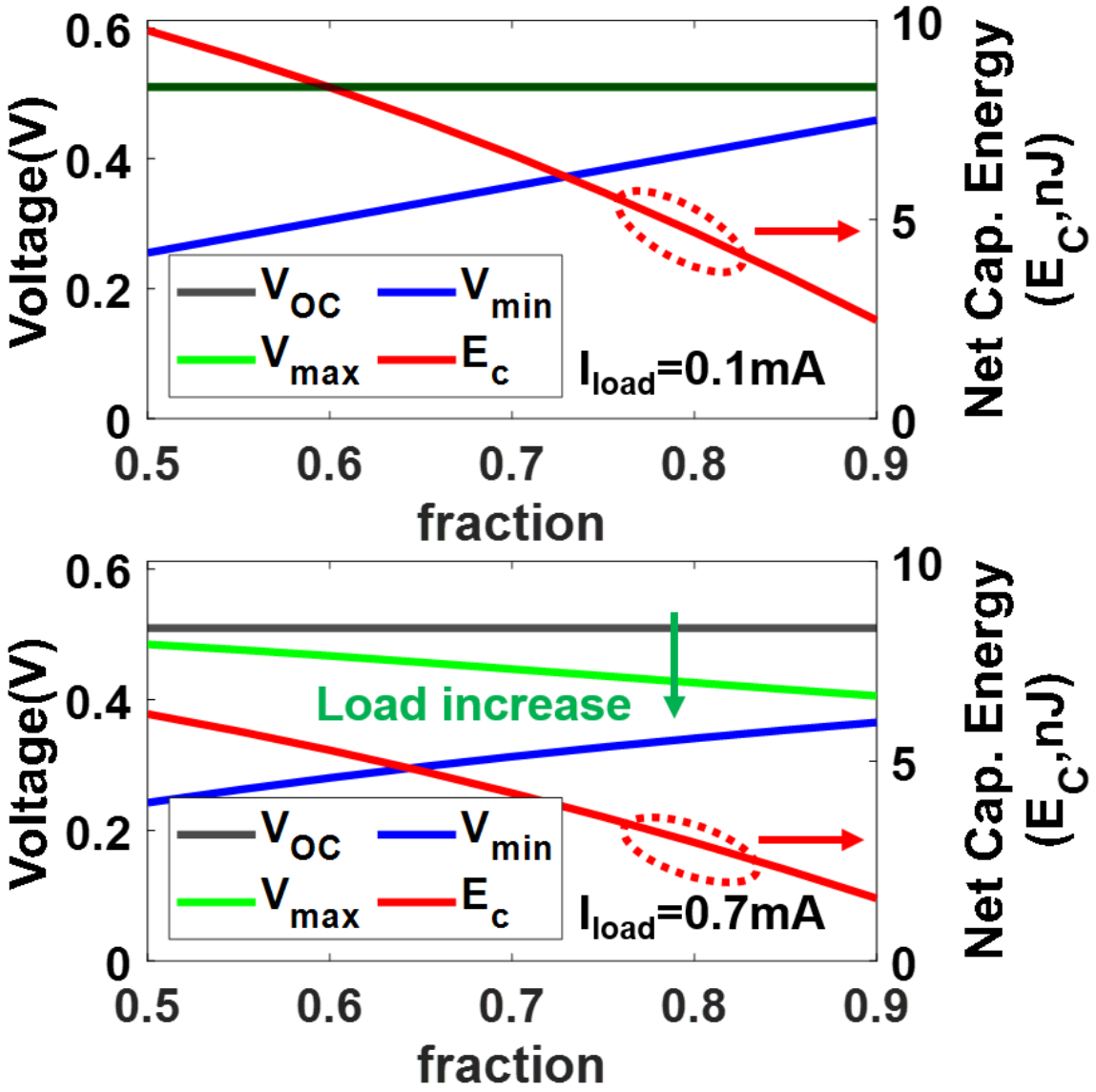


Figure 5.6: Maximum/minimum voltage and hysteresis energy for different fractions (V_{min}/V_{max}) at equilibrium for load current=0.1mA (top), 0.7mA (bot). ($V_{OC} = 0.51V$, $I_{SC} = 1mA$, $C_{IN} = 100nF$, $C_{OUT} = 1.1\mu F$).

without loss of generality:

$$I_{hvst,TEG}(t) = I_{SC}(1 - \frac{V_{hvst}(t)}{V_{OC}}) \tag{5.13}$$

$$V_{max,TEG} = V_{OC} - (V_{OC} - V_{min})e^{-\frac{T_{IDLE}I_{SC}}{C_{IN}V_{OC}}} \tag{5.14}$$

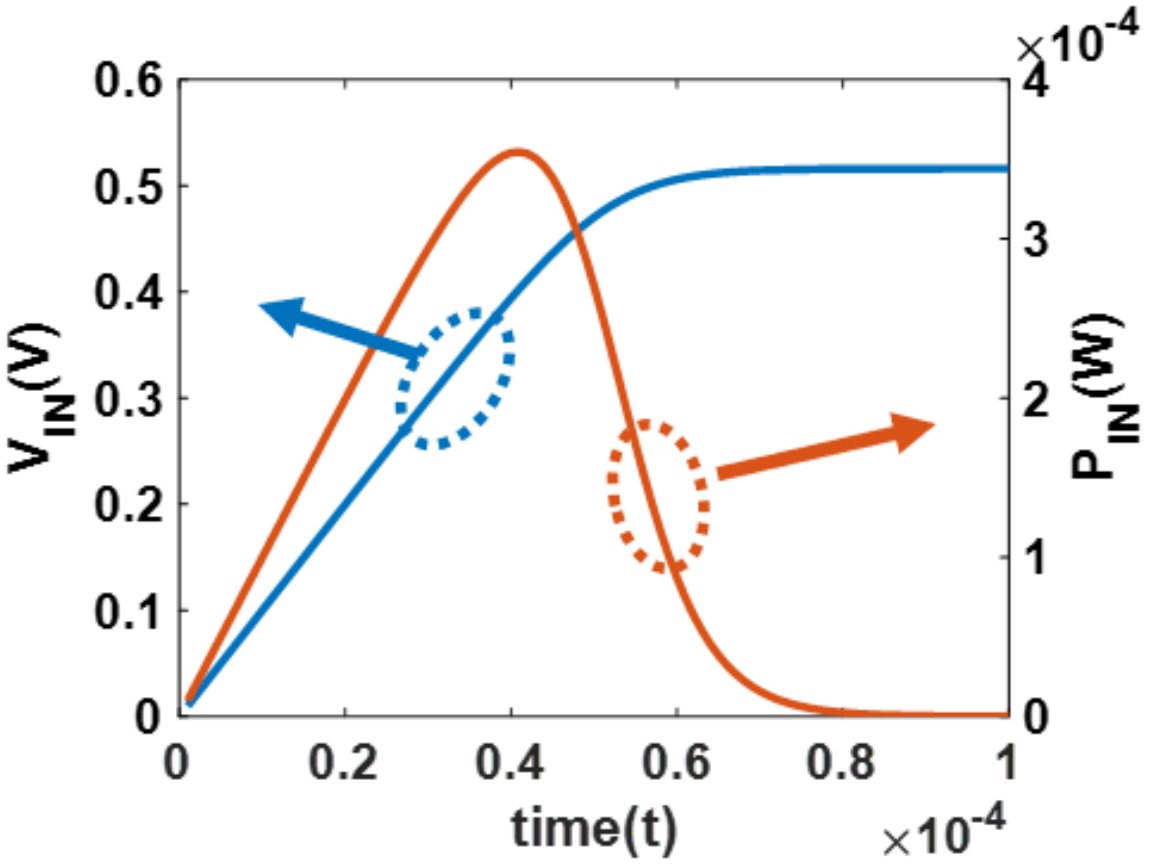


Figure 5.7: Transient of harvesting voltage (P_{IN}) and power (P_{IN}) for an ideal PV source when PMU is IDLE.

Continuing with the derivation with PV harvesting characteristics, another variable to be noted is the IDLE period (T_{IDLE}). T_{IDLE} is purely a function of the load current, output ripple and output capacitance because the IVR is OFF during IDLE periods. When the output hysteresis is maintained during DC-DC PFM operation, output ripple is controlled and T_{IDLE} is near constant. However, in the proposed scenario, output hysteresis is limited by the boosted charge from source hysteresis (as shown in section 4.5.1). Therefore, T_{IDLE} also changes with different fractions. For sake of simplicity, the following derivation assumes a linear decrease in T_{IDLE} with increased fractions to account for this effect. Substituting $V_{max} \times fraction$ for V_{min} in (5.12), we can then plot the source regulation metrics as shown in Fig. 5.6 when the system reaches equilibrium. It can be seen that the regulation window can be tuned by modifying the fraction. Furthermore, even when V_{max}

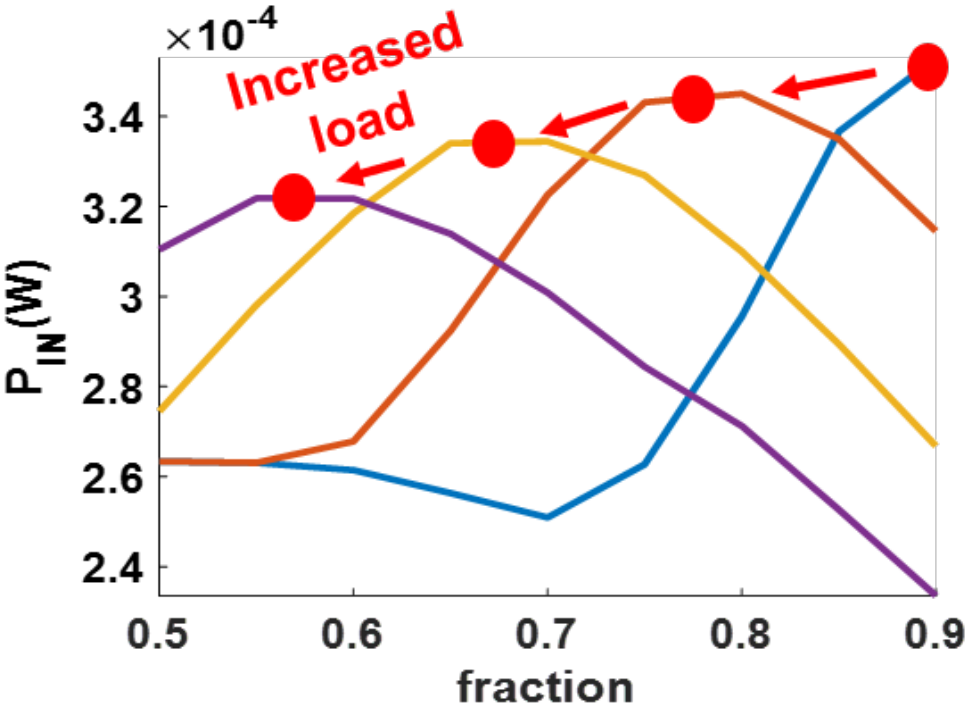


Figure 5.8: Shift in maximum input power for different fractions with respect to change in load.

no longer reaches V_{OC} when load is increased, the harvesting window can be readjusted by modifying FSH fractions.

Going back to the derived equation, (5.10), we can utilize the transient of harvesting voltage (Fig. 5.7) to also derive a transient of harvested power for the input source. This power-transient can then be used to approximate the average input power based on the change in harvesting windows for different fractions under load variations. This is plotted in Fig. 5.8. As observed, the peak input power shifts to different fractions as the load varies, and a constant fraction can lead to loss in input power and therefore harvesting efficiency. Traditional FOCV approaches neglect the impact of load and force-sample OCV conditions by either disconnecting the PMU [11] or using a dummy cell [40]. The former presents risks in power delivery (therefore requires multi- source/storage EHDSs), and the latter has large overhead. In the proposed EHDS, we address this challenge via integrating on-the-fly "fraction configure-ability" into a fractional sample & hold circuit that allows for

OCV-free MPPT tracking where load-sensing is directly performed with the LI-TB-MPPT circuit.

5.1.4 Configurable Switching Frequency: EHDS efficiency tuning

Switching frequency directly impacts PMU impedance. As the interface between harvesting sources and EHDS output, PMU impedance not only affects the quality of supplying loads but also harvesting conditions. Fig. 5.5 shows inductor current waveforms for high-frequency multi-pulse operation (black) and low-frequency single-pulse operation (red) [29].

Different techniques that perform frequency modulation for MPPT impedance matching, such as adaptive ON time [32], adaptive OFF time [55], and direct frequency/duty cycle tuning [19], have been proposed. However, these approaches rely completely on hysteresis regulation of the harvesting voltage, or use look-up tables and do not consider the impact on PMU operation.

When the optimal harvesting voltage (V_{MPP}) changes with input power, it also imposes a change in the conversion ratio that the PMU needs to maintain. This, along with changes in load demand, affects the conversion efficiency of the PMU [23]. One method to restore lost efficiency when the PMU undergoes variation is to allow frequency tuning.

It has been shown in prior work that oscillator frequency plays a critical role in determining PFM IVR efficiency [48, 29]. When switching frequency is manipulated to modulate harvesting conditions, it must also consider the change conversion ratio and conversion efficiency that it imposes and perform co-optimization between the harvesting source and the PMU to achieve maximum EHDS output power. Similarly, when load variations result in changes in PMU operation, its impact on harvesting conditions will need to be adapted.

The designed system implements a system-level MPPT for EHDSs that re-configures the oscillator switching frequency to compensate for efficiency loss due to the effect of both factors (load and V_{MPP} variations). This is done by embedding the frequency-tuning

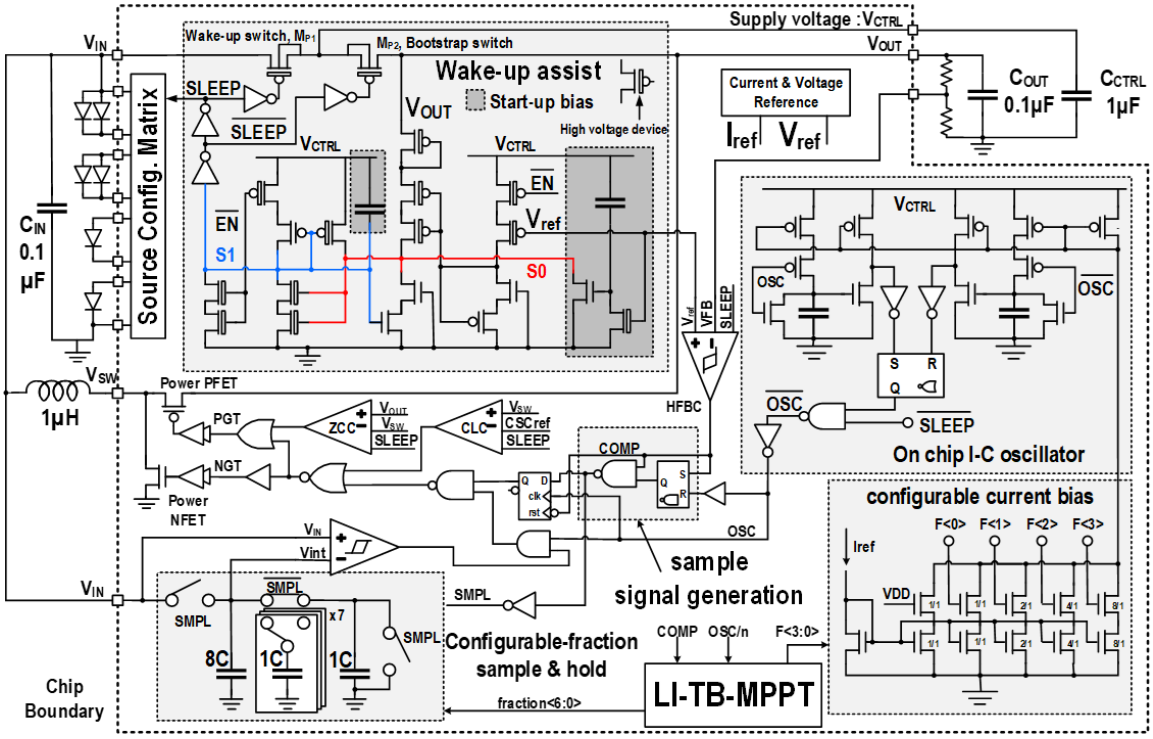


Figure 5.9: Detailed schematic of proposed system implementation.

loop within the output-based LI-TB-MPPT decision. Through this method, variations in both the conversion efficiency and harvesting efficiency are inherently considered during maximizing output power.

5.2 Implementation

This section will introduce implementation details of the proposed EHDS. Corresponding to Fig. 5.1, Fig. 5.9 shows a combined schematic of all analog circuits in the system to show their dependencies. The following will introduce the operation and design of each individual block in detail.

5.2.1 Wake-up Assist circuit

The wake-up assist circuit (Fig. 5.10) composes an analog latch that senses two voltages to determine the state of control power for the system. The reference voltage (V_{ref}) is sensed with a voltage detector circuit [11], which is followed by a second stage to detect

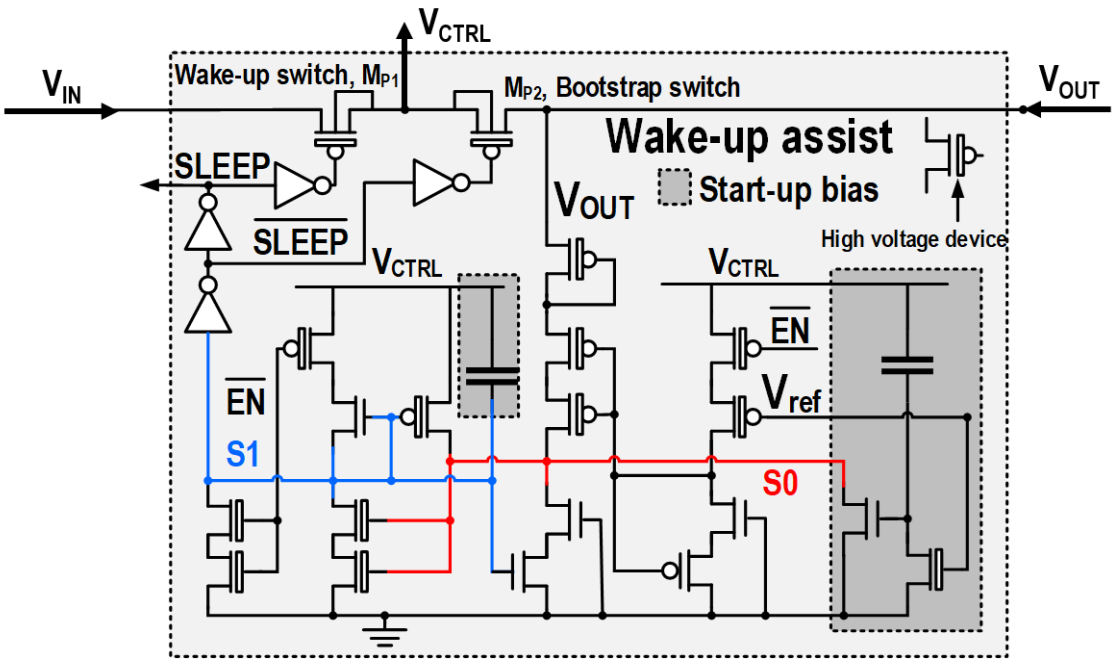


Figure 5.10: Analog wake-up assist (WUA) circuit schematic for robust wake-up configuration.

the output voltage of the EHDS. During cold-start, V_{IN} charges up first through harvested power from the input source. A portion of the power flows through P-N junctions of PMOS transistors and increases the control voltage. As V_{CTRL} increases, MOS capacitors within the highlighted start-up bias circuits initialize nodes S0 (red) to "ground", S1 (blue) to "V_{CTRL}" and connects V_{CTRL} to V_{IN} via wake-up switch M_{P1}. The two voltage detectors and output latch ensures that these values are maintained and S1 also closely follows the increase in V_{CTRL} to ensure that the digital SLEEP signal outputs a robust "1" even at low control voltages. This is a critical characteristic as the SLEEP signal is used to control digital logic, source configuration and bias gates of analog components. Any offset from the supply rail can propagate and amplify into incorrect configurations, especially at sub-threshold voltages (< 0.4V). The SLEEP signal is also used to: (1) place the regulator in the IDLE mode (bias-gate comparators and oscillator) to reduce V_{CTRL} power and prevent potential input voltage drop from premature switching activity, and (2) configures the PV diodes in series to increase V_{IN} (and the connected V_{CTRL}) during cold-start. Once both

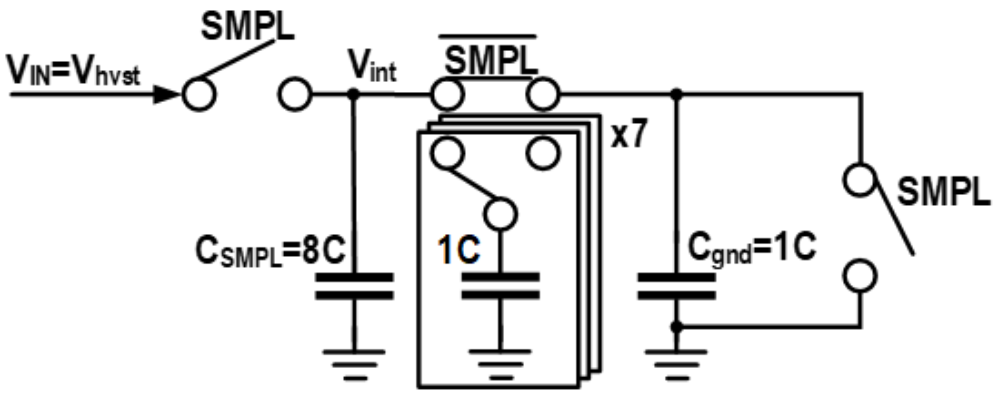


Figure 5.11: Sample and hold circuit with configurable fractions through capacitive charge sharing.

V_{ref} and V_{OUT} have become sufficiently high, SLEEP becomes low and the WUA connects V_{CTRL} to V_{OUT} (i.e., enter the bootstrap mode via bootstrap switch M_{P2}). After entering normal bootstrap operation, the regulator is enabled and the source is re-configured (to prevent over-voltage and reduce series resistance) with a low SLEEP signal. High voltage devices are selectively implemented between every path from V_{CTRL} to ground in the wake-up assist circuit to reduce standby power overhead (<15pW in simulation) and provide high threshold voltage levels.

5.2.2 Configurable Fractional Sample & Hold

The Fractional Sample & Hold (FSH) circuit is based on a charge-sharing sample and hold circuit. Fig. 5.11 shows a schematic of the FSH circuit implemented with MOS capacitors and transmission gate switches. The internal voltage (V_{int}) is the voltage that is held and sent to the PFM BR input comparator (Fig. 5.1) for harvesting window control. When the sample signal (SMPL) is high, C_{SMPL} is connected to V_{IN} and the grounding capacitor C_{gnd} is drained. When SMPL is low, V_{IN} is disconnected, the charge across C_{SMPL} and C_{gnd} are redistributed, and V_{int} settles at a fraction of V_{IN}, determined by the capacitance ratio between C_{SMPL} and C_{gnd}. Compared to resistor dividers, this topology has the advantage of low static power consumption when providing sufficiently fast sampling speed.

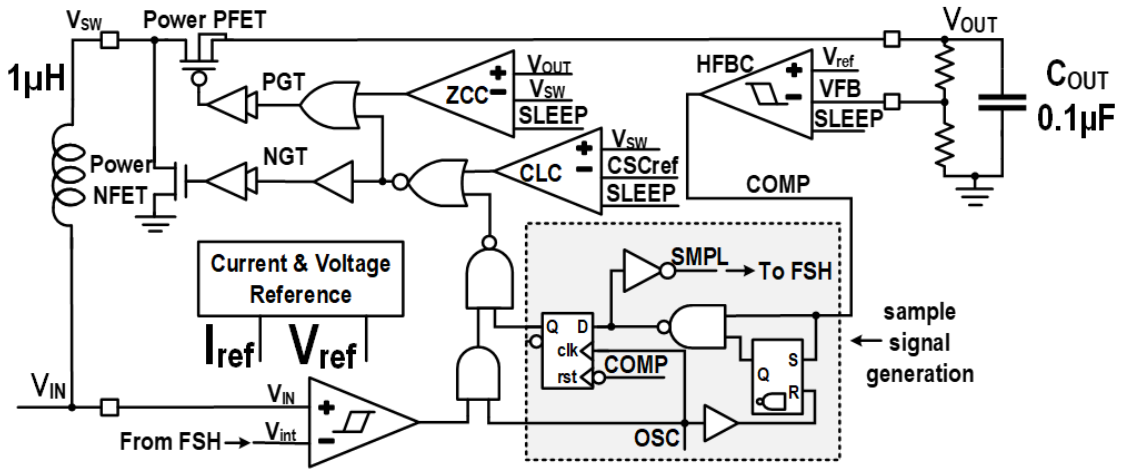


Figure 5.12: Main control path with embedded sample (SMPL) signal generation.

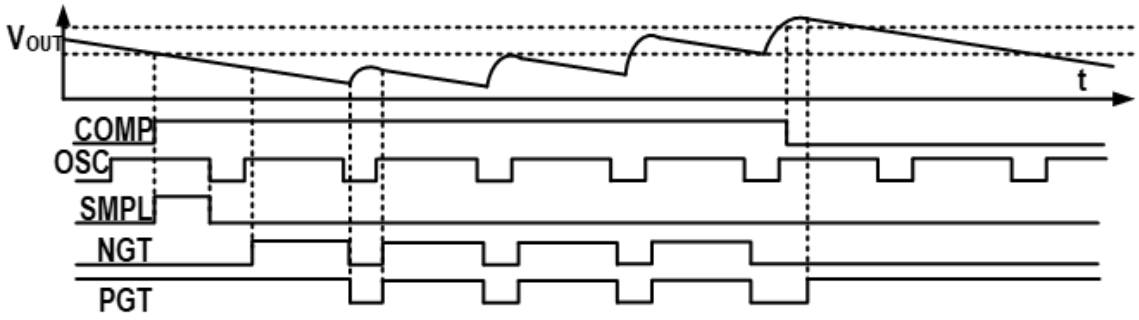


Figure 5.13: Waveform for sample signal generation in the PFM control path.

To allow fraction configure-ability, 7 MOS capacitors can be switched between C_{SMPL} and C_{gnd} to support eight different configurations of sampling fractions (Fig. 5.6). The minimum fraction that can be applied to the sampled voltage occurs when all configuration capacitors are connected to C_{gnd}, and the maximum fraction occurs when all capacitors are connected to C_{SMPL}. This flexibility allows the FSH to perform tracking while eliminating the area [11] and disconnection [40] overhead of traditional FOCV approaches. The configuration is updated every regulation cycle by the LI-TB-MPPT circuit to ensure input voltage fluctuations can be tracked on-the-fly, even when increase in load reduces the maximum input voltage as explained in subsubsection 5.1.3.

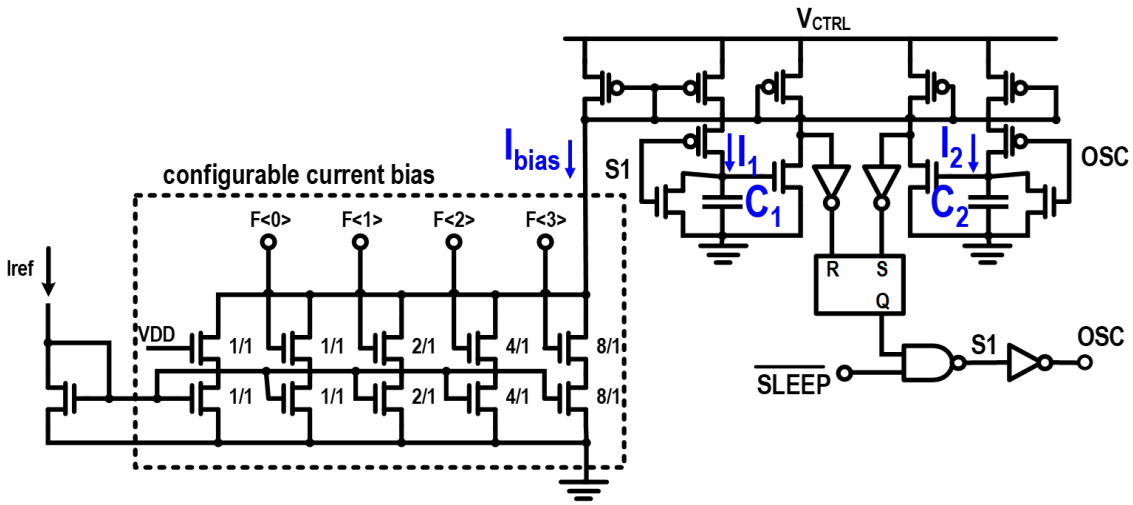


Figure 5.14: Configurable frequency oscillator schematic.

5.2.3 PFM control path

The main control path is shown in Fig. 5.12. Output regulation is performed by the hysteresis feedback comparator (HFBC), which compares a resistor-divided feedback voltage with the on-chip V_{ref}. The input hysteresis comparator output overwrites oscillator clock to stop the PMU and to prioritize source voltage regulation before the OSC signal is passed to later stages. A zero-current comparator (ZCC) and a current limit comparator (CLC) close the power PFET and power NFET, when the inductor current falls below zero or surpasses a pre-designed current limit, respectively. This is done by comparing the switching node voltage V_{SW} with V_{OUT} and another on-chip reference CSC_{ref} in a similar manner as prior works [29]. The CLC senses inductor current through an internal NFET and resistor that is placed in parallel to the low-side power NFET. The current limit is designed to be approximately 20mA to prevent imposing extensive voltage drop on the input capacitor. Additionally, sample signal generation is embedded in the PFM control path to create a "SMPL" signal before any switching activity begins. The flip-flop blocks OSC signal propagation until sampling is completed (Fig. 5.13).

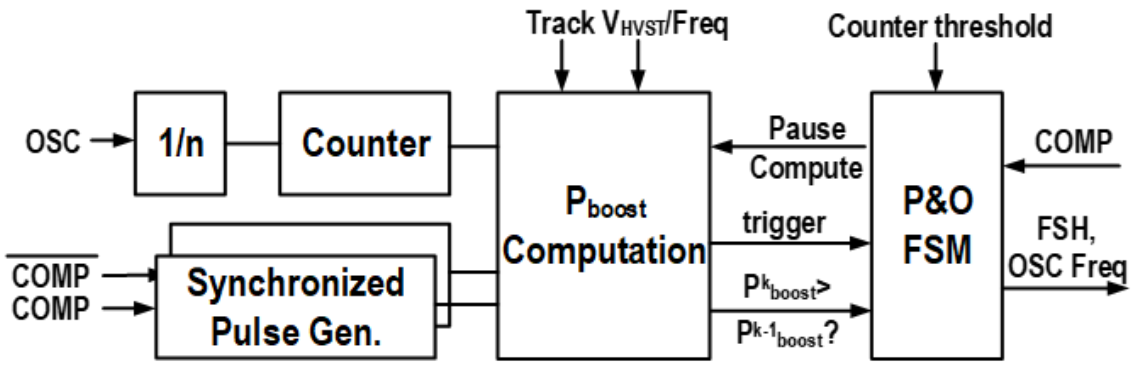


Figure 5.15: LI-TB-MPPT block diagram.

5.2.4 Configurable frequency oscillator

A configurable-frequency current-capacitor oscillator is designed for creating switching signals for the PMU and the system clock. Different frequencies can be made though changing the configurable current bias. The advantage of the current-capacitor design is that it delivers a stable duty-cycle robust to process-voltage-temperature variations, which is determined by the ratio of mirrored currents I_1, I_2 and capacitors C_1, C_2 [29]. The impact of frequency variations [56] can be countered through allowing MPPT to tune configurations for the bias current branch when it tracks for maximum output power.

5.2.5 Load Inclusive Time Based MPPT

A schematic of the LI-TB-MPPT implementation is shown in Fig. 5.15. The MPPT circuit uses a divided clock from the IVR oscillator to achieve a balanced 50% duty cycle for computation. Also, this allows enough computation time for core combinational logic that computes power metrics to complete. The same clock is used to create synchronized pulses at the rising/falling edges of the "COMP" signal that indicate the boundary between ACTIVE and IDLE periods. The operation of the tracking cycle is illustrated in Fig. 5.16. The digital synchronization block creates pulses that trigger computation only at rising and falling edges of the COMP signal. The P_{boost} computation engine logs counted clocks during T1 and T2 (as N_{ON} and N_{OFF} in the figure) and computes P_{boost} from these values. Dig-

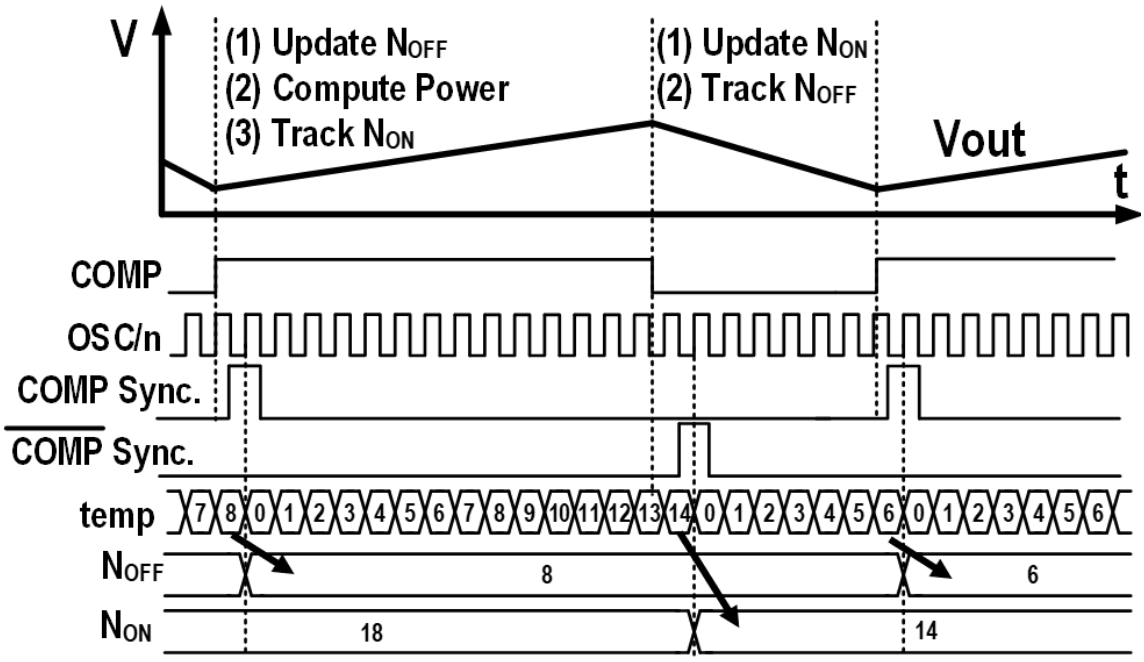


Figure 5.16: MPPT operation waveform.

ital threshold checks (for counter overflow and load-change re-triggering) are implemented in the MPPT finite state machine before the computed "higher power: $P^{k}_{boost} > P^{k-1}_{boost}$" decision is fed to the perturb and observe finite state machine (P&O FSM). In the event of a load-step, not only does the PMU conversion efficiency change with the IDLE period, the harvesting voltage re-charging is also affected as discussed in subsubsection 5.1.3. A threshold of $N_{OFF}/8$ is applied for resetting tracking registers under such scenarios. Because we are using a time-based approach, additionally resets and processing steps are coded into the main P_{boost} computation block to adapt to cases when frequency is modulated by the P&O FSM. Digital threshold checks (for counter overflow and load-change re-triggering) are implemented in the MPPT finite state machine (Fig. 5.17) before the computed "higher power" decision is fed to the perturb and observe finite state machine (P&O FSM). The P&O FSM modulates the FSH fraction and oscillator frequency to search for an operating point that minimizes boosting time at given load.

The P&O FSM implements the following algorithm for hill-climbing: 1) The FSM first attempts a change in EDHS configuration; 2) The output power of the EHDS is compared

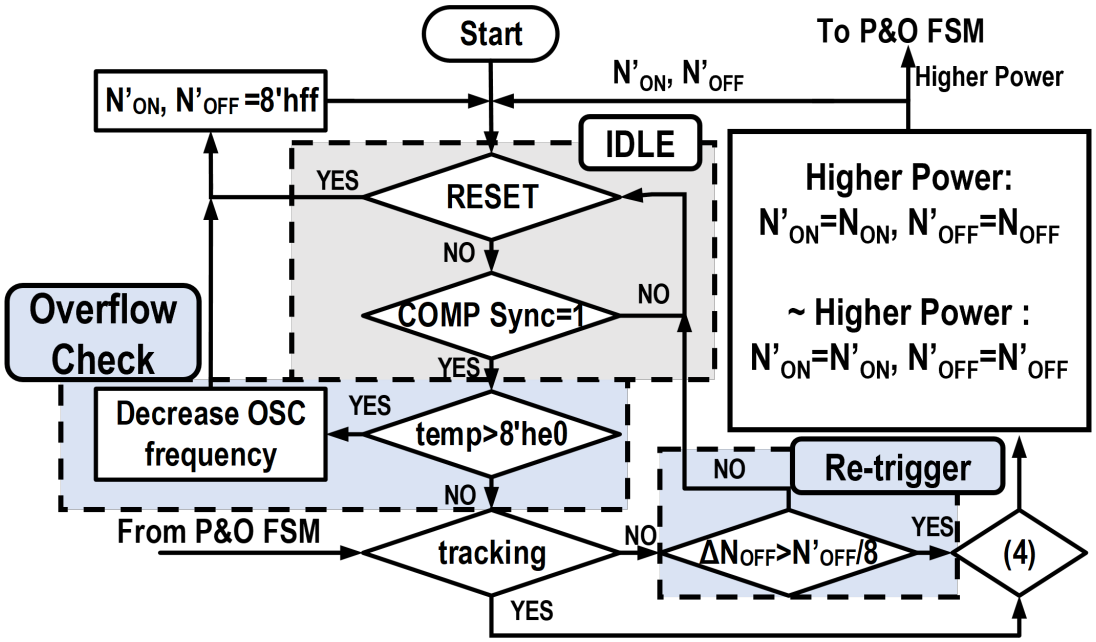


Figure 5.17: P_{boost} computation flow diagram with digital threshold checks.

to prior states with the power-evaluation engine; 3) If "higher power" is observed, the FSM continues changing EHDS configurations in the same direction and re-evaluates. If not, the system converges back and attempts a different change. Decisions to modulate the FSH fraction and oscillator frequency are updated at the beginning of every output regulation cycle during the search for an optimal operating point for the EHDS. To prevent extensive computation and "ringing" activity around a located MPP, the P&O FSM allows only three encounters of a lower power condition and pauses tracking activity until 1) triggered by a "load change" condition that is integrated into the main block 2) after a number of regulation cycles has passed, where the counter threshold is defined through the serial-to-parallel interface (SPI) for testing purposes.

We also simplify the boosted power metric for efficient computation because it is not necessary to obtain the absolute value of the metric for hill-climbing MPPT. Instead, only a single-bit decision is required: whether the computed metric of one state is higher than another. Our first step is to avoid division operations that are used in (5.3), as they are

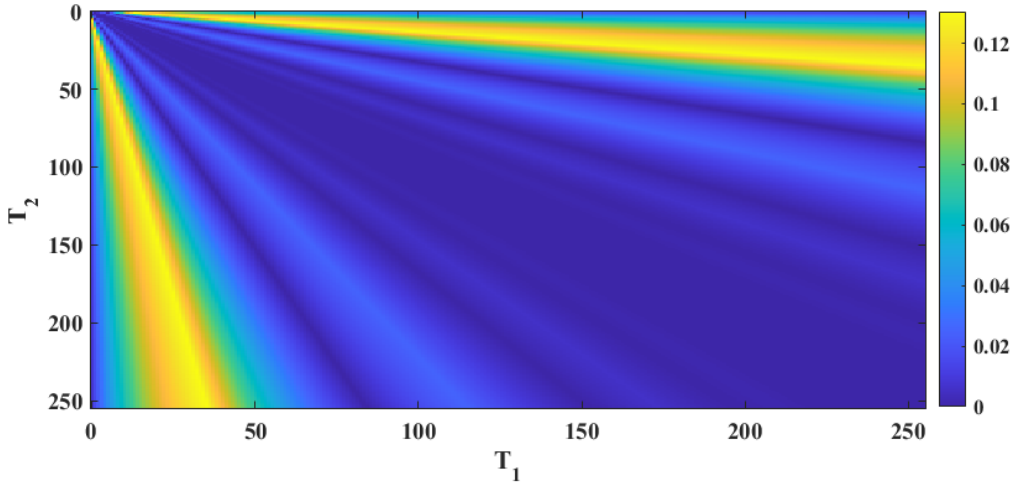


Figure 5.18: Relative difference ratios from ideal computation of y'^2/x to implemented quantized computation.

computation heavy.

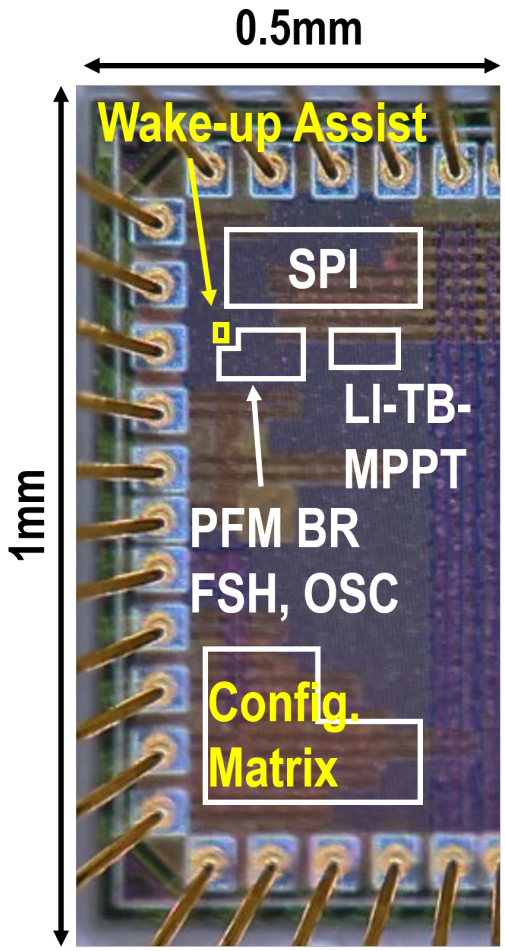
$$P_{boost} > P'_{boost} \iff (\frac{1}{T_1} + \frac{1}{T_2}) > (\frac{1}{T'_1} + \frac{1}{T'_2}) \tag{5.15}$$

$$(5.15) \implies T'_1 T'_2 (T_1 + T_2) > T_1 T_2 (T'_1 + T'_2) \tag{5.16}$$

Next, we perform a second step of conversion by computing intermediate values of $x = (T_1 + T_2)/2$ and $y = (T_1 - T_2)/2$. To prevent negative values, initial comparison of T_1 and T_2 is performed and the larger value is re-assigned to T_1 for computation. substituting x and y into (5.16) and rearranging the inequality, we can reach (5.17):

$$(5.16) \implies x' - y'(\frac{y'}{x'}) > x - y(\frac{y}{x}) \tag{5.17}$$

The multiplication and division in $y(y/x)$ is addressed by quantizing the division into powers of $1/2$ and performing bit-shifting for multiplication. The error rate introduced by this binning (with 5% tolerance) is 2.6% for 8-bit timing information, with the majority of errors lying in corner cases that have very unbalanced ACTIVE and IDLE periods which



General	
Technology	65nm
OSC(@1V)	6MHz~20.8MHz
Wake-up Assist	
Area	0.000322mm^2
FSH	
Area	0.000133mm^2
Configuration Matrix	
Area	0.0476mm^2
Configurations	3
LI-TB-MPPT	
Area	0.0032mm^2
Clock Division	1/8
Counter Width	8 bits
Search Algorithm	Perturb & Observe

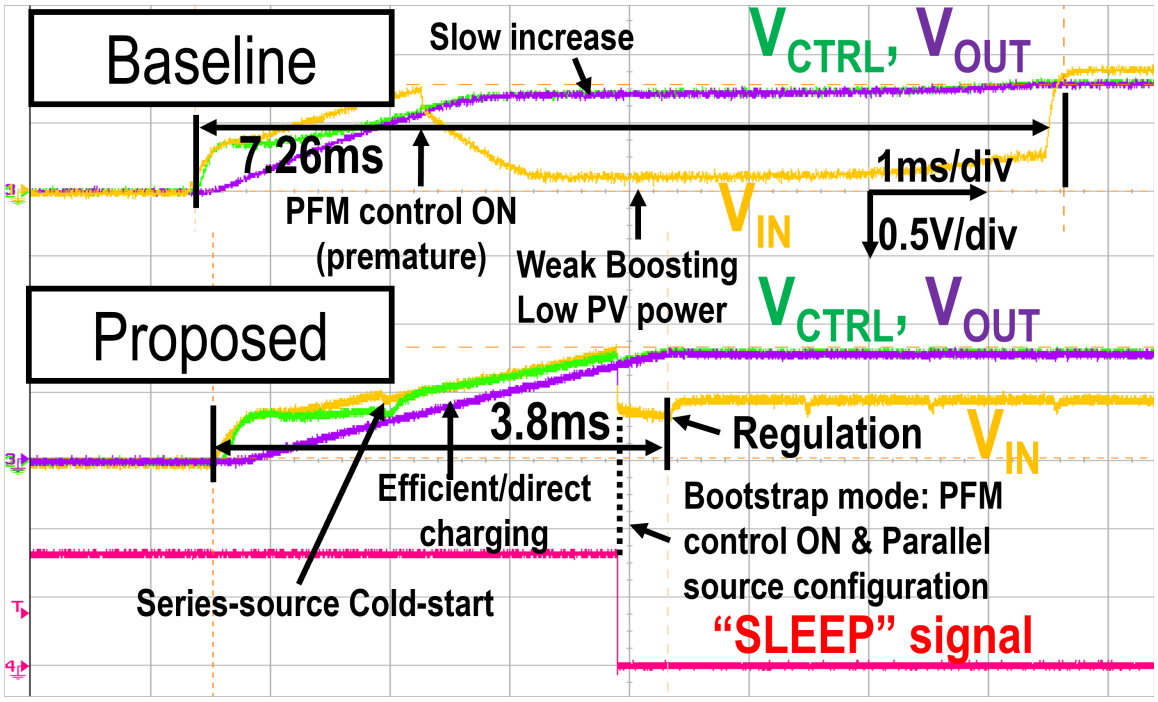
Figure 5.19: Chip micrograph and specifications.

rarely occur in implementation (Fig. 5.18).

An exhaustive search of the total number of errors that can be propagated to the final decision of $P_{boost} > P'_{boost}$ shows lower than 0.0095% error rate. To prevent these cases from occurring, digital filters can be applied similar to the ones shown in the following section. The synthesized area can be reduced by $2.2\times$ with observation registers added. Without testing harness, the projected area reduction can be up to $6.1\times$.

5.3 Measurement Results

A test-chip is fabricated in 65nm CMOS, packaged in LCC44, and integrated on-board with PV diodes (VBPW34S). A chip micrograph with the functional blocks marked is



Configuration	Wakeup time(@6klux)	Lowest wakeup intensity (klux)
Baseline	7.26ms	6 (3-stack), 17 (2-stack), failed (1-stack)
Proposed	3.8ms	1

Figure 5.20: Measurement waveforms for input voltage, output voltage, control voltage and SLEEP signal.

shown in Fig. 5.19. The integrated EHDS uses a 1µH inductor, an input capacitance (C_{IN}) of 0.1µF, a control voltage capacitance (C_{CTRL}) of 1µF and an output capacitance (C_{OUT}) of 0.1µF. Higher capacitance is added on the control voltage, rather than the output node, to reduce voltage drop from charge sharing with output capacitance when the PMU is switched into bootstrapped mode. Both will serve as decoupling capacitance for V_{CTRL} and V_{OUT} regulation once the system wakes up. The measured switching frequency of the oscillator is 6MHz to 20.8MHz at V_{CTRL}= 1.0V, with an average duty cycle of 80%. The relatively high frequency enables reduction in both inductance and C_{IN}.

5.3.1 Wake-up Assisted Cold-start

Fig. 5.20 shows measurement waveforms of bootstrap cold-start with and without the proposed wake-up assist circuit. During baseline experiments, the testing harness overwrites the SLEEP signal and the source matrix is powered externally to ensure a stable configuration is asserted. On the other hand, only the testing harness is powered externally (for observation) during the measurement for the proposed approach and everything else is free-running from harvested power. Even with this slight disadvantage, the proposed wake-up assisted cold-start presents superior performance. To compare with the autonomous source-stacking enabled by the WUA, the baseline waveform shown is measured also with a stack-of-three source configuration. In both experiments, V_{CTRL} and V_{OUT} rise with V_{IN} increase initially through drain-to-body P-N junctions of the Wake-up switch (Fig. 5.10) and the Power PFET (Fig. 5.12). Low input voltage observed in the baseline measurements that arise from premature switching activity restricts inductor current build-up and results in inefficient boosting. The consequent long-ACTIVE periods further leads to extensive current drawn, even lower input voltage, and, ultimately, slow increase in both V_{CTRL} and V_{OUT}. From this example, we can see the benefit of connecting V_{CTRL} to V_{IN} for accelerated charging during cold-start. The waveform also clearly shows the point where cold-configuration of the harvesting matrix occurs autonomously. With biasing gating of unused PFM control blocks, the bootstrap current of the PMU can be reduced from 42µA active current (measured from an always-ON state) to 4 µA leakage. After the WUA senses that the EHDS is ready for bootstrapped operation, the SLEEP signal also re-configures the harvesting source into parallel configurations for bootstrapped operation. Overall, the system achieves 2× reduction wake-up time (7.26ms→3.8ms) by: 1) enabling robust cold-configuration of harvesting sources in series to create high voltage, 2) direct/efficient charging of control voltage from the input source, 3) avoiding weak-boosting periods before V_{CTRL} reaches nominal operation voltage completely, and 4) minimizing PMU power with bias-gating during cold-start. We also measure that the minimum light intensity needed is

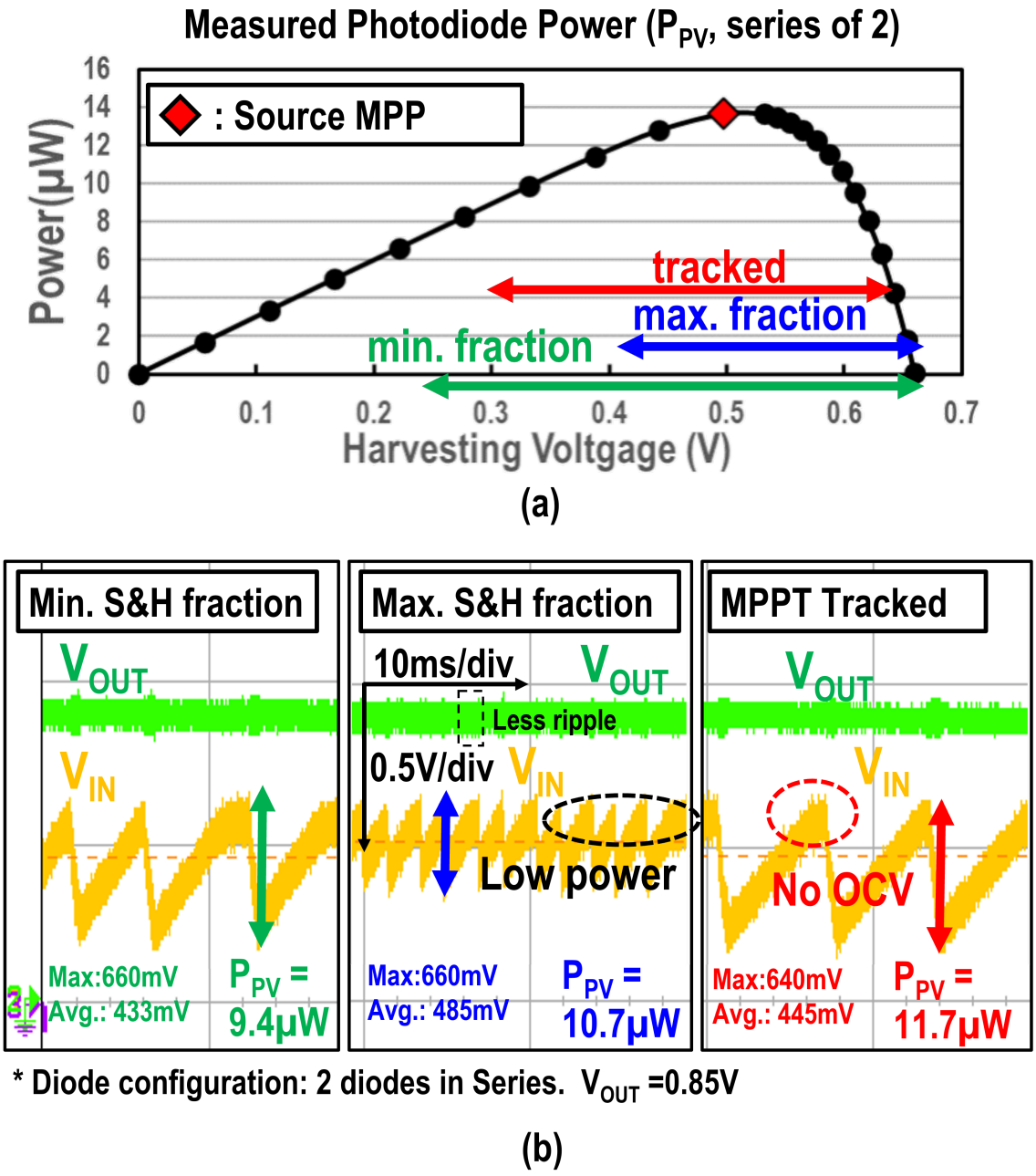


Figure 5.21: Measurement waveforms for input voltage with fixed fractions (open-loop) v.s. with MPPT-tuned fractions (closed-loop). (a) DC Power-voltage. (b) Transient measurements.

reduced by at least 6× with the proposed approach.

5.3.2 Fraction tuning with LI-TB-MPPT

Fig. 5.21(a) shows the PV power as a function of harvesting voltage when harvesting under roomlight with the source matrix configured in a stack of 2. Fig. 5.21(b) shows the input and output (regulated at 0.85V) waveforms when fractions are fixed at minimum, maximum and when it is tracked by LI-TB-MPPT. As explained in subsubsection 5.1.3, we can observe that different fractions result in different V_{min} and V_{max} pairs when the system reaches equilibrium. Therefore, the harvesting window is successfully controlled by controlling sample and hold fractions in the FSH circuit. Measurement waveforms with minimum and maximum fractions acquired by overwriting MPPT decisions with the testing harness are compared to when closed-loop tracking results. For a low fraction (with more capacitors connected to C_{gnd}, Fig. 5.11), the PMU is allowed to boost more charge during ACTIVE, which results in a higher ripple in the output voltage, and longer IDLE periods when V_{IN} charges back to V_{OC}. For a high fraction, PMU boosting is cut short by the input comparator and less drop in V_{IN} is observed. This also reduces the output voltage spike and ripple. It can be seen that both minimum and maximum fractions harvest from voltages where PV diodes produce low power due to low voltage ($<$0.4V) or low current (@$>$0.6V). Allowing the LI-TB-MPPT to search for an optimum setting avoids such conditions and up to 9% improvement in measured input power is observed.

5.3.3 Frequency tuning with LI-TB-MPPT

Fig. 5.22 shows transients of the LI-TB-MPPT re-tuning oscillator frequency on-the-fly. The frequency range of the configurable oscillator (6MHz to 20.8MHz) has been designed for two reasons. The first is to ensure the PMU can enter multi-pulse operation at high loads for improved efficiency. The second is to limit the input voltage drop (with only 0.1µF input capacitance) from inductor current pulses when the harvested power is low. This experiment is conducted in a two-step process to prevent initiating a re-trigger event as shown in Fig. 5.17. Fig. 5.22(a) represents the first step where no external load is applied

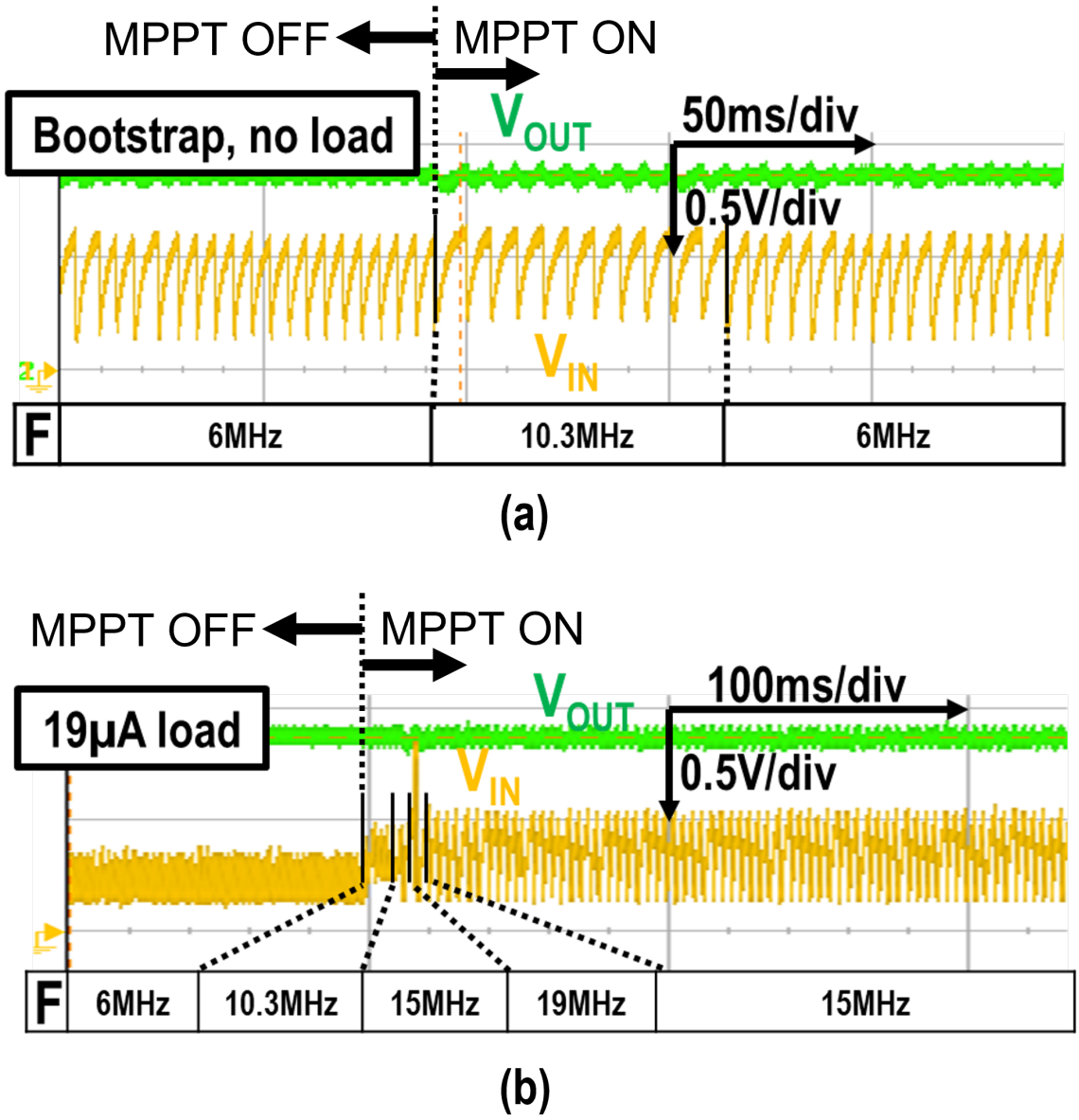


Figure 5.22: Measurement waveforms for input voltage with frequency tuning. (a) Self-powered. (b)19µA load. (F is the switching frequency of the PMU.)

and the EHDS supplies itself with the power boosted from photodiodes that are powered with room light. We can observe that although the EHDS attempts to increase the frequency (F=6MHz→10.3MHz) initially, it converges back after a few regulation cycles as the P&O algorithm finds that the increase in frequency does not provide significant benefit in increasing system performance. Fig. 5.22(b) also initializes the EHDS with F=6MHz in open-loop before MPPT tracking is enabled, except in this case, a current sink applies

19 μA load on the output node of the EHDS. The increased load results in shorter IDLE periods and a drop in the input voltage when the frequency is fixed at a configuration of F= 6MHz. When the MPPT is enabled, the EHDS auto-selects a configuration of F=15MHz after 20ms.

It can be observed that the P&O search with frequency configuration avoids applying low-voltage biasing conditions to the harvesting source, thus increasing robustness of EHDS operation. Although the same output power is delivered when regulated at the same load, a separate experiment demonstrates that the proposed MPPT approach increases the maximum load/power, at which output regulation is maintained, by 10% (40μW $\rightarrow$ 44μW) under an input intensity of 6klux. Additionally, compared to asynchronous FOCV sampling [18, 40] where tracking response time depends on the sampling frequency, an advantage of integrating sampling into the PFM control path is that input fluctuations can be tracked every regulation cycle and LI-TB-MPPT ensures that output variations can be tracked within a few regulation cycles **without needing to enter OCV conditions.**

Fig. 5.23 shows the measured efficiency and PMU power consumption across different loads when the switching frequency is maximum, minimum, and tuned by LI-TB-MPPT. The IDLE frequencies for the first two cases are the same as their active frequencies (F_{active}), but are observed to be auto-selected as 6MHz across MPPT-tuned measurements. We can observe that both efficiency and power increase with load for all three cases. Although lower frequency reduces power consumption of the PMU for improved end-to-end efficiency at low load, higher frequency produces higher efficiency at high load by reducing ripple loss from spurious single pulse boosting. By allowing the LI-TB-MPPT circuit to modulate the converter frequency during ACTIVE and IDLE periods, MPPT-tuned results always present maximum efficiency. A peak end-to-end efficiency of 74.9% is observed at 1.5mA load current, which is 2.7% and 3.1% higher than both fixed-frequency configurations.

Fig. 5.24 shows the LI-TB-MPPT circuit modulating frequency at different input volt-

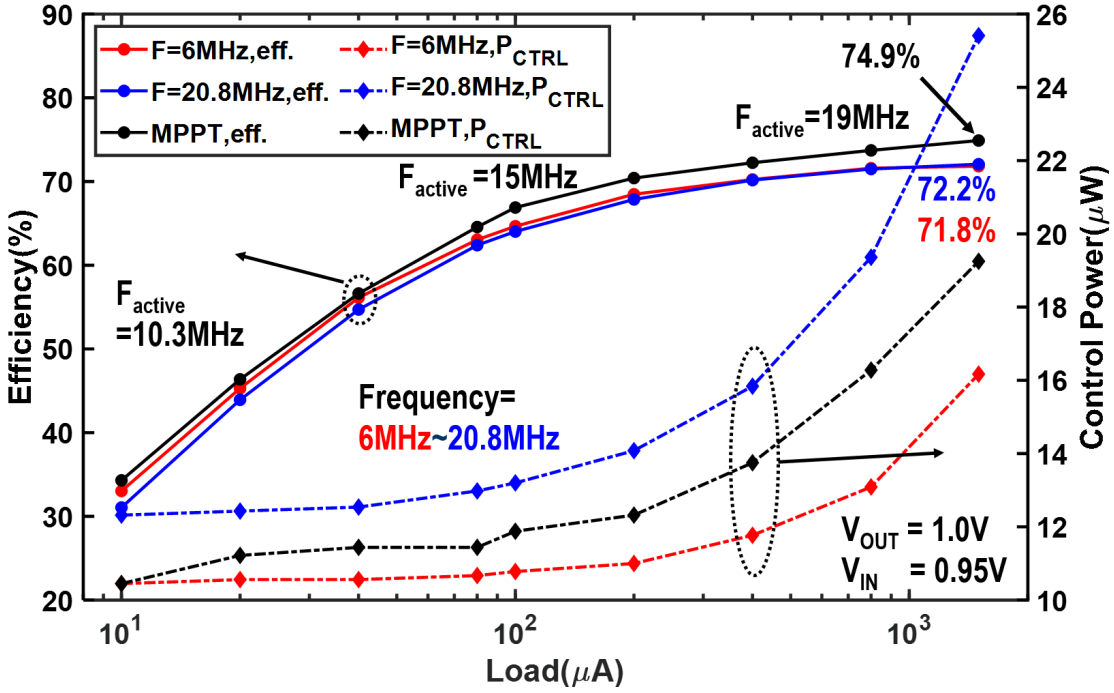


Figure 5.23: Measured end-to-end efficiency and system power for MPPT tracking at different loads. (F_{active} is active switching frequency of PMU, controlled configuring current bias in Fig. 5.14 through LI-TB-MPPT.)

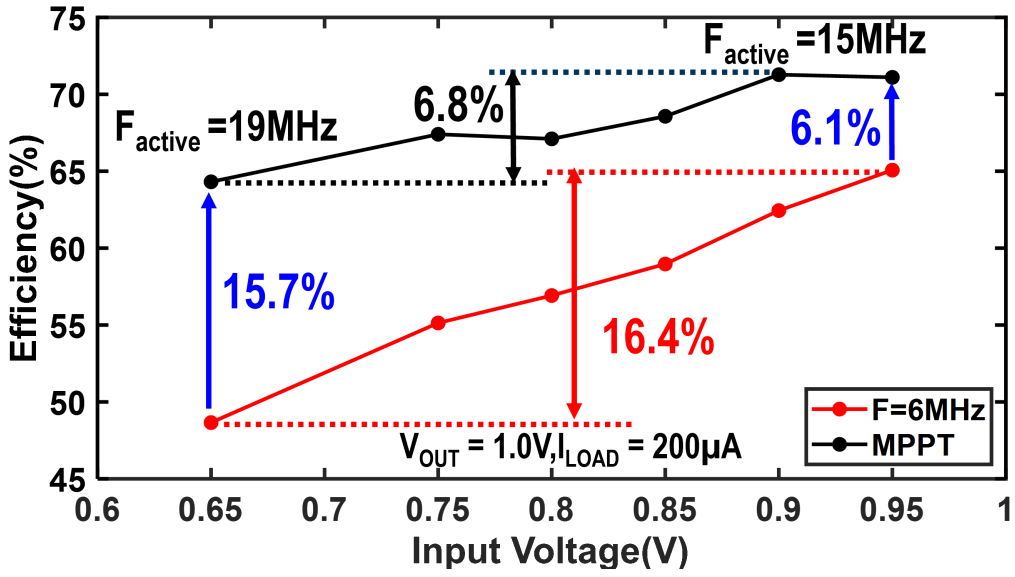


Figure 5.24: Measured end-to-end efficiency at different input voltages.

ages. A change in input voltage not only changes the conversion ratio, but also inflicts a direct change in the inductor current slope. The impact of this effect is especially high

when the frequency is low as the peak inductor current will be limited by the input voltage in single-pulse operations. Therefore, an increase in frequency is often needed to restore the "boosting ability" and efficiency of the PMU as input voltage decreases. We can observe an efficiency improvement between 6.1% and 15.7% (blue) when the active frequency is tuned by the LI-TB-MPPT circuit. The variation in efficiency across input voltage is also reduced, from a 16.4% change (red) to 6.8% change (black).

5.3.4 Comparison with prior works

Table 5.1 shows a summary of the EHDS with the designed chip compared with state-of-the-art EHDS implementations in existing literature. This work achieves a peak conversion efficiency of 74.9% with an input capacitance of 0.1 μF and an inductance of 1 μH. While prior works have demonstrated over 80% end-to-end efficiency, it can be seen from the table that these were achieved with passives that are much higher in value. It has been shown in prior work that increased inductance can benefit conversion efficiency [27]. Fig. 5.25 shows a breakdown of loss components for our EHDS and their impact on the end-to-end efficiency. This breakdown has been constructed based on a PFM-transient loss model [48] and modified to capture the input harvesting window control specific to the proposed EHDS. The total loss due to all the control circuits (i.e., total current drawn from V_{CTRL}) is measured as 31.5 μW, which includes 10.38 μW (9.13 μW due to leakage) for the LI-TB-MPPT and 1.94 μW for the configuration matrix. Its contribution to total loss is included in the model separately as "Bias" power and "Chip Leakage". The conduction loss, switching loss, and board leakage are computed based on both measurement values (clock frequency, duty cycle, output hysteresis, feedback potentiometer, etc.) and simulation data (R_P, R_N, driver slew-rate and switching energy, etc.). By including the non-ideal loss components characterized from both measurement and simulated data, we can see that the modeled end-to-end efficiency matches the measurement results shown in Fig. 5.23. From the modeled loss breakdown, we can observe that the conversion efficiency

Table 5.1: Comparison to state-of-the-art EHDSs

Metric	[4]	[27]	[39]	[18]	[11]	[19]	**This Work**
Technology	350nm	180nm	180nm	180nm	180nm	180nm	**65nm**
Converter Scheme	PFM	DCM	PFM+PSM	BFHC	DCM	DCM	**PFM**
Input Capacitance	47µF	1µF	10µF	-	-	-	**0.1µF**
Other Capacitance	15µF	0.2µF	30µF	-	-	1µF	**1.1µF**
Inductance	22µH	47µH	10µH	82µH	47µH	100µH	**1µH**
Frequency	31.2kHz	12.8Hz	10kHz	30kHz	30kHz	8kHz	**6MHz-20.8MHz**
Maximum Efficiency	83% @1.5mW	55% @1.2nW	83% @90µW	84% @67µW	89% @50µW	80% @400µW	**74.9% @1.5mW**
Maximum Power**	2.5mW	4nW	10m W	107µW	1mW	2mW	**2mW**
MPPT	TB	No	Current	FOCV	FOCV	Look-up Table	**2-D LI-TB-MPPT w/ FSH+Frequency**
Tracking Efficiency	96%	-	96%	-	-	-	**85%(source) 99%(system)**
MPPT Area*	-	-	-	$0.03mm^2$	$0.05mm^2$	$0.01mm^2$	$\mathbf{0.0033mm^2}$
Cold-start	No	No	No	Yes	Yes	Yes	Yes
Wake-up Area*	-	-	-	$0.4mm^2$	$0.9mm^2$	$0.96mm^2$	$\mathbf{0.000322mm^2}$**(WUA)** $\mathbf{0.047mm^2}$**(config.)**
Wake-up Time	-	-	-	300s	11s	252ms	**3.8 ms**
EHDS Active Area*	$25mm^2$	$1.53mm^2$	$4.62mm^2$	$1.2mm^2$	$1.5mm^2$	$2.52mm^2$	$\mathbf{0.058mm^2}$

"-": not reported or unavailable, PFM = Pulse Frequency Modulation, DCM =Discontinuous Conduction Mode, PSM=Pulse Skipping Modulation, BFHC= Boost/Flyback Hybrid Converter, TB= Time-based

* Estimated from chip area reported in corresponding reference and proportion of related blocks presented in chip micrographs.;

** Maximum power reported and/or shown in efficiency plots.;

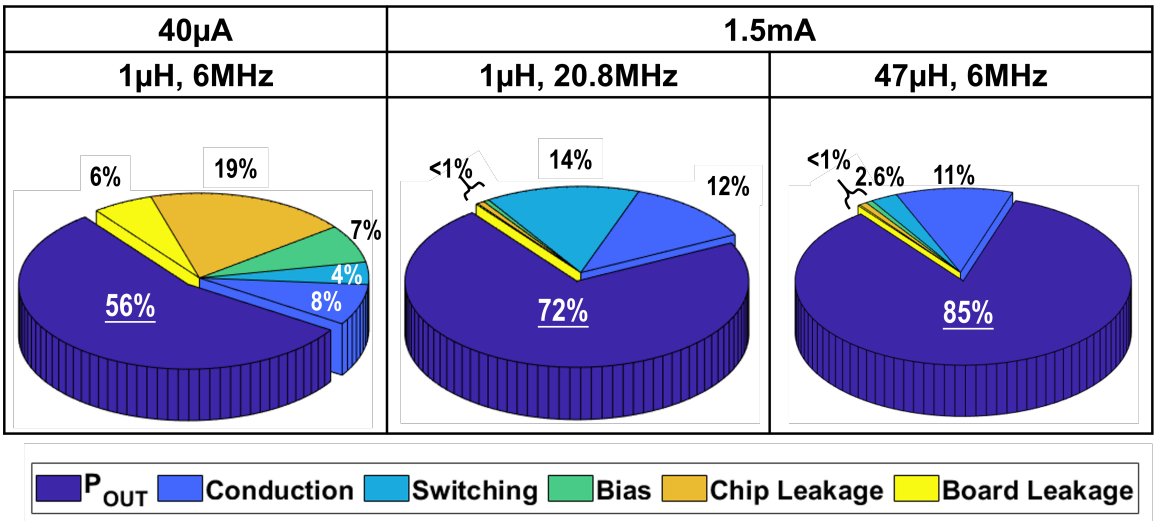


Figure 5.25: Breakdown of loss components at 40µA and 1.5mA load ($V_{OUT} = 1.0V$, $V_{IN} = 0.95V$)with 1µH and 47µH inductance.

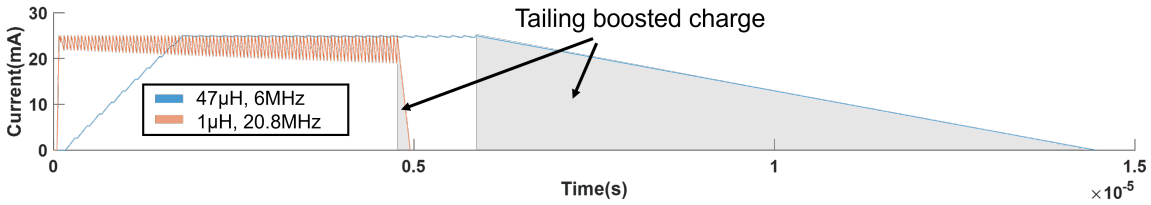


Figure 5.26: Simulated inductor current with 1µH at 20.8MHz and 47µH inductance at 6MHz, boosting at 1.5mA load.

at low power (P_{OUT}= 56%@40µA) is mainly limited by leakage components (25%), and as expected the contribution of conduction loss and switching loss becomes more significant under high power (P_{OUT}= 72%@1.5mA).

While the proposed design is demonstrated in a low-cost EHDS with reduced passive values, improved efficiency can also be achieved when higher-quality passives are available. Fig. 5.25 also shows a test case where up to 85 % conversion efficiency can be achieved when our EHDS uses a 47 µH inductor (as in reference [11]) and fixed switching frequency of 6MHz. The gain in efficiency is a result of reduced current ripple and frequency, which is shown in Fig. 5.26. However, as shown in the figure, the increased inductance also results in a large amount of boosted charge due to the reduced inductor current slope when switching events stop. This additionally requires increased input ca-

pacitance and output capacitance to reduce voltage ripple for harvesting and regulation, respectively. Although the proposed system can achieve competitive end-to-end efficiencies when similar passive values are used compared to prior EHDSs, peak efficiency is not the main focus of the design. A key contribution of this work is that the proposed system can support high levels of reduction in explicit passive values needed for operation, which ultimately signifies reduced system cost.

The proposed system also presents orders of magnitude lower active area with the proposed MPPT and wake-up assist approaches. When considering the scaling of technology nodes, this work still presents over $3\times$ reduction. Furthermore, most of the active area in this EHDS is dominated by the configuration matrix and not the control system as the size of the transmission gates have been designed with an R_{ON} of 0.5 Ohms to interface with up to 10mA harvester current. The size of these gates can be scaled accordingly when strength of harvesting sources change to gain additional area reduction. In addition, the output-based tracking achieves system-level tracking efficiency of up to 99%. The measured line regulation is 11.9mV/V and the load regulation is 0.174mV/µA. Finally, a wake-up time of 3.8ms can be attributed to both reduced input/control/output capacitance and the additional $2\times$ improvement presented in section 5.3.1.

5.4 Summary and discussions

This section presents a complete methodology for ripple-tolerant PFM harvesting from DC harvesting sources. Instead of strictly confining harvesting voltage to tight MPP windows, the harvesting voltage is allowed to drop to lower thresholds when the PMU is active and allowed to replenish itself during PMU IDLE periods. A corresponding system-output MPPT approach is further proposed to address challenges that arise from this alternative harvesting scheme. A test-chip implementation demonstrates successful cold-start, MPPT, and high efficiency power delivery with orders of magnitude lower active area and on-board inductor/capacitor values compared to prior works. Overall, the system presents

an all-in-one solution for EHDSs with a peak efficiency of 74.9% for compact, low-cost applications.

To demonstrate that the wake-up assist and LI-TB-MPPT+FSH methods can allow the system to achieve fast wake-up and robust power delivery without the overhead of backup resources, the EHDS has been implemented in a single-input single-output (SISO) topology without multiple harvesting sources nor backup storage elements. However, also because the system is only supplying and regulating a single load, the transient behavior of MPPT against input power variation is difficult to observe via measurement. An increase in input power simply results in near-VOC conditions because the input power is higher than what is required to sustain output regulation. Therefore, Fig. 5.21 demonstrates FSH from an alternative standpoint: fixing input conditions and allowing the EHDS to self-tune. However, the presented approaches are not limited to SISO designs and can all be adapted to multi-input multi-output (MIMO) architectures.

Compared to MIMO topologies [32], the presented EHDS represents a different research direction that focuses on reducing (rather than adding) system complexity/cost. Additionally, the fast wake-up enabled can be especially beneficial for systems that utilize on-demand power delivery to minimize standby power. One such application that could greatly benefit from these advantages is that of authentication ICs, which will be explained in the following section.

CHAPTER 6

VISIBLE LIGHT BASED AUTHENTICATION IC

The target application selected to demonstrate the contributions of this thesis is that of an authentication IC. Many industrial applications increasingly require secure authentication in supply chain and operations and deploy physical tags on high-value items to enable tracking or prevent forgery. The physical tags need to consume little or no power at all and are generally wireless in nature to ensure convenience of access. The prevalent implementation of such tags include bar-codes interrogated using visible lights. Visible bar-codes are easily accessible, but for the same reasons, they can also easily be tampered with or replicated by an adversary.

Radio Frequency Identification (RFID) authentication tags have emerged as alternatives to bar-codes to improve security [1, 2, 3]. RFID tags improve security by using ICs with on-chip encryption and secret keys. Near-field inductive links are used for both on-demand charging and communications [9, 7, 8]. The tags are normally inaccessible (powered down). During an interrogation cycle, a specially-designed RF probe uses inductive coupling to transfer energy and "wake up" the tags; followed by wireless transmission of input (plaintext) data. The tag encrypts the plaintext and transmits the ciphertext back to the probe verifying authenticity [5, 6]. However, RFIDs suffer from electromagnetic (EM) interference from surrounding signals and devices leading to the possibility of undesired wake-up and side-interrogation (Fig. 6.1) [9].

An alternative approach, and the one implemented in this thesis, is to couple simplicity of visible light authentication with secure ICs. This can be achieved by using photovoltaic properties to transduce visible light for both power and data links [20, 57]. As visible light bands can be easily directed and contained, adversarial interference can be limited. Visible light communication (VLC) can also extend the range of interrogation compared to

inductive RF coupling. On-chip photodiodes in CMOS process allow compact integration of modules to implement a single authentication IC that protects secret keys in silicon. Note that, a key tribute of visible light communication (VLC) is the need for line-of-sight communication, which restricts authentication to open-space and direct interaction, but also prevents hidden adversarial access.

This architecture is selected to utilize the high availability and exposure of the visible light band in our surroundings and the ability to transduce/sense this energy with CMOS compatible processes. Both traits promote the prospect of designing/developing a self-powered SoC with minimal overhead. On-chip implementation of signal sensing and authentication with a test-chip in 65nm CMOS is presented and evaluated with silicon measurement data.

6.1 System Architecture

Fig. 6.2 shows a simplified schematic of the system architecture. On-board photodiodes are used for receiving wireless transfer of optical power from the authentication probe. An on-chip boost regulator (BR) is used to boost the received voltage and generate a regulated voltage to power other components. The on-chip signal sensing (photodiode, PD, array and RZ-SA block shown) and data encryption (PRINCE) modules are power gated by a

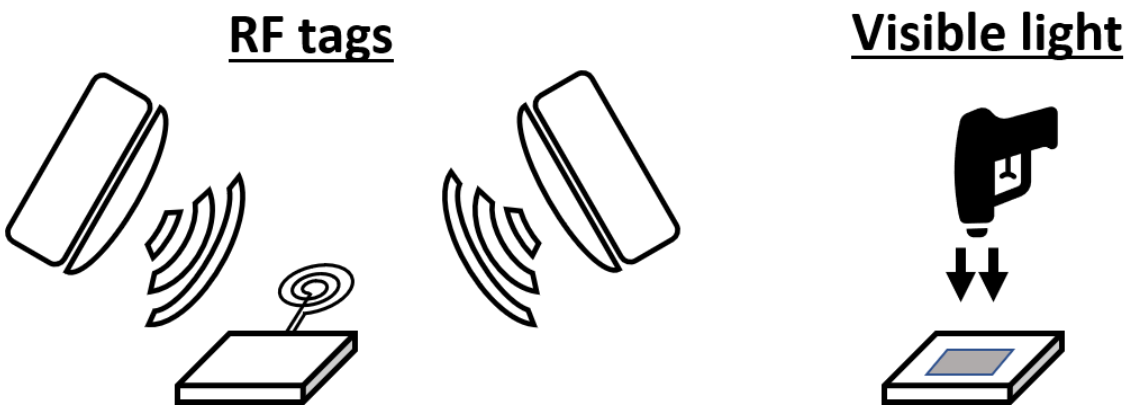


Figure 6.1: Comparison of RF and VL applications.

wake-up finite state machine (FSM) at the regulator output. The FSM is triggered by PFM control outputs and a schematic is shown in Fig. 6.3.

A typical interrogation cycle for the chip is illustrated in Fig. 6.2. Interrogation starts by shining any external light source to on-board photodiodes to wake up the IC. The on-chip PFM BR harvests energy from the photodiodes in this process and power gates are enabled to power the sensing and encryption modules after VOUT is charged up. The plaintext

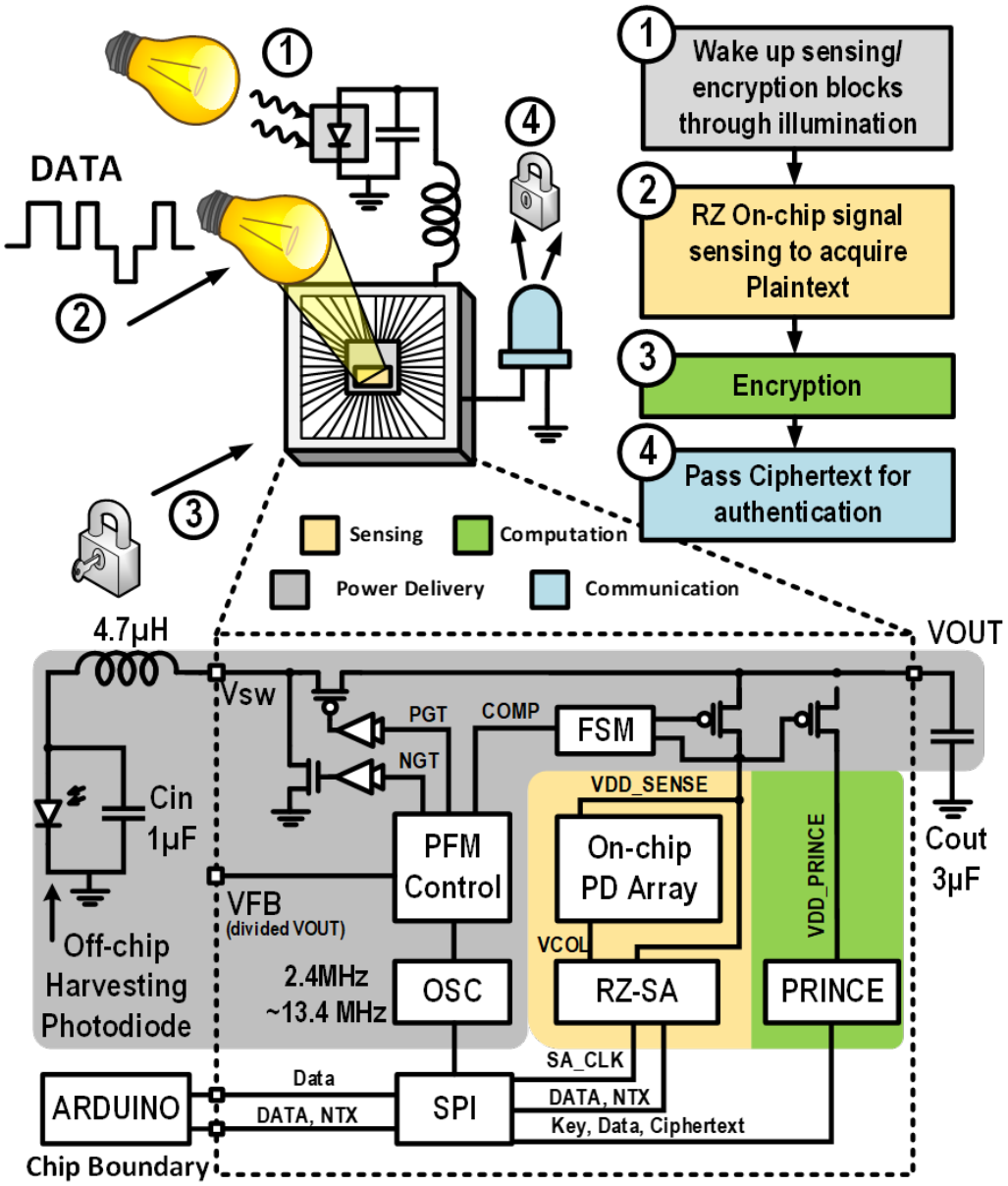


Figure 6.2: System Architecture and target application

is transmitted by controlling light intensity using an off-the-shelf Light Emitting Diode (LED), or even simple finger gesture in room light, and sensed by an on-chip photodiode array. The sensed plaintext is encrypted by the on-chip PRINCE engine and the encrypted ciphertext is transmitted by controlling an on-board LED.

6.2 Sensing and Data Communication

Photodiodes (PDs) have been integrated on-chip with CMOS circuits for sensing and communication applications [58, 57]. Fig. 6.4 illustrates common receiver analog-front-end (AFE) circuitry and single active-pixel sensor (APS) schematics. Different structures have been proposed for the trans-impedance-amplifier (TIA) in receiver AFEs[57, 59, 60]. Using reverse-biased photo diodes increases illumination sensitivity by sensing short-circuit (and/or reverse-bias) current. However, a higher (compared to integrated digital logic) voltage domain is often required for the photodiodes to remain in reverse-bias conditions when input illuminance fluctuates. The sensing down-link implemented in this work uses an alternative topology that eliminates the need for higher-voltage (or negative) biasing. The method includes two steps, a voltage-to-time conversion from the open-circuit voltage (OCV) of on-chip PDs, and a time-to-digital conversion to generate return-to-zero logic states.

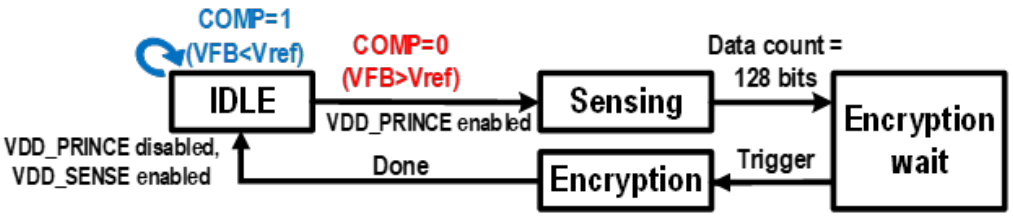


Figure 6.3: FSM for full interrogation cycle.

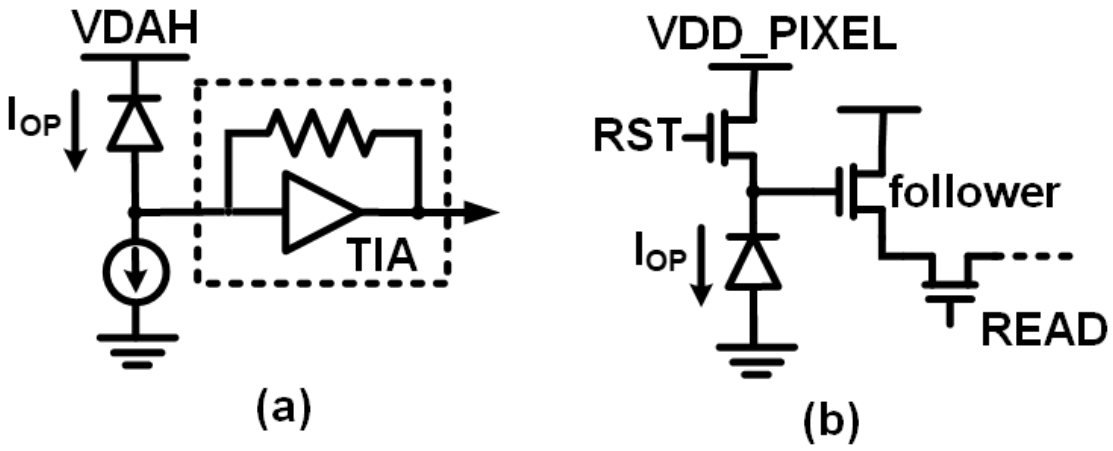


Figure 6.4: (a) Optical receiver AFE input (b) CMOS APS.

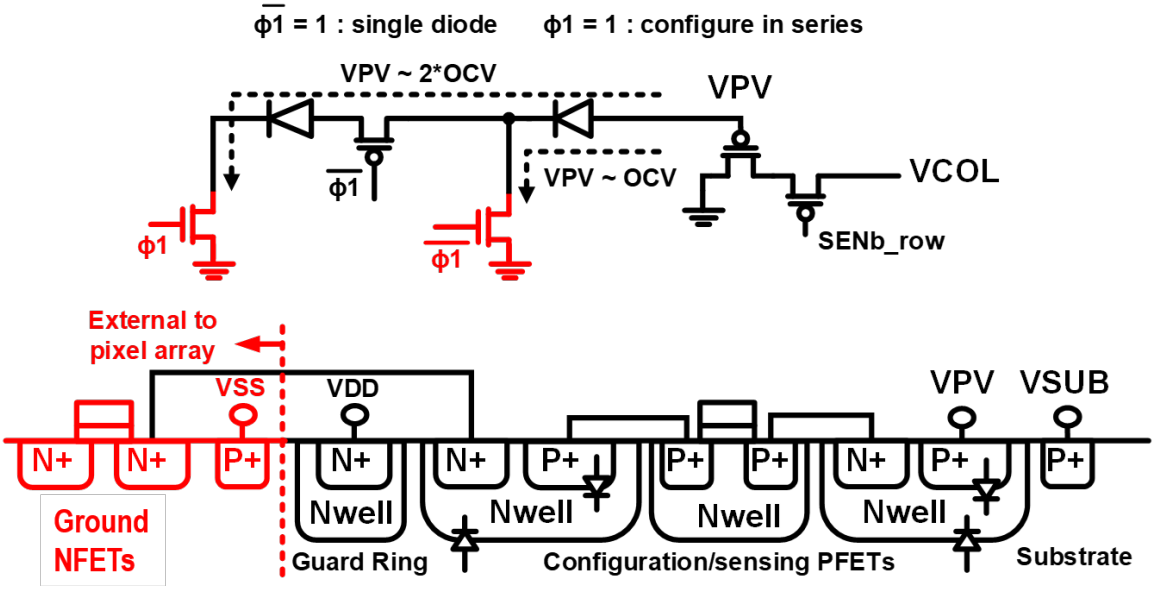


Figure 6.5: Configurable stacked photodiode array.

6.2.1 Photodiode Design

A re-configurable PD architecture is designed as shown in Fig. 6.5. CMOS PDs have been tested to be able to generate higher on-chip voltage through stacking [50]. The PD response is improved by stacking two diodes in series to create a higher sensing voltage and using the "floating substrate (P) to N-well (N)" as a secondary diode [12] to increase sensitivity (Fig. 6.5). However, to allow a locally-floating substrate, only PMOS transistors are used

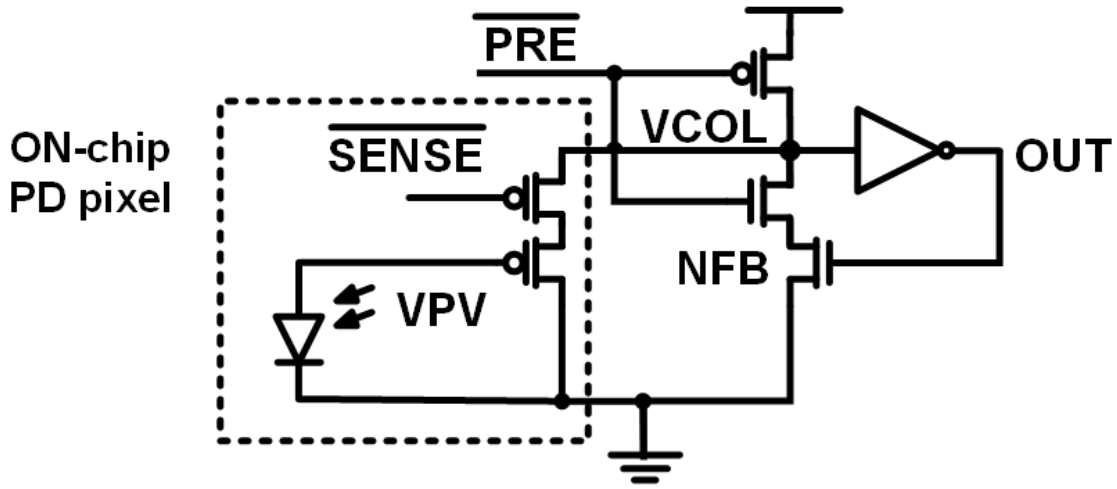


Figure 6.6: Schematic for voltage-to-time conversion (VTC).

for stacking diodes and all NMOS transistors that are used to ground cathode nodes of the diodes are placed external to the photodiode pixel array (Fig. 6.5: Ground NFETs). At extremely low light intensities, single-diode sensing is preferred with this topology as the configuration PFETs limit the discharge of the sensing voltage when diodes are stacked (VPV$>$V$_{th}$).

6.2.2 CMOS Photodiode Voltage-to-Time conversion

In this work, a dynamic sense amplifier with PMOS discharge is used to convert the analog voltage of open-circuit photodiodes to timing data (Fig. 6.6). This decouples the photocurrent (I_{op}) from adding to the power overhead in the sensing circuit. The sensing topology utilizes the fact that input light intensity maps monotonically to OCV of on-chip photodiodes. During the initial pre-charge phase, $\overline{\mathrm{PRE}}$ is low and VCOL is pre-charged to VDD. When sensing, $\overline{\mathrm{SENSE}}$ is switched low and the anode voltage of the PD (VPV) is passed to VCOL with a threshold voltage offset and the OUT node latches through the feedback transistor, NFB. A higher VPV (at higher input light intensity) will result in slower switching time of the OUT signal. Consequently, different voltage levels of VPV are represented by the changes in the switching time of the DSA output. This sensing topology requires the VTC to be slower than typical high-gain sense amplifiers. The PFET follower enables

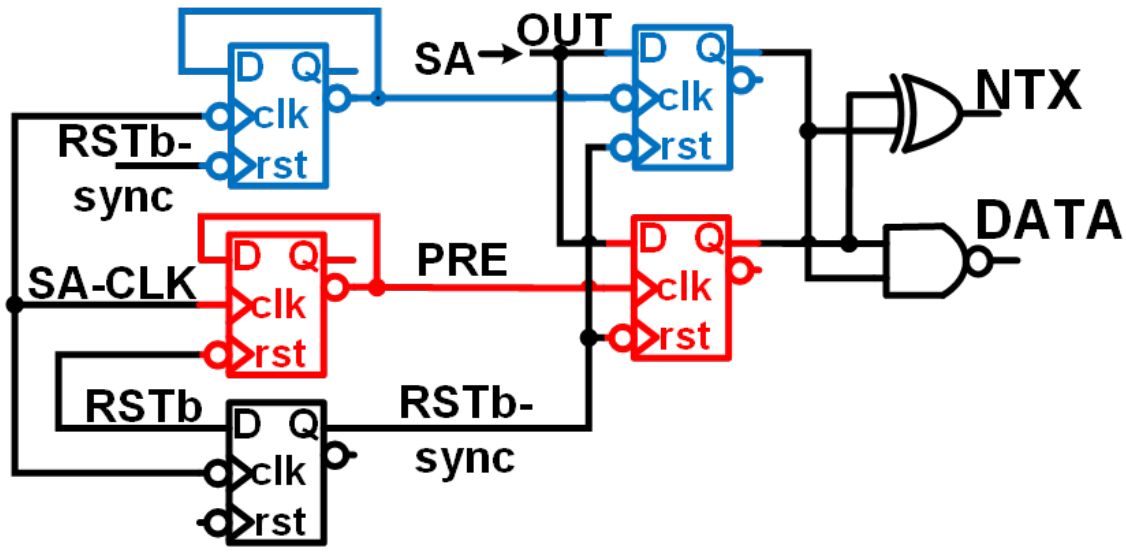


Figure 6.7: Schematic for time-to-digital conversion (TDC).

this capability and the offset it introduces also increases sensitivity at low light, low VPV conditions (by increasing latching time for comparison with SA-CLK).

6.2.3 Time-to-Digital Return-to-Zero Circuit

To further distinguish this timing information into three levels, “Zero”, “Non-Transmitting (NTX)”, and “ONE”, the RZ sensing compares DSA output relative to SA-CLK edges to output create “DATA”, and “NTX” at every two SA-CLK periods. Apart from a flip-flop for synchronizing reset edges, two positive-edge triggered flip-flops and two negative edge triggered flip-flops generate the sampling edges for the SA output (Fig. 6.7).

A simplified waveform of the overall operation of the return-to-zero sense amplifier (RZ-SA) topology is shown in Fig. 6.8. Under low-light conditions, the SA switches faster and the OUT signal latches before both sampling edges, which is distinguished as a logic “ZERO”, a medium light intensity will cause the “NTX” signal to switch high, and a high intensity results in a logic “ONE”. The level-based-sensing incorporated in the RZ-SA conversion steps makes it robust to background noise, and provides flexibility in frequency of input signal modulation, thus relieving the need to design specialized transmission probes.

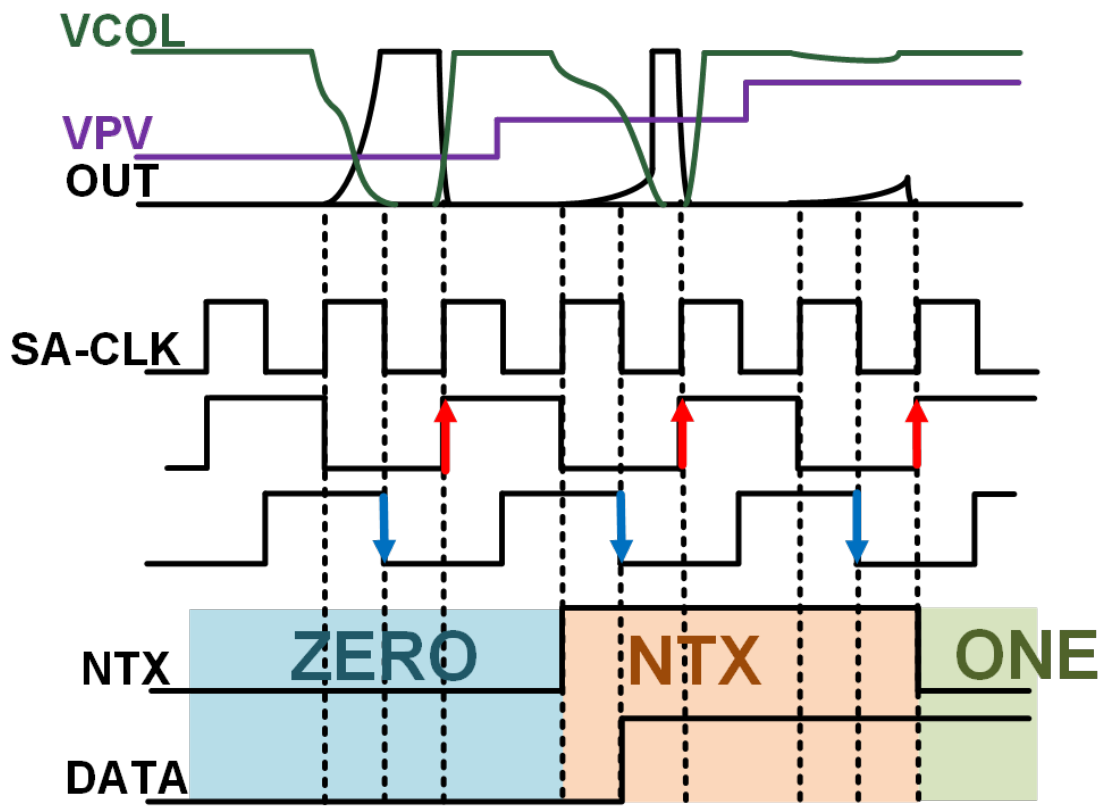


Figure 6.8: Sample waveform of critical nodes in RZ-SA operation.

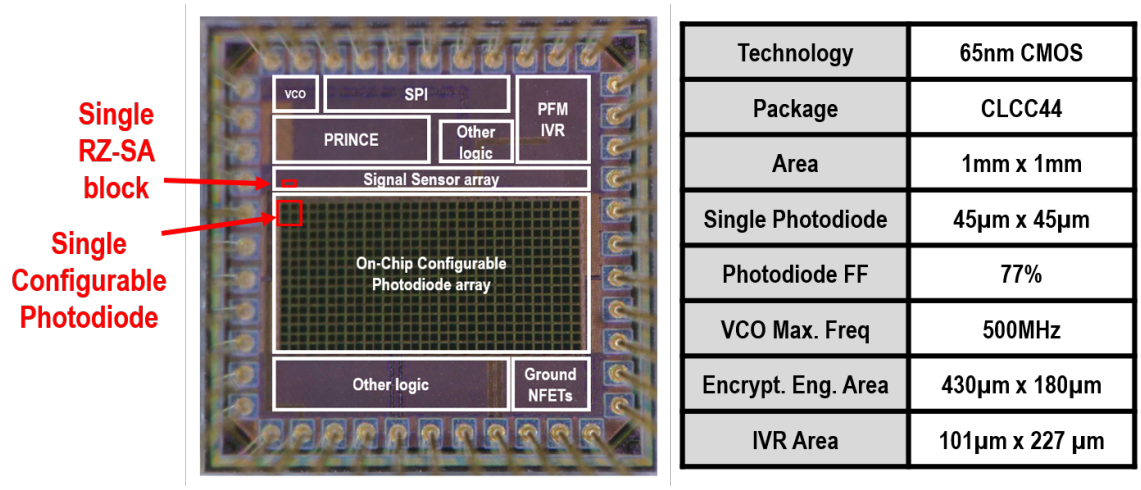
Inter-state transition noise can be filtered with simple debouncing logic and adaptability to lighting conditions can be done by designing/tuning with different SA-CLK frequencies, allowing different methods of light intensity modulation to be used for input.

6.3 Measurement Results

6.3.1 Chip micrograph and Measurement Board

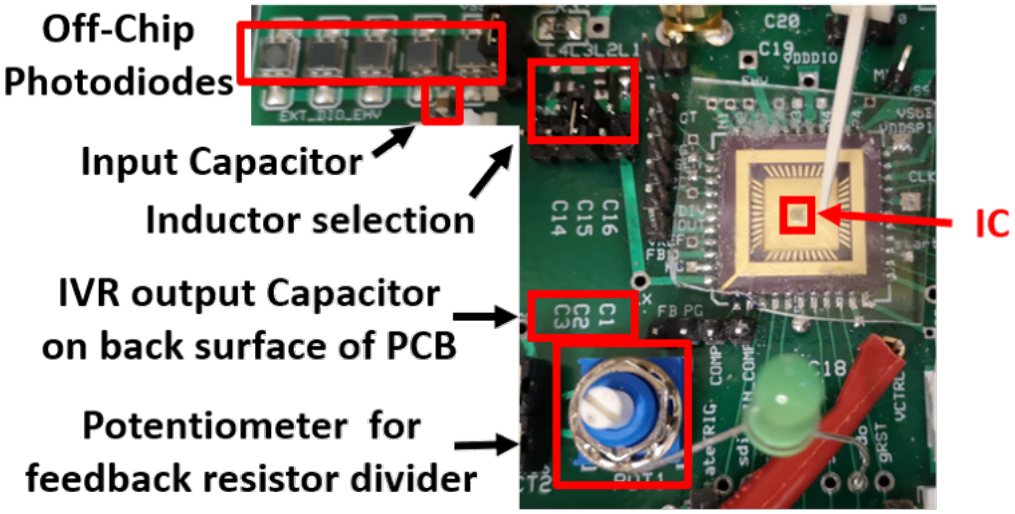
Fig. 6.9a shows a chip micrograph. The IC is fabricated in a 65nm CMOS technology and packaged in CLCC 44. The total die area is 1mm^2. Although a total of 16×8 configurable photodiodes are created as an array, only a single RZ-SA block and configurable photodiode within the array is needed for system operation. Therefore, the total active area (excluding testing harness) needed to demonstrate full system operation occupies 0.08046mm^2.

Fig. 6.9b shows the PCB layout corresponding to the schematic shown in Fig.6.2 for



Technology	65nm CMOS
Package	CLCC44
Area	1mm x 1mm
Single Photodiode	45µm x 45µm
Photodiode FF	77%
VCO Max. Freq	500MHz
Encrypt. Eng. Area	430µm x 180µm
IVR Area	101µm x 227 µm

(a)



(b)

Figure 6.9: (a) Chip micrograph (b) Measurement printed circuit board (PCB).

testing the IC. Passive components and off-chip photodiodes are also highlighted. We use an array of 5 off-chip photodiodes (with device:VBPW34S) to create the harvesting source and a potentiometer is used to tune feedback voltage for output regulation level modulation.

A schematic of the complete measurement setup and observation tools is shown in Fig. 6.10 A flashlight is applied to the external diodes to serve as an active input source and a function generator can be used to create input signals for down-link communication. Configurations and computation results are observed through an Arduino DUE board that

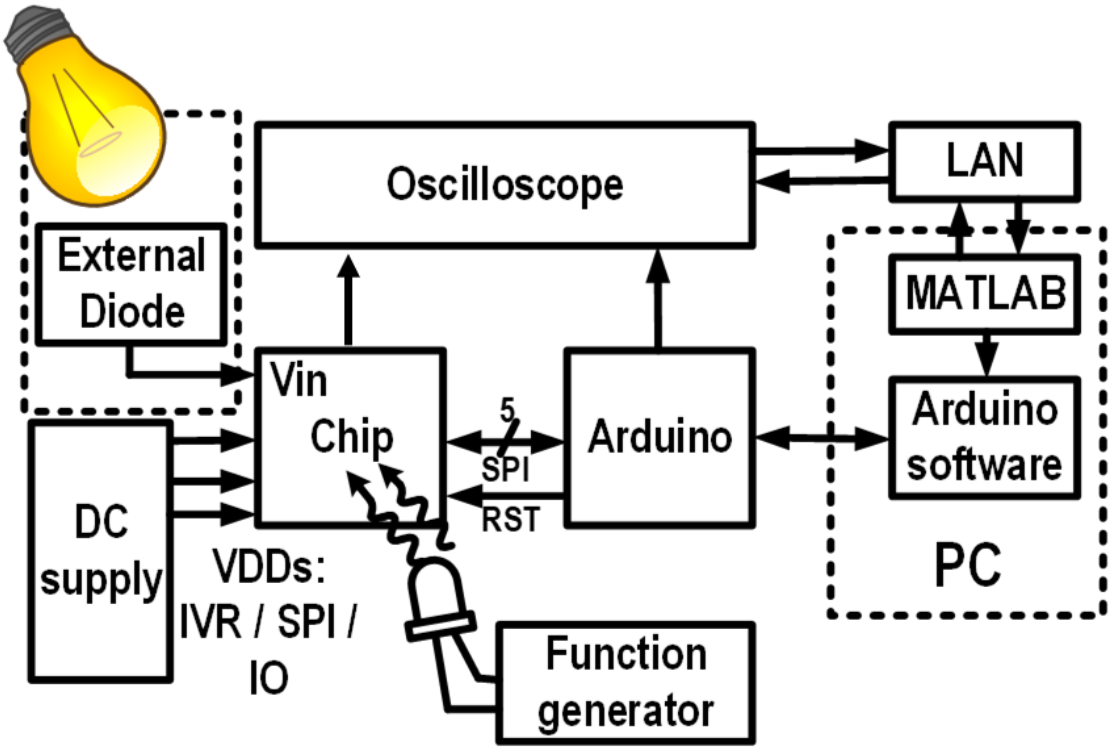


Figure 6.10: Schematic of setup for measurement testing.

communicates with the on-chip serial-to-parallel interface (SPI). Additionally, waveforms are observed through the oscilloscope.

6.3.2 System Operation

Down-link

Fig. 6.11 shows a characterization of the RZ-SA circuit (Down-link) when sensing DC input voltage at given SA-CLK frequency. The maximum data receive rate (DRR) at which plaintexts can be downloaded to the SoC is defined by the maximum rate of variations of the input light intensity that can be successfully transduced into sensing voltage transitions and distinguished by the RZ-SA circuit. Fig. 6.12 shows the measured maximum DRR at different input signal light intensities for a fixed SA-CLK frequency of 600KHz. Stacking photodiodes and enabling a locally-floating substrate improves the DRR. A slower SA-CLK moves the NTX and ZERO thresholds to a higher intensity value, which improves

DRR when operating the sensor with a high light intensity. With a 300KHz SA-CLK and 500lux to 19.95Klux input light signal variation (created by a function-generator-controlled LED in room-light), the chip demonstrates a maximum DRR of 53.8Kbps (Fig. 6.13). The data rate is sufficient to achieve 750 authentications per second.

The major limiting factors for DRR include: 1) the sensitivity of on-chip diodes, 2) the parasitic capacitance at the sensing voltage node, 3) the slew rate of the input light intensity, and 4) the frequency of the sampling clock. In the presented design, the SA-CLK frequency (derived from the IVR oscillator) can be increased to 13MHz to alleviate the last factor. The first three factors affect the maximum rate at which the sensing voltage can respond to light intensity variations. Using specialized CMOS processes designed for image sensing, increasing the overall PD area, and eliminating metal stacks over the PD area can improve the light sensitivity of the PDs. Further, it is possible to increase the maximum DRR by increasing the slew rate and intensity swing of the input signal and using a higher SA-CLK frequency in a darker setup.

Full Interrogation cycle

Fig. 6.14 shows measured transient waveforms of the IC's power link response to an interrogation. An ARDUINO board is programmed to 1) enable LED switching (input DATA) and 2) create a trigger for encryption to start once the IVR output reaches regulation level. The AM light signal for plaintext DATA is sensed and observed through a devoted I/O ("DATA obs."). The IVR control logic and SPI are supplied externally, while PRINCE and sensing circuits are powered by the IVR. In nominal room light conditions, the IVR output is only 170mV and the IC remains IDLE. The boost regulator output reaches regulation (set to 0.68V in this experiment) after 20ms with 59Klux light intensity on the off-chip photodiode array (supplied by a flashlight). The FSM receives the regulation signal and enables the power gate to supply the PRINCE encryption engine. This transition triggers a short period ($\sim$5ms) of glitches to occur at the direct output of RZ-SA sensing circuits

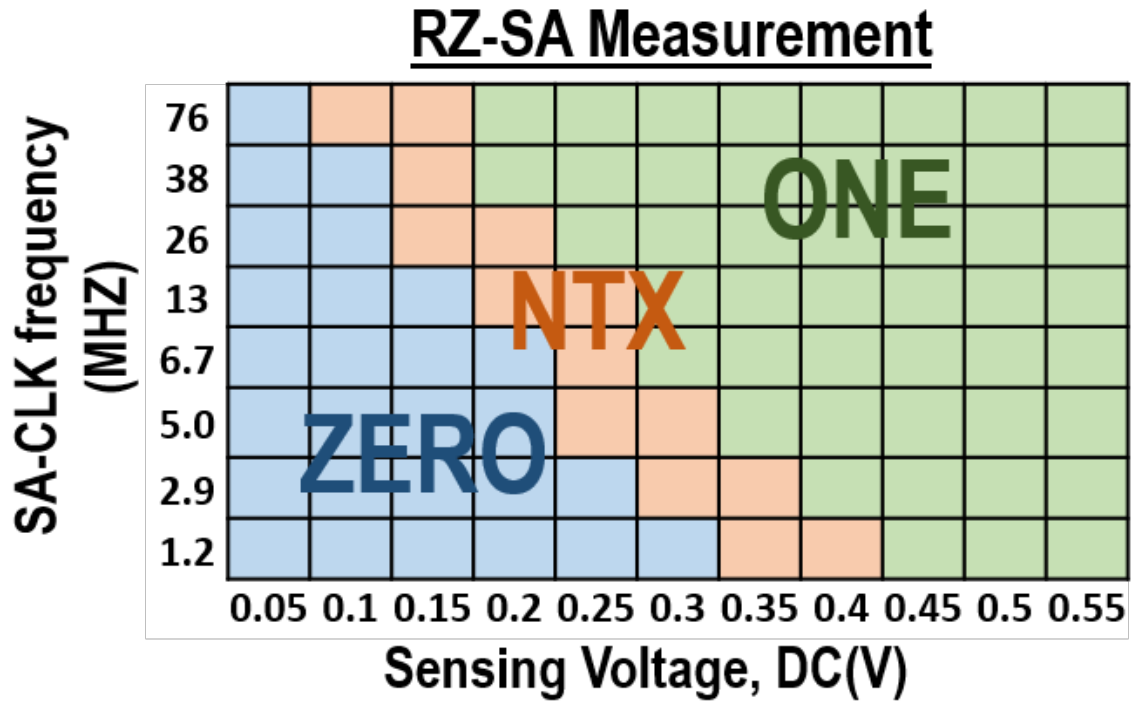


Figure 6.11: Characterization of RZ-SA sensing thresholds.

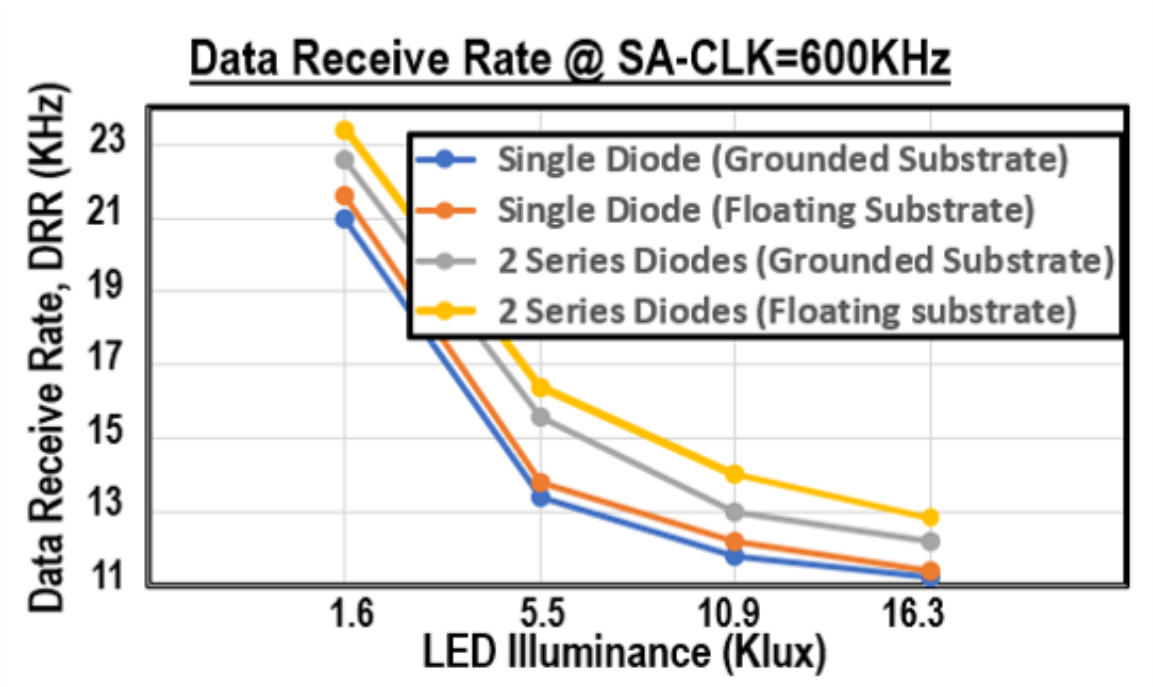


Figure 6.12: Data receive rate of IC at different light intensity for fixed clock frequency.

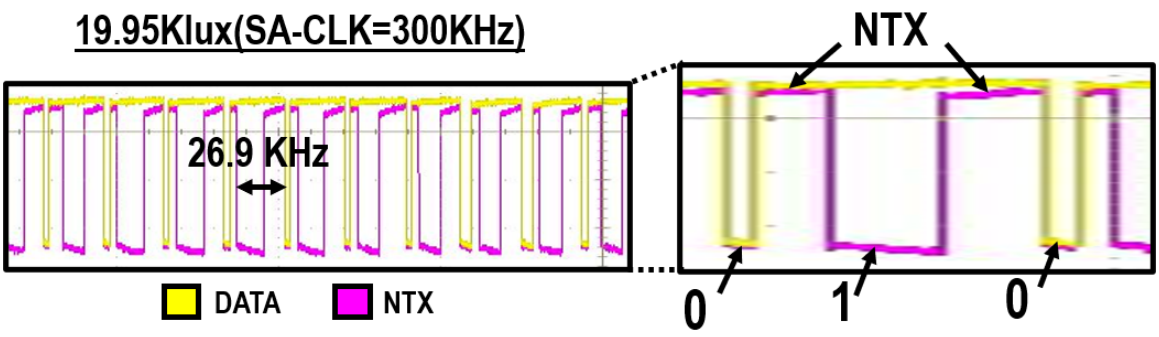


Figure 6.13: Measured RZ-SA output from LED input.

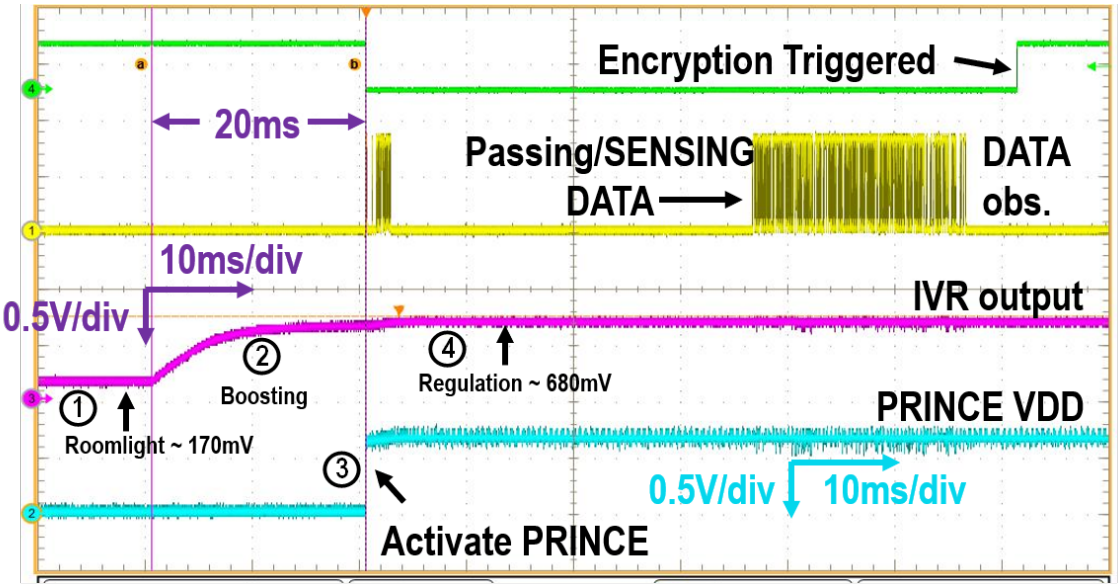


Figure 6.14: Measured critical waveforms of IC power-link during an interrogation.

before DATA is passed. However, the glitches can be filtered by adding an additional state in the on-chip FSM that waits for a second regulation "COMP" signal. Finally, the IVR successfully stabilizes the supply as both sensing and encryption occur consecutively.

6.3.3 Demonstration of Operation

The authentication IC utilizes Amplitude Modulated RZ sensing which is independent of frequency. Therefore, no specialized probe is necessary to interrogate the IC and methods of signal input can vary from modulating active light sources such as controlling LED

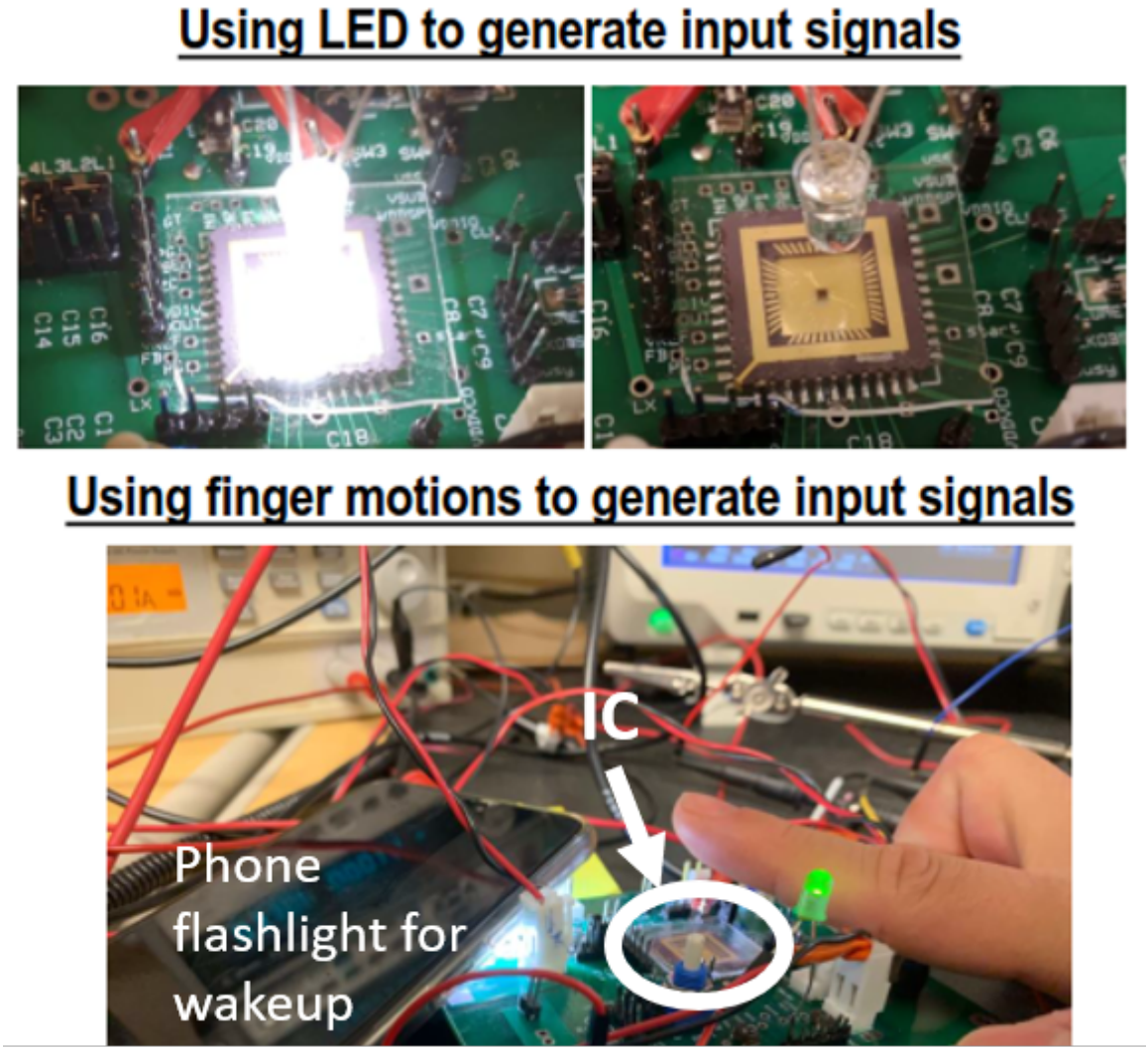


Figure 6.15: Input modulation methods tested (LED and finger motions) and wake-up demonstrated with common cellphone flashlight (bottom).

signals and phone flashlight intensities to applying shade with non-transparent obstacles. This is demonstrated in Fig. 6.15.

Active illumination can allow a lower SA-CLK frequency for sampling input signals by providing higher sensing voltage (Fig. 6.11) across the PDs. In Fig. 6.15, this is demonstrated with an LED that is connected to a function generator.

Alternatively, passive shading with obstacles to create input signals can also be made possible by applying higher SA-CLK frequency. Fig. 6.16 demonstrates the generation of different light intensities corresponding to different sensed signals, which is mainly asso-

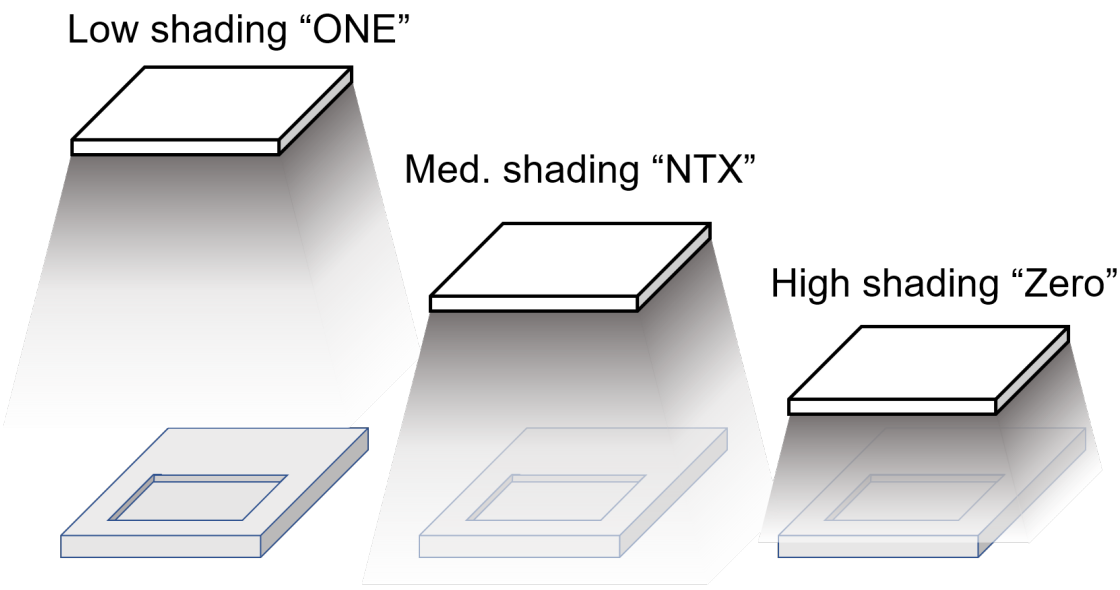


Figure 6.16: Method of applying shade to IC.

ciated with the distance of the obstacle from the IC. Under bright room light conditions (>500 lux), using a divided clock from the IVR oscillator is sufficient to distinguish the effect of shading. However, at lower background light conditions, the maximum sensing voltage is limited by the sensitivity of on chip photodiodes. In order to ensure that a “ONE” can be transmitted, the “NTX” band needs to be pushed to lower thresholds by further increasing the SA-CLK frequency.

6.4 Comparison to prior works

A few prior works have demonstrated board-level prototypes for authentication modules with light-based communication IDs[61, 62]. However, to the best of the authors’ knowledge, this is the first paper to demonstrate a single authentication IC using visible light for both data and power links.

Table 6.1 compares the presented design with other light-interrogated authentication modules [61, 62]. Compared to prior board-level designs with only light-based communication, this work presents a single IC with visible light for both data and power links. The down-link with on-chip sensing prevents physical bypassing for enhanced security and en-

Table 6.1: Comparison to existing light-based IDs

References		**This Work**	[61]	[62]
Single Chip		**Yes**	No	No
Technology		**65nm**	-	-
Data Link		**Visible light**	Visible light	IR light
Data Rate		**<1bps−53.8Kbps**	$\sim$ 615bps	36Kbps
On-Chip Sensing		**Yes, CMOS photodiode + sensing circuit**	No	No
Battery Power	Idle	**2.29μW**	5.4μW	1.1mW
	Active	**2.29μW**	4.8mW	12.9mW
Power Link		**Off-Chip Photodiode + On-Chip PFM IVR**	No	No
Computation		**PRINCE**	RISC-V	RISC CPU

ables a relatively high data rate at lower power. Moreover, the power link is used to supply power-consuming sensing and encryption circuits that are only enabled during interrogation. During the idle mode, only the control circuits of IVR are powered by an external battery. Hence, the measured battery power (idle power) is much lower (approximately 2.29μW) compared to prior light-based interrogation modules.

Table 6.2 compares this work with existing ICs on wireless authentication tags and chargers. The sensing/receiving circuits consume 458nW during IDLE and 38.4μW during active (at 1.2MHz SA-CLK). The PRINCE encryption engine consumes 46.9μW with operating frequency of 0.78MHz at 0.7V. However, the power for sensing and encryption are both fully supplied through the IVR from off-chip diodes and do not contribute to IDLE power (power gated in IDLE mode). Overall, the idle (battery) power of the IC is similar to prior works using RF power/data links. The power consumption of the I/O driver for the on-board LED (uplink) consumes approximately 12.9mW(@3.3V) when driving an "ON" state for the LED. This is comparable to RF up-links where Chi et al. have shown a peak

Table 6.2: Comparison to state-of-the-art authentication ICs

Metric	**This Work**	[5]	[6]	[1]	[2]
Technology	**65nm**	130nm	65nm	130nm	130nm
Data Link	**Visible Light Communication**	RF	RF	RF	RF
Data Protocol	**AM, Return-to-Zero**	PPM,OOK	PWM 100% ASK	ASK	ASK
Data Link	$<$ 1**bps to 53.8Kbps**	125Kbps	100Kbps	106Kbps	106Kbps
Power Link	**PV**	RF	PV	RF	RF
Power Converter	**PFM IVR**	Regulating Voltage Multiplier	Switch Capacitor	LDO	LDO
Interrogation methods	**LED/object shading**	RF	RF	RF	RF
Dedicated Probe Necessary	**No**	Yes	Yes	Yes	Yes
Operating Frequency	**1.2MHz**	-	2MHz*	-	1.92MHz*
Idle Power	**2.29μW(@0.8V)**	3.6μW	-	-	-
Security	**PRINCE**	SHA3	Elliptic-Curve	3DES+TRNG	OTP memory
Throughput	**750 tags/sec**	30 tags/sec	-	3* transactions/sec	-
Range	**10cm**	-	5cm	10cm	-
Active Area	**0.31mm^2(w/ single diode)**	$0.74mm^2$	$1.6mm^2$	$3mm^2$	$1.1mm^2$

* estimated from paper; PPM=Pulse Position Modulation; OOK=On-Off Keying; PWM=Pulse Width Modulation; ASK=Amplitude Shift Keying; LDO=Low Dropout Regulator; TRNG=True Random Number Generator; OTP=One-Time-Programmable

power of 49.3mW [63] and Shakib et al. have shown a DC power of 17.5mW [64]. The up-link consumes $\sim 0.4\mu$J energy to transmit a 64bit data.

This work presents a lower data rate (53.8Kbps) compared to prior works (100Kbps). The encryption latency is negligible compared to the data transmission latency. Overall, an authentication rate of 750 tags/sec (64 bit tags: total latency= $64 \times (1/53.8kbps) + 12clockcycles \times (1/0.75MHz) + 64 \times (1/1MHz)$) can be achieved. The interrogation range is approximately 10cm under room light when using simple interrogation devices such as flashlight/shading obstacle/off-the-shelf LED. However, the range can be increased by using higher light intensity/concentration; up to 8 meters has been reported in prior work[61].

6.5 Summary

To summarize, contributions highlighted in this section include:

1) An authentication IC with visible-light-based interrogation is designed and demonstrated in 65nm CMOS.

2) A visible light based power-link is presented that uses photodiodes and IVR to wake up the authentication IC upon active illumination.

3) A low-power on-chip signal sensing scheme is developed and demonstrated with configurable sensing ranges.

The architecture can be extended to applications that include, but are not limited to, authentication. The low-idle power design allows it to be integrated with existing systems while introducing minimal overhead. As explained in section 6.2, the sensing range of the RZ-SA method is dependent on the sampling clock frequency. This allows the IC to be configured to fit low-background-light or bright-surrounding scenarios which not only provides deployment flexibility but also reduces the limitations of creating fixed operating

conditions. The frequency-independent sensing after wake-up can be utilized as a Human-Computer-Interface for creating boost signals, generating temporary initial vectors, or simply as a touch-free input device. Also, the merit of using direct-able visible light allows multiple devices to operate in close proximity in parallel, with little concern for interference.

CHAPTER 7

PROJECTED SELF-POWERED AUTHENTICATION

The authentication IC design shown in Chapter 6 successfully demonstrates a target application where low-power IoE devices can be deployed. However, static power consumed by the IVR still requires additional maintenance overhead. The self-powered EHDS in Chapter 5 demonstrates several tributes that can be used to improve the power management approach in Chapter 4. A fully self-powered authentication IC can thus be realized combining merits of these designs. This chapter will investigate projected power, performance and area of the system.

7.1 Performance Projections

7.1.1 Cold-start with undesired-wakeup filtering

As explained in subsection 4.5.2, an always-on IVR is used to prevent undesired wake-up in prior cold-start approaches. However, the power overhead can be prevented by adapting the wake-up assist approach explained in subsection 5.2.1. The prior EHDS configures the source configuration matrix under "SLEEP" conditions to use a default stack of three input sources. This setting is based on the observation that the reference circuit stabilizes at around a supply voltage of 0.8V (Fig. 7.1). As the V_{OC} of photodiodes show levels around 270mV under room-light conditions, a stack of three diodes is sufficient to allow wake-up at near room light illuminance levels. To prevent the EHDS from starting at room-light, the configuration matrix logic simply needs to be modified to a default stack of two diodes in series.

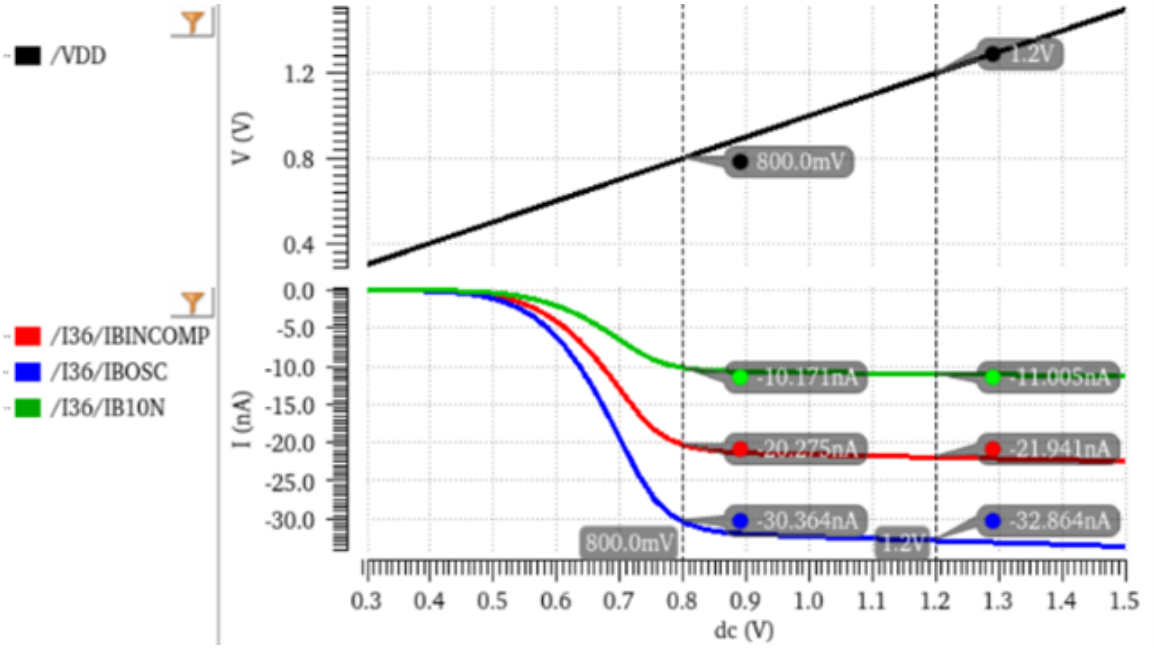


Figure 7.1: DC sweep of voltage/current reference circuit.

7.1.2 Time-based multiplexing of frequency tuning

PVT variations can impact IVR performance as indicated in subsection 4.4.1. However, by allowing the MPPT to track optimum frequency settings (subsection 5.3.3), the impact on conversion efficiency can be reduced to a minimum. However, additional time-multiplexing control may need to be implemented to ensure that frequency re-configuration does not affect the sampling clock for signal sensing.

7.2 On-chip Photodiode Harvesting

While we have only utilized on-chip photodiodes for signal sensing in Chapter 6, it has been demonstrated in prior work that these resources can also be used for harvesting purposes [11, 6]. Prior literature has also investigated the amount of power that photodiodes in non-specialized CMOS processes can generate [12], which can be used as a reference to evaluate EHDSs that target on-chip powering.

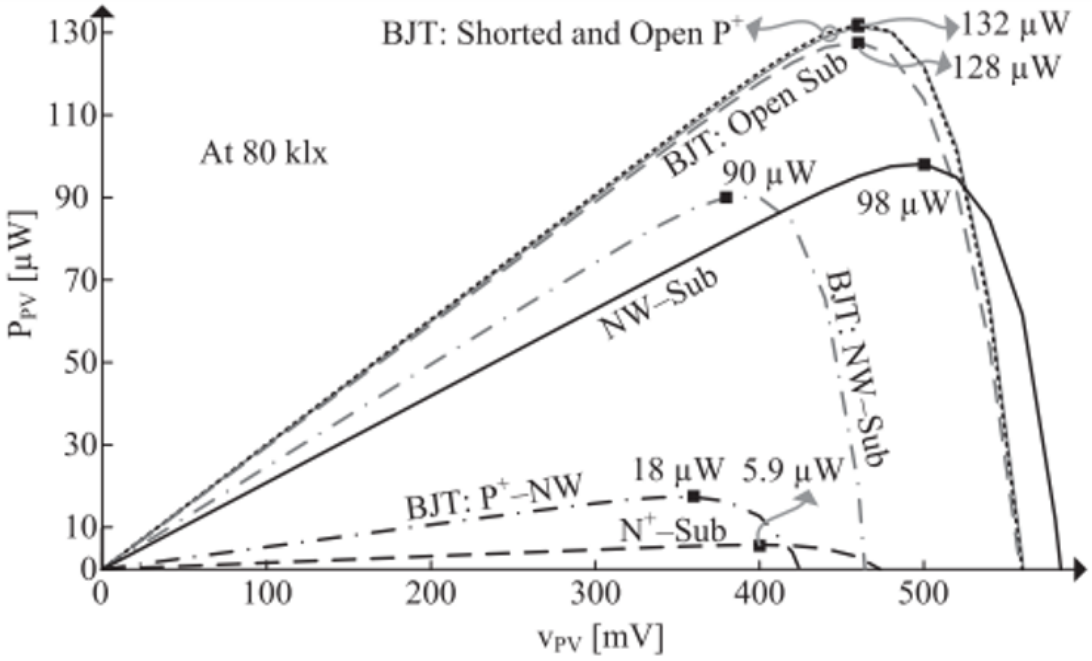


Figure 7.2: Power extracted from on-chip photodiodes in CMOS processes [12].

7.2.1 Area Projections

As seen in Fig. 7.2, up to 130 µW power per mm^2 can be generated at 80 klux by allowing the NW-Sub to serve as a secondary diode. To achieve full energy autonomy without external sources, the design of other blocks will need to consider this power budget along with restrictions in area.

The largest block in the prior EHDS demonstrated in Chapter 5 is the configuration matrix. The source configuration matrix previously demonstrated in Fig. 5.19 occupies approximately $0.0476mm^2$. Which can be a relatively high overhead considering on-chip harvesting resources. If this area is converted for photodiode implementation, a projected 6.118µW can be gained.

Fig 7.3 shows an illustration of the diode implementation described in subsection 6.2.1. However, instead of allowing a stack of 2, we have increased the number of transistors to allow select-able stacks of 1, 2, 3 and diodes in series. When using a stack of 3, the last diode is individually connected to sensing transistors as shown in Fig. 6.5. Therefore, a

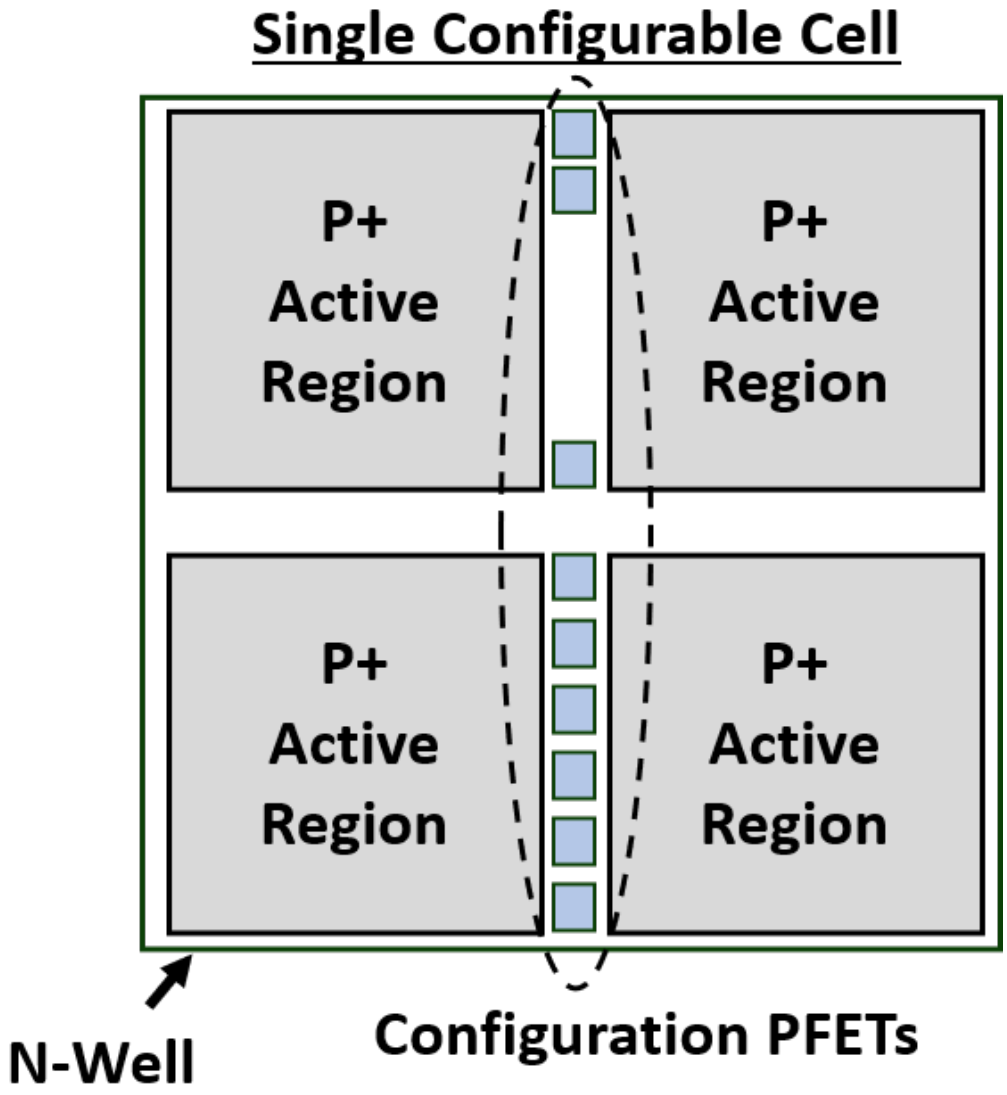


Figure 7.3: Layout of a single configurable diode.

total of 3 (series transistors) + 4(parallel output transistors) + 2 (sensing transistors) are needed and illustrated in the figure. With this setting, we can still achieve a 77% fill factor by placing transistors under metal stacks needed to maintain foundry design rules. With the fill factor known, the total active photodiode area can thus be projected based on system requirements such as the minimum input power demand.

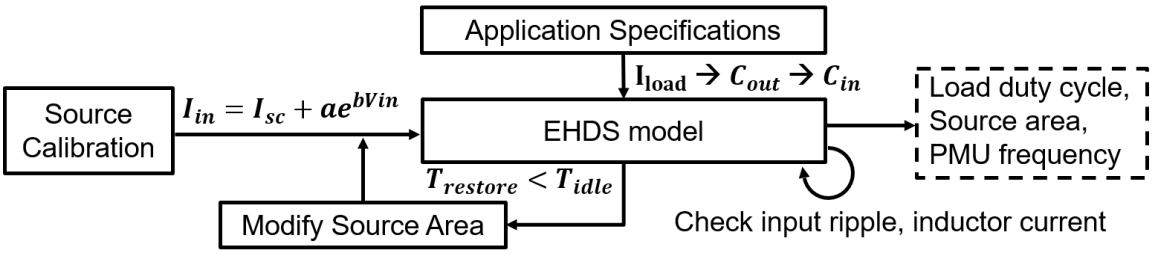


Figure 7.4: EHDS performance projection and optimization flow.

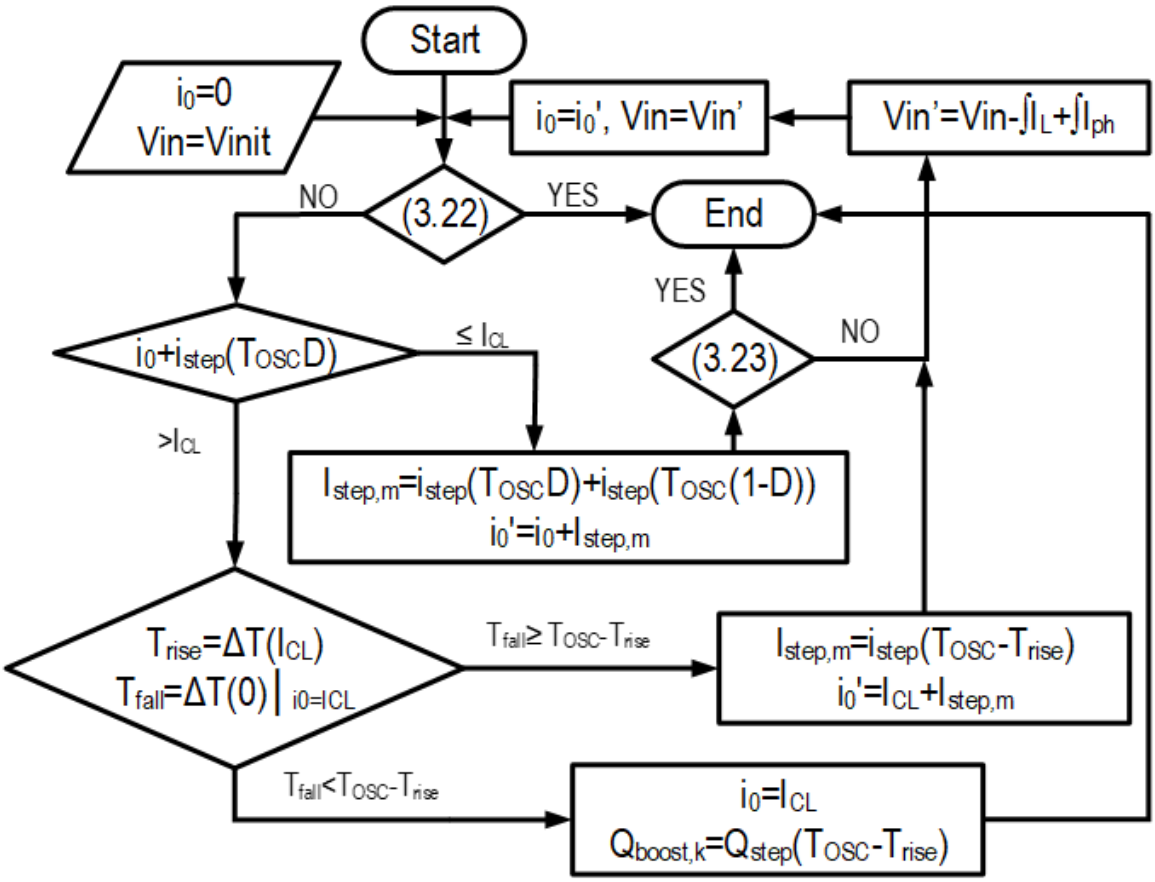


Figure 7.5: Flow diagram for performing harvesting voltage transient modeling.

7.3 Full System

A projected fully self-powered device can thus be envisioned based on the aforementioned discussions. While most of the EHDS can re-use existing designs, the design of the on-chip photodiodes should be visualized based on the output load demand. Fig. 7.4 illustrates the process utilized for system performance projections. System parameters are determined by

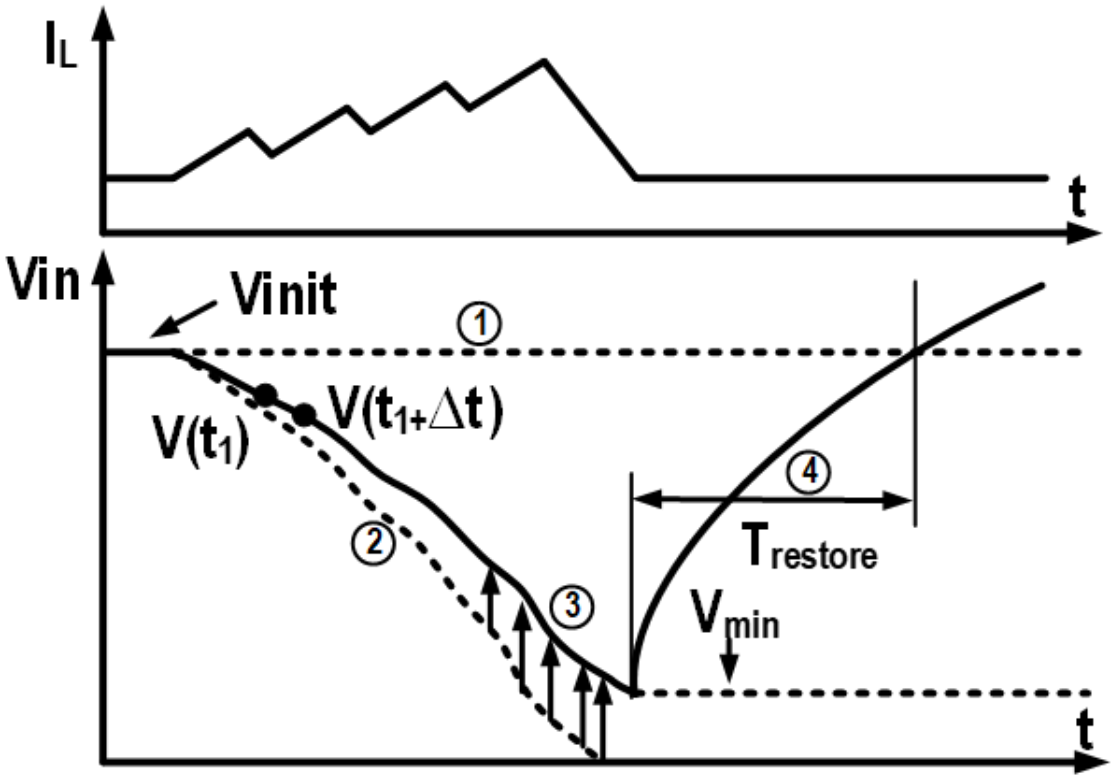


Figure 7.6: Harvesting voltage computation steps.

computing explicit passive components based on application specifications [65, 66, 67, 68] and the size of the harvester is estimated based on modeled results. The output capacitance is derived first based on the prior system latency estimations shown in section 6.3. The input capacitance is selected as half the output capacitance due to the input ripple tolerance of the EHDS design. A design space exploration is then performed with the simulator model to (1)decide the photodiode active area needed to maintain output regulation, (2)decide IVR frequency and inductance to ensure input voltage drop is tolerable, (3) determine the duty cycle of the output if input power is restricted.

Because the harvesting voltage behaviour is no longer strictly confined as assumed in the system-level validation model presented in section 3.3, the power conversion model also needs to be modified. To ensure the model can capture the impact of harvesting voltage transients during converter operation, a "semi-simulator" model has been developed. Fig. 7.5 illustrates modifications made based on the DC-DC conversion model flow pre-

sented in subsection 3.2.2 with detailed descriptions presented in Fig. 7.6.

The inductor current behaviour is determined based on the same criteria as the previous DC-DC PFM conversion model. For each inductor current step, however, additional input voltage tracking and updating is incorporated. When a change in inductor current is encountered, the tracking array for Vin is first extended to accommodate space for following computation steps. Secondly, the drop in input voltage solely due to inductor current is computed with Equation 3.20 and is computed for the full extended array. Then, each element (V($t_1 + \Delta t$)) is updated in an iterative manner by integrating the input current ($I_{pv,V(t_1)}$) across the unit step Δt and added to the input voltage. The minimum input voltage (V_{min}) at the end of PMU switching activity is then used as a reference to compute the restore time ($T_{restore}$) with Equation 5.11.

Table 7.1 shows three different designs based on different application specifications. The low load design allows lower output capacitance needed to maintain the output voltage when the PMU is IDLE. A 4nF capacitance is selected to ensure the source can restore from the 0.31V harvesting voltage drop when the PMU is ACTIVE. The higher input ripple also results in slightly lower harvesting efficiency compared to the "typical" design. However, autonomy can still be achieved with 0.27mm^2 photodiode area while ensuring boot-strapped operation of the PMU. The low input design demonstrates a scenario where the input power restricts the duty cycle of the load. Following a similar procedure as that used to determine "low load" and "typical" designs, the photodiode area would need to be larger than 4mm^2 to ensure load operation with $>$90% duty cycle. However, the active area would be much larger than the PMU and the design would dominate the silicon area. By reducing the duty cycle to approximately 15%, only 0.8mm^2 is needed.

Table 7.1: EHDS designs to target different applications.

Design		low load	typical	low input
Max. Load Current		**10μA**	40μA	40μA
I_{SC}(per mm^2)		100μA	100μA	**20μA**
V_{OC}*		600mV	600mV	**450mV**
Input Capacitance		2nF	8nF	8nF
Other Capacitance		4nF	16nF	16nF
Inductance		1µH	2µH	0.5µH
IVR Frequency		10MHz	20MHz	2MHz
Harvesting Efficiency		81%	86%	82%
Input Ripple		0.31V	0.21V	72%
Battery Power(W)	Idle	0	0	0
	Active	0	0	0
Total Active Area (mm^2)	PMU+MPPT	0.011mm^2	0.011mm^2	0.011mm^2
	Photodiode	0.27mm^2	0.55mm^2	0.8mm^2
Load Duty Cycle**		98%	95%	15%
*600mV and 450mV are observed at 80 klux, 20 klux respectively. **Based on input voltage restore time.				

7.4 Discussions

7.4.1 EHDS integration with Dual-purpose photodiodes

Limited on-chip area has always been a universal concern for designers. While on-chip diodes can be used as PV diodes for harvesting, the area/cost overhead for devoted photodiodes can be high. Re-configuring photodiodes within image sensors (when applicable) for harvesting has been proposed as an alternative [69, 13, 70], with overhead in extra transistors that reduce the fill factor of photodiodes. Through careful time-multiplexing of

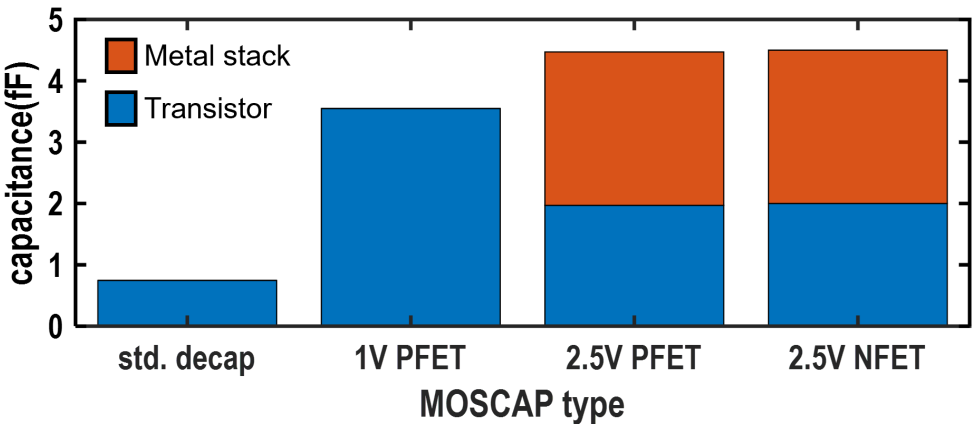


Figure 7.7: Simulated capacitance of different MOS-caps per unit area of standard cell decoupling capacitor (std. decap.)

harvesting and operation phases, energy-balance based autonomy has been demonstrated in these works. Park et.al.[71] implemented a different sensing mechanism to accommodate only the usage of the substrate-to-Nwell diode for harvesting, which allows simultaneous harvesting and sensing as well.

One of the key merits of the proposed EHDS is the small footprint needed for implementation. Therefore, it introduces very little overhead to systems that already have photovoltaic sensors within the design if integrated. Furthermore, specialized processes that are customized for image-sensing designs often use less metal stacks and allow higher transducing sensitivity and can therefore exhibit higher power density compared to that observed for standard CMOS processes [12].

7.4.2 Increasing input capacitance

Although the harvesting scheme presented in section 5.1 allows reduction in the minimum amount of passives required for input ripple filtering, the system still benefits from increased input capacitance. Apart from integrating on-board capacitors, methods to increase capacitance on-chip are also available. Two types of on-chip capacitors are typically available Metal-insulator-Metal (MIM) capacitors and Metal-oxide-semiconductor (MOS) capacitors. MIM capacitors generally reside in higher-level metals and are commonly used

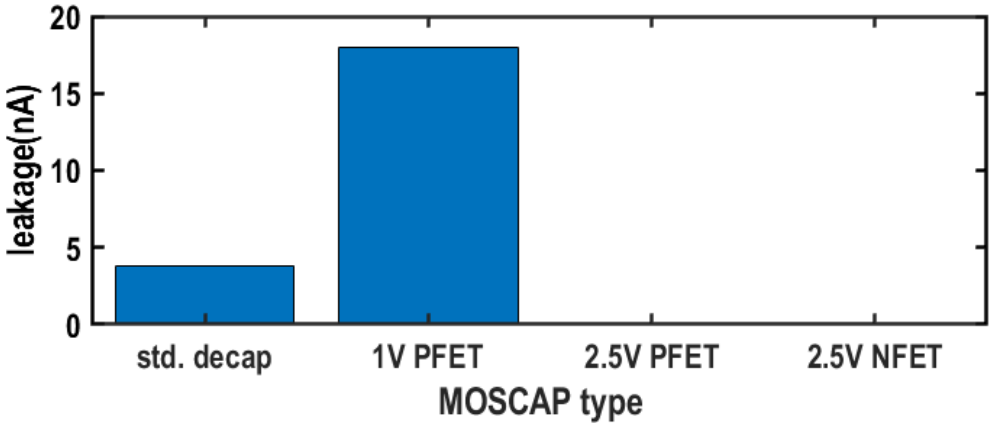


Figure 7.8: Simulated leakage of different MOS-caps.

to serve as explicit on-chip capacitors in IVRs. However, because on-chip photodiodes require metal vacancies for light to pass, vertical stacking of MIM capacitors over photodiodes would not be allowed. Therefore, placement of MIM capacitors would be restricted. A more promising candidate for increasing on-chip capacitance would be to use MOS capacitors instead. Because Fig. 7.7 shows a post PEX characterization of the capacitance that can be created with different configurations of MOS capacitors. Standard CMOS decoupling capacitors (std. decap) utilize both N-type and P-type transistors and can be integrated with synthesized logic easily. However, it's area utilization is also restricted. To increase the capacitance density, single transistor MOS capacitors are created under the same footprint restrictions. Using only 1V P-type transistors (PFET), the capacitance density can be increased by approximately 4.8 fold to 3.55fF per unit area. However, leakage is also increased linearly to 18 nA.

To reduce the leakage, 2.5V devices are also tested with slightly lower capacitance (2fF) but significantly lower leakage (74fA). Interleaved metal stacks are also created on top of the transistors to increase the capacitance further to 4.5fF in post PEX characterizations. A test-design shows that approximately 0.95pF capacitance can be integrated by fitting 2.5V MOS capacitors into every instance of each configurable photodiode in Fig. 6.9a without introducing any area overhead, which can lead to 121pF extra on-chip capacitance overall.

CHAPTER 8
CONCLUSION AND FUTURE WORK

Energy harvesting and delivery systems increase lifetime, robustness and energy efficiency of standalone systems. This thesis details design considerations and detailed implementation of EHDSs for sub-mW operation. The low footprint, fast wake-up attributes benefit many low duty cycle applications and can be widely adapted for use in modern day low-power SoCs. In this chapter, we walk through a summary of the main contributions of this thesis in section 8.1 and a brief discussion on future research opportunities in section 8.3.

8.1 Dissertation Summary

The thesis starts with verifying challenges in power management for standalone devices and introduces unique features that need to be addressed when energy harvesting is incorporated. Chapter 3 demonstrates a detailed analysis of PFM IVR operation and design trade-offs that affect loss and efficiency. A charge-equilibrium based transient modeling scheme is developed to capture multi-pulse operation for improved loss and efficiency modeling accuracy. The model is validated with silicon measurement and simulation data for PMU-only DC-DC conversion and further compared with transient simulation data for EHDS harvesting. Finally a demonstration of a fast co-design procedure with the model is presented for maximization of post-silicon conversion efficiency with embedded inductors.

After identifying critical design parameters that affect conversion efficiency, it is critical to understand at which points and what possible scenarios the PMU needs to prioritize designing for optimal system operation. Over-design can result in unnecessary overhead that can be otherwise avoided. A key metric that determines the lifetime of battery powered systems is the IDLE power. Instead of attempting to design the PMU to achieve high conversion efficiency for both high-power conversion when the load is ACTIVE and

low-power conversion when the load is IDLE, Chapter 4 introduces an alternative power management scheme where only the PMU consumes battery power and load activation is controlled based on input power available. Silicon measurements show a boosting time of 2.5ms under 5Klux illumination for a 3µF output capacitance. The testchip is then used to evaluate possible efficiency optimization schemes, PVT variation countermeasures and challenges for a key contribution of this thesis: PFM MPPT operation.

Chapter 5 presents an EHDS that has been designed to address challenges priorly outlined in Chapter 4. The system achieves up to 75% conversion efficiency and 85% source tracking efficiency and >99% system tracking efficiency with low footprint and passives. A wake-up assist circuit allows accelerated cold-start of only 3.8ms at 6klux illuminance. The time-based MPPT shows 9% increase in harvesting efficiency by tuning fractions of the fractional sample&hold circuit and 3% and 15% increase in conversion efficiency by tuning oscillator frequency under load and input voltage variations. Implementation details to reduce computation overhead for the digital TB-MPPT block and analog wake-up assist circuit are also presented.

Chapter 6 demonstrates a sample design of a low-power standalone device: a visible light based authentication IC. The design incorporates the power management scheme presented in Chapter 4 and further includes on-chip communication down-links and an encryption engine. Details of the AM sensing scheme are presented and discussed with characterizations from silicon measurements.

Chapter 7 discusses projections of a fully self-powered SoC by integrating prior designs presented in Chapter 4 to Chapter 6. A semi-simulator has been developed based on the DC-DC conversion model in Chapter 3 to evaluate EHDS performance when the PFM EHDS presented in Chapter 5 is used. Three EHDS designs are then presented based on diverse target specifications where on-chip harvesting with CMOS photodiodes are used to achieve system power autonomy.

8.2 Summary of Contributions

The key contributions of this thesis can be summarized as:

- **Development of an analytical model and simulator for PFM power conversion and harvesting:** A high accuracy model is developed to quickly explore high-level design of PFM IVRs and enable tailoring the EHDS design depending on the target loading module/input source behavior. The model is verified by both simulation and silicon data. Harvesting voltage tracking is additionally implemented to constitute a semi-simulator for PFM harvesting to model EHDS operation with limited power and is used for design projections for different target specifications where harvesting sources can be integrated on-chip.

- **Demonstrate system-focused solutions for ensuring robust PFM harvesting with reduced resources (capacitance, inductance, footprint):** Critical challenges for PFM harvesting are identified with silicon measurements and used as guidelines to design an all-in-one solution for low-power energy harvesting. The proposed approach "borrows" energy from IDLE states by increasing the input regulation window while controlling thresholds to ensure energy equilibrium. A complete system is developed to adapt to this change including an output-based MPPT tracking algorithm, configurable sampling fraction based harvesting efficiency tuning and switching frequency based conversion efficiency tuning. The approach also reduces the passives needed for the EHDS. Wake-up assist circuitry is designed to accelerate bootstrapped cold-start operation while introducing little area overhead for implementation.

- **Design and testing of a visible-light (VL) centric authentication SoC:** A low-power sensing method with on-chip photo-diodes for visible-light based data receiving is developed to and integrating with a off-chip harvesting power link to

demonstrate full interrogation cycle of a low-power authentication IC. A converter-embedded load-wake-up scheme is created with a pulse frequency modulated (PFM) boost regulator (BR) is designed with input-power based load control. The implementation decouples high-power loads from battery power and uses the PFM-BR for on-demand power delivery from harvesting sources. This approach reduces system IDLE power significantly by ensuring that only the PFM-BR remains ON and "waiting" for on-demand operation and that loads are activated only when input power is adequate. Additional power-gate control with existing PFM BR regulation signals enhances wake-up operation robustness by reducing BR load during system wake-up. Projected self-powered design with prior PFM EHDS is also presented.

8.3 Future Research Opportunities

With the prior techniques implemented, a fully self-contained EHDS for low-power harvesting has been demonstrated. However, the design still relies on off-chip inductors to provide sufficient inductance for the IVR to boost from low voltages without introducing voltage ripples that cannot be controlled. Preliminary tests and simulations indicate that it is possible to create PFM control based LDOs with the exact same control circuitry of PFM BRs by disabling lower-side power stage (N-type) in a typical IVR design. Though higher ripple is introduced from the hysteresis regulation compared to analog/digital high-speed low dropout regulators (LDOs), sufficient margin is still guaranteed ($V_{ripple} \sim 50$mV) for digital loads. To integrate PFM LDOs into EHDSs, however, several measures must also be taken. The basis of LDO operation inherently assumes that the input voltage must be higher than the target voltage levels of the load. Therefore, the first modification is to ensure the harvesting voltage remains high. Instead of converting back to parallel diodes after wake-up, diodes should remain stacked during typical operation as well. Furthermore, instead of entering bootstrapped operation after wake-up, the wake-up assist circuitry should maintain V_{IN}-to-V_{CTRL} connections throughout system operation. A second modification

needed is additional control to maintain input voltage levels are needed, operation of analog comparators suffer from the same PVT variations as the oscillator in subsection 4.4.1. As the input voltage is now supplying the LDO control voltage, additional measures such as modifying harvesting source stacks based on input intensity [14] should be considered either as a part of MPPT or as an individual block.

Another direction is to implement a system level resource-optimization approach. Operations of low-power SoCs often happen in sequential block/module activation. Instead of only connecting loading modules to the PMU output voltage (V_{OUT}), one can re-use unoperating modules as additional on-chip capacitance that can be distributed to input/output nodes of the PMU as needed. For example, up-link transmission modules typically only operate for a short period of time at the end of every system cycle to communicate computed/sensed results. Connecting the module to the PMU output would result in a rough power consumption of $I_{leakage}/\eta_{conversion}$ that will be opposed on the harvesting source. However, by connecting the module to the input, not only is the loss in conversion mitigated, but the leakage is also reduced due to the lower voltage ($V_{OUT} > V_{IN}$ for BRs). Furthermore, the decoupling capacitors in the module can then be used as input capacitance, which would be blocked by the in the original configuration. However, for this implementation to be realistic, even with clock gating, leakage of loading modules must be reduced to a minimum with either ground-side power gates or by designing with high-voltage devices or in low-leakage processes.

The current target application targets one-shot interrogation schemes where each access is independent of another. However, this is not always the case. To restore critical data and states after a power-interruption, non-volatile storage is often needed in processors that operate on state-dependent computation. To reduce energy consumption from data movement to storage macros, non-volatile flip-flops have also been proposed [72]. Integrating non-volatile devices into the current system would allow check-pointing [73] when input power fluctuates and could be one of the more useful research directions that will not only

increase the robustness of the harvesting system but also allow a vast variety of potential applications to be realized.

Appendices

APPENDIX A

PUBLICATION LIST

Journal:

- **E. Lee**, N. M. Rahman, V. C. K. Chekuri, A. Singh and S. Mukhopadhyay, "A low power authentication IC for visible light based interrogation," in IEEE Transactions on Industrial Electronics.
- **E. Lee**, V. C. K. Chekuri and S. Mukhopadhyay, "A PFM boost harvester with System-level Self-tuned Maximum Power Point Tracking," in IEEE Transactions on Power Electronics. (Submitted)

Conference:

- **E. Lee**, M. F. Amir, S. Sivapurapu, C. Pardue, H. M. Torun, M. Bellaredj, M. Swaminathan and S. Mukhopadhyay, "A System-in-Package Based Energy Harvesting for IoT Devices with Integrated Voltage Regulators and Embedded Inductors," 2018 IEEE 68th Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2018, pp. 1726-1731
- **E. Lee**, N. M. Rahman, V. C. Krishna Chekuri and S. Mukhopadhyay, "An Authentication IC with Visible Light Based Interrogation in 65nm CMOS," 2020 IEEE Custom Integrated Circuits Conference (CICC), Boston, MA, USA, 2020, pp. 1-4
- V. C. K. Chekuri, A. Singh, N. M. Rahman, **E. Lee** and S. Mukhopadhyay, "Aging Challenges in On-chip Voltage Regulator Design," 2020 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 2020, pp. 1-8
- N. M. Rahman, **E. Lee**, V. C. Krishna Chekuri, A. Singh and S. Mukhopadhyay, "A Configurable Dual-Mode PRINCE Cipher with Security Aware Pipelining in 65nm

for High Throughput Applications," 2020 IEEE Custom Integrated Circuits Conference (CICC), Boston, MA, USA, 2020, pp. 1-4

- V. C. Krishna Chekuri, N. M. Rahman, **E. Lee**, A. Singh and S. Mukhopadhyay, "A Fully Synthesized Integrated Buck Regulator with Auto-generated GDS-II in 65nm CMOS Process," 2020 IEEE Custom Integrated Circuits Conference (CICC), Boston, MA, USA, 2020, pp. 1-4

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