

**DESIGN, MODELING, OPTIMIZATION, AND BENCHMARKING  
OF INTERCONNECTS AND SCALING TECHNOLOGIES AND  
THEIR CIRCUIT AND SYSTEM LEVEL IMPACT**

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The Academic Faculty

by

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**DESIGN, MODELING, OPTIMIZATION, AND BENCHMARKING  
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*For my parents*

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## **LIST OF SYMBOLS AND ABBREVIATIONS**

AES	Advanced Encryption Standard
Al	Aluminum
ALD	Atomic Layer Deposition
ALU	Arithmetic Logic Unit
AR	Aspect Ratio
BCB	Beyond CMOS Benchmarking
BEOL	Back End of Line
CAD	Computer Aided Design
CD	Critical Dimension
CGP	Contacted Gate Pitch
CMOS	Complementary Metal-Oxide-Semiconductor
CMOSH <sub>P</sub>	CMOS High Performance
CMOS <sub>LV</sub>	CMOS Low Voltage
CMP	Chemical-Mechanical Polishing
Co	Cobalt
CPI	Cycles per Instructions
CPU	Central Processing Unit
Cu	Copper
CVD	Chemical Vapor Deposition
DTCO	Design Technology Co-Optimization
EDA	Electronic Design Automation
EDP	Energy Delay Product

FEOL	Front End of Line
FinFET	Fin Field-Effect Transistor
GAA	Gate-All-Around
IC	Integrated Circuit (IC)
ILD	Interlayer Dielectric
LDPC	Low Density Parity Check
LER	Line Edge Roughness
LFET	Lateral Nanowire Gate-All-Around Field-Effect Transistor
MB	Metal Barrier
MP	Metal Pitch
NW	Nanowire
P&R	Place and Route
PDK	Process Design Kit
PDP	Power Delay Product
PPA	Power Performance Area
PVD	Physical Vapor Deposition
RC	Resistance Capacitance
RMG	Replacement Metal Gate
RTL	Register Transfer Level
Ru	Ruthenium
SCE	Short Chanel Effect
Ta	Tantalum
TaN	Tantalum Nitride
TEM	Transmission Electron Microscopy
TFET	Tunneling Field Effect Transistors

ThinTFET Two-dimensional heterojunction interlayer TFET  
TMD Transition Metal Dichalcogenide  
VNW Vertical Nanowire

## SUMMARY

This research focuses on the future of integrated circuit (IC) scaling technologies at the device and back end of line (BEOL) level. This work includes high level modeling of different technologies and quantifying potential performance gains on a circuit and system level. From the device side, this research looks at the scaling challenges and the future scaling drivers for conventional charge-based devices implemented at the 7nm technology node and beyond. It examines the system-level performance of stacking device logic in addition to tunneling field effect transistors (TFET) and their potential as beyond-CMOS devices. Finally, this research models and benchmarks BEOL scaling challenges and evaluates proposed technological advancements such as metal barrier scaling for copper interconnects and replacing local interconnects with ruthenium. Potential impact on performance, power, and area of these interconnect technologies is quantified for fully placed and routed circuits.

# CHAPTER 1. INTRODUCTION

## 1.1 Device Scaling: Moore's Law and Dennard Scaling

The computing and semiconductor revolution of the past 50 years has been driven by the extraordinary scalability of integrated circuits (IC). The transistor counts of ICs have roughly doubled every 2 years, enabling increasing functionality and reducing cost per transistor, accompanied by an era of improving device performance as showcased in Figure 1. The doubling of transistors every 2 years was first observed by Gordon Moore in 1965 [1]. Following Moore's observation, Dennard from IBM presented the traditional scaling relationship of planar MOSFETs. In his paper, he describes how scaling transistor dimensions and oxide thickness while increasing channel doping improves device performance at a similar rate for the same power density [2]. This continuous scaling of transistors provided a roadmap for the semiconductor industry to enable ever increasing performance at reduced cost for many decades [3].

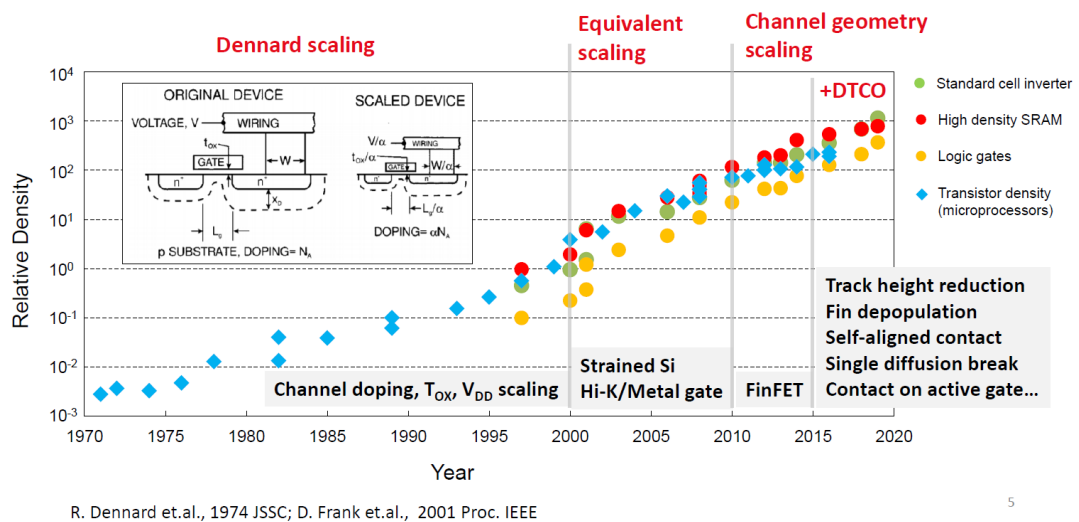
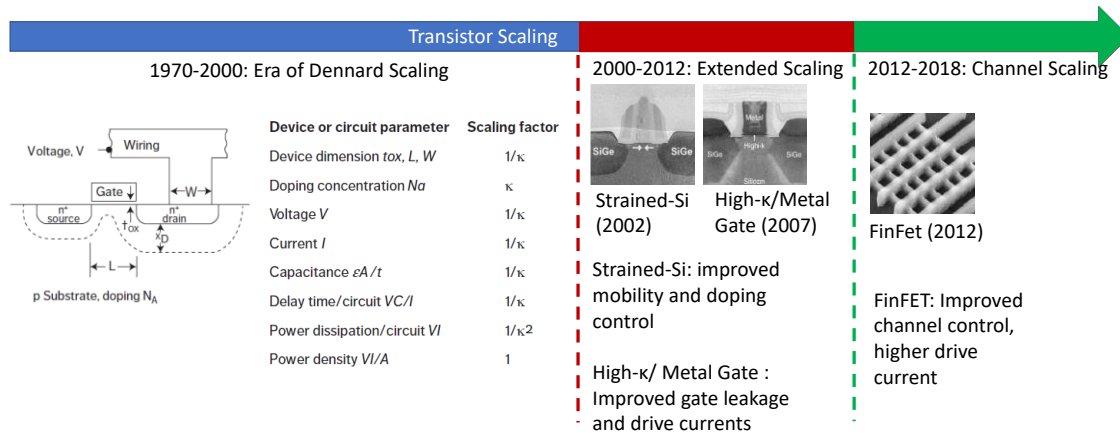


Figure 1 – Moore's Law: History of Scaling and Innovations [4]

### 1.1.1 Traditional Planar Device Scaling Challenges

As device scaling successfully continued into the early 2000, new challenges started to arise. When device performance improvements slowed due to limits in channel doping, the industry moved to stressed and strained channels to help improve electron mobility while minimizing device leakage. In traditional Dennard scaling, gate oxide thickness scaling is also necessary to maintain the same gate capacitance. By the early 2000, the industry standard SiO<sub>2</sub> gate oxide had reached its scaling limits, with tunnelling current through the gate dielectric becoming a substantive portion of power dissipation. This required the industry to innovate towards high- $\kappa$  dielectric materials like hafnium oxide, which enabled thicker oxides that reduced tunnelling currents. With these innovations, performance scaling was maintained through the 2000s [3].

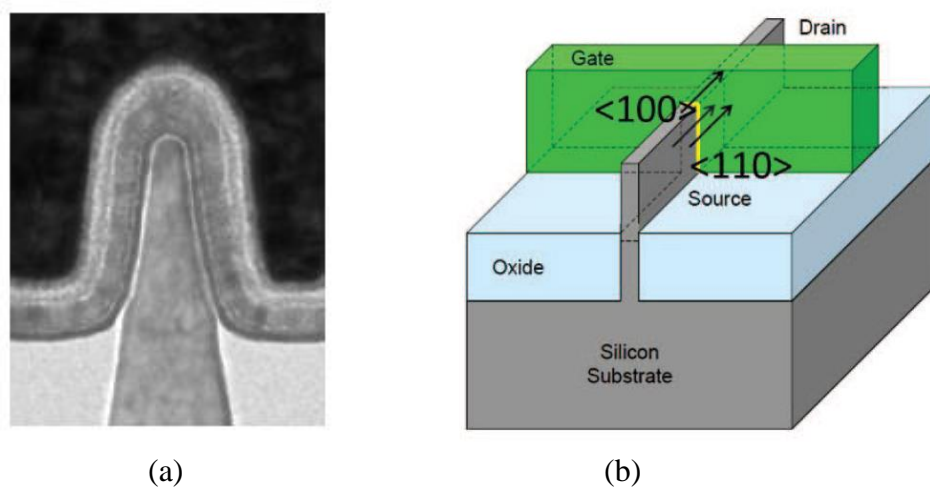


**Figure 2 – Eras of Transistor Scaling Innovations [2-5]**

### 1.1.2 Challenges of device scaling sub 22nm: Movement to FinFET

Despite the many innovations to extend planar MOSFET scaling, there was difficulty maintaining the same progress below 32nm. At the 22nm technology node, the

industry started moving from planar MOSFETs to FinFET devices (also referred in literature as tri-gate) as shown in Figure 3. FinFETs offer better performance per unit power compared to traditional planar MOSFETs. This is achieved by increasing the effective gate capacitance by raising the channel above the substrate plane resulting in fin-like structures [6]. The gate wraps around the raised portion of the device on three sides, increasing the capacitive surface area per planar footprint area. This allows the reduction of device leakage currents and enables lower threshold-voltages through better gate control. As device scaling continues to the 7nm and 5nm nodes, new device structures are being examined as potential successors to current FinFET technologies.



**Figure 3 – (a) Transmission Electron Microscopy (TEM) of PMOS Tri-gate/FinFET channel under the gate [4] (b) Tri-gate/FinFET transistor architecture [7]**

### *1.1.3 Gate-All-Around devices and Complementary Logic*

With the success and wide adoption of FinFET devices, additional challenges emerged for the sub-5nm technology nodes. Short-channel effects and doping variations become a challenge for maintaining device density and performance at these small

dimensions. Due to the increasing challenges of FinFET technology, the next evolution for the ultimate CMOS device is the gate-all-around (GAA) device. In a GAA device, the entire channel is surrounded by the gate on all sides, providing the ultimate electrostatic control. One promising candidate for GAA is the lateral nanowire gate-all-around FETs (LFET) with its improved electrostatic control and compatibility with high- $\kappa$  gate dielectric and stressed channels [8-10].

While LFETs have promising scaling opportunities, interconnect scaling has increasingly become a bottleneck in IC performance. Interconnect resistivity is increasing with scaling due to size effects, and interconnect capacitance scaling faces many challenges and limitations due to mechanical requirements [11]. By stacking transistors on top of each other, a more compact logic cell can be achieved with a smaller footprint area. This helps to reduce the average interconnect length, improving overall system performance. Although both vertical and lateral stacked structures are possible for nanowire GAA FETs, the lateral topography of LFETs is less disruptive to existing CMOS technologies and design. In addition, a strain relax buffer can provide channel stress and improve mobility for LFETs [10, 12].

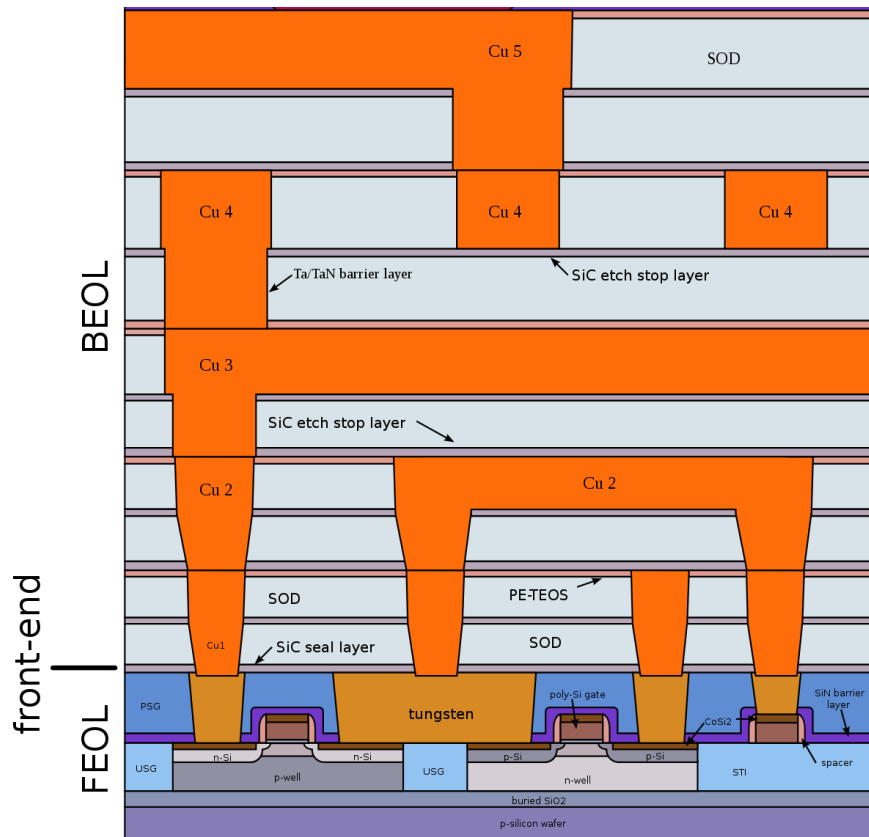
#### *1.1.4 Beyond CMOS Devices: TFETs*

As traditional IC technologies approach fundamental scaling limits due to electron thermal energy and undesired tunneling currents, new classes of devices are being explored as potential alternatives to achieve optimal device performance and energy consumption. For low-power applications, in recent literature, the tunneling field-effect transistor (TFET) device has gained a lot of popularity due to its low leakage properties.

In a conventional thermionic MOSFET, device current is controlled by raising and lowering the energy barrier height through which electrons are injected from the source to drain. This barrier height is modulated by adjusting the gate voltage. In TFET devices, the primary current injection method is by interband tunneling. Instead of modulating the barrier height, the barrier width is modulated to allow interband tunneling when the TFET is turned on. TFETs promise low leakage, steep subthreshold slopes and low supply voltages, but also have low on-currents. In addition, TFETs generally have a larger footprint compared to CMOS and have unidirectional current flow. With these potential benefits and drawbacks, it becomes important to understand how these devices would perform compared to conventional CMOS technology [13, 14].

## **1.2 Interconnect Scaling and Challenges**

Transistors are fabricated on silicon wafers in a series of processes often referred to as the Front-End-of-Line (FEOL). After device fabrication, the transistors need to be functionally connected to one another. This is done through metallization layers that connect all the devices together and is often referred to as the Back End of Line (BEOL) as shown in Figure 4.

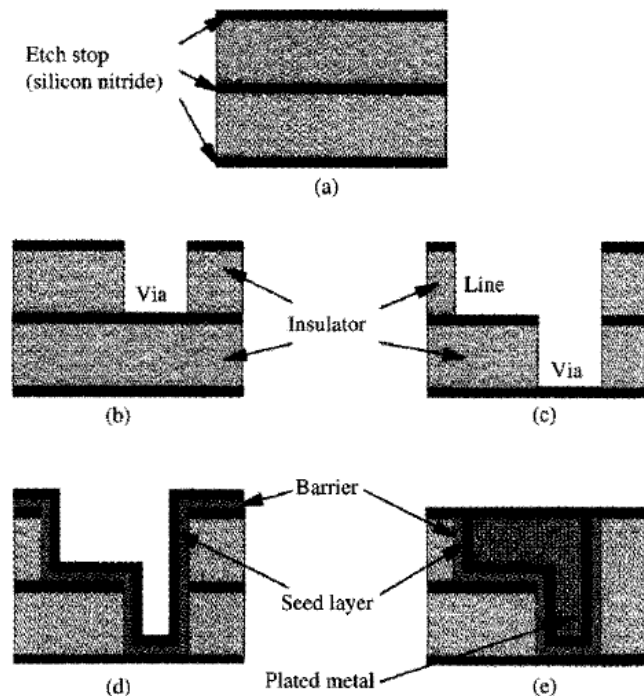


**Figure 4 – CMOS Chip Structure in 2000s (Cepheiden, Wikipedia 2006)**

In traditional dimensional scaling of interconnects, when the transistors shrink in dimensions, the interconnect's parasitic capacitance also decreases. However, this scaling also increases the resistance of the interconnects because of the reduced cross-sectional area, ensuring the overall RC delay generally remains constant. Traditional with each successive technology node, device performance improves while interconnect RC delay stayed constant and increasingly contributed to a larger share of the total delay. New advances to interconnect delay are required to improve the performance of ICs.

### 1.2.1 Traditional Al interconnects to Cu

In the past, aluminium (Al) was used as the main interconnect conductive material due to its relative ease of processability and compatibility with silicon. However, due to the increasing share of the delay coming from interconnects, new materials were required to improve interconnect resistance and thereby IC performance. Copper (Cu) became the industry standard wiring metal of choice due to its high conductivity, better reliability and higher resistance to electromigration. Cu has a bulk resistivity of  $1.7\mu\Omega\text{-cm}$  compared to aluminium's  $2.7\mu\Omega\text{-cm}$ . The two main challenges of using copper are that it requires a barrier/liner bi-layer material to prevent the diffusion of Cu into the surrounding dielectric and to ensure a void-free Cu fill. In 1997, IBM researchers demonstrated Cu dual damascene process integration for the BEOL stack which continues to be the industry standard to today [15]. A typical dual damascene process flow is shown in Figure 5 [15, 16].



**Figure 5 – Dual Damascene Process [5]: a) Deposition of ILD with etch stop, b) Pattern and etch via trench, c) Pattern and etch wire trench, d) barrier and metal seed-layer deposition, e) Cu electroplating, CMP, and capping layer**

### *1.2.2 Challenges of Cu interconnects and size effects*

Modern scaling of copper interconnects presents many challenges. As wire dimensions scale below 22nm, copper resistance increases exponentially due to size effects. Some of these factors include decreased grain size, higher surface reflectivity, and poor scaling of highly resistive MB/liner materials which take up large portions of the copper wire volume. Additional technology innovations are required to further extend scaling for future technology nodes.

### *1.2.3 Low- $\kappa$ dielectric and air gap*

Beyond just improving interconnect resistance, interconnect capacitance is another area of focus for scaling and improvements. Interconnect capacitance contributes not only to RC delay, but also to dynamic power dissipation. The power dissipated in the interconnects is due to switching activity in the wire of all the nets. The main contribution to this power dissipation is from the wire and cell pin load capacitance. The primary method of reducing the interconnect capacitance is to use a low- $\kappa$  interlayer dielectric material (ILD) material. Conventionally, the ILD material used is SiO<sub>2</sub> with a dielectric constant of 3.9. To reduce the dielectric constant of a material, one can reduce the dipole interaction of the atoms and/or reduce the density of the material by increasing the interatom spacing. This can be achieved by doping the SiO<sub>2</sub> with carbon or fluorine. The integration of low- $\kappa$  dielectric has been implemented using carbon doped SiO<sub>2</sub>. The silicon bond to carbon has both smaller dipole interaction and creates larger interatom spacing. This results in a reduction of dielectric constant with reported values in the range of 2.6–3 [17].

Another method to reduce the dielectric constant is to introduce voids in the ILD material by using porous silicon. Adding pores to the ILD material can reduce the capacitance of the ILD with the trade-off of reducing the mechanical strength of the material. The chemical-mechanical polishing (CMP) processing during the dual damascene process introduces a lot of mechanical stress. If the ILD material is not mechanically stable enough, it can be damaged during the CMP process.

For the ultimate low- $\kappa$  dielectric material, an air gap would have a dielectric constant close to 1. Air gaps have been introduced to the BEOL stack starting in the 14nm technology node by Intel Corporation. However, there are many design rules and process challenges that restrict the usage of air gaps to a few layers in the overall stack [18].

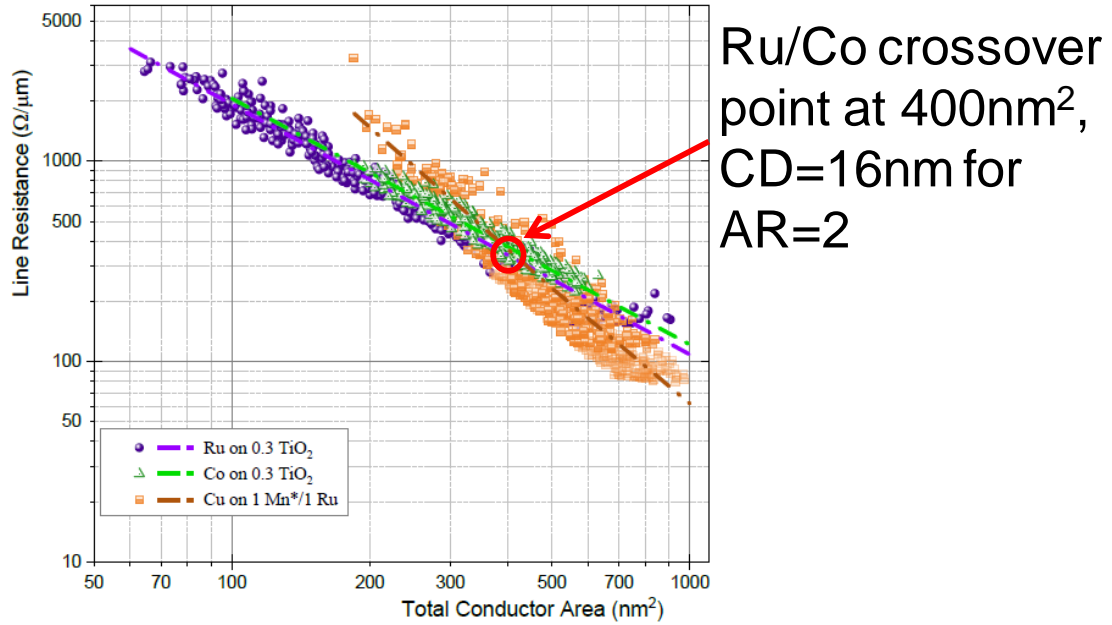
#### *1.2.4 MB/Liner and Reliability Challenges*

As IC scaling continues to 7nm technology node and beyond, wire dimensions are scaled to narrow pitches especially at the local metal-levels to accommodate dense logic and memory on chip. The copper metallization for the BEOL requires a barrier and liner material to prevent Cu from diffusing into the surrounding dielectric as well as provide a seed layer to ensure void free copper fill. The percentage of interconnect cross-sectional area occupied by the highly-resistive barrier liner for copper can be as much as 50% of the wire volume [19, 20]. The current industry standard metal barrier and liner bilayer material is Tantalum/Tantalum Nitride (Ta/TaN). While this bilayer material has been used successfully for many technology generations, it has been shown that it is difficult to scale beyond 4nm thickness [21, 22].

New bilayer materials have been proposed to extend scaling of the liner materials. It has been shown in literature that adding Ruthenium (Ru) or Cobalt (Co) to the barrier material TaN can help maintain barrier integrity of TaN for thicknesses as low as 0.8nm [22]. TaN/Ru and TaN/Co bilayer materials as thin as 2nm have been demonstrated to pass most reliability tests [22].

#### *1.2.5 New Metal Materials for Scaling of Local Interconnects*

Due to increasing copper resistivity from size effects for sub-20nm wires and challenges in metal barrier scaling, there have been proposals to use new metals for local interconnects such as Ruthenium (Ru) and Cobalt (Co). While these metals have a higher bulk resistivity compared to copper, they do not require a barrier and are less prone to size-effects that are observed in copper. Ru also has superior reliability and is more resistant to electromigration compared to Cu. Experimental data from literature shows that Ru and Co have better resistances per unit length compared to copper for feature sizes below 16nm for aspect ratios (AR) of 2 [23] as seen in Figure 6. These new metal options have great potential to replace Cu interconnects for sub-16nm local interconnects.



**Figure 6 – Comparison of Cu, Ru, and Co Line Resistance versus Total Conductor Area [23]**

### 1.3 Thesis Overview

With IC scaling challenges driving many technological innovations, it becomes important to understand the performance implications. In the following chapters, we will explore some of these future scaling enablers and proposed new devices that will further extend scaling and performance gains in the future.

## **CHAPTER 2.     STACKED LOGIC DEVICE FOR LATERAL NANOWIRE FIELD-EFFECT TRANSISTORS (LFET)**

Previous works have extensively examined the device performance of various configurations of LFETs with different source/drain contacting schemes [9, 10, 24]. A wrap-around contact scheme for the source and drain, where contact is directly made to a fin of Si and SiGe lattice, reduced contact resistance and improved ON currents for the device [10].

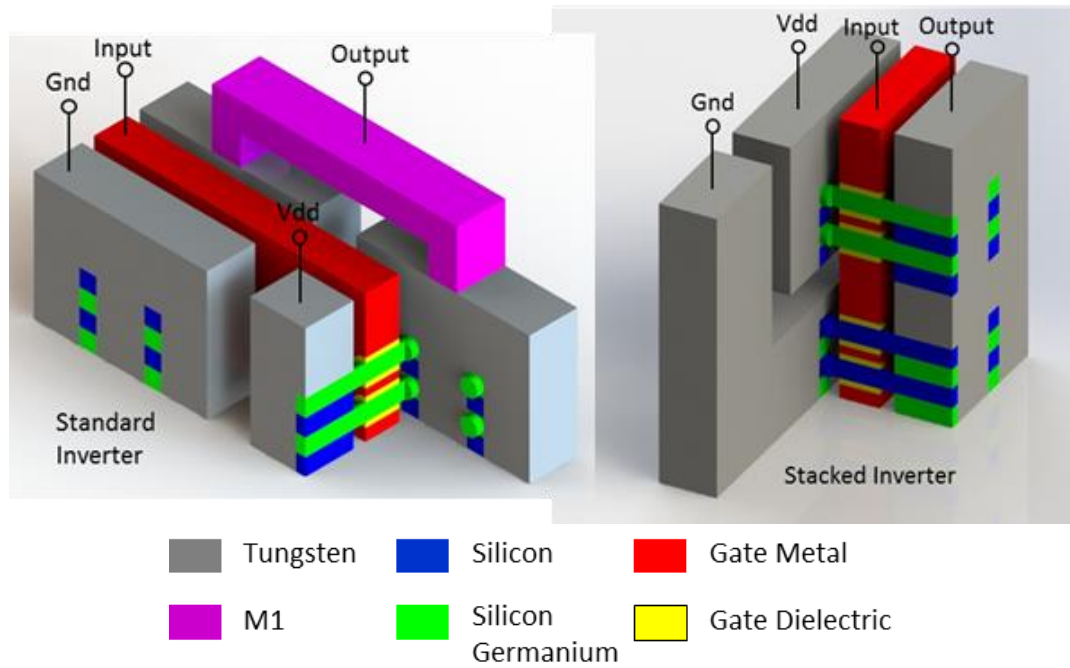
To further improve the device density and performance, two CMOS logic structures are proposed that utilize stacking of n- and p-type LFETs on top of each other to achieve a more compact logic cell. Reducing the cell area reduces the average interconnect length, improving interconnect and system performance. This stacked approach for a more compact device is complementary to current efforts to continue technology scaling and does not suffer from the same issues the industry faces in the scaling of gate pitch, metal pitch and fin pitch. Some of those issues include reduced electrostatic control due to short channel effects (SCE), increased wire resistance due to size effects, and increased contact resistance and gate fill considerations. To quantify the potential performance of such devices, the parasitic capacitance and resistances are accurately captured by an electrostatic field solver and are compared against LFETs. In addition, system-level performance analyses are performed to capture the impact of the reduced cell area on overall system performance. The stacked structure leads to shorter interconnects, reducing overall delay. System-level analyses also enable the study of trade-offs among performance, power, and

area, giving insights to interconnect and thermal related issues that cannot be captured at only the device-level benchmarking.

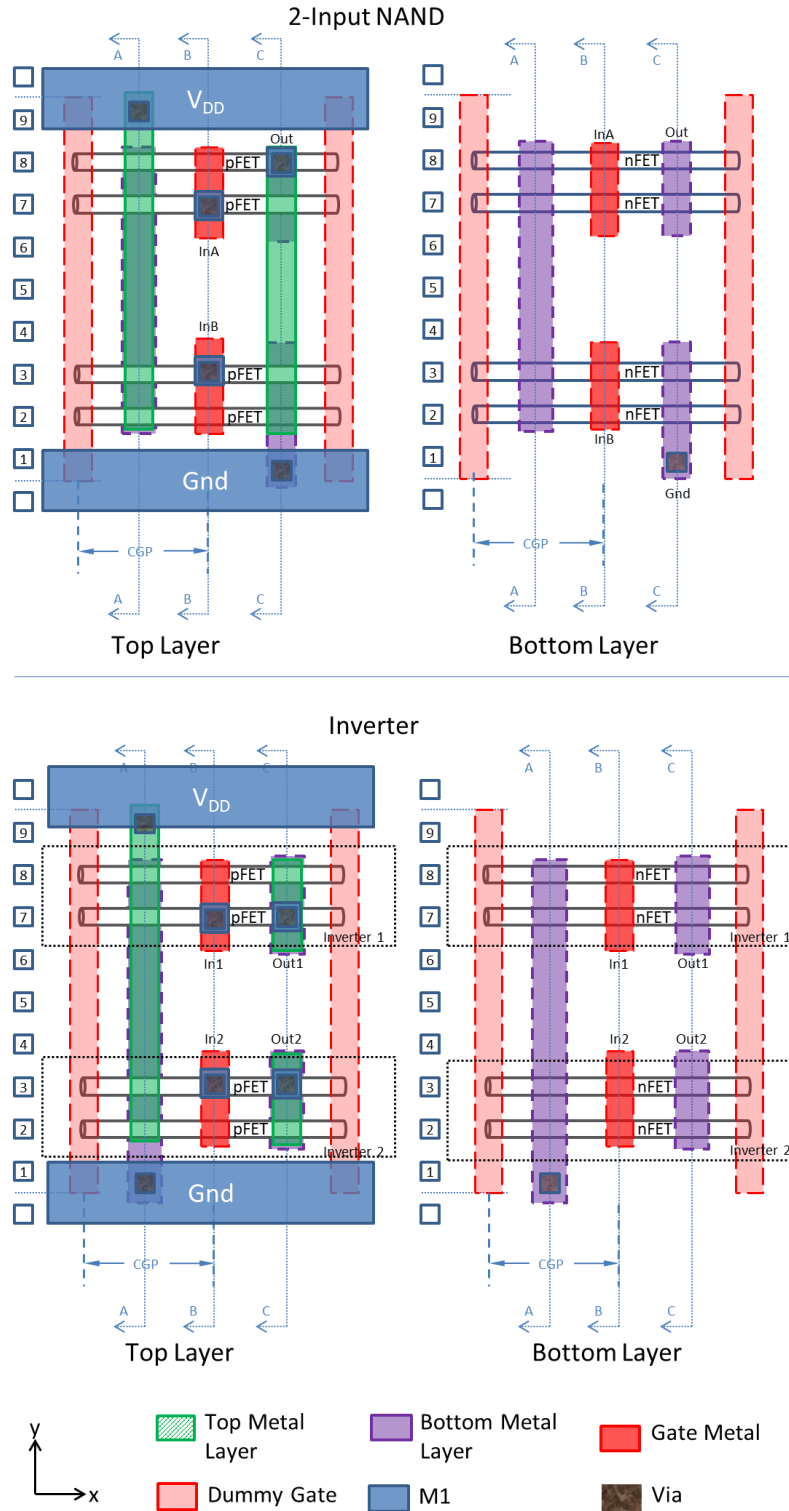
## **2.1 Stacked Device Layout and Structure**

Two stacked logic CMOS structures for LFETs are proposed in this chapter: inverter and 2-input NAND. The basic LFET structures and device characteristics are based on work from [9, 10, 24]. The stacked logic CMOS structure consists of an NFET layer at the bottom and a PFET layer on top. This structure, where every NFET is paired with a PFET, is a natural complement for CMOS design. 3D models for a typical 2D inverter structure and stacked inverter are depicted in Figure 7.

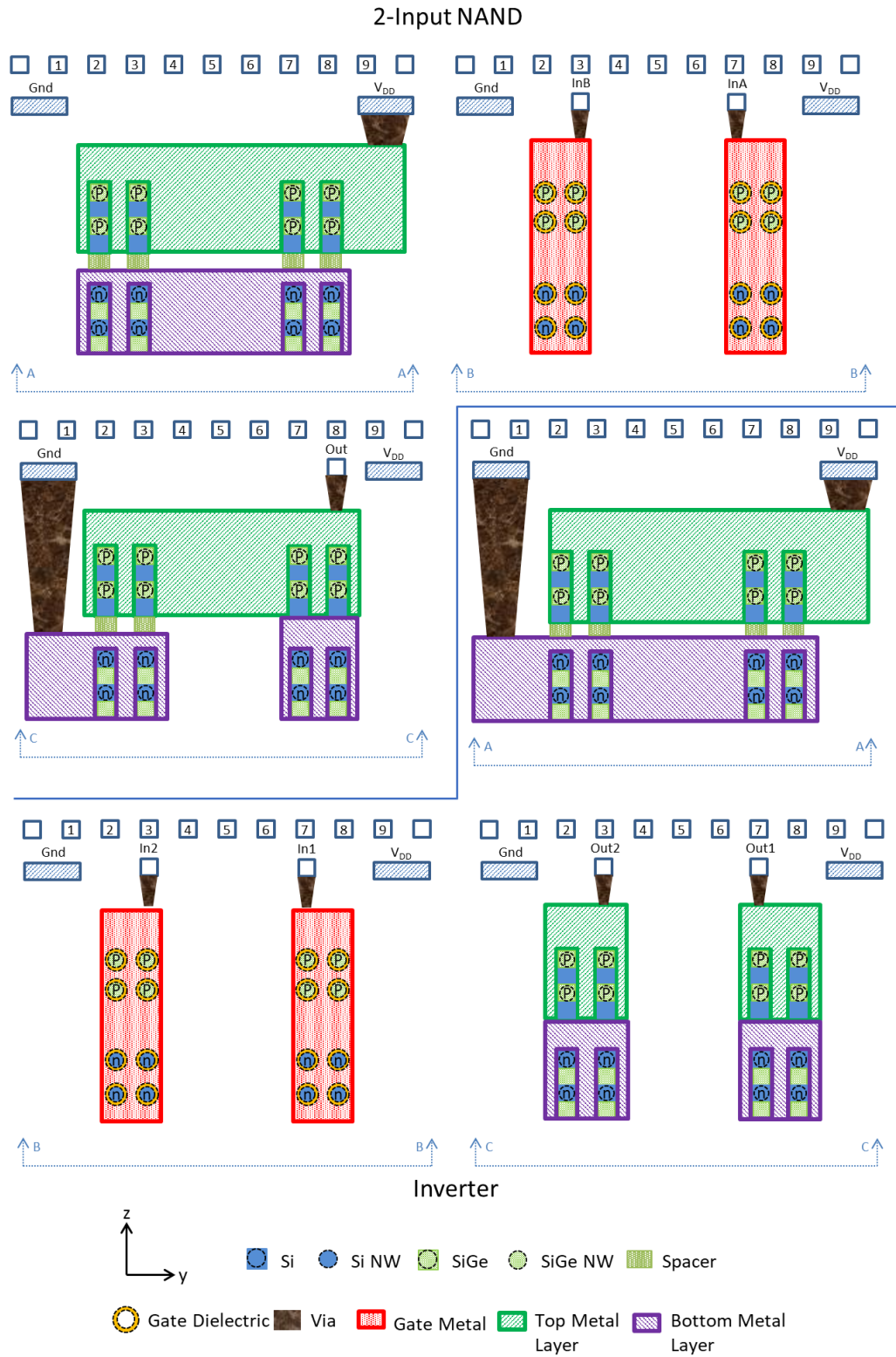
Figure 8 shows the top layout view for an inverter and NAND2 cell. The cell heights for both devices are 9 metal pitches (MP), with top and bottom supply and ground rails. Figure 9 shows the cross sections of the inverter and NAND2 cells. Separate  $V_{dd}$  and ground rails at M1 allow ready access for chip level routing via higher metal levels.



**Figure 7 – 3D sketch of a standard cell 2x2 LFET inverter and a stacked 2x2 LFET inverter.**



**Figure 8 – Top view of stacked 2-Input NAND structure and inverter. The top layer shows the M1 supply and ground rails with the PFET transistors connections, and the bottom layer shows the NFET connections.**



**Figure 9 – Cross sectional view of stacked 2-Input NAND structure and inverter. The cell height in metal pitches is numbered on top.**

The layouts presented for the two logic cells use the same cell height to conform to physical layout design standards. The metal routing is also unidirectional for a lithography friendly design. The cell height for a single device is 3 metal pitches (MP) by 2 contacted gate pitches (CGP) wide. For a conventional structure, the inverter gate has a cell height of 9 MP and is 2 CGP wide, and for a NAND2 gate the cell height is 9MP and its width is 3 CGP. By stacking PFETs on top of the NFETs, two inverters can fit into the same footprint as the conventional layout, reducing the effective cell area of a single inverter by 50%. For the NAND2 cell, the stacked structure can fit in the same cell footprint of a 2D inverter, reducing the cell width from 3 CGP to 2CGP. This results in a reduction in area by 33%. The area comparison between the standard architecture and stacked LFET structure is summarized in Table 1. The basic process assumptions are summarized in Table 2.

**Table 1 – Standard 2D Cell and Stacked Cell Footprint Summary and Comparison**

<b>Logic Cell</b>	<b>Std. Cell Footprint</b>	<b>Stacked. Footprint</b>	<b>% Reduction</b>
NAND2	27 MP·CGP	18 MP·CGP	33
Inverter	18 MP·CGP	9 MP·CGP	50

**Table 2 – Process Assumptions for 2x2 LFET**

Parameters	Values
Contacted Gate Pitch, CGP [nm]	32
Metal Pitch, MP [nm]	24
NW Diameter, $D_{nw}$ [nm]	7
Gate Oxide Thickness, $T_{ox}$ [nm]	0.5 nm SiO <sub>2</sub> 1.5 nm HfO <sub>2</sub>
Gate Length, $L_g$ [nm]	14
Spacer Thickness, S/D extension [nm]	5
Nanowire Pitch [nm]	14
S/D Width [nm]	20
Fin Pitch [nm]	27
Vertical Nanowire Pitch (VNW) [nm]	14
$\epsilon_{spacer}$	5.5

## 2.2 Device Parasitic Modeling

The device characteristics and performance for different configurations of LFETs using standard layout architecture are investigated in references [9, 10, 24]. The performance of LFETs with different configurations is benchmarked at the system level [24], indicating that a LFET structure utilizing 2fins/2stack (2x2) provides best performance-energy trade-offs. Therefore, the 2x2 LFET structure is used for the baseline and stacked structure. The parasitic capacitance and resistance for the stacked inverter structure are characterized and compared with a model of the standard inverter layout. The

3D field solver Raphael [25] is used to model the parasitic capacitance and resistance of the inverter structures.

### 2.2.1 Parasitic Capacitance

3D models of the standard inverter and the stacked structures are created in Raphael to analyze and compare the input gate capacitance for both structures. Key process assumptions and parameters in Table 2 are used to create the models in Raphael.

In the basic 2x2 LFET structure, the vertical nanowire pitch is 14 nm and the fin height is 28 nm. In the LFET models presented in [9], the LFET device has a gate-to-top dimension of 25 nm. This requirement is based on the replacement metal gate (RMG) process requirements and access resistance considerations [26, 27]. In the stacked inverter structure, the gate can be formed in the same process steps for both the NFET and PFET input since they are tied together for the inverter and NAND2. The gate-to-top dimension for the bottom transistor can therefore be relaxed, leading to a shorter device height. A shorter device height reduces the overlap capacitance between the gate and source/drain contacts, leading to a reduction in input gate capacitance of 13% compared to the standard inverter structure. The Raphael capacitance model results are summarized in Table 3.

**Table 3 – Parasitic Input Capacitance for Standard and Stacked Cells, and Parasitic Resistance for Stacked Cells for 2x2 LFET Inverter**

Inverter Parasitic Parameters	Values
Standard Cell Input Capacitance [aF]	403
Stacked Parasitic Capacitance [aF]	351
Stacked Parasitic Resistance [ $\Omega$ ]	229

### 2.2.2 *Parasitic Resistance*

The parasitic resistance modeling of the LFET is based on the wrap contact reported in [10] where the source/drain contacts are made of tungsten. For the stacked inverter structure, the access to the bottom electrodes requires going through the top layer, increasing parasitic access resistance for the stacked structure.

For the stacked inverter, the pull-up network is the same as the unstacked case since it is located on top and readily accessible. However, the access resistance increases for the pull-down network. An additional resistance path exists from the drain contact of the top transistor to the bottom drain, as well as a long ground via to the bottom transistor on the source side. The additional resistance path is modelled in three parts in Raphael. The first part consists of the PFET drain contact down to the top contact of the NFET drain. The second part consists of a long ground via from the M1 ground rail to the bottom NFET source contact. The last part consists of the side access of the source contact to the fins. The total stacked parasitic resistances for the top drain contact, ground via, and side access are evaluated in Raphael. The total additional access parasitic is evaluated to be  $459\ \Omega$ . Since this resistance only exists for the pulldown network, an average parasitic resistance of  $229\ \Omega$  is added to the intrinsic resistance for the benchmarking in the next section. This resistance provides an additional 38% of the parasitic access resistance evaluated in [24]. The stacked parasitic resistance is shown in Table 3.

## 2.3 **System-Level Modeling**

The system-level modeling is performed for the standard LFET structure and stacked logic structure. For the system-level simulation, a validated open source simulator IntSim [28] is adopted to efficiently evaluate the performance of the 2x2 LFET structures at the 5nm node. For a given operating frequency target, interconnect networks are optimized to obtain metal pitches on different metal levels for a given set of system parameters. The ON currents and leakage currents from [24] are used as input to the model. Device performance at three different supply voltages is analyzed: 0.6V, 0.5V and 0.4V. Total power is evaluated based on the dynamic and static components of the system. Input capacitance and resistances used in the system models are based on the minimum sized inverter.

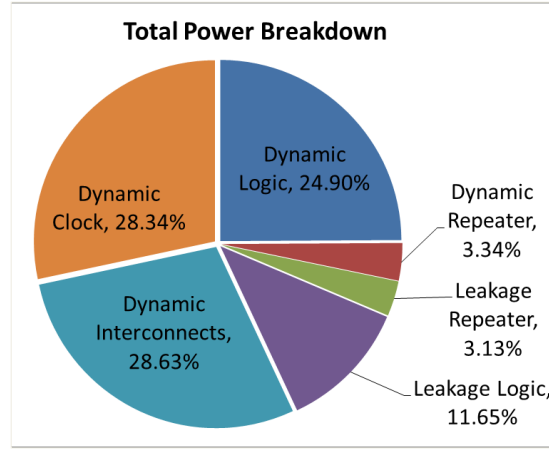
The stacked logic structure reduces the cell footprint of an inverter by 50% and a NAND2 by 33%. This reduction in area leads to shorter interconnects, improving overall interconnect performance at the system level. Because of the reduced footprint of the stacked cell, the chip area can also be reduced by 30% while still maintaining the same gate density as the unstacked case. Reductions in chip area further decreases average interconnect length and improves overall system-level interconnect performance.

Device parasitic properties figure prominently in the model. The input capacitance is the dominant component for calculating dynamic logic and clock power, and an increase in access resistance impacts the critical path delay.

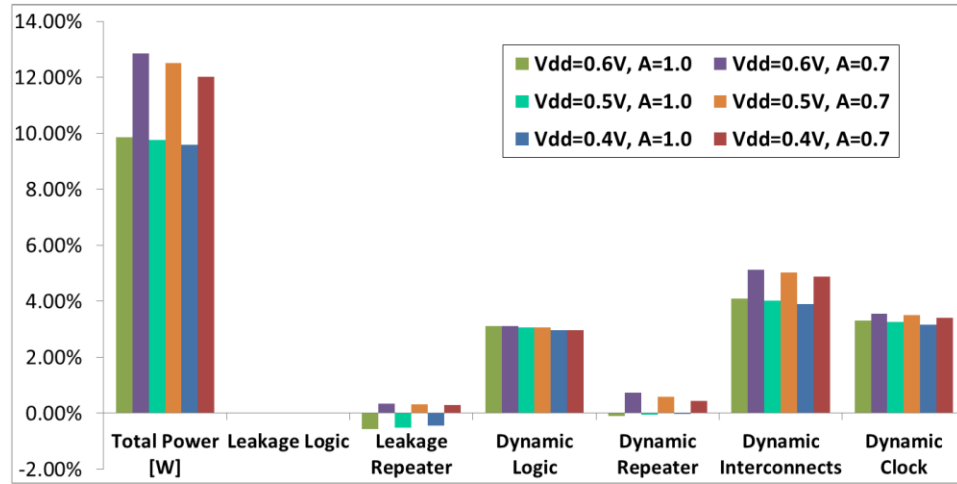
## **2.4 System-level Benchmarking Results**

A total system power breakdown utilizing conventional standard cells for 2x2 LFET is presented in Figure 10(a). The supply voltage is set to 0.6V and the frequency is fixed at 1.1GHz. Dynamic power dissipations in interconnects, clock distribution and logic

gates are the largest components of the total power dissipation. Figure 10(b) shows the percent power savings for the stacked structure compared to the conventional layout for supply voltages of 0.6V, 0.5V, and 0.4V. The frequency is fixed at 1.1GHz and the available chip area for placement and routing is varied from  $0.7\text{mm}^2$  to  $1\text{mm}^2$ . The comparison in power savings is made with respect to the unstacked case with a chip area of  $1\text{mm}^2$ . A maximum power savings of 12.9% is observed at 0.6V supply voltage for a chip area of  $0.7\text{mm}^2$ . Shorter interconnects due to smaller cell footprint and chip area result in a 17.9% reduction in dynamic interconnect power, or 5.0% of the total power. A 13% reduction in input capacitance results in 12.5% reduction in dynamic logic and clock, or 3.1% and 3.6% of total power, respectively. The results in Figure 10 (b) reflect the improvement in interconnect and capacitance due to the smaller cell footprint and shorter NFET device.



(a)

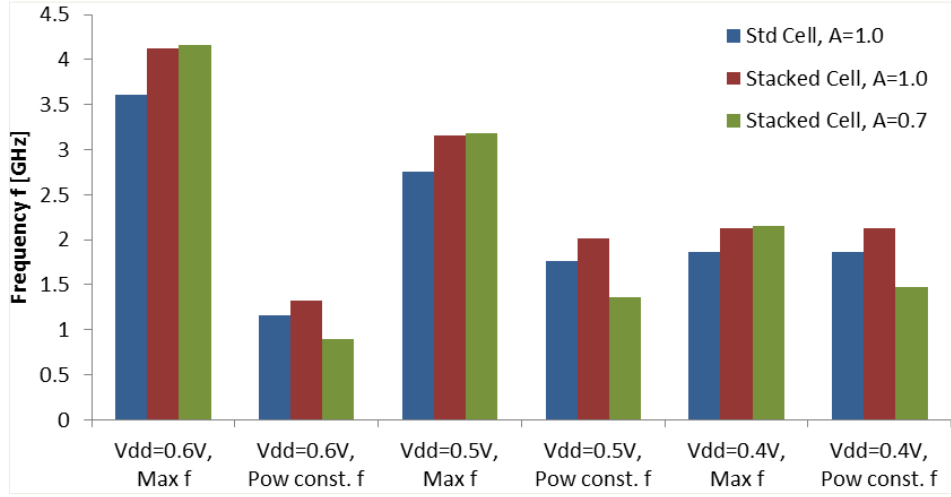


(b)

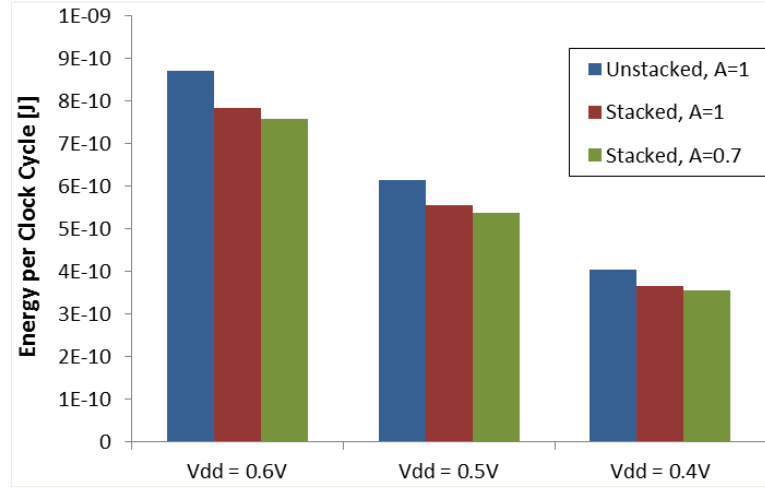
**Figure 10 – (a) Projected power breakdown for standard 2x2 LFET at 0.6V supply voltage and 1.1GHz. (b) Percent system power savings of stacked logic compared to standard LFET cell at 1.1GHz. Supply voltage is varied from 0.6V to 0.4V and chip area is varied from 1mm<sup>2</sup> to 0.7mm<sup>2</sup>. The percent power breakdown for different categories are normalized to the total power.**

Figure 11(a) shows the maximum operating frequency of the system and the maximum operating frequency for a power density budget of 100W/cm<sup>2</sup>. The overall operating frequency of the system, determined by the critical path delay, improves for the stacked logic design. This improvement is primarily driven by the reduction in interconnect length and device input capacitance. The impact on the delay due to the increased access

resistance is more than compensated by these improvements. With thermal considerations and a power density budget of  $100\text{W}/\text{cm}^2$ , the maximum operating frequency of the system becomes power limited. There is a trade-off in terms of power versus performance. When the system performance is limited by the power budget, reducing the supply voltage decreases the dynamic power of the system and allows a higher operating frequency. This is at the cost of an increased critical path delay due to lower ON currents. For supply voltages of 0.5V and 0.6V, the maximum operating frequency is power constrained. When supply voltage is reduced to 0.4V, the system becomes limited by the critical path delay.



(a)



(b)

**Figure 11 – (a) Maximum operating frequency (Max f) and power density constrained frequency comparison of standard and stacked cells. Stacked cell chip area is varied from 1 to 0.7mm<sup>2</sup>. (b) Energy per clock cycle comparison for stacked and unstacked logic. Frequency is set to 1.1GHz, supply voltage is varied from 0.6 to 0.4V, and stacked cell chip area is varied from 1mm<sup>2</sup> to 0.7mm<sup>2</sup>.**

When the system is power density constrained, the maximum frequency for the stacked case for a reduced chip area of 0.7mm<sup>2</sup> is lower than the unstacked case. This is primarily due to the power savings of 12.9% not scaling at the same rate as the chip area reduction of 30%.

The switching energy per clock cycle is plotted in Figure 11(b). The frequency is fixed at 1.1GHz and the supply voltage is varied from 0.6V to 0.4V. The stacked device exhibits better switching energy efficiencies due to shorter interconnects and improved device capacitance, which improves with smaller chip area. An energy reduction of 10% and 12-13% is observed for the stacked logic when chip area is  $1\text{mm}^2$  and  $0.7\text{mm}^2$ , respectively.

## **2.5 Conclusion**

Standard cells using stacked logic layout are presented for an inverter and a 2-input NAND gate. The new layout enables a 30% reduction in chip area for a given gate density. The new device structure also enables a shorter NFET, leading to a smaller input capacitance. Both the reduction in cell area and input capacitance allows the new structure to have up to 12.9% reduction in total power and 12-13% reduction in switching energy. In addition, creating a 3D structure as a standard cell and characterizing the parasitic of the cell allows compatibility with existing placement and routing tools.

While the new design structures offer potential improvements in both power and area, additional work is required to determine fabrication feasibility and cost concerns. A standard cell library can be generated to give a more complete and accurate analysis and benchmarking regarding the potential area savings from the stacked cell structure. Thermal considerations are required to evaluate the impact to the system performance, especially for a power density limited situation.

# **CHAPTER 3.     GENERIC SYSTEM-LEVEL MODELING AND OPTIMIZATION FOR BEYOND CMOS DEVICE APPLICATIONS**

Recent efforts in benchmarking new devices have evaluated the potential performance of the energy and delay for 32-bit adders and Arithmetic Logic Unit (ALU) for Beyond CMOS Benchmarking (BCB) [14, 29]. Current benchmarking models are good for 32-bit ALU, but it is architecture and circuit specific and does not consider area constraints and power budgets. A system level approach will extend this study to evaluate and optimize system performance for a single logic core. A more general system model is useful to uniformly compare various technologies with different architecture and complexity, allowing the benchmarking to scale to more complex logic cores where these devices will ultimately be used. With a flexible system model, throughput can be optimized by finding optimal supply voltage and number of gates, which represents a system architecture complexity and functionality. Using this optimization process, the impact of various power budgets on the optimized throughput performance in terms of energy-delay product (EDP) can be evaluated.

Using the generic system model approach, this chapter uniformly models and optimizes three promising TFET devices, GaN Heterojunction TFET, WTe<sub>2</sub> Two-dimensional heterojunction interlayer TFET (ThinTFET), and WTe<sub>2</sub> Transition Metal Dichalcogenide TFET (TMD TFET), and compares their system performance with ITRS projections for CMOS high performance (CMOSH<sub>P</sub>) and low voltage (CMOSL<sub>V</sub>) devices.

### 3.1 Generic System Model

A generic system model is used to quickly estimate the system level performance of various technology nodes. Existing system model IntSim is modified and used to model the power performance for each device technology. Intsim is an interconnect CAD tool that estimates the optimal interconnect pitch for each wiring level, co-optimizes signal, power, and clock interconnects based on stochastically derived wiring distributions. It also provides estimates for the system level power consumption for a given set of system parameters [28]. For a given operating frequency target, interconnect networks are optimized to obtain metal pitches on each metal level for a set of system parameters.

The advantage of using such a model is that it is a fast, generic model, captures system parameters and power, and has been validated with commercially available CPUs. While it is not as accurate as physical design models, it provides insightful trends and starting design parameters.

#### 3.1.1 Empirical CPI Model

For this work, an empirical cycles per instruction (CPI) model is used in conjunction with the generic system model to calculate the system throughput based on the number of transistors used in the system. The empirical CPI is based on the observations that a power law relation exists between CPI and the number of logic transistors. Previous works have shown a power-law relationship between number of logic gates and cycles per instructions. This has been verified based on 8 Intel processors using data extraction from existing CPU and CPU benchmarking specification SPECint. An updated CPI model is used in this study for the Intel microprocessor family [30].

$$CPI_{logic} = 2.466(N_{transistor})^{-0.420} \quad (1)$$

where  $N_{transistor}$  is the number of logic transistors in millions.

The functionality of the system can be improved by increasing the number of transistors, leading to a smaller CPI; however, a more complex system requires more interconnects, which imposes more constraints on the maximum frequency at which the system can operate. Therefore, when the empirical CPI model is combined with a clock frequency model and the area is fixed, there is a trade-off between system's operating frequency and CPI that gives an optimal throughput.

### 3.1.2 Optimization Methodology Flow

As mentioned before, for the system model in this study, IntSim is used to predict the optimal operating frequency for a given supply voltage ( $V_{dd}$ ) and number of gates ( $N_{gates}$ ). The maximum frequency that can be successfully achieved while staying within power budget is estimated and the maximum throughput is calculated using the empirical CPI model.

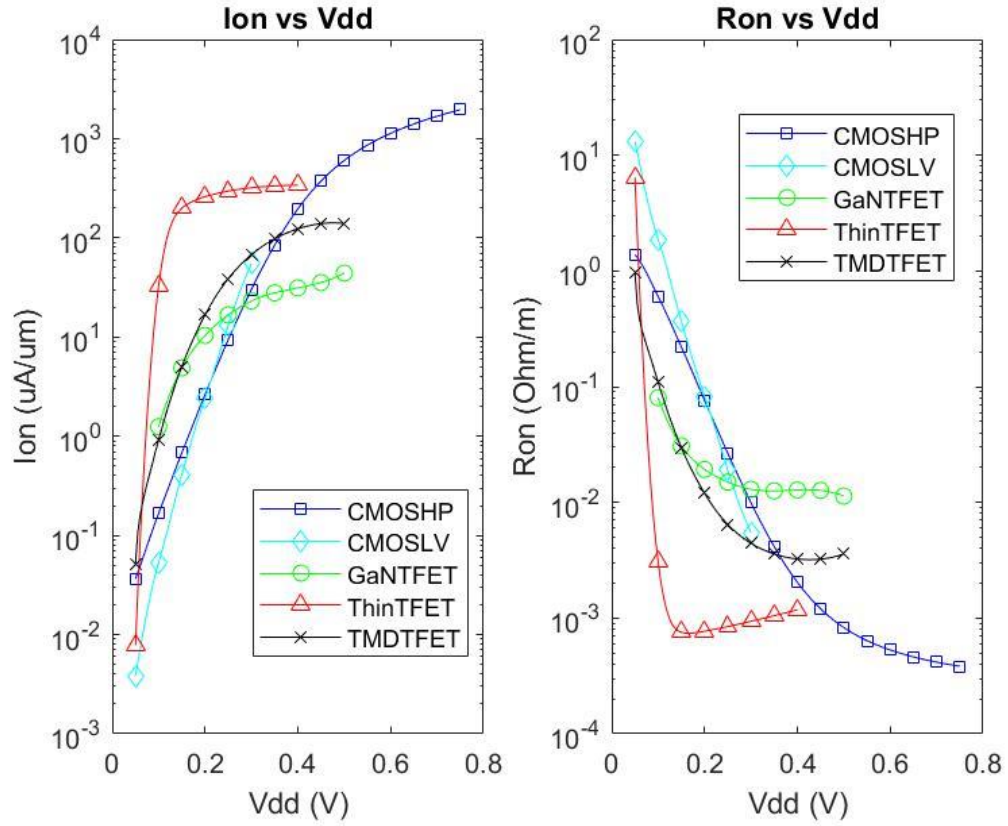
At the core of the parameter optimization is supply voltage and the number of logic gates. Supply voltage controls the on-current for the device and governs the system operating frequency, while the number of gates impacts our CPI. For a fixed supply voltage and number of gates, the highest operating frequency will give us the highest throughput for these two design points. The goal is to find a valid system-level model that operates at the highest frequency within a given power budget.

By sweeping  $V_{dd}$  and  $N_{gates}$ , the parameters that maximize the processor throughput for a given power budget and design space can be found. When looking at various power budgets, the different constraints impact the performance, and a comparison is made with different device technologies.

### 3.1.3 *Input Data and Device Technologies*

The system model requires input data for on-current, off-current and input capacitance for different device inputs. This work evaluates sidewall-gated GaN/InN heterojunction TFET (GaNTFET) [31, 32], WTe<sub>2</sub> Two-dimensional heterojunction interlayer TFET (ThinTFET) [33], and WTe<sub>2</sub> Transition Metal Dichalcogenide TFET (TMDTFET) [34, 35] and compares system performance with conventional CMOSHP and CMOSLV devices. All data are kept consistent with the physical dimensions presented in previous Beyond CMOS Benchmarking (BCB) works [14, 29] and ITRS Roadmap for the 2018 node [36].

The IV curves (Figure 12) and input capacitances for the evaluated devices are taken from published sources [31-35]. To optimize  $V_{dd}$  for a given power budget, the full IV curve for  $I_{on}$  and  $I_{off}$  along with voltage dependent input capacitance for multiple supply voltage data points are extracted from these works.

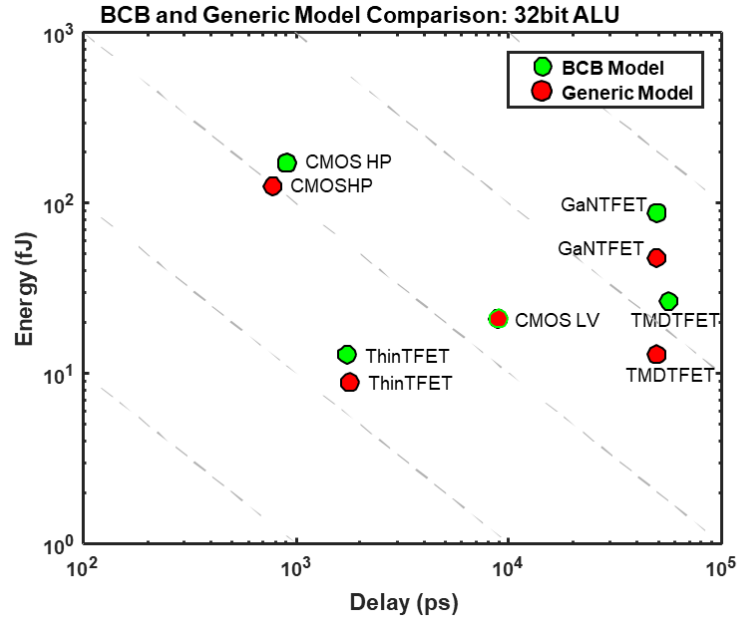


**Figure 12 – Input on-current and on-resistance data for different device technologies**

## 3.2 Simulation Results

### 3.2.1 System Model Comparison of ALU and Single Logic Core

A comparison between the BCB 3.0 simulator [37] and the generic system model is made for a 32-bit ALU. See Figure 13 for the comparison of energy and delay between the two models. In general, the two models show similar trends, with the generic system models more optimistic in energy for less complex systems.



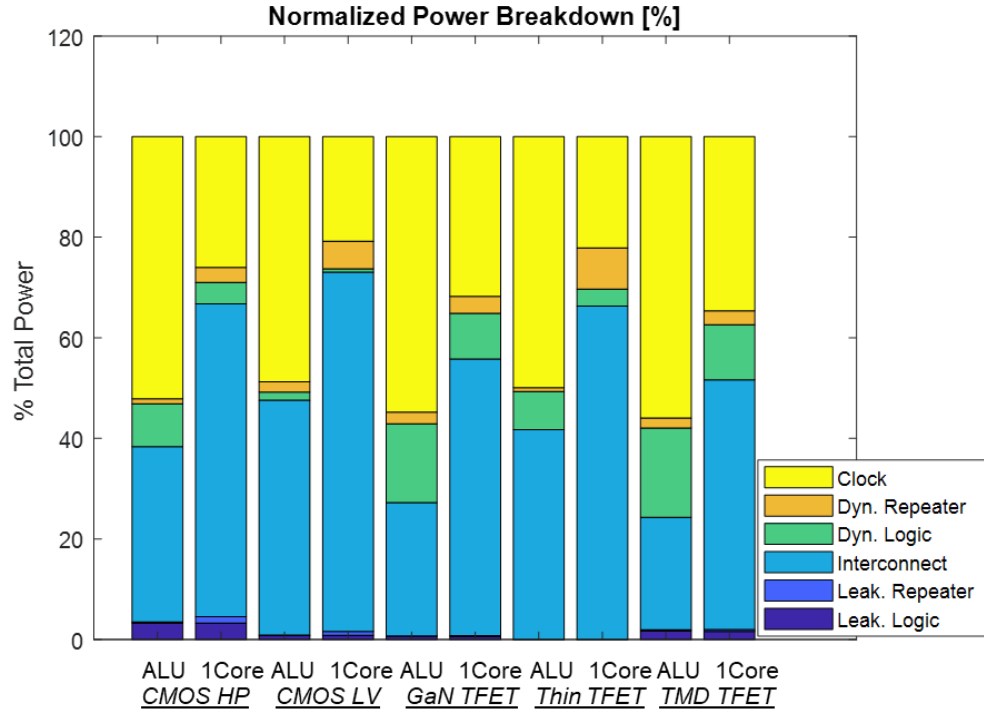
**Figure 13 – Trend comparison of Energy vs Delay between BCB model with Generic System model for a 32-bit ALU.**

### 3.2.2 Power Breakdown

The power breakdown for a 32-bit ALU and single logic core is evaluated and shown in Figure 14. For evaluating the system model extension of the ALU to a single logic core, the same device input is used. The key parameters used in the model are shown in Table 1. The normalized power breakdown shows that as the circuit becomes larger and more complicated, system overhead starts to take a larger proportion of the power. Interconnect power doubles in proportion compared to the rest of the power breakdown. This comparison using the system model highlights the more critical role of interconnects and repeaters in more complex systems. Having a more flexible model that captures the interconnect network and optimizes it for different design points is important when looking at more complex systems.

**Table 4 – Table of Input Parameters for System Model Comparison of ALU and Single Logic Core**

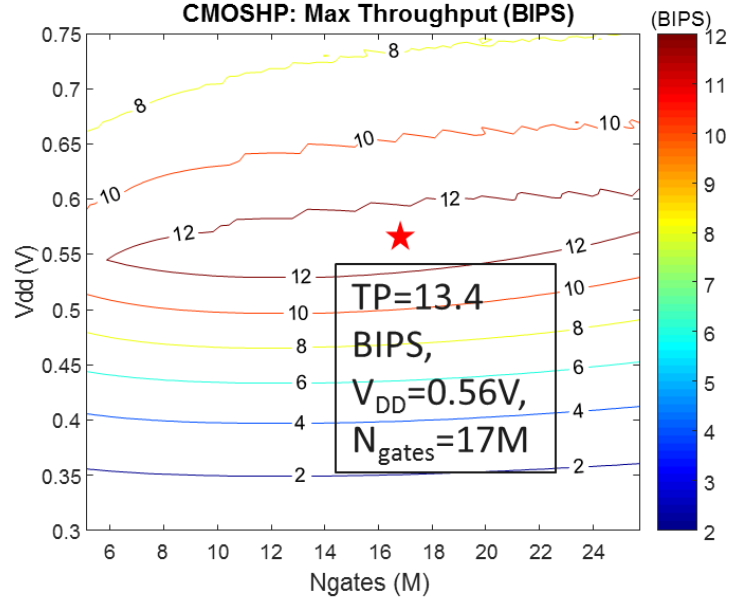
<b>Key Parameters</b>	<b>Values</b>
ALU $N_{\text{gates}}$	1500
ALU Area [ $\text{mm}^2$ ]	$3.6 \times 10^{-4}$
Single Logic Core $N_{\text{gates}}$ (Million)	16.3
Single Logic Core Area [ $\text{mm}^2$ ]	3.9
Logic Depth	10
Power Budget Density [ $\text{W}/\text{cm}^2$ ]	90
Activity Factor	0.1



**Figure 14 – Power breakdown comparison for 32-bit ALU and single core processor (1Core) for different device technologies.**

### 3.2.3 Throughput Optimization

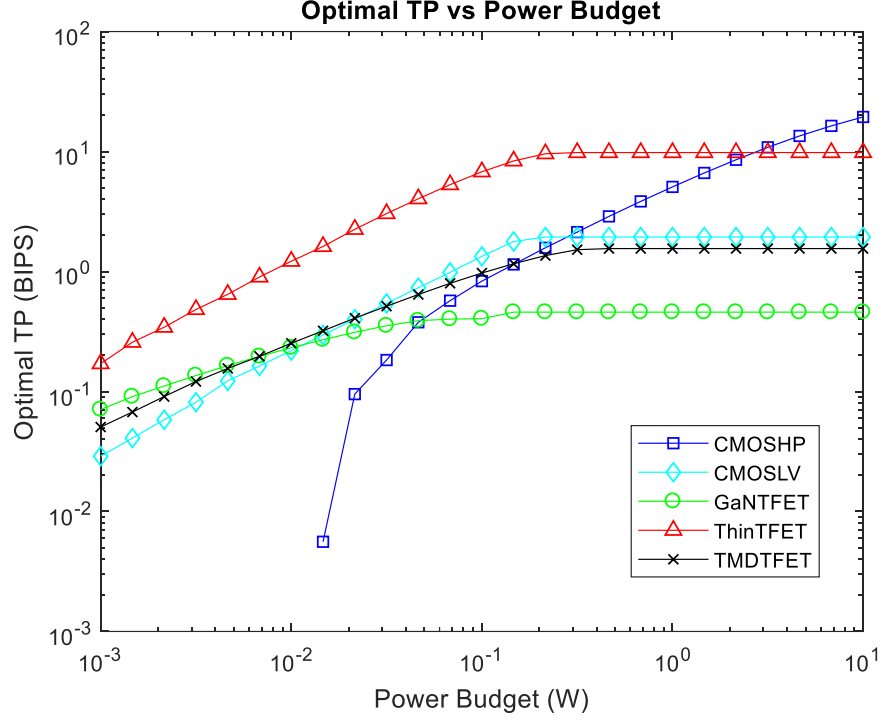
By using the empirical CPI model, there is a tradeoff between number of gates and higher operating frequency due to large gate widths for a fixed area. This leads to an optimal number of gates. A fixed chip area of  $5\text{mm}^2$  is used for the single logic core optimization. Throughput is limited at higher supply voltages due to power budget constraints, and an optimal  $V_{dd}$  can also be found for a given power budget. The optimization algorithm finds the highest throughput for a given  $V_{dd}$  and  $N_{gates}$  pair based on the empirical CPI model. This is done by finding the highest operating frequency that meets the power budget constraint for a given  $N_{gates}$  and  $V_{dd}$ . See Figure 15 for a typical optimization result for CMOSHP.



**Figure 15 – CMOS HP optimal throughput contour plot. Area is fixed at  $5\text{mm}^2$ . Power budget is set to  $4.6\text{ W}$ , with a power density of  $93\text{W}/\text{cm}^2$**

### 3.2.4 Throughput vs Power Budget

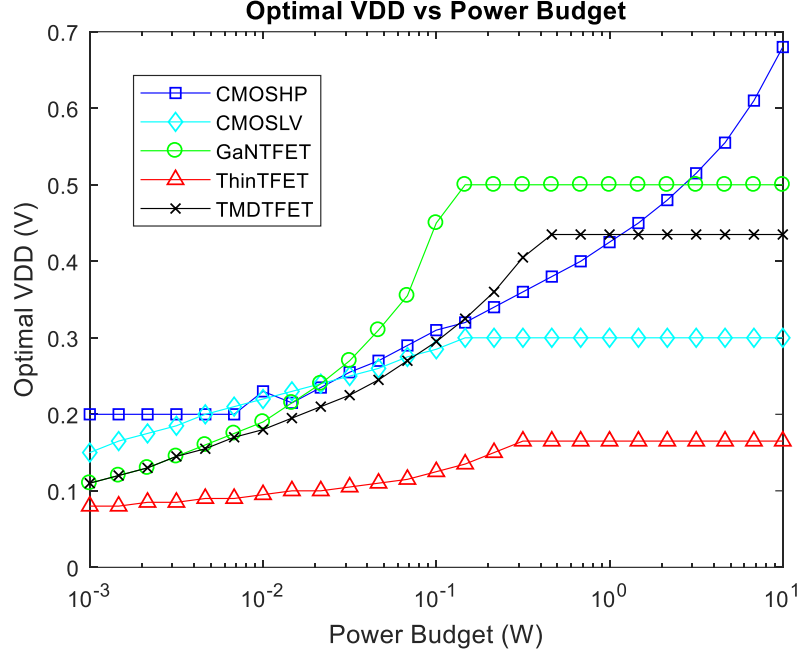
The results of optimizing throughput for a range of power budgets are shown in Figure 16. The power budget limits the supply voltage and frequency the system can operate. Low-power TFET devices perform better in terms of throughput when compared to CMOS LV for low power applications ( $<0.1\text{W}$ ,  $2\text{W}/\text{cm}^2$ ). For high performance applications, CMOSHP still performs the best in terms of throughput at high power budgets ( $>2.5\text{W}$ ,  $50\text{W}/\text{cm}^2$ ). The optimal  $V_{dd}$  and  $N_{gates}$  at each point will be shown in the next subsection.



**Figure 16 – Optimal throughput result versus power budget for different device technologies**

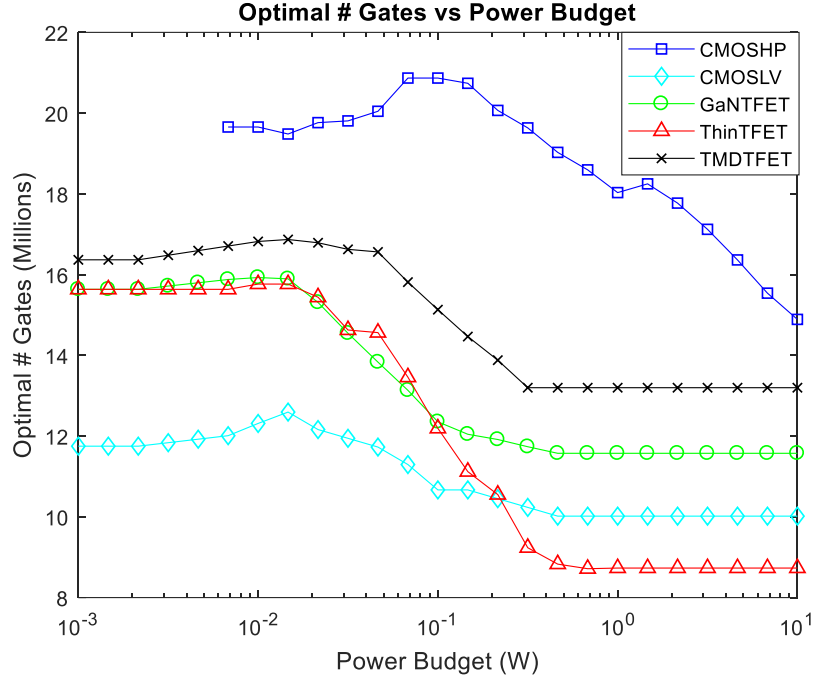
### 3.2.5 System Optimization Trends for $V_{dd}$ and $N_{gates}$

When optimizing for throughput for various power budgets, a trend for  $V_{dd}$  and  $N_{gates}$  emerges. Figure 17 shows the  $V_{dd}$  trend as power budget increases. At low power budgets, the system power is constrained and requires lower supply voltages to satisfy the requirement. As power budget increases, the optimal supply voltage also increases to allow for higher on-currents and operating frequency. For the lower power TFET and CMOS devices,  $V_{dd}$  quickly saturates to the maximum value as throughput saturates. CMOSHP; however, continues to increase due to its larger  $V_{dd}$  range and higher on-currents. For all cases, the optimal supply voltage settles to a  $V_{dd}$  that corresponds to its minimum  $R_{on}$ .



**Figure 17 – Optimal  $V_{dd}$  trends for different device technologies and power budgets**

A trend for the optimal number of  $N_{gates}$  is shown in Figure 18. At low power budgets, the system model favors more gates for lower CPI, which allows throughput to increase by increasing the functionality of the system without increasing power significantly. As power budget increases,  $N_{gates}$  approaches the optimal value associated with the preferred  $V_{dd}$  for maximum throughput due to the tradeoff between higher  $N_{gates}$  and lower CPI versus lower  $N_{gates}$  and higher frequency.

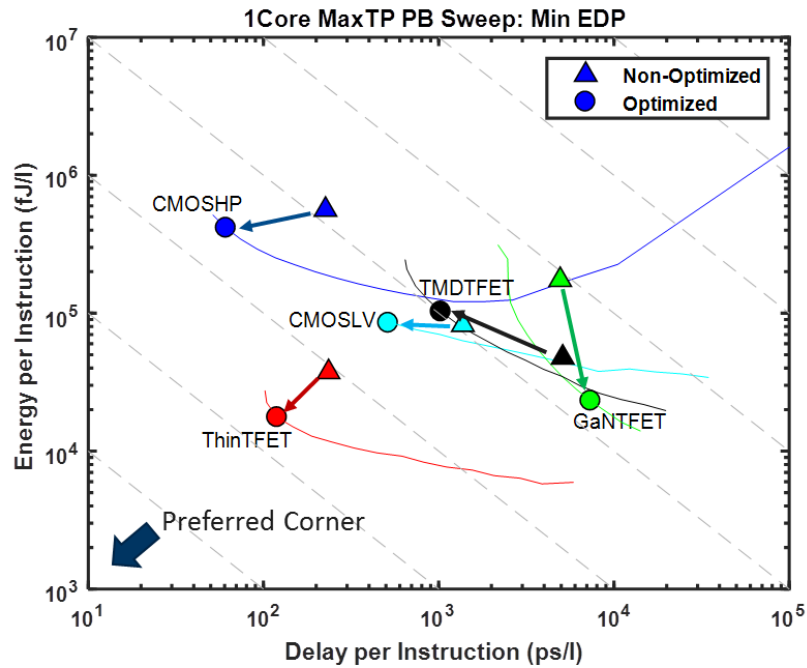


**Figure 18 – Optimal number of gates (Ngates) trend for different device technologies and power budgets.**

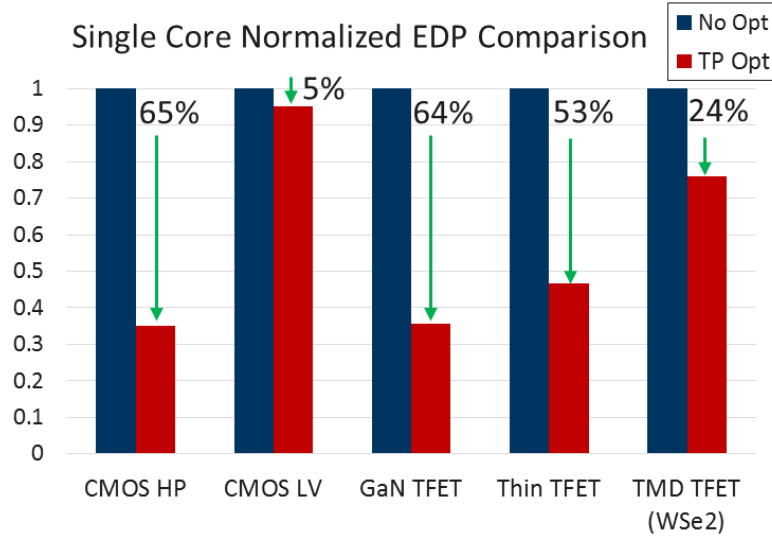
### 3.2.6 Optimization with minimum EDP: Single Core vs Optimized Single Core

Using the system-level modeling approach in conjunction with the empirical CPI, the number of gates is optimized to maximize throughput for a range of power budgets. As the number of gates increases, the device width decreases when the area and gate density is fixed. This decreases the on-current and maximum frequency at which the system can operate. However, if larger devices are used to increase the system operating frequency, the number of gates is reduced, increasing the number of cycles per instruction. This tradeoff leads to an optimal number of gates to maximize system throughput. The results of the optimization in terms of energy and delay are shown in Figure 19 and Figure 20. The minimum EDP is evaluated for a range of power budgets and the results are tabulated in

Table 5. Overall improvements are made in terms of EDP due to the optimization of number of gates and supply voltage. For TFET devices, GaN TFET benefitted the most from the optimization of the single core with an improvement of 64% in EDP. This is primarily driven by reducing the power budget and operating at a lower frequency and supply voltage.



**Figure 19 – Energy vs Delay per instruction results for different device technologies. The solid lines represent the optimized results for a range of power budget. The circle indicates the optimized results that correspond to the minimum energy delay product for that range of power budgets. The lower left-hand is the preferred corner that corresponds to a lower energy delay product.**



**Figure 20 – Normalized energy delay product comparison between the non-optimized case and the optimized case from a range of power budgets.**

**Table 5 – Optimized Minimum EDP Results for a Range of Power Budgets for Different Device Technologies**

Technology	Optimal PD [W/cm <sup>2</sup> ]	Optimal V <sub>dd</sub> [V]	Optimal N <sub>gates</sub> [M]
CMOS HP	92.83	0.56	16.9
CMOS LV	6.32	0.3	9.3
GaN TFET	0.06	0.15	19.1
Thin TFET	2.94	0.14	13.1
TMD TFET (WSe <sub>2</sub> )	2	0.3	18.4

### 3.3 Conclusion

In this study, a fast system-level model is applied to three beyond CMOS devices and the system level performance is evaluated. The system model is compared with the beyond CMOS benchmarking approach and shows good agreement for the 32-bit ALU. The system level approach is applied for a single logic core evaluation, and the interconnect bottleneck is shown through the doubling in power in proportion to overall system. Optimization is performed for a single logic core analysis, and EDP is shown to improve up to 64% in the case for the sidewall-gated GaN/InN heterojunction TFET. In optimizing throughput for a range of power budgets, a trend in  $V_{dd}$  shows an increase as the optimal point becomes less constrained by the power density limits. Higher  $N_{gates}$  is favored at lower power budgets before decreasing in favor of high frequency at higher power budgets.

## **CHAPTER 4. MODELING AND BENCHMARKING BACK END OF THE LINE TECHNOLOGIES ON CIRCUIT DESIGNS AT ADVANCED NODES**

As IC scaling continues to 7nm semiconductor technology node and beyond, interconnects present a grand challenge to circuit and system performance. When wire dimensions are scaled to narrow pitches at local metal-levels to accommodate dense logic and memory on chip, the percentage of interconnect cross-sectional area occupied by the highly-resistive barrier liner (Ta/TaN) for copper can be as much as 50% [19, 20]. This has motivated industry to explore advanced metallization options like Ru and Co that do not require a barrier and are less prone to size-effects that are observed in copper. However, these advanced interconnect options require further integration efforts to compete with copper wires at an 18nm width [23]. Here we present a quantitative analysis of the impact of barrier liner thickness on circuit-level Power-Performance-Area (PPA) metrics. We define the BEOL stack technology and design Advanced Encryption Standard (AES) and Low Density Parity Check (LDPC) circuit blocks by using the state-of-the-art physical design methodologies.

### **4.1 Design Flow and Methodology**

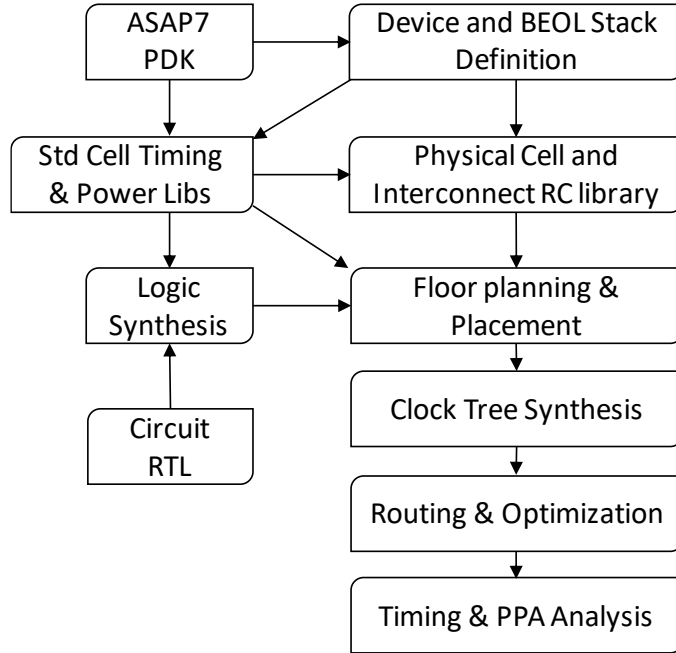
#### *4.1.1 Design Flow Overview*

The modeling framework follows the general design flow shown in Figure 21. For our circuit RTL definition, we use an AES and LDPC circuits available online from OpenCores. The AES circuit has random logic and moderate routing demand while the

LDPC circuit has high routing demand [19]. The AES and LDPC circuit RTL is synthesized using Synopsys Design Compiler and ASAP7 PDK standard cell libraries [38]. We then create and calibrate our own BEOL parameter files based on published resistance and via models and extract the RC parasitics using Quantus QRC extraction. Using the synthesized netlist and parasitic extraction from our custom BEOL files, we perform placement and routing using the commercial EDA tool Innovus from Cadence. At this stage, floorplanning, placement, pre-route optimization, routing, and post route optimization are completed within Innovus. After placement and routing (P&R), timing and power analysis reports are generated using tools built into the EDA tools and Tempus Timing Signoff Solution.

#### *4.1.2 ASAP7 PDK*

This work uses the ASAP7 PDK for the 7nm node, which is released and openly available from Arizona State University (ASU). This PDK has libraries for 4 different threshold voltage ( $V_t$ ), SLVT, LVT, RVT, and SRAM. In the case studies presented in this work, only the typical threshold libraries (RVT) are used [38-40].



**Figure 21 – General Design Flow and Modeling framework for circuit-based analysis.**

## **4.2 BEOL Modeling, Technology Development and Metal Barrier Scaling Case Study**

### *4.2.1 ICT Development and Wire and Via Resistance Models*

The BEOL stack dimensions for ASAP7 PDK and resistance parameters used in this work are given in Table 6. These values are used to create the interconnect files (ICT) used in this chapter for RC extraction. The metal thickness to width aspect ratio is 2 for each level in the stack. Resistance values are based on IMEC's published semi-empirical models that consider grain and sidewall scattering effects along with line edge roughness (LER) effects [41]. The self-aligned via resistance values are based on Coventor

SEMulator3D simulations similar to those done in [8] and published IMEC papers [9]. A description of different metal barrier/liner cases is given in the next section.

#### 4.2.2 *Metal Barrier Engineering*

Cu interconnects require a barrier/liner bi-layer material to prevent the diffusion of Cu into the surrounding dielectric and to ensure a void-free Cu fill. The original ASAP7 PDK assumes self-forming barriers are available and can result in very optimistic copper resistances. In this work we present a metal barrier/liner engineering case study based on more realistic assumptions for the barrier/liner material and experimentally calibrated resistance models where we examine the impact of scaling the thickness of TaN metal barrier and Ruthenium liner. TaN is typically deposited using PVD, and Ruthenium is deposited using CVD. Directional PVD of TaN results in thinner sidewall and thicker bottom coverage [42, 43]. In this work we assume 50% sidewall coverage for the PVD TaN as shown in Figure 22 a).

Metal barrier scaling presents many challenges and consumes a large portion of Cu cross-sectional area at the local levels. In section IV of this work, we compare the performances of 3 case studies for different metal barrier engineering scenarios. The first case represents the current industry best known method (BKM) that passes most reliability tests with 2nm TaN/2nm Ru bottom coverage. The second case is called the Thin scenario and represents one of the projected lower limits of barrier engineering with 1nm TaN/1nm Ru bottom coverage [22]. The third case (ImpVia) assumes current BKM barrier engineering for line resistances with advances in via resistance, either through near

barrierless via fill using ALD, prefill, or other proposed technologies. The resistance for each metal level for the three cases are given in Table 6.

**Table 6 – BEOL Key Layer Parameters and Resistances**

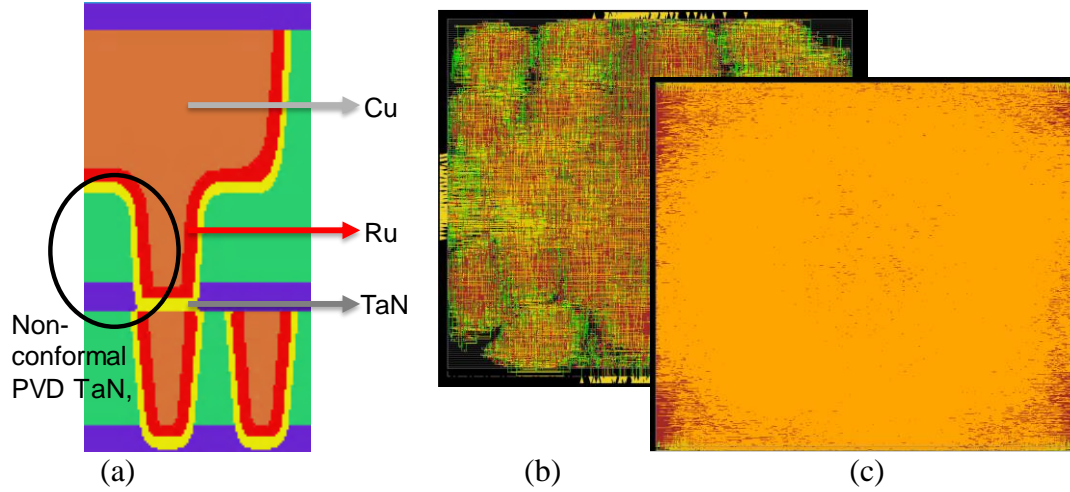
<b>Metal / Via</b>	<b>Width/Pitch (nm)</b>	<b>BKM MB/Liner</b>	<b>Thin MB/Liner</b>	<b>ImpVia</b>
M1-M3	18/36	244 $\Omega/\mu\text{m}$	164 $\Omega/\mu\text{m}$	244 $\Omega/\mu\text{m}$
V1-V3	18/36	116 $\Omega$	59 $\Omega$	39 $\Omega$
M4-M5	24/48	92 $\Omega/\mu\text{m}$	69 $\Omega/\mu\text{m}$	92 $\Omega/\mu\text{m}$
V4-V5	24/48	29 $\Omega$	17 $\Omega$	13 $\Omega$
M6-M7	32/64	37 $\Omega/\mu\text{m}$	30 $\Omega/\mu\text{m}$	37 $\Omega/\mu\text{m}$
V6-V7	32/64	9.6 $\Omega$	6.7 $\Omega$	5.0 $\Omega$
M8-M9	40/80	19 $\Omega/\mu\text{m}$	17 $\Omega/\mu\text{m}$	19 $\Omega/\mu\text{m}$
V8	40/80	3.2 $\Omega$	2.6 $\Omega$	2.3 $\Omega$

### 4.3 Experimental Setup and Results Comparison

#### 4.3.1 Experimental Setup

In our circuit benchmarking, we analyze the Power, Performance, and Area (PPA) results of two circuits: AES and LDPC. Comparing the results of two circuits provides a more diverse analysis on the impact of BEOL parameters on the two different circuit design groups.

For the circuit optimization and P&R, the initial footprint area targets 45% core utilization based on the synthesized netlist to allow headroom for P&R repeater insertion and optimization. For our results comparison, the target frequency and area are fixed for all cases. The final GDS layouts for the two different circuits are shown in Figure 22 (b) and (c).



**Figure 22 – (a) Local interconnect model cross-section and GDS layout of case BKM for (b) AES and (c) LDPC Circuit.**

#### 4.3.2 Metal Barrier BKM vs Thin Scaling Results

In the first experimental setup, we compare the updated BEOL technology file that is developed for the current industry BKM with the Thin case where the bottom MB liner thickness can be scaled down by 50%. The local interconnects line resistance improves by 33% and via resistance by 49%. This has a direct impact on the effective frequency of the AES circuit as seen in our benchmarking results shown in Table 7. We see an 9.49% improvement in effective clock frequency and 6.75% reduction in the number of repeaters. When we adjust total power to the effective frequency and calculate the Power Delay Product (PDP), an overall 4.18% improvement is observed. We see this is primarily driven by the overall decrease in net resistance of the circuit.

For a much more interconnect dominant circuit like the LDPC, the impact on the effective frequency is much more pronounced. We see in Figure 22 (c) the routing congestion for the LDPC circuit is much denser in the GDS layout compared to the AES

circuit. We observe a much higher 25.74% improvement in effective frequency and a better PDP of 8.29%. Much of the PDP efficiency gain is driven by the 18.2% reduction in the required number of repeaters for the Thin case.

#### *4.3.3 Metal Barrier Thin vs ImpVia Results*

Using the same optimization and P&R process described in the previous section, we analyze the PPA results comparing the impact of BKM and improved via case on the circuit performance. For the AES circuit, there is a 7.1% improvement in effective clock frequency and 3.37% improvement in PDP. While the total net resistance improves by 40%, the AES circuit is a more cell dominated design and is less sensitive to the improvement of the wire and via resistances.

For a more routing demanding LDPC design, we observe a higher (15.36%) improvement in effective clock frequency and a 6.49% improvement in PDP. The improved via case has better timing while requiring fewer repeaters and a lower total wire length.

**Table 7 – Iso-Area Performance Results Comparison between current industry BKM, Thin Scaled MB, and Improved Via BEOL RC Extraction**

		AES Circuit					LDPC Circuit				
		<i>BKM</i>	<i>Thin</i>	<i>Iso-Area</i> <i>Δ%</i>	<i>ImpVia</i>	<i>Iso-Area</i> <i>Δ%</i>	<i>BKM</i>	<i>Thin</i>	<i>Iso-Area</i> <i>Δ%</i>	<i>ImpVia</i>	<i>Iso-Area</i> <i>Δ%</i>
Target freq. (GHz)		3	3		3		1.8	1.8		1.8	
Cell count (#)		17,735	17,017	-4.05%	17,089	-3.64%	88,779	80,597	-9.22%	85,223	-4.01%
Inv / Buffer Count (#)		6,934	6,466	-6.75%	6,502	-6.23%	39,753	32,518	-18.20%	36,344	-8.58%
Worst slack (ns)		-0.059	-0.025	-57.63%	-0.033	-44.07%	-0.436	-0.233	-46.56%	-0.304	-30.28%
Effective freq. (GHz) *		<b>2.55</b>	<b>2.79</b>	<b>9.49%</b>	<b>2.73</b>	<b>7.10%</b>	<b>1.01</b>	<b>1.27</b>	<b>25.74%</b>	<b>1.16</b>	<b>15.36%</b>
Power (mW) @ eff. frequency	Total	5.70	5.98	4.91%	5.90	3.48%	47.93	55.27	15.32%	51.70	7.87%
	Internal	2.69	2.83	5.11%	2.78	3.38%	13.34	14.89	11.60%	13.89	4.06%
	Switching	3.01	3.15	4.74%	3.12	3.58%	34.58	40.37	16.76%	37.81	9.34%
	Leakage	0.002	0.002	-0.51%	0.002	0.74%	0.010	0.009	-13.48%	0.010	-8.14%
Power Delay Product (mW·ns)		<b>2.24</b>	<b>2.14</b>	<b>-4.18%</b>	<b>2.16</b>	<b>-3.37%</b>	<b>47.53</b>	<b>43.59</b>	<b>-8.29%</b>	<b>44.44</b>	<b>-6.49%</b>
Core Utilization (%)		78.74	77.17	-1.99%	77.75	-1.26%	88.84	80.83	-9.02%	84.50	-4.89%
Total WL (um)		64,810	63,032	-2.74%	64,185	-0.96%	863,346	818,842	-5.15%	831,985	-3.63%
Pin capacitance (pF)		20.4	20.4	-0.05%	20.5	0.78%	90.7	82.9	-8.61%	87.1	-4.05%
Wire capacitance (pF)		8.7	8.4	-4.34%	8.6	-1.90%	164.5	153.8	-6.48%	157.2	-4.44%
Tot. Net Resistance (Mohms)		25.7	14.5	-43.34%	15.3	-40.39%	248.8	143.3	-42.39%	164.7	-33.79%
Footprint (μm x μm)		46.2x 46.2	46.2x 46.2		46.2x 46.2		97.5x 97.5	97.5x 97.5		97.5x 97.5	

\* Effective frequency is calculated by adjusting the target clock period by the WNS.

#### 4.4 Conclusion

This work presents a modeling framework to study the impact of various interconnect parameters on the circuit performance. Using realistic assumptions for the BEOL barrier/liner stack along with experimentally calibrated resistance models, we develop our own interconnect technology file. Using this framework, fully routed AES and

LDPC circuit designs are implemented studying the impact of barrier/liner thickness scaling.

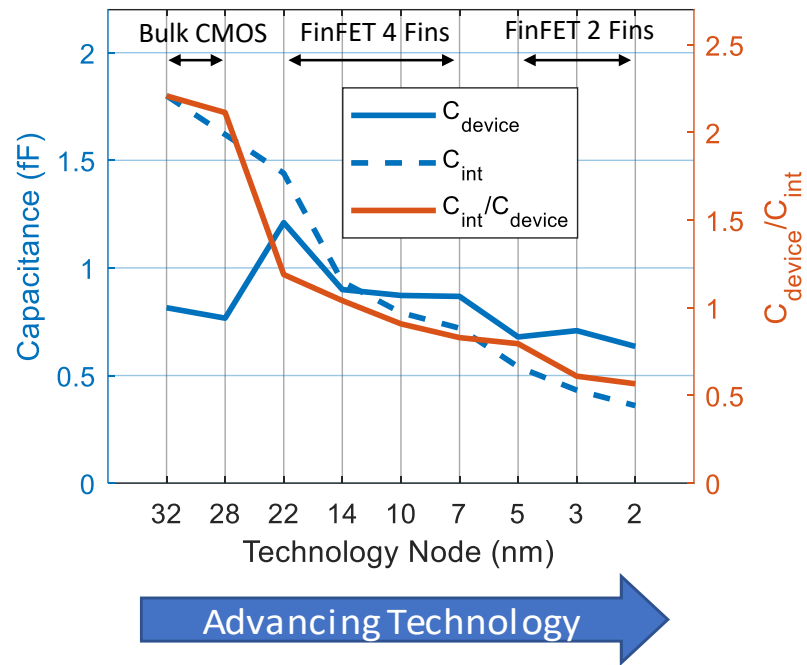
In our benchmarking results, we see that the impact of the improving the metal/barrier liner scaling depends on the circuit design. The improvement in frequency performance can range from 9.49% for a moderately routing demanding AES circuit to 25.74% for a high routing demand LDPC circuit. Advances in via technology alone can also improve performance by as much as 15% for high routing demanding circuits. As advanced technology nodes continue to scale down, the performance penalty at those nodes will only be exacerbated if thin barrier/liner layers do not become available.

## **CHAPTER 5. FROM INTERCONNECT MATERIALS AND PROCESSES TO CHIP LEVEL PERFORMANCE: MODELING AND DESIGN FOR CONVENTIONAL AND EXPLORATORY CONCEPTS**

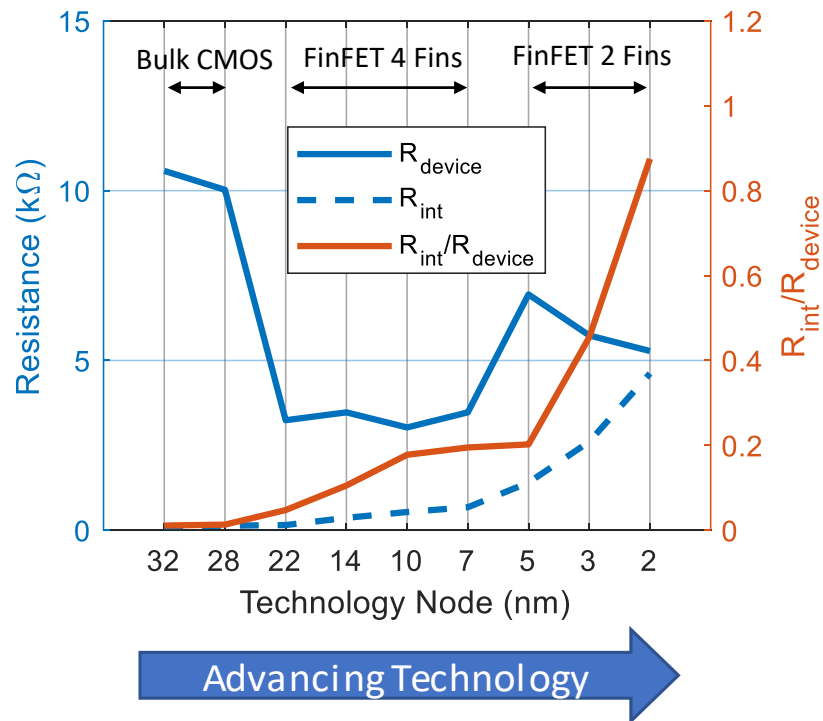
Relentless scaling of transistors and wires to enhance transistor density and system-level performance has resulted in severe implications on advanced metallization processes and performance. Back End of Line (BEOL) parasitics are increasingly dominated by interconnect resistance due to severe size effects in copper wires and challenges to metal barrier scaling [44, 45]. New materials have been explored to replace copper wires and vias, like cobalt and ruthenium, that exhibit higher bulk resistivity ( $\rho_{\text{bulk}}$ ) values compared to copper but can lead to lower effective resistivities due to thin barrier-liner requirements and lower size effects. Literature has shown that the crossover point for ruthenium resistance is beyond the 7nm node, when wires/vias are scaled to around 14nm critical-dimension (CD) [46]. In this chapter we (i) review the scaling trends for R and C values of interconnects and transistors, (ii) perform a detailed sensitivity study focused on the impact of BEOL processes on system-level performance, (iii) evaluate copper technology at the 7nm node at a system level with various enhancements to barrier/liner, vias and Aspect-Ratio (AR) optimizations to push copper interconnect performance/power, and (iv) compare the flavors of 7nm copper interconnect based systems with designs based on ruthenium wires and vias and showcase the crossover point where it is beneficial to replace copper wires/vias.

## 5.1 Device and Interconnect Scaling Trends

Device and interconnect technologies defined and projected for a wide spectrum of technology nodes, from 32nm to 3nm, are surveyed [47-51], and the device RC is compared against the interconnect RC by assuming a wire length of 100 Metal-Pitch (MP) (Figure 23 and Figure 24). With per-unit-length interconnect capacitance remaining relatively fixed across technology nodes, dimensional scaling leads to shorter local and intermediate interconnects and less capacitance for the same design specifications (this may however change if new systems are designed with larger memories and floorplans). At the same time, device capacitance has increased with the transition from bulk/planar devices to FinFET devices, as shown in Figure 23. We observe from the ratio of device to interconnect capacitance that interconnect capacitance becomes less of a factor at advanced nodes (Figure 23); another factor leading to this conclusion is the interconnect resistance rapidly increasing at scaled dimensions. We observe an overall decrease in device resistance with advancing technology, with a noticeably larger drop in resistance when transitioning from bulk to FinFET technologies which was done to achieve better electrostatic control and higher current drive (Figure 24). When we compare the interconnect resistance with device resistance, we see interconnect resistance becoming a larger share of the overall path delay. With the capacitance and resistance changes at advanced nodes, there are proposals to improve interconnect resistance by either widening [20] or using higher AR wires at the expense of increasing parasitic capacitance to help alleviate the resistance bottleneck at the local metal levels.



**Figure 23 – Interconnect and Device Capacitance Trends for advancing technology nodes**



**Figure 24 – Interconnect and device resistance trends for advancing technology nodes**

The major limitations of copper technology have come down to the barrier/liner requirements, and the implication of this requirement on wire and via resistances is substantial [52]. Cobalt and ruthenium have shown to provide less severe size effects and become competitive below a CD of 14nm (assuming ultra-scaled liner widths are possible for copper wires), largely due to having lower mean-free-path ( $\lambda$ ), lower  $\rho_{\text{bulk}} * \lambda$  which serves as a proxy for size effects, and higher melting-point/activation energies enabling liner-free/thin liner wires/vias [53, 54].

## 5.2 Modeling and Benchmarking Methodology

We present the place and route (P&R) results of different interconnect scenarios on power, performance, and area (PPA). We perform the analysis for two representative circuits which have different importance for interconnect and via in design PPA metrics [52]; the two designs are: Advanced Encryption Standard (AES), which has random logic and moderate routing demand, and Low-Density Parity Check (LDPC), with its high routing demand [19]. The BEOL resistance models are based on published models for Cu interconnects that have been calibrated to experimental data [41, 55], and the RC extraction for the BEOL stack is performed using Cadence® Quantus™. The technology is based on the predictive ASAP7 7nm Process Design Kit (PDK) [38] as specified in Table 8.

**Table 8 – Key ASAP7 Technology Design Parameters**

Key Parameters	Values
$V_{dd}$ (V)	0.7
Gate length, $L_g$ (nm)	21
Contacted Gate Pitch (nm)	54
Cell Height (tracks)	7.5
Fin Width/Pitch (nm)	6.5/27
Gate Width/Pitch (nm)	21/54
M1-M3 (Local Interconnect) CD/Pitch (nm)	18/36
M4-M5 CD/Pitch (nm)	24/48
M6 CD/Pitch (nm)	32/64

The designs are all evaluated under an ISO-area constraint. We then establish a reference baseline scenario based on current industry's Best-Known Method (BKM) obtained from [56]. We assume a copper BEOL stack with a metal barrier (MB) that has a bottom thickness of 4nm. All other BEOL scenarios defined in Table 9 are benchmarked against the base BKM case.

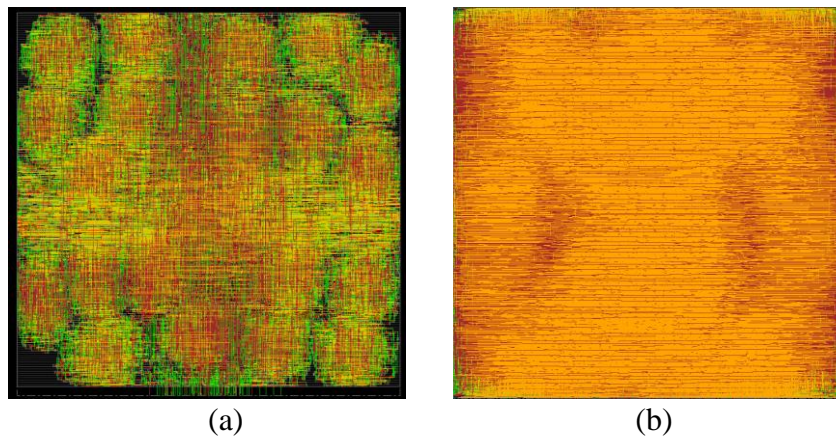
**Table 9 – Different Scenario Assumptions in this Work for MB and Adhesion (TiO<sub>2</sub>) Thickness for Bottom and Sidewalls**

<b>Scenario 1: BEOL MB Scaling</b>		
<u>Case</u>	<u>Wire MB t<sub>bottom</sub>/t<sub>side</sub> (nm)</u>	<u>Via MB t<sub>bottom</sub>/t<sub>side</sub> (nm)</u>
BKM	4 nm / 3 nm	4 nm / 3 nm
MB <sub>thin</sub>	2 nm / 1.5 nm	2 nm / 1.5 nm
Via <sup>++</sup>	4 nm / 3 nm	1 nm / 1 nm
<b>Scenario 2: Local Interconnect MB Scaling</b>		
M <sub>local</sub> -MB <sub>thin</sub>	2 nm / 1.5 nm	2 nm / 1.5 nm
M <sub>local</sub> -MB <sub>thin</sub> (wire)	2 nm / 1.5 nm	4 nm / 3 nm
M <sub>local</sub> -MB <sub>thin</sub> (via)	4 nm / 3 nm	2 nm / 1.5 nm
<b>Scenario 3: Ru and High AR Local Interconnects</b>		
M <sub>local</sub> -Ru	0.3nm (TiO <sub>2</sub> )	0.3nm (TiO <sub>2</sub> )
M <sub>local</sub> -Ru-AR3	0.3nm (TiO <sub>2</sub> )	0.3nm (TiO <sub>2</sub> )
M <sub>local</sub> -BKM-Cu-AR3	4 nm / 3 nm	4 nm / 3 nm

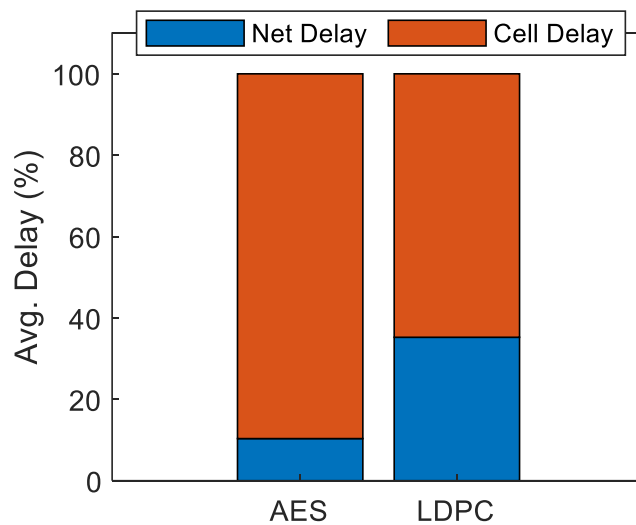
### 5.3 Interconnect Scaling and Sensitivity Scenarios and performance Results

The final design implementations are presented in Figure 25. Prior to delving into the detailed sensitivity analysis, we analyzed the delay breakdown for the top critical paths with the BKM case, and we see that the net delay contributes 10% and 35% of the total delay for the AES and LDPC circuits, respectively (Figure 26). Hence, our expectations for any interconnect process optimizations are limited within these bounds for these designs. Since the AES design is less wire-delay dominated (Figure 26), we expect the impact of improving interconnect technologies will be more apparent in the LDPC circuit.

We attempt to isolate the PPA improvement obtained from just the BEOL process improvements and the additional improvement gained through design tool optimization algorithms by performing one set of analyses by plugging in the new wires/vias in an existing design and extracting PPA (Table 10 and Table 11), and the second set of analyses complemented with EDA optimizations (Table 12 and Table 13).



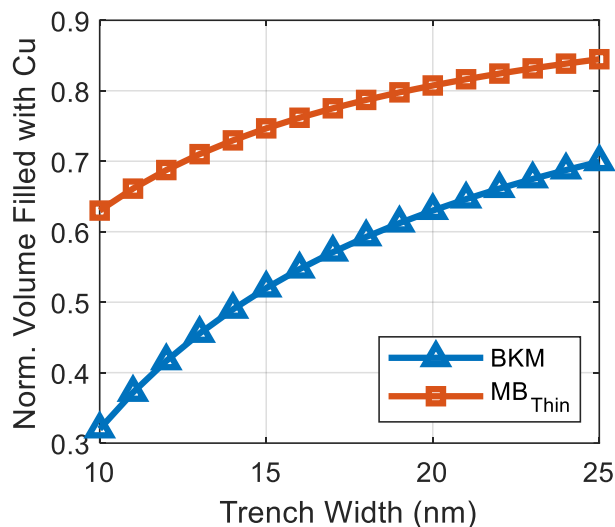
**Figure 25 - BKM GDS layout for (a) AES and (b) LDPC Circuit**



**Figure 26 – Percent net delay of top 50 critical paths for AES and LDPC circuits based on BKM P&R. Total net delay accounts for 10% and 35% of the total delay for the top 50 critical paths of AES and LDPC circuits, respectively.**

### 5.3.1 Scenario 1: BEOL Stack Metal Barrier Scaling

In addition to rapidly increasing interconnect resistance, the highly resistive MB has not scaled at the same rate due to process and reliability concerns. At 18nm trench width, the MB consumes as much as 40% of the wire volume (Figure 27). In the first experiment, we benchmark the impact of thinning the MB material ( $MB_{thin}$ ) from 4nm to 2nm, which improves both line and via resistances; and in the second, we only improve via resistance ( $Via^{++}$ ) as in Table 9.



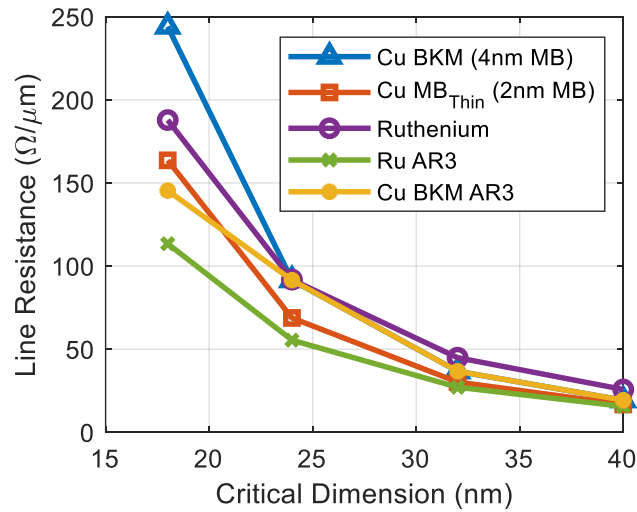
**Figure 27 – Proportion of wire filled with Cu**

Without EDA optimizations, thinning barrier materials ( $MB_{thin}$ ) and improving vias ( $Via^{++}$ ) show similar improvements for the AES circuit (Table 10). In the interconnect dominant LDPC design,  $MB_{thin}$  shows a greater (i.e. 15.56%) improvement in performance compared to 9.19% for  $Via^{++}$  highlighting the importance of both wire- and via resistance to system performance (Table 11).

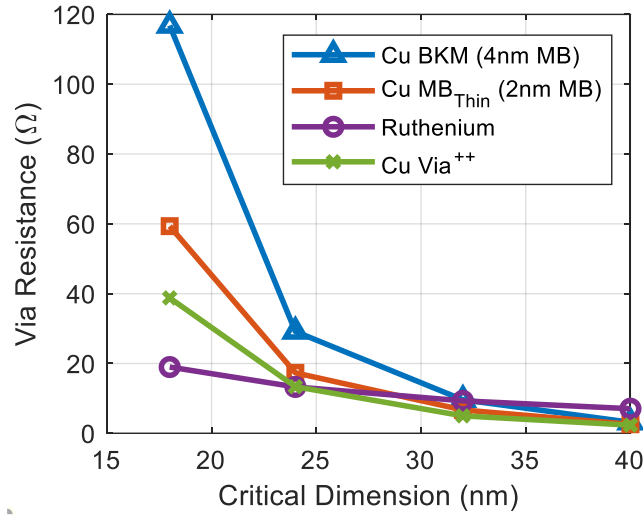
With re-optimization, we see additional performance gains for both  $MB_{thin}$  and  $Via^{++}$  for both circuits (Table 12 and Table 13). The tool extends the performance gains while using less buffers and wiring, which leads to a better power delay product (PDP).

### 5.3.2 Scenario 2: Local Interconnect/Via Metal Barrier Scaling

The wire resistance drastically changes from node-to-node at the local metal levels (Figure 28 and Figure 29), hence in the following sections we focus on local metals only. In addition, we perform a sensitivity analysis on the impact of improving only wire resistance ( $M_{local}-MB_{thin}(wire)$ ) and only improving via resistance ( $M_{local}-MB_{thin}(via)$ ).

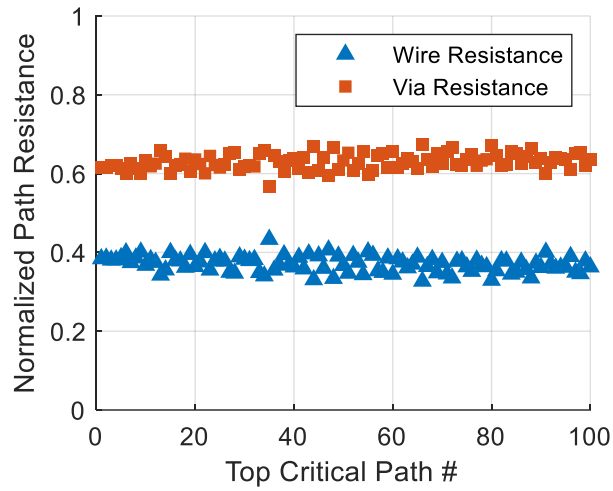


**Figure 28 – Line resistance for different CD**

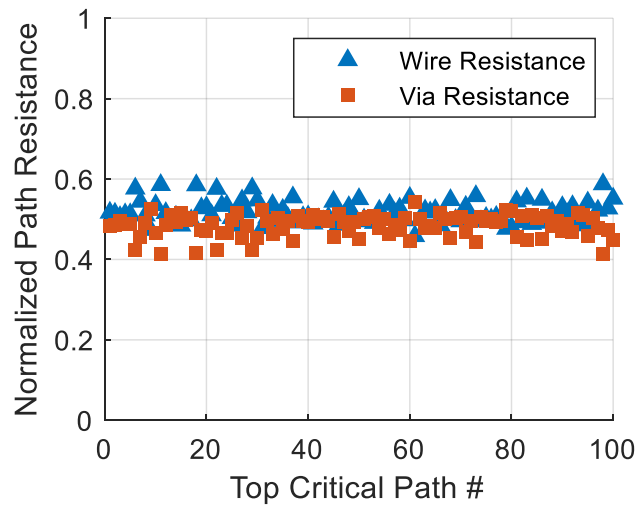


**Figure 29 – Via resistance for different CD**

Without EDA optimizations, thinning only the local interconnect MB in the design results in 0.6×-0.8× the improvement achieved by thinning the entire BEOL stack, highlighting that the local metals are largely limiting the wire-delay dominated critical paths (Table 10 and Table 11). Additionally, via resistance is more important in improving the critical path delay. When we look at the wire and via resistance for the top critical paths in Figure 30 and Figure 31, we see that via resistance is a larger part of the total net resistance for the AES circuit compared to the LDPC circuit. With EDA optimizations, we see the tool compensating for the better wire resistance for the LDPC circuit.  $M_{\text{local-MB}_{\text{thin}}(\text{wire})}$  resulted in a 16.1% improvement compared to 11.6% for the  $M_{\text{local-MB}_{\text{thin}}(\text{via})}$  case (Table 12 and Table 13).



**Figure 30 – Normalized breakdown of net resistance from wire vs via for the top 100 critical paths. Results are based on AES P&R for BKM. Average  $R_{\text{wire}}$  is 37% for top 100 paths.**



**Figure 31 – Normalized breakdown of net resistance due to wire vs via for the top 100 critical paths based on P&R results for BKM of LDPC circuit. Average  $R_{\text{wire}}$  is 52% for top 100 paths.**

### 5.3.3 Scenario 3: Alternative Metals and High Aspect Ratio

We explore new materials and schemes for the local interconnects. The first case looks at the impact of replacing local interconnects with Ruthenium ( $M_{\text{local-Ru}}$ ). Ruthenium as an alternative metal does not require a MB and is less sensitive to size effects compared to Cu. Based on published results [3,19] the line and via resistances are shown in Figure 28 and Figure 29. At 18nm CD, Ru line resistance already performs better than Cu with 4nm MB. Because Ru does not require a resistive MB, the via resistance is superior to copper. We also explore high-AR wires, which have been proposed to alleviate the resistance bottleneck at the expense of parasitic capacitance. We consider high AR interconnects (i.e., AR=3) for both Ru ( $M_{\text{local-Ru-AR3}}$ ) and Cu ( $M_{\text{local-BKM-Cu-AR3}}$ ). From our parasitic extraction for M1-M3, we see AR3 can improve resistance by 40% while increasing net capacitance by 28%. For cases where resistance is dominant, this tradeoff in resistance and capacitance can help improve overall performance.

From our results (Table 12 and Table 13), Ru local metals have similar and sometimes better performance gains than the  $MB_{\text{thin}}$  case motivating the move to ruthenium sooner. For the high AR cases, we see little change in performance but a larger hit to power due to the increased capacitance.

## 5.4 Conclusion

In this chapter, we have performed a detailed sensitivity analysis of BEOL processes on advanced node physical design implementations. In particular, we have looked into implications of barrier-liner, via bottom- and side-wall liner thickness advancements for copper wires and explored ruthenium-based wires with geometry optimizations for

improved design PPA. With rapidly increasing via resistances and dense local connections, via resistance plays an important role in overall system performance. At the 7nm technology node, Ru interconnects already show good improvement to performance. Ru line resistance is already comparable to Cu and the barrierless vias have much lower resistance compared to Cu, contributing more to the gain in performance. For the high AR Ru and Cu, we see very little performance gains for all cases at the 7nm technology despite better resistance. Power dissipation also increases due to higher interconnect capacitance. However, we expect larger performance gains with high-AR wires at more advanced nodes when resistance is further exacerbated due to dimensional scaling.

**Table 10 – AES Results for Fixed P&R Design**

<b>Scenario 1: BEOL MB Scaling (AES)</b>		
<u>Case</u>	<u>Eff. Freq. [GHz]</u>	<u><math>\Delta\%</math> Eff. Freq.</u>
BKM	2.55	
MB <sub>thin</sub>	2.70	5.95%
Via <sup>++</sup>	2.69	5.66%
<b>Scenario 2: Local Interconnect MB Scaling (AES)</b>		
M <sub>local</sub> -MB <sub>thin</sub>	2.67	4.81%
M <sub>local</sub> -MB <sub>thin</sub> (wire)	2.58	1.03%
M <sub>local</sub> -MB <sub>thin</sub> (via)	2.66	4.26%
<b>Scenario 3: Ru and High AR Local Interconnects (AES)</b>		
M <sub>local</sub> -Ru	2.72	6.52%
M <sub>local</sub> -Ru-AR3	2.67	4.81%
M <sub>local</sub> -BKM-Cu-AR3	2.54	-0.25%

**Table 11 – LDPC Results for Fixed P&R Design**

<b>Scenario 1: BEOL MB Scaling (LDPC)</b>		
<u>Case</u>	<u>Eff. Freq. [GHz]</u>	<u><math>\Delta\%</math> Eff. Freq.</u>
BKM	0.99	
MB <sub>thin</sub>	1.14	15.56%
Via <sup>++</sup>	1.08	9.19%
<b>Scenario 2: Local Interconnect MB Scaling (LDPC)</b>		
M <sub>local</sub> -MB <sub>thin</sub>	1.081	9.19%
M <sub>local</sub> -MB <sub>thin</sub> (wire)	1.029	3.91%
M <sub>local</sub> -MB <sub>thin</sub> (via)	1.034	4.45%
<b>Scenario 3: Ru and High AR Local Interconnects (LDPC)</b>		
M <sub>local</sub> -Ru	1.11	12.47%
M <sub>local</sub> -Ru-AR3	1.09	10.50%
M <sub>local</sub> -BKM-Cu-AR3	0.97	-1.85%

**Table 12 – Final Optimization Results for AES Circuit**

<b>Scenario 1: BEOL MB Scaling (AES)</b>											
Case	Eff. Freq. [GHz]	$\frac{\Delta\%}{\text{Eff. Freq.}}$	$P_{\text{tot}}$ [mW]	$P_{\text{in}}$ [mW]	$P_{\text{sw}}$ [mW]	$P_{\text{lk}}$ [mW]	PDP	$\frac{\Delta\%}{\text{PDP}}$	Cell Count (#)	Buf / Inv (#)	Total WL [ $\mu\text{m}$ ]
BKM	2.55	0	5.59	2.64	2.95	0.002	2.19		3,719	6,934	64,810
MB <sub>thin</sub>	2.79	9.49%	5.96	2.82	3.14	0.002	2.14	-2.72%	3,579	6,466	63,032
Via <sup>++</sup>	2.73	7.10%	5.96	2.81	3.15	0.002	2.18	-0.55%	3,620	6,502	64,185
<b>Scenario 2: Local Interconnect MB Scaling (AES)</b>											
M <sub>local</sub> -MB <sub>thin</sub>	2.69	5.66%	5.91	2.78	3.12	0.002	2.19	-0.01%	3,777	6,781	64,386
M <sub>local</sub> -MB <sub>thin</sub> (wire)	2.62	2.62%	5.68	2.66	3.02	0.002	2.17	-1.11%	3,859	6,756	65,900
M <sub>local</sub> -MB <sub>thin</sub> (via)	2.64	3.43%	5.75	2.69	3.06	0.002	2.18	-0.57%	3,629	6,787	65,450
<b>Scenario 3: Ru and High AR Local Interconnects (AES)</b>											
M <sub>local</sub> -Ru	2.77	8.58%	6.02	2.88	3.13	0.002	2.17	-0.92%	3,487	6,355	62,329
M <sub>local</sub> -Ru-AR3	2.78	8.88%	6.14	2.86	3.28	0.002	2.21	0.83%	3,513	6,070	63,776
M <sub>local</sub> -BKM-Cu-AR3	2.55	0.00%	5.63	2.60	3.03	0.002	2.21	0.64%	3,706	6,667	64,876

**Table 13 – Final Optimization Results for LDPC Circuit**

<b>Scenario 1: BEOL MB Scaling (LDPC)</b>											
Case	Eff. Freq. [GHz]	$\frac{\Delta\%}{\text{Eff. Freq.}}$	$P_{\text{tot}}$ [mW]	$P_{\text{in}}$ [mW]	$P_{\text{sw}}$ [mW]	$P_{\text{lk}}$ [mW]	PDP	$\frac{\Delta\%}{\text{PDP}}$	Cell Count (#)	Buf/Inv (#)	Total WL [ $\mu\text{m}$ ]
BKM	0.99	0	38.17	10.07	28.09	0.01	38.54		81,695	31,355	796,050
MB <sub>thin</sub>	1.20	21.11%	43.65	11.98	31.66	0.01	36.39	-5.57%	75,758	27,733	765,692
Via <sup>++</sup>	1.16	17.59%	43.13	11.35	31.77	0.01	37.04	-3.89%	80,419	30,435	792,815
<b>Scenario 2: Local Interconnect MB Scaling (LDPC)</b>											
M <sub>local</sub> -MB <sub>thin</sub>	1.20	20.82%	44.40	11.75	32.64	0.01	37.11	-3.71%	75,983	27,858	755,628
M <sub>local</sub> -MB <sub>thin</sub> (wire)	1.15	16.10%	44.25	11.77	32.48	0.01	38.48	-0.13%	78,863	30,027	776,213
M <sub>local</sub> -MB <sub>thin</sub> (via)	1.11	11.61%	41.84	11.06	30.77	0.01	37.85	-1.78%	81,111	31,251	795,236
<b>Scenario 3: Ru and High AR Local Interconnects (LDPC)</b>											
M <sub>local</sub> -Ru	1.19	20.10%	43.58	11.48	32.10	0.01	36.64	-4.92%	77,033	27,815	768,353
M <sub>local</sub> -Ru-AR3	1.19	20.10%	45.99	11.84	34.14	0.01	38.66	0.31%	74,823	27,312	746,873
M <sub>local</sub> -BKM-Cu-AR3	1.02	3.06%	43.12	10.93	32.18	0.01	42.25	9.63%	82,698	33,014	801,275

## CHAPTER 6. CONCLUSION, FUTURE SCALING CHALLENGES AND OUTLOOK

### 6.1 Conclusion

In today's semiconductor landscape, the ever-increasing costs and challenges for advanced IC fabrication require innovative solutions to address scaling limitations. It becomes crucial to manage the cost and risks to production, making it important to understand where the next innovation will take us in terms of performance and scaling gains. This body of work assesses some of these proposed technological innovations and their performance implications at the circuit and system level.

In chapter 2, a stacked CMOS NAND2 and inverter based on lateral nanowire GAAFETs is proposed to reduce the footprint area of the device, thereby enabling further planar density scaling and reducing the average interconnect length at the system level. The proposed structures are modeled and the key parasitics are extracted using field solver Raphael. Using validated open-source simulator IntSim, the system-level power and performance gains are evaluated for the new device structures. The stacked structures are projected to reduce power by 12.9% and EDP by 12-13%.

In chapter 3, newly proposed TFET devices are evaluated for their power and performance gains. To benchmark TFET circuits, IntSim is used as a generic system modeler to benchmark and optimize TFET circuits and benchmark against conventional CMOS circuits. The supply voltage ( $V_{dd}$ ) and number of gates ( $N_{gates}$ ) are optimized for maximum throughput in instructions per second. Finally, we concluded that even with

optimization, TFET devices are best suited for low power applications due to their low leakage power and low on-current.

In chapter 4, we explore the impact of BEOL parasitics on fully placed and routed circuit designs. The BEOL RC parasitics are modeled for advanced 7nm technology nodes using process emulation tool SEMulator3D, and the impact of scaling of MB/liner on wire and via are explored using industry standard EDA tools. We see from the results that the performance gains depend on the circuit. Our results show 9.49% improvement in performance for a more moderately routing demanding circuit like AES and as much as 25.74% improvement in performance for a high routing demand LDPC circuit

Finally, in chapter 5 we explore device and BEOL scaling trends. Our work on modeling BEOL RC and evaluating key metrics on fully place and routed circuits is further extended to include wire vs via sensitivity analysis, evaluating alternative interconnect metal ruthenium, and high aspect ratio metals for both ruthenium and copper. We show that replacing only the local interconnects with ruthenium gives similar performance boost as being able to thin the MB/liner for the entire BEOL stack. For high-AR wires, we show that the improvement in the resistance is offset by the increased parasitic capacitance. However worsening resistance for future technology nodes may necessitate the need for high-AR wires.

## **6.2 Future Work, Scaling Challenges and Outlook**

Beyond the 7nm technology node, scaling roadmaps for 5nm and beyond show a new paradigm shift from FinFET to GAA devices. Some of these devices include nanoribbon and nanowire devices that will have new device characteristics with their own

unique set of benefits and challenges that will need to be benchmarked for performance and power gains.

In addition, Design Technology Co-Optimization (DTCO) plays a vital role in standard cell scaling with proposed buried power rails and stacked logic devices playing an important role in further packing more transistors into a smaller footprint [57-60]. These changes will need to be quantified and benchmarked to evaluate their performance benefits.

Beyond device and processing innovations, EDA tools also play an important role in the final system PPA. These complex tools have many features that impact the performance of the final design. In this body of work, our EDA flow utilizes various vendors for circuit RTL synthesis and physical design. For future work, fully integrating the EDA tools from one vendor, from synthesis through place and route, would take advantage of new features that provide feedback to the tool throughout the flow, providing more consistent results and optimization.

Future work would also benefit from further PDK development. Recharacterization of libraries for multi supply voltages and other metallization options will further explorations of BEOL options and their impact on the standard cell libraries. In addition, the circuit benchmarking would benefit from using larger circuits such as ARM processors that include memory in their design. This would better capture real world applications.

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