CHARACTERIZATION AND MODELLING OF ANOMALOUS PROPERTIES OF SIO_2, SI_3N_4 AND AL_2O_3 NANOLAMINATES

A Dissertation Presented to
The Academic Faculty

By

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology

December 2021

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In the Name of God, the Most Compassionate, the Most Merciful.

ACKNOWLEDGEMENTS

Many people deserve thanks for their help on my adventurous Ph.D. path. My utmost gratitude goes to my wonderful advisor, Professor Jeffrey Davis, whose kind demeanor and smile make everyone's day so much better. I was incredibly fortunate to have been educated by him not only in my field of work, but so much more beyond that. He taught me patience, perseverance, teamwork, scientific writing, critical reasoning, and has helped me tremendously to become an independent thinker and researcher. He lent me his scientists' "binoculars" so that among all the experiments, observations, and analysis, I could really focus on work that has the potential to make impactful contributions to the scientific community and the world. I am beyond lucky to have you as my advisor and mentor, Professor Davis, and I sincerely hope to continue my collaborations with you for years to come.

I am also very grateful to my other committee members: Professor Azad Naeemi and Professor Muhannad Bakair, for their encouragements, insightful comments, and valuable feedbacks. I further thank Professor John Cressler and Professor Hamid Garmestani for their time and accepting to be part of my committee.

I am thankful to all the people (every single person behind the scenes) who have helped me throughout my research ups and downs as well as all my professors and the ECE graduate advisors at Georgia Tech. A special thanks to Devin Brown, Walter Henderson, Eric Woods, Tran-Vinh Nguyen, and all the kind and wonderful IEN/MCF staff and trainers for training with the instruments, persistent help with experiments and inspiring me to work hard through my problems. I have learned so much from every one of you and I am forever grateful for that.

Words cannot express how truly grateful I am to my parents. My Mother, Dr Hamideh Tehrani Haeri, who has simply been the best and most important teacher every second of my life. This journey would have been impossible without you, Mum, and in the words of Abraham Lincoln, "All I am, or hope to be, I owe to my angel mother." My Father,

Dr Mirsaeid Mousavi Karimi, who rightfully talked me out of becoming a philosopher of mathematics at the naïve age of 17 when I was applying to undergraduate schools, and I thank God that I listened to him and ended up where I am today. You have always been an incredible mentor, guidance and support throughout my entire life, Dad. Words do not do justice in expressing how thankful I am to you. My lovely sister, Zahra, who constantly inspires me in every aspect of life. You are so thoughtful, intelligent and overly wonderful and without all your support, I would not have been able to finish this work. I also thank my parents-in-law, Mrs Masoumeh Tohidifar and Dr Ali Mohaghar for their kindness and all their supports and encouragements. I am thankful to God that I have all of you in my life.

And finally, but most importantly, I express numerous thanks to my lovely husband and life companion, Mohammad. Your selfless love, care and support is simply one of a kind. We started this journey together years ago and had no idea that it was going to be such a bumpy ride, but you stuck with me kind and strong throughout every single obstacle. Thank you for patiently putting up with any hardship that I imposed on you. It has been an incredible and unique experience to live, grow, study and raise our son together with you, Dr Mohammad Mohaghar. And last but not least, I thank my beloved 6-year-old son, Mehdi. He came into my life and taught me the true value of time. Not only he made these years of research more pleasurable (and of course challenging), but he made me truly become more productive. You taught me to observe every little detail of life and work with so much more love and passion, Mehdi. I apologize for all the times that I missed out on being with you and I hope that you read this one day when you grow up and realize the amazing impact you had on me and my work.

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SUMMARY

Current research on ($\sim$ 20 nm) SiO_2, Si_3N_4 and Al_2O_3 nanopowders (NPs) has revealed anomalous increases in permittivity over conventional bulk values due to localized dipole polarization effects on the surface of these NP particles. The present work has proposed alternative material structures, which are constructed using nanolithographic techniques to explore the high-polarization surface effects seen in NP research. This work has particularly focused on fabricating and modelling anomalous behavior of the permittivity of nanolaminate devices constructed from a combination of SiO_2, Si_3N_4 and Al_2O_3 materials. The main takeaways of this work are as follows:

1. Strong surface dipole formation leads to high average permittivity at the air interfaces of SiO_2, Si_3N_4 and Al_2O_3. Specifically, the behavior at these interfaces were investigated and modelled using FEM simulations to identify the average surface permittivity values over a specified volume.

2. As air breaks down at low electric field, the aforementioned devices were encapsulated with different combinations of SiO_2, Si_3N_4 and Al_2O_3 layers in interdigitated electrode (IDE) configurations. The subsequent measurements showed significant deviations in capacitances, which are attributed to the dipole and bond formations that occur at the interfaces between the nanolaminate layers. The nanolaminate IDE structures have electric fields that are parallel to the dielectric interfaces, which could activate the highly polarizable interfacial regions more effectively than the traditional parallel plate electrode (PPE) structures.

3. Because the materials in this study inherently have high breakdown field strengths there is a potential energy storage opportunity for future capacitive devices that utilize these experimental observations and simulation results. Preliminary projections indicate that capacitive devices with a high-density of nanolaminates with laminate

thicknesses from 2-5 nm could produce devices with volumetric energy densities that are on a much higher range than conventional supercapacitors.

CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1 Survey of Current Research

With the increasing energy needs for portable computation, communication, and sensor networks, it is important to develop integrated solid-state capacitive energy storage devices that can have operational lifetimes that match the corresponding transistor loads that they power, are quick charging, lightweight, and powerful. Subsequently, these capacitor devices will need to have dielectrics that are able to have low loss, compatible with very-large-scale integration (VLSI) technologies, have the ability to store electrostatic energy in a very small and dense space and a very large number of recharge cycles. One of the main current approaches to achieve such goals is to increase the effective dielectric constant of composite materials with high dielectric strength by incorporating high-k dielectric materials into existing nanotechnologies (Li, Zhang, and Ducharme, 2007). This chapter will review these approaches and contrast them to the approaches taken in this research.

1.1.1 High-k Dielectric Material and Device Research

The term high-k dielectric refers to material with a powerful ability to concentrate an electric field and hence provide increased capacitance, which leads to higher capability to store electrostatic energy. To be more precise, the energy density, U_E in a dielectric is defined by the following equation:

$$U_E = \int_0^E \varepsilon_0 \varepsilon_r E dE, \quad (1.1)$$

where ε_0 is the dielectric constant of vacuum, ε_r (i.e. k) is the relative permittivity of the material, and E is the applied electric field. Hence, it is possible to obtain higher energy

density by using materials that have some of the highest dielectric permittivities (ε_r). Due to their unique properties, high-k (i.e. high ε_r) materials have numerous applications in metal oxide and organic field-effect transistors (MOSFETs and OFETS) (Kamata, 2008; Peimyoo *et al.*, 2019), electroluminescent devices, non-volatile memory devices (Houdt, 2005; Ni *et al.*, 2018), actuators (Zhang *et al.*, 2002; Molberg *et al.*, 2010), and energy storage devices (Huang and Jiang, 2015). Similarly, scientists and engineers have tried to combine high dielectric strength polymers with high-k oxide nanoparticles in a polymer matrix (Huang *et al.*, 2014). However, the biggest problem with organic polymers is that, despite having a high breakdown field strength and ease of processing, most of them have a low dielectric constant and a high loss (Nasreen *et al.*, 2000). Another major disadvantages of integrating high-k materials into large-scale integrated systems is that they tend to have a narrower bandgap, which eventually leads to a larger leakage current (Zhang and Solanki, 2001).

Furthermore, there has been a variety of research in the area of enhancing the permittivity of dielectric materials using supercapacitors, superlattices of ferroelectric composites (Sarkar, Ranjith, and Krupanidhi, 2007), homogeneous ferroelectric materials (Ang and Yu, 2007), buried-layer capacitors, and laminate material. Supercapacitors, which currently have about an order of magnitude smaller energy density than lead acid batteries (Wu *et al.*, 2013) and electrolytic capacitors, can be distinguished based on the storage mechanism as electrochemical double-layer capacitors (EDLCs), pseudo-capacitors, and hybrid capacitors (González *et al.*, 2016). EDLCs rely on advanced electrodes made of nanoporous carbon materials that have extremely large surface areas to enhance the capacitance of these structures (Sharma and Bhatti, 2010; Guidi and Kawamura, 2010). However, EDLCs have electrodes that can wear out under heavy use, and their electrolytic aqueous solutions can evaporate (Signorelli *et al.*, 2009). Furthermore, EDLCs have low breakdown voltages that limit the energy density of these devices (Signorelli *et al.*, 2009).

Pseudo-capacitors, on the other hand, are fabricated with metal oxide based electrodes,

conductive polymers or porous carbons. They combine electrochemical and capacitive charge storage mechanisms and hold a large amount of charge compared to EDLCs as the charge storage involves rapid redox reactions that occur on the surface of the pseudo-capacitor electrode surface and not inside the bulk as observed in batteries. However, they also face major problems since fast redox reactions can cause the electrodes to swell and shrink, leading to very poor stability (González *et al.*, 2016).

Ferroelectric superlattices are composed of multiple thin layers of ferroelectric materials that are structurally compatible and are stacked in a sequence in such a way that they show unique properties that would not otherwise exist. They have a lot of potential and applications in novel device design including memory sensors, spin filters, magnetic sensors, etc. (Singh and Prellier, 2007). However, current multiferroic superlattice structures face a number of challenges. Firstly, they have a permittivity tunability of around only 55%, which is supposedly higher than any single homogeneous polycrystalline thin film of their constituent materials, but still remains relatively low (Sarkar, Ranjith, and Krupanidhi, 2007). Tunability, n, is a measure of dependence of the permittivity, ε, of the ferroelectric material on an applied electric field, E, which is defined as $n = \varepsilon(0)/\varepsilon(E)$. Further, any disruption in the periodicity of the superlattices can lead to a drastic decline in the polarizability of the ferroelectric structure.

Similarly, homogeneous ferroelectric materials such as Bi-doped $SrTiO_3$ ceramics that are observed to have "giant" dielectric constants that are caused by Maxwell-Wagner effects are shown to be very poor at storing energy since they have significantly high loss and low breakdown field strength (Ang and Yu, 2007). Furthermore, the other remaining aforementioned structures also typically do not have the breakdown field strengths to be a competitive alternative (Ducharme, 2009).

There are several factors that influence breakdown field strength and loss (leakage current), which include bonding structure, interfacial properties, bandgap of the materials, mean-free path of electrons, and possible electron tunneling mechanisms. In high-k ma-

terial, where narrower bandgap causes a large amount of loss, this limitation is significantly mitigated by inserting an insulating interfacial layer between the electrodes and the nanolaminate layers to block the charged carrier transport which reduces leakage current and enhances breakdown strength (Lee *et al.*, 2013; Coss *et al.*, 2011; Wu *et al.*, 2007). The researchers in Lee *et al.* (2013), for example, reported that using a 5 nm Al_2O_3 interfacial layer effectively optimizes the dielectric properties of Al_2O_3/TiO_x nanolaminates. In particular the data in Lee *et al.* (2013) shows that the 5 nm Al_2O_3 top interfacial layer can significantly reduce the leakage current density while maintaining a high dielectric constant. However, as it was shown by Lee *et al.* (2013) and Wu *et al.* (2007), ultra-thin (i.e. sub 2 nm) interfacial Al_2O_3 can cause direct tunneling and hence lower the breakdown field strength.

One of the most reliable ways to develop solid-state capacitive energy storage devices with high permittivity, large energy and power density, low leakage, and an enormous number of recharge cycles, is to use certain low loss, high-breakdown field strength materials such as silicon dioxide, silicon nitride, and aluminum oxide. Silicon dioxide (SiO_2) is one of the most popular choices of dielectrics with numerous applications in silicon based devices (Gritsenko, 2009). Silicon nitride (Si_3N_4) is second to SiO_2 as one of the most widely used dielectrics as well as an important material for use in electronic devices. It is a great moisture barrier so that thin, dense films of it are able to inhibit diffusion of water, oxygen and sodium ions. Aluminum oxide (Al_2O_3) has also been widely popular as an insulating material in large scale integrated devices due to its thermal stability, reliability, flexibility, accessibility and high breakdown field strength (Cho *et al.*, 2002; Yang *et al.*, 2015; Huang and Jiang, 2015; Kim *et al.*, 2009).

These dielectric films have also been widely used in dielectric gates, surface passivation films, as antireflective coating and passivation layers in integrated circuits (Bermudez and Perkins, 2004) due to their stability and resistance to diffusion. Oxide/nitride laminate structures, on the other hand, have been a popular choice of insulator in memory

storage devices, in particular, flash memory silicon chips, and capacitors because of the Si_3N_4/SiO_2 interface due to the abnormally large trapping of electrons (Gritsenko *et al.*, 1998; Gritsenko, 2009).

Similarly, many engineers and material scientists have experimented with utilizing the oxide/nitride interface in applications of thin SiO_2/Si_3N_4 electrets, which are used in sensors, actuators and vibration energy harvesters (Leonov *et al.*, 2012; Renaud *et al.*, 2013; Amjadi, 1999; Díaz-Ballester *et al.*, 2014; Chen, Lv, and Zhang, 2008). These electrets are compatible with complementary metal oxide semiconductor (CMOS) processing, which allows low cost production for large volumes (Renaud *et al.*, 2013). The potential barrier at the SiO_2/Si_3N_4 interface is hugely important for charge trapping at temperatures up to approximately 400 °C (Amjadi, 1999). The electrets with SiO_2/Si_3N_4 interface are extremely stable at high temperatures and have a very high breakdown field strength and low leakage current (Leonov *et al.*, 2012). Further, the Si_3N_4 layer provides an excellent barrier such that charge retention is possible even at elevated humidity without surface treatment (Amjadi, 1999; Díaz-Ballester *et al.*, 2014).

Driven by mobile electronic applications, the market for non-volatile memory and charge trap flash memory cells has been growing rapidly. The $TaN/Al_2O_3/Si_3N_4/SiO_2/Si$ (TANOS) structure has fast program/erase (P/E) speed and reliable properties compared with the traditional $Si/SiO_2/Si_3N_4/SiO_2/Si$ (SONOS) memory. This has been attributed to the existence of high-k Al_2O_3 blocking layer and energy band gap, which make it possible to have a higher electric field in the SiO_2 tunneling layer to enhance the P/E speed, and a higher electron barrier to suppress the gate back-tunneling during an erase operation (Yu-Qiong *et al.*, 2014; Liu *et al.*, 2012; Kim *et al.*, 2012). TANOS memory devices can be fabricated in a fast and simple manner, are robust to defect related leakage issues and allow optimal device scaling (Wang *et al.*, 2007). At the moment, however, the TANOS structures face problems such as slow erase and poor charge retention.

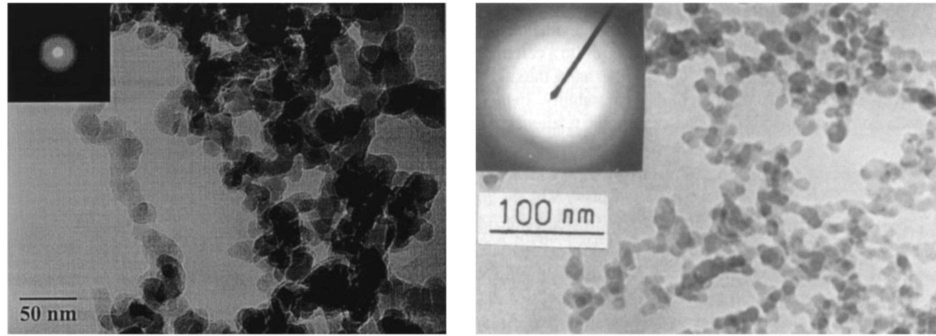
1.1.2 Nanopowder Compact Research

In the late 1990s, several researchers studied ways to enhance the permittivity of compact nanopowders of SiO_2, Si_3N_4, and Al_2O_3 (Mo, Zhang, and Wang, 1995; Tepper and Berger, 1999; Zhang *et al.*, 1996). The researchers in Mo, Zhang, and Wang (1995), Tepper and Berger (1999), and Zhang *et al.* (1996) found that these nanopowders, which have particle diameters on the order of 20 nm, can have anomalous increases in permittivity over bulk values that are associated with the localized surface dipole polarization properties of these nanoparticles. It should be noted that permittivity, which is a *macroscopic* property of the material, is related to polarization, which is a *microscopic* property of the materials using the Clausius-Mossotti relation as follows:

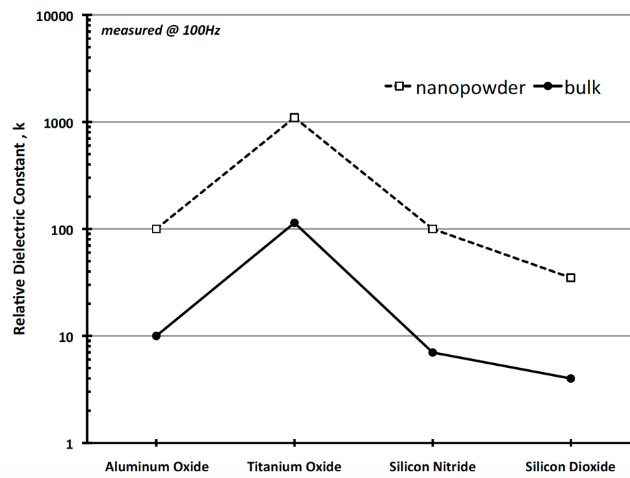
$$\frac{\varepsilon_r - 1}{\varepsilon_r + 2} = \frac{N\alpha}{3\varepsilon_0}, \tag{1.2}$$

where N is the number density of the polarizable molecules (in SI-units number per cubic meter), and α is the molecular polarizability (in SI-units C·m^2/V).

Figure 1.1 (a-b) illustrates TEM images of some of these nanopowders, which can have a $\sim 10\times$ increase in permittivity over bulk values at 100 Hz (Tepper and Berger, 1999; Zhang *et al.*, 1996). This type of polarization is not attributed to Maxwell-Wagner polarization that are seen in many heterogeneous mixture of lossy dielectrics (Kannadassan *et al.*, 2014; Shen, Ge, and Cao, 2001; Mo, Zhang, and Wang, 1995; Tepper and Berger, 1999; Zhang *et al.*, 1996) and ferroelectrics (Shen, Ge, and Cao, 2001; O'Neill, Bowman, and Gregg, 2000), where there is charge accumulation at the interface of two or more materials due to the difference in the materials' charge carrier relaxation times and conductivities. Instead, it is possibly due to enhanced rotational polarization of strong dipoles created by oxygen and nitrogen surface vacancies or localized space charge polarization due to possible dangling bonds present at the interfaces of the nanopowders (Zhang *et al.*, 1996).



(a) (b)



(c)

Figure 1.1: This image in (a) shows TEM bright field image of the as-received SiO_2 nanopowder with amorphous spherical particles of about 20 nm after Tepper and Berger (1999), and (b) shows bright field TEM image of nanostructured amorphous Si_3N_4 after Wang, Zhang, and Mo (1994). (c) illustrates the measured 10x increase in relative dielectric constants of nanopowder compacts over bulk values at 100 Hz after Mo, Zhang, and Wang (1995), Zhang *et al.* (1996), and Tepper and Berger (1999).

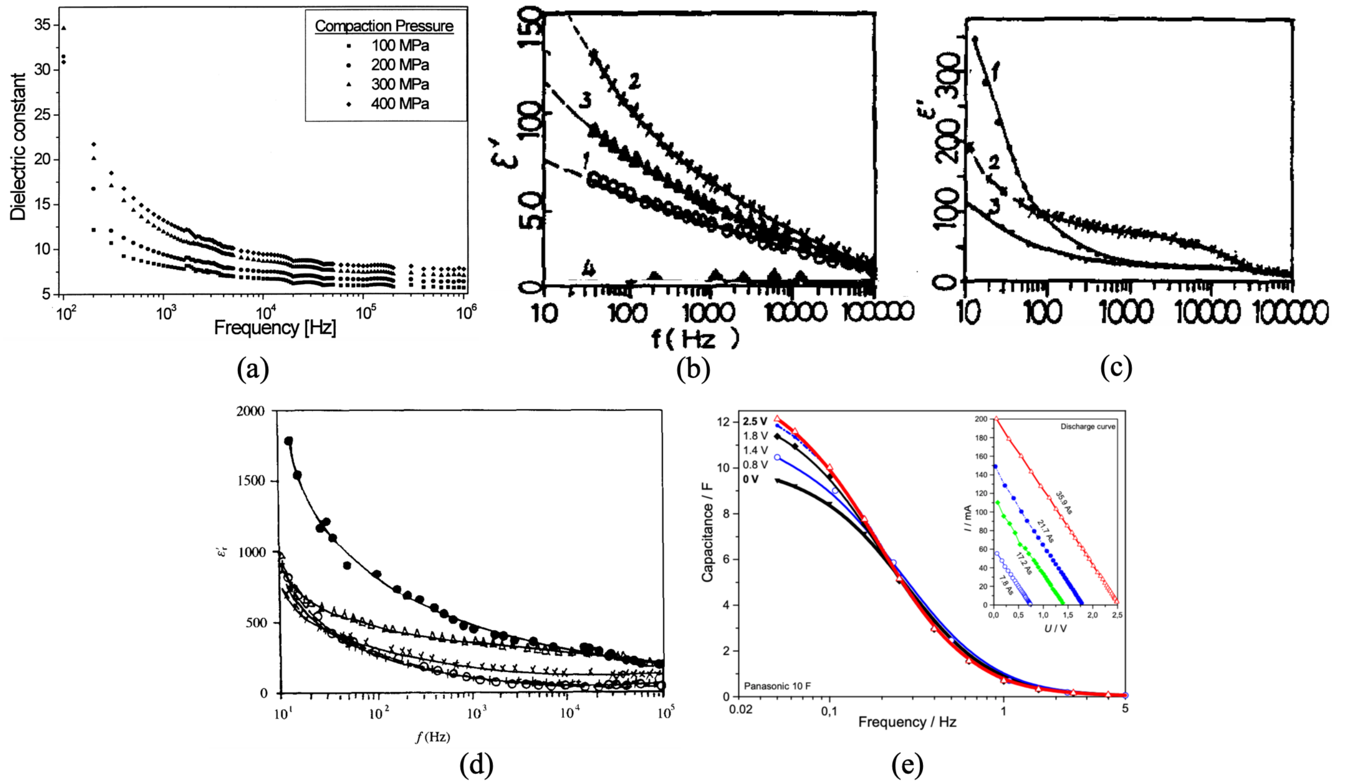


Figure 1.2: Plots of the frequency response of nanopowder research for silicon dioxide in (a) after Tepper and Berger (1999), alumina in (b) after Zhang *et al.* (1996), silicon nitride in (c) after Zhang *et al.* (1996) and (d) TiO_2 after Zhang *et al.* (1996). The graph in (e) illustrates the frequency response of a current commercial supercapacitor used as a storage device after Kurzweil, Frenzel, and Gallay (2005).

As seen in Figure 1.1 (a) after Tepper and Berger (1999) and Zhang *et al.* (1996), the internal surfaces of these porous compacts can be quite large. Unfortunately, the breakdown voltages of these porous nanopowder compacts are low because the breakdown field strength of the air voids is only 3×10^4 V/cm and the randomized structure and voids present in the compacts counteracts the surface effects and therefore lower the permittivity tremendously. This frequency dependence, as seen in Figure 1.2 (a-d) after Tepper and Berger (1999) and Zhang *et al.* (1996), limits high frequency applications of these materials.

However, the attribute of highly polarizable interfacial dipoles with slow relaxation times could make them highly suitable for energy storage applications, very much like enhanced supercapacitors. For example, Figure 1.2 (e) shows the frequency response of a

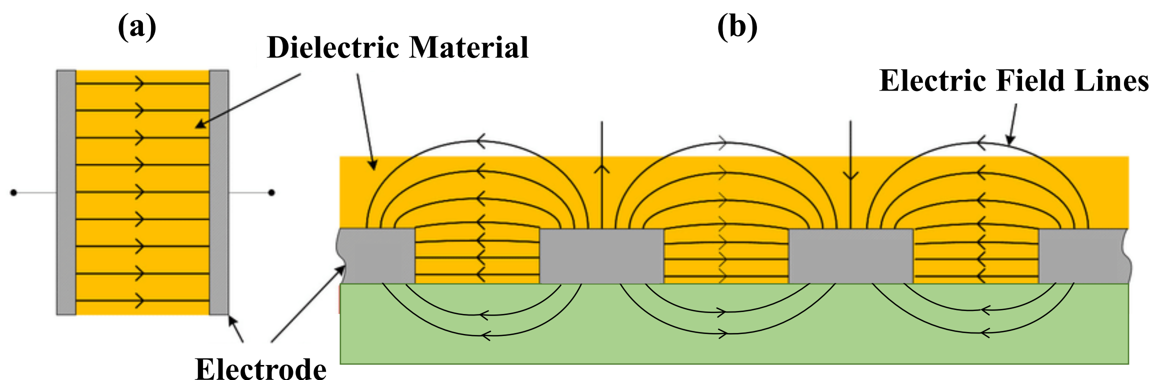


Figure 1.3: Schematic showing a comparison between (a) PPE and (b) IDE configuration.

current conventional supercapacitor and reveals that the general frequency response of the supercapacitors and nanopowders are very similar. This correspondence points to the potential application of these nanolaminate materials in this research work. The reason that supercapacitors have a lower frequency response is because of the relatively slow movements of ions that accumulate or evacuate from the surface of highly porous electrodes (Ostadi, Kazerani, and Chen, 2013). For nanopowder composites some of the proposed mechanisms, such as rotational dipoles created by oxygen or nitrogen vacancies, have slow relaxation times as well (Zhang *et al.*, 1996). At the moment, further characterization and understanding of these interfaces is necessary to ascertain if the anomalous behavior of the aforementioned nanolaminate materials can be incorporated into a possible solid-state capacitor device design that could be optimized for higher energy density and storage.

1.1.3 Electrode Configurations with MIM Structures

Solid-state capacitors with highly stable and low leakage dielectrics are indeed very important building blocks of modern electronics. In these systems, the electrode geometry makes a major contribution to increasing electric field and volumetric energy density. Electrode geometry can be of two primary types namely, parallel plate electrode (PPE) configuration and interdigitated electrode (IDE) configuration as shown in Figure 1.3.

Compared to the PPE configuration, the in-plane interdigitated design of electrodes are known to offer many advantages despite having lower areal energy density: 1) they have narrow interspaces between isolated electrode "comb" fingers achieved by routine microfabrication techniques or other advanced patterning fabrication techniques; 2) they have ultrahigh power and energy storage capabilities (Wu, Feng, and Cheng, 2014; Beidaghi and Gogotsi, 2014); 3) their structure allows for electrical measurements of very low conductivity materials, and 4) measurement of dielectric properties is possible due to a high inter-electrode capacitance.

IDEs and IDE arrays also have a myriad of applications including humidity sensors (Mahapatra *et al.*, 2020), biomedical sensing systems (Huynh, 2017), bacterial detection systems (Brosel-Oliu *et al.*, 2019), electrochemical sensors (Yassine *et al.*, 2016), electrostatic micropower generators (Rica, Fernández-Sánchez, and Baldi, 2006), impedimetric sensors (Gerwen *et al.*, 1998), and so forth. The in-plane configurations of IDEs could facilitate the fabrication of small and condensed energy storage devices that can be integrated with other microelectronic devices mounted on a planar integrated circuit, which is beneficial for the miniaturization of the entire nano- and microelectronic systems. These merits allow IDE energy storage systems to be prospective candidates for direct on-chip integration to power miniaturized electronics.

1.1.4 Rationale for Proposed Research

This research proposes alternative material structures, which will be constructed using nanolithographic techniques to accentuate and capitalize on the empirical observations and explore the high-polarization surface effects seen in nanopowder research. As part of the proposed research, characteristics of the interfacial regions will be studied and modelled using the appropriate fabrication, characterization and simulation modelling tools, while at the same time virtually eliminating voids and randomized microstructure inherent in current nanopowder compacts. In particular, this work will focus on demonstrating and modelling

anomalous deviations of the permittivity of nanolaminate composite materials constructed from a combination of SiO_2, Si_3N_4, and Al_2O_3 an IDE configuration. In the proposed IDE geometry, the nanolaminate composite structures have electric fields that are parallel to the dielectric interfaces, and this tangential direction of polarizability has not been exclusively studied in the literature. Potential deviations in permittivity at these interfaces could be present because of variations in dipole and bond formations that occur at the interfaces between the laminate layers. Such anomalies have been measured in nanopowder compacts over the last 20 years (Tepper and Berger, 1999; Wang, Zhang, and Mo, 1994); however, no systematic study characterizing the average polarizability of these interfacial dipoles for these materials exist in the literature.

Thin films have been shown to have an increase in dielectric breakdown strength (Shen, Ge, and Cao, 2001), and micro-laminate films have been used in high voltage and high temperature applications (Leonov *et al.*, 2012; Amjadi, 1999; Díaz-Ballester *et al.*, 2014); however, no studies of sub-10 nm PECVD-grown (SiO_2 and Si_3N_4) and electron-beam evaporated (Al_2O_3) laminate structures of these materials have been made to understand the impact on composite dielectric permittivity, leakage current and breakdown field strength. The overall goal of this investigation is to determine if nanolaminate structures of these high dielectric strength materials that are commonly used in VLSI fabrication can be useful in the construction of compact energy storage devices. The second part of this chapter explains and elaborates on the details of the goals to be obtained in this research.

1.2 Objectives and Outline of Present Work

There are five main objectives to this proposed research ranging from characterizing interfacial polarizability to understanding if these interfacial effects can be used to construct a new energy storage device. Specifically, they are listed as follows.

1. Develop new characterization methods to accurately model the average dipole polarization at dielectric interfaces of nanolaminate stacks.

Understanding the effective polarizability and dipole density of dielectric and semiconducting interfaces has numerous applications in the development of sensors, computational elements, and energy storage devices. The complexity of the molecular and bonding topology makes it difficult to characterize the average polarizability and dipole density that is needed for device modeling and optimization. Therefore, this research will develop a new and efficient technique to characterize the average dipole density and polarizability that can develop between dielectric interfaces. The resultant interfacial polarizability is one that is fully distinguished from enhanced polarizability resulting from Maxwell-Wagner effects as seen in Kannadassan *et al.* (2014) and Shen, Ge, and Cao (2001).

To accomplish this goal, this research will couple the experimental fabrication and characterization of high density, in-plane IDE capacitors with a finite element method (FEM) COMSOL Multiphysics simulation model to investigate possible anomalous interfacial polarizability at abrupt dielectric interfaces. In the FEM simulations, these interfaces will be modelled as thin ($\sim$ 1 nm) homogeneous layers. This general model has been proposed by Giustino, Umari, and Pasquarello (2003) and Giustino and Pasquarello (2005) whose authors performed extensive quantum mechanical (QM) simulations; however, this model has not been adequately explored in EM device simulation of energy storage devices.

Specifically, as this work will show in Chapter 2 and 3 of this thesis, the behavior at the interface between SiO_2/air, Si_3N_4/air, Al_2O_3/air, Si_3N_4/SiO_2, Al_2O_3/SiO_2 and Al_2O_3/Si_3N_4 will be studied to identify the average interfacial permittivity values. There are currently many research papers that have studied and characterized charge trapping at such interfaces and extracted bulk permittivities (Gritsenko *et al.*, 1998; Gritsenko, 2009; Gritsenko *et al.*, 1999; Theeten *et al.*, 1981), but none have touched upon interfacial dipole formation and its impact on polarization enhancement. For devices that need to capitalize on molecular polarization at material interfaces, this new methodology provides reliable and repeatable results that can be used to create accurate electromagnetic and circuit models.

2. Measure air/dielectric dipole response for SiO_2, Si_3N_4, and Al_2O_3 materials.

To fully engage the interfacial dipoles that exist between the nanocomposite layers of SiO_2, Si_3N_4, and Al_2O_3 dielectric materials, this research will use an in-plane, IDE capacitor geometry where the nanolaminate composite structures have electric fields that are *parallel* to the dielectric interfaces. This IDE capacitor configuration is highly sensitive to the polarization of the interfacial regions of the uninterrupted path of the interfacial plane from one electrode to another. From a circuit point of view, this interface connects the electrodes and, therefore, presents itself as a parallel capacitive component that directly adds to the bulk capacitance.

Currently, there are no experiments with nanolaminates and microlaminates of SiO_2, Si_3N_4, and Al_2O_3 dielectric materials in an IDE configuration, which highlights an opportunity for possible discovery in this research. Further, this investigation provides new and efficient methodologies to study the anomalous polarizability at the interface of SiO_2/air, Si_3N_4/air, and Al_2O_3/air nanocomposite structures using reliable two-dimensional FEM and equivalent circuit models. Understanding the surface polarization is important for these materials as the air-dielectric interface has many applications in micro-electro-mechanical systems (MEMS) capacitor cantilevers (Prashanthi *et al.*, 2013), humidity sensors (Saha *et al.*, 2005; Cho *et al.*, 2020; Meira *et al.*, 2020), surface fluorescence studies (Tarcha *et al.*, 1999), and imaging liquid films, droplets, and other weakly adsorbed material using surface polarization forces (Hu, Xiao, and Salmeron, 1995).

In order to validate the methodology in Task 1, the first set of experiments will focus on extracting the average permittivity at the interface between SiO_2, Si_3N_4, and Al_2O_3 and air (i.e. the average surface permittivity). This is important as it sets the benchmark for further studying the highly polarizable dipoles which exist at the interface of these dielectrics in nanolaminate stacks. Following the experiments explained previously in Task 1, high-density capacitive IDE metal geometries will be fabricated using electron beam lithography (EBL) on top of three primary insulators namely, SiO_2, Si_3N_4 and Al_2O_3. The SiO_2 and Si_3N_4 composite layers will be grown using plasma enhanced chemical vapor deposition

(PECVD), and the Al_2O_3 layers will be grown using an electron-beam evaporator tool. The SiO_2/air structure will have a 1000 nm SiO_2 layer, the Si_3N_4/air will have a 900 nm SiO_2 substrate layer and a 100 nm of Si_3N_4 layer, and finally, the Al_2O_3/air structure will have a 900 nm SiO_2 substrate layer and a 100 nm of Al_2O_3 layer. Fabrication, characterization and FEM modelling and simulation of these three structure types will give the opportunity to characterize and measure the properties of highly polarizable dipoles at these dielectric/air interfaces, which have not yet been extensively studied or understood in literature.

3. Measure dielectric/dielectric dipole response and dielectric strength for SiO_2, Si_3N_4, and Al_2O_3 nanolaminates using IDE capacitor structure.

Another area that has potential ramification for solid-state storage devices is the interfacial polarizability and the subsequent effective permittivity of interfacial regions between ultra-thin nanolaminate layers of SiO_2, Si_3N_4 and Al_2O_3. For example, many researchers have tried to utilize the oxide/nitride interface through the application of thin SiO_2/Si_3N_4 electrets, which are used in sensors, actuators and vibration energy harvesters (Leonov *et al.*, 2012; Renaud *et al.*, 2013; Amjadi, 1999; Díaz-Ballester *et al.*, 2014; Chen, Lv, and Zhang, 2008). These electrets are compatible with CMOS technology and processing and could have low cost production for ultra-large volumes (Renaud *et al.*, 2013). Further, the authors in Lisiansky *et al.* (2006) and Bartzsch *et al.* (2009) have studied SiO_2/Si_3N_4/Al_2O_3 stacks for scaled-down memory devices, and as insulation layers in pressure sensors due to their high breakdown field strength, high insulation resistivity and high area yield, respectively. Finally, these same three materials have been used in nanopowder compacts that have demonstrated enhanced permittivity due to interfacial dipoles (Mo, Zhang, and Wang, 1995; Tepper and Berger, 1999; Zhang *et al.*, 1996).

Therefore, as part of this research, the characteristics of these nanolaminate interfacial regions will be studied in PPE and IDE capacitor devices where in the latter, the dielectric layers will be encapsulated in order to maximize the breakdown field strength of these devices. Similar to the structure proposed earlier for dielectric/air experiments, these

nanolaminate layers in the IDE devices will be oriented relative to the electrodes so that the electric fields will have a large component that is parallel to the laminate interfaces so as to maximally activate the highly polarizable dipoles. As mentioned in Task 2, the circuit model perspective emphasized the importance of using an IDE device to study the effective permittivities of these interfaces because they can be modelled as a parallel capacitive component. PPE structures are not as sensitive because an interfacial layer presents itself as a series connected capacitor, and having a large anomalous interfacial permittivity would not significantly change the overall measured capacitance of a PPE device.

4. Characterize alternating encapsulation layers of thin nanolaminates for anomalous interfacial permittivies and stress analysis using IDE structure.

Because energy storage devices that might utilize these newly characterized interfacial properties will need multiple layers, this task will explore the implications of residual stresses that can build up in these structures. The bulk relative dielectric constants of SiO_2, Si_3N_4 and Al_2O_3 materials will be measured as a part of this research using conventional parallel plate capacitors. In addition, this research effort will also explore the impact of residual stress on the permittivity characteristics of alternating nanolaminate encapsulation layers of SiO_2 and Si_3N_4 dielectric materials in an IDE device configuration using FEM modeling and experimental measurements.

5. Run current-voltage testing and estimate the maximum projected volumetric energy density limits of a small-scale energy storage device.

This final task will include the characterization, modelling, and current-voltage tests and current-density-voltage characteristics of the aforementioned nanolaminate IDE capacitor and PPE structure types with anomalies at dielectric interfaces. It will also be demonstrated whether they have potential application as energy storage devices. The permittivity and breakdown voltage characteristics at these interfaces could have highly important implications for solid-state capacitive energy storage devices. Using improved,

state-of-the-art nanolaminate devices could help overcome many of the shortcomings of current energy storage technologies. For example, typical electrochemical batteries have low power density and a limited number of recharge cycles. The power density issue of batteries results in slow recharge times and limits their applicability to drive high-power loads. Limited recharge cycles can result in high recurring cost for products, and the environmental problems of battery disposal will only get worse as our society continues toward a heavy dependence on electrical energy storage. Hence, if the suggested test structures prove effective, this technology could impact a broad range of energy storage applications ranging from transportation, computing, communication, robotics, renewable-energy power stations, microburst energy storage devices for energy harvesting applications in ultra-low power computing and sensor applications and a variety of portable applications.

CHAPTER 2

THE EXPLORATION OF ANOMALIES AT THE INTERFACES OF SIO_2, SI_3N_4 AND AL_2O_3 NANOLAMINATES WITH AIR

2.1 Introduction

In this part of the research, the average surface polarization characteristics of the interfacial regions between SiO_2/air, Si_3N_4/air, and Al_2O_3/air have been studied and effective permittivities are extracted at the dielectric/air surface. The result of the work in Chapter 2 is the development of a macroscopic material model at dielectric interfaces that has parameters that can be empirically extracted using a nanoscale IDE (comb) capacitor structure coupled with quasi-electrostatic FEM simulations. This chapter will explain and discuss the fabrication process of PPE and nanolaminate IDE structures, FEM modelling and simulation, the errors associated with both fabrication and simulation and the results and discussions of this part of the research.

2.2 Microfabrication of PPE Structures

In order to measure the bulk characteristics of the PECVD deposited SiO_2 and Si_3N_4 and of the e-beam evaporated Al_2O_3 layers, homogeneous PPE capacitive structures are fabricated and tested. These results will be used in the simulation of more complicated IDE structures that are discussed later in the chapter.

2.2.1 Substrate Preparation

For this fabrication process and all the experiments performed in this research, a lightly-doped p-type $< 100 >$ silicon wafer with resistivity of 8-12 Ω-cm is used as a substrate. In most MEMS device fabrications, it is common to use single-side polished p-type wafers

(with boron as dopant) with $< 100 >$ orientation due to their relatively higher resistivity. Next, the wafers are coated 1 μm SiO_2 layer using the Unaxis PECVD tool to improve electrical isolation of the substrate, promote adhesion of the layers deposited later on top, and provide protection of the wafers against any diffusion. This step of the process is depicted in Figure 2.1 (a).

2.2.2 Photoresist Spin-Coating

A thin layer of polymethyl methacrylate (PMMA) A6 photoresist layer is created on the aforementioned SiO_2 layer by spin-coating using the SPS G3P8 Spin Coater. An initial ramping stage from 0 to 5000 rpm at an acceleration of 2000 rpm/s is used which helps spread the photoresist evenly and cover the entire sample as shown in 2.1 (b). To measure the thickness of the photoresist layer, first, a small part of the photoresist is scratched, then the resist thickness is measured using the Tencor P15 Profilometer.

2.2.3 EBL Exposure and Development of Bottom Electrode

In this step, the photoresist layer on the deposited SiO_2 is exposed by the Elionix ELS G-100, which is a high-speed, ultra high-precision thermal field emission (TFE) EBL system at an exposure current of 3 nA. PPE capacitors with 76 μm by 76 μm bottom electrode plates with a with 50 μm by 50 μm pad extension as seen in Figure 2.1 (g) are fabricated on the spin-coated wafer. During this process, electrons transfer their energy and scatter within the PMMA photoresist, eventually causing a form of scission which breaks the original polymer into segments of lower molecular weight. The patterns are developed using a mixture of 1 part methyl isobutyl ketone (MIBK) and 1 part isopropanol (IPA) for approximately 2 minutes and inspected post develop using an Olympus MX61 Microscope. This step of the process is illustrated in Figure 2.1 (c).

2.2.4 Bottom Electrode Evaporation and Lift-Off

E-beam evaporation is a thermal evaporation process, which allows the direct transfer of a large amount of energy into the source material, enabling the evaporation of metals and dielectric materials with very high melting temperatures. Further, e-beam evaporation has much higher deposition rates than processes such as sputtering or resistive evaporation. There are currently 3 e-beam tools at the IEN facility at Georgia Tech: the CHA E-beam Evaporator 1 (dielectrics), CHA E-beam Evaporator 2 (metals), and the Denton Explorer E-Beam Evaporator (metals and dielectrics). In this research, the metallic PPE plates and contact pads are deposited using the Denton Explorer E-Beam Evaporator where a high-intensity beam of electrons is focused on the center of a crucible containing the metal to be evaporated. During this step of the fabrication process, a 10 nm Cr layer and a 100 nm Cu layer are heated to a high vapor pressure by electron bombardment in high vacuum which are then transported by diffusion where the Cr and Cu layers are deposited by condensation on the sample respectively as shown in Figure 2.1 (d). It is important to note that for the sample devices that will later have a Al_2O_3 dielectric layer deposited in between the electrodes, an extra 5 nm Cr layer is evaporated on the 100 nm Cu layer for better adhesion between Cu and Al_2O_3. Next, for lift-off, the metallized wafer is doused in a Microposit Remover 1165 heated at 120 °C for a duration of 1 hour and then it is thoroughly cleaned using a triple wash with acetone, IPA and methanol followed by a 10 s ultrasonic bath.

2.2.5 Deposition and Evaporation of Dielectric Layers

PECVD is a process that utilizes plasma to enhance chemical reaction rates of the precursors at a fast rate and lower temperatures, which is highly critical in the manufacturing process of semiconductors. There are currently 2 PECVD tools available at Georgia Tech: the Unaxis PECVD, and the Oxford Inductively Coupled Plasma (ICP) assisted PECVD. Both PECVD tools enable high density and relatively low temperature (less than 400 °C) thin film deposition of SiO_2 and Si_3N_4 dielectrics. In this step of the PPE fabrication pro-

cess, the wafer is cleaved into three samples, on two of which, 100 nm of SiO_2 or Si_3N_4 layers are deposited using the Unaxis PECVD. For the third PPE sample, the Denton Explorer is used to evaporate 100 nm of Al_2O_3 dielectric film. This step of the process is shown in Figure 2.1 (e). The thicknesses of all three dielectric layers are verified using the Woollam M2000 Ellipsometer.

2.2.6 EBL Exposure, Development, Evaporation and Lift-Off of Top Electrode

Similar to the previous exposure of the bottom electrode, the three samples are initially spin-coated with (PMMA) A6 photoresist at 5000 rpm at an acceleration of 1000 rpm/s and the top electrode pattern is exposed at a current of 3 nA using the EBL tool. The samples are then developed using a mixture of 1 part MIBK and 1 part IPA and inspected post develop using an Olympus MX61 Microscope. The final step of the PPE fabrication process is the evaporation of the top electrode metal, which consist of a 10 nm Cr layer and a 100 nm Cu layer similar to the bottom electrodes minus contact pad extensions. Next, the samples are left in a Microposit Remover 1165 solution at 120 °C for a duration of 1 hour and then cleaned using acetone, IPA and methanol followed by a brief ultrasonic bath (if needed). These last steps of PPE fabrication process are illustrated in Figure 2.1 (f).

2.3 Electrical Measurements and PPE Permittivity Extraction

To extract the bulk relative dielectric constants of SiO_2, Si_3N_4 and Al_2O_3, multiple electrical tests are carried out using an HP4284A LCR 4-point probe meter at f = 1 kHz with an AC amplitude of 1 V with zero offset bias and the average measured capacitance values for the three PPE devices are shown in Table 2.1. Two of the probe tips (V_{High}, I_{High}) are placed on the top electrode pad and the remaining two (V_{Low}, I_{Low}) are positioned on the contact pad for the bottom electrode. Extra care must be taken as to not destroy the metallic electrodes as they can easily scratch off with the probe tips.

Next, with the use of an analytical parallel plate model, $\varepsilon_r = Cd/\varepsilon_0 A$, with $A =$

Table 2.1: Capacitance measurements and bulk permittivity extraction of SiO_2, Si_3N_4 and Al_2O_3 PPE structures with 100 nm dielectric thicknesses and 76 μm by 76 μm plate area.

Dielectric Layer	Average Measured C [pF]	Extracted Bulk Permittivity
SiO_2	2.20	k_{SiO_2} = 4.3
Si_3N_4	3.37	$k_{Si_3N_4}$ = 6.6
Al_2O_3	5.08	$k_{Al_2O_3}$ = 9.9

Table 2.2: PECVD deposition of SiO_2 and Si_3N_4 and e-beam evaporation of Al_2O_3 dielectric layers for the three IDE structure types.

Structure	Deposited Layer	Total Thickness
Type 1	SiO_2	1000 nm
Type 2	SiO_2	900 nm
	Si_3N_4	100 nm
Type 3	SiO_2	900 nm
	Al_2O_3	100 nm

5.78×10^{-9} m^2, $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m, and $d = 100 \times 10^{-9}$ m, these measured capacitance values are used to extract the relative bulk permittivity ε_r, of SiO_2, Si_3N_4 and Al_2O_3 as k_{SiO_2} = 4.3, $k_{Si_3N_4}$ = 6.6 and $k_{Al_2O_3}$ = 9.9, respectively as shown in Table 2.1.

2.4 Microfabrication of IDE Capacitive Test Structures

In the first step of the IDE fabrication process, which is depicted in Figure 2.2 (a), three lightly-doped p-type $< 100 >$ Si wafers with resistivity of 8-12 Ω-cm are initially coated with a SiO_2 layer using the Unaxis PECVD tool to improve electrical isolation and provide protection of the wafers against diffusion. Each wafer holds a distinct structure type that has various combinations of SiO_2, Si_3N_4 and Al_2O_3 dielectric layers as listed in Table 2.2 and shown in Figure 2.3.

Once the desired combination of SiO_2, Si_3N_4 and Al_2O_3 layers have been deposited on each 4” wafer as shown in Figure 2.2 (b), they are cleaved into smaller, 1” square samples using a diamond scribe. The thicknesses of the thick SiO_2 layers are verified using a Nanospec Reflectometer, and for the 100 nm Si_3N_4 and Al_2O_3 layers, the Woollam M2000 Ellipsometer is used.

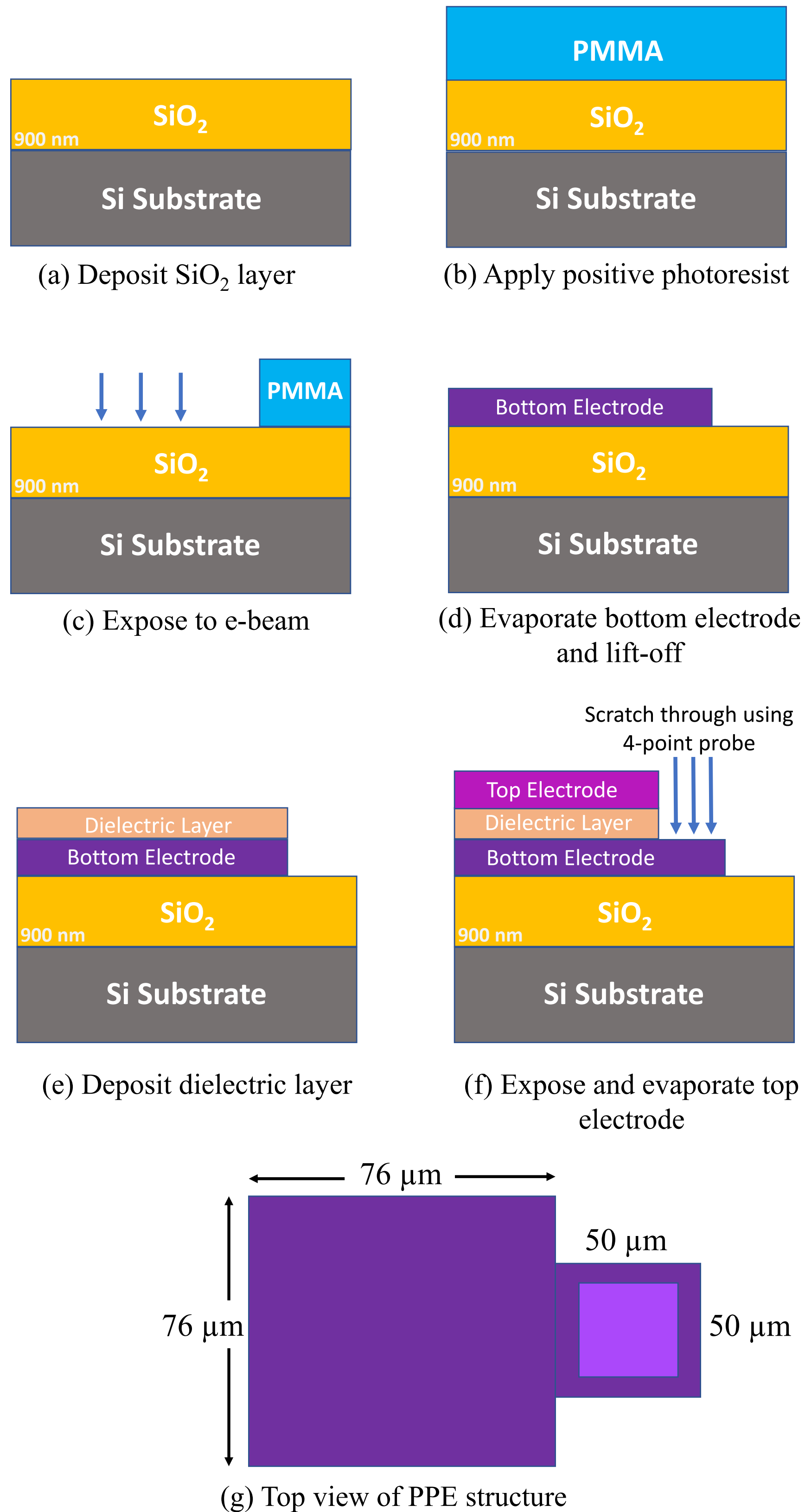


Figure 2.1: Main steps of the capacitive PPE structure fabrication process (figures are not to scale).

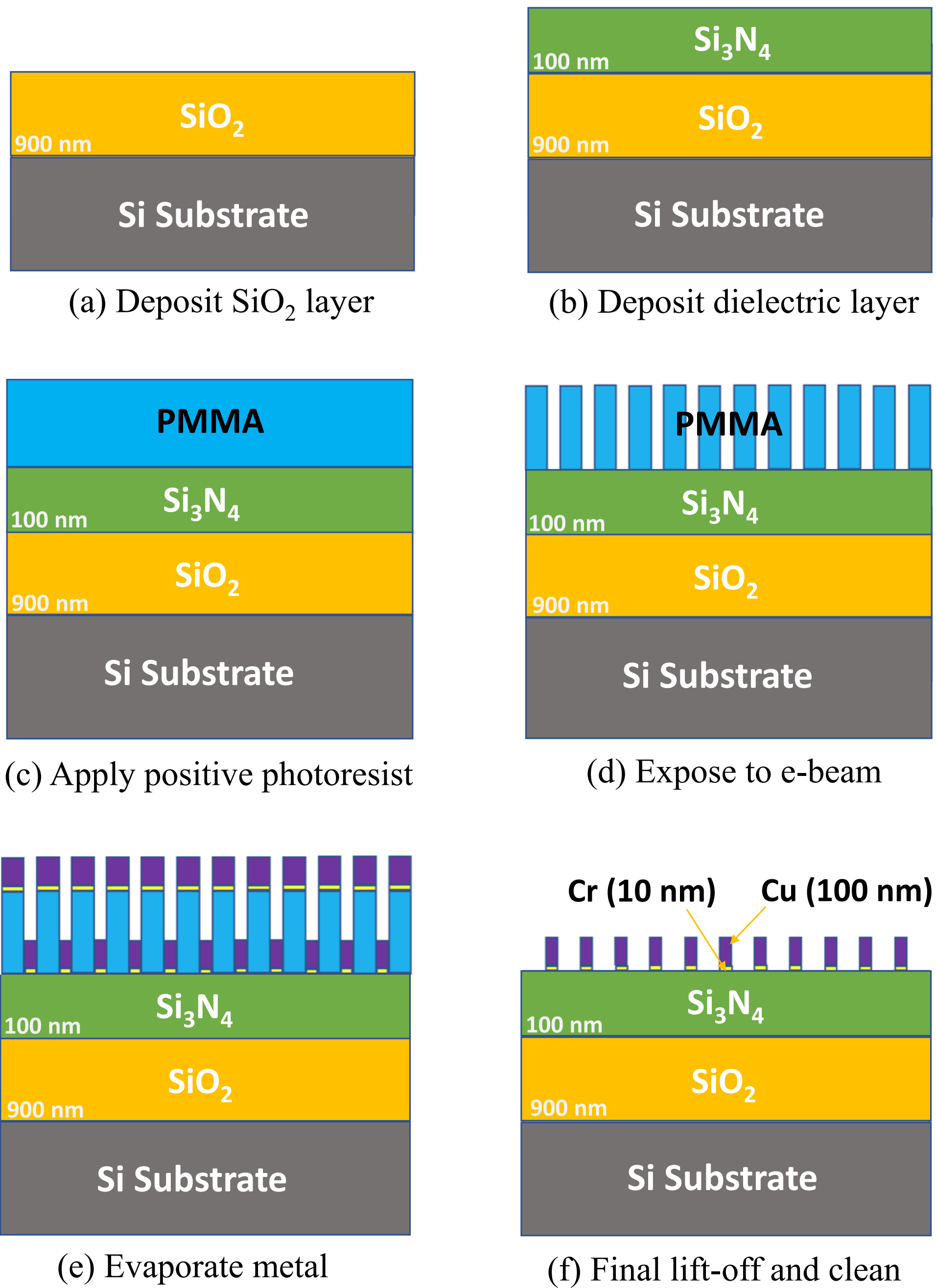


Figure 2.2: Main steps of the IDE capacitive test structure fabrication process (figures are not to scale).

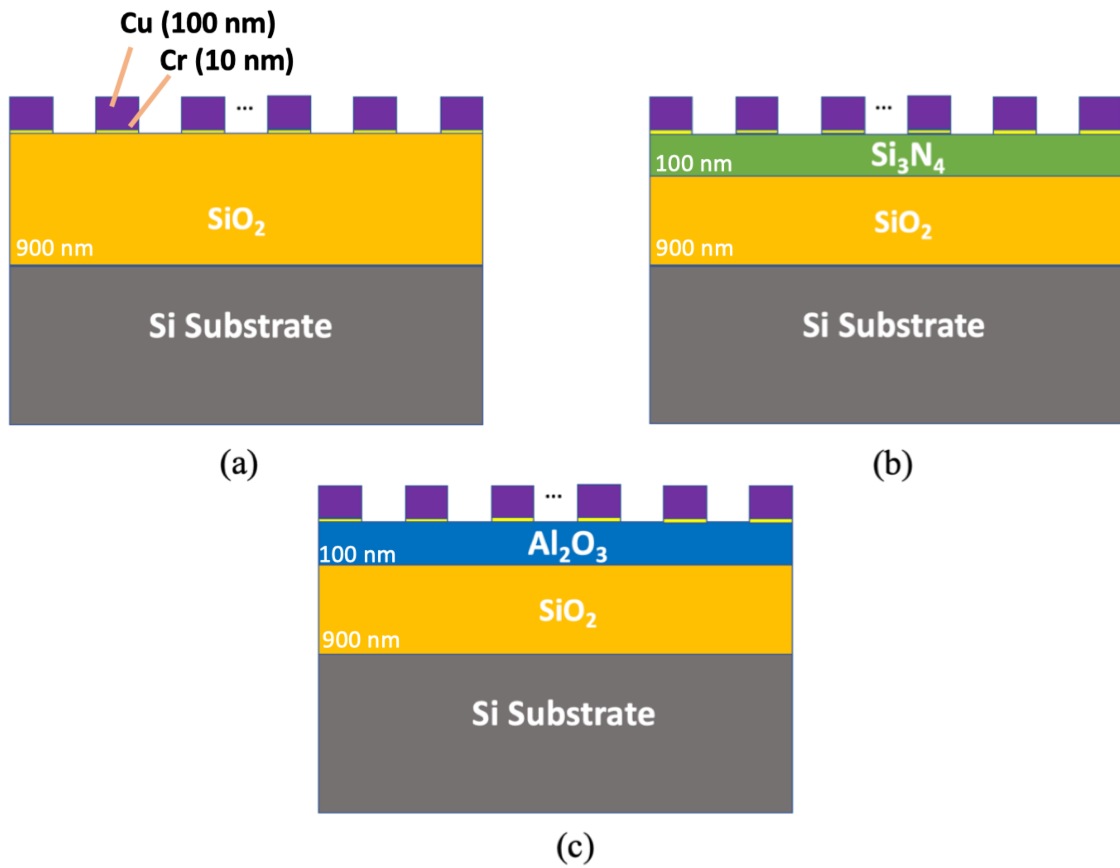


Figure 2.3: Three IDE test structures where (a) structure Type 1 is composed of 1000 nm SiO_2, (b) structure Type 2 consists of 900 nm of SiO_2 and 100 nm of Si_3N_4 and (c) structure Type 3 is made of 900 nm of SiO_2 and 100 nm of Al_2O_3 (figures are not to scale).

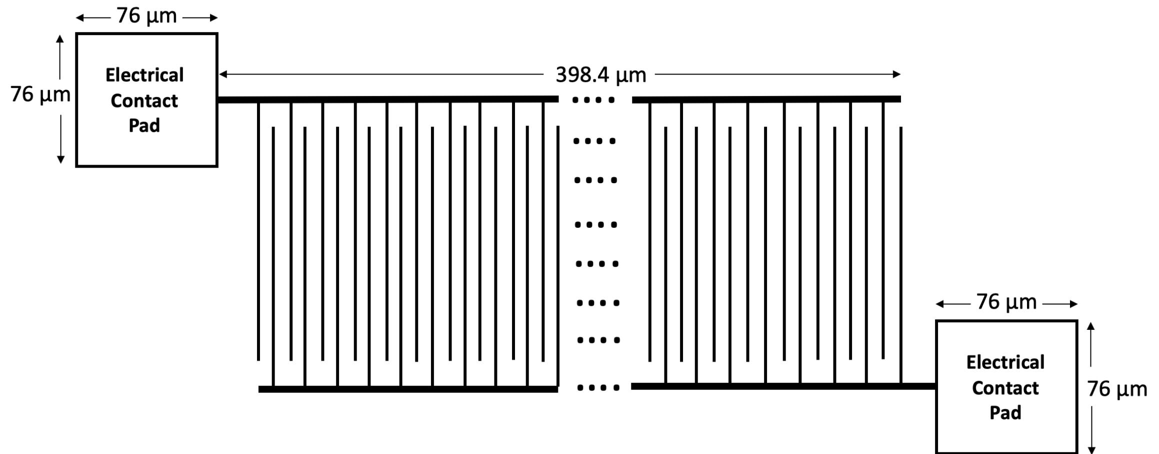


Figure 2.4: Top view schematic of the experimental capacitor test structures created with EBL to achieve high energy density with small electrode-finger dimensions.

A layer of PMMA A6 photoresist layer is then created on the aforementioned deposited layers by spin-coating using the SPS G3P8 Spin Coater at 5000 rpm at an acceleration of 2000 rpm/s as shown in 2.2 (c). The thickness of the photoresist layer is measured using the Tencor P15 Profilometer. In the next step, the photoresist layer on the pattern shown in 2.2 (d) is exposed by the Elionix ELS G-100 EBL tool at an exposure current of 3 nA. In-plane IDEs with electrode-finger spacing of 200 nm are fabricated on each sample with 1000 interleaved electrode-fingers as shown in Figure 2.4. The patterns are then developed using a mixture of 1:1 MIBK:IPA solution and inspected post develop using an Olympus MX61 Microscope.

Similar to the PPE devices, the metallic electrode-fingers and the contact pads of the IDE structure (10 nm Cr followed by 100 nm Cu) are evaporated using the Denton Explorer E-Beam tool as shown in Figure 2.2 (e). The finger widths and spacings of the capacitors are verified using a Hitachi S-4700 Scanning Electron Microscope (SEM) as shown in Figure 2.5.

In order to have good metal lift-off from the very fine and delicate EBL features of the capacitor devices, it is important to have PMMA photoresist patterns which have a slight undercut in the sidewalls. In this way the metals - Cr and Cu in this case - which have

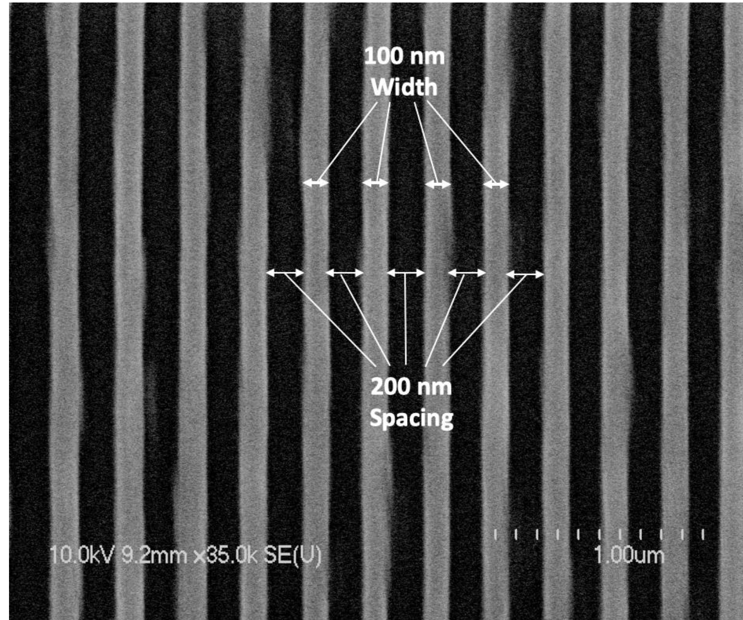


Figure 2.5: SEM image of the top view of the electrode-fingers with 200 nm spacing for the three IDE capacitor structures.

been deposited using the E-Beam Denton Explorer, do not adhere to the patterns' sidewalls which would prevent release of the metal films on top of the PMMA layer from the metal films adhering to the surface of dielectric layers. For lift-off as displayed in Figure 2.2 (f), the metallized sample is left in a Microposit Remover 1165 heated at 120 °C for a duration of 2 hours to remove all the unwanted metal from the capacitive patterns on the sample. Next, the samples are cleaned using a triple wash with acetone, IPA and methanol followed by a brief ultrasonic bath.

2.4.1 Experimental Sources of Variation

In order to extract a good approximation of the average dipole polarization of the material interfaces, the possible device variations, errors in measurement, and modeling errors need to be understood and minimized. In order to approach this minimization, highly precise lithographic techniques and robust device designs are chosen to help achieve this goal.

In all nano- and microfabrication processes and experimentations, there are process induced variations, which can impact multiple design parameters, yield and device reliability.

For the experiments carried out for this research, the possible variations include: (a) deposition uniformity of dielectric laminate layers, (b) geometric variations, and (c) capacitive finger yield. Despite the fact that PECVD is not commonly used for thin laminate layers, it has substantial advantages over other chemical vapor deposition (CVD) and atomic layer deposition (ALD) techniques including higher deposition rates at relatively lower temperatures of 250 °C to 400 °C. For small area samples and substrates, PECVD is an excellent choice to achieve conformal Si_3N_4 and SiO_2 laminate layers which adhere well to the substrate (Mackenzie *et al.*, 2005; Warner *et al.*, 2012) and can have high quality interfacial transitions with low defects. Similarly, e-beam evaporation of Al_2O_3 has major advantages including high control of evaporation rate and almost zero thin film contamination (Hong-Hsin Huang).

In a 100 keV EBL exposure which is used in this research fabrication process, beam aberrations and more importantly electron scattering events known as proximity effect, can cause undesired areas near and outside of the patterns to be exposed by the incident beam. This can lead to poor yield, significant irregularity and variations in patterns and even pattern collapse. Geometric variations are more prominent in highly dense features and can result in spacing differences between adjacent fingers, finger line widths, line-end shortening and corner rounding due to proximity effect.

EBL exposure dose represents the charge concentration of the electron beam and determines the amount of photoresist removed during developing on the desired pattern. Fluctuations in the exposure dose, which could have a more pronounced effect due to photoresist thickness variation, can change the amount of embedded electrons in the laminate SiO_2, Si_3N_4 and Al_2O_3 layers as well as cause geometric device variations. Specifically, this can result in finger spacing changes at different exposure doses that can have an impact on capacitance measurements. In fact, at higher doses it is observed that finger widths increase while the spacing between the fingers decrease which leads to higher capacitance measurements as shown in Figure 2.6. To validate that this dose dependence and enhancement of

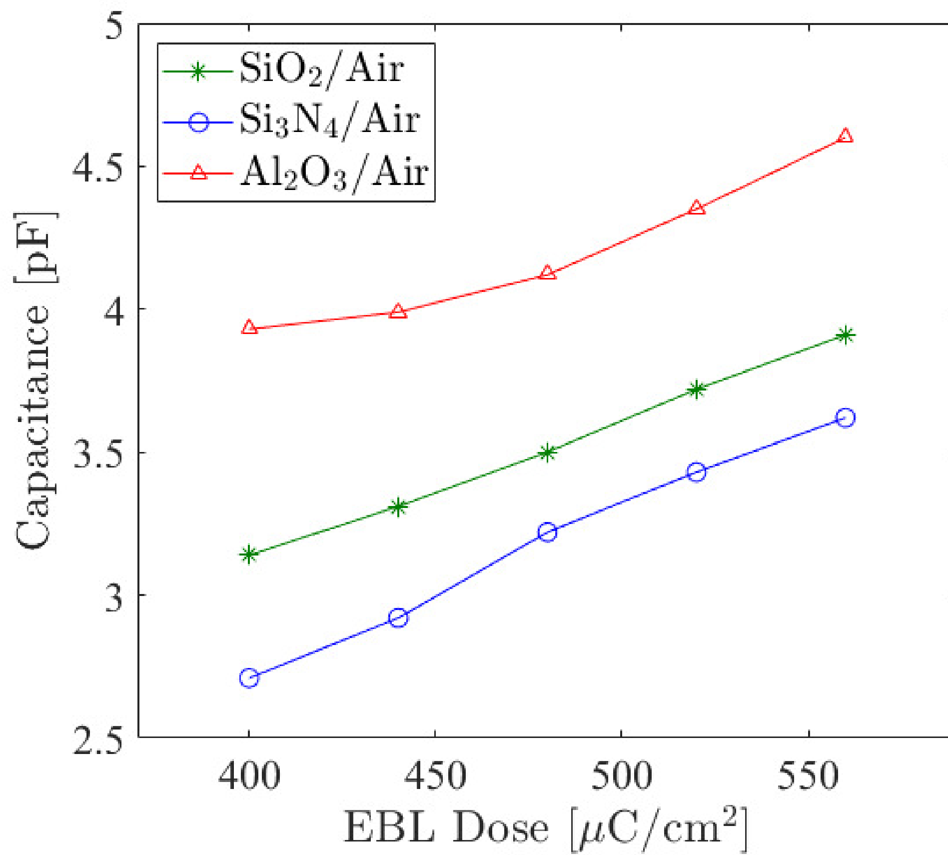


Figure 2.6: Plot of the measured capacitance of the three IDE test structures measured at f = 1 kHz at standard room temperature. The trend shows a rise in capacitance values as the EBL dose increases for all the devices.

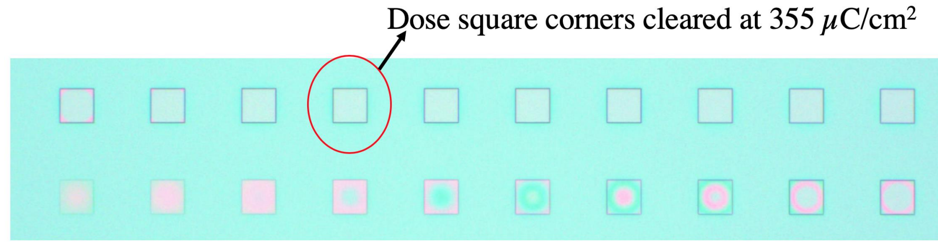


Figure 2.7: The optical microscopy image of 20 reference EBL dose squares with doses ranging between 150-449 μC/cm^2. For this post development particular inspection, the remnant PMMA were fully cleared at dose = 355 μC/cm^2.

capacitance values are not due to enhanced finger yield or some other unknown variation due to electron beam radiation, the devices are systematically inspected visually using as shown in SEM Figure 2.5 and verified to have high finger yield and spacing regularly.

2.4.2 Fabrication Model Validation

To overcome these pattern imperfections and to enhance the resolution pattern, proximity effect correction (PEC) must be used during the exposure process. Further, the exposure dose and develop time must be optimized to achieve a consistent pattern result. Using a variety of doses, the patterns are developed in several steps and the develop time is determined using a set of twenty reference dose squares. As shown in Figure 2.7, these dose squares are visually inspected to check if they are completely clear of any remaining photoresist. Figure 2.8 shows a plot of the applied EBL dose for the dose squares against the remaining photoresist thickness for an optimized sample. Once the final development has been optically inspected, the thickness of the photoresist inside each dose square is measured using a profilometer, and further developed until the reference dose feature is fully clear, which is an indication that the patterns are ready for metal evaporation. In these experiments, a final EBL base dose of 400 μC/cm^2 is used to expose all subsequent structures presented in this research because it was found that this dose produces a minimum in all geometric variations.

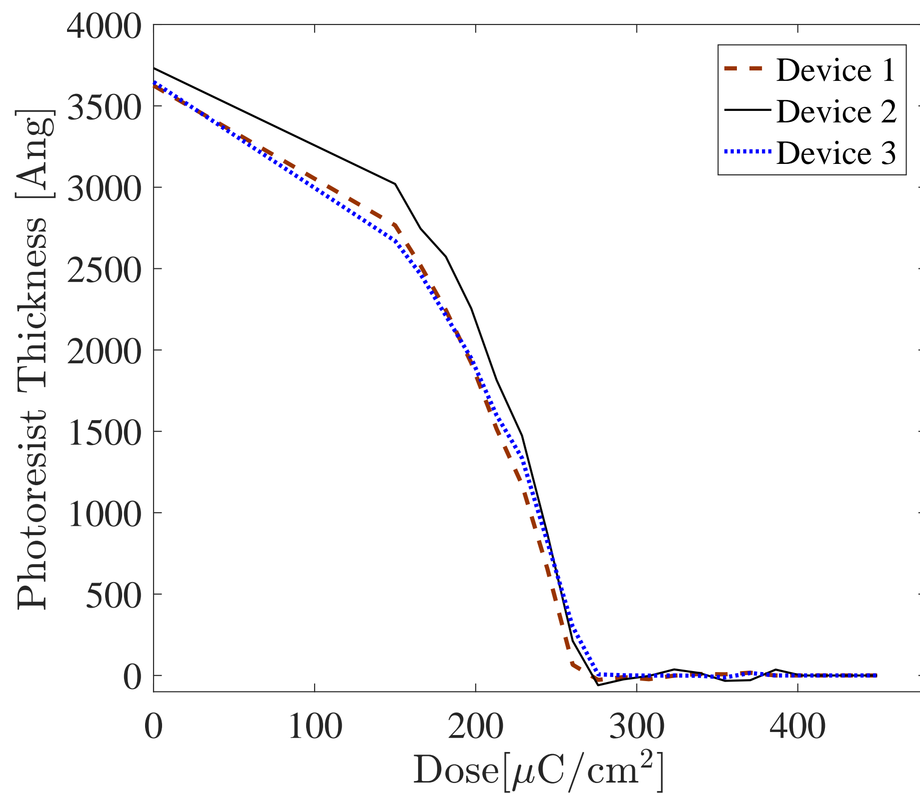


Figure 2.8: Plot of experimental EBL exposure dose versus remaining PMMA photoresist thickness on reference dose squares.

Once all possible fabrication efforts have been made to minimize the variations of the present experiments, it is important to provide a statistical uncertainty analysis to examine the statistical convergence of the collected measurement data. Assuming that μ is a true mean of electrical measurement data, equation (2.1) can be used to find the sample size n required to be 100($1-\alpha$)% confident that the error in estimating μ is less than a desired error percentage E_{er} (Montgomery and Runger, 2010; Mohaghar, 2019), which is assumed to be at most 3% in these experiments with specific levels of confidence for each experiment:

$$n = (\frac{100 \times \sigma z_{\alpha/2}}{E_{er}\mu})^2, \tag{2.1}$$

where $(1 - \alpha)$ is the confidence coefficient, $z_{\alpha/2}$ is the upper $100\alpha/2$ percentage point of the standard normal distribution and σ is the standard deviation (Montgomery and Runger, 2010; Mohaghar, 2019).

Figure 2.9 shows the convergence of ensemble average capacitance for each of the three aforementioned structures. Based on these results, it can be said with 99.5% confidence that the mean of statistics for the measurement data for Structure 1 (SiO_2/air) will not exceed 1.5% of total ensemble average capacitance when the sample size is around 74. For Structure 2 (Si_3N_4/air), it can be said with 99.5% confidence that μ for the measurement data will not exceed 1% of total ensemble average capacitance when the sample size is around 72, and for Structure 3 (Al_2O_3/air), μ for the measurement data will not exceed 3% of total ensemble average capacitance with 99.5% confidence when the sample size is around 85. This shows very promising results in the repeatability and reliability of the fabrication process across the samples for the three structure types.

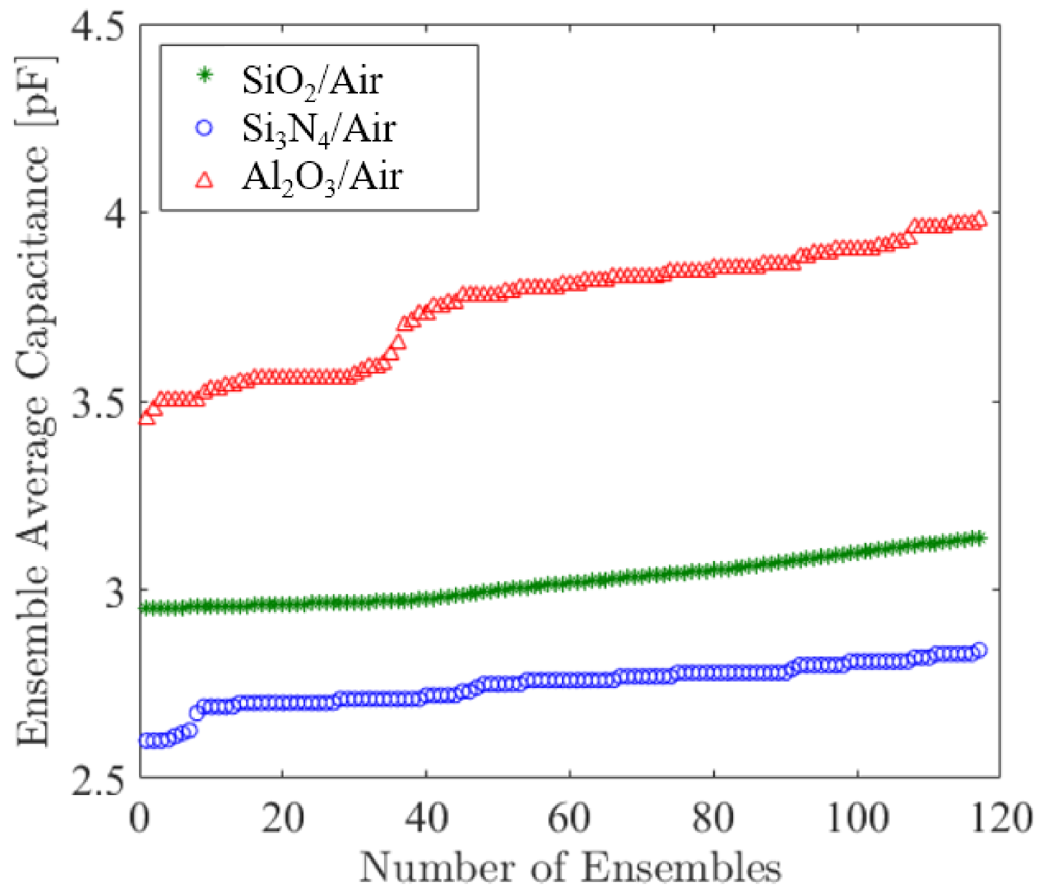


Figure 2.9: Convergence in the ensemble average capacitance of the three IDE structure types (Si_3N_4/air, Si_3N_4/air, and Al_2O_3/air) versus the number of data ensembles.

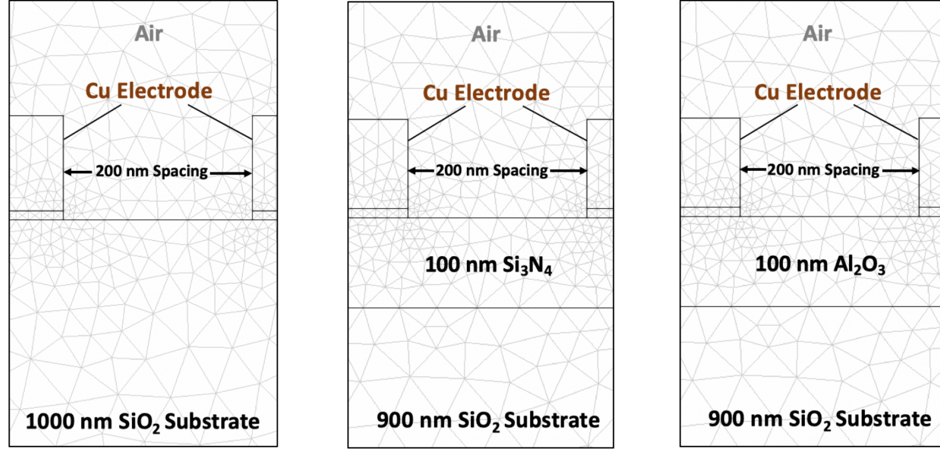


Figure 2.10: A zoomed COMSOL Multiphysics® screen capture of (a) a SiO_2/air device with refined triangular mesh used to estimate electric energy density; (b) a Si_3N_4/air device; and (c) an Al_2O_3/air device.

2.5 FEM Modelling and Simulation of IDE Structures

2.5.1 Test Structure FEM Simulation

To further validate the interfacial polarization effects evident in experimental measurements, three, two-dimensional optimized FEM models are built in COMSOL Multiphysics® to calculate the electrical energy density in an isotropic media with a fine triangular mesh and Dirichlet boundary conditions at each electrode. The models in Figure 2.10 depict nominal structures where three electrodes (100 nm of Cu on top of 10 nm of Cr) with 200 nm spacing are placed on top of different combinations of Si_3N_4, SiO_2 and Al_2O_3 layers, where the bulk permittivities of the SiO_2, Si_3N_4 and Al_2O_3 dielectric layers are determined from direct measurements using previous parallel plate experiments to k_{SiO_2} = 4.3, $k_{Si_3N_4}$ = 6.6 and $k_{Al_2O_3}$ = 9.9, respectively as explained in Section 2.3. Once the electric fields are calculated in each region, a subdomain integration of electrical energy density is carried out over the entire simulation window.

The energy stored in the electric fields is then used to calculate the total mutual capacitance of the 1000-fingered IDE capacitor. Once the overhead capacitance is also extracted from the simulation models for the three structure types as shown later in Section 2.5.3, the

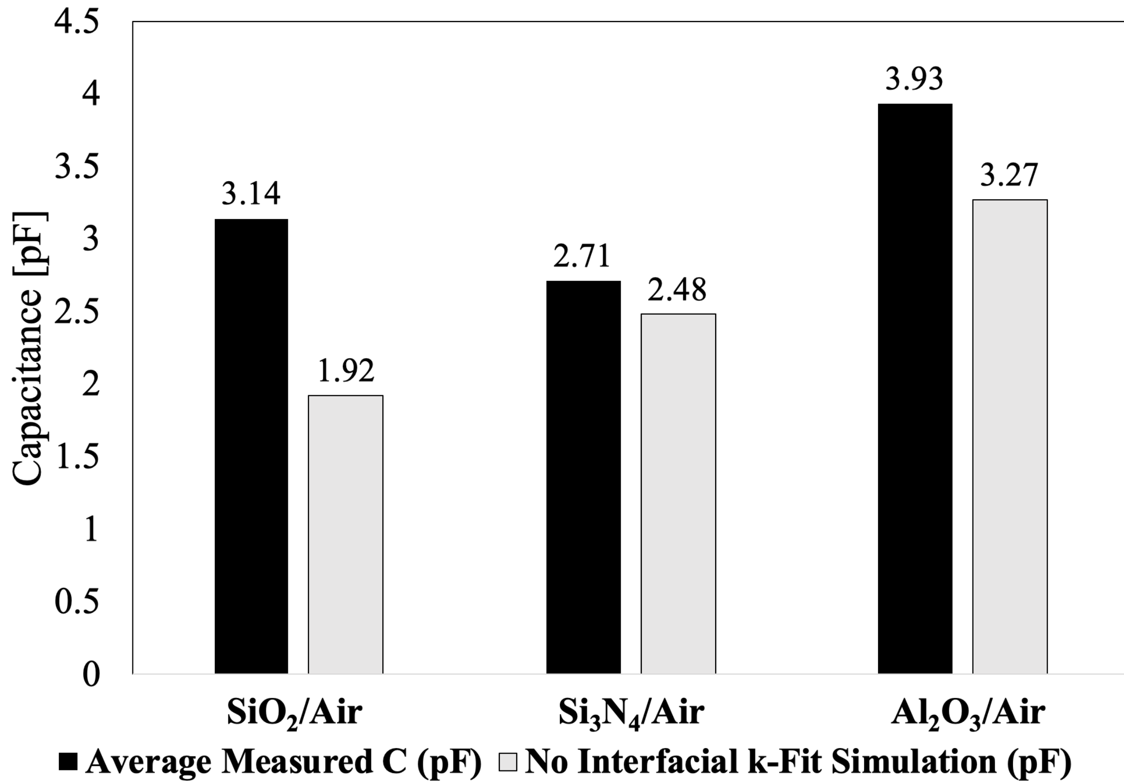


Figure 2.11: Bar graph of the average measured capacitance of SiO_2/air, Si_3N_4/air, and Al_2O_3/air test devices measured at f = 1 kHz at standard room temperature as well as the FEM simulation of each test structure ignoring interfacial effects.

total capacitance values are plotted as shown in Figure 2.11.

2.5.2 Simulation Sources of Error

This section of Chapter 2 presents a general framework for the sources of variation and error in two-dimensional quasi-electrostatic alternating current (AC) FEM COMSOL Multiphysics® simulation models of the proposed multi-interface structures. FEM is a numerical method for obtaining solutions to boundary-value problems with a finite degree of freedom (Jin, 2015). In this method, a complex system governed by Laplace's equations is partitioned into smaller elements and nodes so that the associated continuous second order partial differential equations can be solved using a finite set of linear equations.

Similar to other numerical analysis methods, FEM is subject to different types of errors

including geometric and boundary modelling error, discretization error and numerical error (Shah, 2002). Modeling error can include oversimplifying assumptions in mathematical and electromagnetic models and overall poor geometry of the modelled system. Numerical errors are mainly due to round off error caused by the limited number of significant digits allowed by the simulation device.

Discretization error, on the other hand, is due to mesh density choices and, also, window sizes for the simulation model. Since the dielectric layers in the three structure types are grown using conformal PECVD (without breaking vacuum) and e-beam evaporation, the metallic electrodes are evaporated using high-precision e-beam evaporation, and optical inspection and STEM characterization show high uniformity of the nanolaminate layers, it is thus assumed that the real world nanolithographic geometric structure has been properly approximated using detailed quasi-electrostatic FEM models. Convergence issues related to window size and mesh density are shown in Table 2.3 for the Si_3N_4/air structure as an example and illustrated in Figure 2.12. It is shown that a small window size with a default mesh density in Figure 2.12 (a) is sufficient to characterize the capacitance per unit length for the capacitive fingers in the IDE structure as it includes almost all the effects of the fringing electric fields in the FEM simulations. The axial uniformity of the electrode-fingers enables a two-dimensional simulation model to be effective; however, the points of discontinuity in the test structure can introduce small perturbative variations in the estimation of the overall capacitance.

2.5.3 Floating Circuit Model and Overhead Validation

To further validate the capacitance estimation of the fabricated test structures and FEM simulation models, the overhead capacitance values which comprise the sum of the capacitances of the two metallic pads, the top and bottom rails, and the non-mutual parts of the IDE fingers as illustrated in Figure 2.13 are measured experimentally and then extracted from FEM simulations for each of the three structure types. Using an equivalent circuit

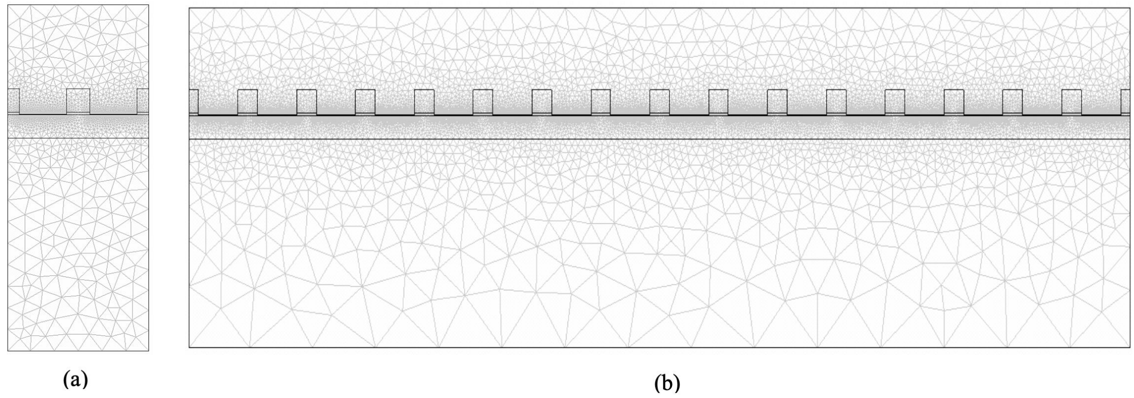


Figure 2.12: The COMSOL Multiphysics® screen capture of a (a) Si_3N_4/air capacitive device with two Cu electrodes with refined triangular mesh used to estimate electric energy density; and (b) a screen capture of the same device structure with refined triangular mesh showing sixteen Cu electrodes.

Table 2.3: Convergence and error analysis of FEM models for the Si_3N_4/air structure.

Number of Mesh Elements	**Total Device Capacitance [pF]**	**Error to Previous Run**
10517	2.8056504	-
42068	2.8014712	0.15%
168272	2.8014712	0%
Vertical "Air Box" Height		
2× Increase	2.8126728	-
4× Increase	2.8171512	0.16%
50× Increase	2.8171512	0%
Number of Capacitor Fingers		
2	2.8014712	-
4	2.8014712	0%
16	2.8014712	0%

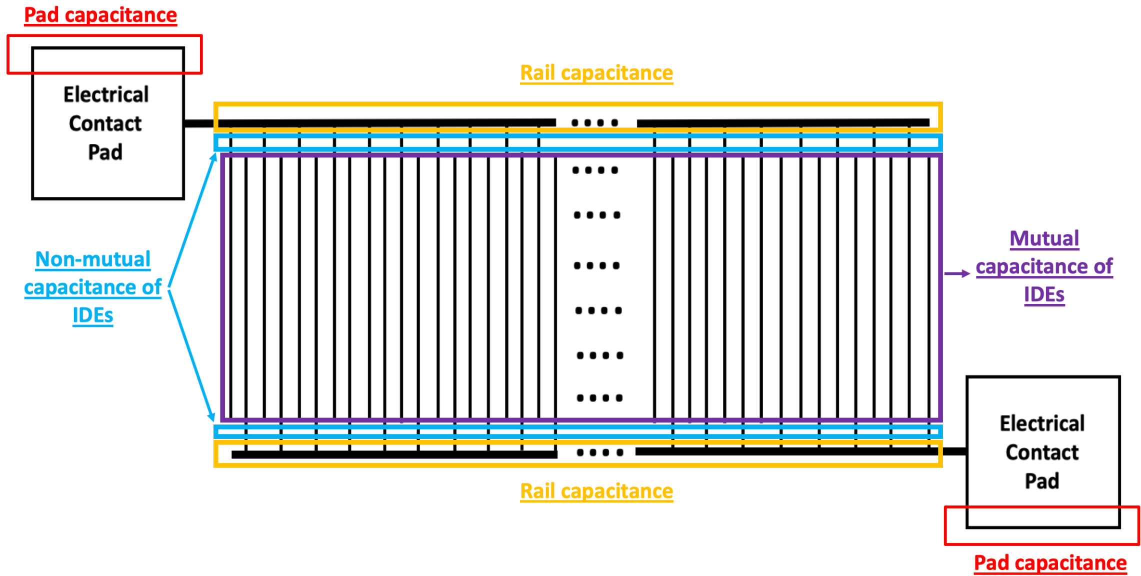


Figure 2.13: Top view schematic of the overhead capacitance components in the IDEs for the three SiO_2/air, Si_3N_4/air, and Al_2O_3/air structure types.

model as illustrated in Figure 2.14, capacitances are extracted from the simulation model with a floating substrate, which assumes that there is no depletion region in the substrate. In Figure 2.14, C_{pad1} and C_{pad2} are the capacitances for each of the pads, C_{rail1} and C_{rail2} are the rail capacitance for the top and bottom rail, and $C_{non-mut}$ is the capacitance for the non-mutual segments of the comb fingers, respectively.

The pads and total overhead capacitances for all test structures are shown in Table 2.4. As it can be seen in Table 2.3, there is a strong agreement between the pads and overhead

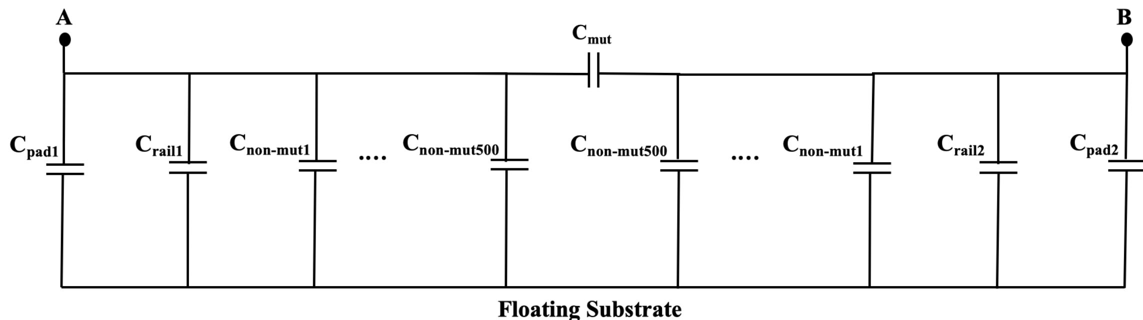


Figure 2.14: The equivalent lumped circuit model including the overhead capacitance and mutual capacitance between the IDEs for the three SiO_2/air, Si_3N_4/air, and Al_2O_3/air structure types.

Table 2.4: A comparison between the average measured capacitance and simulation values for the three SiO_2/air, Si_3N_4/air, and Al_2O_3/air IDE structure types. PC represents isolated Pad Capacitance and OC represents the overall Overhead Capacitance.

		PC (pF)	**% Error**	**OC (pF)**	**% Error**
Structure 1 SiO_2/Air	**Measurement**	0.109	-	0.158	-
	Simulation	0.108	0.917%	0.158	0%
Structure 2 Si_3N_4/Air	**Measurement**	0.115	-	0.154	-
	Simulation	0.112	2.609%	0.150	2.597%
Structure 3 Al_2O_3/Air	**Measurement**	0.118	-	0.162	-
	Simulation	0.117	0.847%	0.159	1.85%

capacitance values for the experiment and FEM simulations, which shows that the absence of a depletion region is an accurate assumption for the FEM models.

2.5.4 Simulation Model Validation of Test Structures

Table 2.4 illustrates that FEM simulation can predict the measurements of various elements of the test structure within 0%-3% error. However, for the parts of the test structure that include significant interfacial components as shown in Figure 2.15, the mismatch between the simulation and the measurements can vary significantly depending on the material composition of the interfaces from 8%-39%.

It is the hypothesis of this work that ignoring the impact of interfacial effects and dipole formation at the interface of SiO_2/air significantly underestimates the measured capacitance of the devices. In fact, as shown in the bar graph in Figure 2.11, there is a 38.8% deviation between the measured average capacitance values for the SiO_2/air structure and the simulations results that ignore the impact of interfacial dipoles. The implication of this and the experimental evidence in Tepper and Berger (1999) addressing the anomalous increase in permittivity at the interfaces of SiO_2 nanocompacts is that the high polarizability of the SiO_2/air interface is drastically impacting the overall permittivity of the devices fabricated for Structure 1. Similarly, there is a 8.49% deviation, and a 16.8% deviation between the average capacitance values and the simulation results for Structure 2 (Si_3N_4/air) and Struc-

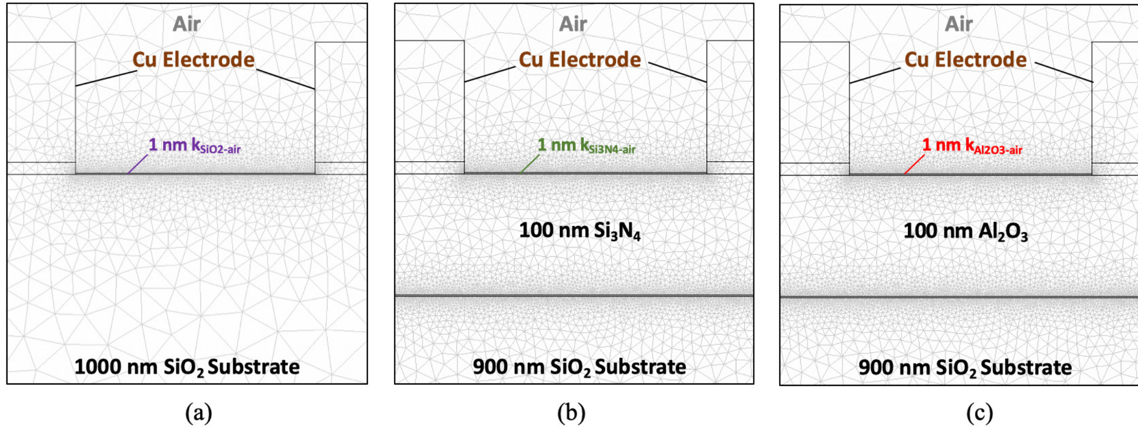


Figure 2.15: The COMSOL Multiphysics® screen capture of the three test structures showing interfacial effects for (a) SiO_2/air interface, (b) Si_3N_4/air interface, and (c) Al_2O_3/air interface.

ture 3 (Al_2O_3/air), respectively.

Hence, to be consistent with the high polarizability of SiO_2, Si_3N_4 and Al_2O_3 compact surfaces, based on the observations, measurements and the nanopowder and nanostructure dipole formation and the interfacial effect explanations in Mo, Zhang, and Wang (1995), Tepper and Berger (1999), Gritsenko (2009), Giustino, Umari, and Pasquarello (2003), Giustino and Pasquarello (2005), and Jameson *et al.* (2006), a new simulation model is suggested in this research which includes interfacial effects that are modeled as regions with extracted permittivities between SiO_2/air, Si_3N_4/air, and Al_2O_3/air layers that is approximately 1 nm thick in all the models as shown in Figure 2.15.

In this set of FEM simulations, using the approximated 1 nm SiO_2/air interface and other FEM model assumptions, the electric energy density per unit length U_L, is obtained from the COMSOL Multiphysics® simulations. Following this, the total capacitance of the device for Structure 1 is calculated using:

$$C = (\frac{2N_{MutualFingers}U_L L_{Mutual}}{V^2}), \tag{2.2}$$

where C is the total capacitance of the mutual part of the electrode-fingers, $N_{MutualFingers} = 500$, U_L is the electric energy density per unit length per electrode-finger pair that is calcu-

lated from simulation, $L_{Mutual} = 80 \times 10^{-6}$ m is the mutual length of the IDEs, and V is the applied voltage at 1 V. The measured total capacitance value, which is comprised of the sum of the capacitance of the mutual part of the IDEs (electrode-fingers) and the overhead capacitance, is then directly compared to the COMSOL Multiphysics® simulation. In the COMSOL Multiphysics® simulation, all the geometric parameters and all but one of the material parameters is known for the simulation. The only parameter for Structure 1 that is not in this measurement/simulation comparison is the value of $k_{SiO_2/Air}$. This value is varied in the simulation until it produces a calculated simulated result that exactly matches the average measurements made for the SiO_2/air interface for Structure 1 devices.

Using the same methodology, $k_{Si_3N_4/Air}$ is extracted from the average measurements for the Si_3N_4/air interface for Structure 2 devices. Similarly, $k_{Al_2O_3/Air}$ is extracted for the Al_2O_3/air interface for Structure 3. Specifically, the interfacial permittivity values of $\mathbf{k}_{SiO_2/Air} \sim 323$, $\mathbf{k}_{Si_3N_4/Air} \sim 58$, and $\mathbf{k}_{Al_2O_3/Air} \sim 160$ are extracted to match the average capacitance measurements for the SiO_2/air, Si_3N_4/air, and Al_2O_3/air, respectively. It should be noted that there was minimal frequency dependence observed across the samples for the three structure types as seen in Figure 2.16.

2.6 Results and Discussions

For the fabricated structures in these experiments, the capacitance and conductance are measured over a range of frequencies (10 Hz - 100 kHz) using an HP4284A LCR 4-point probe meter under ambient conditions at standard room temperature (25 °C). Figure 2.17 shows the relative frequency histogram of capacitance measured for 117 sample devices for Structure 1 (SiO_2/air), 181 sample devices for Structure 2 (Si_3N_4/air), and 149 sample devices for Structure 3 (Al_2O_3/air) at f = 1 kHz with an AC amplitude of 1 V with zero offset bias. A thorough visual inspection and SEM characterization of these devices as well as the aforementioned convergence and error analysis shows an almost 100% yield of devices, which means that there are no broken IDEs, PMMA residue or other miscellaneous

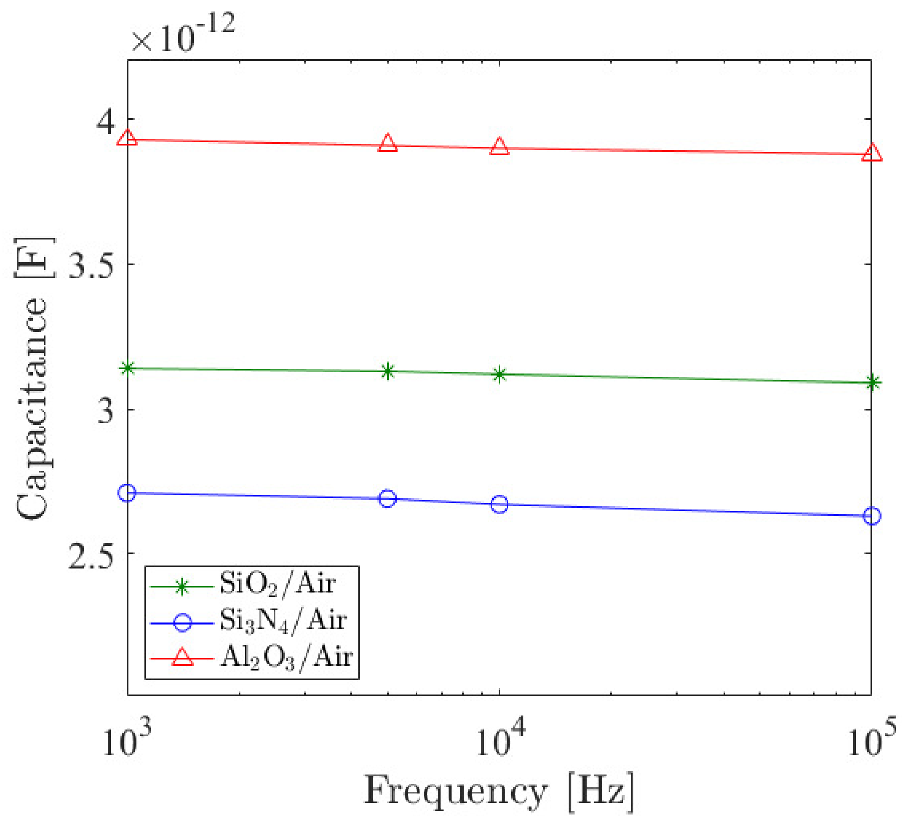


Figure 2.16: Plot of the frequency dependence of capacitance across the three SiO_2/air, Si_3N_4/air, and Al_2O_3/air IDE structure types.

damage such that there are no outliers in the data as illustrated in Figure 2.17.

Further, the intensity of the electric field, E, for the SiO_2/air structure type is illustrated in Figure 2.18 in a color map as well as the gradient of the electric field as a function of a particular vertical path in this structure. As for electric measurements, the electric field E between electrodes for all the three IDE SiO_2/air, Si_3N_4/air, and Al_2O_3/air structure should be approximately:

$$E \approx V/d \approx 1/(2 \times 10^{-5}) = 5 \times 10^4 V/cm, \tag{2.3}$$

where V is the maximum applied voltage, which is 1 V, and d is the distance between the comb capacitor electrodes, which is 200 nm. As it can be seen in Figure 2.18, the electric field along this path increases and reaches a value of 4.5×10^4 V/cm in between the middle of the two electrodes, and decreases down to zero as one moves deeper into the substrate, which is the same for all three IDE structure types.

It is postulated in this work that the dipoles formed by oxygen surface vacancies may be the cause of significant increase in permittivity values at the SiO_2/air regions as was also noted by researchers in Tepper and Berger (1999). Specifically, the researchers in Tepper and Berger (1999) reported that the anomalous increase in the permittivity at the SiO_2 amorphous nanopowder particles is due to the high density of dangling bonds at the surface of the particles, and showed that this permittivity drops drastically by annealing the SiO_2 particles using heat treatment at temperatures up to 600 °C due to the destruction of the Si dangling bonds. Similarly, the authors in Mo, Zhang, and Wang (1995) explain that the many oxygen ion vacancies in Al_2O_3 and the abundance of oxygen and nitrogen ion vacancies in Si_3N_4 nanostructures give rise to strong dipole moments which in turn lead to a very strong rotation direction polarization, hence, much higher permittivity at the nanoparticle air interfaces.

In this research, our primary goal is to develop an equivalent interfacial material model that can be used to predict capacitance and conductance values for devices that have these

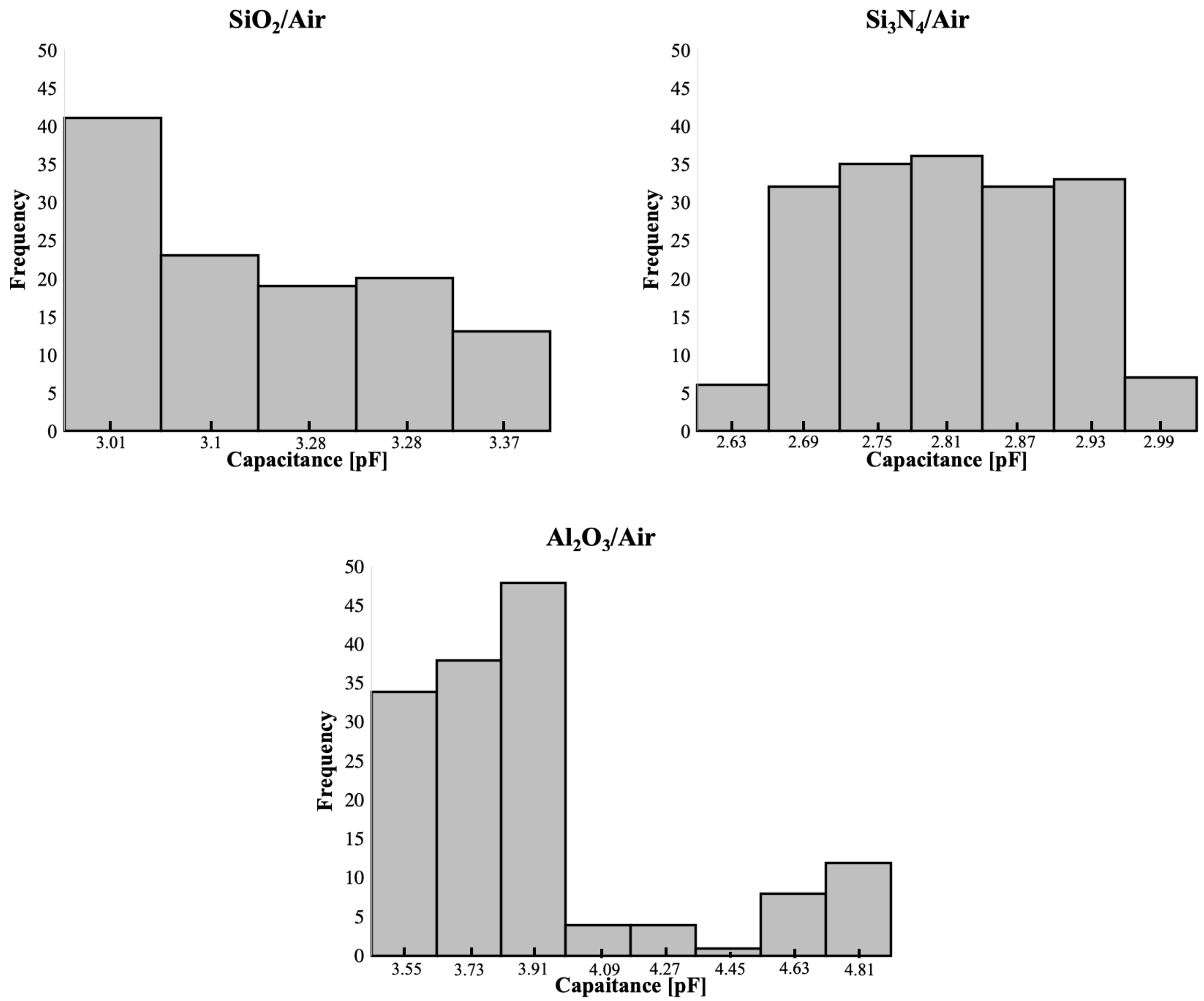


Figure 2.17: Bar graphs of the relative frequency of capacitances measured for all the sample devices fabricated for the three IDE SiO_2/air, Si_3N_4/air, and Al_2O_3/air structure types.

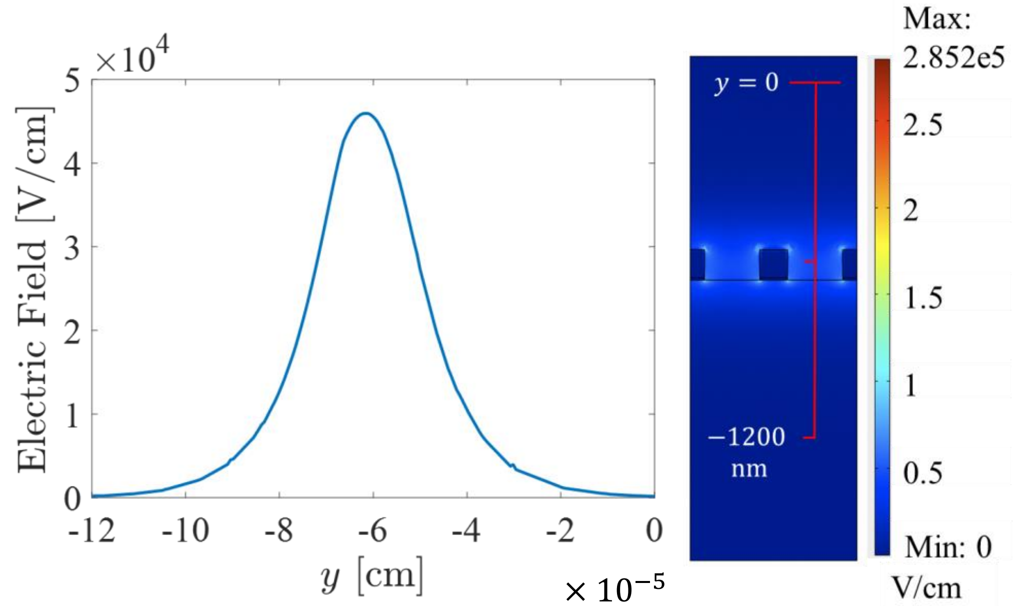


Figure 2.18: Plot of the electric field intensity profile as a function of a particular vertical path shown by the above red line for the SiO_2/air structure.

particular interfacial regions. It is our argument that a model with a smaller geometric thickness would have a larger permittivity value to account for the electrical impact of the interface on a macroscopic scale. Therefore, if we were to use a different thickness other than 1 nm, then it is the assumption of this work that the equivalent interfacial material model would have a different value for the empirically extracted permittivity in simulation; however, this different thickness-permittivity combination would still predict the overall device characteristics.

As with many empirically based models, care must be taken to not overly interpret the values that are extracted in the model, but we do put forth that this model does represent the average polarizability of the molecules in the ~ 1 nm thick region. Furthermore, making sure that the material relaxes back to its bulk state within 1 nm, which is indicated in the aforementioned references, is an important aspect as to its efficacy such that the region in the model localizes where the anomalous molecular behavior resides in the material. It should be said with emphasis that for this research, the thickness of the interfacial layer of 1

nm is consistently used throughout the entire work which allows for consistent comparisons between different interfaces that are characterized in this chapter and later chapters.

The permittivity modelling at these interfaces has important implications for solid-state energy storage capacitors, advanced sensor design, and solid-state memory devices. This part of the research illustrates a new methodology for characterizing the average polarizability of various molecular topologies that are present at the interfaces between materials that are created with specific growth mechanism.

In addition, this methodology could result in expedited investigation of a wide range of material interface combinations without the time and resource limitations of quantum modeling and detailed surface spectroscopy. For devices that need to take advantage of molecular polarization at material interfaces, this new methodology provides macroscopic and repeatable results that can be used to create accurate electromagnetic and circuit models for exploratory device design. In the next chapter,the results and modelling methodology from this chapter will be used to analyze the average interfacial properties between SiO_2, Si_3N_4, and Al_2O_3 dielectric stacks.

CHAPTER 3

FABRICATION, MODELLING AND SIMULATION OF ENCAPSULATED SIO_2, SI_3N_4 AND AL_2O_3 IDE STRUCTURES

3.1 Introduction

In Chapter 2, it was shown using FEM simulations that ignoring the impact of strong dipole formation at SiO_2/air, Si_3N_4/air and Al_2O_3/air interfaces consistently underestimates the overall capacitance of these IDE capacitors. This result proved that there is great potential in characterizing the anomalous surface properties of these dielectric materials. In this chapter, it is demonstrated that dielectric/dielectric interfaces of these dielectric materials (e.g. SiO_2, Si_3N_4, and Al_2O_3) potentially have an anomalous interfacial polarizability component that is tangential to the interfaces, which has not been extensively studied.

To explore this component, extensive experimental measurements of the capacitances of IDE devices are used to excite heterogenous dielectric interfaces with electric fields that are parallel to the planes of those interfaces. Unlike the experimental results shown in literature for PPE devices where the electric field is perpendicular to interfacial planes (Conde *et al.*, 2012; Campabadal *et al.*, 2011; Yota, 2011; Huebner *et al.*, 1999), the electric fields in the proposed nanolaminate IDE structures in this chapter excite a parallel component of permittivity. Although there are a significant number of experiments that study laminates in PPE configurations, there are no rigorous experiments in the literature with nanolaminates of SiO_2, Si_3N_4, and Al_2O_3 materials in the proposed IDE configuration that enables the study of the parallel component of the permittivity of the interfaces between the dielectrics.

In this chapter, it is firstly shown that IDE capacitors that are encapsulated with SiO_2, Si_3N_4, or Al_2O_3 that have no heterogeneous interfaces in the vicinity of electrodes can be modeled precisely (less than 1% error) using FEM simulation without any fitting pa-

rameters. Following the homogeneous IDE structure results, this validated measurement technique is applied to estimate the average polarizability, in the form of an effective permittivity value, in a sufficiently small volume encompassing the dielectric interfaces of Si_3N_4/SiO_2, Al_2O_3/SiO_2, and Al_2O_3/Si_3N_4 in 200 nm-spacing IDE structures. Using this new extraction technique for a given set of dielectric growth methods, it is shown through a set of statistically significant set of experiments, the existence of a large component of polarizability that is parallel to the interfacial plane between Si_3N_4/SiO_2 ($k_{Si_3N_4/SiO_2}$ = 1419), Al_2O_3/SiO_2 ($k_{Al_2O_3/SiO_2}$ = 2373), and Al_2O_3/Si_3N_4 ($k_{Al_2O_3/Si_3N_4}$ = 428). Additionally, this chapter will provide documentation of stress-induced device failures with certain IDE structure architectures fabricated using different combinations of SiO_2, Si_3N_4 and Al_2O_3 dielectric materials. Lastly, the final portion of this chapter will expand on the significance of this polarization and how it affects interfacial permittivity in both IDE and PPE devices.

3.2 Model Validation of Homogeneously Encapsulated IDEs

To further validate the two-dimensional quasi-electrostatic modelling and simulations of the interfacial polarization effects evident in experimental measurements from Chapter 2, the same FEM models are built and simulated for homogeneously encapsulated structures in this chapter. Specifically, the proposed simulation model is tested to illustrate that it is possible to accurately predict the capacitance of SiO_2/SiO_2, Si_3N_4/Si_3N_4 and Al_2O_3/Al_2O_3 structures that do not have heterogeneous dielectric interfaces between the electrodes as shown in Figure 3.1. The dielectric/air interfacial permittivities at the very top of these structures are kept the same values as extracted in Chapter 2 namely, $k_{SiO_2/Air} \sim 323$, $k_{Si_3N_4/Air} \sim 58$, and $k_{Al_2O_3/Air} \sim 160$. The bulk permittivities of these dielectric materials are maintained at k_{SiO_2} = 4.3, $k_{Si_3N_4}$ = 6.6, and $k_{Al_2O_3}$ = 9.9, respectively. Here, three 2-D FEM models are built in COMSOL Multiphysics® to calculate the overall energy density per unit length as shown in Figure 3.1. The energy stored in the electric fields is then used to calculate the total mutual capacitance of the 1000-fingered IDE capacitors for the

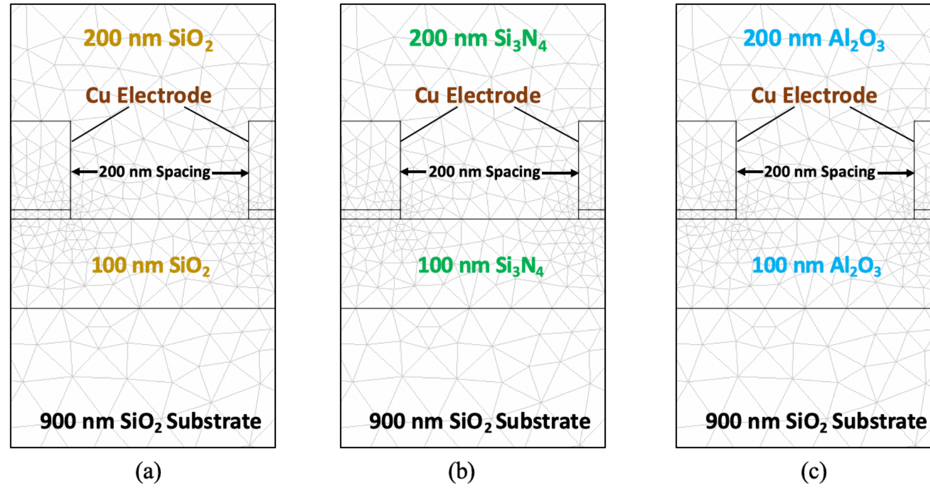


Figure 3.1: Schematic of the zoomed COMSOL Multiphysics® screen captures with refined triangular mesh used to estimate electric energy density for (a) a SiO_2/SiO_2, (b) a Si_3N_4/Si_3N_4, and (c) an Al_2O_3/Al_2O_3 homogeneous IDE device.

SiO_2/SiO_2, Si_3N_4/Si_3N_4 and Al_2O_3/Al_2O_3 structures. The bar graphs plotted in Figure 3.2 illustrate that the average measured capacitances over a set of approximately 105 samples of the three encapsulated structures depicted in Figure 3.1 match the FEM simulation of those encapsulated structures with no interfacial effects included in the FEM model. This is a pivotal step in the validation of the FEM models that shows that the interfaces of SiO_2/SiO_2, Si_3N_4/Si_3N_4 and Al_2O_3/Al_2O_3 dielectric layers, which are believed have no or negligible anomalies, can be accurately modelled and characterized without using an interfacial layer model between the dielectric/dielectric layers in the simulations models. In other words, there are no fitting parameters in these models that predict the capacitance of these structures with an error of less than 1%.

3.3 Heterogeneously Encapsulated IDEs

To capitalize on the dielectric/air interface anomalies of SiO_2/air, Si_3N_4/air and Al_2O_3/air structures from Chapter 2 and the aforementioned absence of anomalies at the interfaces of SiO_2/SiO_2, Si_3N_4/Si_3N_4 and Al_2O_3/Al_2O_3 layers, we will proceed to study the interfacial polarization effects at the interface of different dielectric combinations of SiO_2, Si_3N_4 and

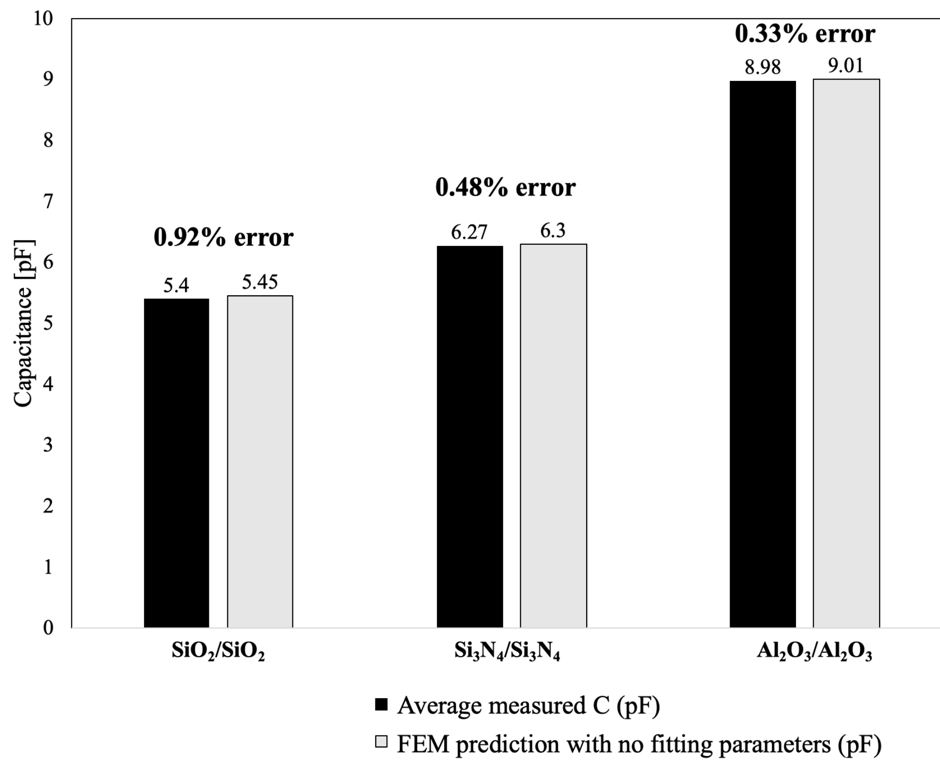


Figure 3.2: Bar graph of the average measured capacitance of SiO_2/SiO_2, Si_3N_4/Si_3N_4 and Al_2O_3/Al_2O_3 encapsulated test devices measured at f = 1 kHz at standard room temperature as well as the FEM simulation of each test structure ignoring interfacial effects.

Table 3.1: PECVD deposition of SiO_2 and Si_3N_4 and e-beam evaporation of Al_2O_3 dielectric layers and their respective encapsulations for the three IDE structure types.

Structure	**Preliminary Layers (100 nm)**	**Encapsulation Layers (200 nm)**
Type 1	Si_3N_4	SiO_2
Type 2	Al_2O_3	SiO_2
Type 3	Al_2O_3	Si_3N_4

Al_2O_3 materials.

3.3.1 Overview of the Fabrication Process

Three, lightly-doped p-type $< 100 >$ silicon wafers with resistivity of 8-12 Ω-cm are initially coated with 900 nm of SiO_2 using the Unaxis PECVD tool to improve isolation. Next, preliminary layers of SiO_2, Si_3N_4 (PECVD) and Al_2O_3 (e-beam) (each with a dielectric thickness of 100 nm), are deposited on top of the preliminary oxide layer. The 4" wafers are then cleaved into three, 1" samples, which are all spin coated and exposed using the EBL, where 1000 interleaved IDEs are fabricated on each sample. All the samples are then developed, inspected, metal evaporated, followed by the final lift-off and the cleaning procedure as explained in Chapter 2, Section 2.2.5 and 2.2.6.

Next, electrical measurements of capacitance and conductance are taken using the HP4284A LCR 4-point probe meter under ambient conditions at standard room temperature (25 °C). All the samples are then taken back to the cleanroom and are encapsulated with SiO_2, Si_3N_4 and Al_2O_3 layers (200 nm each) as shown in Table 3.1. It should be noted that all the preliminary layers listed in Table 3.1 are deposited on top of 900 nm of SiO_2 (isolation layer) as explained previously. Figure 3.3 shows a representation of the encapsulated structures.

3.3.2 FEM Modelling and Simulation

Three, two-dimensional FEM models are built in COMSOL Multiphysics® as shown in Figure 3.4 to calculate the electrical energy density in an isotropic media with a fine trian-

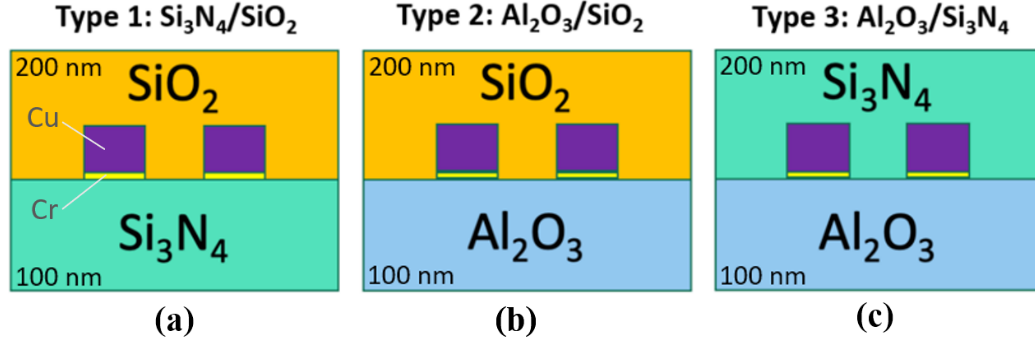


Figure 3.3: A (not-to-scale) schematic of structures where both (a) Type 1, with 100 nm of Si_3N_4, and (b) Type 2, with 100 nm of Al_2O_3, are encapsulated with 200 nm of SiO_2. In structure (c) Type 3, 100 nm of Al_2O_3 is encapsulated with 200 nm of Si_3N_4 (figures are not to scale).

gular mesh and Dirichlet boundary conditions at each electrode. The COMSOL models in Figure 3.4 show the zoomed version of the nominal structures where three electrodes (100 nm of Cu on top of 10 nm of Cr) with 200 nm spacing are placed on top of either SiO_2 or Si_3N_4 or Al_2O_3 dielectric layers. The permittivities of the dielectric/air layers at the top of the structures are set from the values extracted for SiO_2/air, Si_3N_4/air, and Al_2O_3/air interfaces to $k_{SiO_2/Air} \sim 323$, $k_{Si_3N_4/Air} \sim 58$, and $k_{Al_2O_3/Air} \sim 160$, respectively. Also, the bulk permittivity values of SiO_2, Si_3N_4 and Al_2O_3 layers are set from direct measurements in Section 2.3 of Chapter 2 to $k_{SiO_2} = 4.3$, $k_{Si_3N_4} = 6.6$, and $k_{Al_2O_3} = 9.9$, respectively.

Once the electric fields are calculated in each region, a subdomain integration of electrical energy density per unit length U_L, is carried out over the entire COMSOL Multiphysics® simulation window. Similar to Section 2.5.4 of Chapter 2, the total capacitance C for all the three structures is calculated. In the COMSOL Multiphysics® simulation of each structure type, all the material parameters are known for structure type 1-3 simulations, except for the dielectric/dielectric interfacial permittivity values of $k_{Si_3N_4/SiO_2}$, $k_{Al_2O_3/SiO_2}$, and $k_{Al_2O_3/Si_3N_4}$, respectively. These dielectric/dielectric interfacial values are varied in the simulation for each structure type until they produce calculated simulated results that exactly match the average measurements made for the Si_3N_4/SiO_2, Al_2O_3/SiO_2, and Al_2O_3/Si_3N_4 interfaces for structure type 1-3 devices. Table 3.2 shows the averaged measured capac-

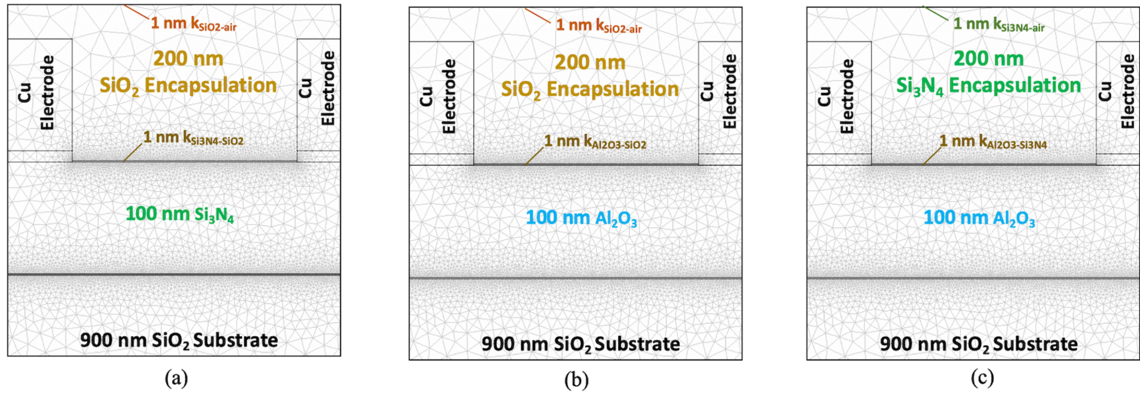


Figure 3.4: Simulation screen capture of the three heterogeneous IDE test structures showing interfacial effects for (a) Si_3N_4/SiO_2, (b) Al_2O_3/SiO_2, and (c) Al_2O_3/Si_3N_4 interfaces.

itances, the FEM simulation results without any interfacial layers, and the results from the simulation models that include the $\sim$ 1 nm interfacial layer as well as the extracted interfacial-k values for the three IDE structure types.

3.4 Data Analysis and Discussions

This section outlines and explains the findings and discussions regarding the interfacial k-fit simulations of the dielectric/dielectric structures including Si_3N_4/SiO_2, Al_2O_3/SiO_2, and Al_2O_3/Si_3N_4 nanolaminate devices compared to average measurement capacitance values for each structure type.

3.4.1 High Permittivity Devices

a. Experimental Observations of Interfacial Anomalies and Empirical Extraction of Interfacial Permittivity Values

In the nanolaminate structures that have been encapsulated with 200 nm of SiO_2, there is a significant increase in the average measured capacitance after encapsulation compared to FEM simulation with no model for interfacial polarizability enhancement values as it can be seen for Type 1 and Type 2 data in Table 3.2. For the Si_3N_4 sample encapsulated with 200 nm of SiO_2, for example, there is a $\sim 3.6\times$ increase in the average measured capacitance

Table 3.2: Pre-encapsulation and encapsulated average measured capacitance and FEM simulation results (with and without k-fit) of Si_3N_4/SiO_2, Al_2O_3/SiO_2, and Al_2O_3/Si_3N_4 structures.

		Averaged Measured Capacitance [pF]		No k-Fit Simulation [pF]		Interfactial k-Fit Simulation	
Structure	Bottom/Top	Pre-encapsulation	Encapsulated	Pre-encapsulation	Encapsulated (no k-Fit)	$k_{dielectric/air}$	$k_{dielectric/dielectric}$
Type 1	Si_3N_4/SiO_2	2.77	9.93	2.48	4.65	$k_{SiO_2/air} = 323$	$\mathbf{k_{Si_3N_4/SiO_2} = 1419}$
Type 2	Al_2O_3/SiO_2	3.9	14.2	3.27	6.33	$k_{SiO_2/air} = 323$	$\mathbf{k_{Al_2O_3/SiO_2} = 2373}$
Type 3	Al_2O_3/Si_3N_4	3.94	8.5	3.27	6.91	$k_{Si_3N_4/air} = 58$	$\mathbf{k_{Al_2O_3/Si_3N_4} = 428}$

compared to the FEM simulation of the Si_3N_4/SiO_2 structure, which only shows a $\sim 1.9\times$ enhancement as shown in Figure 3.5. Similarly, in the case of the Al_2O_3/SiO_2 structure, there is a also significant increase in the average measured capacitance of the devices ($\sim 3.6\times$) compared to the simulated value (only $\sim 1.9\times$) as illustrated in Figure 3.5.

The Al_2O_3/Si_3N_4 structure presents itself as a somewhat unique case among all the encapsulated devices since the encapsulation/pre-encapsulation capacitance ratios for both electrical measurement and FEM simulation seem to increase by the same amount ($\sim 2.1\times$) as shown in Figure 3.5. The disparity in the increases in capacitance before and after encapsulation for the averaged measurements compared to the FEM simulations shows that by simply relying on the bulk properties of the dielectric layers of the encapsulated structures and ignoring the interfacial effects at the interfaces consistently underestimates the actual capacitance of these devices.

Hence, whilst the permittivity of the SiO_2/air encapsulant layer is kept at a value of $k_{SiO_2/Air} \sim 323$ as obtained in Chapter 2, the interfacial permittivity of Si_3N_4/SiO_2 is extracted to be $k_{Si_3N_4/SiO_2} \sim 1419$ to match the average measurements for this structure as shown in Figure 3.6. Similarly, whilst the interfacial permittivity value of SiO_2/air is kept at $k_{SiO_2/Air} \sim 323$, the interfacial permittivity of the Al_2O_3/SiO_2 nanolaminate layer is extracted as a very large value, $k_{Al_2O_3/SiO_2} \sim 2373$ as seen in Figure 3.6. For the Al_2O_3/Si_3N_4 encapsulated structure, the permittivity k-fit at the interface of Al_2O_3/Si_3N_4 is extracted at $k_{Al_2O_3/Si_3N_4} \sim 428$, whilst the interfacial permittivity of Si_3N_4/air is kept at $k_{Si_3N_4/Air} \sim 58$ as extracted in Chapter 2.

It is postulated that there is strong adhesion between the underlying Si_3N_4 and Al_2O_3 layers and the 200 nm encapsulating SiO_2 layer in both Si_3N_4/SiO_2 and Al_2O_3/SiO_2 structures. This is due to the fact that SiO_2 has a lower coefficient of thermal expansion (CTE) than Si_3N_4 and Al_2O_3, respectively. CTE, which is represented by the symbol α_L, is defined as the tendency of the material to change its shape, size and volume in response to a change in temperature. Hence, since $\alpha_{SiO_2} < \alpha_{Si_3N_4}$, and Al_2O_3, $\alpha_{SiO_2} < \alpha_{Al_2O_3}$, as all

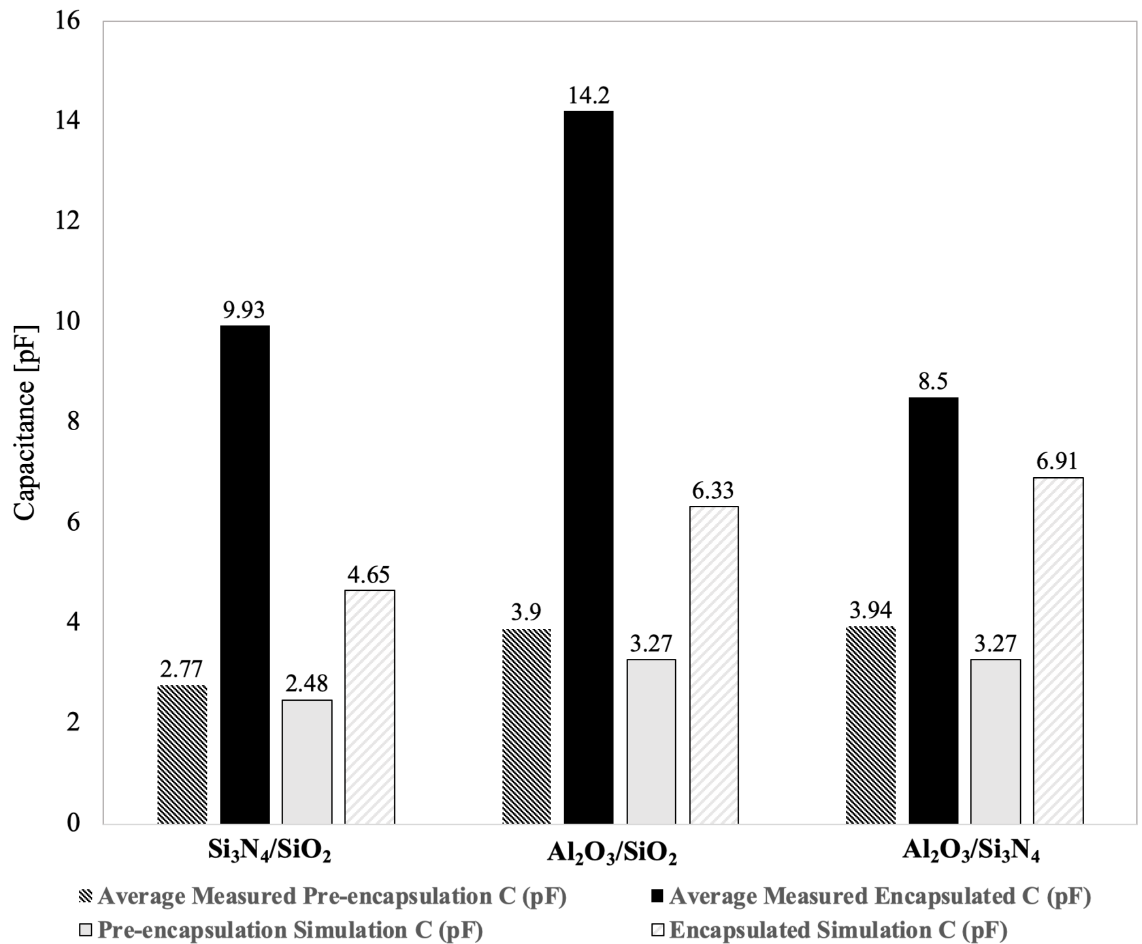


Figure 3.5: Bar graph of the average measured capacitance and the FEM simulations (ignoring interfacial effects) of Si_3N_4/SiO_2, Al_2O_3/SiO_2 and Al_2O_3/Si_3N_4 test devices before and after encapsulation.

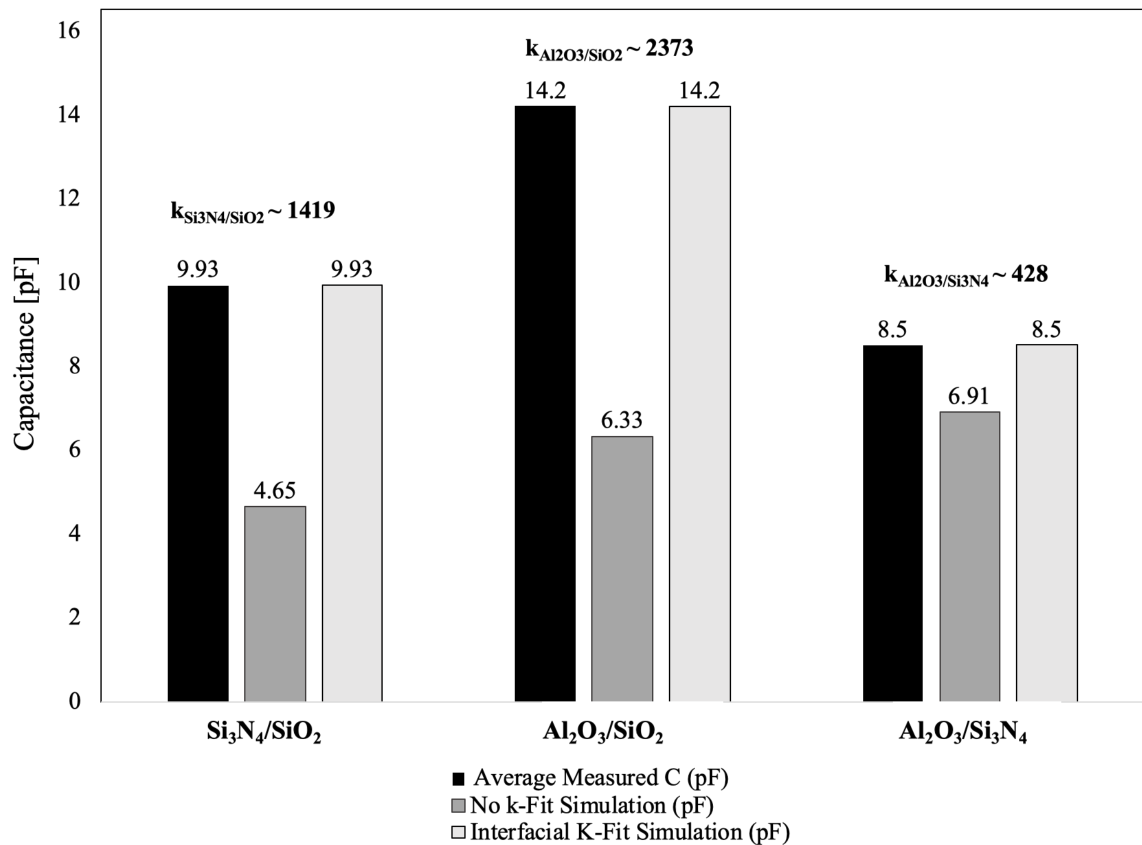


Figure 3.6: Bar graph of the average measured capacitance of Si_3N_4/SiO_2, Al_2O_3/SiO_2 and Al_2O_3/Si_3N_4 test devices measured at f = 1 kHz at standard room temperature as well as the FEM simulations of each test structure both ignoring and considering interfacial effects.

Table 3.3: CTEs of metals and dielectric materials used in this chapter.

Material	**CTE at 20 °C (per degree °C × 10^{-6})**
Cu	17
Cr	7.5
Si	2.6
SiO_2	0.24
Si_3N_4	3.3
Al_2O_3	8.1

the components in the structures including the metallic electrodes undergo multiples temperature changes, the SiO_2 encapsulant layer changes less considerably in shape, size and volume compared to the other parts of the structure, in particular the underlying dielectric layers, which implies that there is little to no delamination at the interface of Si_3N_4/SiO_2 and Al_2O_3/SiO_2 nanolaminate layers, respectively, therefore, resulting in a smoother dielectric interface. The values for CTEs of the materials used in this chapter are listed in Table 3.3.

As it was pointed out by Mo, Zhang, and Wang (1995), the high number of oxygen and nitrogen vacancies at the Si_3N_4 and the strong dipole moments at the interface of Al_2O_3 nanostructures leads to high rotational polarization, which in turn enhances the permittivity at the nanoparticle air interfaces for both materials. Here, since it is the hypothesis that there is good adhesion between the Si_3N_4/SiO_2 and Al_2O_3/SiO_2 layers as seen in Zou and Zhangn (2011), Kaiser *et al.* (1995), Sinha, Levinstein, and Smith (1978), and Xing *et al.* (2020), it is possible that the electric field is accentuated near the oxygen (for both encapsulated structures) and nitrogen vacancies (Si_3N_4/SiO_2 structure) at the interface of the dielectric layers.

It is postulated that similar to the two aforementioned encapsulated devices, for the Al_2O_3/Si_3N_4 device, there is good adhesion at the interface of Al_2O_3/Si_3N_4 layers, which is possibly due to the fact that $\alpha_{Si_3N_4} < \alpha_{Al_2O_3}$. In their work, Kaiser *et al.* (1994) used ultra-low Al_2O_3/SiO_2 dielectric multilayers (where the Al_2O_3 layers were e-beam evaporated) as the coating layer in excimer lasers and observed that both multilayer mean

background absorption and absorption at localized spikes were reduced drastically due to smooth Al_2O_3/SiO_2 interface. They further evaluated the multilayer dielectric interfacial properties using Atomic Force Microscopy, Photothermal Microscopy, absorption measurements and Spectroscopy of Sputtered Neutrals (Kaiser *et al.*, 1994).

Dameron *et al.* (2008) has reported that using a single Al_2O_3/SiO_2 bilayer in heat-stabilized polyethylene naphthalate polymer substrates reduces corrosion and system degradation substantially due to the strong and well-adhered Al_2O_3/SiO_2 interface. Further, they observed that the SiO_2 layer deposited on top of the Al_2O_3 layer successfully filled pinhole defects present at the surface of the Al_2O_3 layer. Further, researchers in Kumar *et al.* (2019) fabricated multilayer highly reflective mirrors consisting of fourteen alternate multilayers of Al_2O_3 and SiO_2 on a glass substrate and found the alternating Al_2O_3/SiO_2 films to have very good adhesion, low defect and excellent hardness. It was similarly shown in a paper by Sinha, Levinstein, and Smith (1978) that plastic flow and deformation characteristics of Al films were not significantly affected by the Si_3N_4 encapsulating films.

b. Tangential and Normal Permittivity Considerations

Polarization tensors of homogeneous crystalline materials at different crystal orientations have been extensively studied over the years (Ammari, Kang, and Lim, 2005; Kim, Kang, and Kim, 2003), but a study of this with composite materials can be a more difficult endeavor, especially excited at lower non-optical frequencies. In fact, capacitors constructed from heterogeneous laminate materials, whether it be a traditional planar laminate stack (Kamata and Kita, 2017; O'Brien, Baechle, and Wetze, 2011; Liu *et al.*, 2019) or even a folded laminate trench in a dynamic random-access memory (DRAM) (Rao *et al.*, 1986; Katsumata *et al.*, 2003), are essentially in a PPE configuration where the applied electric field vectors are orthogonal to the plane of the dielectric interfaces. Subsequently, the myriad of experimentations over the years with SiO_2, Si_3N_4, and/or Al_2O_3 laminates (Conde *et al.*, 2012; Campabadal *et al.*, 2011; Yota, 2011; Huebner *et al.*, 1999) are not appropriate to study the dipole polarizability of the interfacial regions from a direction that

is *parallel* to these interfaces, which is better suited with an IDE device.

The closest experiments that potentially reveal interfacial polarizability values in multiple directions for SiO_2, Si_3N_4, and/or Al_2O_3 come from NP composites materials where there are electric field directions that are in a variety of orientations relative to the NP/host dielectric interface; however, determination of exact linear properties is difficult in randomly mixed materials. Nonetheless, anomalously high effective permittivities of these nanopowder compacts have been measured and reported in the literature. For example, SiO_2, Si_3N_4 and Al_2O_3 nanopowder compacts have demonstrated enhanced permittivity that is roughly $10\times$ greater than bulk values at low frequencies due to polarizability of dipoles existing at the surfaces (Mo, Zhang, and Wang, 1995; Tepper and Berger, 1999; Zhang *et al.*, 1996).

As part of the validation of directional polarization in SiO_2, Si_3N_4 and Al_2O_3 material interfaces, three PPE structures with different bi-layer dielectric combinations between the electrodes are fabricated as shown in Fig. 3.7 using the methodology explained in Chapter 2. The first PPE test structure has 100 nm SiO_2 and 200 nm Si_3N_4 deposited using PECVD. The second PPE device has 100 nm of Al_2O_3 (evaporated using e-beam) and 200 nm of SiO_2, and the final structure contains 100 nm of Al_2O_3 and 200 nm of Si_3N_4 sandwiched between the Cr/Cu electrodes as illustrated in Fig. 3.7. The order of dielectric material deposition and evaporation in the PPE structures follow that of heterogeneous IDE devices previously shown in Table 3.1.

Similarly, 2-D FEM models of these PPE structure are simulated using the simulation tool once without a high-k interfacial layer and a second time with 1 nm high-k interfacial layers between each bi-layer. The interfacial permittivities of the bi-layer PPE structures are kept at $k_{Si_3N_4/SiO_2} \sim 1419$, $k_{Al_2O_3/SiO_2} \sim 2373$, and $k_{Al_2O_3/Si_3N_4} \sim 428$ as extracted previously. In both set of simulations, the energy stored in the electric fields is used to calculate the total capacitance of the bi-layer PPE capacitors. The results shown in Table 3.4 clearly illustrate that there is a very good match (less than 1.5% error) between the

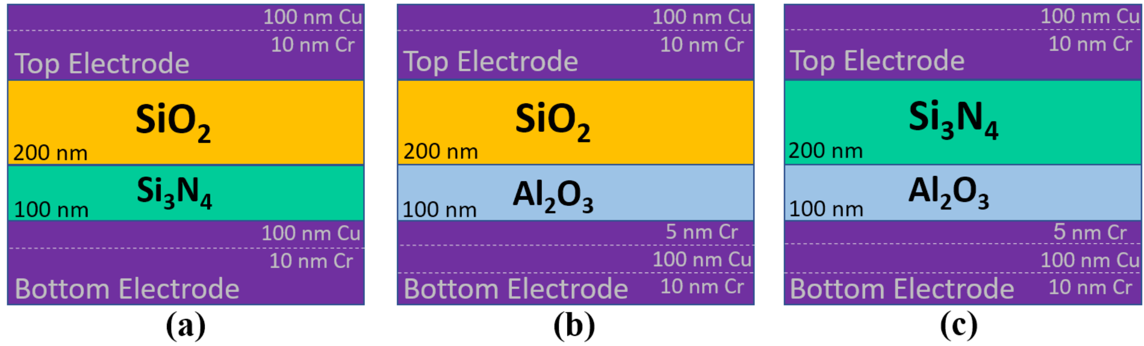


Figure 3.7: A (not-to-scale) schematic of bi-layer PPE devices with (a) Si_3N_4/SiO_2, (b) Al_2O_3/SiO_2 and (c) Al_2O_3/Si_3N_4 dielectrics. The extra 5 nm of Cr on the bottom electrode are used to help with the adhesion between Cu and Al_2O_3.

Table 3.4: A comparison between the average measured capacitance, the no high-k, and high-k simulations of bi-layer PPE structures.

Bottom/Top Dielectric	**Measured C [pF]**	**No High-k Simulation [pF]**	**High-k Simulation [pF]**
Si_3N_4/SiO_2	1.01	1.00	1.00
Al_2O_3/SiO_2	1.20	1.19	1.19
Al_2O_3/Si_3N_4	1.28	1.26	1.26

capacitances of the fabricated PPE devices and the simulated structures *with or without* a high permittivity 1 nm interfacial layer. This is in contrast with the IDE data shown in Table 3.2, where there is a significant mismatch between the experimental and simulation results without the enhancement of the 1 nm interfacial layer model.

Unlike the IDE test structures, these PPE structures do not have the sensitivity to characterize the normal component of permittivity because most of the voltage drop in the device is across the bulk material. The voltage drop in the device over a thin 1 nm layer is very small in comparison to the bulk regions which have 300 times greater thickness. This is illustrated in simulation such that, to 3 significant figures, the capacitance of the PPE device does not change with the inclusion of high-k values for the interface as seen in Table 3.4. This can also be illustrated with basic equivalent capacitor models as seen in Fig 3.8. The higher sensitivity of the electrical properties of the IDE structures is due to the configuration of the equivalent material capacitances which are in a parallel configuration,

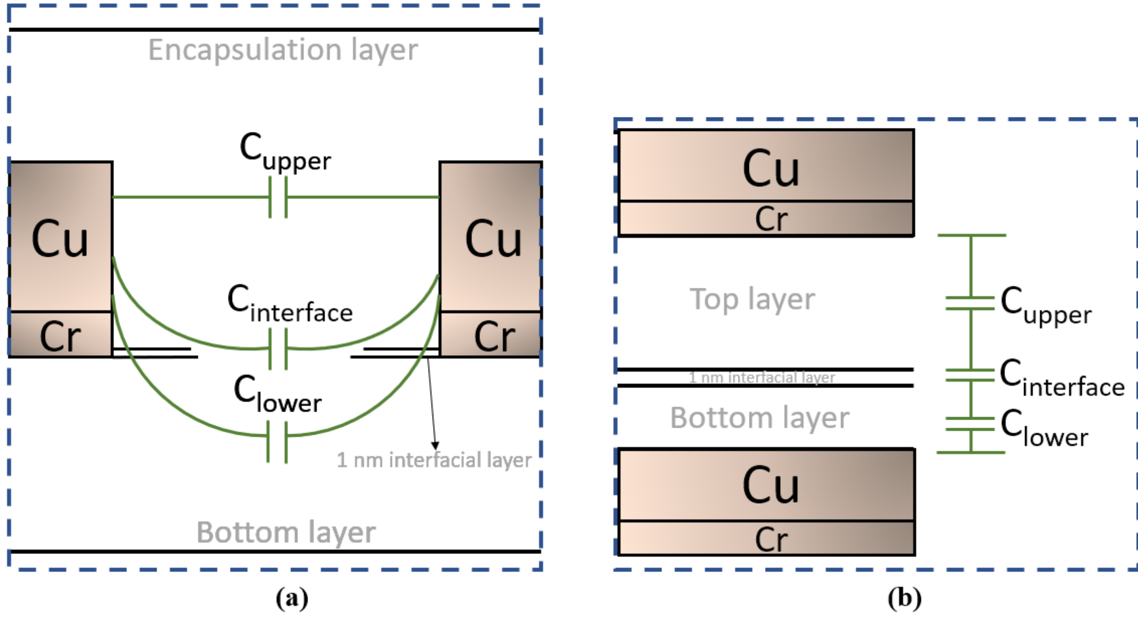


Figure 3.8: Equivalent circuit models showing different capacitive components for (a) an encapsulated IDE device and (b) a bi-layer PPE structure.

which then sums to give the total capacitance as:

$$C_{eq} = C_{upper} + C_{lower} + C_{interface} \tag{3.1}$$

However, for the PPE configuration as seen in Fig 3.8 (b), each material layer is modelled with a series connected set of capacitors, which gives:

$$\frac{1}{C_{eq}} = \frac{1}{C_{upper}} + \frac{1}{C_{lower}} + \frac{1}{C_{interface}}, \tag{3.2}$$

Unlike the IDE structure, the overall bi-layer PPE capacitor is not highly sensitive to a higher interfacial capacitance. This is especially true given the thickness of the interfacial capacitance in the PPE orientation, which is approximately:

$$C_{interface} \approx \frac{k_{interface}\varepsilon_0 A_{PPE}}{t_{interface}}, \tag{3.3}$$

where $k_{interface}$ is the interfacial permittivity, ε_0 is the permittivity of free space, A_{PPE} is

the surface area of the PPE electrodes, and $t_{interface}$ is the thickness of the high-k interfacial layer (~ 1 nm). Subsequently, the PPE devices fabricated in this research cannot confirm or deny the presence of an anomalous permittivity component in the direction normal to the interface. However, given the plethora of PPE experiments in the literature involving thin film stacks of Si_3N_4/SiO_2 (Sharma, Hooda, and Sharma, 2018), Al_2O_3/SiO_2 (Gambino *et al.*, 2019), and Al_2O_3/Si_3N_4 (Ho *et al.*, 2014) that have not reported capacitance anomalies, it seems reasonable that the normal polarizability component should be within a range that is close to the bulk values. This observation in the literature when combined with the results of this part of the chapter suggests that the interfaces of these materials have a high degree of anisotropic permittivity behavior at low frequencies (smaller than 1 kHz).

3.5 Stress Induced Device Failures

Delamination and cracking, whether at the dielectric/substrate interface, dielectric/dielectric interface or within the dielectric film itself, is one of the major issues responsible for film failure and occurs as a result of stresses that are caused by different parameters including CTE mismatch, particle impact or indentation and film shrinking or swelling (Nazir and Khan, 2017). This can lead to significant changes in the interfacial properties within the fabricated structure, which can become more complex due to the sensitivity of film/substrate and dielectric/dielectric interfacial bonding to pre-treatment and contamination, the thickness of each deposited film, and the properties of both the film and substrate, all of which would require extensive fracture mechanics modelling. This section will explore the effect of CTE mismatch on heterogeneous IDE device performance using FEM stress modeling, experimental observations and simulation of these IDE structures.

3.5.1 Impacts of CTE Mismatch between Laminates

Regardless of the deposition technique, dielectric films are always under some form of stress. Residual stress measures the amount of disorder present between the substrate and

the dielectric film introduced during film deposition (called intrinsic stress) and/or thermal treatment (thermal stress). The former is related to the film structure and occurs during the process of film growth. Thermal stress, on the other hand, develops when the dielectric films and the substrate undergo heat/thermal treatment at a temperature that is lower or higher than film deposition temperature. As each deposited film and the substrate generally have different CTEs, they shrink or expand at different rates in reaction to changes in temperature for a two layer system.

When the CTE of a dielectric layer is higher than that of its underlying nanolaminate layer or substrate, for instance when a SiO_2/air device is encapsulated with either Si_3N_4 or Al_2O_3, then once the temperature drops, the layer underneath shrinks less than the one above it, which can hinder the encapsulant layer to shrink fully, hence leading to "tensile stress" as shown in Figure 3.9 (a). On the other hand, if the CTE of the encapsulating film is lower than that of the underlying layer/substrate underneath, then the layer(s) underneath shrinks more than the encapsulant layer during cooldown, which results in "compressive stress" (Berdova *et al.*, 2015) as shown in Figure 3.9 (b).

Dielectric films thinner than their entire underlying substrate can lose adhesion due to high residual stress, which can lead to cracking/delamination. When there is very high tensile stress, the encapsulant layer may undergo "crack-induced delamination" as shown in Figure 3.9 (a) after (Berdova *et al.*, 2015). Whereas, when compressive stress in the dielectric films exceeds the critical bonding strength of the films with the underlying layer(s)/substrate, buckling delamination may occur as illustrated in Figure 3.9 (b) (Berdova *et al.*, 2015).

PECVD-deposited dielectric films such as SiO_2 and Si_3N_4 are highly common in the nanoelectronics and microelectronics industries. As the fabrication processes of most nano- and microelectronic devices require multiple thermal cycles (i.e. exposure to different temperatures) for the deposition or annealing of each layer of material deposited, full understanding of the thermo-mechanical properties of PECVD films is required to help under-

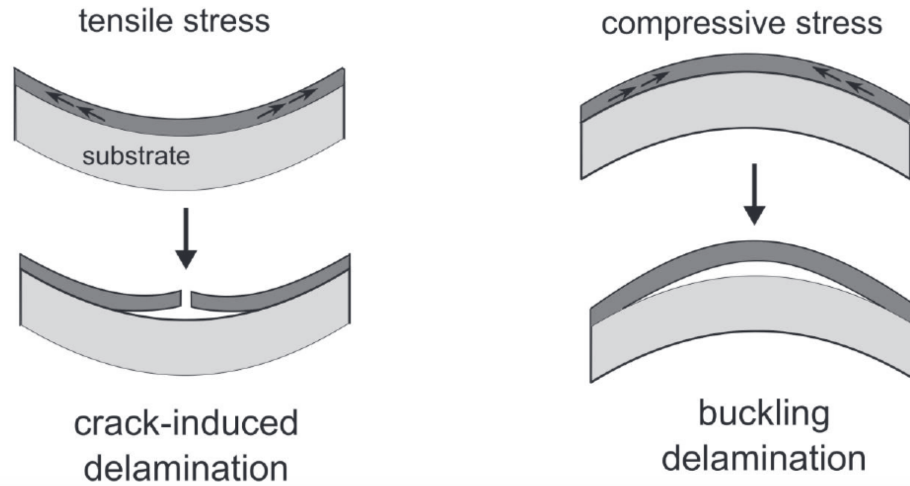


Figure 3.9: Schematic of dielectric film failure under (a) high residual or (b) compressive stress after (Berdova *et al.*, 2015).

stand and analyse the optimize mechanical reliability of devices, as stress development during fabrication is inevitable. In the case of encapsulating SiO_2 with Si_3N_4, since the CTE of SiO_2 is lower than Si_3N_4, i.e. $\alpha_{SiO_2} < \alpha_{Si_3N_4}$, it is likely that the Si_3N_4 encapsulation layer will undergo some degree of delamination. This means that post cool-down, the Si_3N_4 layer will change its shape, volume and density, which will result in a large drop in the overall capacitance of the encapsulated nanolaminate SiO_2/Si_3N_4 structure due to voids introduced between the electrodes. Similarly, since Al_2O_3 has a much higher CTE than its underlying SiO_2 layer, i.e. $\alpha_{SiO_2} \ll \alpha_{Al_2O_3}$, and a relatively larger CTE than Si_3N_4, there is a high probability that delamination will occur in both structures, thereby causing a decrease in the anticipated average measured capacitance after encapsulation.

Indeed, if the three IDE structures with high chances of delamination of encapsulation layers including SiO_2/Si_3N_4, SiO_2/Al_2O_3, and Si_3N_4/Al_2O_3 are simulated using 2-D FEM in COMSOL Multiphysics®, since the y-stress and the shear stress are maximum at the edges of the two nanolaminate layers as shown in the y-tensor and the xy-tensor plots in Figure 3.10 (b) and (c), there is a good chance that the top layer gets delaminated easily at the edges. It should be noted that the Cu electrodes on top of the 100 nm di-

electric nanolaminate film will also add additional tensile stresses, which will increase the chance of delamination of the encapsulation layer significantly as shown in Figure 3.11. It has been shown in SiO_2/barrier interfaces found in typical Cu interconnect structures that they are highly susceptible to subcritical debonding and delamination similar to stress-corrosion cracking in bulk glasses (Lane, Liu, and Shaw, 2004). It has been observed that the underlying Cu pads also contribute to the strain energy released when the encapsulating film delaminates, making the available driving energy for delamination much higher. The driving energy released during debonding/delamination has been shown to have a strong dependence on the size and spacing of the Cu pads, the modulus and thickness of the Cu layer, and the modulus of the adhered dielectric layer (Lane, Liu, and Shaw, 2004).

In the opposite case, where the top layer has a lower CTE such as the devices fabricated and analyzed in Section 3.3, the layer on top experiences a compressive stress while the bottom layer experiences a tensile stress. In this case, since the centre of the interface of the layers experiences the least amount of stress, this leads to good adhesion between the two layers. Although the shear stress is still maximum at the edges as shown in Figure 3.12 (c), however, the type of bending of the two layers helps with their adhesion and prevents delamination Figure 3.13. In other words, the two stresses balance each other out.

In the FEM model gradient plots shown in Figure 3.10 and 3.12, it is apparent that they only show the two dielectric layers undergoing stress as well as the "air box" and the electrodes have not been included. In the case of the encapsulated devices where the deposition is carried out in several steps under different temperatures, the stress state of the underlying substrate/layer is always relevant. Each film/layer will always be deposited, in the ideal case, at zero stress for the present temperature. Meanwhile, the system is dynamically relaxing at each moment in time to minimize the free energy. This will yield stress gradients everywhere throughout the film. Once the system returns to the room temperature there will be an additional stress associated with CTE mismatch, which, consistent with boundary conditions will also be spatially dependent. Hence, if every single component of stress

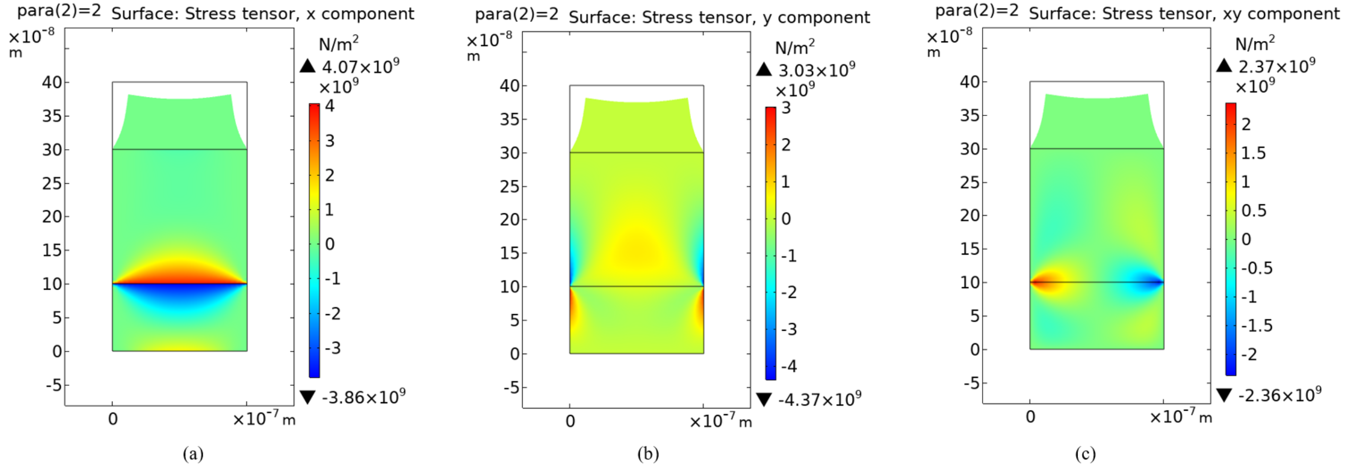


Figure 3.10: The FEM simulation plots for the (a) x-Tensor, (b) y-Tensor and (c) shear stress between a 100 nm Si_3N_4 and a 200 nm of Al_2O_3 encapsulation layer, where the bottom layer has a lower CTE than the encapsulant.

were to be included in the simulation, a few things would have to be taken into account: the fact that even if each layer is deposited stress-free during its own deposition, it will undergo additional stresses after cool down, and also when the next layer is deposited on top, there are always "additional" stresses building up at all times. However, the final result of the FEM simulations for the complete model including the electrodes will be not be fully accurate since COMSOL Multiphysics® is not able to include all the additional stresses in the aforementioned steps.

3.5.2 Experimental Evidence of Delamination Device Failures

Using the same fabrication method explained in Section 3.3.1, when the order of the dielectric layers used in structure Type 1-3 are reversed as shown in Table 3.5 and depicted in Figure 3.14, the average measured capacitances of the devices are found to be lower as predicted, which suggests that there could be possible delaminations at the dielectric/dielectric interface as suggested and validated by theory and the FEM stress simulations.

Similar to the methodology explained in Section 3.3.2, three, 2-D FEM models are built and simulated in COMSOL Multiphysics® as shown in Figure 3.15. In the COMSOL Multiphysics® simulation of each new structure type, all the material parameters are

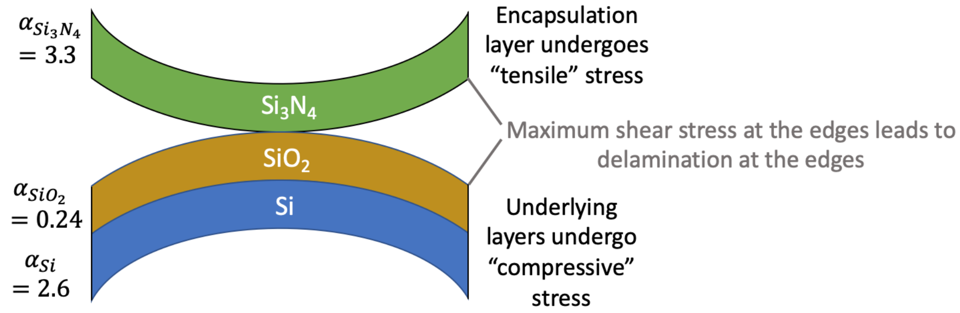


Figure 3.11: Schematic of a nanolaminate structure where the encapsulation layer has a higher CTE than the bottom layer, which makes the top layer undergo "tensile" stress and the bottom layer, "compressive" stress. The maximum stress at the edges leads to delamination of the encapsulation layer

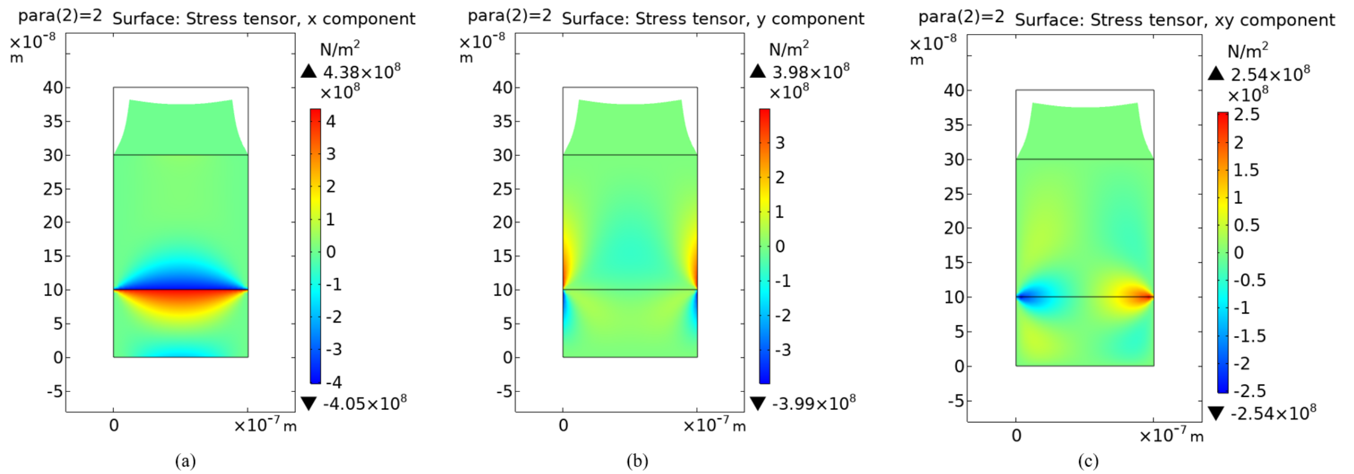


Figure 3.12: The FEM simulation plots for the (a) x-Tensor, (b) y-Tensor and (c) shear stress between a 100 nm Al_2O_3 and a 200 nm of Si_3N_4 encapsulation layer, where the bottom layer has a higher CTE than the encapsulant.

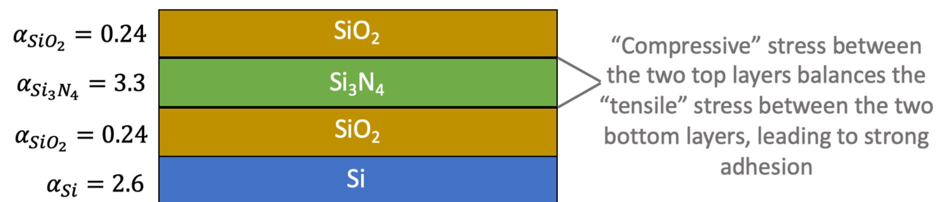


Figure 3.13: Schematic of a nanolaminate structure where the encapsulation layer has a lower CTE than the bottom layer, which makes the top layer undergo "compressive" stress and the bottom layer, "tensile" stress. The types of the stresses at the layers stops the encapsulation layer from delamination and leads to strong adhesion.

Table 3.5: PECVD deposition of SiO_2 and Si_3N_4 and e-beam evaporation of Al_2O_3 dielectric layers and their respective encapsulations for the three other IDE structure types.

Structure	Preliminary Layers (100 nm)	Encapsulation Layer (200 nm)
Type 4	SiO_2	Si_3N_4
Type 5	SiO_2	Al_2O_3
Type 6	Si_3N_4	Al_2O_3

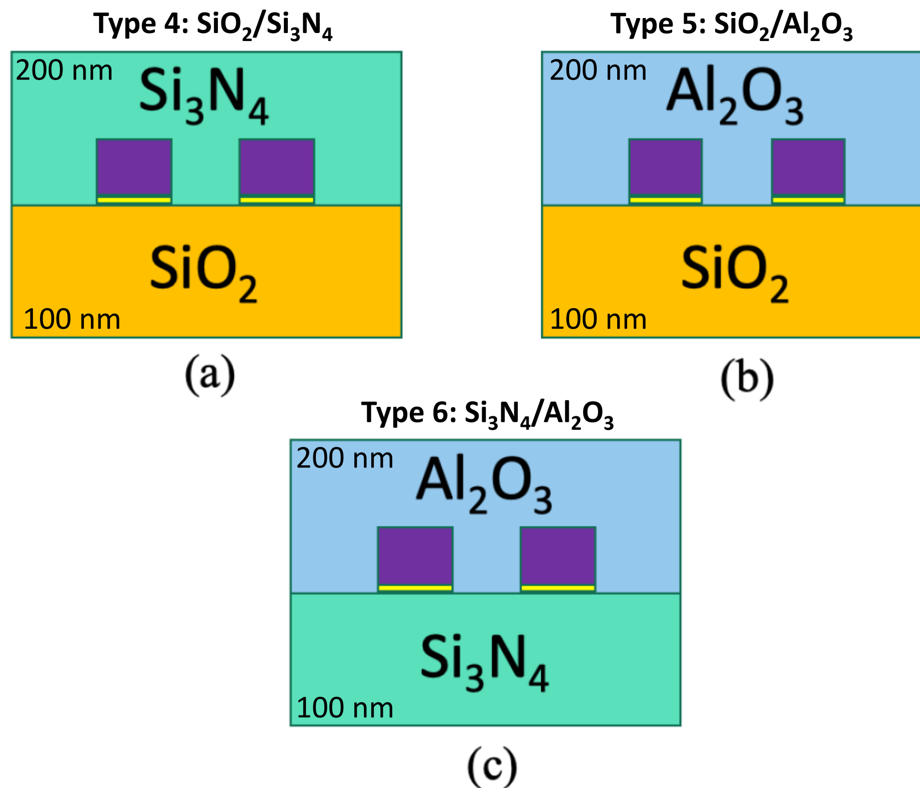


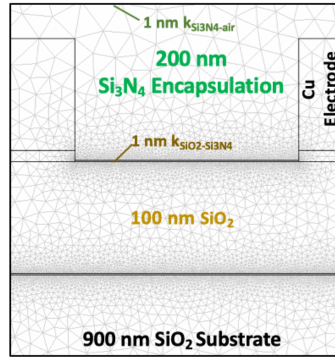
Figure 3.14: Schematic of three structures where (a) in structures Type 4, 100 nm of SiO_2 is encapsulated with 200 nm of Si_3N_4. In structure Type 5 and Type 6, (b) 100 nm of SiO_2 and (c) 100 nm of Si_3N_4, are encapsulated with 200 nm of Al_2O_3, respectively.

known for structure Type 4-6 simulations, except for the dielectric/dielectric interfacial permittivity values of k_{SiO_2/Si_3N_4}, k_{SiO_2/Al_2O_3}, and $k_{Si_3N_4/Al_2O_3}$, respectively. These dielectric/dielectric interfacial values are varied in the simulation for each structure type until they produce calculated simulated results that exactly match the average measurements made for the SiO_2/Si_3N_4, SiO_2/Al_2O_3, and Si_3N_4/Al_2O_3 interfaces for structure Type 4-6 devices. Table 3.6 shows the averaged measured capacitances, the FEM simulation results without any interfacial layers, and the results from the simulation models that include the ~ 1 nm interfacial layer as well as the extracted interfacial-k values for these new three structure types.

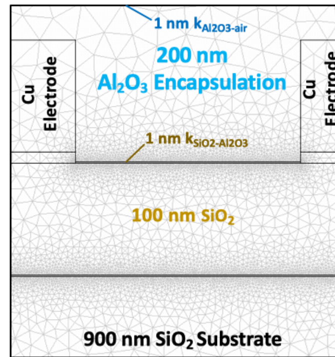
In all these cases, the measured capacitance is consistently lower than the simulation, which implies a device defect is occurring. For example, in the case of encapsulating the SiO_2 sample with a 200 nm Si_3N_4 layer (structure Type 4 in Table 3.5), there is a $\sim 1.4\times$ increase in the average measured encapsulated capacitance compared to the un-encapsulated SiO_2/air sample. On the other hand, the simulated encapsulated capacitance has a $\sim 3.5\times$ increase, which shows that the simulated capacitance value overestimates the average measured capacitance as shown in Figure 3.16. Similarly, there is a significant increase in the simulated encapsulated capacitance of the SiO_2/Al_2O_3 structure ($\sim 3.8\times$), compared to the average measured capacitance of this structure ($\sim 2.2\times$ increase) as shown in Figure 3.16. The Si_3N_4/Al_2O_3 structure (Type 6 in Table 3.5) also shows less increase in the averaged measured capacitance ($\sim 1.9\times$ increase) compared to the simulation value ($\sim 3.2\times$ increase after encapsulation).

Although the capacitances of the SiO_2/Si_3N_4, SiO_2/Al_2O_3 and Si_3N_4/Al_2O_3 structures show an increase after encapsulation, these encapsulated devices seem to have been compromised to introduce some voids and air gaps because the average measured capacitance is consistently less than the FEM simulations that only includes bulk permittivity values with no extra interfacial capacitance.

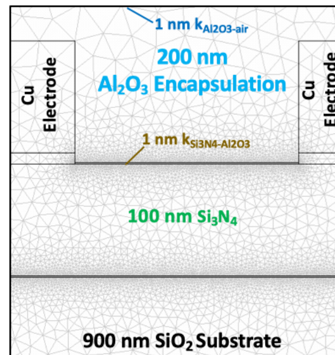
This means that it is in fact not possible to extract the SiO_2/Si_3N_4 interfacial permit-



(a)



(b)



(c)

Figure 3.15: A simulation screen capture of the three test structures showing interfacial effects for (a) SiO_2/Si_3N_4, (b) SiO_2/Al_2O_3, and (c) Si_3N_4/Al_2O_3 interfaces.

Table 3.6: Pre-encapsulation and encapsulated average measured capacitance and FEM simulation results (with and without k-fit) of SiO_2/Si_3N_4, SiO_2/Al_2O_3, and Si_3N_4/Al_2O_3 structures.

		Averaged Measured Capacitance [pF]		No k-Fit Simulation [pF]		Interfactial k-Fit Simulation	
Structure	Bottom/Top	Pre-encapsulation	Encapsulated	Pre-encapsulation	Encapsulated (no k-Fit)	$k_{dielectric/air}$	$k_{dielectric/dielectric}$
Type 4	SiO_2/Si_3N_4	3.16	**4.5**	1.92	**5.5**	$k_{Si_3N_4/air}$ = 58	k_{SiO_2/Si_3N_4} = N/A
Type 5	SiO_2/Al_2O_3	3.17	**6.97**	1.92	**7.32**	$k_{Al_2O_3/air}$ = 160	k_{SiO_2/Al_2O_3} = N/A
Type 6	Si_3N_4/Al_2O_3	2.65	**5.01**	2.48	**7.91**	$k_{Al_2O_3/air}$ = 160	$k_{Si_3N_4/Al_2O_3}$ = N/A

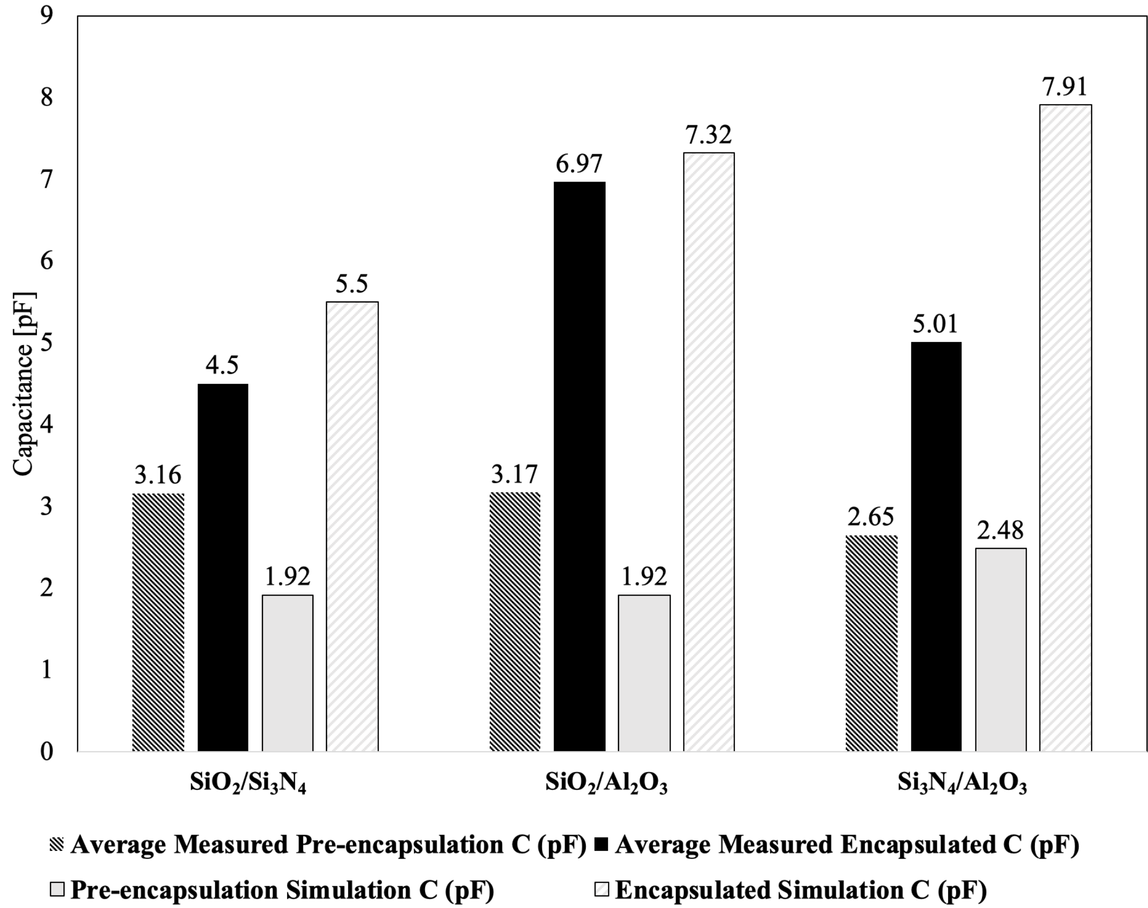


Figure 3.16: Bar graph of the average measured capacitance and the FEM simulations (ignoring interfacial effects) of SiO_2/Si_3N_4, SiO_2/Al_2O_3 and Si_3N_4/Al_2O_3 test devices before and after encapsulation.

tivity to match the average measurements, whilst keeping the Si_3N_4/air interfacial permittivity, $k_{Si_3N_4/Air} \sim 58$. Similarly, whilst the Al_2O_3/air interfacial permittivity is kept at $k_{Al_2O_3/Air} \sim 160$, it is not possible to extract a dielectric/dielectric interfacial permittivity at the interface of SiO_2/Al_2O_3 or Si_3N_4/Al_2O_3 nanolaminates as illustrated in Figure 3.17.

Given the stress and electrostatic simulations and the electrical measurements, it is highly likely that there is delamination at the interface of the Si_3N_4 encapsulant layer in the case of Type 4, and possible further delamination of the Al_2O_3 encapsulant layer for Type 5 and Type 6 structures as Al_2O_3 has a higher CTE than its underlying SiO_2 and Si_3N_4 layers, respectively, i.e. $\alpha_{SiO_2} < \alpha_{Si_3N_4} < \alpha_{Al_2O_3}$.

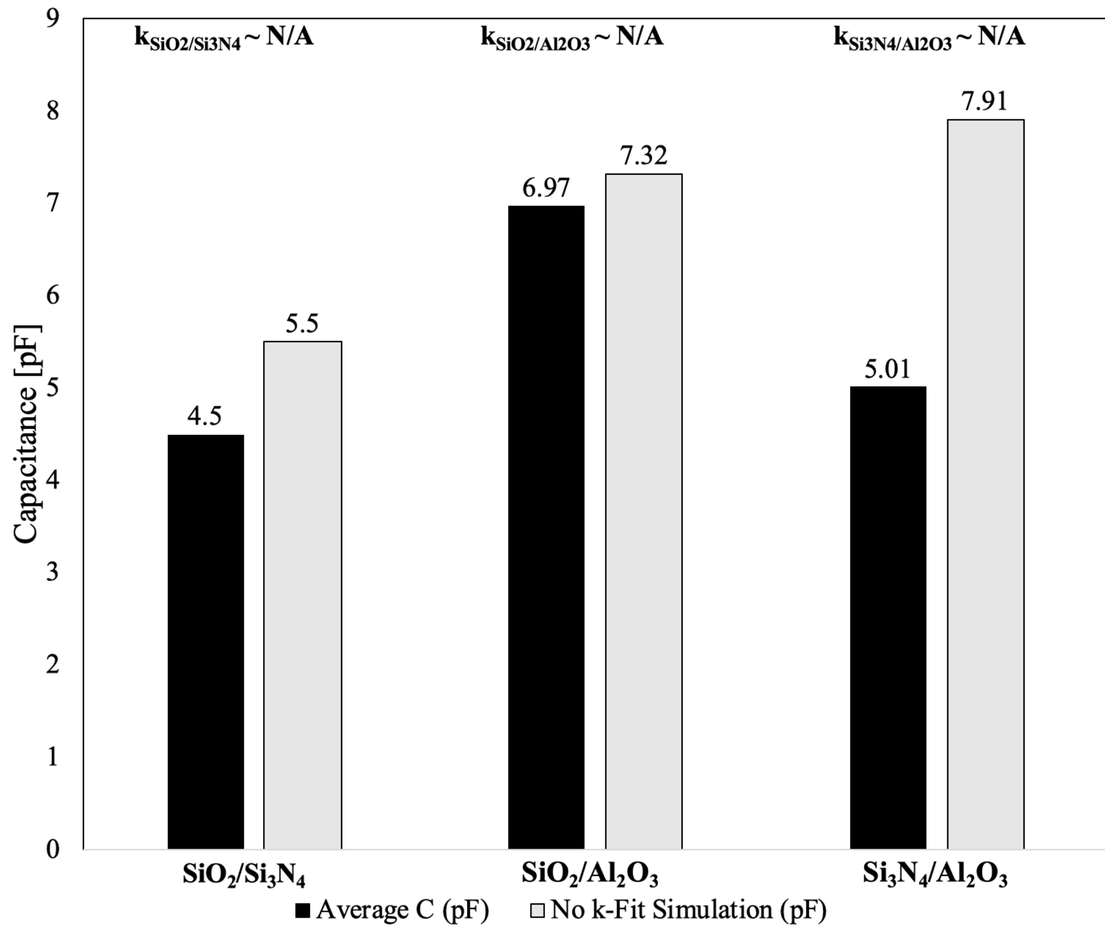


Figure 3.17: Bar graph of the average measured capacitance of SiO_2/Si_3N_4, SiO_2/Al_2O_3 and Si_3N_4/Al_2O_3 test devices measured at f = 1 kHz at standard room temperature as well as the FEM simulations of each test structure.

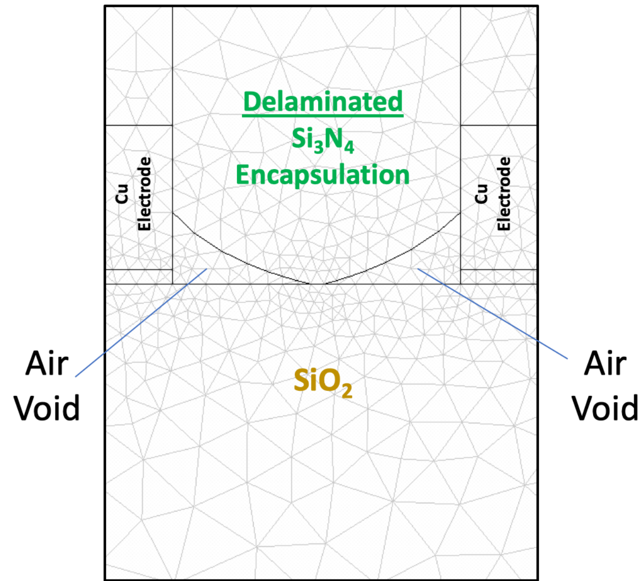


Figure 3.18: A COMSOL Multiphysics® screen capture of delamination of the encapsulation layer in a SiO_2/Si_3N_4 structure.

Using 2-D FEM simulation models, it is possible to verify that if the encapsulation layers in structure Type 4-6 devices undergo delamination and some air gaps are introduced as shown for the SiO_2/Si_3N_4 encapsulated structure in Figure 3.18, the simulated capacitances of the structures also decrease to match the average measured capacitance of these devices as shown in Figure 3.19. In the case of the SiO_2/Si_3N_4 structure, where there is a 18% difference between the average measured capacitance and the FEM simulation result after encapsulation, introducing 16% air voids in the structure decreases the simulated capacitance to match the average measured capacitance as seen in Figure 3.19. Similarly, the 4.7% and the 37% deviation between the average measurements and simulation results post encapsulation for the respective SiO_2/Al_2O_3 and Si_3N_4/Al_2O_3 devices presented in Figure 3.17 are compensated when $\sim$ 4.5% and $\sim$ 35% air voids are added due to the encapsulation layers in the two aforementioned structures.

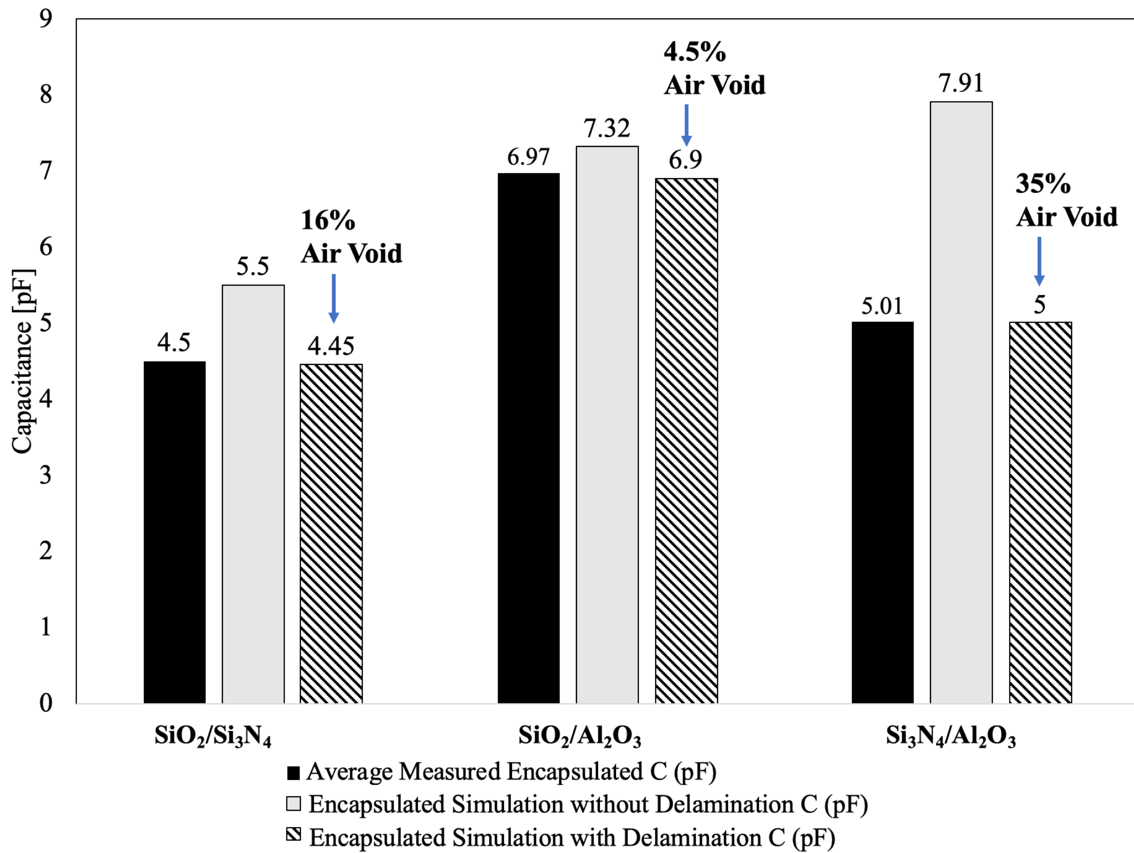


Figure 3.19: Bar graph of the average measured encapsulated capacitance and the FEM simulations of SiO_2/Si_3N_4, SiO_2/Al_2O_3 and Si_3N_4/Al_2O_3 test devices after encapsulation before and after delamination.

3.6 Summary and Conclusions

The investigation in this chapter highlights the importance of studying the polarizability at the interface of Si_3N_4/SiO_2, Al_2O_3/SiO_2, and Al_2O_3/Si_3N_4 nanolaminate structures using reliable two dimensional FEM models. The results in Section 3.2.2 show that the FEM models of homogeneously encapsulated structures are an accurate tool to model the impact of strong polarizability at these dielectric/dielectric interfaces. By using the appropriate quasi-static electromagnetic assumptions, it has been shown that the strong dipole formation of each interface in low-stress devices can be accurately modelled and characterized using a ~ 1 nm interfacial dielectric layer at the interface of Si_3N_4/SiO_2, Al_2O_3/SiO_2, and Al_2O_3/Si_3N_4 nanolmiante layers in the FEM simulation model. The interfacial permittivity for the three aforementioned structures were extracted to be $k_{Si_3N_4/SiO_2}$ = 1419, $k_{Al_2O_3/SiO_2}$ = 2373 and $k_{Al_2O_3/Si_3N_4}$ = 428, such that there is a perfect correlation between measured capacitance data and the simulated values for all three structures. The implications of this high interfacial permittivity on multi-layer encapsulation devices, IDE device leakage current and energy storage device architecture will be explored in later chapters.

In addition to this key discovery of a high average polarizability at the interface, the fabrication of these IDE devices and the order of the encapsulants is important to creating test structures that can measure these interfacial polarizations. For example, in the case of reversely encapsulated devices, it has been shown theoretically, using FEM simulations and validated by experimental results that uncontrollable stress degrades device performance as it causes deformation of dielectric films and interfaces and delamination as well as impacting electrical (and other) properties. It is commonly accepted that irreversible stress develops in PECVD films, but at the moment, is not entirely clear how this mechanism occurs. The lack of published literature for irreversible stress development in PECVD and e-beam evaporated dielectric films has hindered the formation of physically based quantitative models of stress-temperature behavior for these films analogous to those for metal

films (Hughey, Michael, and Cook, 2004).

CHAPTER 4
IMPACT OF DIELECTRIC FILM STRESS ON PERMITTIVITY ANOMALIES OF BI-LAYER AND ALTERNATING SI_3N_4/SIO_2 NANOLAMINATE IDE STRUCTURES

4.1 Introduction

In the previous chapters, homogeneous and bi-layer PPE and IDE structures were fabricated in order to investigate and model anomalous behavior at the interfaces of heterogeneous dielectric layers. In this chapter, the aim is to capitalize on the previous findings in bi-layer structures to investigate anomalously high average polarizability at the dielectric interfaces of heterogeneous structures with alternating multilayer nanolaminates as the encapsulation layer. Specifically, the permittivity anomalies at the Si_3N_4/SiO_2 interface will be compared in an IDE configuration in bi-layer and alternating multilayer encapsulated structures. However, it has been reported that depositing alternating dielectric layers on top of metallic electrodes can lead to high residual stresses due to the significant difference between the CTEs of the materials involved, which may cause deviations of device performance.

To investigate the effects of such stresses and their impacts on interfacial permittivity, two test structures are fabricated such that the first one has low internal stresses and the other has higher stresses. The 'low-stress' structure, which has the same topology as Type 1 structure from Chapter 3, consists of 100 nm of Si_3N_4 deposited on 900 nm underlying SiO_2 layer and is encapsulated with 200 nm of SiO_2 between the metallic electrodes in an IDE structure as illustrated in Figure 4.1 (a). This structure is referred to as Sample 4a in this chapter. The 'high-stress' structure namely, Sample 4b, is a Si_3N_4/air device that is encapsulated around metallic electrodes with alternating nanolamimate Si_3N_4/SiO_2

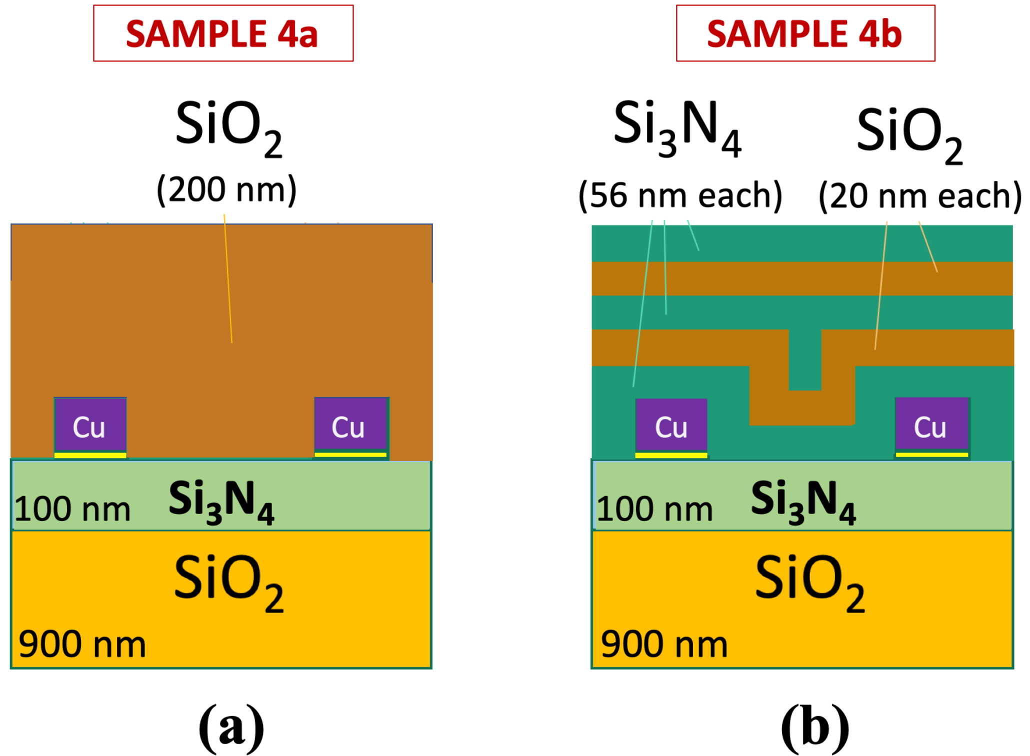


Figure 4.1: Schematic of two structures, where 100 nm of Si_3N_4 is encapsulated with 200 nm of (a) SiO_2 and (b) 5 alternating Si_3N_4/SiO_2 nanolaminate layers.

encapsulation layers with a total thickness of 200 nm, as shown in Figure 4.1 (b). As a part of this work, a simulation of the stresses will be performed in both structures and electrical capacitance measurements will be used to extract effective permittivities of the interface in both the low stress and high stress structures.

4.2 Experimental Design with Stress Considerations

This section will present the FEM stress models for the 'low-stress' heterogeneous bi-layer Si_3N_4/SiO_2 Sample 4a structure, and the 'high-stress' alternating Si_3N_4/SiO_2 encapsulation Sample 4b structure. The impact of residual stresses on interfacial permittivity in these structures will then be investigated using experimental measurements and FEM simulation results.

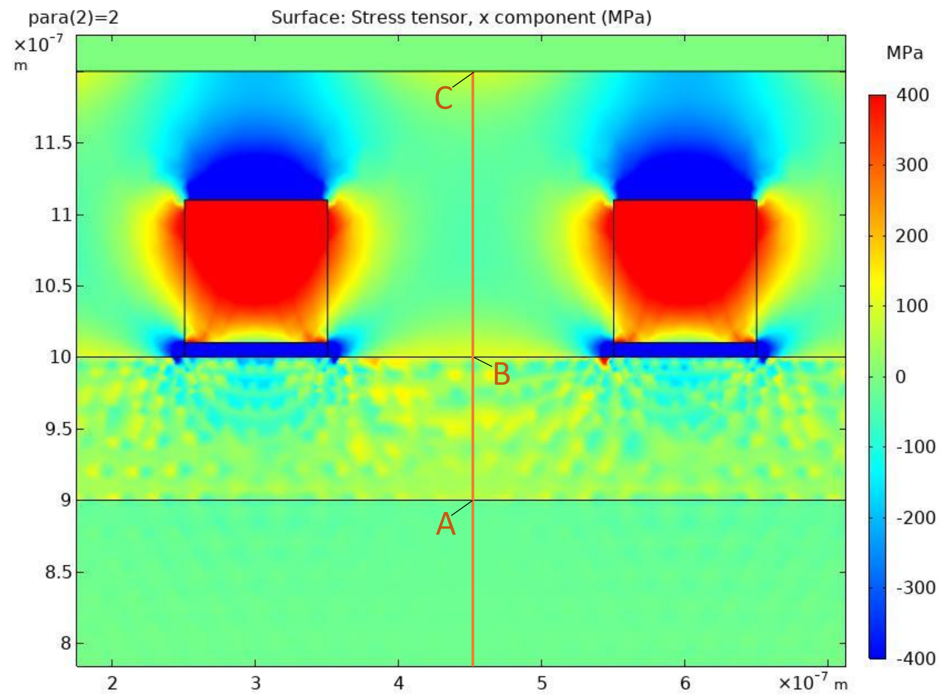


Figure 4.2: A stress simulation screen capture of a heterogeneous bi-layer Si_3N_4/SiO_2 structure, where 100 nm of Si_3N_4 is deposited on top of 900 nm of SiO_2 and is encapsulated with 200 nm of SiO_2 (Sample 4a).

4.2.1 Stress Modeling and Simulation of Nanolaminate IDEs

Using the 2-D Solid Mechanics Interface in COMSOL Multiphysics®, the thermal stresses present in multilayer IDE structures can be modelled and simulated effectively. Thermal stress is defined as mechanical stresses that are caused by changes in temperature and CTE mismatch in the materials used in the structure. In this section, Sample 4a, which is the 'low-stress' heterogeneous bi-layer Si_3N_4/SiO_2 structure, and the 'high-stress' alternating Si_3N_4/SiO_2 encapsulation Sample 4b structure are modelled so as to calculate the stress profile in the x-direction as shown in Figure 4.2 and Figure 4.4, respectively. Using the actual Unaxis PECVD Si_3N_4/SiO_2 deposition temperature (250 °C), the thermal/mechanical stresses of Sample 4a and 4b are simulated and plotted along a specific cut in the middle of the devices as illustrated in Figure 4.3 and Figure 4.5, respectively.

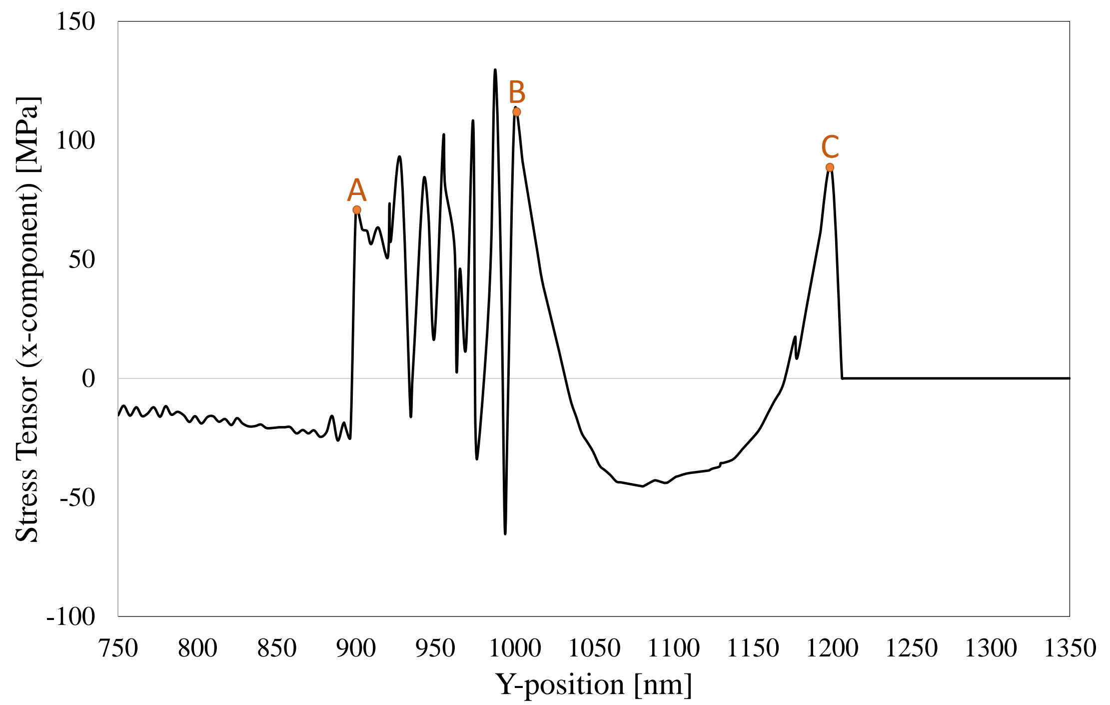


Figure 4.3: The x-component of the stress tensor for the bi-layer Si_3N_4/SiO_2 Sample 4a structure.

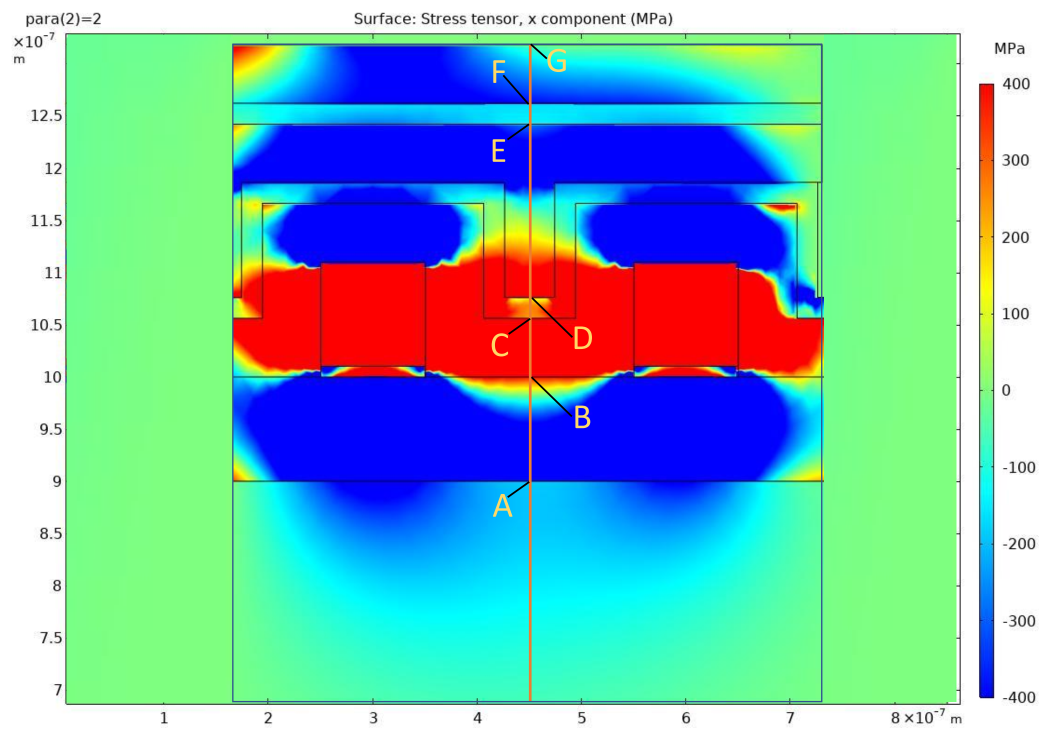


Figure 4.4: A stress simulation screen capture of a Si_3N_4/air structure (Sample 4b) encapsulated with 200 nm of alternating Si_3N_4/SiO_2 nanolaminate layers.

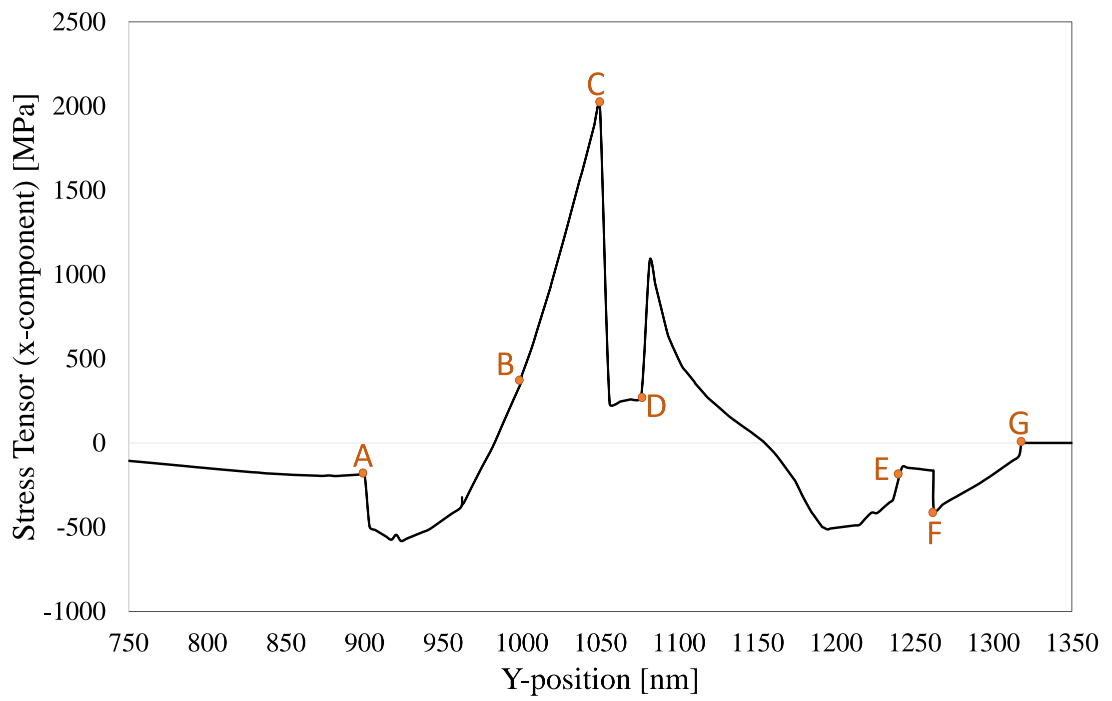


Figure 4.5: The x-component of the stress tensor for the alternating Si_3N_4/SiO_2 nanolaminate layer structure (Sample 4b).

Specifically, the simulated stresses with refined triangular mesh plotted for the heterogeneous Sample 4a (between y = 750 nm to y = 1350 nm) as illustrated in Figure 4.3 display fluctuations between point A and B, as defined in Figure 4.2. This region is within the 100 nm Si_3N_4 layer sandwiched between the underlying 900 nm SiO_2 and the 200 nm SiO_2 encapsulation layers. The maximum differential stress within the entire Sample 4a structure occurs around point B which is exactly at the Si_3N_4/SiO_2 interface. Gradually, the absolute magnitude of stress decreases and then increases between point B and C with minimal fluctuations, which is within the 200 nm SiO_2 encapsulation layer as seen in Figure 4.3.

For the Si_3N_4/SiO_2 (alternating encapsulation layers) Sample 4b structure shown in Figure 4.5, initially, tensile stress gradually increases from point A (marked on Figure 4.4) at y = 900 nm (i.e. the very first Si_3N_4/SiO_2 interface) to point B, at y = 1000 nm (the interface between the 100 nm Si_3N_4 and the first 56 nm Si_3N_4 encapsulation layer). It should be noted that there are no differential stresses between point A and B, contradictory to the bi-layer Sample 4a stress plot. This is due to the fact that the first deposited encapsulation layer in Sample 4b is a 56 nm Si_3N_4, which is the same dielectric material as its underlying 100 nm Si_3N_4 layer. Hence, the 100 nm Si_3N_4 layer is experiencing less stress once the first Si_3N_4 encapsulation layer is deposited.

The magnitude of stress continues to increase from point B and reaches a maximum value of the entire stresses within Sample 4b at point C, which is at the interface between the first 56 nm Si_3N_4 and the second 20 nm SiO_2 encapsulation layers. This stress is almost an order of magnitude higher than the Si_3N_4/SiO_2 interface in the bi-layers. The stresses change between positive and negative (compressive and tensile) values throughout the encapsulation region between point D all the way to point G, which is at the top of final Si_3N_4 encapsulation layer as illustrated in Figure 4.5.

Similar to the explanation given in Section 3.3 of Chapter 3, the FEM stress models in this chapter do not include the entire residual mechanical and thermal stresses caused by the actual "thermal cycles" (including every cool-down and heating of all the deposited layers)

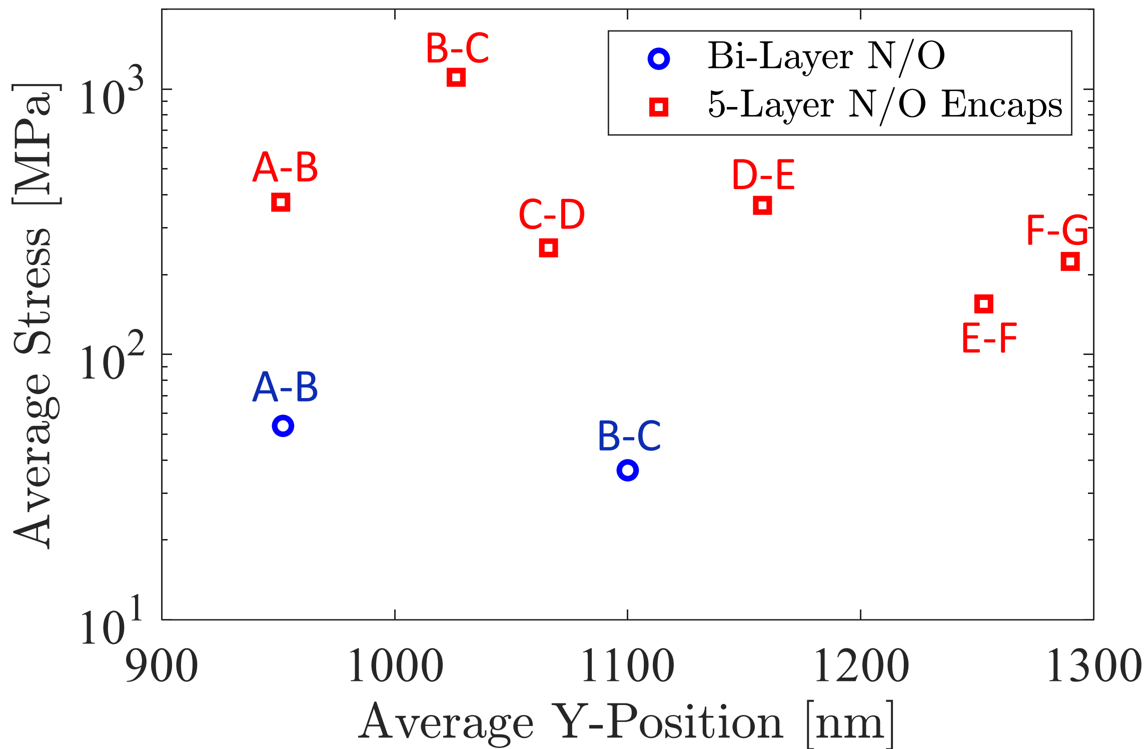


Figure 4.6: Scatter plot of the average simulation stresses within the (a) bi-layer Si_3N_4/SiO_2 Sample 4a and (b) Sample 4b with the alternating Si_3N_4/SiO_2 nanolaminate layers.

as COMSOL Multiphysics® does not have the capability to include all these stresses. However, the simulated stress models successfully convey one of the most important messages of this chapter: *that there is a significant difference in the quality and magnitude of stress in the two aforementioned structures.* The average stresses throughout the deposited layers in Sample 4a and 4b are illustrated in Figure 4.6, which shows a significant order of magnitude difference between the average stresses in the bi-layer Si_3N_4/SiO_2 layers in Sample 4a and Sample 4b, where the dielectric layers are deposited above the metallic electrodes in an alternating manner. The FEM stress simulation results in this section strongly indicate that the thickness of the dielectric layers and the type of deposition of the Si_3N_4/SiO_2 layers in Sample 4a and 4b have a major role in changing the magnitude and types of residual stresses throughout the entire structures.

Table 4.1: Average measured capacitances and FEM simulation results of Si_3N_4/air structures encapsulated with 200 nm of SiO_2 and 200 nm of Si_3N_4/SiO_2 alternating layers (Sample 4b) deposited without breaking vacuum.

Encapsulation Type (200 nm)	Average Measured C [pF]	No k-fit Simulation [pF]	Interfacial k-fit Simulation	Simulation C [pF]
SiO_2	9.93	4.65	$k_{Si_3N_4/air}$=58 **$k_{Si_3N_4/SiO_2}$=1419**	9.93
Si_3N_4/SiO_2 (5 layers)	8.89	6.09	$k_{Si_3N_4/air}$=58 **$k_{Si_3N_4/SiO_2}$=2986**	8.89

4.2.2 Fabrication and FEM Modelling of Nanolaminate IDEs

Sample 4a and 4b are fabricated with the same IDE structure as described in Chapter 2 and 3 using the methodology explained in Chapter 2, Section 2.4. In Sample 4a, a Si_3N_4/air sample (where 100 nm of Si_3N_4 is deposited on 900 nm of SiO_2 isolation layer on Si wafer) is encapsulated with 200 nm of SiO_2 as shown in Figure 4.1 (a), similar to Type 1 structure shown in Chapter 3. For Sample 4b, the same Si_3N_4/air sample is encapsulated with 5 layers of alternating Si_3N_4 (3 layers – each layer has a thickness of 56 nm) and SiO_2 (2 layers – each layer has a thickness of 20 nm) as illustrated in Figure 4.1 (b). The deposition of alternating Si_3N_4/SiO_2 layers in Sample 4b is carried out without breaking vacuum using PECVD. Electrical measurements of capacitance and conductance are conducted using the HP4284A LCR 4-point probe meter under ambient conditions at standard room temperature (25 °C) as shown in Table 4.1.

Further, using the appropriate quasi-static electromagnetic assumptions, the FEM model for the two fabricated structures are built in COMSOL Multiphysics® as illustrated in Figure 4.7. The FEM model for Sample 4a shown in Figure 4.7 (a) is simulated using the bulk permittivity values extracted in Chapter 2, and the SiO_2/air surface permittivity value of $k_{SiO_2/Air} \sim 323$. For Sample 4b, the extracted permittivity value of $k_{Si_3N_4/Air} \sim 58$ is used for the Si_3N_4/air interface. Both samples are then simulated without a 1 nm interfacial Si_3N_4/SiO_2 layer, which significantly underestimates the average measured capacitance

values for the two structures as shown in Table 4.1.

Next, an interfacial high-k permittivity value of $k_{Si_3N_4/SiO_2} \sim 1419$ is used as extracted previously for structure Type 1 in Chapter 3, for **both** Sample 4a and 4b to predict the measured capacitance of the two encapsulated structures. Using the aforementioned bulk and interfacial permittivity values, the simulated capacitance for the FEM model for both Sample 4a and 4b structures are calculated as 9.93 pF and 7.47 pF, respectively. These values are compared with actual average capacitance measurements from fabricated devices for Sample 4a and 4b. Although the values in Sample 4a completely match the experiment, the Sample 4b prediction still continues to underestimate the value of the measured capacitance, which could imply that the interface under the high stress condition is even more anomalous. As it can be seen in Table 4.1, using the interfacial permittivity value of $k_{Si_3N_4/SiO_2} \sim 1419$ significantly underestimates the average measured capacitance of Sample 4b. Hence, while maintaining all the bulk and dielectric/air permittivity values the same as extracted before, a new high-k interfacial value namely, $k_{Si_3N_4/SiO_2} \sim 2986$ is extracted for the interface between Si_3N_4/SiO_2 alternating encapsulation layers to perfectly match the post-encapsulation average measured capacitance of Sample 4b as shown in Table 4.1.

4.3 Discussion of Results

As it can be seen in Table 4.1, the average measured capacitance of Sample 4a matches with the FEM simulation model of the structure using an interfacial k-fitting of ~ 1419 that was extracted for the same heterogeneous structure namely Type 1 in Chapter 3. However, using this interfacial permittivity value, the simulated capacitance for Sample 4b significantly underestimates the averaged measured capacitance for this structure and a much larger interfacial k-value of $k_{Si_3N_4/SiO_2}$=2986 has been extracted as demonstrated in Table 4.1. This result indicates that there could be a correlation and perhaps underlying causation between the stresses and permittivities in these fabricated structures, such that the lower stress structure namely Sample 4a, produces less interfacial anomalies compared to the

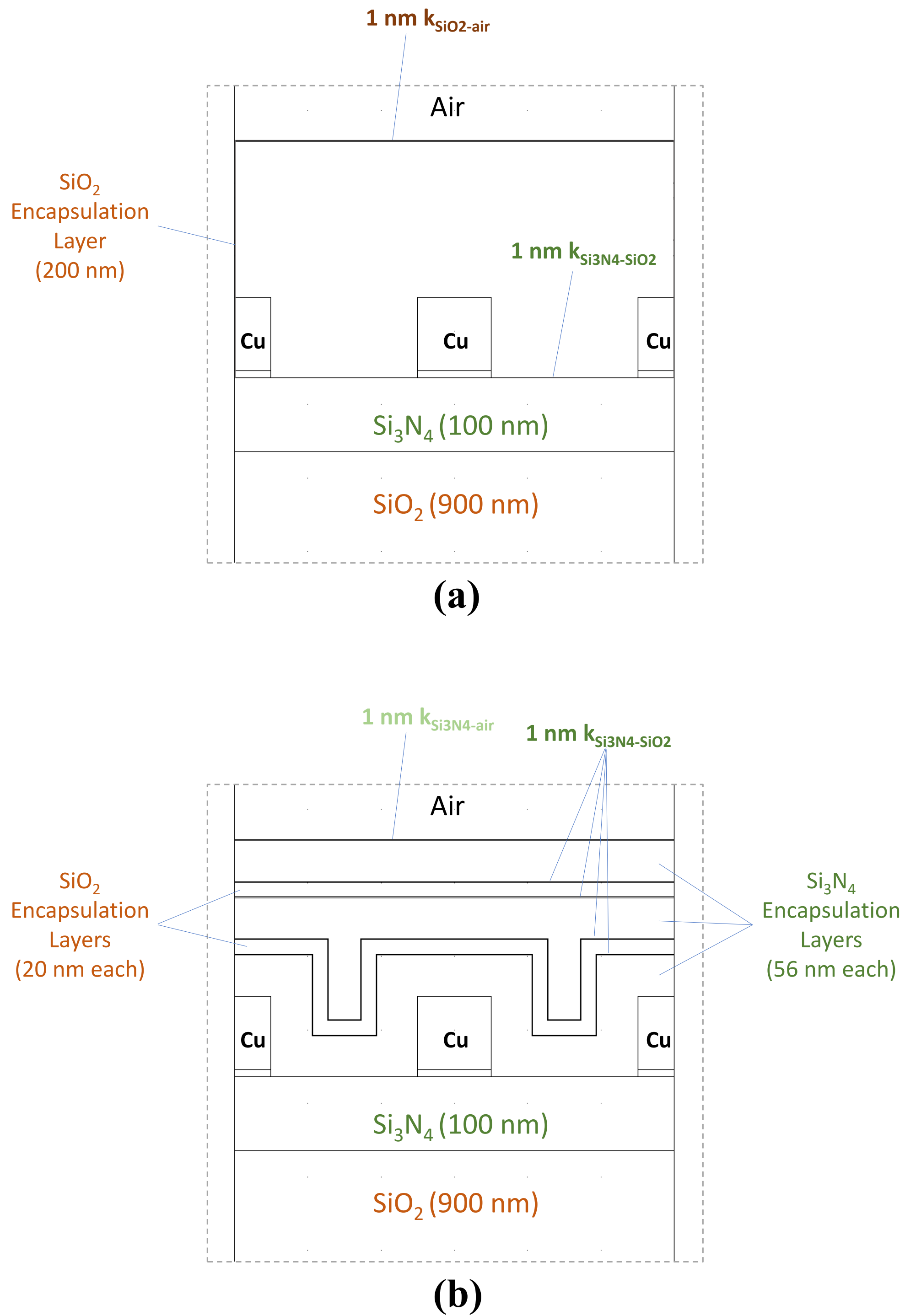


Figure 4.7: A simulation screen captures of two structures, where a Si_3N_4/air device is encapsulated with 200 nm of (a) SiO_2, and (b) 5 alternating Si_3N_4/SiO_2 nanolaminate layers.

higher stress Sample 4b.

As mentioned previously in Chapter 3, PECVD-deposited Si_3N_4 and SiO_2 films undergo residual stress during deposition and cool-down phases caused by a mismatch of CTEs of the dielectric layers and the metallic electrodes. A typical stress-temperature response mentioned in literature for these films involves compressive thermal-mechanical stress development upon exposure to heating, followed by tensile thermal stress development once the film cools down (to room temperature) (Hughey, Michael, and Cook, 2004; Thouless, Gupta, and Harper, 1993; Vinci, Zielinski, and Bravman, 1995; Keller, Baker, and Arzt, 1999). The stress simulations, fabrication and FEM simulations of Sample 4a and 4b in this chapter suggest that residual stress is behind the increase in the permittivity with the increasing number of dielectric nanolaminate layers.

Previous work has demonstrated that compressive in-plane residual stress or out-of-plane tensile stress could lead to an increased permittivity value of bulk materials. It has been amply shown both numerically and experimentally in multilayer ceramic capacitor (MLCC) structures that residual and compressive in-plane stress in the layers of the MLCC increases as more dielectric layers are deposited. Researchers in Yang *et al.* (2008) have reported that there is a strong dependence between the bulk permittivity of MLCC structures, such that the bulk permittivity increases with increasing compressive stress. The authors in Yang *et al.* (2008) have demonstrated using 2-D FEM simulation coupled with X-ray diffraction measurements that compressive in-plane stress in MLCC at a frequency of 1 kHz is a dominant factor to improve bulk permittivity. The researchers in Böse *et al.* (2011), Nakano, Nomura, and Takenaka (2003), Park *et al.* (2005), and Shin *et al.* (2005) have similarly observed enhancements in bulk permittivity in multilayer dielectric elastomer actuators when the amount of stress in the dielectric films is increased.

Similarly, in certain materials such as ferroelectric, it is possible that under uniaxial stress the position of ions in the lattice change by these internal forces resulting in the capacitance change. MLCC with Ni internal electrode have been shown to have higher

capacitance and bulk permittivity under increased uniaxial stresses (Saito and Chazono, 2003). In such a structure, however, the increase in capacitance was only observed when uniaxial compressive stresses were applied in a particular direction (parallel to the internal Ni electrode plane) (Saito and Chazono, 2003).

4.4 Summary and Conclusions

The stress and electrostatic FEM models of two encapsulated structures containing different thicknesses and deposition orders of Si_3N_4/SiO_2 layers (Sample 4a and 4b), have been coupled with the fabrication experimental results to extract the interfacial permittivity values at these dielectric interfaces in the two devices in IDE configurations. The overall mechanical stresses and electric field distributions in the alternating nanolaminate Sample 4b structure have been simulated and the interfacial permittivity has been found to be much higher than the bi-layer Sample 4a structure. The increase in stresses and the resulting changes in bonding energies is believed to be the leading cause in the higher interfacial permittivity in Sample 4b ($k_{Si_3N_4/SiO_2} \sim 2986$) as compared to Sample 4a ($k_{Si_3N_4/SiO_2} \sim 1419$). Figure 4.8 compares the maximum stress and interfacial permittivity values of the bi-layer Sample 4a structure and the alternating nanolaminate Sample 4b structure. Although the stress FEM simulations in this chapter do not capture all the residual, tensile and compressive stresses in the aforementioned structures, the correlation found in these experiments between residual stress and interfacial permittivity are in general agreement with reported enhancements in bulk permittivity in multilayer ceramic capacitors after structural stresses are increased.

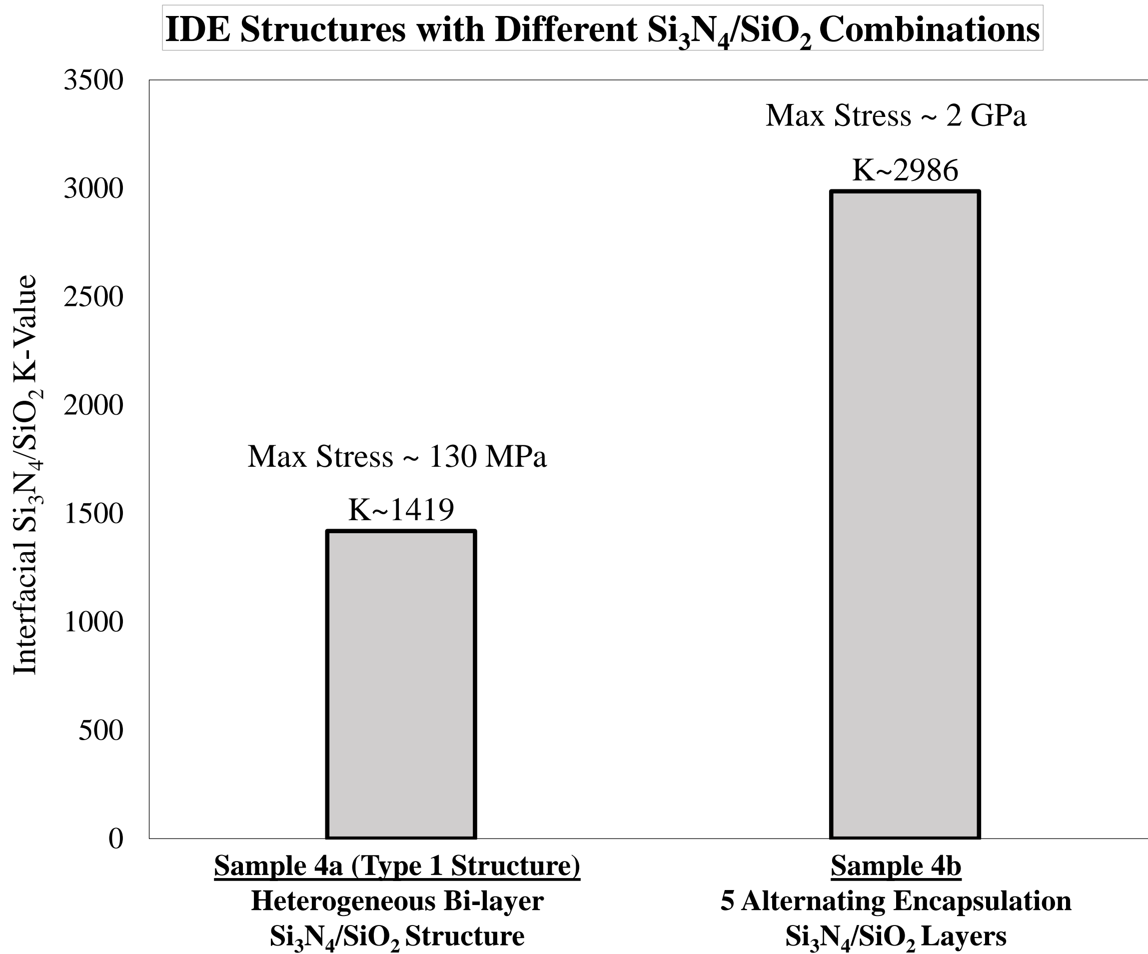


Figure 4.8: Bar graph of interfacial k-values for (a) bi-layer Si_3N_4/SiO_2 (Sample 4a) structure, and (b) 5-layer Si_3N_4/SiO_2 encapsulation layers (Sample 4b) structure.

CHAPTER 5
LEAKAGE CURRENT TESTING AND CONDUCTION MECHANISMS OF PPE AND IDE STRUCTURES

5.1 Introduction

The objective of this chapter is to better understand the current density-voltage (J-V) behavior in homogeneous and heterogeneous PPE and IDE devices and to investigate whether the anomalies at the interface of dielectric/dielectric materials in such structures deleteriously affects the leakage current in a capacitor. Further, the aim is to gain insight into the different conduction mechanisms behind the J-V characteristics in these structures and use this insight to later propose the design of a high-density energy storage device with low loss and high breakdown voltage.

In the following parts of this chapter, the results of extensive current-voltage (I-V) testing of homogeneous and heterogeneous PPE and IDE structures are used to determine and understand the bulk J-V characteristics, the effects of anomalous interfacial regions on leakage current, and the existing conduction mechanisms governing leakage current in IDE and PPE devices. Using the experimental and simulation results from this chapter, the projected energy density calculations for an ideal, low-leakage, high-breakdown and high-density energy storage device is presented in the next chapter of this work.

5.2 Current-Voltage (I-V) Measurement Setup

For the I-V measurements of the homogeneous and heterogeneous IDE and PPE devices, a Keithley 2450 Source Meter (SMU) Instrument is used. The purpose of such measurements is to perform I-V testing that enables the measurement of low current densities before dielectric breakdown. Care is taken so that these measurements are conducted at low enough

applied voltages that would not destroy the IDE or PPE devices. The I-V measurements for the aforementioned devices are conducted at a standard room temperature of 25 °C. From each IDE and PPE structure, 7 devices are tested, which sums to an overall number of 84 I-V measurements. These electrical measurements are then averaged and plotted as shown in Section 5.3.

5.3 Measurement Results and Discussions

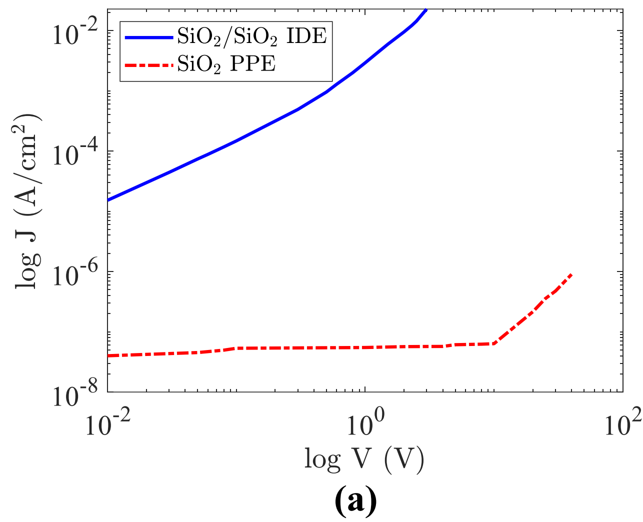
This section will investigate the effects of the heterogeneous dielectric interface on leakage current characteristics in homogeneous and heterogeneous IDE and PPE devices and will further explore the conduction mechanisms responsible for leakage current using J-V characteristics of these structures.

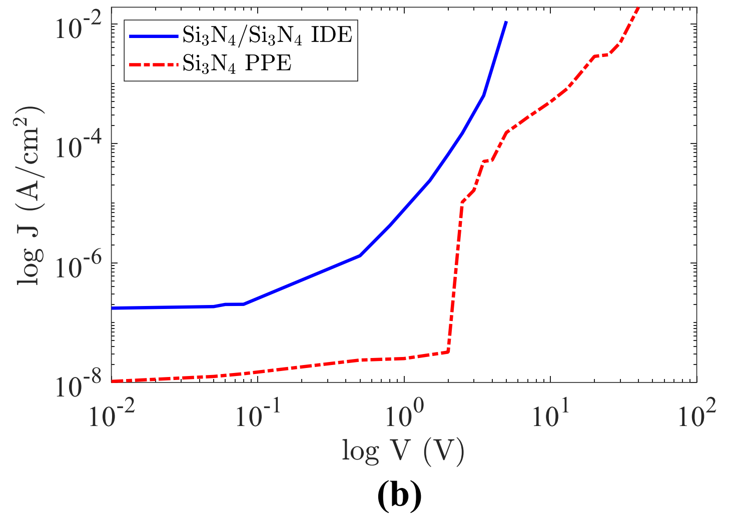
5.3.1 Effects of Interface on Leakage Current Characteristics

a. Homogeneous IDE and PPE Devices

Figure 5.1 illustrates the J-V plot in log-log curves that compare the homogeneous IDE and PPE structures. These plots consistently show that the leakage current is higher with an IDE geometry than a PPE geometry. For example, in the J-V characteristic plot shown in Figure 5.1 (a), the IDE homogeneous SiO_2 device has orders of magnitude larger leakage current than the SiO_2 PPE device. There is also approximately, an order of magnitude difference between the leakage currents of the homogeneous Si_3N_4 IDE and Si_3N_4 PPE and between the Al_2O_3 IDE and Al_2O_3 PPE structure as illustrated in Figure 5.1 (b) and (c), respectively. These differences in leakage are occurring in homogeneous IDE and PPE devices that have no anomalous interfacial planes that could cause additional low resistance current paths.

Subsequently, it is reasoned that the non-uniformity of the electric field in the IDE structure, as opposed to the constant and uniform field between the parallel plates in the





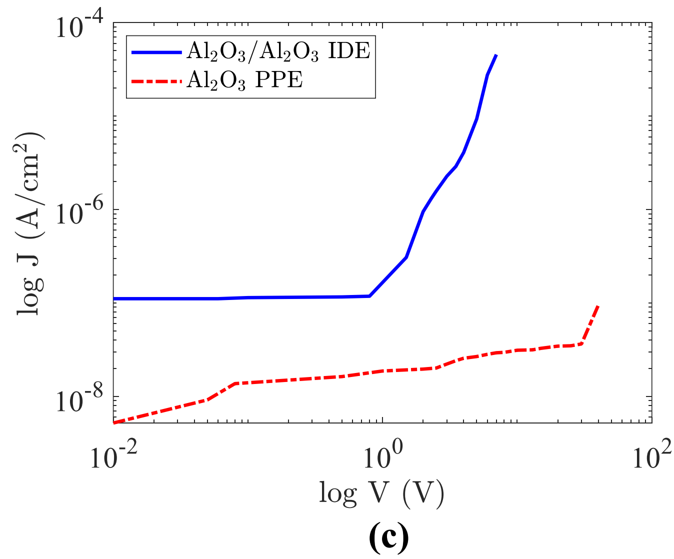


Figure 5.1: J-V characteristic plots for the (a) IDE SiO_2 and PPE SiO_2, (b) IDE Si_3N_4 and PPE Si_3N_4, and (c) IDE Al_2O_3 and PPE Al_2O_3 homogeneous devices.

PPE devices, could result in more leakage paths. For example, Figure 5.2 shows the electric field profile for the homogeneous IDE and PPE structures at V = 0.1 V. As it can be seen in this figure, the electric field fluctuates between one electrode finger to the adjacent electrode in a homogeneous IDE SiO_2 device, where the highest fields are located at the edges of the electrodes, whereas the field remains constant between two parallel electrodes in a PPE SiO_2 structure. These high fields around the electrode could be a source of high carrier injection into the dielectric, and they are completely non-existent in the PPE structure. This suggests that the PPE electrode design for a future energy storage device would be a better configuration to drastically reduce leakage currents; however, the IDE structures are more suitable to study the tangential interfacial permittivity because of their sensitivity to this electrical property.

b. Homogeneous vs Heterogeneous Structure in IDE Devices

This section will explore the difference between the J-V characteristics for the heterogeneous IDE structures and their homogeneous IDE counterparts as shown in Figure 5.3. As it can be seen in Figure 5.3 (a), both Si_3N_4/SiO_2 and SiO_2 IDE structures have very similar J-V characteristics. Subsequently, it appears that the leakage is dominated by the bulk oxide between the electrodes. Therefore, this experimental result implies that the Si_3N_4/SiO_2 interface has almost no impact on the leakage of the device. This result is highly significant because the interfacial permittivity in previous sections has been so high ($k_{Si_3N_4/SiO_2} \sim 1419 - 2986$). This experimental observation highly suggests that this material combination could be a viable candidate for a possible future device design.

In addition, the J-V characteristic plots for the Al_2O_3/SiO_2, SiO_2, and Al_2O_3 IDE structures also suggest that the addition of the interface does not impact overall leakage current. As shown in Figure 5.3 (b), the Al_2O_3/SiO_2 device actually has an order of magnitude lower leakage current than the homogeneous SiO_2 IDE device, but a higher leakage than the homogeneous Al_2O_3 IDE structure as shown in Figure 5.3 (b). As mentioned, this implies

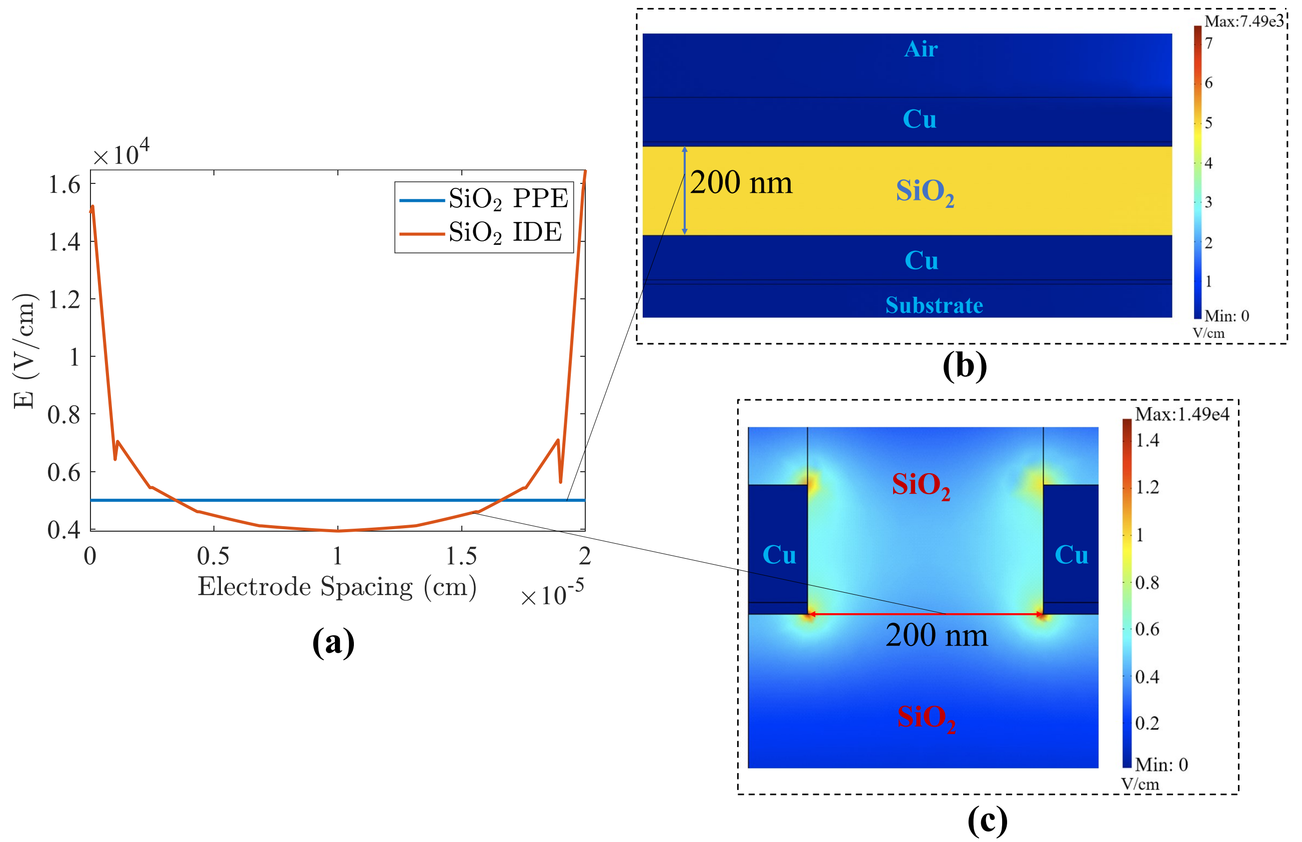
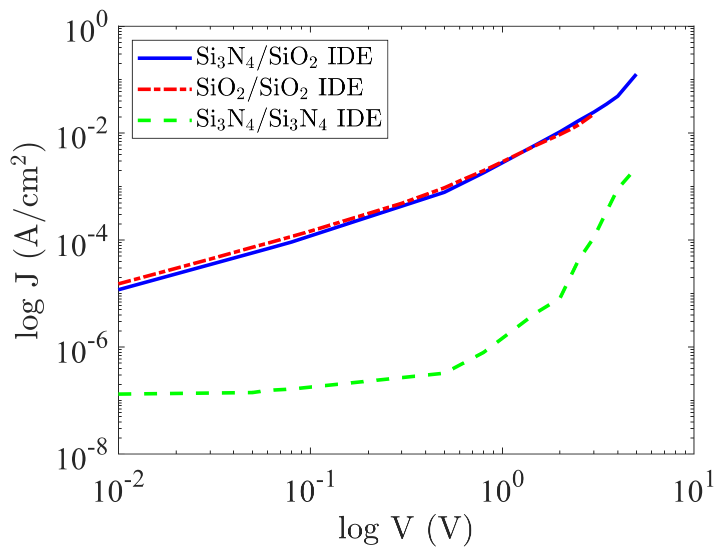
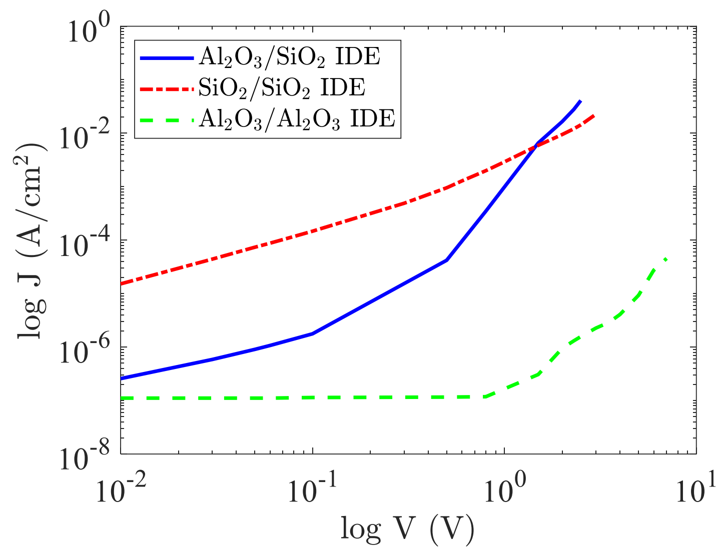


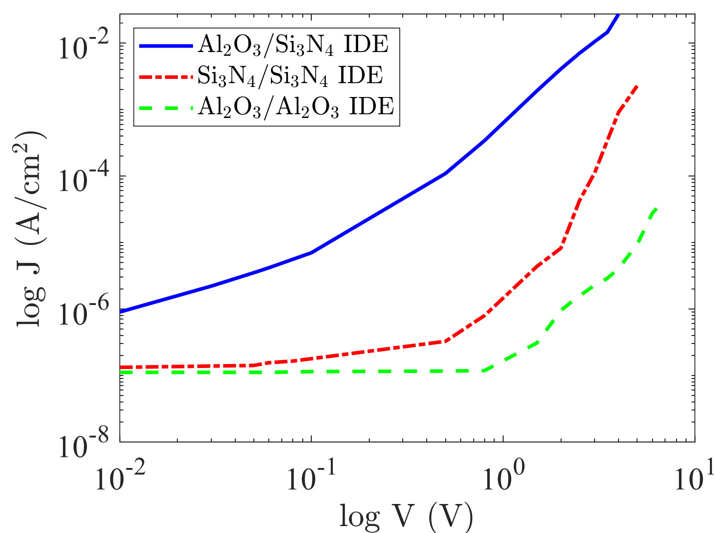
Figure 5.2: Plot of (a) electric field vs electrode spacing characteristics between two electrodes for homogeneous (b) PPE SiO_2, and (c) IDE SiO_2 devices with 200 nm electrode spacing at 0.1 V.



(a)



(b)



(c)

Figure 5.3: J-V characteristic plots for the heterogeneous and homogeneous IDE devices with (a) Si_3N_4/SiO_2, SiO_2, and Si_3N_4, (b) Al_2O_3/SiO_2, SiO_2, and Al_2O_3, and (c) Al_2O_3/Si_3N_4, Si_3N_4, and Al_2O_3 dielectrics.

that the heterogeneous Al_2O_3/SiO_2 structure has a relatively low-leakage interface. This low leakage and high interfacial permittivity ($k_{Al_2O_3/SiO_2}$ = 2373) results are also highly encouraging for incorporation of this Al_2O_3/SiO_2 interface into an energy storage device. It is not completely understood why the insertion of an Al_2O_3 substrate would decrease leakage current so dramatically in the bulk SiO_2 material, but the superior device characteristics are highly positive for future device design.

There is an interface, however, that does seem to worsen the leakage current. As seen in Figure 5.3 (c), the higher leakage current in the Al_2O_3/Si_3N_4 heterogeneous IDE structure compared to the other two homogeneous IDE devices implies that the addition of the heterogeneous interface has deteriorated the quality of the Al_2O_3/Si_3N_4 heterogeneous device, which could be due to more voids and defects at the interface in this structure. Subsequently, this result implies that this would be a poor choice to incorporate into an energy storage device.

Furthermore, in these two promising interfaces the addition of more layers in more complex devices appears to have even more benefits in lowering the currents in these IDE structures. For example, Figure 5.4 (a) shows the J-V characteristics for a heterogeneous Si_3N_4/SiO_2 device and a Si_3N_4/air structure encapsulated with 5 layers of alternating Si_3N_4/SiO_2 as was shown for Sample 4b is Chapter 4. The comparison between the two structures indicates that the addition of multiple Si_3N_4/SiO_2 layers has not increased leakage, however, the multilayer structure actually has over an order of magnitude *lower* leakage current than the bi-layer IDE device. This further reinforces the fact that the presence of a heterogeneous Si_3N_4/SiO_2 interface does not lead to higher loss as compared to the homogeneous IDE structures. Similarly, the comparison between J-V characteristics of a bi-layer Al_2O_3/SiO_2 structure shown in Figure 5.4 (b) and a multilayer encapsulation of 5 Al_2O_3/SiO_2 layers (each layer has a thickness of 20 nm) illustrates that the multilayer device has a lower leakage current than its bi-layer counterpart. The plots in Figure 5.4 further highlight the reliability of multilayer Si_3N_4/SiO_2 and Al_2O_3/SiO_2 structures for further

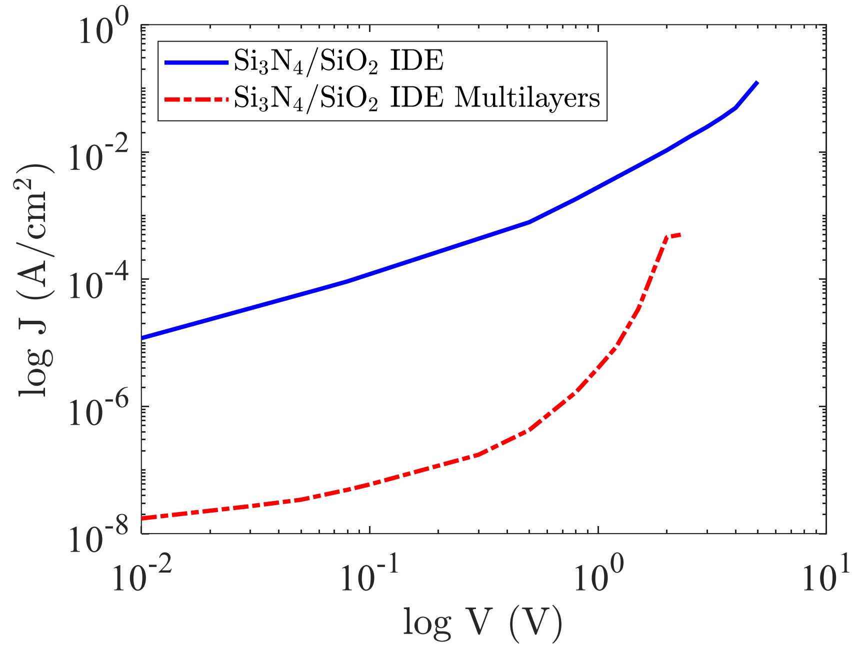
exploration into the design of energy storage devices made from these nanolaminates.

5.3.2 Low Voltage Conduction Mechanisms in IDE and PPE Test Structures

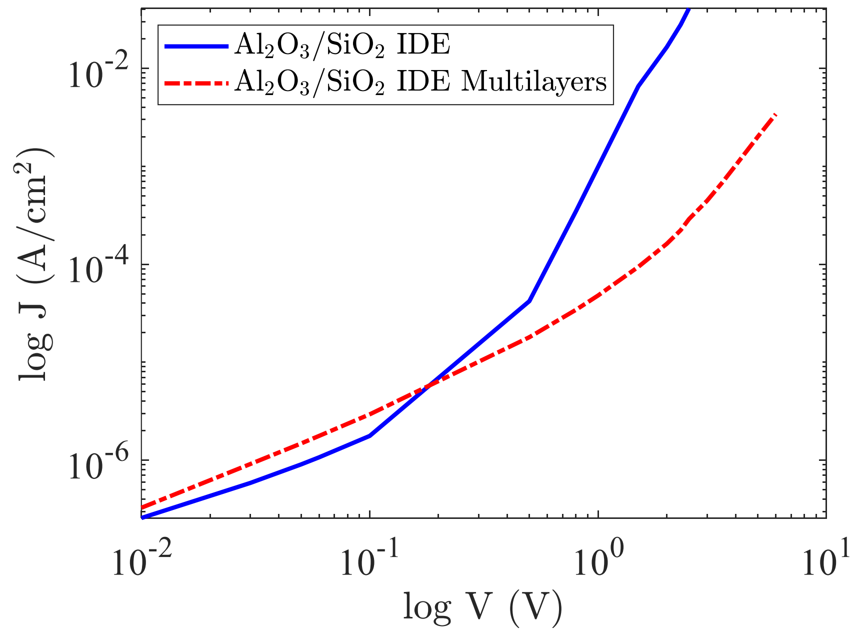
In these dielectric materials, the energy bandgap is large, and the electrons are tightly bonded, such that electrical conductivity is low. The conduction current of these materials that are excited with low electric fields are typically very small since they have inherently low conductances, which are on the order of 10^{-12}–10^{-10} S. However, as a larger electric field is applied, the electric charge due to the electron injection, hole injection, and electron-hole pair generation in these dielectrics can increase, which leads to higher leakage currents and, eventually, an electrical breakdown.

In general, there are two main types of conduction mechanisms, namely electrode-limited conduction mechanisms and bulk-limited conduction mechanisms. The former depends on the electrical properties at the electrode-dielectric contact. The most important parameter in this type of conduction is the barrier height at the electrode/dielectric interface. This type of conduction mechanism includes (1) Schottky (or thermionic) emission. (2) Fowler-Nordheim tunneling, (3) direct tunneling, and (4) thermionic-field emission. The bulk-limited conduction mechanisms, on the other hand, which mostly depend on the properties of the dielectric itself include (1) Poole-Frenkel emission, (2) hopping conduction, (3) ohmic conduction, (4) space-charge-limited conduction (SCLC), and (5) ionic conduction (Neusel, Jelitto, and Schneider, 2015; Chiu, 2014; Sharma, Hooda, and Sharma, 2018).

In all these subcategories of electrode-limited and bulk-limited conduction mechanisms except for ohmic conduction and SCLC, conduction currents and the resulting leakage generally occurs at high temperatures (Neusel, Jelitto, and Schneider, 2015; Chiu, 2014). In this chapter, all the I-V testings are conducted at low test voltages at room temperature. Hence, it is observed that the dominant conduction mechanism in the fabricated dielectric films are ohmic conduction and SCLC. To explore other possible conduction mechanisms



(a)



(b)

Figure 5.4: J-V characteristic plots for the heterogeneous multilayer encapsulated IDE devices with (a) Si_3N_4/SiO_2, and (b) Al_2O_3/SiO_2 dielectrics.

such as Poole-Frenkel and Fowler-Nordheim tunneling, it is necessary to conduct further current testing at a wide range of temperatures for different durations of time.

Ohmic conduction in a dielectric film is characterized by the presence and movement of mobile electrons in the conduction band or mobile holes in the valence band, which mostly originate from impurities, voids, and defects in the dielectric. In this case, the current density increases linearly with the applied electric field according to Ohm's law. The bandgap is too wide for any significant intrinsic conductivity, however, there will still be a small number of carriers such as electrons that may be excited to the conduction band from the valence band or voids and defect levels. The current density J for ohmic conduction in a PPE or IDE structure is expressed as (Neusel, Jelitto, and Schneider, 2015):

$$J = \sigma E = (n\mu_n + p\mu_p)qE, \tag{5.1}$$

where σ is the electrical conductivity, E is the electric field, n is the number of free electrons in the conduction band, p is the number of free holes in the valence band, q is the electron charge, and μ_n and μ_p are the electron and hole mobility, respectively. The electric field E in a homogeneous dielectric PPE capacitor is defined as:

$$E = \frac{V}{d}, \tag{5.2}$$

where V is the voltage applied to the electrodes and d is the spacing between them. In this conduction mechanism, the double logarithmic J-V plot is linear and has a slope, s = 1.

If, in a solid material such as a dielectric film, the voltage is further increased to a certain value V_{TR} beyond the ohmic range, and charge carriers are injected at an ohmic contact into the dielectric material, a transition from ohmic to space-charge-limited current (SCLC) takes place at V_{TR}. SCLC is dominated by charge (electron or hole) carriers that are injected by the metallic electrode into the insulator and become partly trapped within defects in the insulator.

The overall log J-log V characteristic plot in the SCLC mechanism is non-linear and is defined by three main relationships namely, Ohm's law ($J_{Ohm} \propto V$), trap-filled (TFL) current ($J_{TFL} \propto V^2$), and Mott-Gurney law ($J_{MG} \propto V^2$).

$$J_{Ohm} = (n_0\mu_n + p_0\mu_p)q\frac{V}{d} \tag{5.3}$$

$$J_{TFL} = \frac{9}{8}\mu\varepsilon\theta\frac{V^2}{d^3}, \tag{5.4}$$

where n_0 and p_0 is the free electron and hole carrier concentration in thermal equilibrium, respectively, ε_0 is the permittivity in vacuum, ε_r is the relative permittivity of the dielectric, and Θ is the ratio of free charge carrier concentration to total carrier (free and trapped) concentration. However, the square law dependence shown in equation (5.4) is only valid when the insulator has traps of a single discreet energy level as shown in Figure 5.5 (a). For the case where the traps are distributed exponentially within the insulator's forbidden band gap as illustrated in Figure 5.5 (b), the current density has a (s+1) power law relationship with $s > 1$, which characterizes the insulator trap distribution. A typical log-log J-V curve for SCLC is illustrated in Figure 5.6.

As the voltage is further increased, the SCLC enters a region namely, "trap-limited" voltage V_{TFL}, at which all shallow traps in the insulator are filled with charge carriers. Hence, V_{TFL} is the voltage at which a there large increase in the current density as all the injected carriers contribute to leakage current. This region is then followed by a "trap-free" SCLC region. In this region, $\Theta = 1$ as all the injected carriers contribute to conduction. Hence, the J-V characteristic in the "trap-free" region is described by the Mott-Gurney relationship (Neusel, Jelitto, and Schneider, 2015; Chiu, 2014; Chiguvare, 2012):

$$J_{MG} = \frac{9}{8}\mu\varepsilon\frac{V^2}{d^3} \tag{5.5}$$

Figure 5.7 and 5.10 illustrate the J-V characteristic of all the aforementioned homoge-

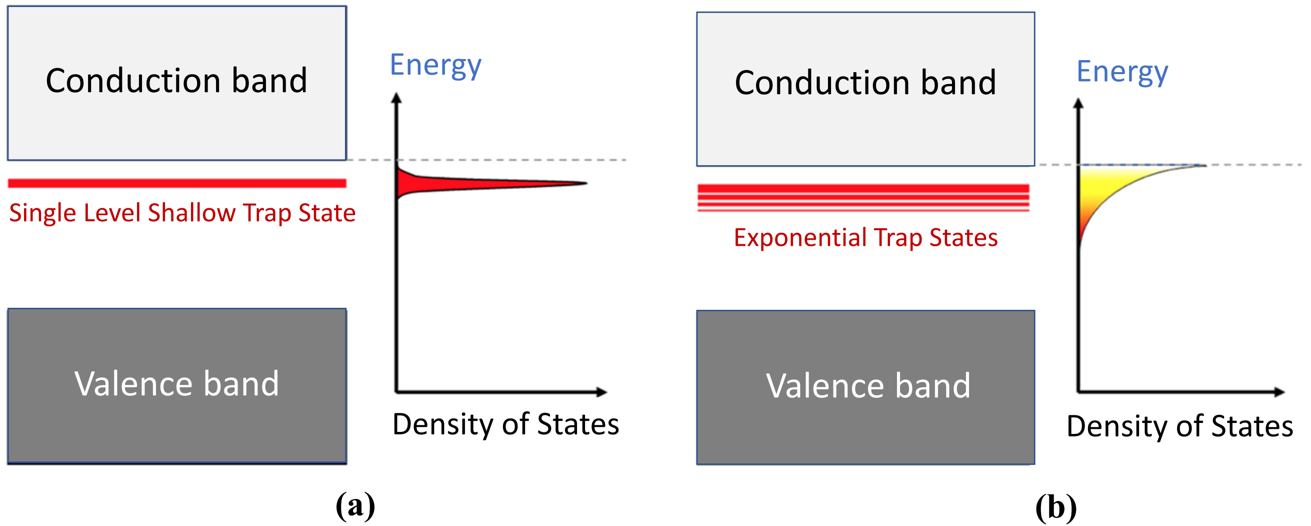


Figure 5.5: Energy band diagram and density of states of (a) single-level shallow trap states and (b) exponential traps states under SCLC regime.

neous and heterogeneous PPE and IDE structures in log-log curves, respectively. In order to distinguish the linear region of the plots (s = 1) from the nonlinear regimes (s $>$ 1), it is necessary to find the coefficient of determination, also known as the "R-squared" values. R^2 values are a statistical measure of how well data points for a sample can fit the line of regression. A R^2 value greater than 0.95 implies a highly linear relationship between the independent variable, which in this case is log V and the dependent variable, i.e. log J. Using the appropriate fitting, the square law dependence between log V and log J can also be determined for the heterogeneous IDE and PPE structures with their dielectric constituent J-V characteristics as illustrated in Figure 5.7 and 5.10, respectively.

As it can be seen in Figure 5.7, the J-V characteristic plots for PPE structures show Ohmic behavior at very low voltages. The low voltage DC electrical conductance G for all the PPE devices can be extracted from I-V measurements in the low voltage region of Figure 5.7, which have been illustrated in Figure 5.8 plots. Using the PPE electrode width W, length L, dielectric thickness T, and electrical conductance G, as illustrated in the PPE

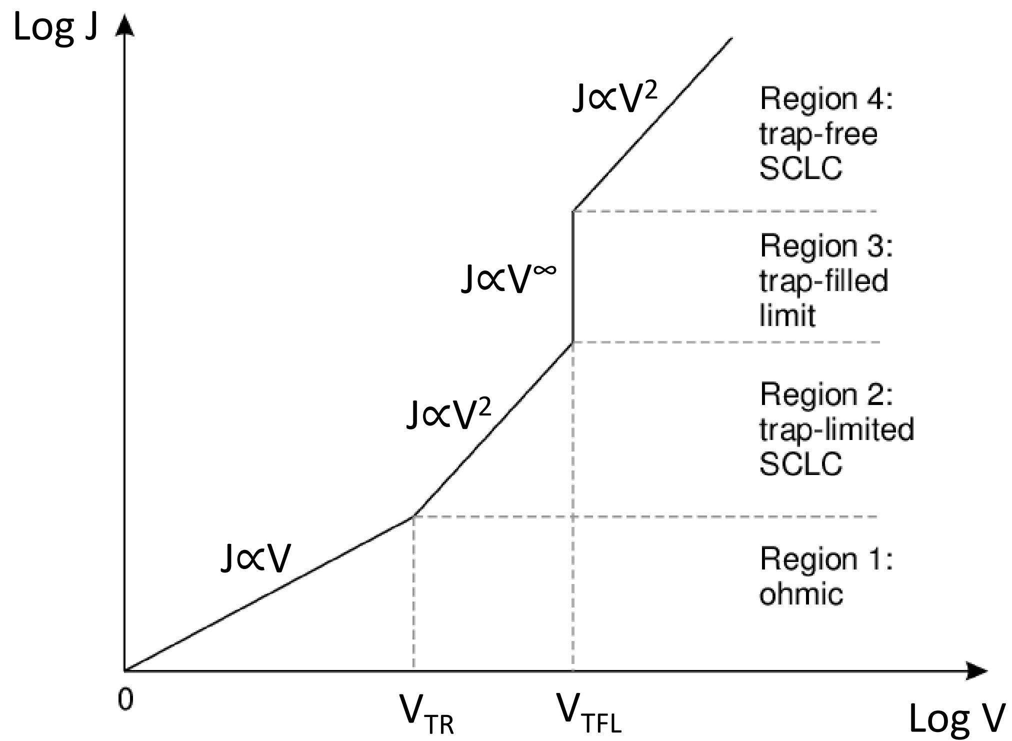
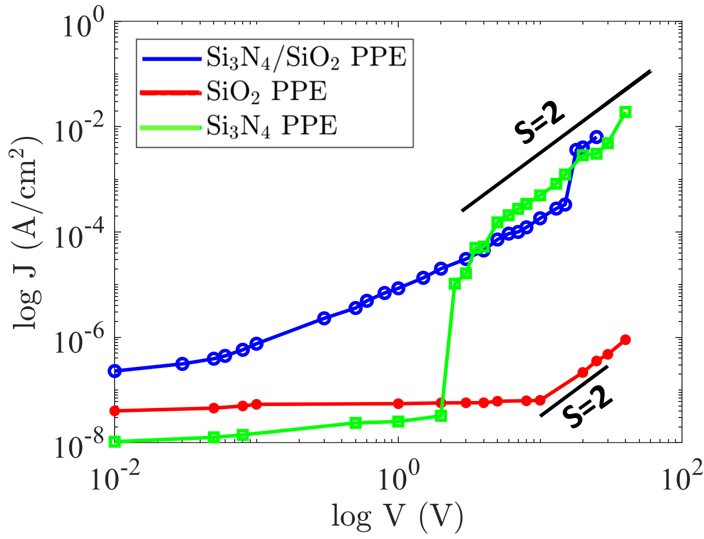
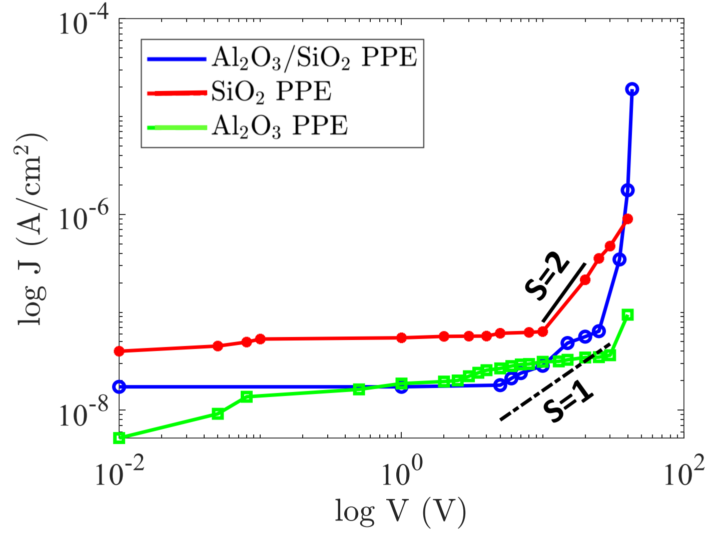
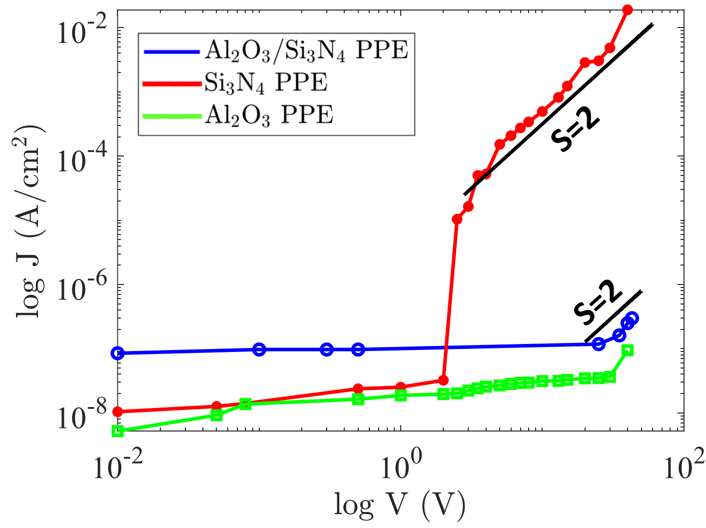


Figure 5.6: A typical current density-voltage characteristic of SCLC current. In this plot, V_{TR} is the transition voltage, where transition from ohmic to SCLC takes place and V_{TFL} is the trap-filled limit voltage.





(a) **(b)**



(c)

Figure 5.7: The J-V characteristic of PPE devices with (a) Si_3N_4/SiO_2, SiO_2, and Si_3N_4, (b) Al_2O_3/SiO_2, SiO_2, and Al_2O_3, and (c) Al_2O_3/Si_3N_4, Si_3N_4, and Al_2O_3 dielectrics.

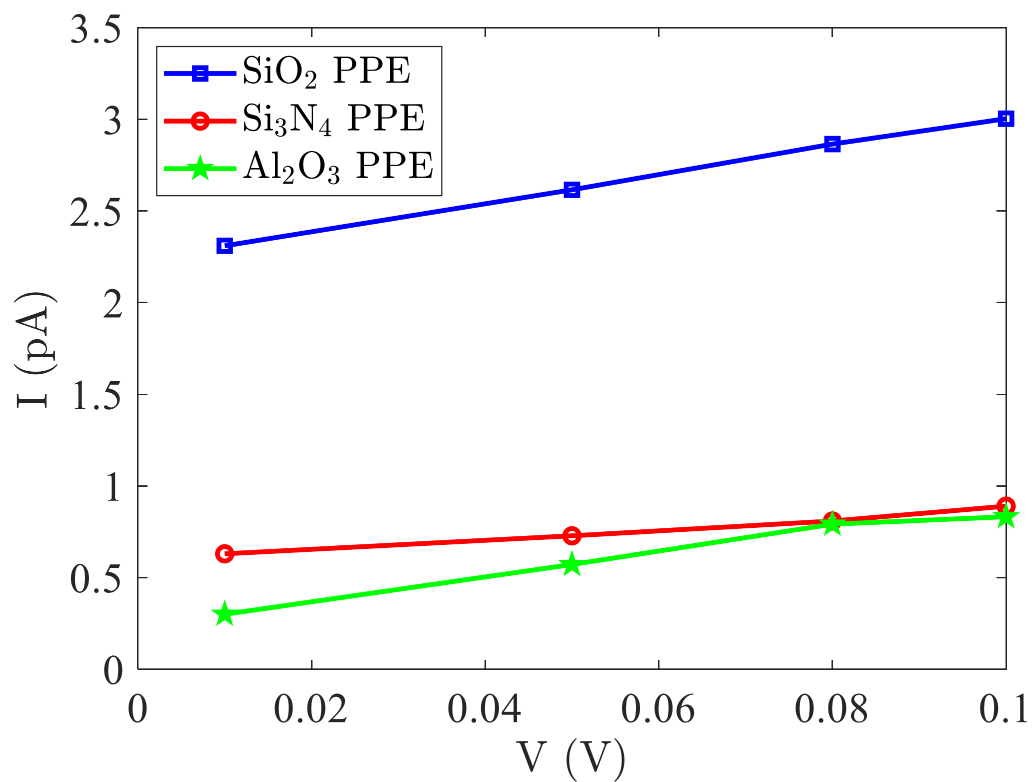


Figure 5.8: The I-V characteristic of homogeneous PPE devices with SiO_2, Si_3N_4, and Al_2O_3 dielectrics at low voltages.

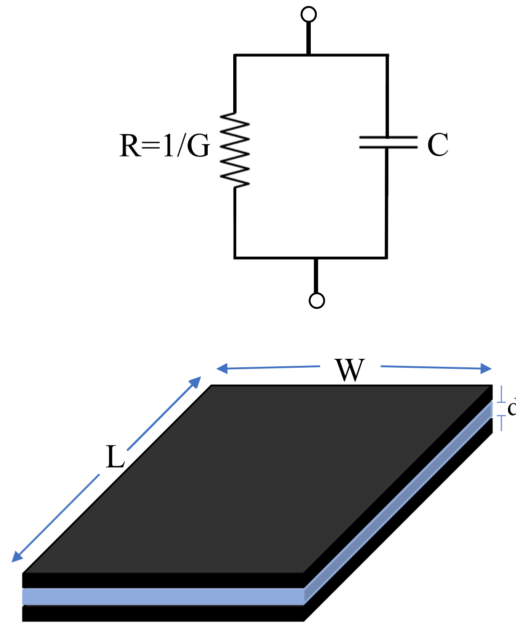


Figure 5.9: Equivalent circuit diagram (top) and structure (bottom) for homogeneous PPE devices.

structure and equivalent circuit model in Figure 5.9 (a), the electrical conductivity σ is calculated as:

$$\sigma = \frac{GT}{WL} \tag{5.6}$$

The conductivity σ can be calculated for each homogeneous (SiO_2, Si_3N_4, and Al_2O_3) PPE device with W = L = 76 μm , and T = 100 nm. These extracted values in Table 5.1 are within an order of magnitude of the approximate electrical conductivity values reported in the literature for SiO_2 (Srivastava, Prasad, and Jr, 1985), Si_3N_4 (Dow, Kim, and Lee, 2017), and Al_2O_3 (Barsoum, 2019), respectively.

As the voltage reaches a high value, however, the PPE structures display highly non-linear characteristics which cannot be easily interpreted using the SCLC model, because in amorphous dielectric films, there are complex, spatially disordered and self-organized microstructures, in which ordered microcrystalline domains are embedded. This implies

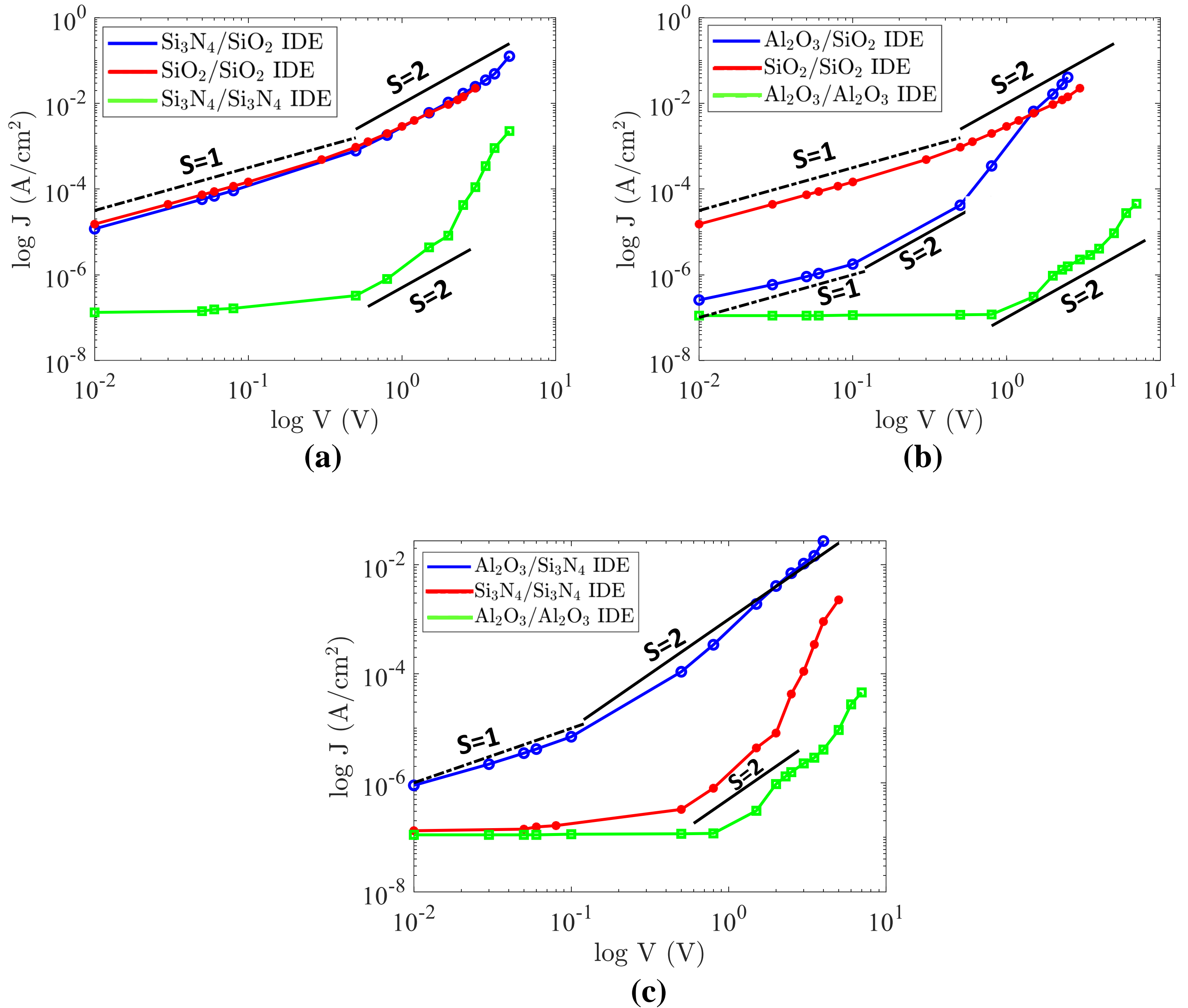


Figure 5.10: The J-V characteristic of IDE devices with (a) Si_3N_4/SiO_2, SiO_2, and Si_3N_4, (b) Al_2O_3/SiO_2, SiO_2, and Al_2O_3, and (c) Al_2O_3/Si_3N_4, Si_3N_4, and Al_2O_3 dielectrics.

Table 5.1: Three homogeneous PPE structures and their respective (approximate) extracted and reported electrical conductivity values.

Structure (Homogeneous PPE)	**σ (pS/m)**	**Reported σ (pS/m)**
SiO_2	36	100
Si_3N_4	27	100
Al_2O_3	20	1

that there is a need for extensive testing and modeling of the nonlinear regions in the SCLC plots. This non-linearity could be the start of a J-V characteristic phase that eventually leads to avalanche breakdown in the PPE devices, which can be characterized accurately using further experimentation and analytical models.

For the J-V characteristics of the IDE structures illustrated in Figure 5.10, it can be seen that almost all the heterogenous IDE structures transition into a non-linear region at lower voltages than their homogeneous IDE constituents, with the exception of the Si_3N_4/SiO_2 IDE structure shown in Figure 5.10 (a). In the J-V characteristic plot shown in Figure 5.10 (b), the heterogeneous Al_2O_3/SiO_2 IDE structure has a significantly lower transition voltage V_{TR}, than homogeneous SiO_2 and Al_2O_3 IDE devices. The same characteristic can also be seen between the heterogenous Al_2O_3/Si_3N_4 and homogeneous Si_3N_4 and Al_2O_3 IDE structures illustrated in Figure 5.10 (c). This suggests that the introduction of a heterogenous dielectric/dielectric interface could lead to higher number of defects such as traps due to dangling bonds, which cause the transition from ohmic to SCLC region to occur at lower voltages.

5.4 Summary and Conclusions

A total number of 84 average I-V measurements have been taken from homogeneous PPE and IDE control test structures and compared to bi-layer PPE and heterogeneous IDE test structures. The PPE homogeneous and bi-layer structures consistently show lower leakage current than their IDE counterparts due to the non-uniformity of the electric field in the IDE structures, in particular at the electrode edges, which leads to higher leakages compared to the constant fields as seen in PPE devices. This could imply that the current mechanisms that are being measured in IDE are electrode-limited at low voltages, which suggests that a different electrode structure is needed for the next phase of this research.

In the heterogeneous IDE devices, both Si_3N_4/SiO_2 and Al_2O_3/SiO_2 structures seem to have superior interfacial properties than the Al_2O_3/Si_3N_4 devices. This is seen in the

comparison of the J-V characteristics of these bi-layer structures with their individual constituent dielectrics, where the Si_3N_4/SiO_2 and Al_2O_3/SiO_2 structures have lower leakage currents compared to the Al_2O_3/Si_3N_4 devices. This shows that in some cases, such as the Al_2O_3/Si_3N_4 structure, the addition of a heterogeneous interface can have adverse effects on leakage behaviour in both PPE and IDE structures. For the other two Si_3N_4/SiO_2 and Al_2O_3/SiO_2 devices and in particular the multilayer encapsulated Si_3N_4/SiO_2 and Al_2O_3/SiO_2 structures, on the other hand, the low leakage characteristic of the interface coupled with high interfacial anomalies extracted in the previous chapters provides a great opportunity to explore these devices further for reliable energy storage purposes. This is despite the fact that none of the PPE or IDE structures in this work have been optimized to improve interfacial characteristics and lower leakage current in these devices. Further testing, characterization and optimization of these PPE and IDE devices can help enhance the interfacial characteristics in these dielectric layers in such structures, which can eventually lead to lower leakage current and improved device reliability for energy storage device design.

CHAPTER 6

PROJECTED ENERGY DENSITY CALCULATIONS OF PPES AND IDES AND IDEAL HIGH-DENSITY DEVICES

6.1 Introduction

Current commercially available electrochemical batteries have the drawback of low power density and a limited number of recharge cycles, which prevent applications that require high power over a short time. Limited recharge cycles can result in high cost for products, and the environmental problems of battery disposal will only get worse as the world continues toward a heavy dependence on electrical energy storage. Furthermore, at the moment, supercapacitors, which currently have about an order of magnitude smaller energy density than lead acid batteries (Wu *et al.*, 2013), have electrodes that can deteriorate, and their electrolytic aqueous solutions may evaporate after several heavy uses (Signorelli *et al.*, 2009). They also have low breakdown voltages that limit the energy density of these devices (Signorelli *et al.*, 2009). In addition, current research in advanced solid-state dielectrics, such as ferroelectric polymers (Sarkar, Ranjith, and Krupanidhi, 2007), superlattices (Singh and Prellier, 2007), and doped ferroelectrics (Ang and Yu, 2007), which has tried to match the energy density of supercapacitors, do not currently have high breakdown field strengths to be reliable alternatives (Ducharme, 2009).

In this chapter, the previously fabricated homogeneous and heterogeneous IDE and PPE devices are investigated in order to utilize them as prospective candidates for energy storage devices. Specifically, a new future device architecture that is made from on-chip PPE structures that utilize the directional interfacial anomalies of very thin (2-5 nm) SiO_2 and Al_2O_3 nanolaminates may have the potential to overcome many of the aforementioned short-comings of current energy storage technologies. Further, it will be shown that if di-

Table 6.1: Measured breakdown voltage values of homogeneous and bi-layer PPE structures.

PPE Structure	Breakdown Voltage [V]
SiO_2	40
Si_3N_4	30
Al_2O_3	43
Si_3N_4/SiO_2	25
Al_2O_3/SiO_2	42
Al_2O_3/Si_3N_4	40

Table 6.2: Measured breakdown voltage values of heterogeneous and multilayer IDE structures.

IDE Structure	Breakdown Voltage [V]
SiO_2	3
Si_3N_4	5
Al_2O_3	7
Si_3N_4/SiO_2	5
Al_2O_3/SiO_2	2.5
Al_2O_3/Si_3N_4	4
5-layer Si_3N_4/SiO_2	3.5
5-layer Al_2O_3/SiO_2	6

electrics can be pushed to the published limits of the electric field strength values, these multilayer devices with ultra-thin nanolaminate layers could produce unusually high volumetric energy density values of up to 1300 J/cm^3 that are several orders of magnitude higher than most current supercapacitors.

6.2 Volumetric Energy Density of Fabricated PPE and IDE Structures

The homogeneous and heterogeneous PPE and IDE structures shown in Fig. 6.1 and 6.2, which have been characterized in Chapter 5 have also been tested for breakdown voltage as shown in Table 6.1 and 6.2, respectively. Further, two other structures with alternating encapsulation layer have also been investigated. These are the alternating Si_3N_4/SiO_2 nanolaminate encapsulated structure from Chapter 4 (Sample 4b) as shown in Figure 6.3 (a) and a heterogeneous Al_2O_3/SiO_2 structure encapsulated with 200 nm of alternating Al_2O_3/SiO_2 layers as illustrated in Figure 6.3 (b).

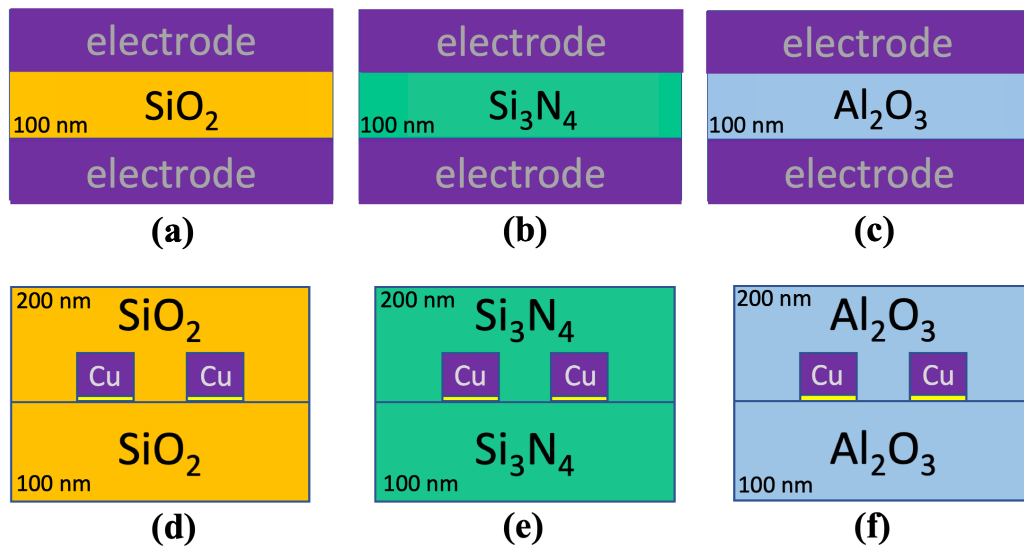


Figure 6.1: Schematic of fabricated homogeneous PPE (a) SiO_2, (b) Si_3N_4, (c) Al_2O_3, and IDE (d) SiO_2, (e) Si_3N_4, and (f) Al_2O_3 devices.

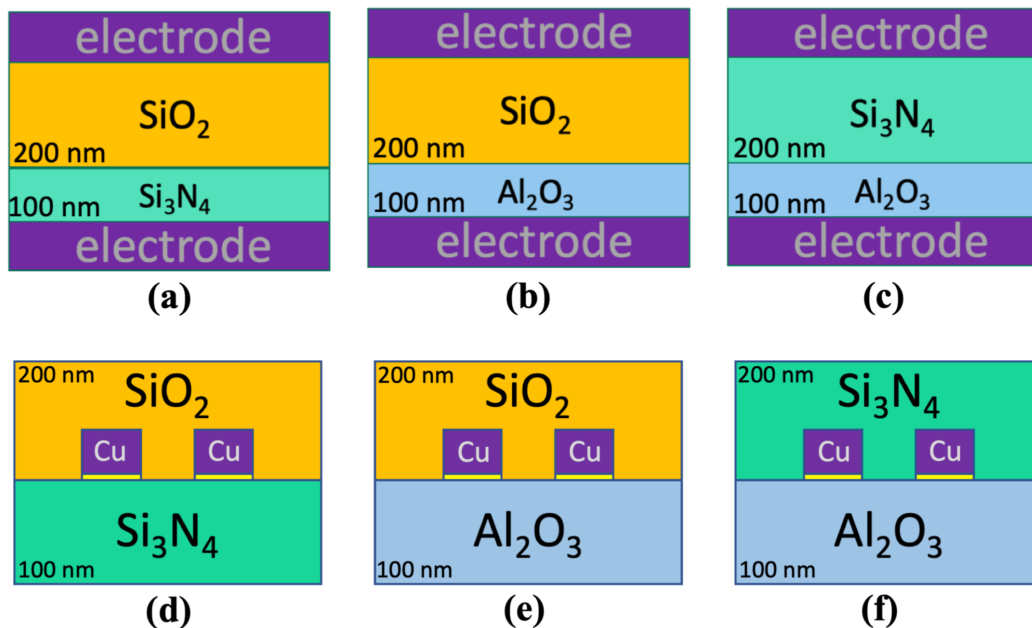


Figure 6.2: Schematic of fabricated bi-layer PPE (a) Si_3N_4/SiO_2, (b) Al_2O_3/SiO_2, (c) Al_2O_3/Si_3N_4, and heterogeneous IDE (d) Si_3N_4/SiO_2, (e) Al_2O_3/SiO_2, and (f) Al_2O_3/Si_3N_4 devices.

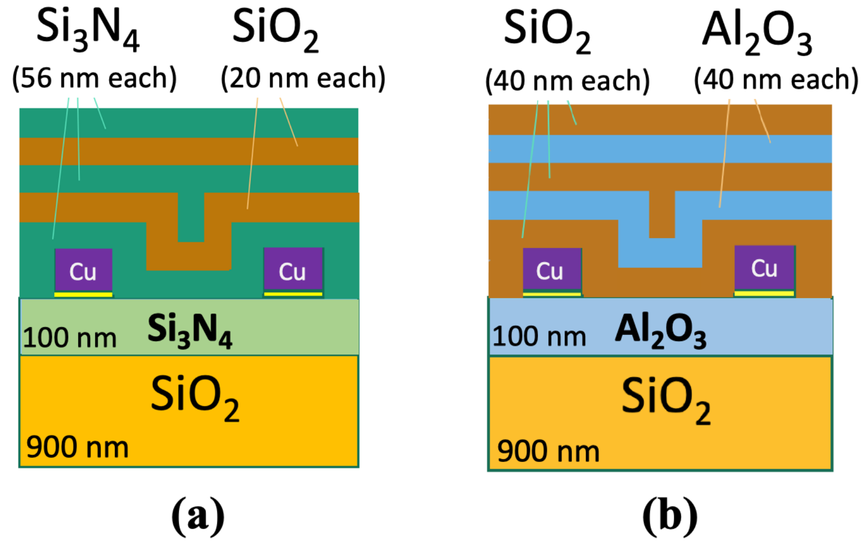


Figure 6.3: Schematic of (a) 100 nm of Si_3N_4/air device encapsulated with 200 nm of alternating Si_3N_4/SiO_2, and (b) 100 nm of Al_2O_3/air structure encapsulated with 200 nm of SiO_2/Al_2O_3 nanolaminate layers.

The onset of dielectric breakdown is generally defined as the failure of an insulator at certain applied voltages V_{bd}, at which there is an abrupt increase in the leakage current flow. The maximum stored energy U can be calculated for each PPE and IDE device using the following equation:

$$U = \frac{\beta^2 C V_{bd}^2}{2}, \tag{6.1}$$

where β is the maximum charging factor. Using the measured C and V_{bd} values from Table 6.2, for the PPEs, at β = 1, the homogeneous PPE structure with Al_2O_3 dielectric has the largest maximum energy capacity as illustrated in Figure 6.1 (c), which is approximately 4.69 nJ (i.e. a volumetric energy density of 8.12 $\mathrm{J/cm^3}$ for a homogeneous PPE volume of 5.78×10^{-10} $\mathrm{cm^3}$). For the PPEs, the bi-layer Si_3N_4/SiO_2 device gives the lowest calculated energy value of 0.32 nJ (i.e. a volumetric energy density of 0.18 $\mathrm{J/cm^3}$ for a bi-layer PPE volume of 1.73×10^{-9} $\mathrm{cm^3}$). Notably, the PPE Al_2O_3 structure has the lowest leakage, lowest conductivity and highest breakdown voltage out of all the other fabricated PPE devices.

For the IDE devices, on the other hand, at β = 1, the lowest energy value is achieved for a homogeneous SiO_2 IDE structure as shown in Figure 6.1 (d), which is approximately 0.048 pJ (i.e. a volumetric energy density of 6.7 $\mu J/cm^3$ for a homogeneous IDE volume of 7.20×10^{-9} cm^3). For the IDEs, the homogeneous Al_2O_3 structure again has the highest energy value of 0.45 pJ (i.e. a volumetric energy density of 62 $\mu J/cm^3$).

To compare the energies of all the devices, the *relative* energy values for the fabricated homogeneous and heterogeneous PPE and IDE structures at β = 1 are plotted in Figure 6.4 and 6.5, respectively. These relative energy values are normalized to the energy of the device with the lowest energy value, which is the bi-layer Si_3N_4/SiO_2 PPE structure in Figure 6.4 and the homogeneous SiO_2 IDE structure in Figure 6.5.

The J-V characteristics that were explored in Chapter 5, the approximate breakdown voltage values for all the fabricated PPE and IDE structures, and the relative energy density values has illustrated that Al_2O_3 is a highly reliable choice of dielectric material for an energy storage device. Further, the addition of SiO_2 on top of Al_2O_3 layer has been shown to create a highly anomalous interfacial region ($k_{Al_2O_3/SiO_2}$ = 2373), where the Al_2O_3/SiO_2 interface does not cause an increase in leakage current as seen in Figure 5.3 (b) and Figure 5.4 (b). The breakdown voltage data for the alternating multilayer encapsulated Al_2O_3/SiO_2 structure shown in Table 6.2 further supports that the addition of multiple Al_2O_3/SiO_2 layers only slightly lowers the breakdown as compared to pure Al_2O_3 samples. Furthermore, the leakage data suggests that the Al_2O_3/SiO_2 interfaces help improve the leakage over pure SiO_2. In fact, generally, it appears as if the bulk SiO_2 may actually limit these devices more than the interfaces themselves. Hence, the energy storage device proposed in this chapter is chosen so that it is composed of thin nanolaminate dielectric layers of Al_2O_3/SiO_2; however, it is in a PPE configuration such that the layers are deposited with interface layers that are *orthogonal* to the metallic electrodes, which allows the highly polarizable interfaces of these layers to be activated more effectively as shown in Figure 6.6.

Figure 6.6 illustrates a theoretical PPE energy storage structure modelled that is sim-

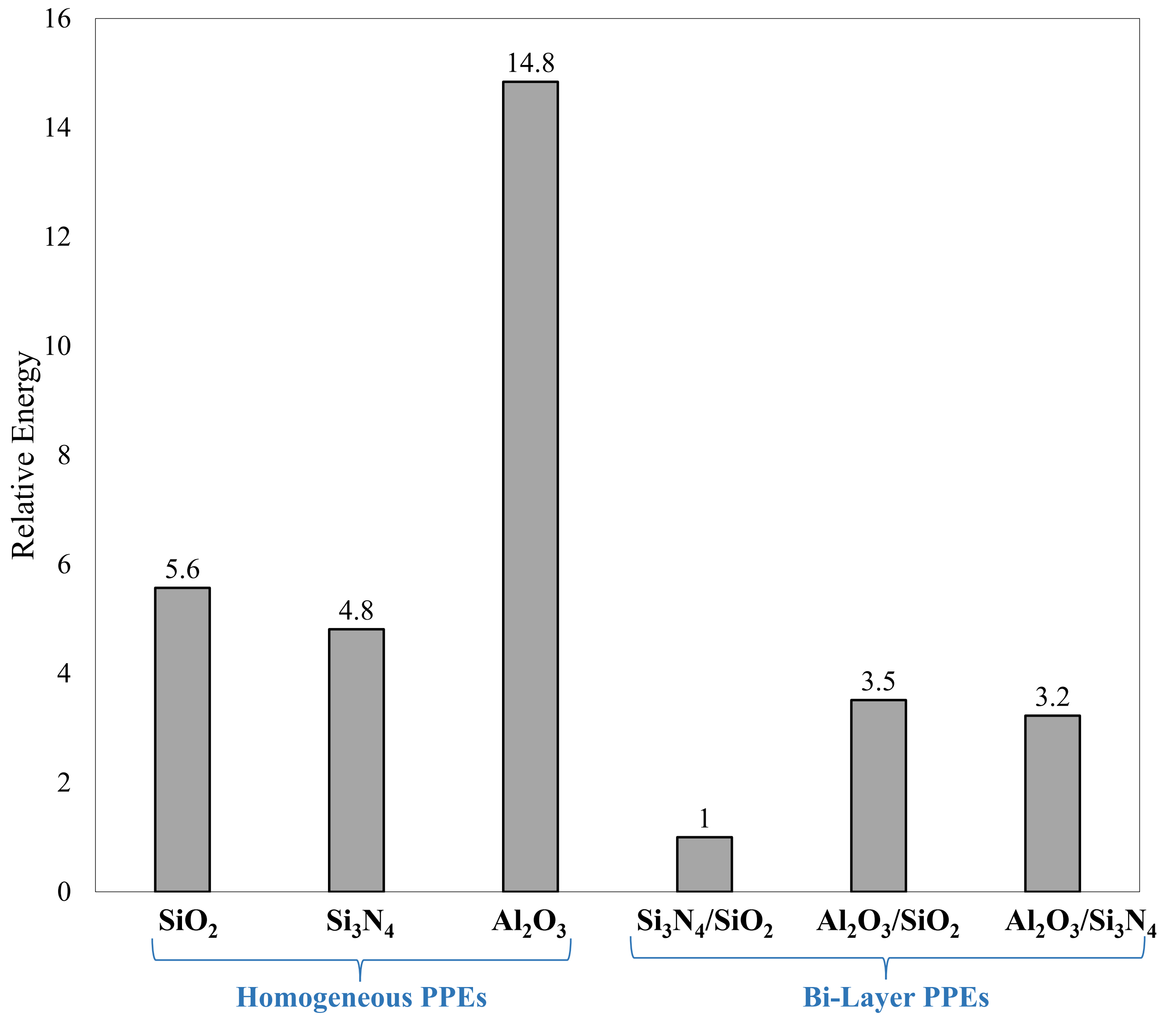


Figure 6.4: Bar graph of relative energy values of homogeneous and bi-layer PPE devices.

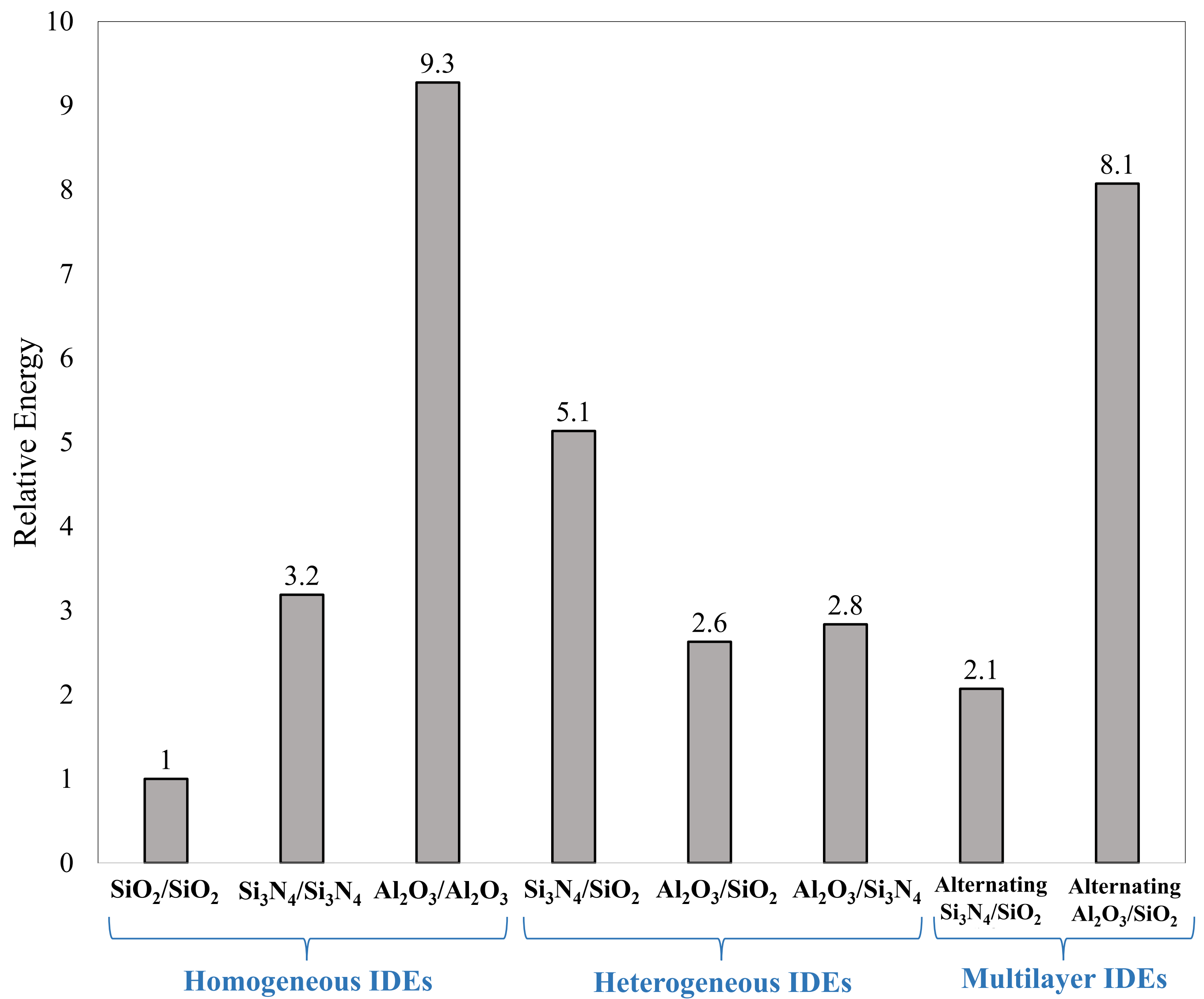


Figure 6.5: Bar graph of relative energy values of homogeneous, heterogeneous, and multilayer IDE devices.

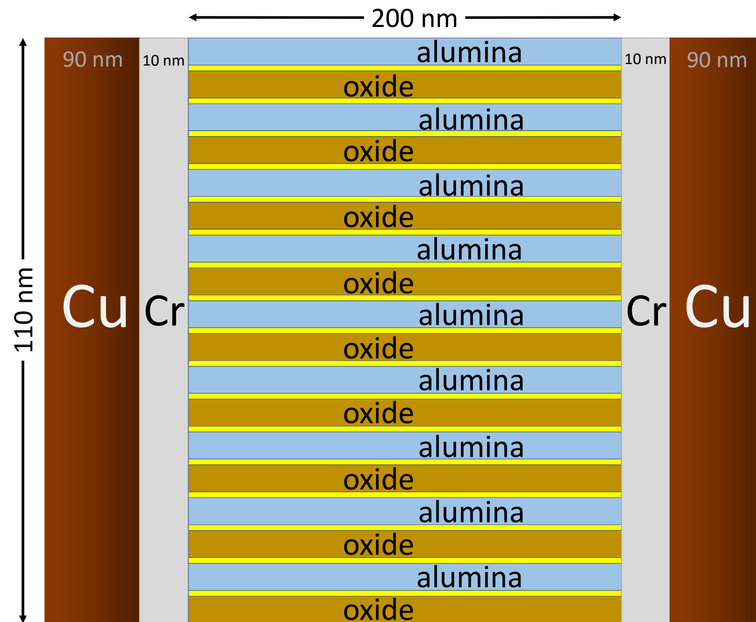


Figure 6.6: FEM model of an 18-layer alternating Al_2O_3/SiO_2 PPE structure with 1 nm high-k interface. Edge effects are eliminated from this simulation so that results can be applied to larger electrode areas.

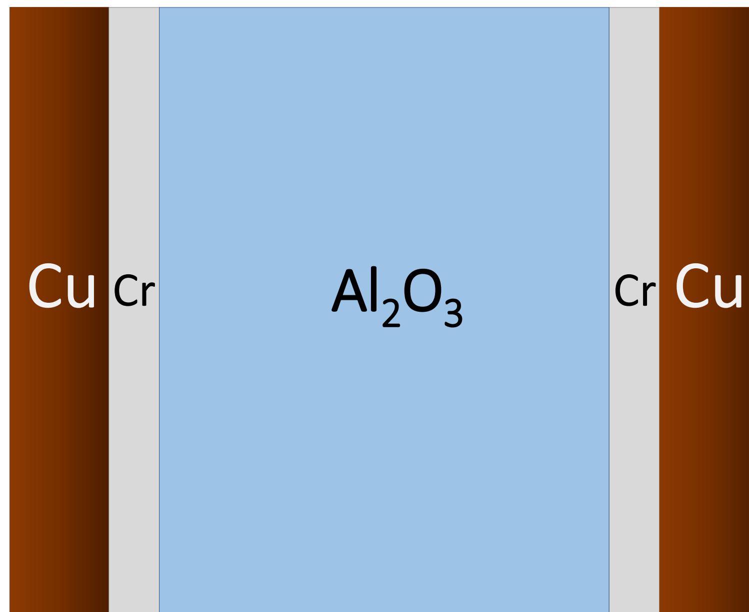


Figure 6.7: FEM model of homogeneous Al_2O_3 control sample.

ulated using COMSOL Multiphysics®, where a total 18 alternating layers of 5 nm SiO_2 (k_{SiO_2} = 4.3) and Al_2O_3 ($k_{Al_2O_3}$ = 9.9) with 1 nm interfacial layer ($k_{Al_2O_3/SiO_2}$ = 2373) are placed between the capacitor electrodes with 200 nm spacing. The maximum storage voltage, V_{max} can be calculated for the PPE configuration shown in Figure 6.6 using:

$$V_{max} = \beta V_{bd} = \beta E_{bd} d, \tag{6.2}$$

where V_{bd} is the breakdown voltage, E_{bd} is the breakdown field strength of the dielectric material, and d is the distance between the electrodes. If the maximum breakdown field strength is comparable to the measurements of SiO_2 in McPherson *et al.* (2002) and Al_2O_3 in Lin, Ye, and Wilk (2005), which are $\sim$ 15 MV/cm and $\sim$ 10 MV/cm, respectively, then V_{bd} for SiO_2 would be $\sim$ 300 V, and for Al_2O_3, it would be $\sim$ 200 V. Here, it will be assumed that the actual breakdown of these materials is approximately half the breakdown strength of the weakest dielectric material in the laminate structure, i.e. β = 0.5. Subsequently, the structure shown in Figure 6.6 is simulated at a maximum voltage V_{Max} = 100 V and the simulated capacitance C including the overhead capacitances for a single IDE energy storage device would be approximately 0.1 pF. The maximum volumetric energy density U_{vol} can be calculated using:

$$U_{vol} = \frac{Energy}{Volume} = \frac{CV_{max}^2}{2} \cdot \frac{1}{device\ volume} \tag{6.3}$$

At V_{max} = 100 V, the maximum obtainable U_{vol} for the energy storage device shown in Figure 6.6 with 5 nm Al_2O_3/SiO_2 multilayers (at β = 0.5) would be approximately **293 $\mathbf{J/cm^3}$**. This volumetric energy storage value is 36 $\times$ higher than that of an energy storage device of the same dimension with homogeneous Al_2O_3 deposited between the electrodes as shown in Figure 6.7.

Figure 6.8 illustrates the maximum obtainable volumetric energy density values for the proposed ideal structure at different dielectric thicknesses (2 - 5 nm) for β = 0.5 and β =

Table 6.3: A comparison of existing energy storage technologies including ideal multilayer PPE with orthogonal dielectrics (based on the data reported by Roundy, Wright, and Rabaey (2003) and Kim *et al.* (2020)).

Technology	**Volumetric Energy [J/cm^3]**
Supercapacitor	10-100
Relaxor ferroelectrics	70-133
Rechargeable batteries	560-1080
Multilayer PPE (β = 0.75)	**659-1303**
Betavoltaic cell	1000-2000
Lithium batteries	2880
Zinc-air batteries	3780

0.75. The volumetric energy densities for a range of β values (0.25 - 1) have also been plotted as shown in Figure 6.9. These values are currently on par or even higher than most reported volumetric energy storage density values. Researchers in Hou *et al.* (2017) have revealed that $SrTiO_3$ (STO) films grown on $La_{0.67}Sr_{0.33}MnO_3$ (LSMO) electrodes could have energy densities up to 307 J/cm^3. Relaxor ferroelectric thin films have been shown to hold energy storage densities as high as 133 J/cm^3 (Kim *et al.*, 2020), and the authors in Pan *et al.* (2018) have reported that energy densities of 70 J/cm^3 can be achieved in lead-free bismuth ferrite-strontium titanate solid-solution films.

Other possible energy density comparisons of this newly proposed multilayer PPE device (at β = 0.75) with current battery technology (Diao *et al.*, 2020; Li *et al.*, 2020; Kong *et al.*, 2020; Jiang *et al.*, 2019; Roundy, Wright, and Rabaey, 2003) and the most recent energy storage materials is shown in Table 6.3, which reveals that this newly proposed energy storage device with ultra-thin (ranging from 2 nm to 5 nm) dielectric layers could have the potential to be a transformative energy storage technology. This is because such a device would have the unprecedented combination of high energy density, high power density, and high longevity that could impact a broad range of energy storage applications in a fast, efficient and reliable manner.

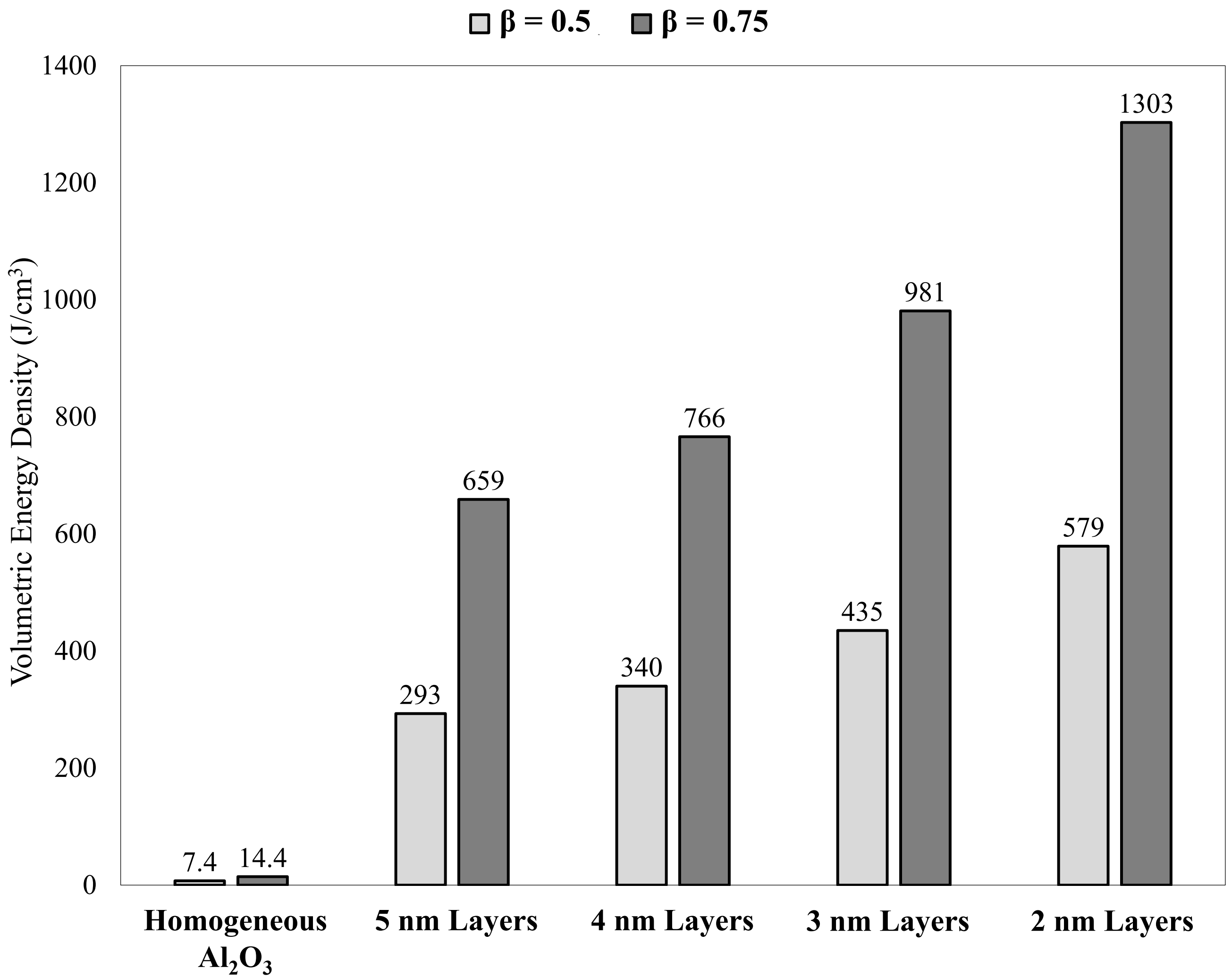


Figure 6.8: Bar graph of simulated capacitance values for a homogeneous Al_2O_3 and an ideal multilayer Al_2O_3/SiO_2 PPE structure with different dielectric thickness values (2 - 5 nm) for $\beta = 0.5$ and $\beta = 0.75$.

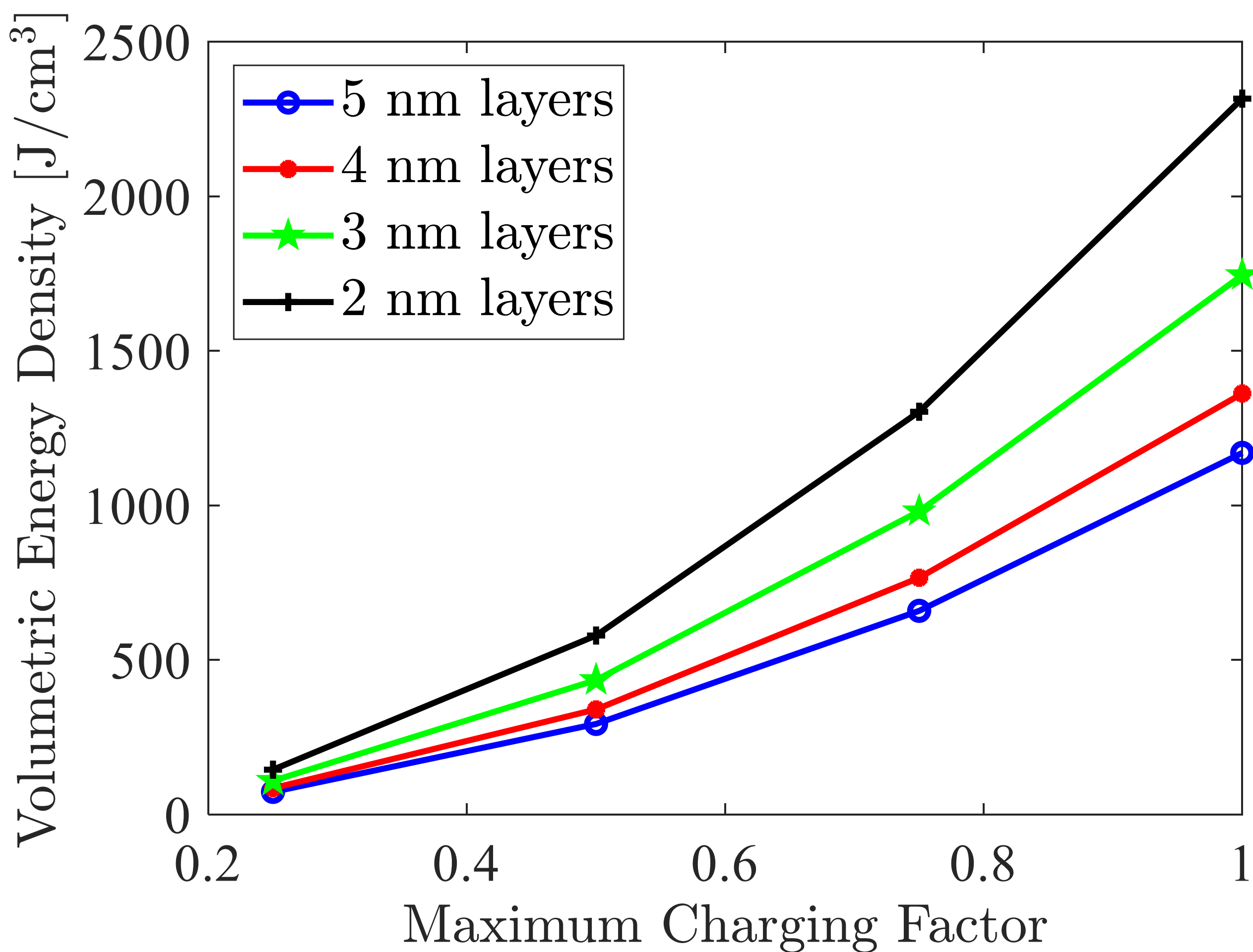


Figure 6.9: Plot of different maximum charging factor values vs maximum projected volumetric energy densities for multilayer Al_2O_3/SiO_2 PPE structures with different dielectric thickness values.

CHAPTER 7

SUMMARY AND CONCLUSIONS

Current research on ($\sim$ 20 nm) SiO_2, Si_3N_4 and Al_2O_3 nanopowders (NPs) has revealed anomalous increases in permittivity over conventional bulk values due to localized dipole polarization effects on the surface of these NP particles (Mo, Zhang, and Wang, 1995; Tepper and Berger, 1999; Zhang *et al.*, 1996). The research in this dissertation has proposed alternative material structures, which are constructed using nanolithographic techniques to explore the high-polarization surface effects seen in NP research. This work has particularly focused on demonstrating and modelling anomalous behavior of the permittivity of nanolaminate devices constructed from a combination of SiO_2, Si_3N_4 and Al_2O_3 materials. The author of this dissertation has successfully developed an efficient and new method to characterize the impact of average dipole density and polarizability that can develop at dielectric/air surfaces and between dielectric/dielectric interfaces of the aforementioned dielectrics in both IDE and PPE configurations.

In the initial part of this work, it was shown that strong surface dipole formation leads to high average permittivity at the air interfaces of SiO_2, Si_3N_4 and Al_2O_3. Specifically, the behavior at these interfaces were studied to identify the average surface permittivity values over a specified volume. Using electrical measurements from a high density in-plane IDE structure and quasi-electrostatic FEM simulation models, an average relative permittivity within a 1 nm interfacial region at 1 kHz was extracted to be $k_{SiO_2/Air} \sim 323$, $k_{Si_3N_4/Air} \sim 58$, and $k_{Al_2O_3/Air} \sim 160$.

However, because air breaks down at low electric fields, the aforementioned devices were encapsulated using different combinations of 200 nm SiO_2 and Si_3N_4 layers in IDE configurations, and subsequent measurements and modelling were applied. Significant deviations in capacitance in IDE structures were measured, and these deviations are attributed

to the presence of the interface. It is believed that variations in dipole and bond formations that occur at the interfaces between the nanolaminate layers are the primary cause of the surprising increase in capacitance. Furthermore, in the IDE geometry, the nanolaminate structures have electric fields that are parallel to the dielectric interfaces, which could activate the highly polarizable interfacial regions more effectively than the traditional PPE structures. In fact, to support this claim, the PPE devices fabricated in this research do not show any anomalous permittivity component in the direction normal to the interface.

As stated, the capacitance measurements in this work illustrate that there is an anomalously high capacitance for devices with just a single heterogeneous interface of Si_3N_4/SiO_2, Al_2O_3/SiO_2 or Al_2O_3/Si_3N_4 that are between the electrodes of an IDE capacitor. Combining these experimental measurements with FEM simulation models, the average permittivities within a 1 nm thick volume at the interfaces of Si_3N_4/SiO_2, Al_2O_3/SiO_2 and Al_2O_3/Si_3N_4 are extracted to be $k_{Si_3N_4/SiO_2}$ = 1419, $k_{Al_2O_3/SiO_2}$ = 2373 and $k_{Al_2O_3/Si_3N_4}$ = 428, respectively. This result is contrary to conventional and fabricated PPE structures with the same bi-layer dielectrics in between the electrodes, where there is no anomalous increase in the measured capacitance.

It was further shown that the addition of multilayer encapsulation layers, such as a five layer Si_3N_4/SiO_2 nanolaminates, can have a significant impact on the interfacial characteristics and extracted permittivity. For example, the Si_3N_4/SiO_2 layers in the alternating encapsulation device has been shown in this work to have significantly higher interfacial permittivity ($k_{Si_3N_4/SiO_2}$ = 2986) than the bi-layer Si_3N_4/SiO_2 structure ($k_{Si_3N_4/SiO_2}$ = 1419). It is proposed that this could be due to stresses that build up in the multilayer structure. This result highlights the opportunities for further investigation of the impact of different stress mechanisms on bulk and interfacial permittivity characteristics using experimentation and simulation modeling.

Because the materials in this study inherently have high breakdown field strengths there is a potential energy storage opportunity for future capacitive devices that utilize these ex-

perimental observations and simulation results. For example, preliminary projections indicate that capacitive devices with a high-density of nanolaminates with laminate thicknesses from 2-5 nm could produce devices with volumetric energy densities that are on a much higher range (i.e. 650-1300 J/cm^3) than conventional electrochemical double layer supercapacitors (i.e. 10-100 J/cm^3).

7.1 Future Work

7.1.1 Investigation of the Impact of Annealing and Heat Cycles on Interfacial Permittivity

The interfaces between SiO_2, Si_3N_4, and Al_2O_3 dielectric films contain various types of defects including dangling bonds that can act as space charge traps and enhance interfacial polarizability as seen in this research. Exposure of such interfaces to different temperatures and so-called heat cycles can significantly impact interfacial permittivity and polarizability. Specifically, it has been observed in literature that exposure of interfacial dangling bonds to high temperatures can cause diffusion of hydrogen, which can eventually lead to a reduction in interfacial permittivity. As part of future work, this phenomena can be explored in heterogeneous bi-layer devices in IDE configuration as well as in multilayer nanolaminates of these dielectric materials, where increasing temperature can have even more pronounced effects on interfacial permittivity due to the complex changes in device stress profiles and hydrogen content. Using previous experimental and simulation results, further extensive testing and TEM, XRD, Ion-TOF and other characterization tools available, new FEM models could be devised in the near future to accurately explore, represent and capture such phenomena.

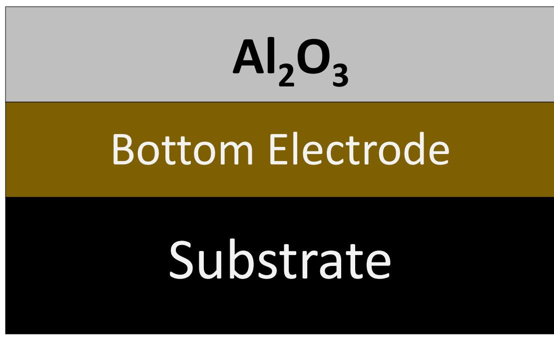
7.1.2 Further Exploration of Electrical Conduction Mechanisms in IDE and PPE Devices

In order to accurately measure and model the breakdown voltage of nanolaminate structures, it is crucial to have a good knowledge and understanding of the dominating conduction mechanisms at high electric fields as well as different temperatures. SCLC mecha-

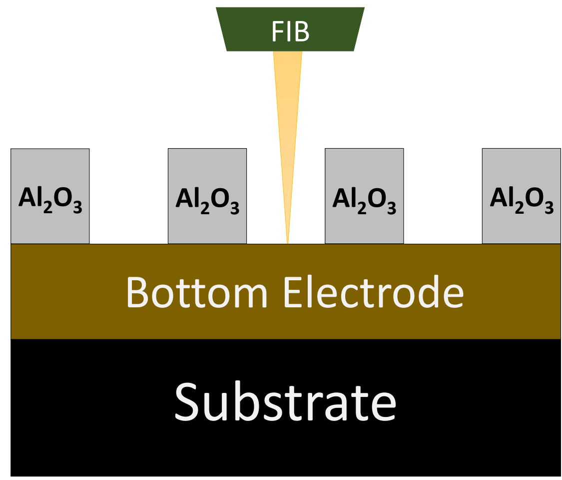
nisms at room temperature were briefly discussed in this work; however, due to the unpredictable nature of amorphous materials in particular in bi-layer and multilayer structures, it is very difficult to interpret the nonlinear regimes of SCLC mechanism. Therefore, it is necessary to further test the fabricated homogeneous and heterogeneous IDE and PPE devices under high temperatures to accurately determine the breakdown voltage and other types of conduction mechanisms that are present. For example, at high temperatures, the calculated permittivity from the Schottky and Poole-Frenkel conduction equations can be compared with experimentally measured permittivity to see if they match. The presence of other bulk-limited and electrode-limited conduction mechanisms can also be explored in future experiments.

7.1.3 Optimization of Multilayer Nanolaminates for High-Density Energy Storage Devices

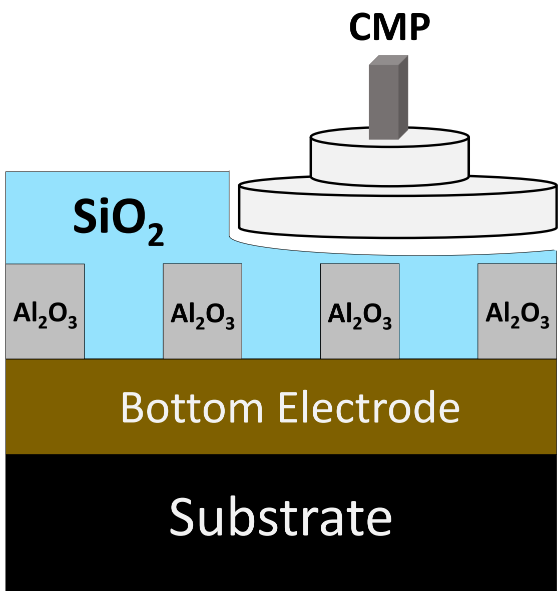
Finally, future work will look into experiments that can identify the source of the observed permittivity anomalies and explore ways to utilize and optimize them for practical energy storage purposes. Figure 7.1 illustrates a summary of the fabrication steps for a PPE Al_2O_3/SiO_2 energy storage device. In the proposed fabrication process, high-precision focused ion beam (FIB) technology will be used to make gratings in the Al_2O_3 layer as shown in Figure 7.1 (b). Further, chemical-mechanical planarization (CMP) methods will be used to polish down the SiO_2 layer as depicted in Figure 7.1 (c). Capacitive energy storage devices made from a large number of such PPE structures that utilize the directional interfacial anomalies of thin SiO_2 and Al_2O_3 nanolaminates may have the potential to overcome many of the shortcomings of current energy storage technologies. The configurations of such PPEs with orthogonally-oriented dielectric layers could facilitate the fabrication of small energy storage devices that integrate well with other microelectronic devices mounted on planar integrated circuits.



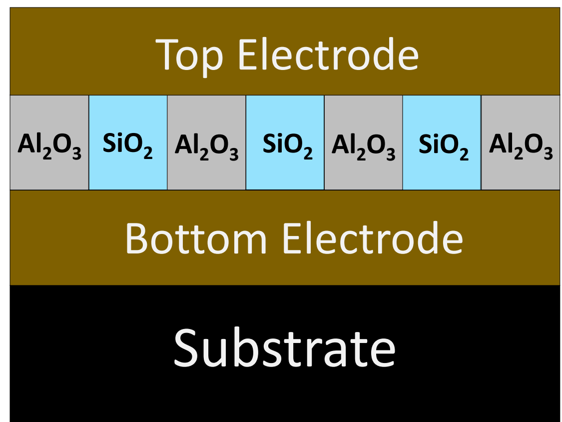
(a) Bottom electrode and Al_2O_3 deposition



(b) Making grating cuts in the Al_2O_3 layer using focused ion beam (FIB)



(c) SiO_2 deposition and chemical-mechanical planarization (CMP)



(d) Top electrode deposition

Figure 7.1: Summarized fabrication steps of a future Al_2O_3/SiO_2 energy storage device.

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