RADIO FREQUENCY AND MILLIMETER WAVE CIRCUIT COMPONENT DESIGN WITH SIGE BICMOS TECHNOLOGY

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RADIO FREQUENCY AND MILLIMETER WAVE CIRCUIT COMPONENT DESIGN WITH SIGE BICMOS TECHNOLOGY

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SUMMARY

The objective of this research is to study and leverage the unique properties and advantages of silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) integrated circuit technologies to better design radio frequency (RF) and millimeter wave (mm-wave) circuit components. With recent developments, the high yield and modest cost silicon-based semiconductor technologies have proven to be attractive and cost-effective alternatives to high-performance III-V technology platforms. Between SiGe bipolar complementary metal-oxide-semiconductor (BiCMOS) technology and advanced RF complementary metal-oxide-semiconductor (CMOS) technology, the fundamental device-level differences between SiGe HBTs and field-effect transistors (FETs) grant SiGe HBTs clear advantages as well as unique design concerns. The work presented in this dissertation identifies several advantages and challenges on design using SiGe HBTs and provides design examples that exploit and address these unique benefits and problems with circuit component designs using SiGe HBTs.

The following is a summary of the contributions of this research:

1. A detailed analysis of the benefits of SiGe HBT technologies versus traditional semiconductor technologies, with focuses on the comparison of advanced RF CMOS and SiGe BiCMOS technologies.
2. The design and demonstration of high-performance bi-directional amplifiers exploiting the superior transconductance/ area property of SiGe HBTs through a loss-compensated X-band phase shifter [1] and a 28 GHz differential bi-directional amplifier (BDA) [2]. These two designs were presented in the 2017 IEEE Radio

Frequency Integrated Circuits Symposium © 2017 IEEE and published in the August 2018 issue of the IEEE Microwave and Wireless Components Letters © 2018 IEEE, respectively.

3. A wideband logarithmic power detector utilizing the exponential *I-V* characteristics of SiGe HBT with temperature compensated bias circuitry. This work was presented in the 2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium [3] © 2019 IEEE.
4. The design and demonstration of novel biasing techniques in SiGe BiCMOS RF switch design for improved performance, illustrated by a high power 60 GHz single-pole double-throw (SPDT) switch and a W-band SPDT switch performance comparison using grounded-emitter vs. floating-emitter reverse-saturated SiGe HBTs. The 60 GHz SPDT switch was presented in the 2019 IEEE Radio Frequency Integrated Circuits Symposium [4] © 2019 IEEE, and the W-band SPDT switch performance study has been submitted to the 2021 IEEE/ MTT-S International Microwave Symposium [5].
5. A 60 GHz high power SiGe differential common-emitter power amplifier with novel three-conductor transmission-line-based Wilkinson baluns and asymmetric directional couplers, exploiting the multi-layered back end of line (BEOL) offered by advanced SiGe BiCMOS technology. This work was presented in the 2020 IEEE/ MTT-S International Microwave Symposium [6] © 2020 IEEE and is to be published in the IEEE Transactions on Microwave Theory and Techniques [7] © 2020 IEEE.

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CHAPTER 1. INTRODUCTION

1.1 Silicon-Based Radio Frequency and Millimeter Wave Technologies

Since the first demonstration of silicon integrated circuit (IC) in 1960, tremendous efforts and innovations have pushed the advancement of silicon-based semiconductor technology at a revolutionary pace. Initially driven by the need for digital complementary metal-oxide-semiconductor (CMOS) switching speed and device density improvement, innovations in CMOS technology provided strong basis and helped the development of silicon-based platforms, such as silicon-germanium (SiGe) bipolar CMOS (BiCMOS) and RF silicon on insulator (SOI), which opened their way for use in the emerging radio frequency (RF) and millimeter wave (mm-wave) applications [8]. The need for highly integrated and cost-effective advanced modern RF and mm-wave radar and communication systems has led to a significant effort in the development of silicon semiconductor platforms as competing alternative to the traditionally dominating III-V compound semiconductor technologies [9].

With additional device, process, and modelling optimization, RF CMOS technologies benefitted greatly from the aggressive digital CMOS scaling that drastically improved transistor switching speed. In recent years, there has been growing interests in further bulk CMOS scaling to move from a planar device to a fin field-effect transistor (FinFET) [10]. However, RF performance of advanced RF CMOS technologies does not scale as well as digital CMOS due to the high sensitivity to layout parasitic resistance and capacitance from device structure, substrate, and BEOL [11]. Other than device scaling, engineering innovations such as SOI [12], the use of high-k dielectric, the introduction of

mobility stressor, and etc. [13] have also pushed the performance of advanced RF CMOS technologies further.

SiGe BiCMOS, on the other hand, has entered the commercial market at a much later time compared to RF CMOS. However, since the first commercially available SiGe HBT platform [14], the tremendous generational growth of SiGe HBT technologies has led to an increasing presence of SiGe BiCMOS platforms in various modern RF and mm-wave applications. In SiGe BiCMOS technologies, SiGe HBTs are normally added to a lagging edge CMOS node, with additional process optimization. While the unity gain cutoff frequency (f_T) performance of CMOS depends greatly on lateral scaling, the f_T improvement of SiGe HBT is primarily driven by vertical scaling [8]. Current state-of-the-art SiGe BiCMOS platforms offers an f_T of 505 GHz and a maximum oscillation frequency (f_{MAX}) of 720 GHz at room temperature [15].

1.2 Technology Device Performance Comparison

The choice for semiconductor technologies needs to be made specific to application. For applications requiring significant portion of logic and lower-power operations, a bulk CMOS technology that is suit for an integrated solution with high-density and low-cost becomes the clear winner. However, for high performance RF and mm-wave front-end designs, CMOS technologies can appear limiting, and a dis-integrated solution with a combination of different platforms is more practical. Therefore, a comparison among the available semiconductor technologies is very informative.

Given the diverse choices of SiGe BiCMOS, RF CMOS, and III-V technologies, reaching a sweeping generalization of the performance differences among them is

inevitably unfair, if not impossible. Nonetheless, some general observations of the differences are helpful to better understand the advantages and disadvantages associated with each device technology. Authors in [9] summarized a relative comparison of the performance metrics of various device technologies as shown in Table 1.1.

Table 1.1 – Relative Performance Comparisons of Various Device Technologies for RFICs (Excellent: ++; Very good: +; Good: 0; Fair: -; Poor: --) [9]

Performance Metric	***SiGe HBT***	***Si BJT***	***Si CMOS***	***III-V MESFET***	***III-V HBT***	***III-V HEMT***
Frequency response	+	0	0	+	++	++
1/f and phase noise	++	+	-	--	0	--
Broadband Noise	+	0	0	+	+	++
Linearity	+	+	+	++	+	++
Output conductance	++	+	-	-	++	-
Transconductance/ area	++	++	--	-	++	-
Power dissipation	++	+	-	-	+	0
CMOS integration	++	++	N/A	--	--	--
IC cost	0	0	+	-	-	--

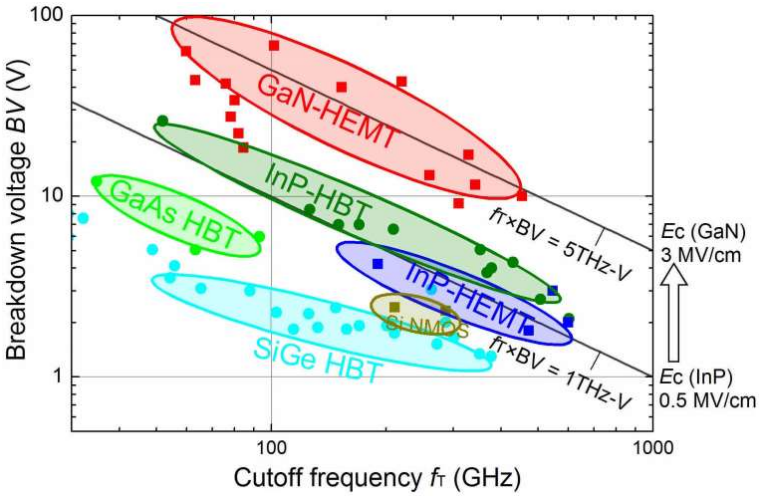


Figure 1.1 – A technology survey in 2013 comparing the state-of-the-art semiconductor technologies in the breakdown voltage vs. f_T trade space [16] © 2013 IEEE.

From a pure device performance perspective, III-V technologies in general are superior compared to silicon-based technologies, as shown by the survey comparing the state-of-the-art semiconductor technology in the breakdown voltage vs. f_T trade space in Figure 1.1, [16]. For sub-terahertz, ultra-wide band, high power, or mission-critical applications, III-V technologies are undoubtedly favored for their device RF characteristics [17], [18]. Though falling behind in device performance, SiGe BiCMOS and RF CMOS technologies outshine III-V technologies from low cost, high yield, and high-level integration perspectives. As a result, there has been increasing interests in advanced RF CMOS and SiGe BiCMOS technologies as potential candidates for the optimization of performance, system size, and die cost [19].

Comparing among Si-based technologies, the state-of-the-art SiGe HBTs offer better frequency response over aggressively scaled RF-CMOS both on bulk Si and SOI. However, both advanced SiGe BiCMOS and RF-CMOS technologies offers device featuring f_T and f_{MAX} close to, or higher than, 300 GHz, which meets the need of significant portion of the RF and mm-wave applications. Perhaps, instead of comparing the best of SiGe BiCMOS and RF-CMOS technologies, comparison studies between SiGe BiCMOS and RF-CMOS technologies with similar f_T and f_{MAX} are more relevant.

1.2.1 Device Noise Performance for Low Noise Amplifier (LNA) Design

When first introduced to the market, SiGe HBTs demonstrated superior device noise performance compared with RF CMOS technologies. This gap was soon closed by the rapid scaling of RF CMOS. In modern low noise applications, both SiGe BiCMOS and RF CMOS technologies are heavily utilized. The device noise performance comparison

between SiGe HBT and RF CMOS has been commented on by various researchers and engineers.

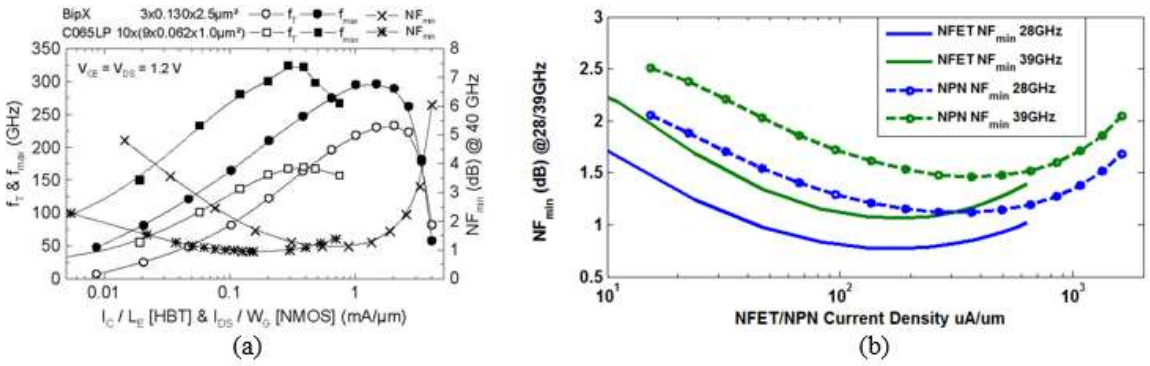


Figure 1.2 – (a) Measured f_T, f_{MAX} and NF_{min} at 40 GHz vs. current density for BipX and 65 nm LP NMOS [20] © 2006 IEEE, and (b) NF_{min} comparison between GLOBALFOUNDRIES 40 nm 45RFSOI and 130 nm SiGe HBT [23] © 2018 IEEE.

The minimum noise figure NF_{min} is an important parameter used to assess the performance of transistor devices. P. Chevalier *et al.* [20] presented performance comparison of a 130-nm SiGe HBT technology based "BipX" [21], and a bulk 65 nm LP NMOS C065LP [22]. The f_T, f_{MAX}, and NF_{min} of the two devices against current density are plotted as shown in Figure 1.2(a). The minimum noise figure measured from the NMOS device is slightly better than that from the HBT. Similar results are also shown by C. Li *et al.*, by comparing simulated NF_{min} of GLOBALFOUNDRIES 45 nm RFSOI NFET and high performance 130 nm SiGe HBT, for Ka band front-end module (FEM) applications [23], shown in Figure 1.2(b). Both studies suggest that, for SiGe BiCMOS and RF-CMOS technologies with similar frequency responses, the RF CMOS technologies offer slightly better NF_{min} performance. As pointed out by authors in [20], the slight inferior noise performance of HBT in above cases could be explained by a higher noise resistance R_n ([24], [25]) which results from lower device development compared to RF-CMOS

technologies. Therefore, RF-CMOS technologies could potentially promise amplifier designs with lower noise figure than those designed using SiGe HBTs of comparable or higher f_T and f_{MAX}.

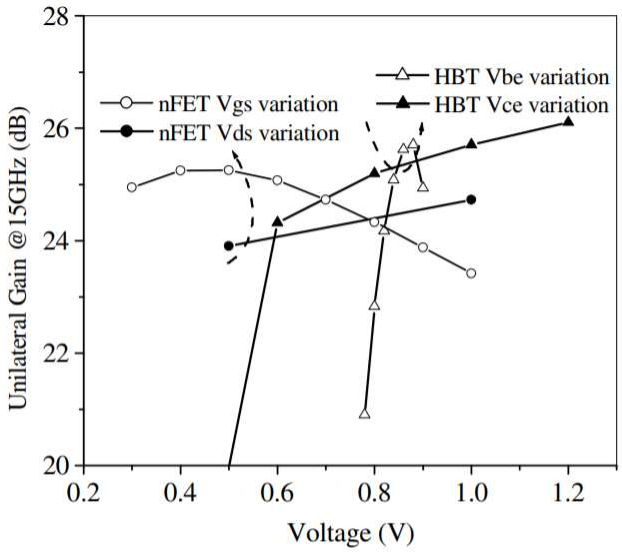


Figure 1.3 – Comparison of unilateral gain vs. V_{gs} (V_{be}) and V_{ds} (V_{ce}) between a 130 nm SiGe BiCMOS and 90 nm bulk RF CMOS technology [26] © 2004 IEEE.

A key advantage of nFET compared to SiGe HBT is its ability to attain high f_T and transconductance (g_m) at low current density, as emphasized by a comparison study between a 130 nm SiGe BiCMOS and a 90 nm bulk RF CMOS technology in [26]. This property of nFET and the nFET's ability to sustain reasonable gain at more aggressively lowered supply voltage compare to SiGe HBT [26], as illustrated in Figure 1.3, make RF CMOS technology more attractive for LNA designs with tight power consumption constraint.

Although RF CMOS can potentially promise better noise performance compared to SiGe HBT, more meticulous layout optimization is required when designing with RF CMOS. In a FET, noise can be primarily attributed to drain to source conductance and gate

resistance, whereas the base-emitter junction shot noise is the primary noise source in SiGe HBT. One important implication of this difference is the difference in sensitivity of noise to circuit layout. Under device size, power consumption, and passive matching constraints, to optimize the noise performance in a RF CMOS design, the total gate length of the FET needs to be maximized to increased conductance but carefully partitioned to minimize the gate resistance. Noise performance of SiGe HBT, on the other hand, is insensitive to emitter length partitioning, as long as the base contact is well designed. As pointed out by S. Voinigescu in [24], this strong layout dependence, together with the high quality factor of the MOSFET input and noise impedances, make CMOS LNAs more sensitive to process variations, impedance mismatch, and model inaccuracy.

1.2.2 Device Comparison for RF and mm-wave Switch Applications

RF switches are essential components in a RF and mm-wave system as they enable transmit/ receive mode toggling, circuit reconfiguration, and performance calibration. In silicon-based technologies, high performance RF switching is achieved through using MOSFETs, SiGe HBTs, or SiGe PIN diodes in series and/ or shunt configurations. Using front-end switch as an example, the series-shunt topology is often adopted for applications operating from DC to lower mm-wave frequencies, with the series device being the main switching device and the shunt device included for enhanced isolation. The series-shunt topology has been successfully demonstrated with FETs, SiGe HBTs, and diodes [27]-[29]. For applications operating at much higher frequencies, the quarter-wave shunt topology is more often used to mitigate the loss from the series switching device [30]-[32]. However, regardless of the choice of topology or the intended frequency of operation, RF switch

designs share similar trade-offs and considerations which determines the choice of device technology and sizing.

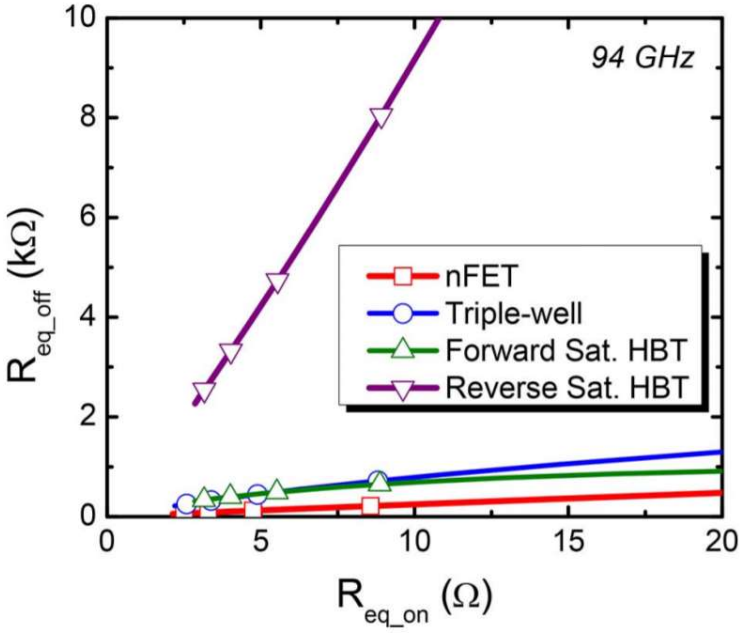


Figure 1.4 – Comparison of equivalent OFF impedance vs. ON impedance for available shunt switching device configurations in GlobalFoundries 90 nm 9HP SiGe BiCMOS technology at 94 GHz [30] © 2014 IEEE.

Two importance device metrics that gauge how well a device can pass or block signal when it is turned ON or OFF are the ON resistance (R_{ON}) and OFF capacitance (C_{OFF}). Given any choice of device technology, the most effective way to reduce R_{ON} is to increase the switching device periphery, at the cost of increased substrate coupling which reduces the effective OFF impedance. The substrate parasitic conduction loss is a significant limiting factor in bulk CMOS and SiGe BiCMOS switch design. When used as a shunt switching device, a reverse-saturated SiGe HBT demonstrates superior effective OFF impedance for a given R_{ON} compared to other bulk silicon transistors, as shown in Figure 1.4 [30]. Since the physical SiGe HBT structure isolates the emitter from the

substrate, most of the substrate loss in SiGe HBT comes from the collector to substrate network. The superiority of a reverse-saturated SiGe HBT when used as a shunt switching device, therefore, results from the fact that it's collector is grounded. When used as a series switching device, SiGe HBT also presents low substrate parasitics compared to a bulk CMOS FET [29]. For silicon-based devices on insulator, however, the issue of substrate loss is largely mitigated. Figure 1.5 compares the ON resistance of a bulk SiGe BiCMOS 240 nm FET with a 40 nm 45RFSOI FET over frequency [23], clearly demonstrating the advantage of SOI over bulk silicon for switch applications. Although SiGe HBT on insulator is commercially available [33], it is much less common compared to CMOS on SOI due to the aggravated electro-thermal and reliability concerns the insulator brings for SiGe HBT [34], [35].

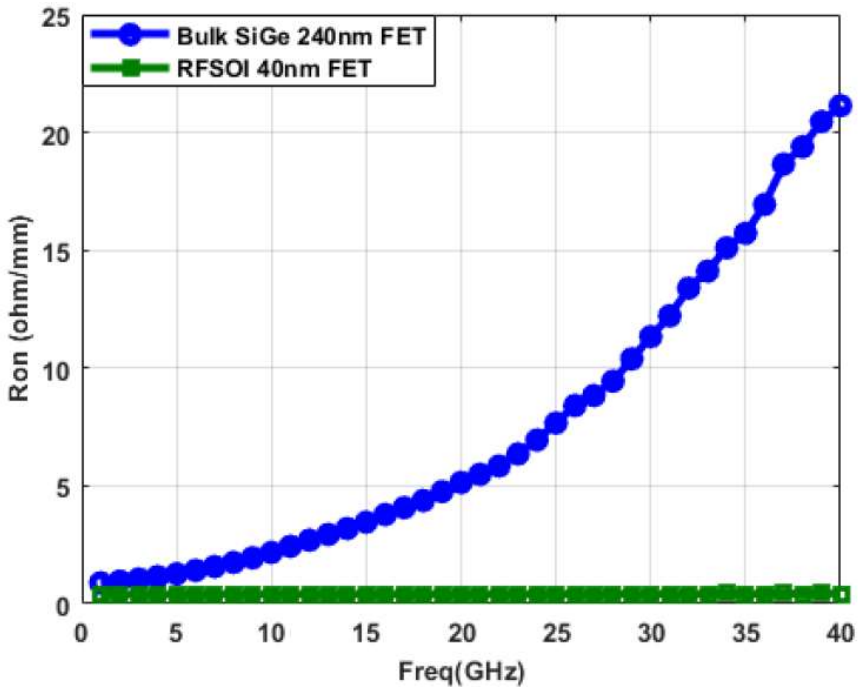


Figure 1.5 – Measured effective R_{ON} comparison of BiCMOS 240 nm FET (blue) and 45RFSOI 40 nm FET (green) [23] © 2018 IEEE.

From the power handling capability perspective, the fact that SiGe HBTs in general have turn-on voltages much higher than the threshold voltage of FETs enables SiGe HBTs to handle much higher voltage swing before they start to compress [30]. In addition, some SiGe BiCMOS technologies also offer SiGe PIN diode optimized for mm-wave switch applications that has high turn-on voltage, high breakdown, and superior performance [36]. However, although a single FET can handle less voltage swing compared to a single SiGe HBT or a single SiGe PIN diode, this disadvantage of FETs can be easily overcome through device stacking [23], a common practice especially suited for RFSOI technologies.

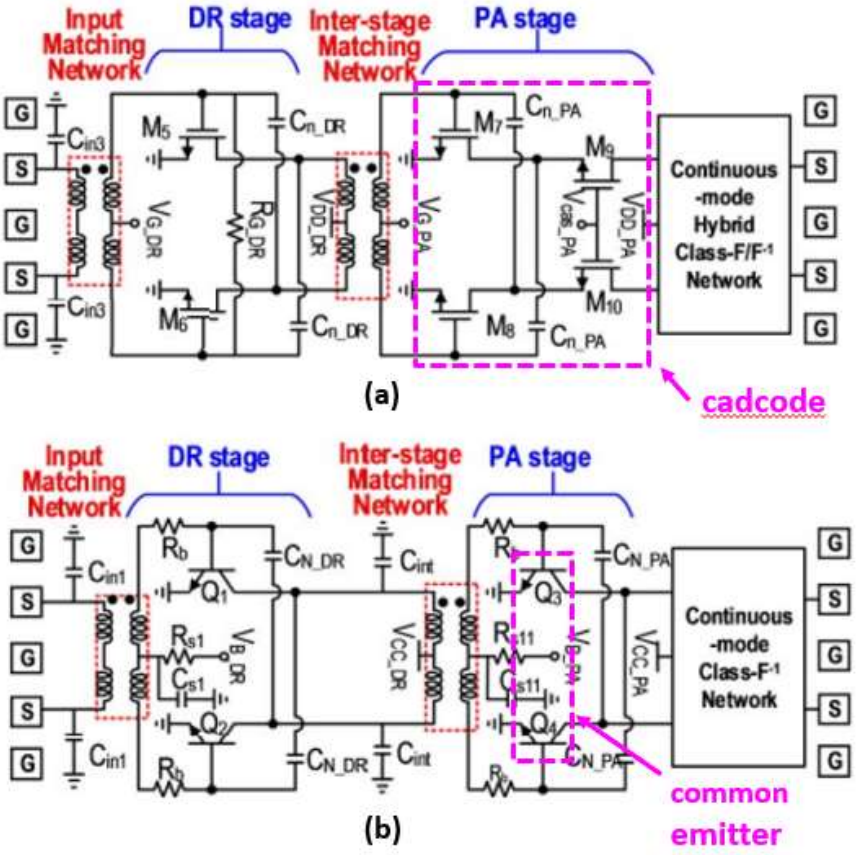


Figure 1.6 – Two mm-wave 5G power amplifier design with similar design concept, output power, efficiency, and gain in (a) a 45 nm RFSOI and (b) a 130 nm SiGe BiCMOS [41] © 2019 IEEE.

1.2.3 Breakdown Voltage of Advanced RF-CMOS and SiGe BiCMOS

As can be observed in Figure 1.1, the trade-off between transistor speed and breakdown voltage apply to all semiconductor technologies. In RF CMOS, the technology scaling reduces the oxide breakdown voltage and the maximum operating voltages defined by wear out mechanisms such as hot-carrier injection, bias temperature instability, and time-dependent dielectric breakdown [37]. Similarly, although through different mechanisms, as the f_T and f_{MAX} of SiGe HBTs evolve, the open-base collector-emitter breakdown voltage (BV_{CEO}) and open-emitter collector-base breakdown voltage (BV_{CBO}) decrease [38]. However, for FETs and SiGe HBTs of similar f_T and f_{MAX}, the maximum sustainable voltage swing of SiGe HBTs is notably higher than that of FETs. To achieve high output power, cascode or stacked design solutions are often needed for RF CMOS processes [39][40], whereas a relatively simpler common-emitter (CE) power cell would suffice for SiGe PA designs. This is illustrated by the comparisons between the two mm-wave 5G power amplifier designs with similar design concept, output power, efficiency, and gain in a 45 nm RFSOI and a 130 nm SiGe BiCMOS technology, shown in Figure 1.6 [41].

Although this gap in power handling capability from the device level difference between RF CMOS and SiGe HBT can be addressed through design techniques such as stacking, on-chip power combining [42], on antenna power combining [43], and etc, doing so inevitably introduce overhead circuit complexity which could lead to challenges for product development, especially when tight design specifications are in place. Take *IEEE 802.11ac* WiFi application for example, the demand for high data rate drives a stringent requirement on PA linearity. The required error vector magnitude (EVM) of the *802.11ac*

standard is -32 dB at the highest data rate [44]. The linearity requirement for the next generation WiFi *IEEE 802.11ax* if even harsher [45]. To satisfy such strict system requirement over process, voltage and temperature variations, the sizing, matching network, and biases network of each stage of the PA need to be carefully and precisely tuned. A simpler power cell topology could drastically reduce the number of variables to account for and thus help shorten the design cycle and time-to-market.

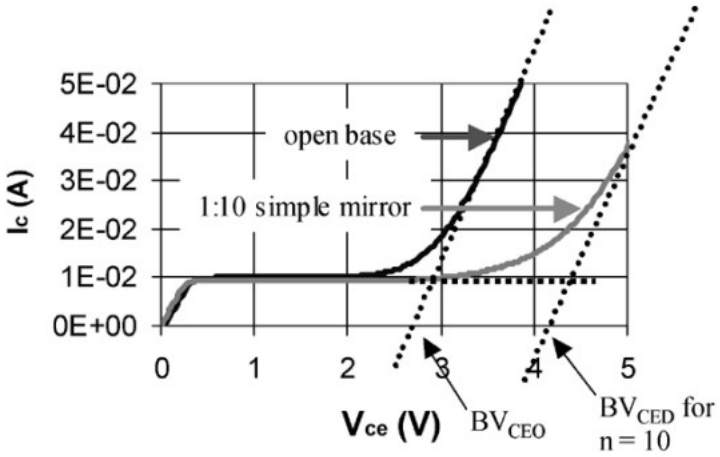


Figure 1.7 – I_C vs. V_{ce} of a 250 nm QUBiC4G SiGe HBT bias with open base and 1:10 simple current mirror [48] © 2005 IEEE.

1.2.4 Unique Design Concerns for Using Bipolar Technologies

SiGe HBTs and SiGe PIN diode are fundamentally different from FETs from a device physics perspective, and the differences incur unique concerns when biasing SiGe HBTs and SiGe PIN diodes. For switch applications where SiGe HBTs are biased in saturation, the base bias current can be in order of a few milli-Amps [46], as compared to FET switches which require no DC bias current. For amplifier applications where SiGe HBTs are biased in forward active region, the base termination of the SiGe HBTs requires extra attention. The breakdown voltage decreases, ranging from BV_{CBO} to $BV_{CEO,}$ with

increasing resistance presented to the base terminal [47]. With proper bias, SiGe HBTs can safely operate beyond BV_{CEO} as shown by the simple DC-IV comparison between open-base bias and current mirror bias plotted in Figure 1.7 [48]. This is a concern well known by designers and needs to be factored into designs as it strongly affect the save-operating voltage of the device, and hence has strong impact on the reliability of the circuits [49].

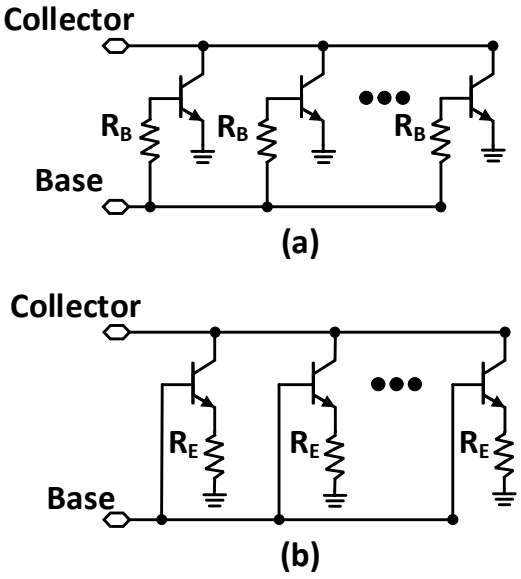


Figure 1.8 – Schematic of HBT arrays with(a) base ballasting and (b) emitter ballasting.

In additional to proper biasing, electro-thermal consideration is also particularly important for SiGe HBTs, especially when used for high power amplifier designs with large power cell arrays. Although electro-thermal effects manifest themselves and call for compensation in RF CMOS technologies [50], bipolar devices are in general more sensitive to temperature variation. The electro-thermal behaviour of SiGe HBTs, if not carefully accounted for, could cause thermal stability problem, known as "thermal runaway", which results in gain collapsing of the amplifier [51]. Emitter or base ballasting techniques (Figure 1.8) are often used to ensure thermal stability for large HBT power cells arrays,

which inevitably lead to additional trade-off between thermal stability and RF performance [52]. In addition to stability concern, the electro-thermal effect can cause EVM degradation to PAs under dynamic operation [53]. During dynamic operation, the junction temperature of the NPN cells increases as the PA turns on. The increase in device junction temperature over the period of signal burst, leads to gain drop of the PA. This gain drop, if not properly compensated for, can cause significant degradation to the dynamic EVM, as approximated by authors in [54].

1.2.5 Other Advantages of SiGe BiCMOS over RF CMOS Technologies

1.2.5.1 Low Frequency Noise

The 1/*f* noise (flicker noise) characteristics of active devices in base band and front-end receiver design is of great importance. For example, in the context of radiometer application, using device with good 1/*f* noise can significantly ease the requirements for chopping and calibration [55].

III-V devices in general have higher levels of 1/*f* noise than silicon-based devices [9]. This is because 1/*f* noise in transistors is primarily caused by defects at the semiconductor-oxide interfaces, and oxide interfaces in III-V technologies tend to be low-quality with much higher defect densities whereas silicon-based devices generally have high-quality oxide interfaces. Between SiGe HBT and RF CMOS, SiGe HBTs in general demonstrate significantly better 1/*f* noise characteristics compared to MOSFETs. This is mainly because FETs operate by passing current in a very thin layer directly under the critical barrier-channel interface, whereas SiGe HBTs are typically grown vertically and hence only a small amount of carriers encounters defects at the oxide interfaces [56]. In

addition, since 1/*f* noise in SiGe HBTs is driven by the base current [57], the increase in current gain from the introduction of germanium in the base of SiGe HBTs further reduces the input-referred *1/f* noise.

1.2.5.2 Total-Dose Radiation Tolerance

For electronic systems operating in radiation-rich environment, semiconductor technologies with good total-dose radiation tolerance are highly desirable as it can potentially reduce the amount of radiation shielding in the payload. Device performance degradation caused by total-dose radiation primarily results from damage at the oxide-semiconductor interfaces. In FETs, this damage accumulates at the critical oxide-channel interface, causing increase in the threshold voltage, reduction of device transconductance, and degradation in 1/*f* noise characteristics. In SiGe HBTs, the relative device performance degradation due total-dose radiation damage is less severe, since the damage mainly occurs at the emitter-base spacer oxide interface which is a less-critical region of SiGe HBTs (as explained in the previous subsection). As shown by J. D. Cressler in [58], across technology generations, critical RF parameters such as f_T, f_{max} and NF only degrade slightly by multi-Mrad(SiO_2) doses.

1.3 Organization

The objective of this research is to study and leverage the unique properties and advantages of SiGe HBT integrated circuit technologies to better design RF and mm-wave circuit components. The work presented in this dissertation identifies several advantages and challenges on design using SiGe HBTs and provides design examples that exploit and address these unique benefits and problems with circuit component designs using SiGe

HBTs. Chapter 2 presents the design of high-performance bi-directional amplifiers exploiting the superior g_m/ area property of SiGe HBTs. A loss-compensated X-band phase shifter and a 28 GHz differential BDA are presented in this chapter. A wideband logarithmic power detector with temperature compensated bias circuitry is presented in Chapter 3. To study and address the unique issues associated with biasing bipolar devices, novel biasing techniques in SiGe BiCMOS high power 60 GHz SPDT switch and a W-band SPDT switch performance comparison study between grounded-emitter vs. floating-emitter reverse-saturated SiGe HBTs are discussed in Chapter 4. In Chapter 5, a 60 GHz high power SiGe differential common-emitter power amplifier with novel three-conductor transmission-line-based Wilkinson baluns and asymmetric directional couplers, exploiting the multi-layered BEOL offered by advanced SiGe BiCMOS technology

CHAPTER 2. BI-DIRECTIONAL AMPLIFIERS

2.1 Introduction

Invented since the early 1900's, the phased array beamforming technique has been well understood and frequently practiced by the RF and mm-wave engineering society. With the 5th generation (5G) new radio wave, this technique is put under the spotlight as a key means to achieve ultra-fast wireless communication. Figure 2.1(a) shows the block diagram of a conventional phased array channel, where the bi-directional transmit and receive functionalities are achieved with separate circuit chains [59].

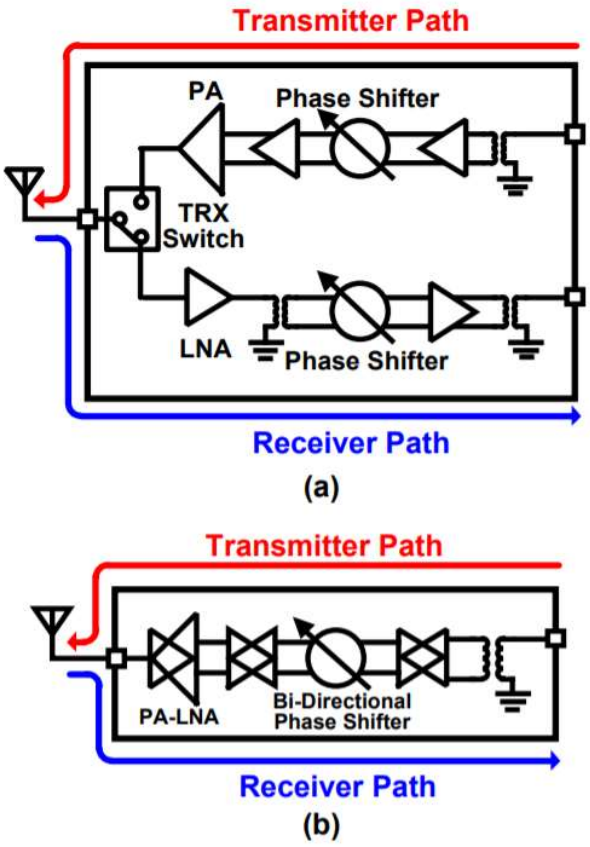


Figure 2.1 – (a) Conventional bi-directional beamformer and (b) bi-directional beamformer with BDA [59] © 2020 IEEE.

As the system complexity and operating frequencies increase in modern phased array designs, the number of transmit/ receive channels increases and antenna size and pitch scale down. A compact chip footprint is therefore highly desirable for cost reduction and low-loss signal distribution from the chip to the antenna [60]. Although the conventional phased array beamformer shown in Figure 2.1(a) has been tried and tested, this approach could fall short in term of the required chip area. The chip area is usually dominated by the inter-stage passive components between each building blocks, and therefore the phased array beamformer chip area can be significantly reduced by sharing the as many circuit components on both the transmit and receive path as possible, as shown in Figure 2.1(b). To enable this approach, high performance BDAs are the essential pieces, and the superior g_m/ area of SiGe HBTs makes SiGe BiCMOS technologies good candidates for high performance BDA design.

2.2 A Bi-Directional, X-Band 6-Bit Phase Shifter with SiGe BiCMOS Active Double-Pole Double-Throw (DPDT) Switches

Among various implementations of phase shifters [61]-[64], switched-type phase shifters offer several advantages such as its bi-directionality, easy implementation, and discrete digital phase shift step control. The conventional all-passive switched-type phase shifter suffers from high insertion loss, despite the efforts in loss optimization [64], [65]. C. Liu *et al.* in [66] proposed loss compensation with distributed amplifier while forsaking the advantageous bi-directionality of the design. Alternatively, BDA is a great candidate for loss compensation in this case as it preserves the bi-directionality of the phase shifter [67]. Presented in this section is a design of a bi-directional, X-band 6-bit phase shifter

using SiGe BiCMOS active DPDT switches. This work was presented in the 2017 IEEE Radio Frequency Integrated Circuits Symposium [1] © 2017 IEEE.

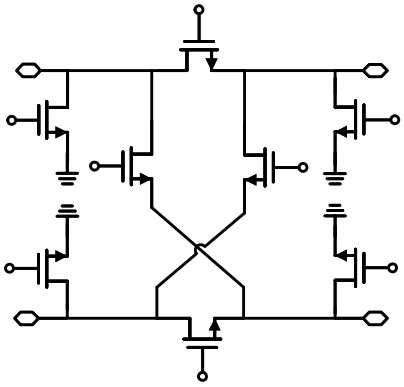
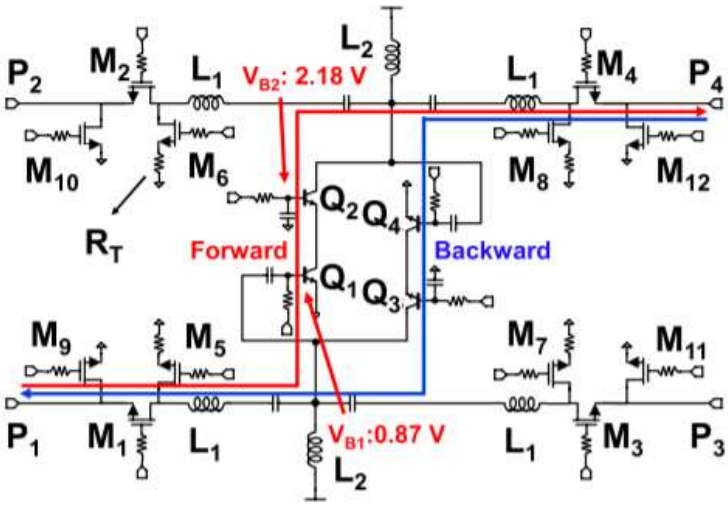


Figure 2.2 – Simplified schematic of passive DPDT switch.



Parameter	Value	Unit
$W_E(Q_1\text{-}Q_4)$	0.12	µm
$L_E(Q_1\text{-}Q_4)$	10	µm
$L(M_1\text{-}M_{12})$	0.12	µm
$W(M_1\text{-}M_4)$	160	µm
$W(M_5\text{-}M_{12})$	60	µm
L_1	550	pH
L_2	2.0	nH
R_T	39	Ω

Figure 2.3 – The schematic of SiGe active DPDT proposed in [68] © 2016 IEEE.

2.2.1 Circuit Design

For all-passive implementation of switched-type phase shifters using passive DPDT switches (Figure 2.2), the overall loss of the phase shifter increases as the number of phase shifting bit increases. The overall loss of a passive phase shifter in X-band could

easily be in the range of 8-10 dB. The 6-bit X-band phase shifter presented in this section employs a SiGe active DPDT switch proposed by M.-K. Cho *et al.* in [68] (shown in Figure 2.3), for loss compensation while preserving the bi-directionality of the phase shifter. The BDA core in this active DPDT design consists of two single-ended cascode amplifiers $Q_{1,2}$ and $Q_{3,4}$ that provide forward and backward signal amplification, respectively. Only one of these two anti-parallel connected amplifiers is turned on at a given instance with the other turned off. To achieve multi-octave bandwidth, terminating resistors R_T are used in the design for resistive matching. The DPDT switching capability is achieved via the four series-shunt single-pole single-throw (SPST) FET switches ($M_{1\text{-}4,9\text{-}12}$) at the four ports.

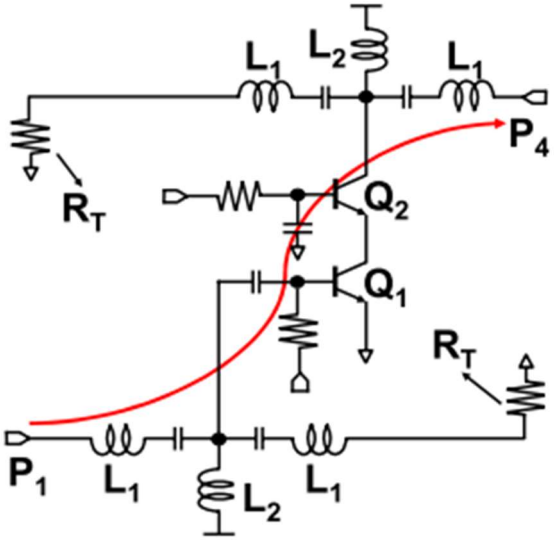


Figure 2.4 – Effective circuit when signal configured to flow from P1 to P4 [68] © 2016 IEEE.

Figure 2.4 shows the effective circuit when the active DPDT switch is configured to route signal from P1 to P4. Bias is applied to the base of transistor Q_2 and therefore turning on the forward cascode amplifier $Q_{1,2}$. At the same time, the base of transistor Q_3 is pulled to ground and thus inactivate the backward amplifier $Q_{3,4}$. Since P1 and P4 are

configured as the through ports, the series FET M_1 and M_4 are turn on and the switches at P2 and P3 are switched to the terminating resistors at the respective ports. In addition to the BDA in the switch design for loss compensation, body-floating and triple-well techniques are also employed in the four SPST switches for loss reduction and linearity enhancement.

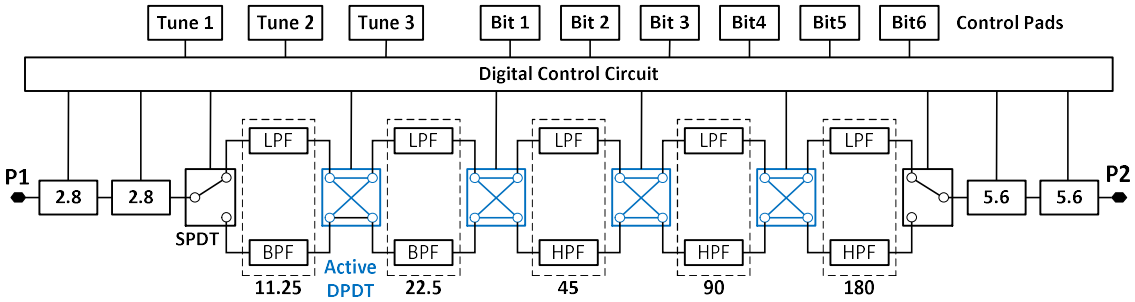


Figure 2.5 – The proposed 6-bit phase shifter using bi-directional active DPDT switches, with three additional tuning bits © 2017 IEEE.

The block diagram of the presented phase shifter is shown in Figure 2.5. A switched HP/ LP topology is used for this phase shifter. To save chip area, band-pass filters are also used for lower phase shifting bits. The 11.25º, 22.5º, 45º, 90º and 180º bits are implemented with LPF and HPF/ BPF networks, as shown in Figure 2.6. The inductances and capacitances are chosen following the methodology described by Q. Xiao in [69] to achieve flat phase response and low amplitude error across the bandwidth. The 5.6º least significant bit (LSB) and the additional three tuning bits (two 2.8º bits and one 5.6º bit) are designed together with the SPDT switches using the topology shown in Figure 2.7 to minimize circuit footprint and to reduce circuit complexity. Additional tuning bits are included in the design to account for potential simulation vs. measurement differences to achieve better phase shift accuracy.

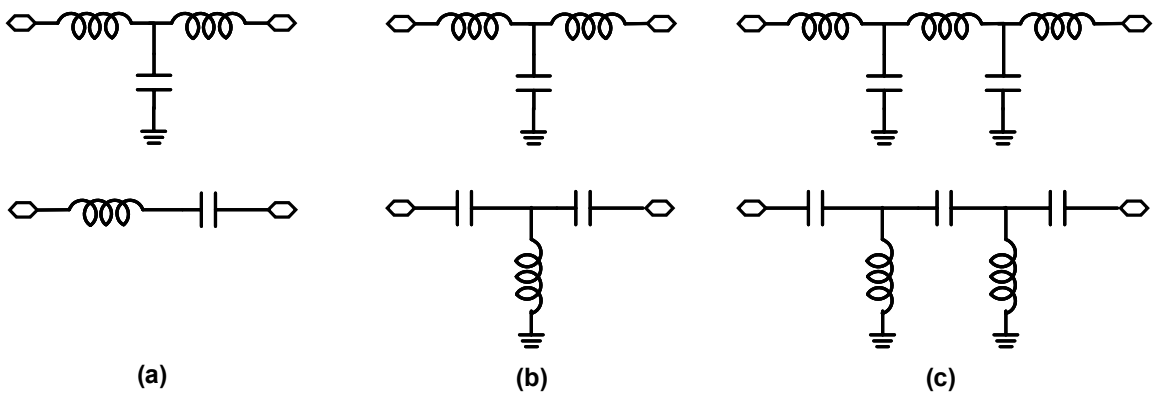


Figure 2.6 – Filter networks used for (a) 11.25º and 22.5º bits, (b) 45º and 90º bits, and (c) 180º bit. A compact L-band broadband 6-bit.

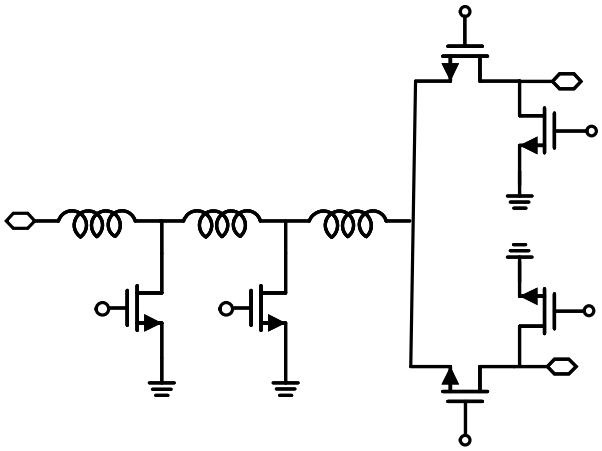


Figure 2.7 – LSB and tuning bit design with SPDT switch.

2.2.2 Measurement Results

The X-band 6-bit phase shifter is implemented in a 130 nm SiGe BiCMOS technology, featuring f_T/ f_{MAX} of 200/ 280 GHz (GlobalFoundries 8HP technology). A microphotograph of the fabricated phase shifter is shown in Figure 2.8. The circuit has dimensions of 2.6 × 1.5 mm^2, including pads. The phase states are controlled using an on-chip switch control circuitry implemented using MOSFETs provided by the process. A standard 2-port SOLT calibration was performed for on-die s-parameter characterization.

The bi-directional operation is verified by measuring and comparing the s-parameters under left-to-right (forward) and right-to-left (backward) bias conditions.

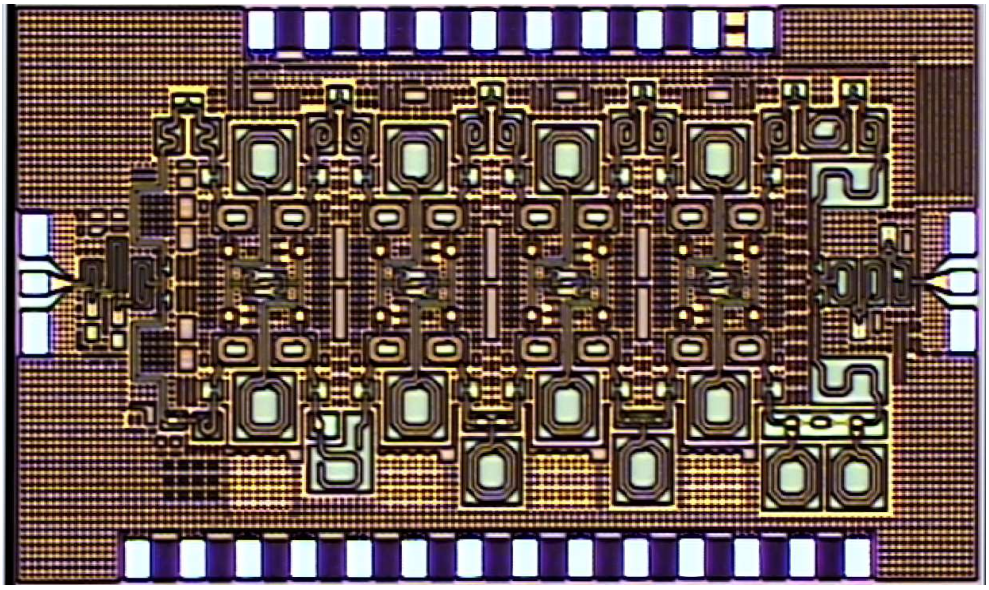


Figure 2.8 – Microphotograph of the X-band 6-bit phase shifter [1] © 2017 IEEE.

Figure 2.9 shows the input and output matching and gain of the reference state of operation. The measured results in both directions show a reasonable match. Figure 2.10 plots the measured input and output return loss and gain of the major states for forward operation. The circuit shows good matching greater than 11.5 dB gain across frequency under all 6 major phase states. An undesired gap is observed between the gain plots of the 6 major states. This is likely caused by imperfect loss matching between the HPF and LPF design. However, despite of this amplitude offset, the RMS amplitude error is still less than 0.9 dB, as shown in Figure 2.12.

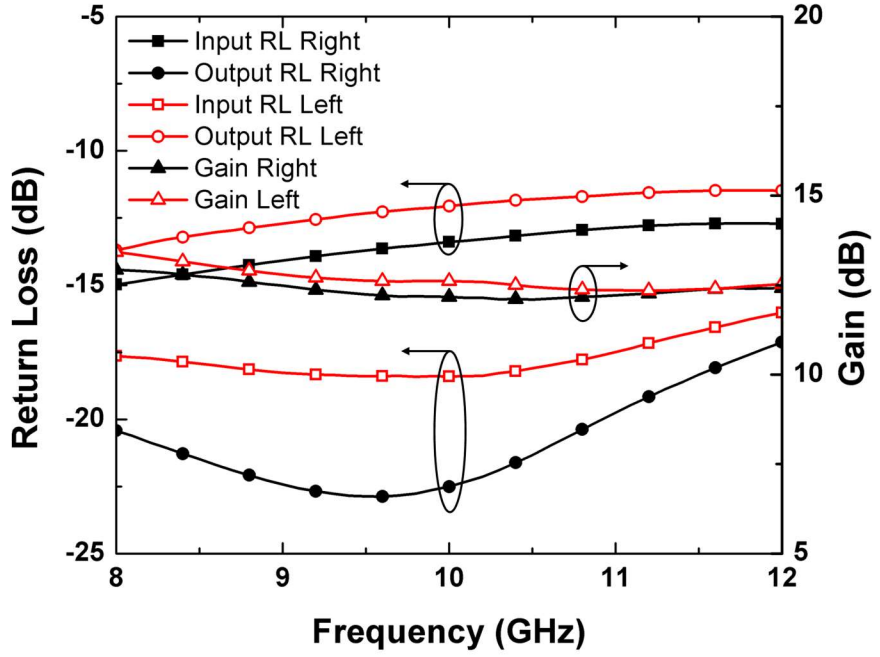


Figure 2.9 – Input and output return loss and gain of the reference state in the forward and backward operations [1] © 2017 IEEE.

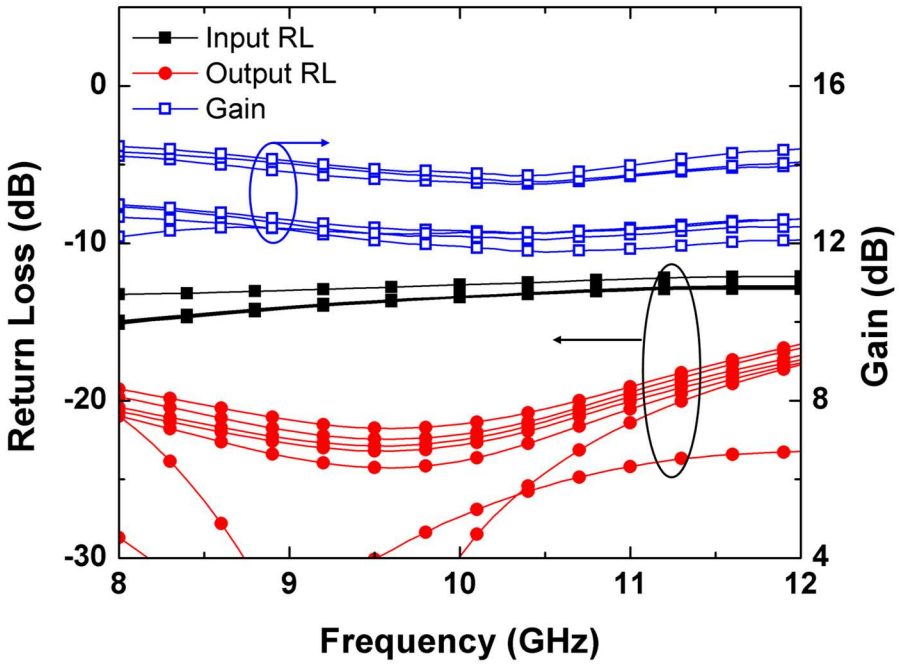


Figure 2.10 – Input and output return loss and gain of the major states for the forward operation [1] © 2017 IEEE.

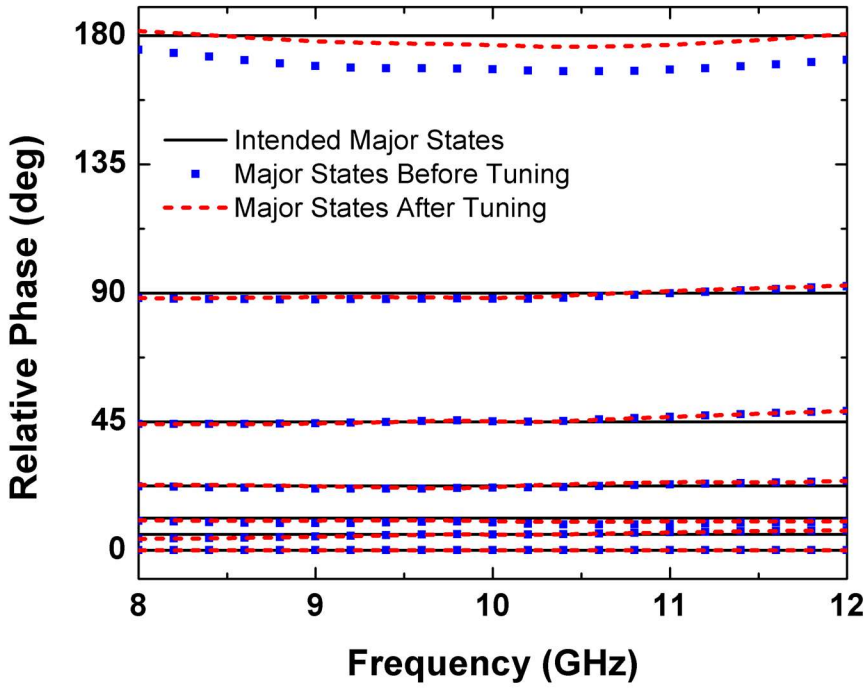


Figure 2.11 – Reference phase and measured major relative phase before and after bit tuning [1] © 2017 IEEE.

The phase performance of the 6 major states are plotted in Figure 2.11 with the black solid line marking the reference relative phase shift curves as benchmark for the measured phase performance of the phase shifter. The blue curved shows the relative phase shift of the design without any bit tuning. Due to the finite order of filter networks used in the design, the flatness of each in-band phase states is limited. The first five bits of the phase shifter element show close matching to the intended relative phase states with relatively low phase error. The phase error of the MSB shows an average of 10-degree phase error as shown in the plot. This is likely a result of inaccuracy in electromagnetic simulation during the design. The significant absolute phase error from the MSB also results in high mean and RMS phase errors. However, this error can be minimized by using the three tuning bits. By merging the control signals of the three tuning bits together with

the control signal of the MSB, the 10-degree gap of the MSB is effectively closed. Consequently, as shown in Figure 2.12, the mean phase error is decreased to -2.4 degrees at the centre frequency and the RMS phase error is decreased to less than 2.2 degrees across the design frequency.

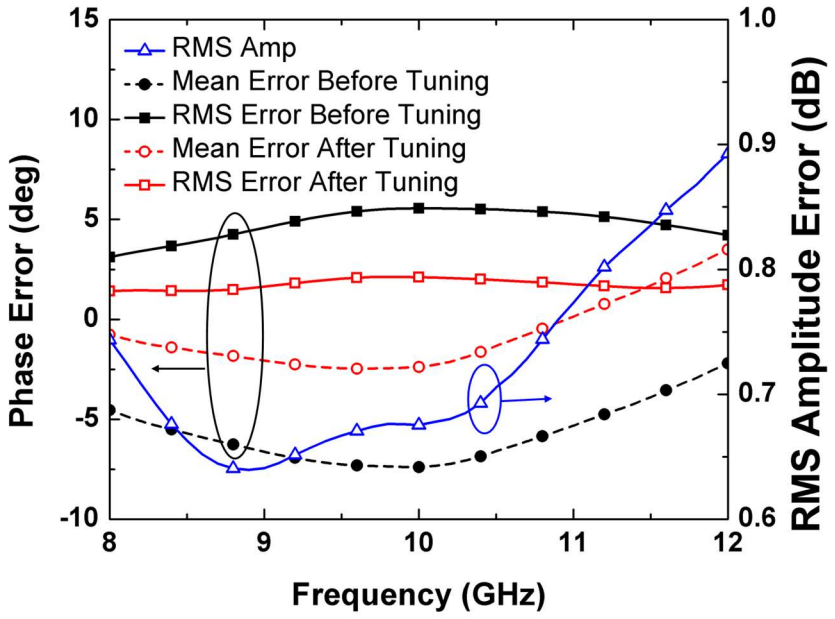


Figure 2.12 – Measured mean and RMS phase error before and after tuning, and RMS amplitude error [1] © 2017 IEEE.

The input-referred 1-dB compression (IP_{1dB}) of the design is measured at center frequency at reference phase stage under forward operation (Figure 2.13). The design shows a -15 dBm IP_{1dB}. The IP_{1dB} of the design is limited by the cascade of the four active DPDT switches. This limited P_{1dB} is a drawback compared to all-passive phase shifter designs where high IP_{1dB} is expected. However, the IP_{1dB} can potentially be improved through design optimization. The performance of this X-band 6-bit phase shifter is compared with similar phase shifter in Table 2.1.

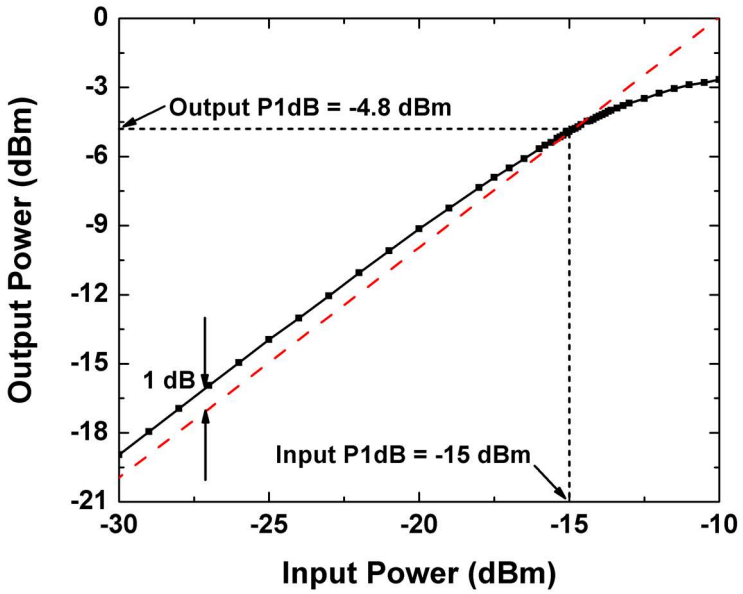


Figure 2.13 – Input-referred 1 dB compression point of the phase shifter measured at center frequency at reference phase stage under forward operation.

Table 2.1 – Performance Comparison of X-Band Phase Shifters

	Tech.	Bits	Freq (GHz)	Gain (dB)	RMS Amp Err (dB)	RMS Phi Err (deg)	IP1dB (dBm)	P_{DC} (mW)	Size (mm^2)
[61]	180 nm SiGe	5	6 – 18	16.5-19.5	< 1.1	< 5.6	-	61.7	0.90
[66]*	130 nm SiGe	5	9 – 11	25	1.2	3.8	-19**	352	15.6
[70]	250 nm SiGe	6	8 – 12	< -2.5	< 2	< 6.4	-11	110	1.55
[71]*	200 GHz SiGe	5	8 – 10.7	11	< 0.6	< 8	-	33	13.3
[72]	180 nm SOI	5	8 – 12	< -10.8	< 0.5	< 6.5	9.3	0	0.89
[73]	180 um SiGe	6	6.5 – 14.5	-9.6 – -12.5	< 0.5	< 2.1	11 – 26	133	0.64
This Work	**130 nm SiGe**	**6**	**8-12**	**> 11.5**	**< 0.9**	**< 2.2**	**-15**	**195**	**3.9**

* Circuits specifications of receive path in a T/R module (including LNA);
** Calculated from output P1dB and gain

2.2.3 Summary

The incorporation of BDA in the design proves effective for loss compensation, as demonstrated by the 6-bit X-band switched high-pass/ low-pass phase shifter design with active DPDTs. The phase shifter presented shows a greater than 11.5 dB gain across the design bandwidth, and the choice of topology results in a low RMS phase error and a low RMS amplitude error. However, due to the four cascaded active DPDT switch stages, the resultant overall input referred 1-dB compression point is an unsatisfactory -15 dBm. Although the power handling capability of this design may be justifiable for certain applications, higher IP_{1dB} is in general more desirable.

2.3 A 28 GHz Switchless, SiGe Bi-Directional Amplifier Using Neutralized Common-Emitter Differential Pair

In the BDA discussed in the previous section, the cascode amplifier structure was adopted to implement the BDA core to achieve sufficient gain with a single-stage amplifier, and to ensure high reverse isolation for circuit stability consideration. For cascode amplifier, the linearity is restricted by the upper common-base transistor which has large voltage swing across the base and collector nodes. While the P_{1dB} performance of the BDA might be acceptable for some application, an alternative topology with better power handling capability is desirable.

In this section, a design of differential anti-parallel cross-coupled common-emitter bi-directional amplifier using SiGe HBTs is presented. The IP_{1dB} at 28 GHz for forward and backward operations are -2.4 dBm and -0.4 dBm, respectively, as compared to the -7.7 dBm IP_{1dB} of the active DPDT design presented in the previous section. This was published

in the August 2018 issue of the IEEE Microwave and Wireless Components Letters [2] © 2018 IEEE.

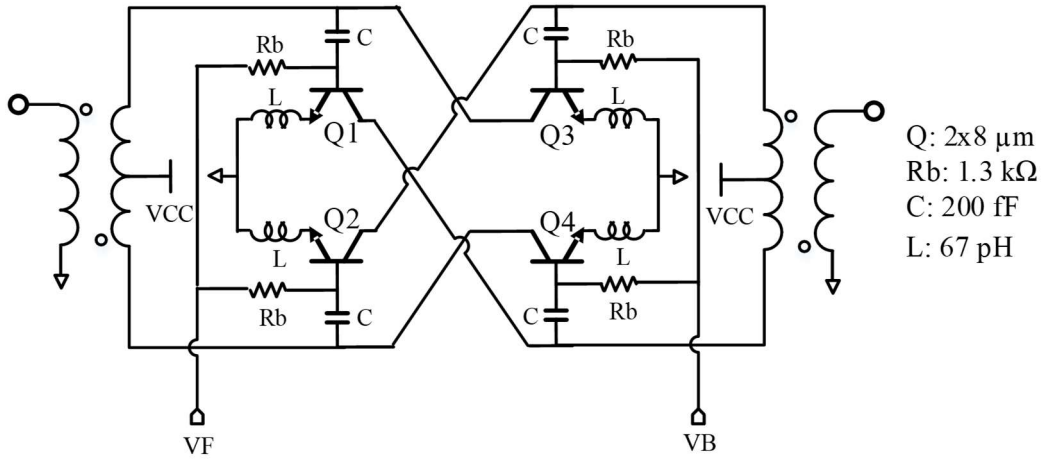


Figure 2.14 – Schematic of differential BDA using cross-coupled SiGe HBT common-emitter differential pairs [2] © 2018 IEEE.

2.3.1 Circuit Design

The differential BDA consists of two cross-coupled differential common-emitter pairs ($Q_{1,2}$ and $Q_{3,4}$) with equal transistor size, for forward and backward operation respectively, as shown in Figure 2.14. No supply switching is required in the design, and instead, a common *VCC* bias is applied to the collectors of both differential pairs through the center-tap of the secondary coils of the transformer baluns. DC blocking capacitors are used to decouple the collector and base biases. The transistors are biased close to peak f_T/ f_{MAX} current density for high linearity. Transformer balun are used at the input and output for on-die single ended characterization.

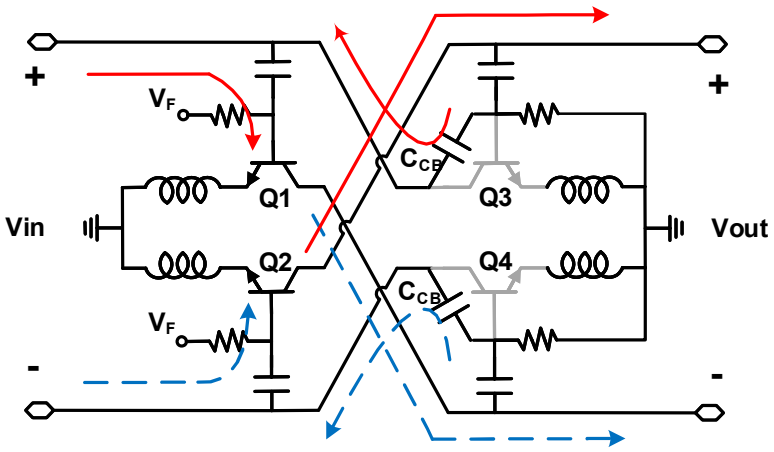


Figure 2.15 – Simplified equivalent circuit of the differential BDA core under forward operation with arrows indicating signal flow.

A simplified equivalent circuit of the BDA core under forward operation is shown in Figure 2.15, with solid arrows representing positive signal flow and dotted arrows representing inverted signal flow. In forward operation, the differential pair Q_1 and Q_2 are turned on and the base biases of transistor Q_3 and Q_4 are pulled to ground. The bases and collectors of differential pair $Q_{1,2}$ are cross-coupled with the collector-base (CB) junctions of transistors $Q_{3,4}$. Since all transistors are equally sized, the capacitances of reverse biased $Q_{3,4}$ CB junctions are comparable to that of $Q_{1,2}$, and therefore the CB junctions of $Q_{3,4}$ are suitable for providing capacitive neutralization [74] for $Q_{1,2}$. This topology takes advantage of the C_{CB} capacitance of the OFF amplifier for capacitive neutralization to enhance the performance of the ON amplifier.

2.3.2 Measurement Results

The proposed 28 GHz differential BDA was implemented using the GlobalFoundries 8HP 130 nm SiGe BiCMOS technology. Figure 2.16 shows the microphotograph of the fabricated differential BDA. The dimensions of the BDA are 0.71

× 0.90 mm^2 including bondpads. A 1.6 V *VCC* was applied to the collectors of the transistors with a 0.91 V base bias for the active differential pair (the actual V_{BE} was 0.86 V from simulation). The circuit consumes 16.8 mA of DC bias current.

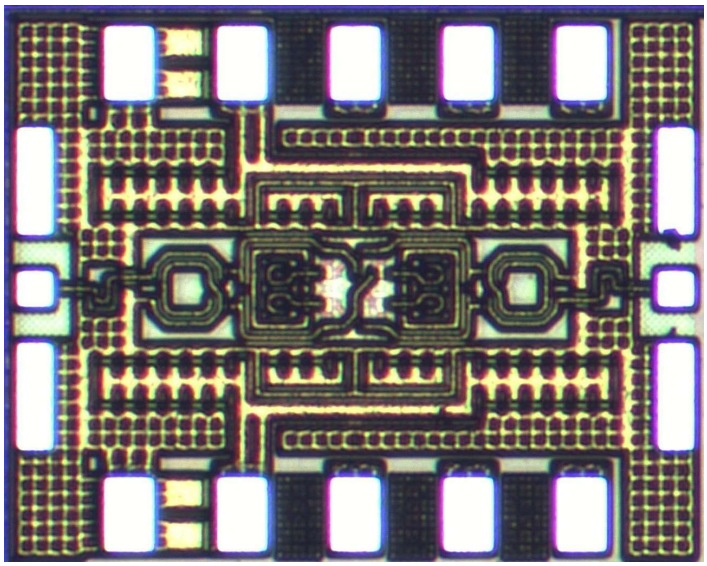


Figure 2.16 – Microphotograph of the 28 GHz switchless differential BDA [2] © 2018 IEEE.

Both the forward and backward operation were characterized and compared. Figure 2.17 shows the measured and simulated return loss under both modes of operation. S_{11} and S_{22} of both operational modes are under -10 dB between 26.5 GHz and 29.5 GHz. The simulated and measured forward and backward gain are plotted in Figure 2.18. The measured forward operational gain is 10 dB, and the gain for backward operation is 8.6 dB, at 28 GHz. The measured gain characteristics show a close match with simulation results, with maximum of 0.6 dB difference. The 1.4 dB gain difference between the forward and backward operations is a result of the asymmetric cross-coupled routing between the two differential pairs. The measured results show 10 GHz 3-dB bandwidth from 22 GHz to 32 GHz for the two operational modes.

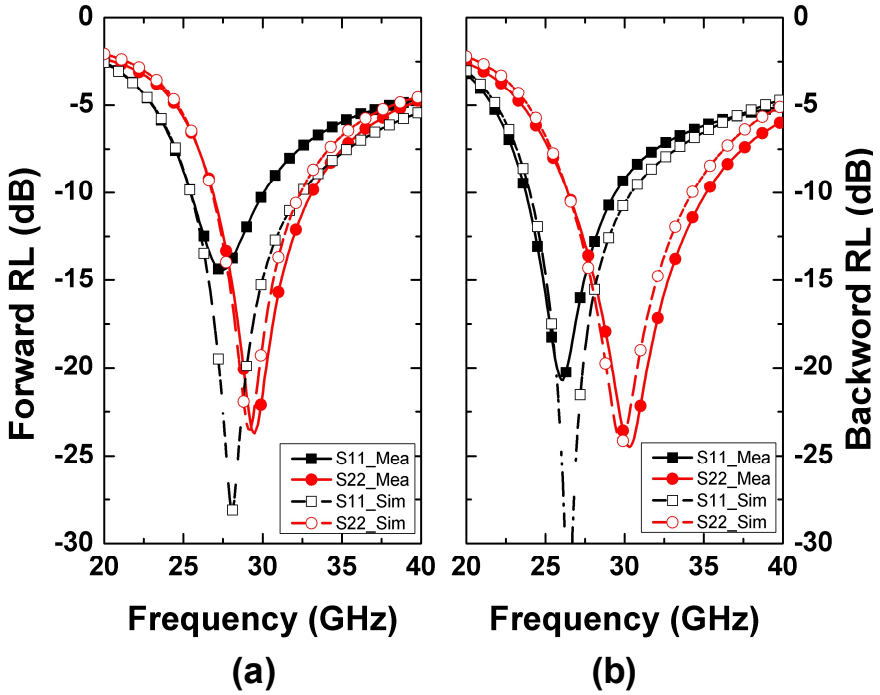


Figure 2.17 –Simulated and measured return loss of the differential BDA under (a) forward and (b) backward operations [2] © 2018 IEEE.

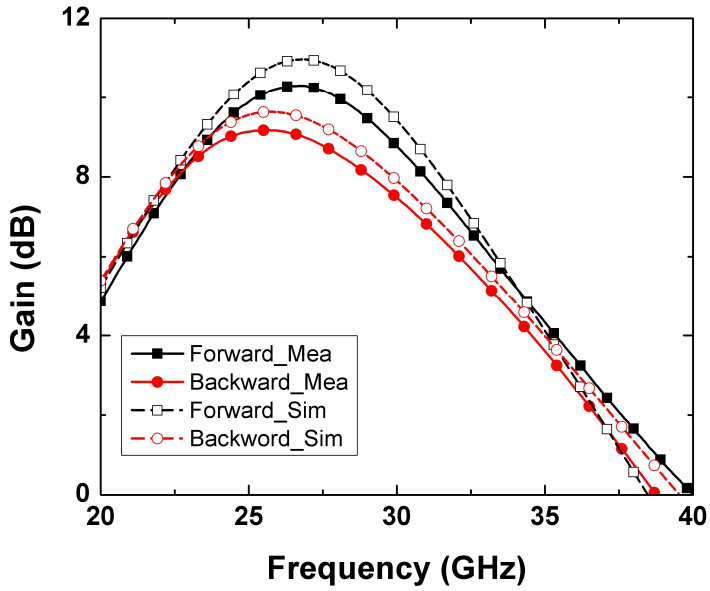


Figure 2.18 – Simulated and measured gain of the differential BDA under forward and backward operations [2] © 2018 IEEE.

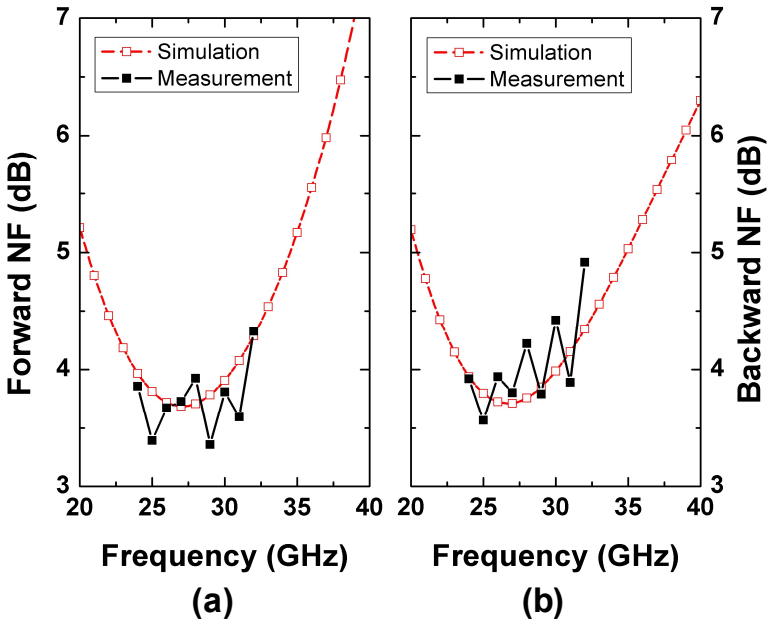


Figure 2.19 –Measured and simulated NF under (a) forward and (b) backward operations [2] © 2018 IEEE.

The noise figures of the two operational modes were measured and plotted in Figure 2.19. Forward operation shows 3.9 dB *NF* at 28 GHz, and the *NF* of backward operation at 28 GHz is 4.2 dB. Figure 2.20 shows the P_{1dB} measurement of forward and backward operations. The measured IP_{1dB} of forward operation is -2.4 dBm, and that of backward operation is -0.4 dBm. The performance of the proposed BDA is compared with other switchless BDAs, as shown in Table 2.2. A differential BDA core, that takes advantage of the parasitics of the OFF amplifier to achieve performance enhancement, has been demonstrated. The proposed BDA shows competitive performance in gain, *NF* and P_{1dB} with modest DC power consumption.

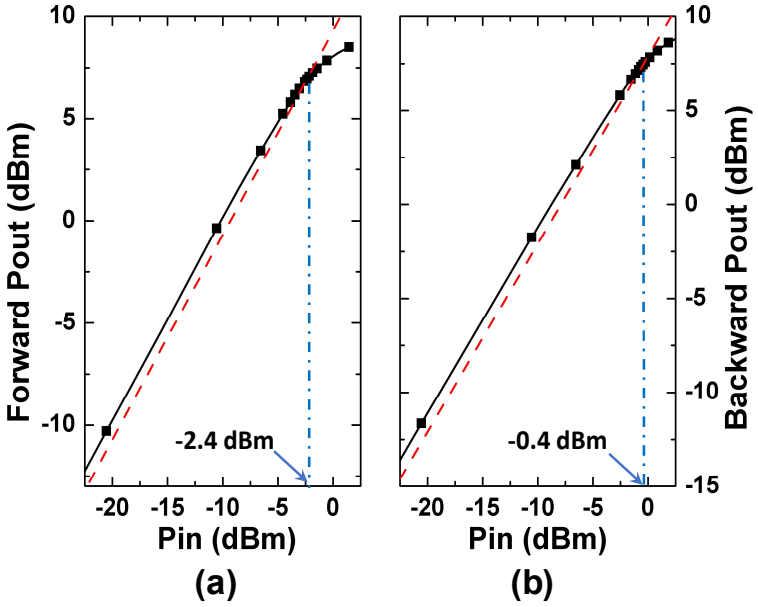


Figure 2.20 – Measured P_{OUT} *vs.* P_{IN} of the differential BDA under (a) forward operation and (b) backward operation [2] © 2018 IEEE.

Table 2.2 – Performance Comparison of Switchless BDAs

Ref	[67]	[75]	[76]	This Work
Tech	65 nm CMOS	130 nm CMOS	130 nm CMOS	130 nm SiGe
Freq (GHz)	55 – 66	8.5 – 10.5	3 – 20	26.5 – 29.5
Gain (dB)	-4.3 – 8.6	> 6.2	> 10	10/ 8.6
RL (dB)	-	> 11	> 9	> 10
OP1dB	-2.0	> 7.4	> 8	6.9/ 7.5
NF (dB)	6.9 (Sim)	< 6.1	3.2 – 6.5	3.9/ 4.2
PDC (mW)	27.6	43	68	26.9
Area (mm^2)	0.8×0.6 (core)	0.39×0.58	0.96×0.85	0.71×0.90

2.3.3 Discussion

The proposed BDA shows comparable gain with the active DPDT design used in previous section but demonstrates much better linearity. Note in the active DPDT design

described in the previous section uses resistive termination to extend the bandwidth of the design. The same resistive matching technique could be applied to the proposed differential BDA design if a higher bandwidth is desired. Doing so would lead to gain degradation, but the resultant bandwidth and P_{1dB} would expect to see a significant improvement.

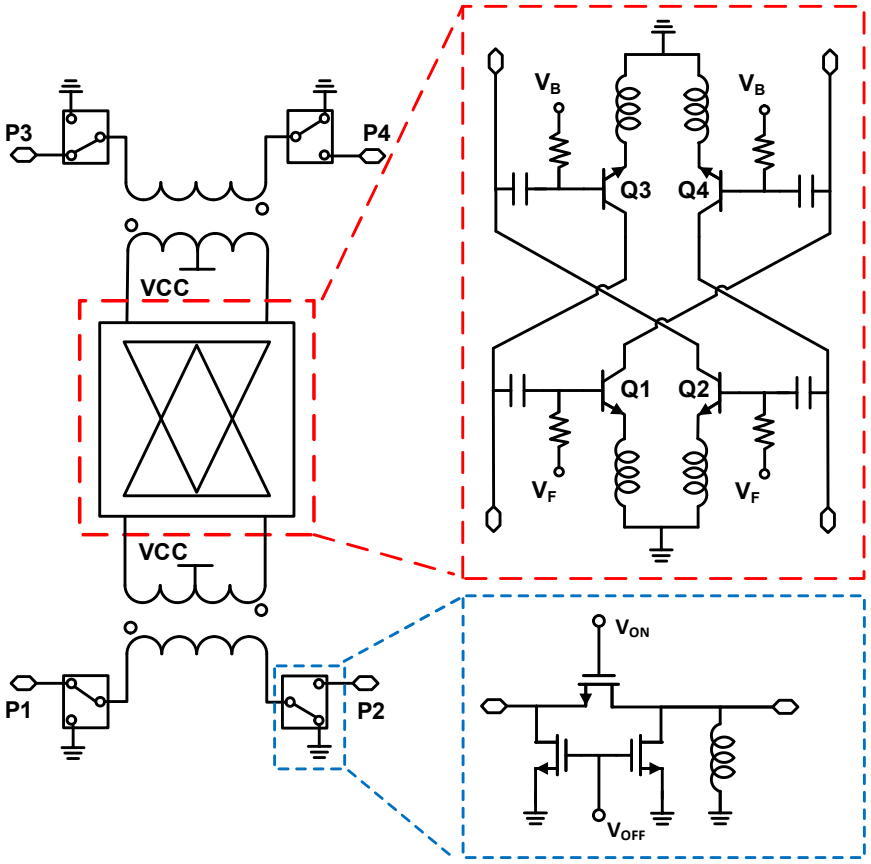


Figure 2.21 – The schematic of an active bi-directional DPDT switch using the proposed differential BDA core.

2.3.3.1 Active DPDT Switch Using the Proposed Differential BDA

As a proof of concept, an active DPDT switch was designed using the differential BDA, as shown Figure 2.21. Two series-shunt SPST switches are connected to the two ends of the primary coil of the input/output balun. The two SPST switches work together to select

the unbalanced signal port and ground terminal of the input/output transformer balun. Two shunt transistors are used in each SPST switch for improved port isolation. To compensate for the additional parasitic capacitance of the FET in the SPST switches, small shunt inductors are added to each terminal for matching.

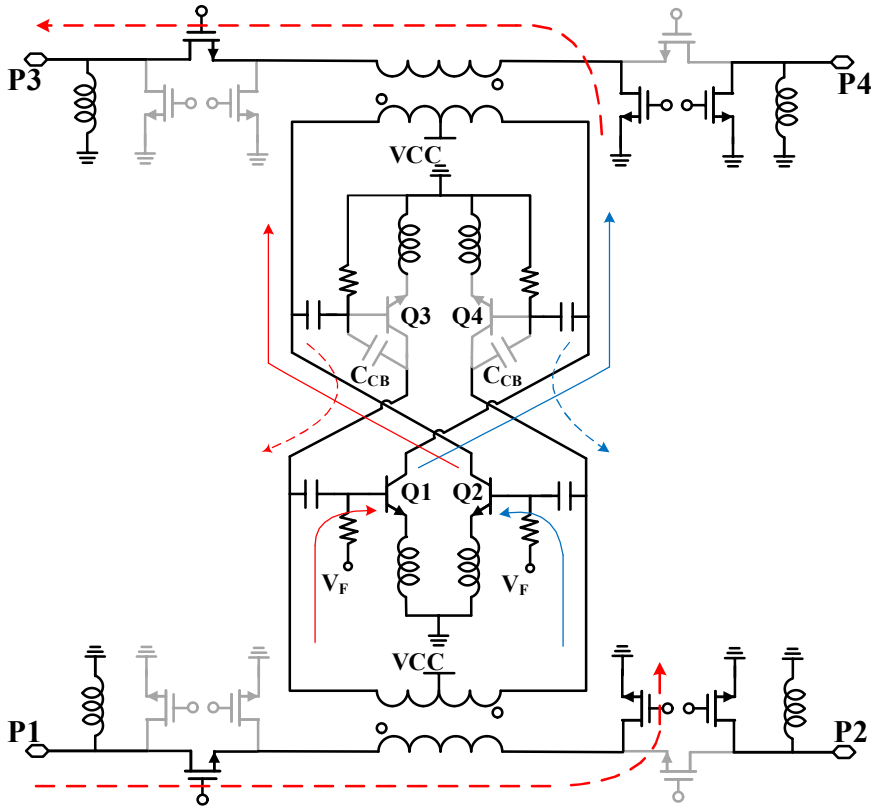


Figure 2.22 – Active DPDT circuit operation when configured for signal flow from P1 to P3.

Figure 2.22 illustrates the circuit operation when configured for signal flow from P1 to P3. To route signal from P1 to P3, the series switch transistor at P1 is turned on and the shunt transistors at P1 are off, thus configuring P1 as the unbalanced signal port of the input transformer balun. The other end of the input primary coil is grounded by the shunt transistor at the P2 side. The single-ended signal from P1 is magnetically coupled to the differential BDA through the input balun. By turning the shunt transistors at P4 and series

transistor at P3 on, the balanced output signal from the neutralized common-emitter differential pair is then coupled to P3 though the output transformer balun.

To route signal from P1 to P4, shunt transistors at P3 and series transistor at P4 are turned on. Compared to the previous scenario where the signal is routed from P1 to P3, the grounded port and unbalanced signal port of the output port are swapped. Therefore, there is an intrinsic 180˚ phase shift comparing the P1-to-P3 signal path to the P1-to-P4 signal path, due to inverted output balun configuration. Similarly, one can expect a 180˚ phase shift comparing P1-to-P3 to P2-to-P3 signal paths resulting from the inverted input balun configuration. This inherent phase inversion can be leveraged into a high-pass/low-pass switch-type phase shift design to mitigate the need for the space-consuming 180˚ filter network. However, more complicated digital control logic is required to correctly count for the number of phase inversion that occurs as the signal is switched among the high-pass and low-pass networks of each phase bit.

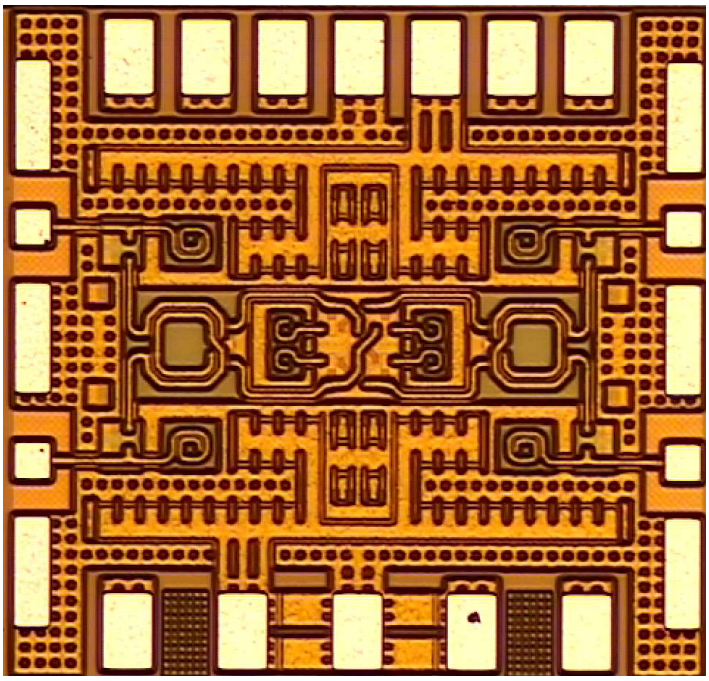


Figure 2.23 – Microphotograph of the proposed active bi-directional DPDT with differential BDA core.

2.3.3.2 Active DPDT Measurement Results and Discussions

The active bi-directional DPDT switch was designed and fabricated using the GlobalFoundries 8HP 130 nm SiGe BiCMOS technology. The microphotograph of the fabricated design is shown in Figure 2.23. The dimensions of the DPDT are 0.85×0.90 mm^2 including bondpads. The circuit consumes 26.9 mW of DC power with a 1.6 V *VCC*. Base bias voltage of 0.895 V is supplied using an external voltage source.

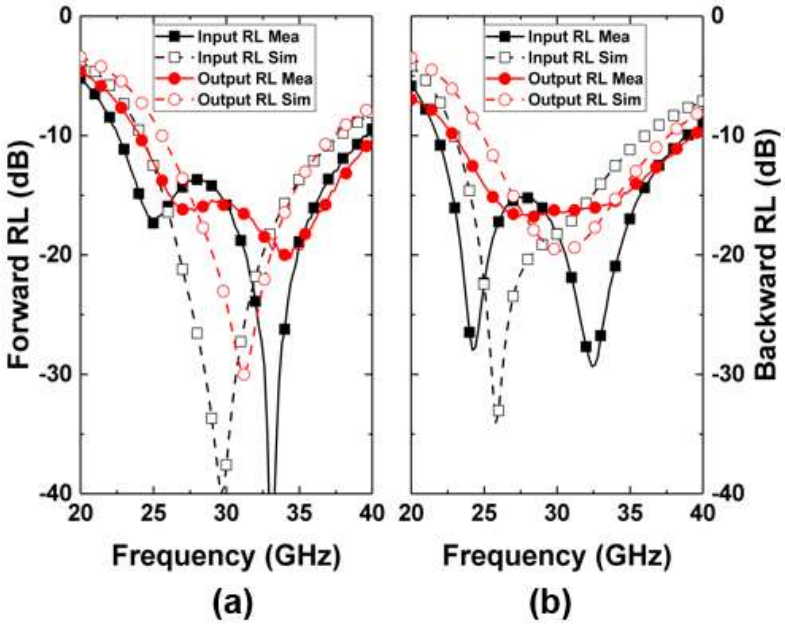


Figure 2.24 – (a) Simulated and measured return loss under P1-to-P3 (forward) operation, and (b) under P3-to-P1 (backward) operation.

For simplicity, only the operational configuration routing signal from P1 to P3 (referred as forward operation) and the configuration routing signal from P3 to P1 (referred as backward operation) are plotted. Figure 2.24 shows the simulated and measured input and output return loss of the forward and backward operations. The measured input and output return loss for both the forward and backward operations are better than 10 dB from 24.1 GHz to 39.3 GHz, showing good input and output matching. The simulated and measured forward and backward operation gain are plotted in Figure 2.25. The peak gain for the forward and backward operations is 6.6 dB and 4.8 dB respectively. The gain difference between the forward and backward operations is a result of asymmetric layout crossings in the signal routing of the amplifier core.

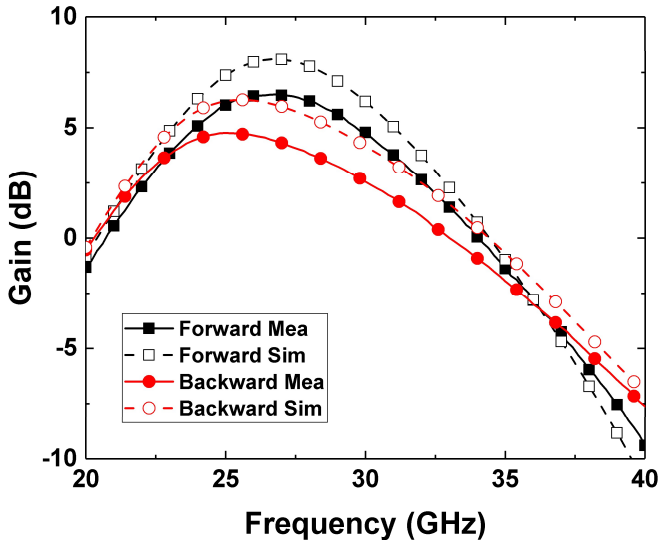


Figure 2.25 – Simulated and measured gain of forward and backward operations.

The measured port-to-port signal isolation for the forward and backward operation is shown in Figure 2.26. For the forward operation routing signal from P1 to P3, S_{21} and S_{43} are the signal isolation between the balanced signal port and grounded terminal of the two input and output transformer balun-switches, respectively. This isolation is achieved through two series-shunt SPST FET switches. S_{13} is the reverse isolation of the amplifier core. The difference between S_{41} and S_{43} is a result of the gain of the amplifier core. The noise figures of the forward and backward operations are plotted in Figure 2.27. The DPDT switch shows noise figure of 6.4 dB and 6.9 dB at 28 GHz for forward and backward operation, respectively.

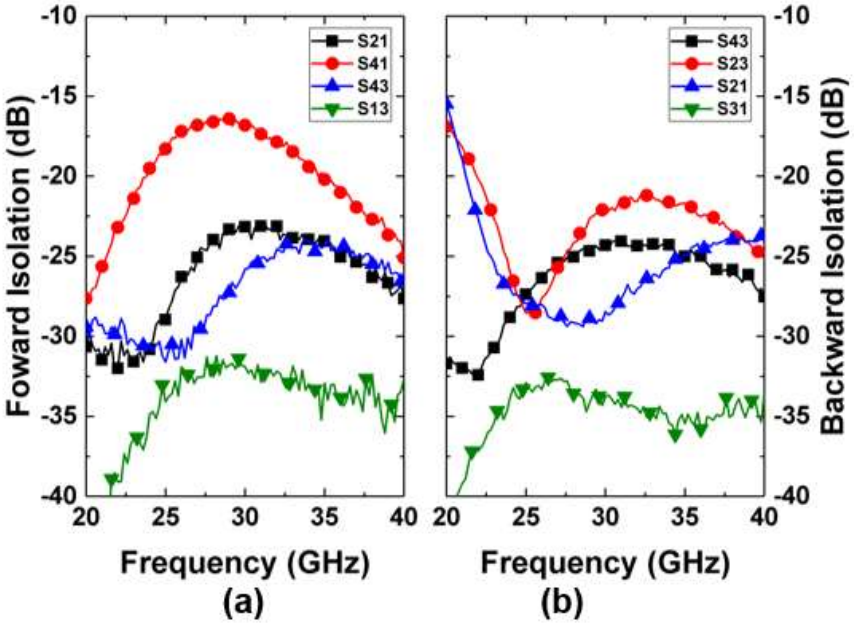


Figure 2.26 – Port-to-port isolation of the (a) forward and (b) backward operations.

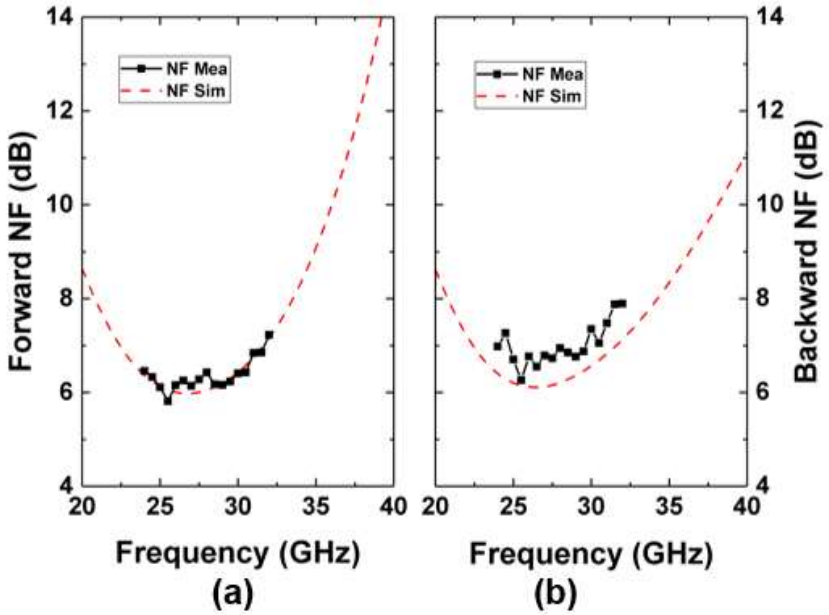


Figure 2.27 – Simulated and measured noise figure of the (a) forward and (b) backward operations.

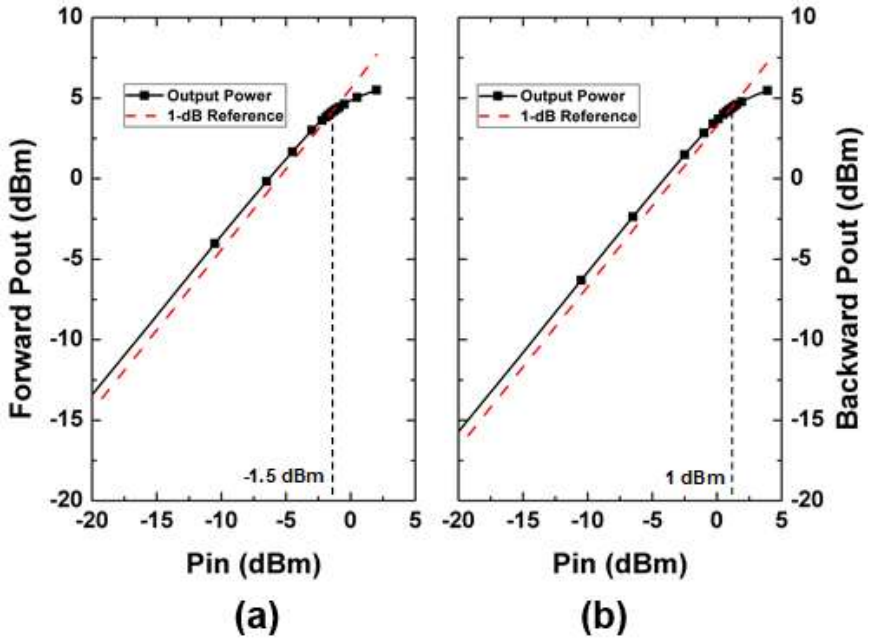


Figure 2.28 – The measured input-referred P_{1dB} of the (a) forward and (b) backward operations at 28 GHz.

Figure 2.28 shows the measured IP_{1dB} of the forward and backward operations. The forward operations shows -1.5 dBm IP_{1dB}, whereas the backward operation shows 1 dBm IP_{1dB}. Figure 2.29 shows the simulated and measured relative phase shift between and the P1-to-P3 and P1-to-P4 signal paths in forward operation and the relative phase shift between the P3-to-P1 and P3-to-P2 signal paths in backward operation. The simulation and measurement show good agreement with small phase shift error at the frequencies of interest. Unlike most switch-type phase shifters that realize 180˚ phase shift using multi-section filter networks, the proposed design achieves 180˚ phase shift by signal polarity selection on the balun-switch. The 180˚ phase shift is therefore less sensitive to passive component and parasitic EM simulation accuracy.

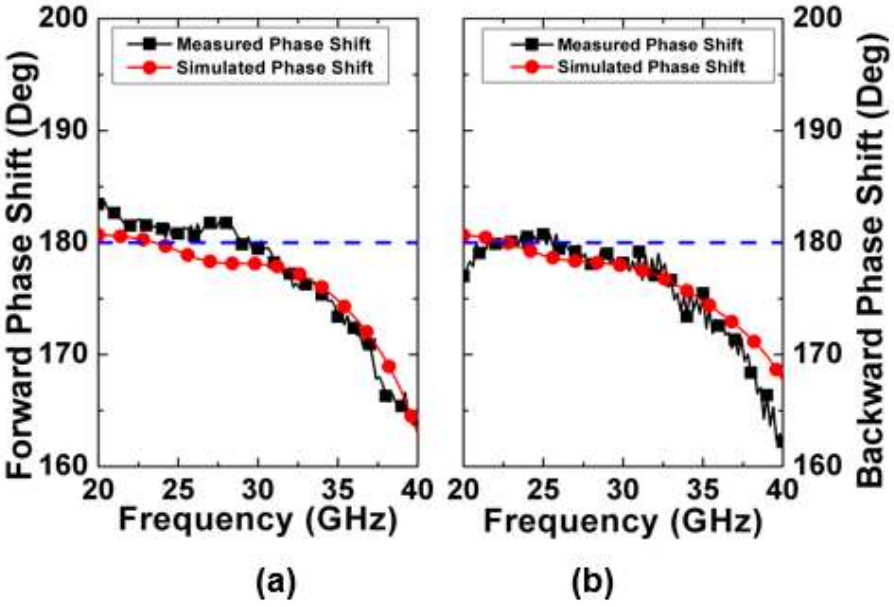


Figure 2.29 – (a) Simulated and measured relative phase shift between P1-to-P3 and P1-to-P4 paths in forward operation. (b) Simulated and measured relative phase shift between P3-to-P1 and P3-to-P2 paths in backward operation.

As shown by the measurement results, the employment of a CE differential bi-directional amplifier core leads to IP_{1dB} improvement compared to active DPDT implementation using anti-parallel single ended cascode amplifier core shown in the previous section. The inherent phase inversion during input/output balun port switching results in an accurate 180˚ phase shift which is an attractive feature for switch-type phase shifter designs, as it provides loss compensation and mitigates the need for area consuming 180˚ phase shift bit implementation.

CHAPTER 3. BROADBAND LOGARITHMIC POWER DETECTOR

3.1 Introduction

In radar and communication systems, high performance power detectors are of important use. For applications operating in extreme environment and applications that can jeopardize human lives upon failure, built-in self-test (BIST) feature that offers on-die system monitoring and continuously verifies the functionality of the system is highly desirable. Figure 3.1 shows the block diagram of a W-band transceiver with BIST [77] where power detectors are deployed on both the transmit and receive path for characterization of the transceiver gain, linearity, and output power. In commercial communication chipsets, power detectors serve the important role to enable accurate amplifier gain and power control which is crucial to link range and power efficiency optimization, as illustrated by the *IEEE 802.11ac* design example in Figure 3.2.

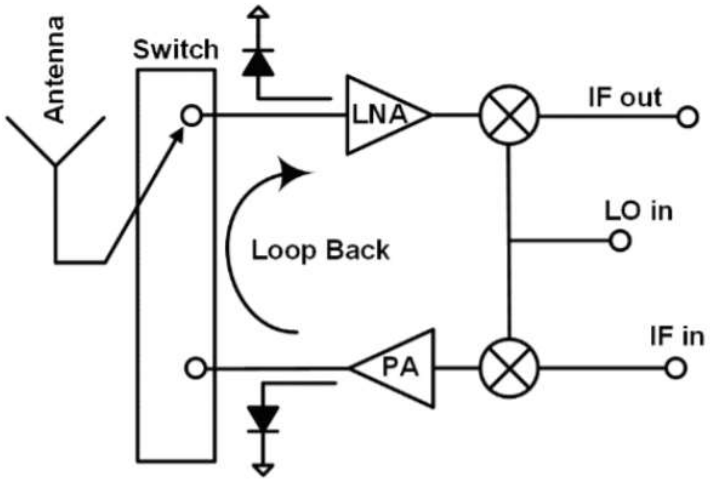


Figure 3.1 – Block diagram of a W-band transceiver with BIST [77] © 2019 IEEE.

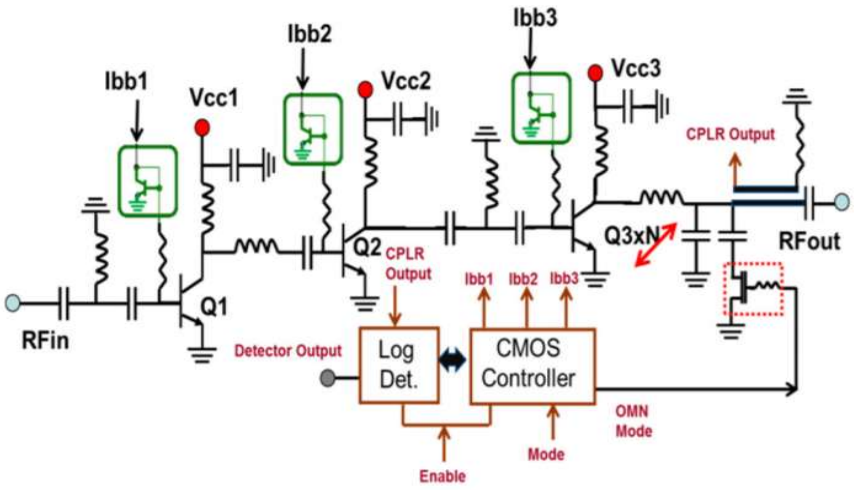


Figure 3.2 – Block diagram of an IEEE 801.11ac power amplifier using an on-chip logarithmic power detector for automatic power control © 2017 IEEE.

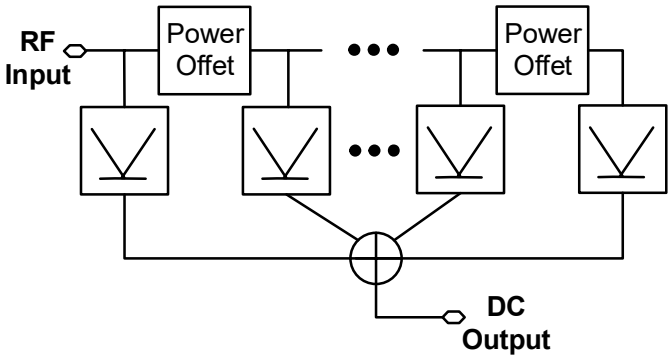


Figure 3.3 – Block diagram of the piece-wise linear approximation implementation of logarithmic power detector.

Compare to a square-law detector that has a linear- linear transfer characteristic, a power detector linear-in-dB transfer characteristic is advantageous as the measured power level is usually specified in a logarithmic scale. The successive detection log amplifiers [79] and true log amplifiers [80] are popular conventional implementations that achieve a logarithmic transfer characteristic through piecewise approximation with several linear detectors placed in parallel and input power level offset introduced among them, as shown in Figure 3.3. The use of cascaded limiting amplifiers effectively provides wide dynamic

range but limits the frequency response of these architectures. Alternatively, the use of gain-offset, parallel amplifier-rectifier branches with wideband signal feed was demonstrated in [81]. Apart from improving dynamic range by lowering the minimum input power through amplifiers, [82] employs series connected passive attenuators to offset input power level at each rectifier branch and thus increase dynamic range through increasing the maximum detection power.

Alternatively, a log amplifier can be used to convert the linear output response of a power detector to linear-in-dB characteristic using the exponential DC I-V characteristics of a transistor without piece-wise approximation. A diode or a diode connected NPN HBT are also good potential candidates [83]. Y. Zhou and M. Y. Chia [79] proposed a log detector by incorporating a log amplifier relying the I-V characteristic of a nFET biased in weak inversion. However, the work showed limited bandwidth and different output characteristic over frequency.

In this Chapter, a log detector with wideband input matching network, showing low log error from 2 GHz to 40 GHz. Linear-in-dB output characteristic is achieved exploiting the exponential I-V characteristic of bipolar device. This work was presented in the 2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium [3]

3.2 Circuit Design

The schematic of the log detector circuit is shown in Figure 3.4. All SiGe HBTs were biased with current mirrors with a reference current by an on-chip reference circuit. For presentation clarity, the reference circuit and all current mirrors are omitted in Figure

3.4. The RF input port is terminated with a 50 Ω resistor to ensure wideband matching. Inductors L_1 and L_2 are used to form a T-section with the input capacitance of Q_1. Resistors R_1 and R_2 are employed at the base of Q_1 and Q_2 for RF signal blocking. Since the circuit contains multiple analog circuit block which are sensitive to mismatch errors, 2-D common centroid layout technique is applied whenever possible.

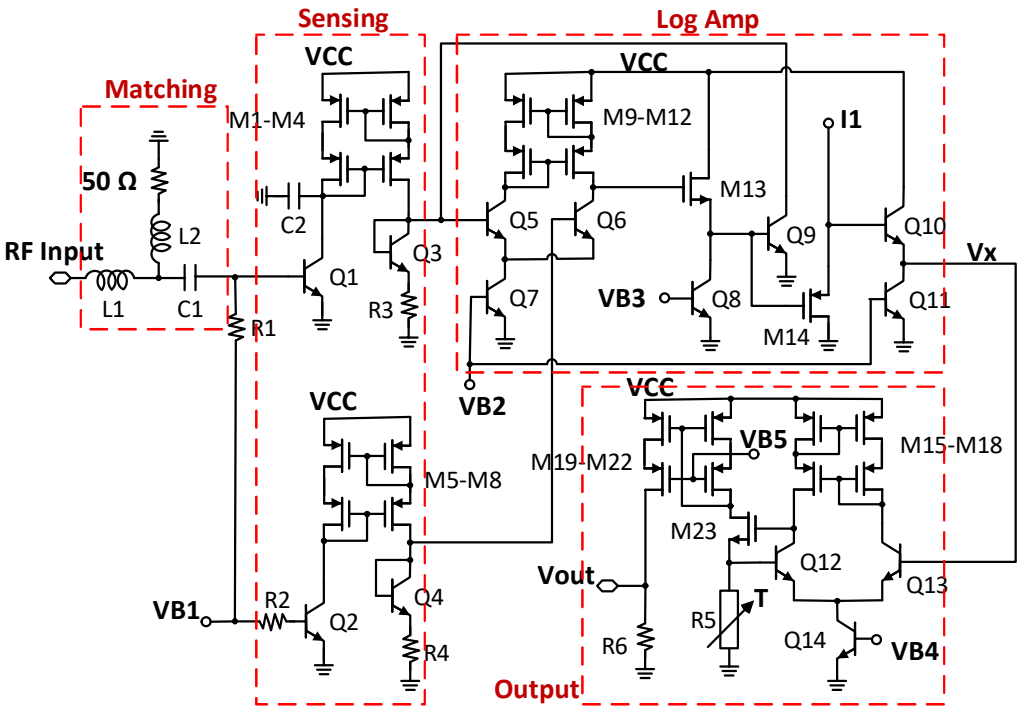


Figure 3.4 – Schematic of the proposed log detector with bias circuit omitted for presentation purpose [3] © 2019 IEEE.

The matched common emitter SiGe HBT pair Q_1 and Q_2 are used as sensing and reference devices. The two transistors are biased with 100 µA of quiescent current. As the input power level increases, the voltage swing at the base of transistor Q_1 increases, which leads to an increase of the DC component of its collector current. The difference in DC current through Q_1 and Q_2 has a linear relation with respect to the input power. The collector currents of Q_1 and Q_2 are mirrored to matched load Q_3-R_3 and Q_4-R_4. The single

stage SiGe HBT op-amp Q_5-Q_7 and M_9-M_{12}, level shifter M_{13}-Q_8, and Q_9 form a negative feedback loop that forces the voltage across load Q_3-R_3 and Q_4-R_4 to be equal. Therefore, the delta current that arises from the increase in RF input power must be sunk by the collector current of transistor Q_9, resulting in an increase in the emitter-base voltage of Q_9. Due to the exponential relation between the collector current and V_{BE} of Q_9, the V_{BE} and input power has a linear-in-dB relation. An additional HBT Q_{10}, matched to Q_9, is introduced to compensate for the strong temperature dependence of Q_9 V_{BE}. R_5 is implemented using series connected nFETs in triode region to partially correct for the output characteristic slope difference over temperature.

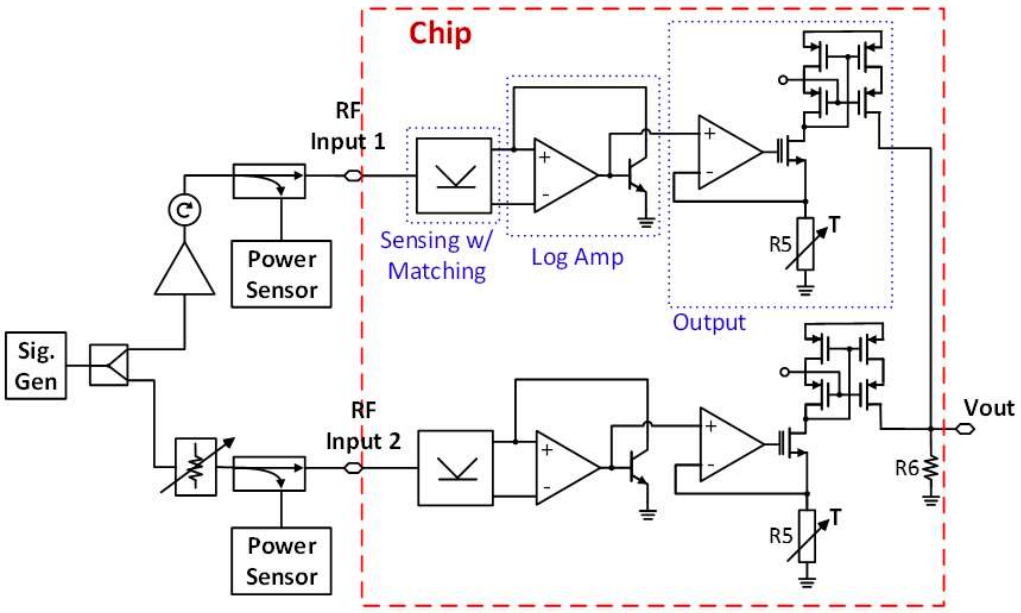


Figure 3.5 – Simplified block diagram of the two-branch log detector. Input power level to the two branches are offset through external amplifier and step attenuator for testing purposes [3] © 2019 IEEE.

The dynamic range of the log detector can be limited by the dynamic range of the square law sensing stage, the dynamic range of the log-amp, dynamic range of the output stage, and device mismatch. However, the dynamic range of the log detector could be

extended using the concept demonstrated in [79]-[82], by introducing another detector branch with an input power level offset and summing the output of the two branches. The power level offset could be implemented by terminating matching network with broadband amplifier or attenuator instead of a 50 Ω resistor. To test this approach, a two-branch version of log detector was designed, as shown in Figure 3.5. For testing purposes, the RF input power level offset was realized with an off-chip amplifier and step attenuator. The output current of the two branches are summed together and converted to a voltage output via a shared load resistor.

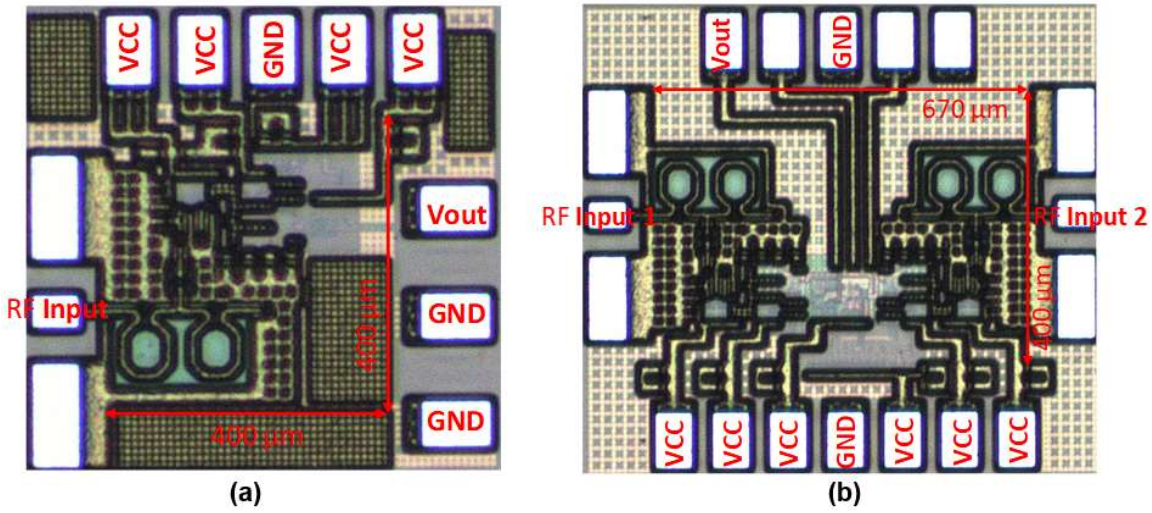


Figure 3.6 – Chip micrograph of (a) single branch log detector and (b) two-branch log detector [3] © 2019 IEEE.

3.3 Measurement Results

The log detectors were designed and fabricated using the 130 nm GlobalFoundries 8HP SiGe BiCMOS process (f_T/f_{MAX} = 200 / 265 GHz). The chip micrograph of the single branch and two-branch log detectors are shown in Figure 3.6. The core of the single branch

log detector occupies 0.40×0.40 mm^2 chip area and the core of the two-branch log detector consumes 0.40×0.67 mm^2.

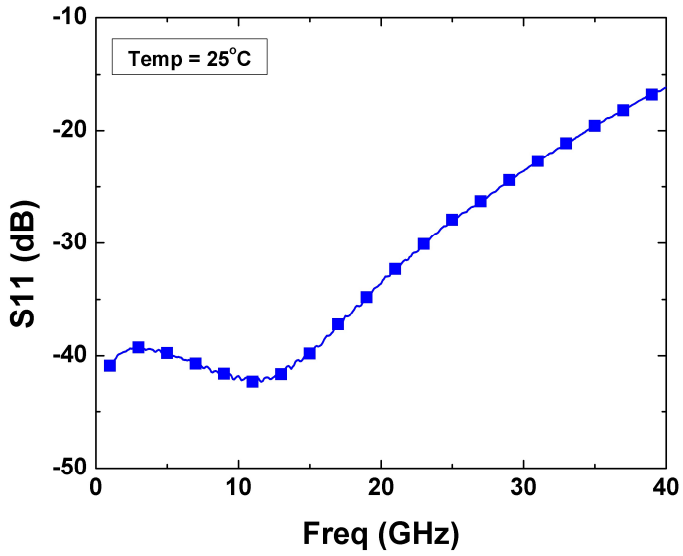


Figure 3.7 – Input matching of the single branch log detector measured at room temperature. Result shows better than 15 dB return loss below 40 GHz [3] © 2019 IEEE.

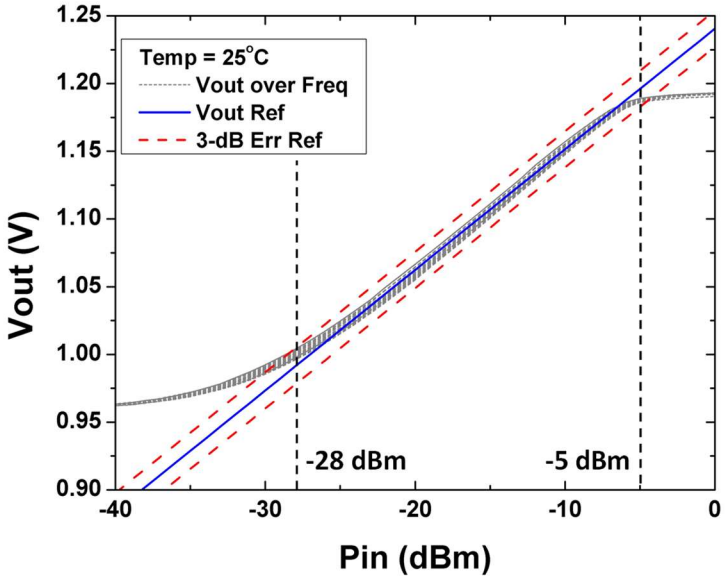


Figure 3.8 – V_{out} vs P_{in} of single branch log detector measured from 2 GHz to 40 GHz with 2 GHz frequency steps at room temperature. Reference with ±1.5 dB log error reference lines are plotted. Results show from -28 dBm to -5 dBm logging range within ±1.5 dB log error [3] © 2019 IEEE.

The S_{11} of the single branch log detector at room temperature was measured as shown in Figure 3.7. The input return loss is greater than 15 dB below 40 GHz, as expected from the wideband input matching scheme. The output voltage vs. P_{in} characteristic of the single branch log detector at room temperature was measured with input power sweep from -40 dBm to 0 dBm from 2 GHz to 40 GHz, in 2 GHz steps. As shown in Figure 3.8, the output characteristics over frequency are closely clustered around the reference line. The red dotted lines marks ±1.5 dB log error references. The log detector shows a 23-dB dynamic range (-28 dBm to -5 dBm) from 2 GHz to 40 GHz with ±1.5 dB log error.

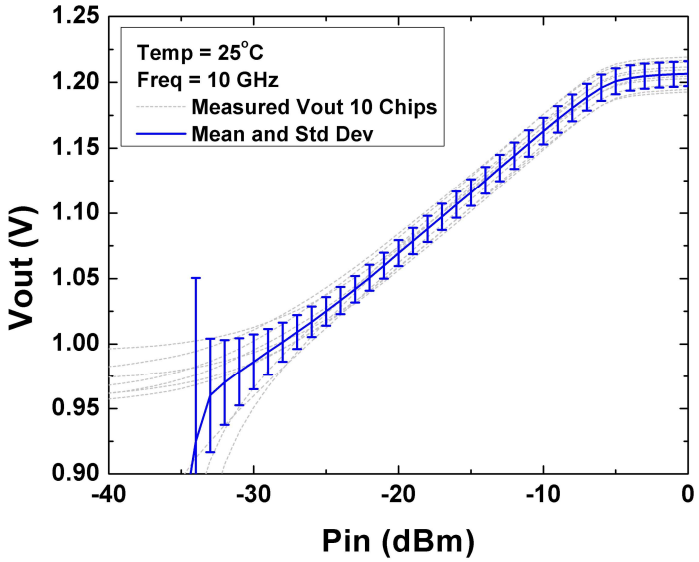


Figure 3.9 – Measured Vout vs. Pin response of the single branch log detector at room temperature of 10 chips with 10 GHz input signal. Mean and standard deviation plotted with solid dash and error bar [3] © 2019 IEEE.

The V_{out} vs. P_{in} characteristics of 10 chips were measured at 10 GHz at room temperature, as shown in Figure 3.9. The average of the 10 measurements are plotted with error bars representing the standard deviation. The measurement variation among the 10 chips in the mid and high input power range can be attributed to chip-to-chip process variations. The slope of the response and offset could be made easily adjustable, if required,

by designing R_5 and R_6 to be trimmable. The standard deviation of the 10 measurements increases significantly as the input power level decreases, thus limiting the dynamic range of the log detector. At low input power levels, the ΔI_{DC} caused by the input power is very small. As a result, the log detector is sensitive to random offset errors between the sensing and reference paths in the sensing stage and op-amp offsets at low input power levels. Apart from layout techniques that improve device matching, this problem can also be addressed with an additional fine trimming mechanism, as demonstrated in [83].

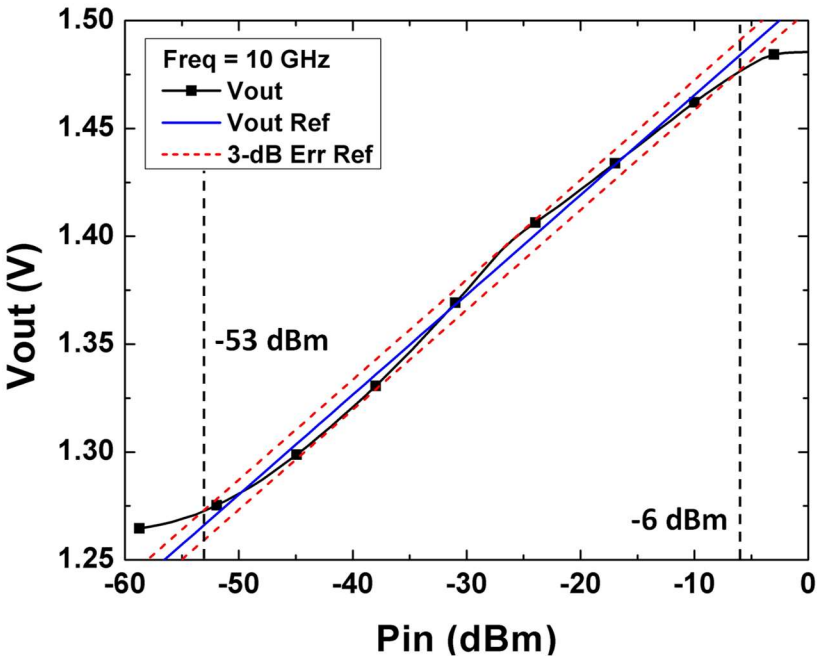


Figure 3.10 – V_{out} vs. P_{in} of the two-branch log detector at 10 GHz and room temperature with 25 dB input power level. The reference and ±1.5 dB log error reference lines are plotted in solid and dotted lines respectively. Results show 47 dB dynamic range within ±1.5 dB log error [3] © 2019 IEEE.

Instead of employing fine trimming circuits to achieve a higher dynamic range, a second branch with offset input power level can be added. Figure 3.10 shows the measure V_{out} vs. P_{in} characteristic of the two-branch log detector with 10 GHz input signal at room temperature. A 25-dB input power level offset was introduced between the two branches

using internal amplifier and attenuator. The reference line and the ±1.5 dB log error reference lines are also plotted. The result shows a 47-dB dynamic range (-53 dBm to -6 dBm) with in ±1.5 dB log error. To further improve the dynamic range of the two-branch log detector, trimming mechanism can be introduced to R_5 and R_6 to better align the slope of the response from each branch.

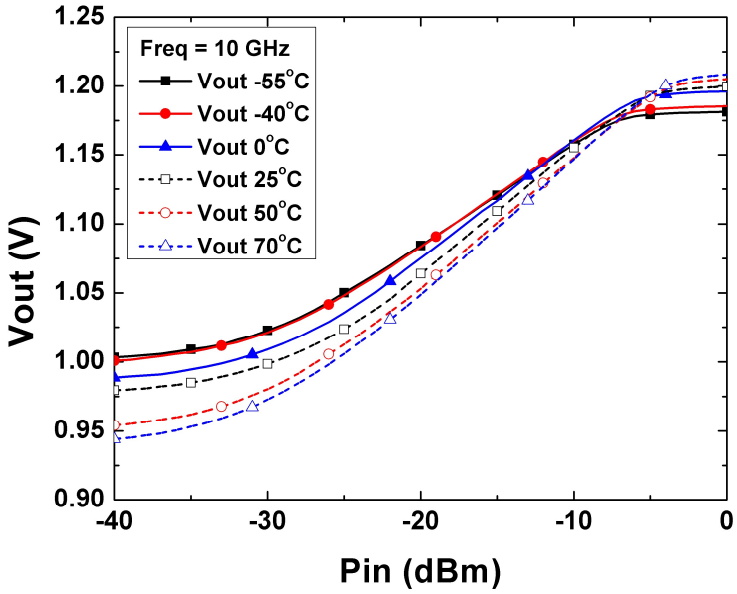


Figure 3.11 – Measured V_{out} vs. P_{in} response of single branch log detector over temperature with 10 GHz input signal [3] © 2019 IEEE.

The V_{out} vs. P_{in} response of the single branch log detector was also measured over temperature, from -55 °C to 70 °C at 10 GHz, as shown in Figure 3.11. Since the performance characteristics of SiGe HBTs are highly sensitive to temperature, the low power V_{out} offsets and the slope of the V_{out} vs. P_{in} response are expected to have a strong dependency on temperature. Figure 3.12 shows the slope of the curves across temperature at -15 dBm input power at 10 GHz. More sophisticated temperature compensation circuits are needed to reduce the log error over temperature, if required.

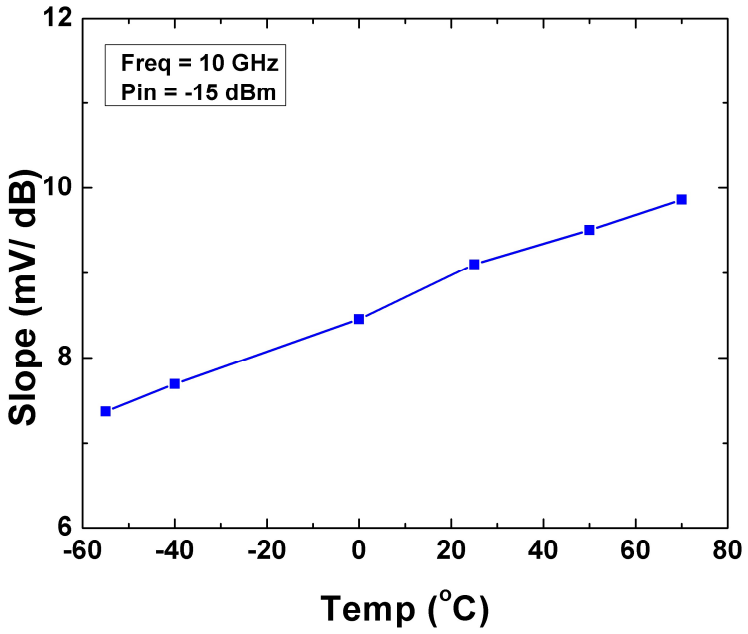


Figure 3.12 – Slope of the V_{out} vs. P_{in} response in Figure 3.11 over temperature at -15 dBm input level [3] © 2019 IEEE.

The V_{out} vs. P_{in} characteristic of the single branch log detector was measured at 77 K temperature with 10 GHz test input signal, even though the on-chip reference circuit is not designed to for such extreme operation conditions. Although the behavior deviates significantly from the measurement result between -55 °C and 70 °C, a linear response is still observed for a significant range of input power, as seen in Figure 3.13.

The single branch log detector design adopts a 2 V *VCC* supply and draws 1.6 mA of quiescent current. The design consumes less than 7.8 mW of DC power across the whole dynamic range. The performance of the proposed single branch power detector is compared with the state-of-the-art power detector designs in Table 3.1.

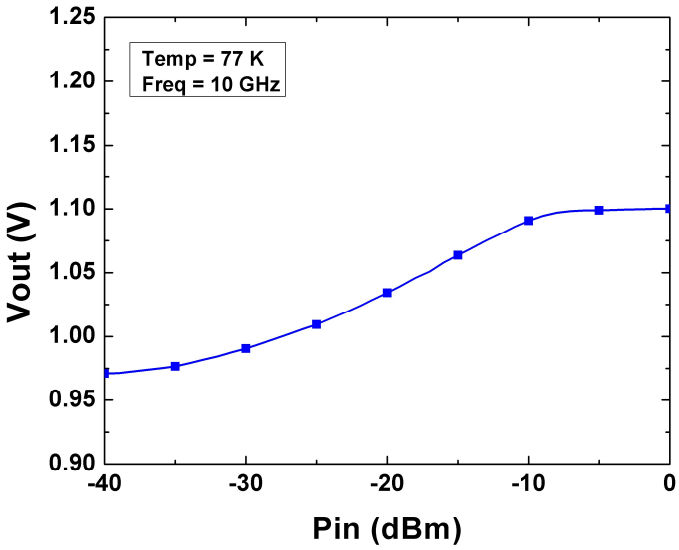


Figure 3.13 – The measured V_{out} vs. P_{in} response of the single branch log detector at 77 K with 10 GHz input signal [3] © 2019 IEEE.

Table 3.1 – Performance Comparison of Power Detectors

	Tech	Freq (GHz)	P_{DC} (mW)	DR (dB)	Log Det.	Area (mm^2)
[81]	130 nm CMOS	2 – 16	35.3	> 50	Yes	1.0×0.75
[82]	180 nm CMOS	0.3 – 10	0.55	42	Yes	0.27×0.42
[83]	130 nm SiGe	100 – 130	0.068	48	Yes	0.60×0.80
[84]	130 nm CMOS	0.125 – 8.5	0.18	18	Yes	0.097×0.13
[85]	130 nm CMOS	7 – 70	0.156	24	No	0.18×0.38
[86]	250 nm SiGe	7 – 20	7.2	52	No	0.52×0.82
This Work	130 nm CMOS	2 – 40	3.2	23	Yes	0.40×0.40

3.4 Summary

This Chapter has presented a single branch 2-40 GHz logarithmic power detector showing better than 15 dB return loss and close V_{out} vs. P_{in} response over frequency. The

single branch power detector shows a 23-dB dynamic range with a ±1.5 dB log error at room temperature. The log detector was measured over temperature to verify the normal circuit operation across temperature. However, additional temperature compensation circuitry is required to improve log error over temperature. The single branch log detector design occupies 0.40×0.40 mm^2 core area and consumes 3.2 mW static DC power with a 2-V supply.

The exponential DC I-V characteristic of SiGe HBT naturally makes it a good candidate for a log amplifier design to achieve the linear-in-dB power detector transfer characteristic. Dedicated analog on-chip bias circuitry is included to ensure stable bias over temperature and to achieve desired DC output voltage shifting. Overall, the SiGe BiCMOS technology that provides both high performance SiGe HBTs and modest performance MOSFETs proofs to be an ideal technology for this implementation of the log amplifier.

CHAPTER 4. MILLIMETER-WAVE SWITCH DESIGN WITH SIGE BICMOS TECHNOLOGY

4.1 Introduction

RF and mm-wave switches are important elements in modern front-ends for pulsed radar and wireless communication applications, as they enable transmit/ receive mode toggling, circuit reconfiguration, and performance calibration. For front-end switch designs, low insertion loss is required to ensure high transmitter efficiency and modest receiver noise figure. High power-handling capability is also a critical criterion for switch design, in order to prevent signal distortion at high transmitted output power levels. Additionally, high isolation is also an important design concern for preventing undesired signal leakage among the signal ports.

PIN diodes and SiGe HBTs have higher C_{OFF} given an R_{ON} compared to that offered by bulk FETs. Moreover, PIN diode and SiGe HBT switches offer better power handling capabilities than CMOS switches at a similar technology node, due their relatively high turn-on voltages. The only main difference between switch design using SiGe PIN diode or SiGe HBT and using FETs is that the bipolar devices require a DC quiescent current to be properly biased. Although seemingly trivial, the biasing techniques in SiGe PIN diode and SiGe HBT switches are indeed worthy of discussion.

4.2 A Compact High-Power SPDT Switch Using Shut-Series SiGe PIN Diodes

SiGe PIN diodes in general have better C_{OFF} given a R_{ON} and have higher turn on voltage as compared to both CMOS and SiGe HBTs, all of which are beneficial for

designing low loss and high power mm-wave switches [87]. As illustrated by the SiGe PIN diode cross-section in Figure 4.1, the anode is formed by the SiGe HBT base epitaxial film , the intrinsic region is formed by silicon epitaxial growth, and the cathode is formed by a deep n+ implant with an n+ reach through for cathode contact. Derived from the B-E junction formation process of SiGe HBTs, the profile of the SiGe PIN diode is further optimized to improve the performance at mm-wave frequencies.

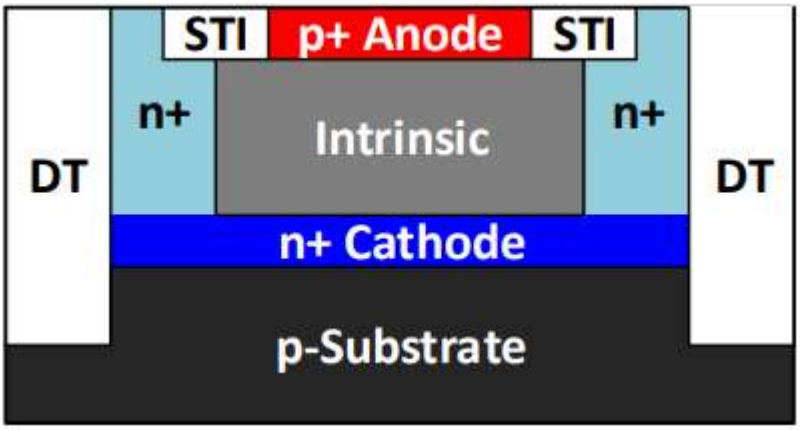


Figure 4.1 – Cross-section of a vertical SiGe PIN diode [31] © 2014 IEEE.

In practice, however, biasing PIN diode switches to fully take advantage of their power handling capability is not straight forward. The most common way to bias SiGe HBTs and PIN diodes in switch designs is to use transmission line stubs to present high impedance, or to resonate with off-capacitance of the devices at the operating frequencies while presenting a low impedance at DC [30], [31], and [87], as illustrated in the simplified typical series-shunt and λ/4-shunt PIN diode SPDTs shown in Figure 4.2. Despite short physical length at millimeter-wave frequencies, the biasing transmission lines still inevitably occupy a significant portion of the total footprint of the switch design, even with meandering.

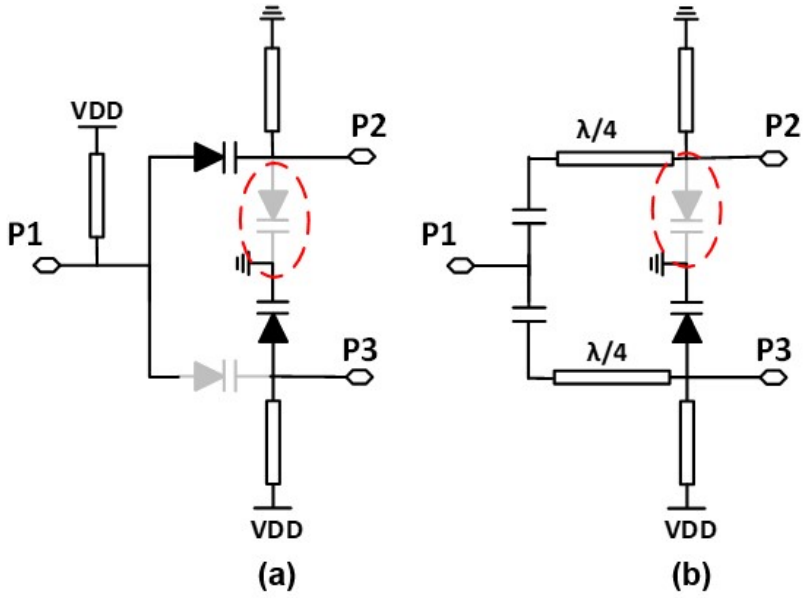
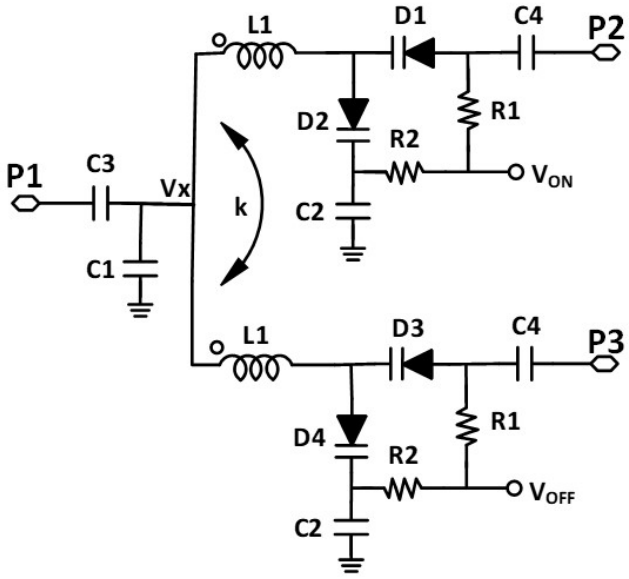


Figure 4.2 – Simplified schematic of (a) series-shunt and (b) λ/4-shunt PIN diode switches with P1 as the antenna port, P2 as the thru port, and P3 as the isolation port. The off-state shunt diodes, circled in the schematics, are usually the limiting factor of the SPDT designs [4] © 2019 IEEE.

Biasing PIN diodes and SiGe HBTs with resistors, on the other hand, is a more desirable alternative in term of circuit compactness, but requires higher bias voltage and power consumption since, unlike CMOS devices, PIN diodes and SiGe HBTs require significant DC bias current to be turned on. The choice of bias resistance value also requires extra attention, since a bias resistance that is too low will lead to RF signal leakage and thus higher insertion loss, while a bias resistance that is too high may cause voltage clipping at high input power level and thus lead to early compression. In addition, for SiGe PIN diodes and SiGe HBT switch designs, to achieve enhanced linearity, reverse bias on the shunt device is often needed [30], [31].

In this section, a resistively biased shunt-series SiGe PIN diode 60 GHz SPDT switch design is proposed for enhanced power handling capability of the switch without the need for additional negative bias. This work was previous presented in [4].



C1	60 fF
C2	1.5 pF
C3	380 fF
C4	465 fF
L1	100 pH
k	0.4
R1	2 kΩ
R2	100 Ω
D1, D3	9 μm^2
D2, D4	16 μm^2
$V_{ON/OFF}$	5 V/ 0 V

Figure 4.3 – Schematic, passive component values and bias condition of the proposed 60 GHz SiGe PIN diode SPDT switch design [4] © 2019 IEEE.

4.2.1 Circuit Design

The schematic, passive component values, and bias conditions of the proposed SPDT switch topology are shown in Figure 4.3.This novel switch topology is constructed using two identical branches, with shunt diodes D_2 and D_4 placed before series diodes D_1 and D_3. When routing a signal between ports P1 and P2, 5 V is applied on V_{ON} with the V_{OFF} node pulled to ground, and D_1 on the thru path and D_4 on the isolation path are thus turned on. A potential difference is established between V_{ON} and V_X, which equals the voltage drop across R_1 and D_1. The off-state diode D_2 is reverse-biased by this potential difference. This helps to prevent D_2 from turning on when a large voltage swings across its

cathode and anode at high power levels, and hence improves the P_{1dB} of this SPDT switch design.

Given a supply voltage and desired diode ON current, the sum of R_1 and R_2 could be readily estimated. The voltage across D_2 can be effectively engineered by changing the resistance ratio between R_1 and R2. To obtain a large reverse-bias voltage across D_2 and to prevent RF signal leakage through R_1, a large R_1 value of 2 kΩ is chosen for this design. A relatively small resistance value of 100 Ω is used for R_2 to minimize its voltage headroom consumption. However, the impedance of R_2 is still much greater than that of C_2 (1.8 Ω at 60 GHz), preventing undesired RF signal coupling into the bias network.

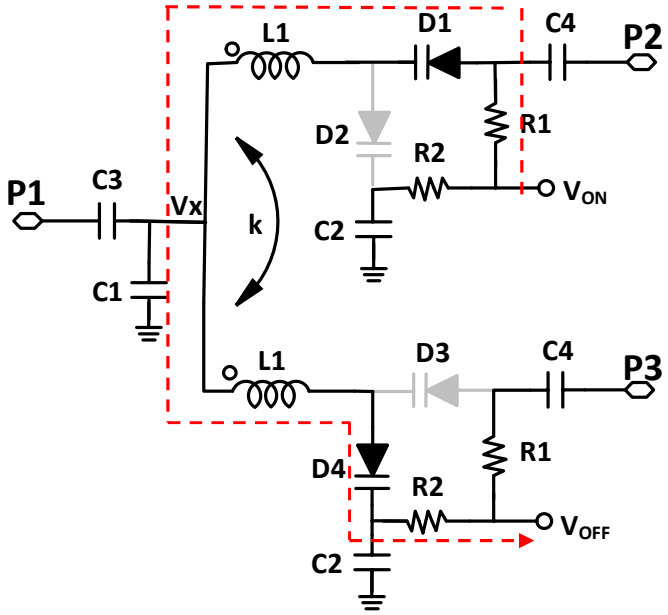


Figure 4.4 – Circuit operation when P2 is the thru port. The red dotted arrow indicates the DC current path [4] © 2019 IEEE.

The matching network of the proposed design uses a C-L-C pi-network topology similar to that presented in [88], except instead of using two individual lumped inductors, coupled inductors are used. The small signal equivalent circuit of configuration in Figure

4.4 is as shown in Figure 4.5(a). For simplicity, the DC blocking capacitor C_3 and C_4, RF shorting capacitor C_2, and bias resistors R_1 and R_2 are neglected. Assuming the R_{ON} of the diodes is small, the equivalent circuit of the thru path between P1 and P2 can be further simplified to as shown in Figure 4.5(b). The use of coupled inductors reduces the total area required for the matching network, since it reduces the amount of self-inductance needed for matching and occupies one inductor footprint instead of two. The coupling factor also provides another degree of freedom for matching network optimization.

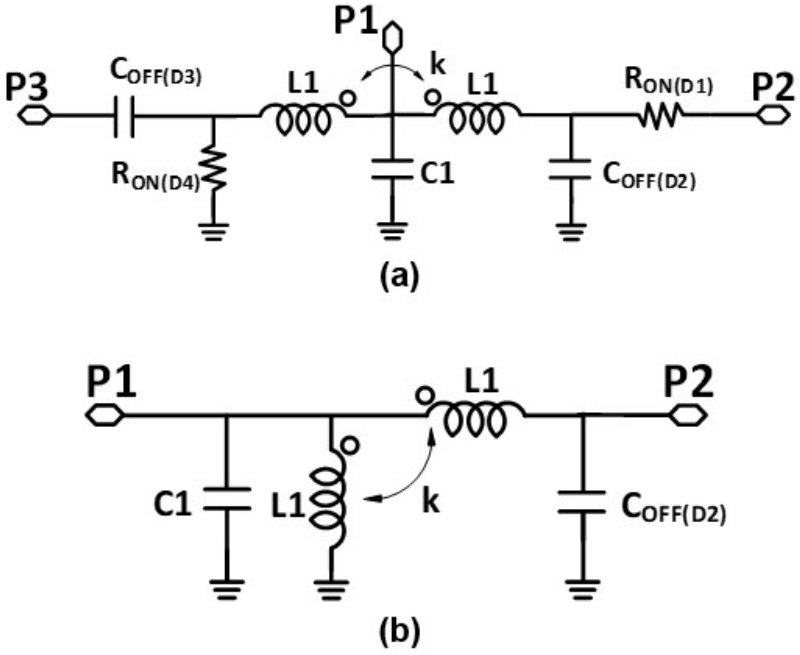


Figure 4.5 – (a) Simplified small signal equivalent circuit of Figure 4.4, and (b) further simplification of (a) [4] © 2019 IEEE.

4.2.2 Measurement Results

The SPDT switch was designed and fabricated using the 130 nm GlobalFoundries 8HP SiGe BiCMOS process (f_T/f_{MAX} = 200/ 265 GHz) using the 7AM BEOL option. Figure 4.6 shows the chip microphotograph of the design where P3 is 50 Ω terminated with an on-

die resistor. The active chip area is 0.20×0.33 mm^2. The circuit consumes 8.5 mW of DC power under 5.0 V bias.

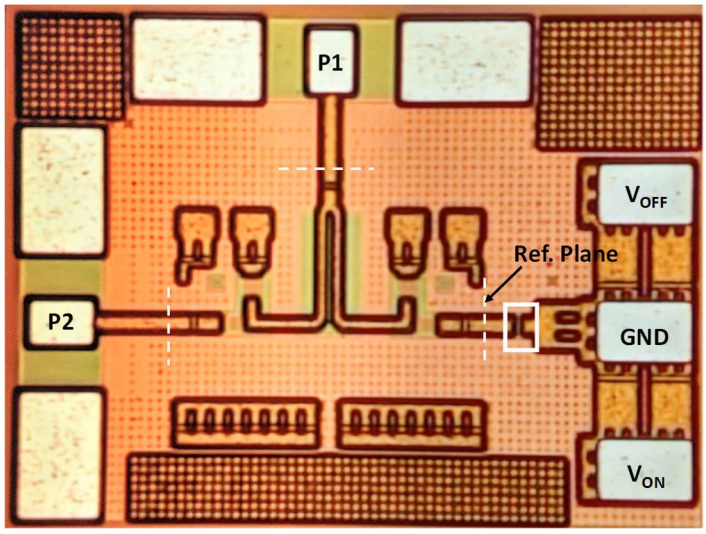


Figure 4.6 – Chip microphotograph of the proposed PIN SPDT switch with P3 terminated with on die 50 Ω resistor [4] © 2019 IEEE.

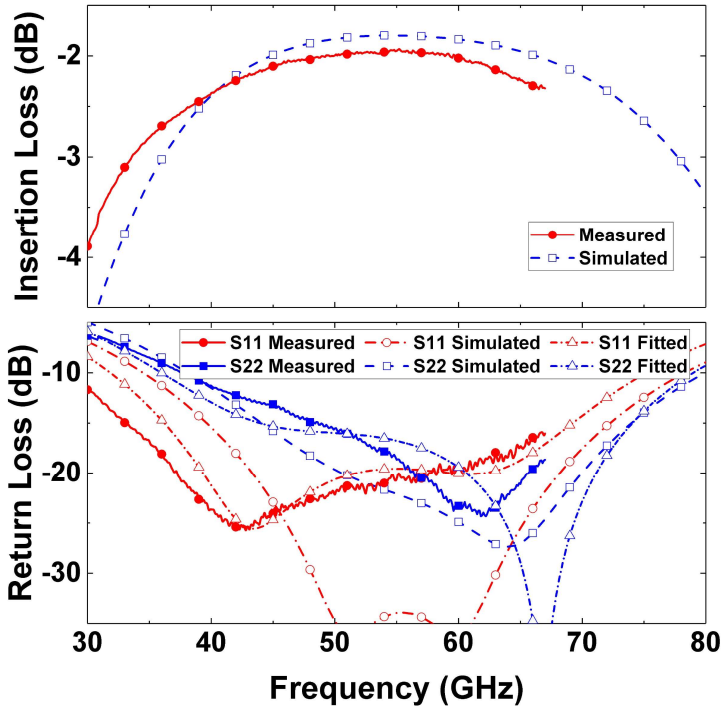


Figure 4.7 – Simulated and measured insertion loss and return loss of the proposed PIN SPDT switch [4] © 2019 IEEE.

A Keysight E8361C PNA was used for on-wafer S-parameter measurements from 30 GHz to 67 GHz. The measurement was de-embedded to the reference plane (shown in Figure 4.6) using a multi-line TRL calibration method. The simulated and measured insertion loss and return loss are plotted in Figure 4.7. The simulated input and output return loss could be reasonably fitted to the measurement by adding two single L-C sections of 5 *f*F shunt capacitor and a 6 pH series inductor before the two shunt PIN diodes. The measured minimum insertion loss of the switch is 2.0 dB, and the insertion loss remains less than 2.5 dB from 38 to beyond 67 GHz. The measured S_{11} and S_{22} are less than -10 dB from 37.8 GHz to beyond 67 GHz. The measured isolation between Rx/Tx to the antenna port is greater than 23 dB up to 67 GHz, and the measured isolation between the Tx and Rx port is greater than 26 dB up to 67 GHz, as shown in Figure 4.8.

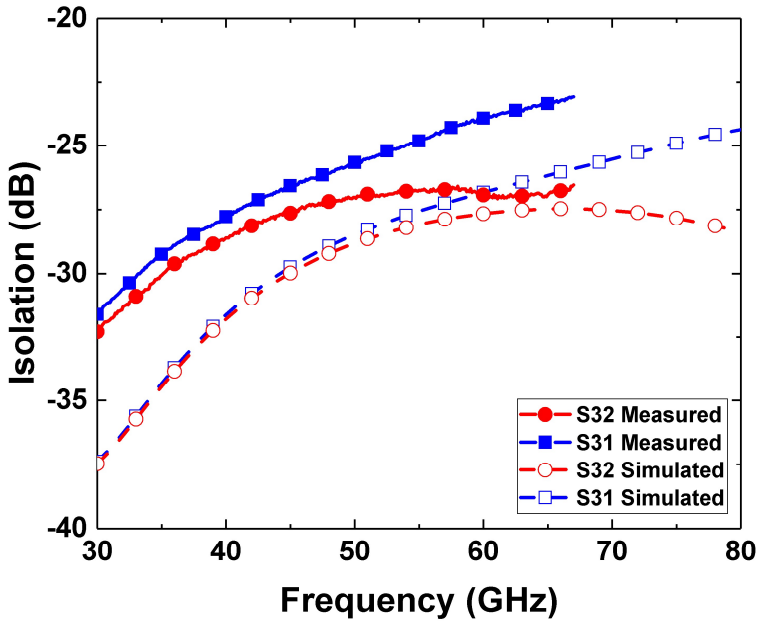


Figure 4.8 – Simulated and measured switch isolation of the proposed PIN SPDT switch [4] © 2019 IEEE.

The IP_{1dB} of the SPDT switch is measured on-wafer using a pair of 100 µm pitch WR-15 waveguide probes at 60 GHz. The signal source setup consists of an OML S15MS source module, a Millitech 53-70 GHz power amplifier, and a Quinstar mechanical attenuator. The input and output power are measured using a 10 dB WR-15 directional coupler and a pair of Keysight V8486 series waveguide power sensors. The loss of the isolators and waveguide components were carefully measured and accounted for, but the pad loss is not de-embedded from this measurement. The measured IP_{1dB} of the proposed SPDT switch is 22 dBm at 60 GHz, as shown in Figure 4.9. Table 4.1 compares the performance of the proposed shunt-series PIN diode SPDT switch with other state-of-the-art millimeter-wave switches. A high P1dB is achieved with the proposed shunt-series topology without the need for a secondary negative bias level. Though the addition of series diodes incurs some additional loss for the SPDT, the insertion loss of the design remains competitive with the performance of other state-of-the-art designs.

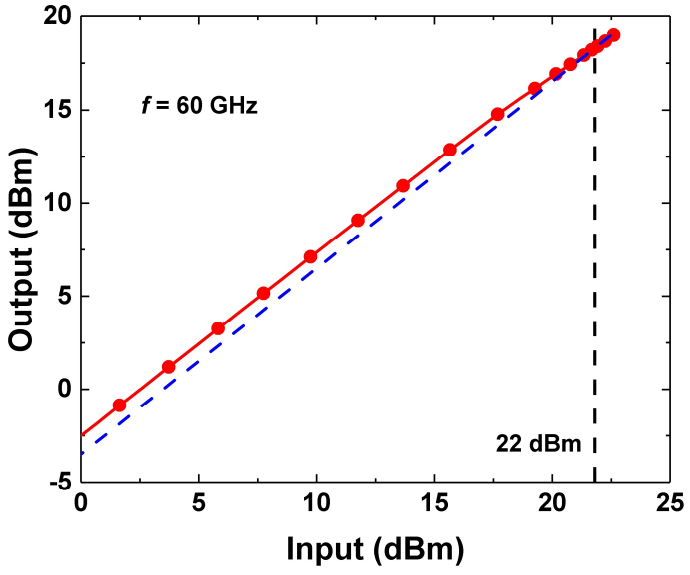


Figure 4.9 – Measured P_{1dB} of the proposed PIN SPDT switch at 60 GHz [4] © 2019 IEEE.

Table 4.1 – Performance Comparison with mm-wave SPDT Switches [4]

	Tech	Device	Topo.	Freq (GHz)	Min IL (dB)	RL (dB)	Iso (dB)	IP1dB (dBm)	P_{DC} (mW)	Core Area (mm^2)
[30]	90 nm SiGe	SiGe HBT	λ/4-shunt	73 – 110+	1.1	> 10	22	17/ 22*	5.9	0.213
[31]	90 nm SiGe	PIN Diode	λ/4-shunt	73 - 133	1.4	> 10	19 – 22	> 24+*	10.2	0.14
[87]	130 nm SiGe	PIN Diode	Series-shunt	50 – 78	2.0	> 12	22 – 35	-	16.8	0.11
[89]	90 nm CMOS	NFET	λ/4-shunt	50 – 70	1.5	> 8	25 – 30	13.6	-	0.27
[90]	65 nm CMOS	NFET	Lumped 4-way comb.	58 – 85	1.8	> 10	22 – 30	10	-	0.015
[91]	45 nm RFSOI	NFET	Series-shunt	DC – 60	2.5 @ 60 GHz	> 10	> 25	9.6	-	0.040
This Work	130 nm SiGe	PIN Diode	Shunt-series	38 – 67+	2.0	> 10	> 23	22	8.5	0.066

* Negative supply used

4.2.3 Summery

The resistive bias network of the proposed design takes advantage of the DC bias current required to turn on the PIN diodes to generate voltage drop to reverse bias the off-state PIN diodes. This biasing scheme prevents the shunt diode from turning on by the large voltage swing across its anode and cathode at input high power levels, and thus leads to an improved P_{1dB}. Though the use of series diode on the signal path incurs some additional insertion loss compared to topologies using only shunt devices, the overall insertion loss of the proposed design remains competitive with the state-of-the-art millimeter-wave SPDT switch designs. The use of series diode also helps to ensure a good port-to-port isolation.

4.3 MM-Wave Switch Using Reverse-Saturated SiGe HBTs in Grounded Emitter (GE) vs. Floating Emitter (FE) Configurations

Although SiGe PIN diodes in general promise better RF and mm-wave performance compared to SiGe HBTs and nFETs, they are not necessarily available in all the SiGe BiCMOS technologies. For SiGe BiCMOS designs where shunt switching is needed, reverse-saturated SiGe HBTs are often used. As discussed in Chapter 1, SiGe HBTs, when configured in the reverse-saturated mode, promise better switching performance compared to forward-saturated HBTs and FETs.

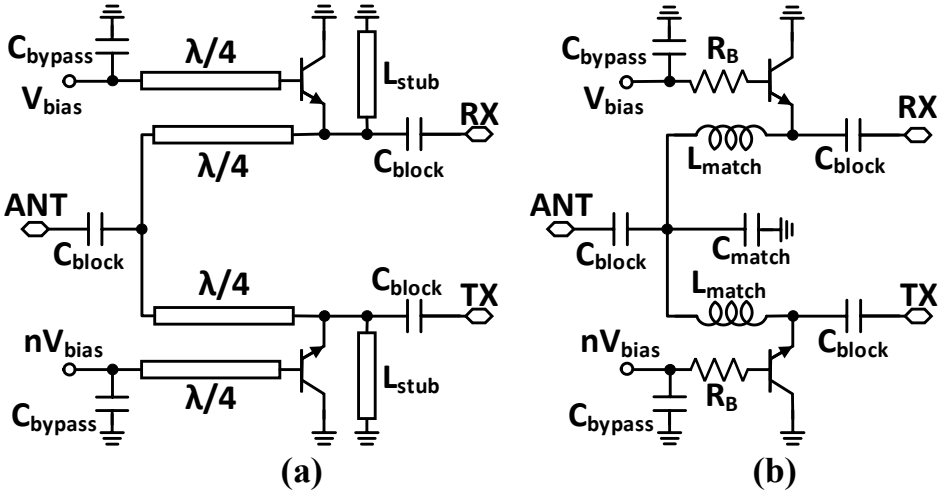


Figure 4.10 – Circuit schematics of (a) conventional quarter-wave shunt SPDT switch design with short shunt stubs in parallel with HBTs, and (b) C-L-C π-network switch [5].

The use of reverse-saturated SiGe HBTs has been widely embraced by engineers in switch designs for difference applications from down to 5 GHz to up to D-band [92]-[95]. However, the ways in which the reverse-saturated SiGe HBTs are biased, particularly at the emitter node, vary among these designs. In the conventional quarter-wave shunt

SPDT design demonstrated by [30] as shown in Figure 4.10(a), shunt short stubs are used in parallel with the SiGe HBTs to resonate with the capacitance of the SiGe HBTs at the intended frequencies of operation. For SiGe HBTs biased in saturation, both the B-E and B-C junctions are forward-biased and DC current flows out of both emitter and collector nodes. Although seemingly trivial, the short stubs in Figure 4.10(a) provide a DC current path for the B-E junction current of the ON-state SiGe HBT. For applications operating at lower mm-wave frequencies, and applications where SPDT switch with more compact footprint is desired, C-L-C π-network switches, as shown in Figure 4.10(b), are preferred alternatives, where resistors are used for base bias and the capacitance of the SiGe HBTs are absorbed into the π-network. Upon closer examination of the DC current flow path in Figure 4.10(b), however, one can notice that the ON-state SiGe HBT presents the desired low ON AC impedance (R_{ON}), even with emitter node DC-floating.

As mentioned in section 1.2.4, also reiterated by the SiGe PIN diode switch example in the previous section, the choice of bias scheme has tremendous effect on the overall performance of circuit designed with bipolar devices. In this section, the differences between the grounded emitter (GE) and floating emitter (FE) configured reverse-saturated SiGe HBTs switches are compared through a W-band SPDT switch test structure designed in a 130 nm SiGe BiCMOS technology. This work has been submitted to the 2021 IEEE/ MTT-S International Microwave Symposium [5].

4.3.1 TCAD Simulation and Test Structure Design

This atypical behavior of the floating emitter configured reverse-saturated SiGe HBT was noted and validated by C. T. Coen in [55] with physics-based technology CAD

(TCAD) simulations performed on a calibrated 4th-generation SiGe HBT model. At high base bias, the B-E junction is forward-biased, even with the emitter node DC floating. The E-B junction potential barrier height differs in the two configurations but converges as the base bias increases. For the FE configured SiGe HBT biased in the ON-state, electron current flow moves from the base into the intrinsic emitter along the E-B spacer oxide interface and are swept across base into the collector, as shown by the current streamlines in Figure 4.11. TCAD simulations further confirm that the small-signal impedance of ON-state SiGe HBTs in the two configurations are identical.

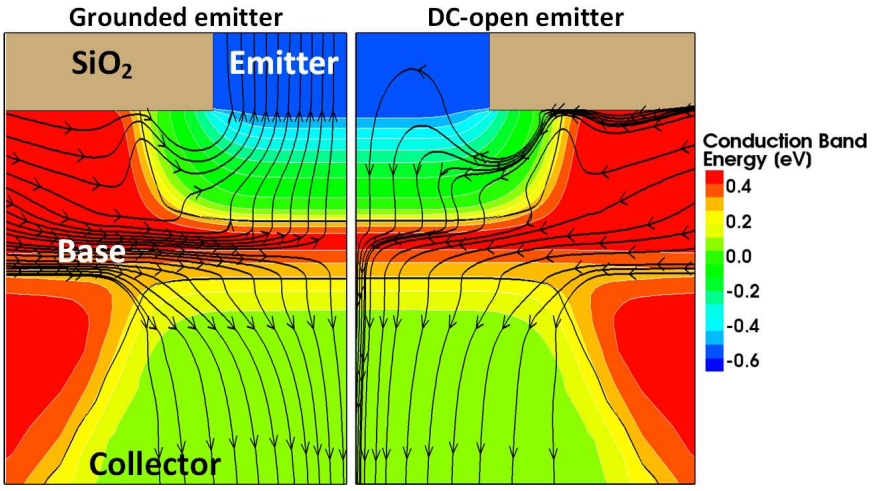


Figure 4.11 – 2-D cross-section of the TCAD SiGe HBT biased in the ON-state, showing simulated conduction band energy contours and streamlines of the internal electron current flow. The emitter is grounded for the left half-device and is floating for the right half-device [55].

Although [55] validated that using a floating emitter does not affect the small-signal performance of the SPDT switch, the effects of the FE configuration on other aspects of the switch performance were not discussed. Therefore, a W-band SPDT switch test structure was designed as a test vehicle to validate the TCAD simulation results and to

examine the performance differences between switches with GE and FE configured reverse-saturated SiGe HBTs.

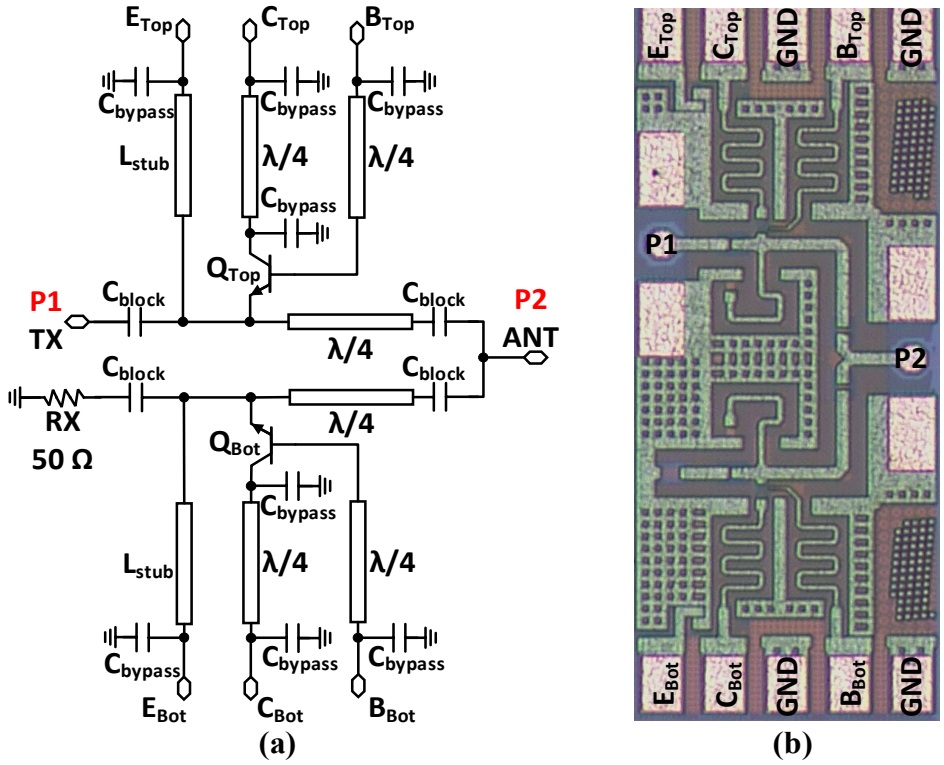


Figure 4.12 – (a) The schematic and (b) chip micrograph of the W-band SPDT test structure. The dimensions of the test structure are 1.18 × 0.48 mm^2 including bondpads [5].

The W-band SPDT test structure was designed and fabricated using TowerJazz SBC18-H3 130 nm SiGe BiCMOS technology, which features 240 GHz f_T and 270 GHz f_{MAX} SiGe HBTs The schematic of the W-band SPDT switch test structure is shown in Figure 4.12(a), and the chip micrograph in Figure 4.12(b). The dimensions of the test structure are 1.18 × 0.48 mm^2 including bondpads. Both the top and bottom SiGe HBTs (Q_{Top} and Q_{Bot}) consist of two parallel 5 μm CBEBC devices with a shared sub-collector.

A modified quarter-wave shunt topology is adopted for the test structure, with a few key modifications:

1. Shunt stubs (L_{stub}) are AC grounded through the bypass capacitor network but connected to bondpads (E_{Top} and E_{Bot}) DC-wise to allow the same test structure to be measured in both the GE and FE configurations. The bypass capacitor networks are carefully designed and simulated to ensure the DC loading on the bondpads do not affect the impedance presented to the emitters at the frequencies of operation.
2. AC grounds are used at the collectors the SiGe HBTs to allow DC access to the transistor collectors. This enables forward Gummel measurements of the devices to be measured, which provides valuable information on the level of damage the devices experience under RF stress conditions.
3. Two DC blocking capacitors are used near the antenna port (P2) to DC-decouple Q_{Top} and Q_{Bot} from each other.

4.3.2 Measurement Results and Observations

4.3.2.1 Measurement Setup

The measurement was setup as shown in Figure 4.13. GSG waveguide probes with 100 μm pitch were used for on-wafer measurements. A Keysight 4155C semiconductor parameter analyzer was used for SiGe HBT DC characterization and as a DC supply. The small-signal measurements were performed using a Keysight E8361C PNA with OML W-band frequency extenders. The large-signal power sweep and high-power RF stressing were achieved with a OML W-band source module, a Millitech VCA, and a Millitech 90-96 GHz PA. A frequency of 92 GHz was chosen for IP_{1dB} measurements and RF stressing,

since the large-signal setup delivers the maximum available power at this frequency. To enable fast and convenient switching between small-signal and large-signal measurements, a pair of Flann Microwave mechanical W-band waveguide switches was incorporated in the setup.

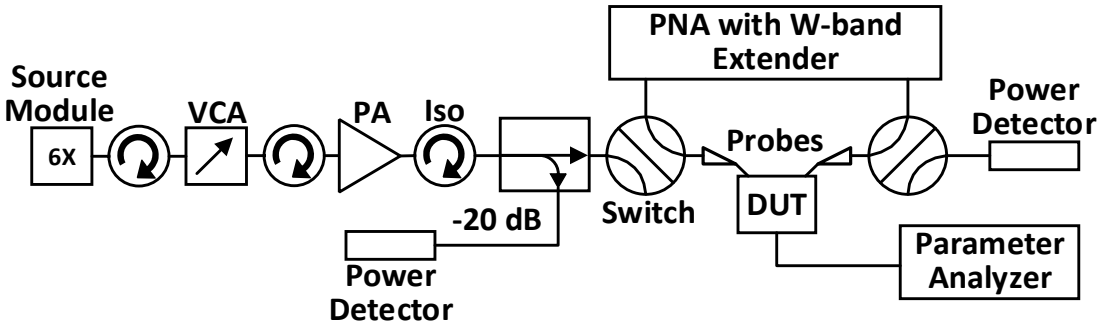


Figure 4.13 – Block diagram of the measurement setup [5].

4.3.2.2 DC Measurement Results

With the collector node grounded, the base current (I_B) of SiGe HBTs in GE and FE configurations were measured with the base voltage (V_B) swept from 0.8 V to 1.0 V, shown in Figure 4.14(a). At 1.0 V V_B, the FE configuration I_B is 80% of that measured in GE configuration. Since the PDK compact model is not well calibrated to the reverse saturated operation, this difference in I_B was not captured by the PDK simulation. Therefore, to further validate the I_B difference in GE and FE SiGe HBT, similar measurements were performed on a 10 μm GlobalFoundries 130-nm 8HP (200/ 265 GHz f_T/f_{MAX}) device and a 12 μm GlobalFoundries 130-nm 8XP (250/ 340 GHz f_T/f_{MAX}) device. The percentage I_B of the SiGe HBTs in FE configuration with respect to I_B in GE configuration are plotted in Figure 4.14(b). Although the percentage I_B over V_B varies,

observe that, with 1.0 V V_B, the I_B in FE configuration is consistently lower than that measured in GE configuration across the three processes being tested.

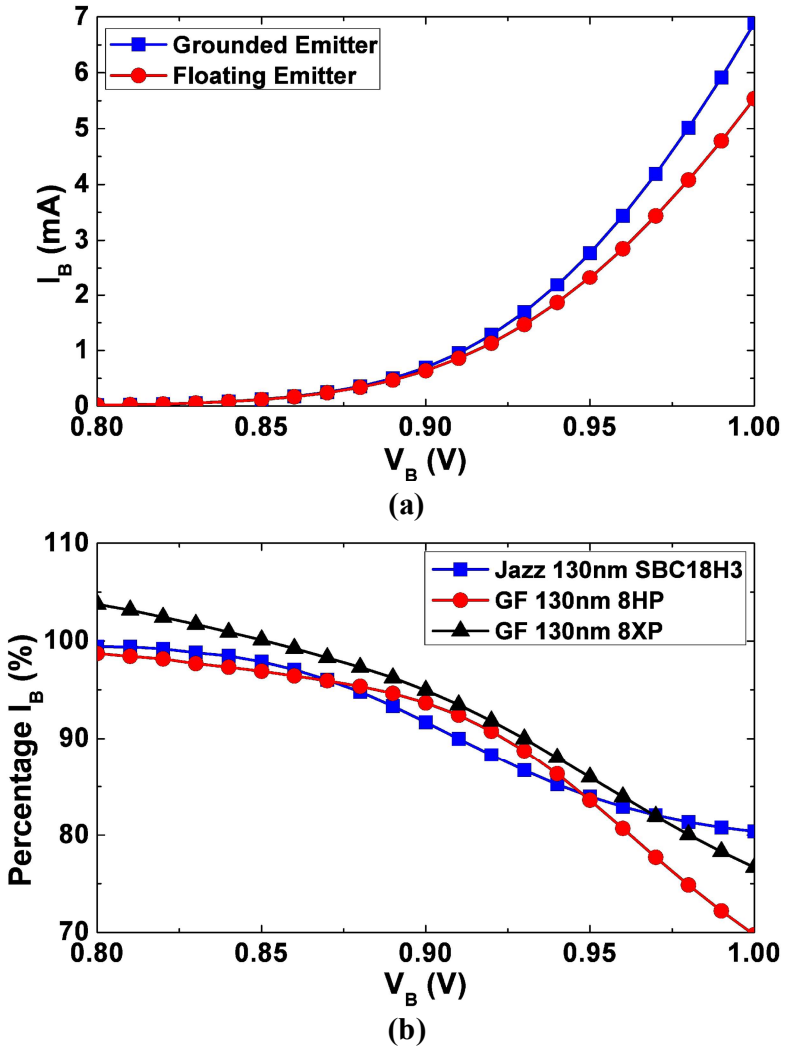


Figure 4.14 – Measured (a) I_B vs. V_B of HBT in switch test structure in GE and FE configurations, and (b) percentage I_B in FE configuration w.r.t. I_B in GE configuration vs. V_B of 2×5 µm Jazz SBC18H3, 10 µm GF 8HP, and 12 µm GF 8XP devices [5].

4.3.2.3 Small-Signal Measurement Results

The small-signal performance of the switch test structure was first measured with the emitter bondpads of the SiGe HBTs grounded, by setting the corresponding Keysight

4155C emitter biasing channels to 0 V. The small-signal performance of the switch test structure was then measured again with the channel disabled. The measurement results are compared in Figure 4.15.

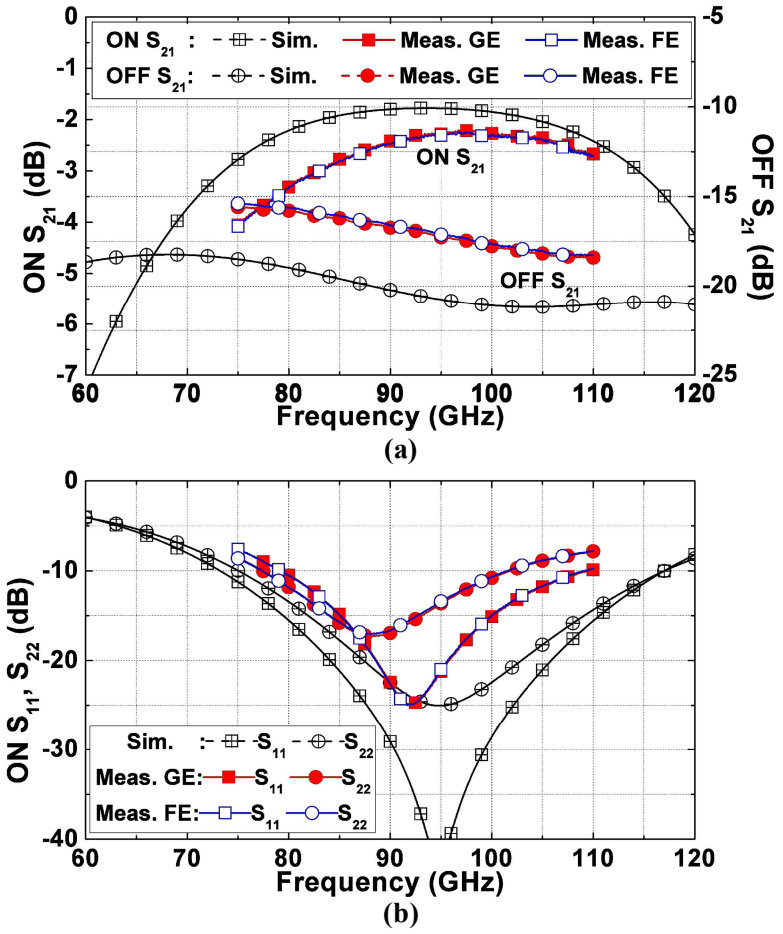


Figure 4.15 – Measured and simulated (a) S_{21} in both ON and OFF state, and (b) S_{11} and S_{22} in ON state operation [5].

The measured small-signal performance of the switch in GE and FE configurations are identical. The measured minimum insertion loss is 2.3 dB and the measured return loss was better than 10 dB between 79.2 GHz and 109.2 GHz. In simulation, the small-signal performance of the GE and FE configured switches are identical as well. The differences between measurement and simulation results are likely due to PDK reverse-saturated SiGe

HBT modelling and EM simulation inaccuracy. Nonetheless, the small-signal measurement results confirm the conclusion from the TCAD simulations that the small signal impedance presented by the reverse-saturated SiGe HBT in GE and FE configurations are identical.

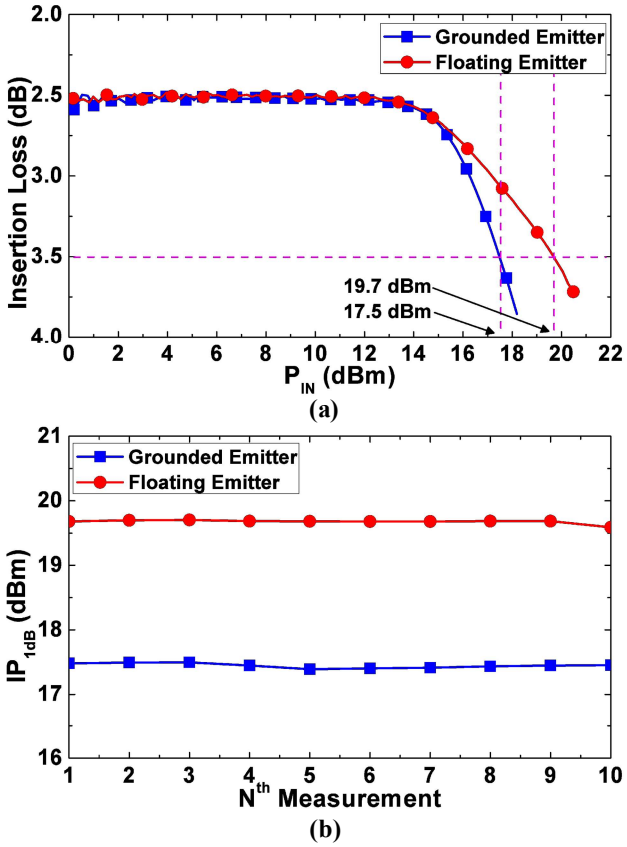


Figure 4.16 – Measured (a) insertion loss of the GE and FE configured test structures vs. P_{IN}, and (b) the IP_{1dB} of the GE and FE test structure over 10 measurements. The GE configured switch showed 17.5 dBm IP_{1dB} and the FE switch demonstrates 19.7 dBm IP_{1dB} [5].

4.3.2.4 IP_{1dB} Measurement Results

The IP_{1dB} was measured on two test structures, with one biased in GE configuration and the other in FE. The DC and small-signal measurements were first performed on these

two fresh test structures to verify the normal operation of both circuits. Power sweep was then performed at 92 GHz, with input power injected from the *TX* port. To prevent excessive damage to the devices from high input, the power sweep stopped roughly 0.5 dB past when 1-dB compression had been reached. The insertion loss vs. P_{IN} of the GE and FE test structures is plotted in Figure 4.16(a). The GE configuration demonstrates 17.5 dBm IP_{1dB}, whereas the FE configuration shows 2.2 dB higher IP_{1dB} at 19.7 dBm with a more gradual roll-off. This suggests that the power handling capability of RF switches with the conventional GE reverse-saturated SiGe HBTs can be improved by simply floating the emitters. To ensure the repeatability of this P_{1dB} result, the same power sweep was performed 10 times on both test circuits, and the measured IP_{1dB} over 10 measurements are plotted in Figure 4.16(b).

4.3.2.5 RF Stress

Thus far, the FE configured test structure shows identical small-signal performance compared with its GE counterpart, but demonstrates lower DC power consumption and superior power handling capability. However, to establish the reverse-saturated SiGe HBT with floating-emitter as a reliable alternative to the conventional topology, it is important to demonstrate that this unconventional biasing scheme does not lead to performance degradation over time for the switch.

After the IP_{1dB} measurement sweeps described in the previous subsection, a 23.3 dBm (0.5 dB lower than the maximum available power) input power was applied at *P1* of the GE and FE configured switch test structures at 92 GHz to provide high-power RF stress for accelerated aging. With the measurement setup in Figure 4.13, the input power level

was monitored and the VCA bias voltage was updated roughly every *10 sec* to ensure that P_{IN} stayed with ±0.2 dB of 23.3 dBm.

Before the IP_{1dB} power sweeps, the forward Gummel characteristics of Q_{Top} were measured, with 0 V V_{CB}, as a reference of pre-stress device performance. Forward Gummel data of the same SiGe HBT was measured again after the power sweeps to check for damage to the device from IP_{1dB} measurement. The two test structures were biased in ON state (1.0 V at B_{Bot} with B_{Top} grounded) and stressed for an accumulated *10,000 sec* period. The stress was interrupted at cumulative intervals of *100*, *200*, *500*, *1,000*, *2,000*, and *5,000 sec* for Gummel and IP_{1dB} measurements to record potential changes to device damage Level, as well as performance degradation over the period of stress. DC, small-signal, and large-signal measurements were repeated on two fresh GE and FE configured test structures, and these two structures were stressed for *10,000 sec* with 23.3 dBm P_{IN} in the OFF state (1.0 V at B_{Top} with B_{Bot} grounded).

Figure 4.17 shows the measured forward Gummel characteristics of Q_{Top} before the IP_{1dB} power sweeps, after the sweeps, and over the ON-state RF stress. In the GE configured switch, P_{IN} sweep up to and slightly beyond IP_{1dB} causes slight base current leakage to Q_{Top} at low-injection region. Over high-power RF stress, more damage accumulated at the B-E junction, as manifested by the increase in low-injection base current leakage over time. The Q_{Top} in FE configured switch, on the other hand, experienced substantially higher level of device damage even before the RF stress. With the 23.3 dBm RF stress, the peak beta dropped from close to 1000 to below 200. From the forward Gummel plots, the FE configured SiGe HBT is clearly more susceptible to RF stress induced damage compared with its GE counterpart.

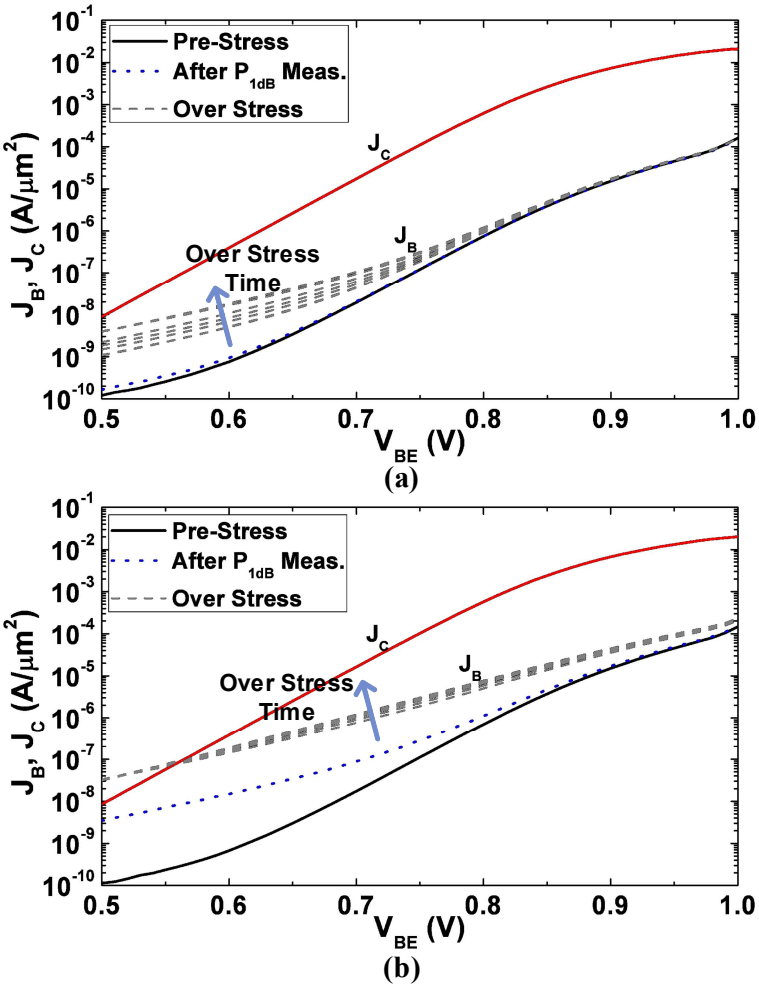


Figure 4.17 – Measured Gummel characteristics with 0 V V_{CB} of Q_{Top} before power sweep, after sweep, and over the period of *10,000 s* ON state RF stress in (a) GE configured and (b) FE configured switches [5].

However, interestingly, and significantly, the measured insertion loss and IP_{1dB} over the period of stress (Figure 4.18) did not show any degradation in both GE and FE configured switches, despite of the drastic difference in device damage levels. In other words, the RF stress induced device damage does not degrade the performance of the SPDT switch with either GE or FE reverse-saturated SiGe HBTs.

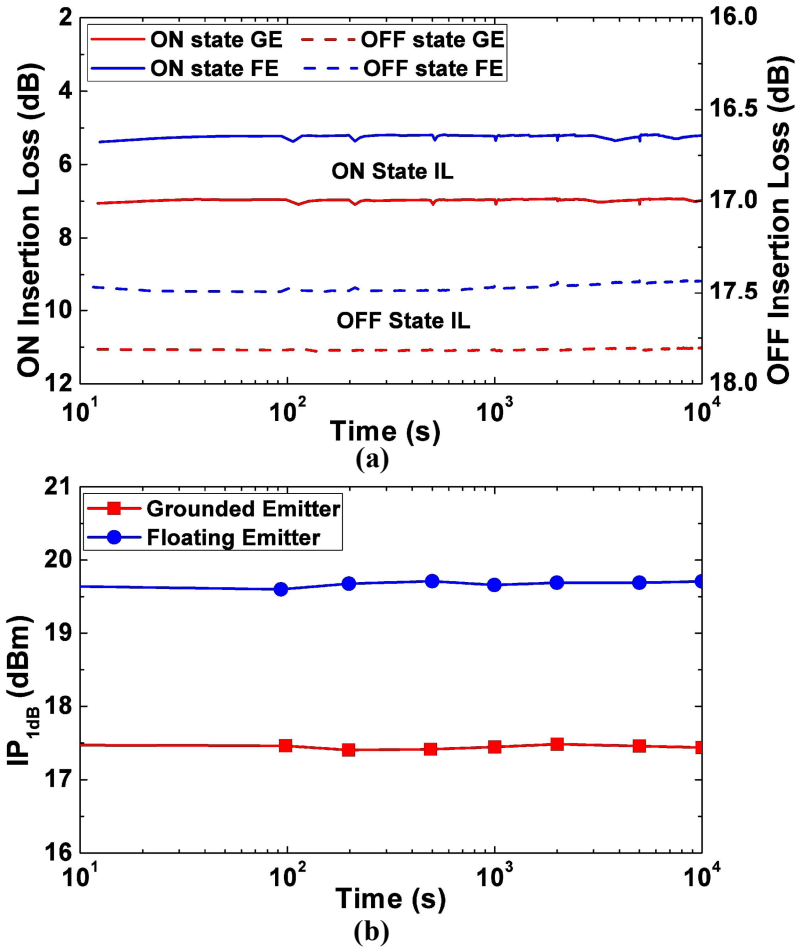


Figure 4.18 – (a) Measured insertion loss of the GE and FE configured switches in ON and OFF state with 23.3 dBm input power at 92 GHz, and (b) measured IP_{1dB} (at 92 GHz) of the GE and FE configured switches between stress intervals [5].

4.4 Summary

A W-band modified quarter-wave shunt SPDT switch test structure has been designed using 130-nm TowerJazz SBC18-H3 SiGe BiCMOS process to examine the performance differences between switches with GE and FE reverse-saturated SiGe HBTs. By simply leaving the emitter DC floating, the switch, while maintaining identical small-signal performance compared with switch using GE SiGe HBTs, promises less distortion to high power signal with less DC power consumption. Although the SiGe HBT in FE

configuration is more suspectable to damage from RF stress, measurement results show that damage in SiGe HBT do not degrade the performance of the switch, thus opening the way for their use.

CHAPTER 5. A HIGH-POWER 60 GHZ SIGE BALANCED POWER AMPLIFIER

5.1 Introduction

To address the exponentially growing data rate demand, the industry and academia are envisioning to employ mm-wave frequency spectrum for 5G communication systems and beyond. To achieve reasonable circuit performance at mm-wave frequencies, device technologies offering high f_T and f_{MAX} are often required. The choice of design platform is traditionally filled by high performance III-V technologies, but with recent development, the presence of RF CMOS and SiGe BiCMOS technologies in mm-wave PA designs have increased significantly. The clear advantages of SiGe BiCMOS and RF CMOS technologies over III-V technologies are their high yield and larger-scale integration capability. However, silicon-based technologies in general have lower breakdown voltage compared to III-V technologies, which present challenges to designs with high power and high power density.

Numerous techniques have been proposed to address this issue. Transistor stacking is a technique commonly used in SiGe BiCMOS and RF CMOS PA designs to improve the power handling capability of power cells by distributing the voltage swing across the stacked transistors [96]. Although effective in addressing the low sustainable voltage swing of single SiGe HBT or MOSFET device, this approach leads to increased design complexity and is restricted by concerns such as the increased parasitics. In addition to power cell design and optimization techniques such as cascode and stacking, power

combining techniques play crucial roles in increasing the maximum output power of PA designs.

Over the years, researchers have successfully demonstrated numerous power combining approaches at mm-wave frequencies. The direct shunt power combining is arguably the simplest, where power cells are placed in parallel and the output current and power of each cell are combined directly [97], [98]. Power combining with a Wilkinson combiner is another in-phase parallel power combining scheme with improved power cell isolation compared to the direct power combining method [99]. The availability of high quality multiple layered BEOL in SiGe BiCMOS and RF CMOS technologies enables realization of 3-D passive structures that open up more sophisticated ways for power combining. Series combining techniques based on couplers and inductive transformers have become common practice in silicon-based PA designs to achieve simultaneous impedance transformation and power combining with a compact footprint [100]-[110]. Recently, three-conductor T-line based sub-quarter wavelength baluns were introduced as promising alternatives to the popular transformer-based power combining scheme, especially when low inductor Q, inter-winding capacitance, and substrate loss pose significant design challenges at mm-wave frequencies. This technique was extensively analyzed and demonstrated in various mm-wave designs [111]-[114]. It is worth mentioning that, other than the above on-chip MMIC power combining techniques, on-antenna power combining schemes have also been demonstrated recently as an attractive co-design solution for improved circuit performance [115]-[118].

In this Chapter, a high power 60 GHz balanced power SiGe power amplifier is presented. The balanced amplifier topology has been frequently used in mm-wave PA

designs for its promise for gain flatness over wide bandwidth, good input and output matching, and stability. Simple common-emitter power cells were used in the design for simplicity. Three-conductor T-line-based power combining structures with simple T-line design equations were proposed in the design for easy tuning. This work was presented in the 2020 IEEE/ MTT-S International Microwave Symposium [6] © 2020 IEEE and is to be published in the IEEE Transactions on Microwave Theory and Techniques [7] © 2020 IEEE.

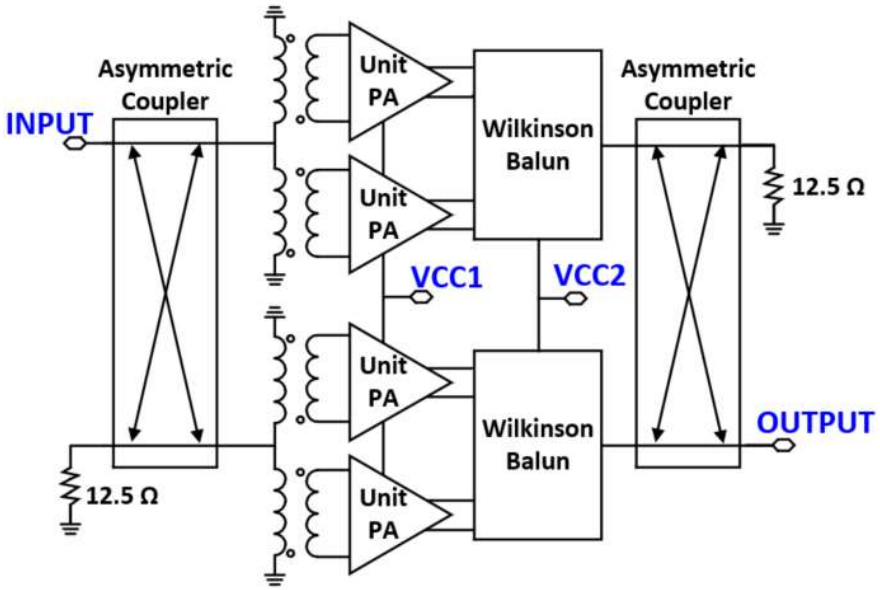


Figure 5.1 – Circuit block diagram of the 60 GHz SiGe balanced PA featuring three-conductor T-line based asymmetric coupled-line coupler and Wilkinson baluns for power combining [7] © 2020 IEEE.

5.2 Circuit Design

The block diagram of the 60 GHz SiGe PA is shown in Figure 5.1. The design features three-conductor T-line based asymmetric coupled-line directional coupler for quadrature-phase combining, and three-conductor Wilkinson baluns for further power combining.

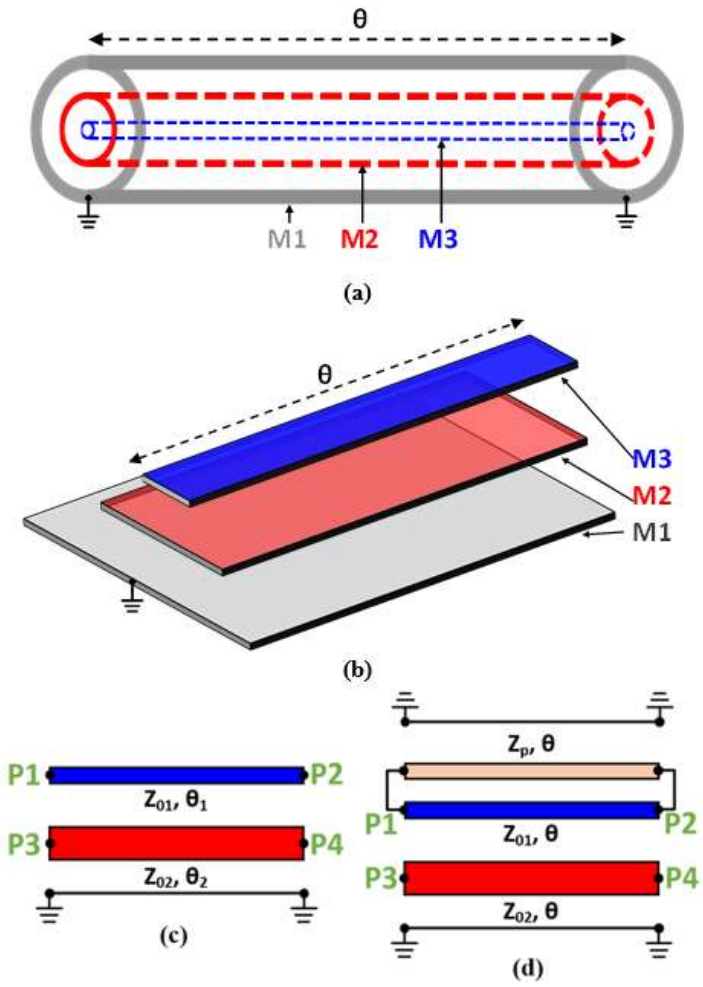


Figure 5.2 – (a) Three-conductor coaxial transmission line, where the center conductor M3 is isolated from the ground M1 by the intermediate conductor M2, and its (b) IC planar counterpart. (c) The simplified circuit diagram representation of the coaxial three-conductor T-line, and (d) the circuit diagram of planar three-conductor T-line with an additional parasitic T-line of characteristic impedance Z_p to model non-ideal shielding [7] © 2020 IEEE.

5.2.1 Three-Conductor T-Line Wilkinson Balun

The concept of a three-conductor T-line structure is not new. It's coaxial implementation, illustrated in Figure 5.2(a), has been used in various applications, such as Bazooka and Marchand baluns [119], [120]. Since M2 provides perfect isolation between M1 and M3, the three-conductor transmission line structure can be represented by two

uncoupled T-lines of the same physical length stacked on top of each other, as illustrated in Figure 5.2(c).

In recent years, the planar implementation of the three-conductor T-line, shown in Figure 5.2(b), has been introduced to IC design to realize a sub-quarter wavelength balun structure for mm-wave series power combining [111]. The planar three-conductor T-line can be represented by the schematic in Figure 5.2(d). Different from the coaxial implementation, M2 layer in the planar implementation cannot provide perfect shielding between M1 and M3, and this imperfect shielding can be modelled by an additional parasitic transmission line between the top conductor M3 and the global ground conductor M1 [112]. However, by adding a side wall on M2, the undesired coupling between M1 and M3 can be minimized.

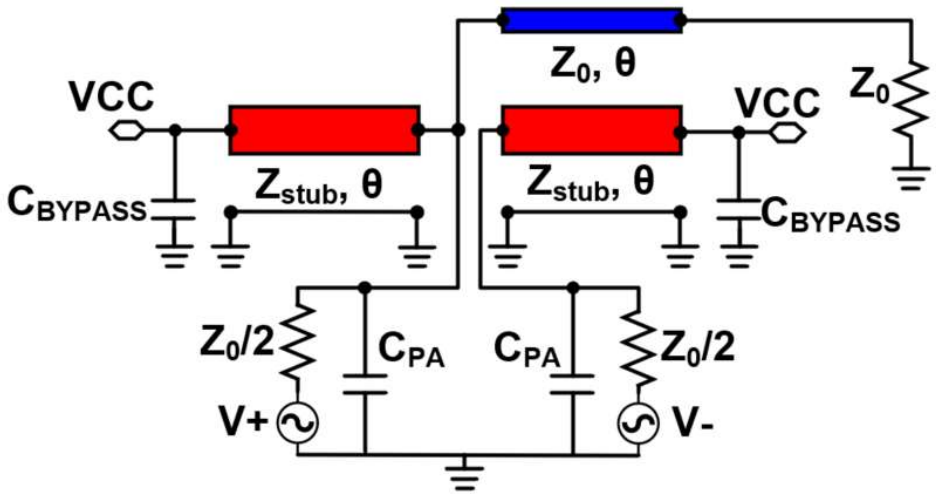


Figure 5.3 – Circuit diagram of 2:1 sub-quarter wavelength balun [7] © 2020 IEEE.

Figure 5.3 shows the circuit diagram of the 2:1 sub-quarter wavelength balun proposed in [111]-[114]. The T-lines of characteristic impedance of Z_{stub} are designed to

resonate with the output capacitance of the PA cells. This balun design achieves 2:1 impedance transformation ratio, and, with Z_0 = 50 Ω, each power cells are sized to drive a 25 Ω optimal impedance. The concept of this sub-quarter wavelength balun can be further extended to realize a 4:1 series power combiner by cascading two of the 2:1 baluns [112].

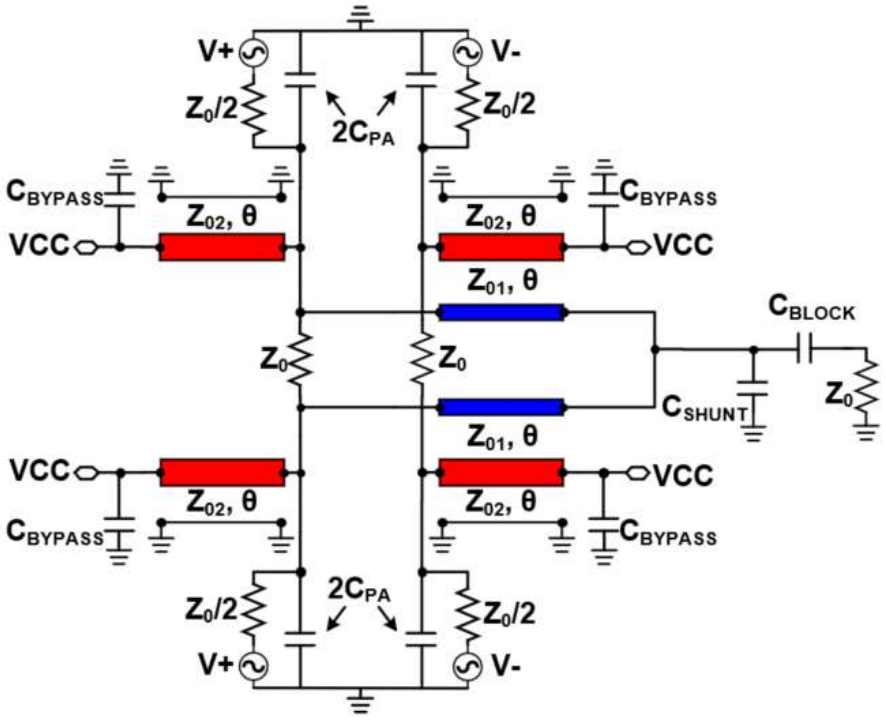


Figure 5.4 – Circuit diagram of the proposed Wilkinson balun [7] © 2020 IEEE.

In this works, instead of cascading the 2:1 sub-quarter wavelength balun in series, the concept of sub-quarter wavelength balun is combined with the capacitively-loaded Wilkinson combiner to achieve 4:1 series-parallel power combiner. The circuit diagram of the Wilkinson balun design is presented in Figure 5.4. Unlike in the sub-quarter wavelength balun design, where the short stubs of characteristic impedance of Z_{stub} is designed to resonate with the output capacitance of the PA cell at f_0, the stubs of characteristic impedance of Z_{02} in the Wilkinson balun are designed to partially resonate with C_{PA}. The

residual capacitance is absorbed into the miniaturized Wilkinson combiner as the capacitive loading. Therefore, combining the design equations of the capacitively-loaded Wilkinson combiner and three-conductor balun, the three-conductor T-line Wilkinson balun design follows:

$$Z_{01} = \sqrt{2}Z_0 \Big/ \sin\theta, \tag{5.1}$$

$$C_{SHUNT} = \sqrt{2}\cos\theta \Big/ Z_0\omega_0 \text{, and} \tag{5.2}$$

$$C_{SHUNT} = 2C_{PA}\,. \tag{5.3}$$

In the present work, Z_0 was set to 25 Ω to match with the subsequent asymmetric coupler, and f_0 was set to 60 GHz. Observing from the above three equations, the value of Z_{01}, and C_{SHUNT} depend only on the electrical length θ, while Z_{02} depends on both θ and C_{PA}. To determine the optimal design values, the electrical length θ was first swept from 20° to 70°, and the calculated Z_{01} and C_{SHUNT} are plotted in Figure 5.5 which serves as a general guideline of the lower bound of practical θ choice. With a short electrical length, for example θ = 30°, the Z_{01} value reaches a 70 Ω, which is not easy to achieve with the BEOL provided by the process used for the present design. Moreover, the bandwidth of capacitively-loaded Wilkinson combiner is known to reduce as the electrical length of the transmission lines shrinks, especially at high frequencies.

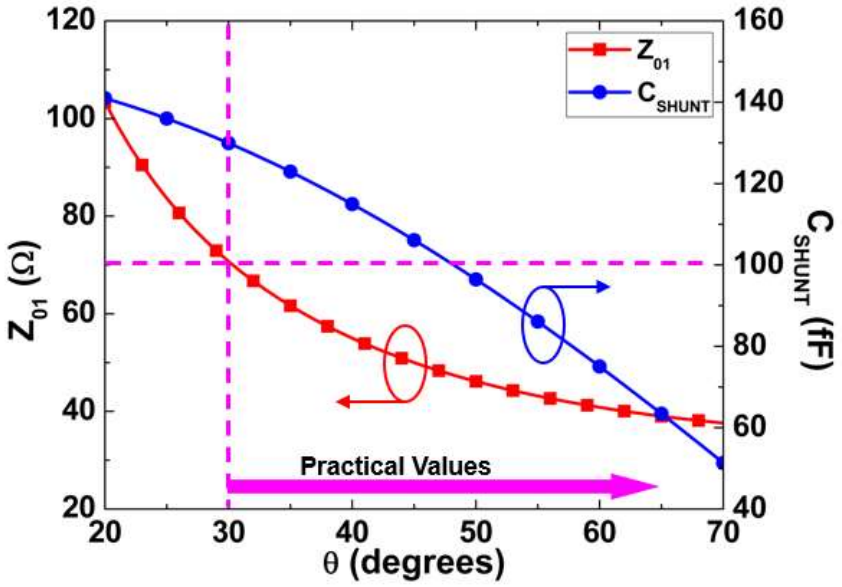


Figure 5.5 – Calculated Z_{01} and C_{SHUNT} vs. θ with Z_0 = 25 Ω and f_0 = 60 GHz. A 70 Ω Z_{01} is required for θ = 30° [7] © 2020 IEEE.

The characteristic impedance Z_{02} depends on both C_{PA} of the power cell and θ. A C_{PA} of 160 *fF* was obtained through load-pull simulation on the common-emitter (CE) differential pair. The calculated Z_{02} is plotted vs. θ in Figure 5.6, with C_{PA} of 120 *fF*, 160 *fF*, and 200 *fF*. As the electrical length increases, for a given C_{PA}, the requires Z_{02} decreases, which, from an implementation perspective, leads to increased M2 metal width. Excessively low Z_{02} should be avoided to prevent bulky layout. More importantly, as discussed in [112], to maximize the bandwidth and amplitude balance of three-conductor sub-quarter wavelength balun, the value of Z_{ratio} (5.4) should be maximized. Since Z_{ratio} decreases with increasing θ and C_{PA}, it is essential, therefore, that one avoid long transmission lines and minimize the output capacitance of the PA cell to improve bandwidth.

$$Z_{ratio} = {Z_{02}}/{Z_{01}} = {\cos\theta}/{2\left(\sqrt{2}\omega_0 Z_0 C_{PA} - \cos\theta\right)}. \quad (5.4)$$

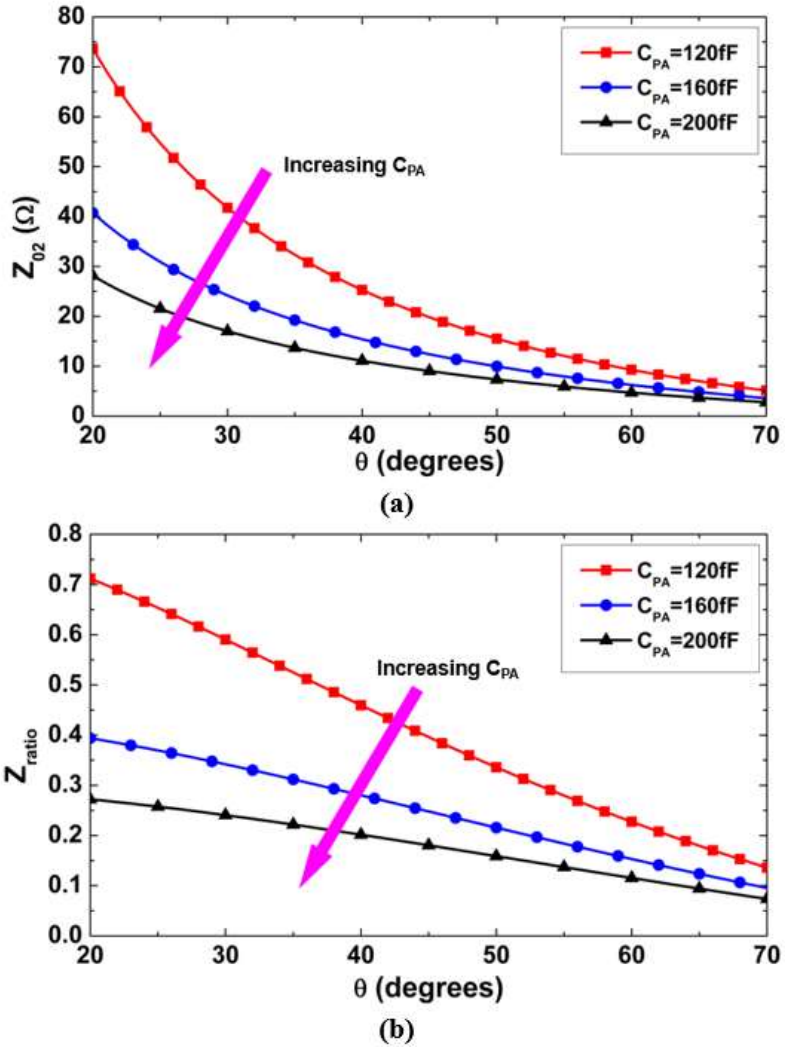


Figure 5.6 – Calculated (a) Z_{01} and (b) Z_{ratio} vs. θ with C_{PA} of 120 *fF*, 160 *fF* and 200 *fF*. Z_0 = 25 Ω and f_0 = 60 GHz [7] © 2020 IEEE.

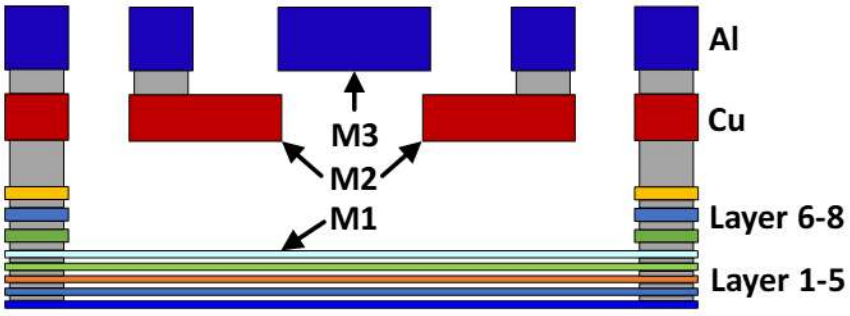


Figure 5.7 – Cross-section of the three-conductor transmission line implemented in the Wilkinson balun combiner [7] © 2020 IEEE.

In this design, a θ of 40° was chosen as a starting point, which resulted in Z_{01} = 55 Ω and Z_{02} = 10.2 Ω. The design was implemented in the 90 nm GlobalFoundries 9HP SiGe BiCMOS technology platform. The top two thick metal layers were used to form the top T-line. However, since the vertical distance between these two layers was not sufficiently large, having a solid ground plane for the top transmission line required a minimum top signal trace width to realize 55 Ω Z_{01}. To ensure the top trace was wide enough to handle the output power without electromigration concerns, the cross-section shown in Figure 5.7 was used, where the ground plane of the top transmission line was opened to allow widened M3 trace, at the cost of degraded isolation between M1 and M3. The value of the bypass capacitance at the end of the T-line stubs were then carefully tuned to compensate for the amplitude imbalance caused by the imperfect isolation.

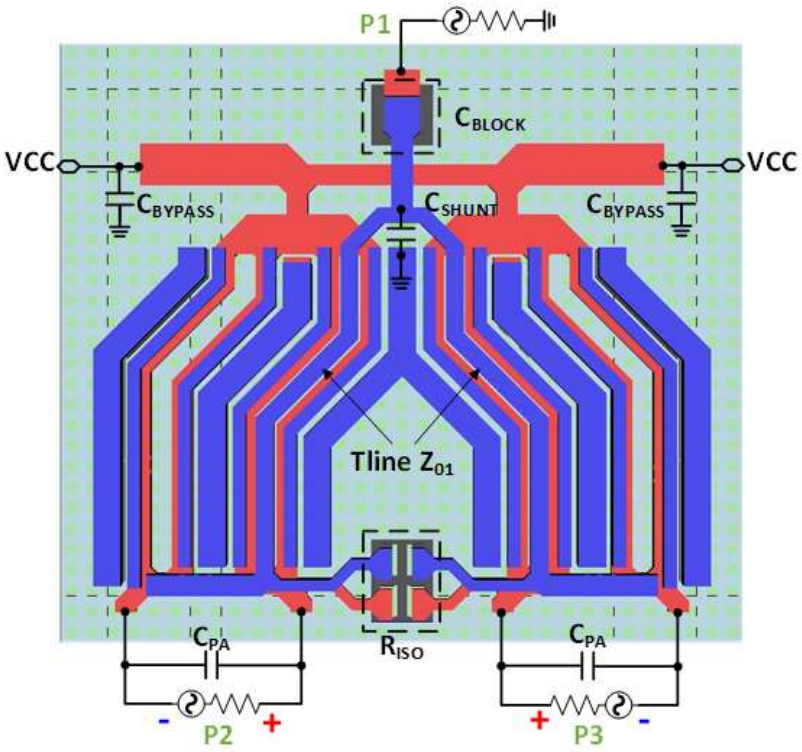


Figure 5.8 – Top view of the proposed Wilkinson balun [7] © 2020 IEEE.

The top view of the proposed Wilkinson balun is shown in Figure 5.8. The isolations resistors were implemented using the BEOL TaN resistors. The bottom five metal layers were connected and used as the global ground. To achieve a low characteristic impedance for the bottom transmission line, side walls were added to the global ground.

5.2.2 Three-Conductor T-Line Asymmetric Coupler

The asymmetric coupled-line coupler has been extensively studied by many researchers [121], [122]. Since it is known that each line of an asymmetric coupled-line section can be terminated with different impedances, the asymmetric coupled-line couplers naturally found their way into power combining and impedance transformation applications [123]-[126].

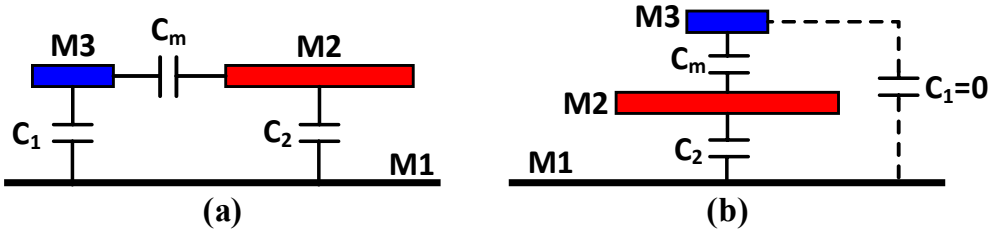


Figure 5.9 – (a) Asymmetric coupled-line and its equivalent capacitance network, where $C_{1,2}$ are the self-capacitance of each line and C_m is the mutual-capacitance between the two, and (b) three-conductor transmission line where $C_1 = 0$ [7] © 2020 IEEE.

As noted by D. M. Pozar [127], assuming TEM wave propagation, the electrical characteristics of coupled lines can be completely determined from the effective capacitance between the lines and the velocity of propagation. Figure 5.9(a) shows the schematic diagram of an asymmetric coupled-line system, where C_1 and C_2 are the self-capacitances of the M3-M1 and M2-M1 T-line pairs, and C_m represents the mutual-

capacitance between M2 and M3. With this capacitance matrix analysis, K. Wincza and S. Gruszczynski in [123] showed that with equal quadrature power splitting at the thru and coupled ports, the maximum achievable impedance transformation ratio with a single asymmetric coupled-line coupler is 2, when the self-capacitance $C_1 = 0$. In planar IC processes, this condition corresponds to the three-conductor transmission line structure, where the top trace is shielded by the intermediate layer, as shown in Figure 5.9(b).

In planar IC processes where, homogeneous media can be assumed, $\theta_1 = \theta_2 = \theta$ in Figure 5.2(c). Since M1 and M3 can be assumed to decouple from each other, the top and bottom transmission lines can be designed and simulated separately first then optimized when combined in the later steps. It is therefore convenient to reach a set of design equations expressed in terms of the characteristic impedances of the top and bottom T-line (Z_{01} and Z_{02}) and their electrical length (θ), similar to that obtained for the Wilkinson balun combiner. Assuming 3-dB quadrature coupling, perfect isolation, equal coupled and thru port impedance, and perfect matching, the following relations are derived in [7]:

$$Z_2 = Z_3 = Z_{02} \sin\theta \,, \tag{5.5}$$

$$Z_2 Z_3 = Z_{01} Z_{02} \,, \tag{5.6}$$

$$Z_1 = \frac{Z_{02} + Z_2}{\cos^2\theta + 1} - j\frac{(Z_{01} + Z_{02})\sin(2\theta)}{2(\cos^2\theta + 1)} \,, and \tag{5.7}$$

$$Z_1 Z_4 = Z_{01} Z_{02} \,. \tag{5.8}$$

Therefore, in an ideal situation, $\theta = 90°$ at the center frequency, $Z_1 = 50\ \Omega$, $Z_{01} = Z_{02} = Z_2 = Z_3 = 25\ \Omega$, and $Z_4 = 12.5\ \Omega$, and $Z_4 = 12.5\ \Omega$. The resultant S_{21} and S_{31} with the above design values are plotted in Figure 5.10(a) ($\Delta\theta = 0$).

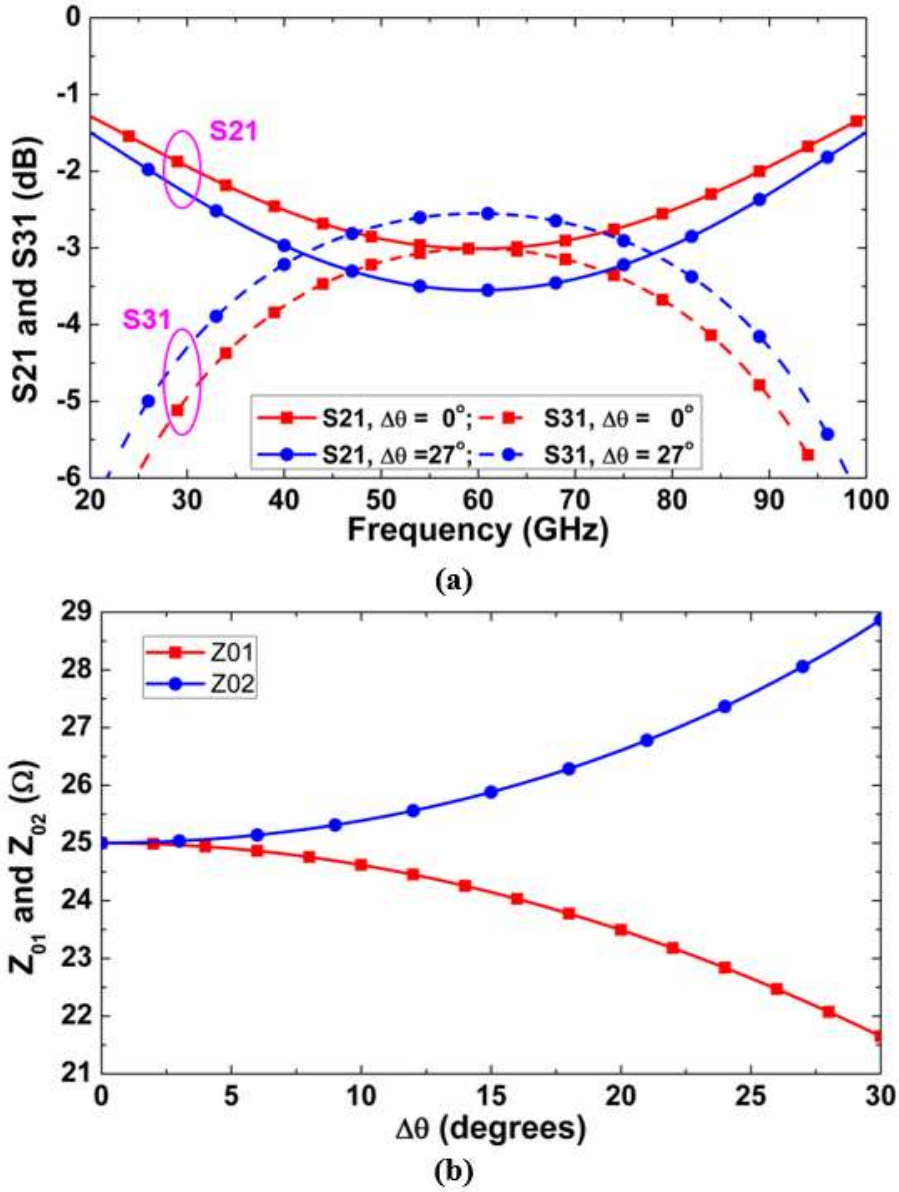


Figure 5.10 – Simulated (a) S_{21}, S_{31}, and (b) S_{11} of the asymmetric coupler with parasitic transmission line. $Z_1 = 50\ \Omega$, $Z_{01} = Z_{02} = Z_2 = Z_3 = 25\ \Omega$, $Z_4 = 12.5\ \Omega$, and $\theta = 90°$ at the 60 GHz. Performance exhibits under-coupling and degradation in matching as coupling between M1 and M3 increases[7] © 2020 IEEE.

A common practice to increase the 1-dB amplitude imbalance bandwidth in a single section 3-dB hybrid coupler design is to intentionally introduce over-coupling at the center frequency. This can be done by slightly modifying (5.5) to

$$Z_2 = Z_3 = Z_{02} \sin(90° \pm \Delta\theta)\,, \tag{5.9}$$

which is the equivalent of saying, instead of enforcing equal S_{21} and S_{31} at the center frequency, they will be designed to be equal at frequencies where the electrical length of the transmission line is 90° ± $\Delta\theta$. Doing so will cause a slight mismatch at the 4 ports, which results in an insignificant insertion loss degradation at 90° ± $\Delta\theta$. With Z_1-Z_4 retaining their original values, the characteristic impedance of the top and bottom transmission lines are then recalculated and plotted vs $\Delta\theta$ in Figure 5.10(b). As $\Delta\theta$ increases, Z_{01} decreases. This can be easily accommodated by increasing the width of the top signal trace. The increase in Z_{02} can be achieved by slightly opening the global ground plane underneath M2 and implementing the bottom transmission line in the elevated CPW fashion.

The 3-D view of the output asymmetric coupler, including the output RF GSG pad, is shown in Figure 5.11. For reliability concerns, M2 was be opened in the fashion similar to that shown in Figure 5.7, which inevitably results in degraded isolation between M3 and the global ground M1. C_1 in Figure 5.9(b) can no longer assume zero. As observed in [123], as the value of C_1 increases, the achievable impedance transformation ratio decreases from two, and to maintain matching at all ports, C_2 and C_m also needs to decrease accordingly. However, the amplitude imbalance between S_{21} and S_{31} can be tuned through intentionally introducing over-coupling during the design process by changing $\Delta\theta$ in (5.9).

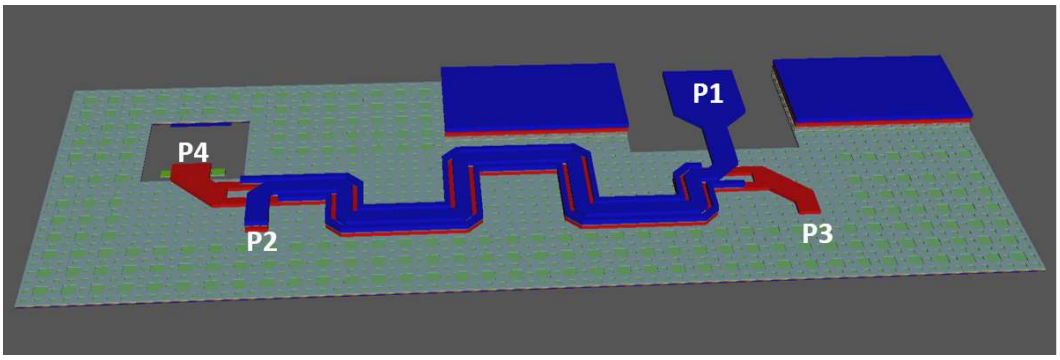


Figure 5.11 – 3-D view of the output asymmetric coupler with output RF GSG pad. P1 is the output port, P2 and P3 are the thru and coupled port, respectively. P4 is terminated with 12.5 Ω N+ sub-collector resistor [7] © 2020 IEEE.

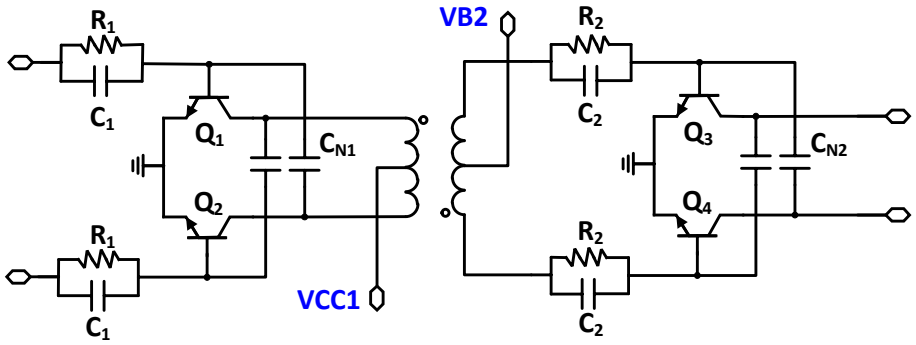


Figure 5.12 – Schematic of the unit PA core. Simple two-stage differential CE with inductor-based transformer inter-stage matching topology was adopted [7] © 2020 IEEE.

5.2.3 Power Cell Design

As a proof of concept for the proposed power combining scheme, a simple two-stage CE with capacitive neutralization topology was adopted for the power cells, shown in Figure 5.12. Inductor-based transformers were used for inter-stage matching with center-taps of the primary and secondary windings used for bias. All the transistors used a collector-base-emitter-base-collector (CBEBC) SiGe HBT layout option. The output transistors Q_3 and Q_4 each consist of six 10×0.1 μm^2 HBTs in parallel and were each sized

to drive a 12.5 Ω load. Load-pull simulations were performed on the Q_3-Q_4 differential pair with Keysight Advanced Design System (ADS) at 60 GHz. A load of 7.5 + j11.5 Ω between the maximum P_{OUT} and maximum PAE points was chosen as the optimal load impedance for this design. This load is roughly equivalent to a parallel connection of 25 Ω R_{LOAD} and C_{PA} of 160 fF.

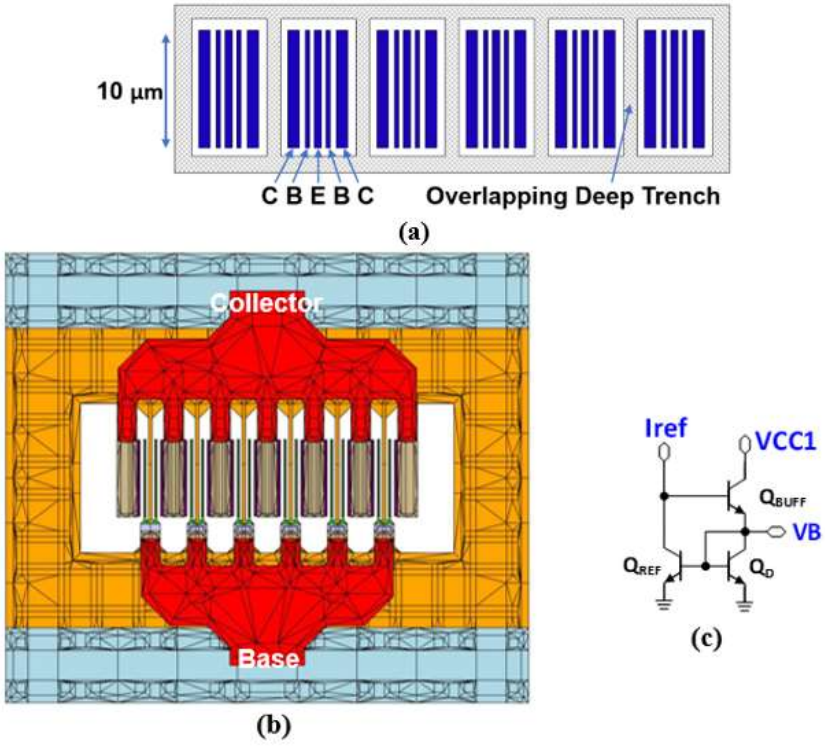


Figure 5.13 – (a) The top view of power transistor (Q_3 / Q_4). Six CBEBC 10 µm HBTs were placed in parallel with overlapping DT. (b) The top view of power transistor test structure. (c) Buffered current mirror bias circuit with additional avalanche current diode Q_D [7] © 2020 IEEE.

The GlobalFoundries 9HP process features deep trench around the HBT devices for improved device-to-device isolation. To achieve a compact power cell footprint, the deep trenches (DT) of the adjacent HBTs were overlapped, the same practice also adopted by [112]. Figure 5.13(a) shows the SiGe HBT configuration of the output power transistors

(Q_3/ Q_4). Even though the DT layers were overlapped in layout, the power transistor was still modelled with six individual HBTs. To verify the performance of the power transistors with overlapping DT, the transistor test structure shown in Figure 5.13(b) was taped-out together with open and short de-embedding structures. Staggered traces and vias were employed to minimize the parasitic coupling between the terminal routings. The power transistor was EM simulated with the Cadence EMX simulator tool.

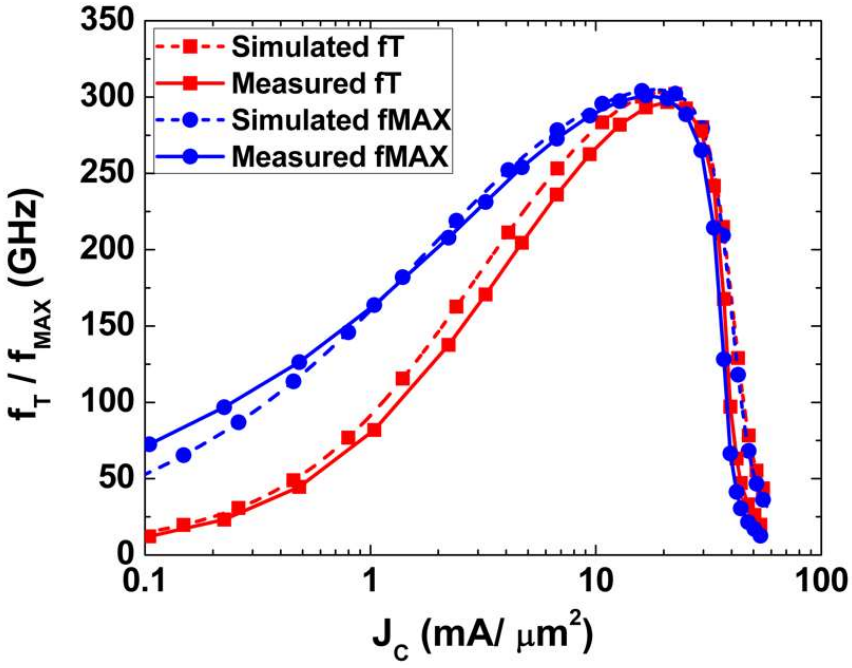


Figure 5.14 – Measured and simulated f_T and f_{MAX} of the power transistor test structure with 0.3 V V_{CB}. Measured f_T and f_{MAX} show a close match with simulation [7] © 2020 IEEE.

Both the base and collector were biased using voltage sources through the internal bias-T of the Keysight E8361C PNA used for the measurement. The collector bias voltage was swept together with the base bias voltage to keep a constant 0.3 V V_{CB} where the peak f_T and f_{MAX} are nominally observed in the 9HP process. The pads were de-embedded with the open and short test structures. The f_T and f_{MAX} were extrapolated using the de-embedded

S-parameters from 12 GHz to 16 GHz. The measured and simulated f_T and f_{MAX} are plotted vs. collector current density, J_C, in Figure 5.14. The measured peak f_T and f_{MAX} and peak f_T and f_{MAX} collector current density match closely with simulations. This indicates that overlapping the deep trench of the individual HBTs does not cause significant errors in the intrinsic and extrinsic parasitics modeling.

However, this does not rule out the all the design concerns for overlapping DT of parallel transistors, especially from a thermal perspective. To push for higher peak f_T / f_{MAX}, the peak f_T / f_{MAX} current density also increases significantly. The high current density, together with small device geometry, lead to very high local power density at each NPN junction. To exacerbate the problem, the deep trench isolation ring raises the thermal impedance of each device compared to Si platforms where the devices are not trench-isolated [128]. At the time of design, no calibrated thermal models were available to capture the mutual thermal coupling between the NPNs, and only device self-heating was enabled, which leads to an underestimation of device junction temperatures. By bring the individual NPNs closer and overlapping the deep trench, the underestimation of junction temperature was made even worse. To better visualize this modeling error, the measured DC-IV characteristics of the power transistor test structure, with forced V_{BE} measurement setup, is plotted with that of simulated results, where no mutual heating between the devices was captured, in Figure 5.15. The DC-IV characteristics of the power transistor test structure were measured with V_{BE} swept from 0.70 V to 0.95 V in steps of 0.01 V. V_{CC} was swept in 0.1 V steps from 0 V to 2.0 V or the nearest 0.1 V when negative base current was measured for each V_{BE}, to prevent unnecessary damage to the device. For presentation purposes, only the DC-IV traces with V_{BE} = 0.72 V, 0.75 V, 0.82 V, and 0.84 V are plotted.

The wafer parameters were first adjusted to match the simulated and measured collector current at low voltage and current level, as shown by the inset in Figure 5.15. The measured collector current with 0.84 V V_{BE} shows a much higher positive slope as the collector voltage increases compared to simulations, and at 1.8 V V_{CC}, the measured I_{CC} is 50% higher than simulation. This implies a much higher device junction temperature compared to simulations.

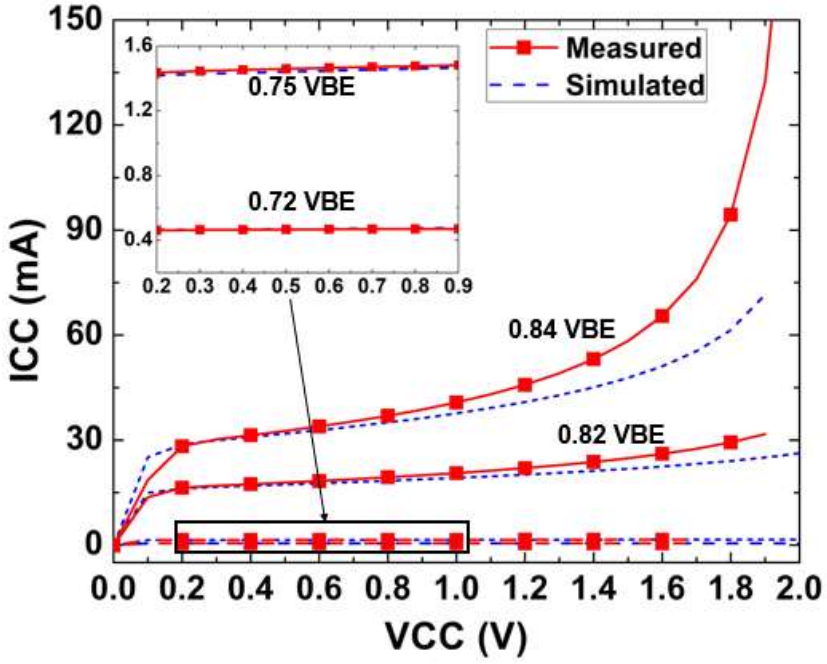


Figure 5.15 – Measured and simulated DC-IV characteristics of the power transistor test structure with V_{BE} = 0.72 V, 0.75 V, 0.82 V, and 0.84 V [7] © 2020 IEEE.

The analysis of thermal effects on PA performance is complicated, since almost all device parameters in SiGe HBTs have a significant temperature dependence. However, it is generally acknowledged that an elevated device junction temperature can result in a drop in small-signal gain, and the increasing junction temperature over output power, if not compensated, can result in premature power saturation [129]. To ensure stable bias across

output power, a buffered current mirror bias was used in the present design. Transistor Q_{BUFF} acted as the beta-helper device and ensured the current mirror sufficient current sourcing capability, especially at high output power level when the base current consumption of the RF power cells became significant. The reference device was placed in close proximity with the output power transistors to increase the thermal mutual coupling between the reference and power cells, and therefore, to better track the power cell junction temperature across the output power level. additional avalanche current diode (Q_D in Figure 5.13(c)) was included to give the bias circuit better avalanche current sinking capability and thus safely allow a supply voltage beyond nominal BV_{CEO} [48]. However, for a more accurate prediction of circuit behavior, careful thermal simulation with calibrated thermal models should be included in the design cycle [129], [130].

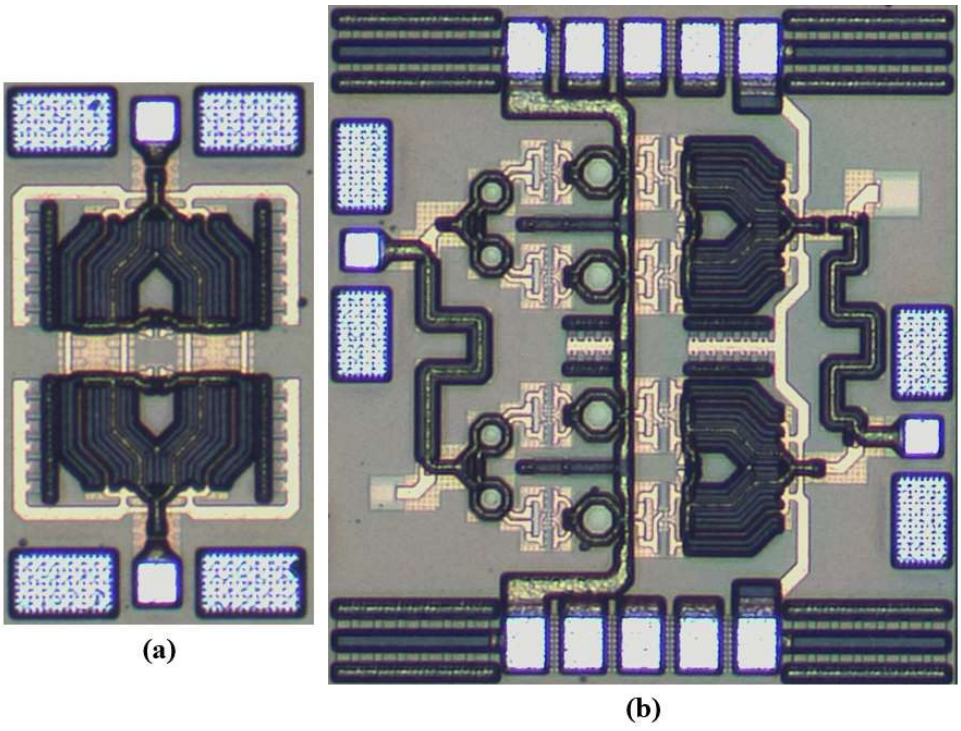


Figure 5.16 – Chip micrograph of the (a) back-to-back Wilkinson balun test structure and (b) the proposed 60 GHz balanced PA. [7] © 2020 IEEE.

5.3 Experiment Results

To test the performance of the 4-to-1 Wilkinson balun combiner, a test structure with two flipped and back-to-back Wilkinson baluns, shown in Figure 5.16(a), was included in the test chip. Metal-oxide-metal (MOM) capacitors were included to load the input ports of the Wilkinson baluns. Open and short test structures were also included in the test chip to de-embed the pad loss from the measured S-parameters of the Wilkinson balun test structure. The Wilkinson balun was designed with a characteristic impedance of 25 Ω. The small-signal performance of the test structure was measured with a 50 Ω system and the measured results were re-normalized to a 25 Ω Z_0. The simulated and measured S_{11} and S_{21} are compared in Figure 5.17(a). The measured minimum insertion loss of the back-to-back Wilkinson balun combiner test structure is 3.1 dB, whereas the simulated minimum loss is 2.5 dB. Both measured and simulated S_{21} include the insertion loss from the load capacitors. Through a back-fitting exercise, it appears that the difference between the simulated and measured minimum insertion loss results likely come from over estimation of the Q factor of the MOM capacitors in simulation.

One distinguishing advantage of Wilkinson combiners is the isolation between the input ports. The isolation resistors in Wilkinson combiners terminate odd-mode signal between the two branches being combined, and therefore help to prevent potential stability concerns from layout asymmetry and power cell mismatch. The port-to-port isolation characteristics of the Wilkinson balun design were simulated with port assignment shown in Figure 5.8. Internal ports were used in the EM structure to allow the usage of PDK models for the isolation resistors. The simulated S_{32} of the Wilkinson balun design with

and without the isolation resistors is plotted in Figure 5.17(b). The use of isolation resistors improves the isolation between the two differential ports by 11.6 dB at 60 GHz.

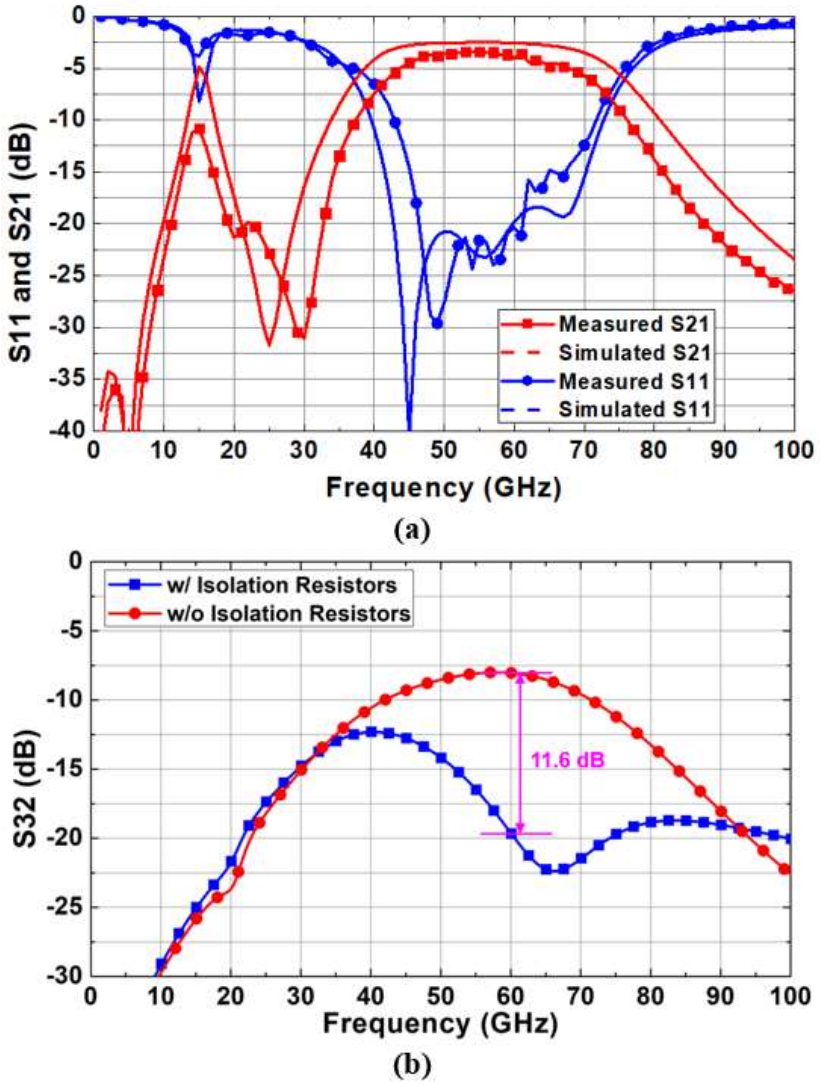


Figure 5.17 – Measured and simulated S_{11} and S_{22} of the back-to-back Wilkinson balun test structure. Minimum measured insertion loss is 3.1 dB including loss from loading capacitors. (b) Simulated port isolation of the Wilkinson balun with and without the isolation resistors [7] © 2020 IEEE.

The simulated performance of the output asymmetric coupler is shown in Figure 5.18. The insertion loss of the output asymmetric coupler is 0.8 dB at 60 GHz. The amplitude imbalance between the coupled and thru path is 0.2 dB at 60 GHz, and the phase

difference between the two paths is 90.1° at 60 GHz. Together with the measured 1.55 dB (half the measured insertion loss of the back-to-back test structure) insertion loss of the Wilkinson balun design, the overall insertion loss of the output matching network is 2.35 dB, equivalent to a 58.2% power combining efficiency.

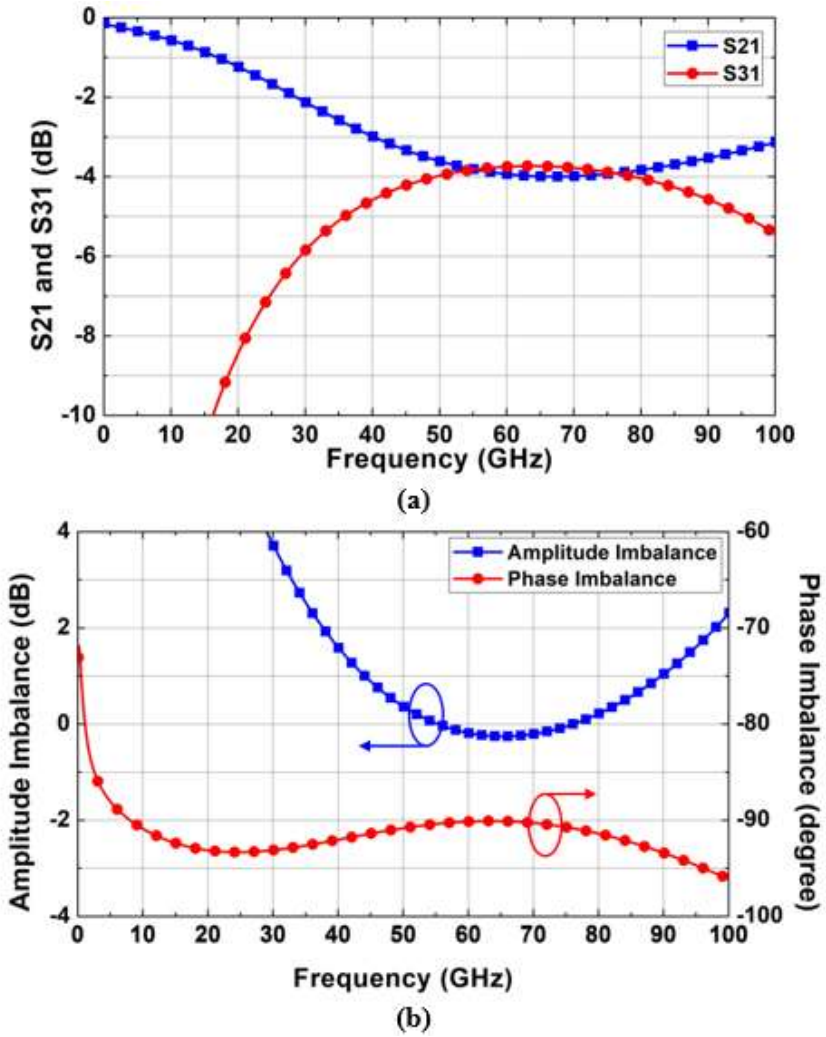


Figure 5.18 – (a) Simulated S_{21} and S_{31} of the output asymmetric coupler, showing 0.8 dB insertion loss at 60 GHz, and (b) simulated amplitude and phase imbalance between the coupled and thru ports [7] © 2020 IEEE.

The chip micrograph of the PA design is shown in Figure 5.16(b). The active area of the design is 0.81 × 0.73 mm^2 and the total chip area including bondpads is 1.15 × 1.06

mm^2. With the bases of the transistors terminated with low impedance, a 2.0 V and 1.8 V V_{CC}'s were used for stage 1 and stage 2, respectively. The small-signal response of the design was measured on wafer using an Anritsu ME7808C broadband network analyzer. The simulated and measured S-parameters are shown in Figure 5.19 The design showed 17.3 dB small-signal gain, with a 3-dB bandwidth of 41.8 GHz, covering from 28.1 GHz to 69.9 GHz. The gain variation is within 1 dB between 32.6 GHz and 66.6 GHz. Both the input and output return loss are greater than 11 dB across the 3-dB bandwidth.

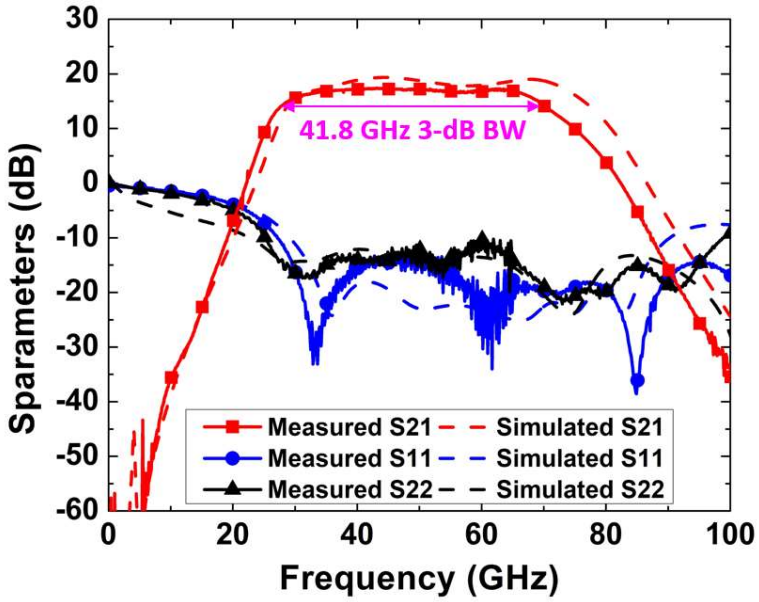


Figure 5.19 – Measured and simulated S-parameters of the balanced SiGe PA. The design 17.3 dB with a 41.8 GHz 3-dB bandwidth. Both input and output return loss are better than 11 dB cross the 3-dB bandwidth [7] © 2020 IEEE.

Power sweeps were performed from 40 GHz to 70 GHz, in 1 GHz steps. The 50 GHz to 70 GHz data was acquired with a Virginia Diode V-band source module, 150 µm WR-15 waveguide probes, and a Millitech V-band VCA. The 40 GHz to 50 GHz data was measured with a Keysight E8257D signal generator and coaxial setup. Shown in Figure 5.20, a 24.4 dBm P_{SAT} was measured with an output *P1dB* of 23.9 dBm. The peak *PAE* at

60 GHz is 14.2%. Measured P_{SAT} and *PAE* from 40 GHz to 70 GHz are plotted in Figure 5.21. The proposed design shows 22.0 GHz 1-dB P_{SAT} bandwidth from 45.0 GHz to 67.0 GHz. The peak *PAE* is greater than 11.5% across the 1-dB P_{SAT} bandwidth.

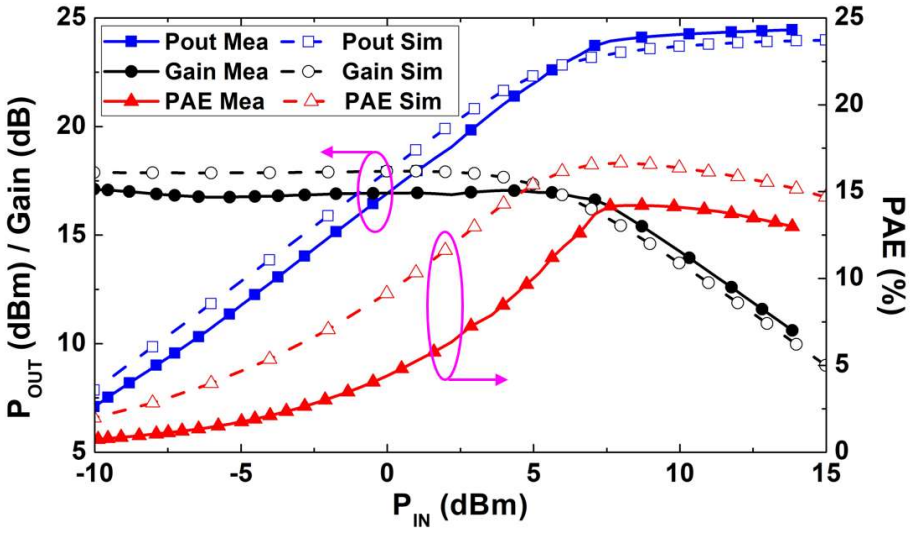


Figure 5.20 – Measured and simulated P_{OUT}, *Gain*, and *PAE* plotted vs. P_{IN} at 60 GHz [7] © 2020 IEEE.

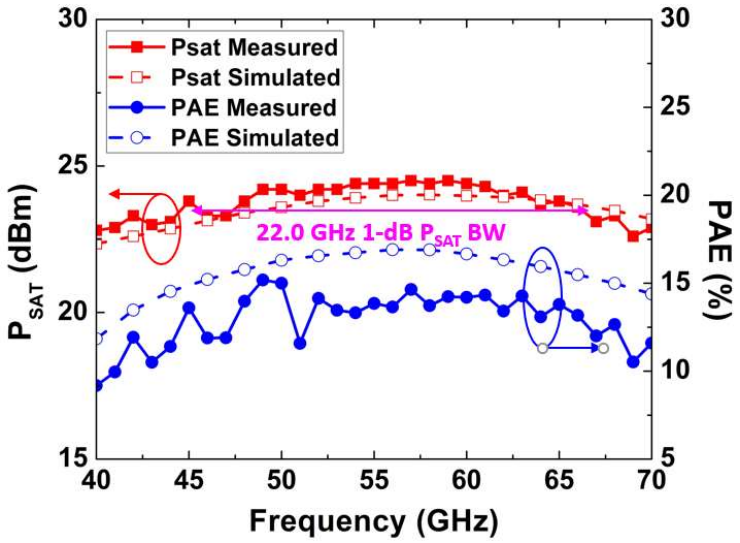


Figure 5.21 – Measured and simulated P_{SAT} and peak *PAE* from 40 GHz to 70 GHz. The 1-dB P_{SAT} bandwidth is 22.0 GHz with peak *PAE* greater than 11.5% across the bandwitdth [7] © 2020 IEEE.

The performance of the proposed balanced SiGe PA is compared with other state-of-the-art designs in Table 5.1. The proposed design demonstrates high output power and good bandwidth.

Table 5.1 – Performance Comparison with SOA Millimeter-wave PAs

Ref.	Tech.	Freq (GHz)	BW (GHz)	P_{SAT} (dBm)	PAE_{MAX} (%)	Gain (dB)	P_{1dB} (dBm)	Area (mm^2)
[97]	65 nm CMOS	64	25.1[a]	23.2	10.0	16.3	19.6	2.04
[98]	120 nm SiGe	70	15.0[a]	24.0	12.0	22.0	21.0	3.34
[99]	120 nm SiGe	60	14.0[a]	21.3	14.4	27.5	19.2	2.30
[100]	90 nm CMOS	58	-	22.2	17.8	19.6	19.7	0.26
[101]	90 nm CMOS	60	24.5[a]	20.6	20.3	20.1	17.6	0.43
[102]	45 nm RFSOI	60	12.0[a]/ 9.0[bc]	29.1	18.4	23.9	24.7	6.60
[103]	65 nm CMOS	65	15.0[a]	20.0	15.0	30.0	16.0	0.11
[104]	65 nm CMOS	63	9.4[a]	23.0	9.4	17.2	20.9	0.72
[105]	40 nm CMOS	60	-	22.6	7.0	29.0	17.0	2.16
[106]	90 nm CMOS	60	-	21.0	13.4	16.8	17.2	0.67
[109]	55 nm SiGe	66	-	23.4	12.5	23.8	20.0	0.17
This Work	**90 nm SiGe**	**60**	**42.0[a]/ 22.0[b]**	**24.4**	**14.2**	**17.3**	**23.9**	**1.22**

[a] 3-dB BW, [b] 1-dB PSAT BW, [c] with 10% VDD increase, [d] stage 1 and stage 2 VCC, respectively

5.4 Summary

In this Chapter, a 60 GHz, high power, wideband, SiGe balanced amplifier was presented, utilizing GlobalFoundries 90 nm 9HP SiGe BiCMOS technology. Three-conductor transmission-line-based asymmetric couplers were employed to achieve simultaneous quadrature combining and impedance transformation. A transmission-line-equation-based analysis of this asymmetric coupler was presented. A compact Wilkinson balun combiner based on three-conductor sub-quarter wavelength balun and capacitively-loaded Wilkinson combiner was proposed to achieve four-way series and parallel power combining. A two-stage common-emitter differential topology was used to implement the unit PAs. To partially alleviate thermal concerns due to overlapping deep trench among NPN SiGe HBT cells and the lack of calibrated thermal models during the design process, current mirror bias circuit was used with reference device placed close to the power transistors to prevent premature power saturation.

CHAPTER 6. CONCLUSION

6.1 Summary of Contributions

The research presented in this dissertation examined the unique advantages and challenges for design with SiGe BiCMOS technology, particularly in comparison with advanced RF CMOS technology. Although silicon-based transistors in general fall behind III-V transistor technologies, they excel in term of integration capability and hence promise great potential for cost reduction. Since advanced CMOS platforms are usually on the leading-edge of technology scaling compared to advanced SiGe CMOS technologies, they are the better options for low-power applications and applications with high logic content. However, the excellent transistor frequency response, thermal noise, *1/f* noise, and higher breakdown voltage of SiGe HBTs make SiGe BiCMOS technologies great choices for front-end circuit designs when they performance of RF CMOS devices start to become limiting. This research leveraged the advantages of SiGe HBT integrated circuit technologies to better design RF and mm-wave circuit component and addressed a few unique challenges associated with circuit design with SiGe BiCMOS technology. The specific contributions of this work include:

1. The demonstration of an X-band 6-bit switched-type phase shifter with SiGe BDA embedded active DPDT switches for loss compensation. The design demonstrated a > 11.5-dB gain in both directions of operation over the 8-12 GHz frequency range, with an RMS amplitude error < 0.9 dB, an RMS phase error < 2.2º, a return loss > 10 dB.

2. The design of a 28 GHz differential neutralized BDA with cross-coupled common-emitter SiGe HBT pairs. The design showed forward and backward gain of 10 dB and 8.6 dB, with *NF* of 3.9 dB and 4.2 dB, respectively, at 28 GHz. The IP_{1dB} at 28 GHz for forward and backward operations are -2.4 dBm and -0.4 dBm, respectively.
3. A broadband logarithmic power detector designed in a 130 nm SiGe BiCMOS technology. The log detector showed 23 dB dynamic range with -28 dBm minimum input power from 2 GHz to 40 GHz with ±1.5 dB log error. The design consumed 3.2 mW of static DC power from a 2-V supply and consumed less than 7.8 mW of DC power over the input power range.
4. The design of a compact, 60 GHz, SPDT switch implemented using SiGe PIN diodes. The design employed a novel shunt-series topology with a resistive biasing scheme for improved power handling capability. The proposed design achieved a minimum insertion loss of 2.0 dB, more than 26 dB of isolation, and IP_{1dB} (at 60 GHz) of 22 dBm.
5. A study of reverse-saturated SiGe HBT switch design with grounded-emitter vs. floating-emitter configurations, carried out on a W-band quarter-wave shunt SPDT switch test structure. The study showed that the floating-emitter configuration had the same small-signal performance, but better power handling capability compared to the grounded-emitter configuration. Despite substantial amount of device damage under high-power RF stress, the switch experienced no performance degradation.

6. The demonstration of a 60 GHz high-power and wide-band balanced SiGe power amplifier with novel three-conductor T-line based Wilkinson balun and asymmetric coupler. Intuitive T-line based design equations and analyses were presented. The design. The design achieved 17.3 dB small-signal gain with 41.8 GHz 3-dB bandwidth from 28.1 GHz to 69.9 GHz. A 24.4 dBm P_{SAT} was demonstrated with a 22.0 GHz 1-dB P_{SAT} bandwidth covering from 45.0 GHz to 67.0 GHz. The circuit showed a peak *PAE* of 14.2% at 60 GHz and the peak *PAE* was above 11.5% across the 1-dB P_{SAT} bandwidth.

6.2 Future Work

The research presented in this work addressed several issues with SiGe BiCMOS RF and mm-wave circuit component design. The following list presents several ideas for extending this research:

1. The broadband high-performance power detector presented in this work can be integrated into a transceiver design with BIST feature. A compact, wideband, and low insertion loss directional coupler design that is insensitive to VSWR variation is highly desirable.
2. Detailed analysis of the damage mechanisms in the shunt reverse-saturated SiGe HBT is much needed. Further work with the help of TCAD simulation and carefully thought-out test structures can lead to a better understanding of the reason behind the decoupled relation between the switch performance and device damage level.

3. While the experiment with the W-band SPDT test structure revealed the benefits of floating-emitter configuration compared to grounded-emitter configuration, further validation of the P_{1dB} improvement across frequency can be informative.
4. The reliability study of shunt reverse-saturated SiGe HBT switching device can be extended to series connected SiGe HBT and examine the effect of different biasing scheme on the performance of series-connected SiGe HBTs. This, together with the reliability study on the shunt reverse-saturated SiGe HBT, could help to shed light on the device damage mechanism on SiGe HBTs biased in saturation.
5. Although this research has pointed out potential electrothermal concerns with high-power SiGe power amplifier design, no further analyses was provided to better model and address the electrothermal effects. Better understanding could be achieved through the used of pulsed device characterization methods and high-speed thermal imager.
6. For a power amplifier design with large power cell array, the thermal time constant can be orders of magnitude lower compared with the signal modulation. The performance of SiGe HBTs is sensitive to the change in device junction temperature during pulsed operation. Power cell layout optimization and novel dynamic temperature compensation techniques are highly desirable to minimize the gain variation due to thermal effect during the dynamic operation of the power amplifier.

REFERENCES

[1] Y. Gong *et al.*, "A bi-directional, X-band 6-Bit phase shifter for phased array antennas using an active DPDT switch," in *Proc. 2017 IEEE Radio Frequency. Integrated. Circuits Symposium*, Honolulu, HI, 2017, pp. 288-291.

[2] Y. Gong *et al.*, "A 28-GHz switchless, SiGe bidirectional amplifier using neutralized common-emitter differential pair," in *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 8, pp. 717-719, Aug. 2018.

[3] Y. Gong *et al*., "A broadband logarithmic power detector using 130 nm SiGe BiCMOS technology," in *Proc. 2019 IEEE BiCMOS Compound Semiconductor. Integrated Circuits and Technology Symposium*, Nashville, TN, USA, 2019, pp. 1-4.

[4] Y. Gong *et al*., "A compact, high-power, 60 GHz SPDT switch using shunt-series SiGe PIN diodes," in *Proc. 2019 IEEE Radio Frequency Integrated Circuits Symposium*, Boston, MA, USA, 2019, pp. 15-18.

[5] Y. Gong *et al*., "Performance improvement of reverse-saturated SiGe HBT millimeter-wave switches with floating emitter configuration," *2021 IEEE/ MTT-S. International Microwave Symposium*, submitted.

[6] Y. Gong and J. D. Cressler "A balanced power amplifier with asymmetric coupled-line couplers and Wilkinson baluns in a 90 nm SiGe BiCMOS technology," in *Proc. 2020 IEEE/ MTT-S. International Microwave Symposium*, Los Angeles, CA, USA, 2020, pp. 1097-1100.

[7] Y. Gong and J. D. Cressler, "A 60-GHz SiGe power amplifier with three-conductor transmission-line-based Wilkinson baluns and asymmetric directional couplers," in *IEEE Transactions on Microwave Theory and Techniques*, to be published. doi: 10.1109/TMTT.2020.3031586.

[8] A. Joseph *et al.*, "Technology positioning for mm wave applications: 130/90nm SiGe BiCMOS vs. 28nm RFCMOS," in *Proc. 2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium,* San Diego, CA, 2018, pp. 18-21.

[9] J. D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*. Boston, MA: Artech House, Inc., 2003.

[10] J. Zhang *et al.*, "Comparison of PMOS and NMOS in a 14-nm RF FinFET technology: RF characteristics and compact modeling," in *Proc. 2020 IEEE 20th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, San Antonio, TX, USA, 2020, pp. 47-49.

[11] GLOBALFOUNDRIES, Santa Clara, CA, USA. *45RFSOI: Advanced 45nm RFSOI Technology*. Accessed: Nov. 4, 2020. [Online] Available: https://www.globalfoundries.com/sites/default/files/product-briefs/pb-45rfsoi.pdf

[12] GLOBALFOUNDRIES, Santa Clara, CA, USA. *22FDX: 22nm FD-SOI Technology*. Accessed: Nov. 4, 2020. [Online] Available: https://www.globalfoundries.com/sites/default/files/22fdx-product-brief.pdf

[13] Kok Wai Johnny Chew *et al.*, "RF performance of 28nm PolySiON and HKMG CMOS devices," in *Proc. 2015 IEEE Radio Frequency Integrated Circuits Symposium*, Phoenix, AZ, USA 2015, pp. 43-36.

[14] J. D. Cressler *et al*., "SiGe technology as a millimeter-wave platform: scaling issues, reliability physics, circuit performance, and new opportunities," in *Proc. 2016 IEEE Compound Semiconductor Integrated Circuit Symposium*, Austin, TX, USA, 2013, pp. 1-3.

[15] B. Heinemann *et al*., "SiGe HBT with fT/ fMAX of 505 GHz/ 720 GHz," in *Proc. 2016 IEEE International Electron Devices Meeting*, San Francisco, CA, USA, 2016, pp. 3.1.1-3.1.4.

[16] K. Shinohara *et al.*, "Scaling of GaN HEMTs and Schottky diodes for submillimeter-wave MMIC applications," in *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 2982-2996, Oct. 2013.

[17] Infineon Technologies Austria AG, Villach, Austria. *Solution brief CoolGaN™ and GaN EiceDRIVER™*. Accessed: Nov. 4, 2020. [Online] Available: https://www.infineon.com/dgdl/Infineon-SolutionBrief_CoolGaN_and_GaN_EiceDRIVER-ProductBrief-v01_00-EN.pdf?fileId=5546d46266a498f50166bf040d9e38b8

[18] Z. Griffith *et al.*, "50 – 250 GHz high-gain power amplifier MMICs in 250-nm InP HBT," in *Proc. 2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium*, Nashville, TN, USA, 2019, pp. 1-6.

[19] A. Joseph and R. Wolf, "Integrated silicon RF front-end solutions for mobile communications," in *Proc. 2013 IEEE 10th International Conference on ASIC*, Shenzhen, 2013, pp. 1-4.

[20] P. Chevalier *et al*., "Advanced SiGe BiCMOS and CMOS platforms for optical and millimeter-wave integrated circuits," in *Proc. 2006 IEEE Compound Semiconductor Integrated Circuit Symposium*, San Antonio, TX, 2006, pp. 12-15.

[21] J. Bock *et al*., "3.3 ps SiGe bipolar technology," in *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.*, San Francisco, CA, 2004, pp. 255-258.

[22] F. Arnaud *et al*., "Low cost 65nm CMOS platform for low power & general purpose applications," in *Digest of Technical Papers. 2004 Symposium on VLSI Technology, 2004.*, Honolulu, HI, USA, 2004, pp. 10-11.

[23] C. Li *et al*., "Ka band FEM design comparison with 45nm RFSOI CMOS and high performance SiGe BiCMOS," in *Proc. 2018 14th IEEE International Conference on Solid-State and Integrated Circuit Technology*, Qingdao, 2018, pp. 1-4.

[24] S. P. Voinigescu et al., "A comparison of Si CMOS, SiGe BiCMOS, and InP HBT technologies for high-speed and millimeter-wave ICs," in *Digest of Papers*. *2004 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2004., Atlanta, GA, USA, 2004, pp. 111-114.

[25] S. P. Voinigescu, High-Frequency Integrated Circuits. New York, NY: Cambridge University Press, 2013.

[26] B. Jagannathan *et al.*, "Speed and power performance comparison of state-of-the-art CMOS and SiGe RF transistors," in *Digest of Papers. 2004 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2004., Atlanta, GA, USA, 2004, pp. 115-118.

[27] C. H. J. Poh *et al.*, "An X-band to Ka-band SPDT switch using 200 nm SiGe HBTs,"in *Proc. 2012 IEEE 12th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Santa Clara, CA, 2012, pp. 183-186.

[28] C. Li *et al.*, "< 0.8dB IL 46dBm OIP3 Ka band SPDT for 5G communication," in *Proc. 2018 IEEE 18th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Anaheim, CA, 2018, pp. 1-3.

[29] C. D. Cheon *et al.*, "A new wideband, low insertion loss, high linearity SiGe RF switch," in *IEEE Microwave and Wireless Components Letters*, vol. 30, no. 10, pp. 985-988, Oct. 2020.

[30] R. L. Schmid *et al.*, "On the analysis and design of low-loss single-pole double-throw W-band switches utilizing saturated SiGe HBTs," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 11, pp. 2755-2767, Nov. 2014.

[31] P. Song *et al.*, "A high-power, low-loss W-band SPDT switch using SiGe PIN diodes," in *Proc. 2014 IEEE Radio Frequency Integrated Circuits Symposium*, Tampa, FL, 2014, pp. 195-198.

[32] J. W. May and G. M. Rebeiz, "Design and characterization of W -Band SiGe RFICs for Passive Millimeter-Wave Imaging," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 5, pp. 1420 –1430, 2010.

[33] T. Thibeault *et al.*, "A study of ultra-high performance SiGe HBT devices on SOI," in *Proc. 2013 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Bordeaux, 2013, pp. 235-238.

[34] T. Chen *et al.*, "Footprint design optimization in SiGe BiCMOS SOI technology," in *Proc. 2008 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Monteray, CA, 2008, pp. 208-211.

[35] B. Guo *et al.*, "The thermal characteristics of SOI SiGe HBT with SiO2/Si3N4/SiO2 insulators," in *Proc. 2018 14th IEEE International Conference on Solid-State and Integrated Circuit Technology*, Qingdao, 2018, pp. 1-3.

[36] B. A. Orner *et al.*, "p-i-n diodes for monolithic millimeter wave BiCMOS applications," in *Proc. IEEE International SiGe Technology and Device Meeting, 2006*, pp. 1–2.

[37] T. Nigam *et al.*, "Material and device innovation impact on reliability for scaled CMOS technologies," in *Proc. 47th European Solid-State Device Research Conference*, pp. 134-138, 2017.

[38] E. Johnson, “Physical limitations on frequency and power parameters of transistors,” in *1958 IRE International Convention Record*, vol. 13, 1965, pp. 27-34.

[39] C. Li *et al*., “A High-Efficiency 5G K/Ka-Band stacked power amplifier in 45nm CMOS SOI process supporting 9Gb/s 64-QAM modulation with 22.4% average PAE,” in *Proc. 2017 Texas Symposium on Wireless and Microwave Circuits and Systems,* Waco, TX, 2017, pp. 1-4.

[40] A. Afsahi and L. E. Larson, “An integrated 33.5dBm linear 2.4GHz power amplifier in 65nm CMOS for WLAN applications,” in *Proc. IEEE Custom Integrated Circuits Conference 2010*, San Jose, CA, 2010, pp. 1-4.

[41] T. Li *et al.*, “Millimeter-wave continuous-mode power amplifier for 5G MIMO applications,” in *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 3088-3098, Jul. 2019.

[42] S. Li *et al.*, “A 28GHz current-mode inverse-outphasing transmitter achieving 40%/31% PA efficiency at Psat/6dB PBO and supporting 15Gbit/s 64QAM for 5G communication,” *in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2020.

[43] S. Li *et al.*, “A 28GHz packaged Chireix transmitter with direct on-antenna outphasing load modulation achieving 56%/38% PA efficiency at peak/6dB back-off output power,” in *Proc. IEEE Radio Frequency Integrated Circuits*, May 2018.

[44] C. P. Huang *et al.*, “A highly integrated dual-band SiGe power amplifier that enables 256 QAM 802.11ac WLAN radio front-end designs,” in *Proc. 2012 IEEE Radio Frequency Integrated Circuits Symposium*, Montreal, QC, 2012, pp. 225-228.

[45] CISCO. (2018). *IEEE 802.11ax: The Sixth Generation of Wi-Fi*. Available: https://www.cisco.com/c/dam/en/us/products/collateral/wireless/white-paper-c11-740788.pdf

[46] R. L. Schmid *et al*., “A 94 GHz, 1.4 dB insertion loss single-pole double-throw switch using reverse-saturated SiGe HBTs,” in *IEEE Microw. Wirel. Compon. Lett*, vol. 24, no. 1, pp. 56-58, Jan. 2014.

[47] M. Rickelt, H.-M. Rein and E. Rose, "Influence of impact-ionization-induced instabilities on the maximum usable output voltage of Si-bipolar transistors," in *IEEE Transactions on Electron Devices*, vol. 48, no. 4, pp. 774-783, April 2001.

[48] H. Veenstra *et al.*, "Analyses and design of bias circuits tolerating output voltages above BV_{CEO}," in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 10, pp. 2008-2018, Oct. 2005.

[49] M. A. Oakley *et al.*, "Large-signal reliability analysis of SiGe HBT cascode driver amplifiers," in *IEEE Transactions on Electron Devices*, vol. 62, no. 5, pp. 1383-1389, May 2015.

[50] K. Sengupta *et al.*, "On-chip sensing and actuation methods for integrated self-healing mm-wave CMOS power amplifier," in *2012 IEEE/MTT-S International Microwave Symposium Digest*, Montreal, QC, 2012, pp. 1-3.

[51] W. Liu *et al.*, "The use of base ballasting to prevent the collapse of current gain in AlGaAs/GaAs heterojunction bipolar transistors," in *IEEE Transactions on Electron Devices*, vol. 43, no. 2, pp. 245-251, Feb. 1996.

[52] S. Maas, "Ballasting HBTs for wireless power amplifier operation," in *Proc. 2006 International Workshop on Integrated Nonlinear Microwave and Millimeter-Wave Circuits*, Aveiro, 2006, pp. 2-5.

[53] S. Yoon, "Static and dynamic error vector magnitude behavior of 2.4-GHz Power Amplifier," in *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 4, pp. 643-647, April 2007.

[54] H. Najjari *et al.*, "Power amplifier with temperature adaptive biasing for improved DEVM," in *Proc. 2018 IEEE Radio Frequency Integrated Circuits Symposium*, Philadelphia, PA, 2018, pp. 320-323.

[55] C. T. Coen, "Silicon-Germanium HBT receiver components for millimeter-wave earth-observing radiometers," Ph.D. dissertation, Georgia Tech School of Elect. Comput. Eng., GA, USA, 2017. [Online]. Available: http://hdl.handle.net/1853/59773

[56] J.-S. Rieh and S. Kim, "Technology and design considerations for millimeter-wave circuits," in *Proc. International Conference on Solid-State and Integrated Circuit Technology*, 2008, pp. 1352–1356.

[57] L. S. Vempati *et al*., "Low-frequency noise in UHV/CVD epitaxial Si and SiGe bipolar transistors," in *IEEE Journal of Solid-State Circuits*, vol. 31, no. 10, pp. 1458–1467, October 1996.

[58] J. D. Cressler, "On the potential of SiGe HBTs for extreme environment electronics," in *Proceedings of the IEEE*, vol. 93, no. 9, pp. 1559–1582, Sep. 2005.

[59] K. Okada and J. Pang, "Millimeter-wave CMOS phased-array transceiver supporting dual-polarized MIMO for 5G NR," in *Proc. 2020 IEEE Custom Integrated Circuits Conference*, Boston, MA, USA, 2020, pp. 1-8.

[60] J. Pang *et al.*, "A 28-GHz CMOS phased-array beamformer utilizing neutralized bi-directional technique supporting dual-polarized MIMO for 5G NR," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 9, pp. 2371-2386, Sept. 2020.

[61] K. J. Koh and G. M. Rebeiz, "A 6-18 GHz 5-bit active phase shifter," in *Proc. 2010 IEEE MTT-S International Microwave Symposium*, Anaheim, CA, 2010, pp. 792-795.

[62] T. Li *et al*, "A 2-24-GHz 360° Full-Span Differential Vector Modulator Phase Rotator With Transformer-Based Poly-Phase Quadrature Network," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems,* to be published. doi: 10.1109/TVLSI.2020.3017707.

[63] T. Li and H. Wang, "A Millimeter-Wave Fully Integrated Passive Reflection-Type Phase Shifter With Transformer-Based Multi-Resonance Loads for 360° Phase Shifting," *IEEE Trans. on Circuits and Systems I (TCAS-I),*, vol. 65, no. 4, pp. 1406-1419, Apr. 2018.

[64] M. T. Gul *et al.*, "A 60 GHz switched-line type phase shifter using body-floating switches," in *Proc. 2013 International SoC Design Conference*, Busan, 2013, pp. 353-355.

[65] R. Wolf *et al*., "A thin-film SOI 180 nm CMOS RF switch," in *Proc. 2009 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, San Diego, CA, 2009, pp. 1–4.

[66] C. Liu *et al.*, "A fully integrated X-band phased-array transceiver in 0.13 um SiGe BiCMOS technology," in *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 2, pp. 575-584, Feb. 2016.

[67] S. Sim, L. Jeon, and J.-G. Kim, “A compact X-band bidirectional phased-array T/R chipset in 0.13 um CMOS technology,” in *IEEE Trans. Microw. Theory Tech.,* vol. 61, no. 1, pp. 562–569, Jan. 2013.

[68] M.-K. Cho *et al.*, “An active bi-directional SiGe DPDT switch with multi-octave bandwidth,” in *IEEE Microw. Wirel. Compon. Lett.,* vol. 26, no. 4, pp. 279-281, Apr. 2016.

[69] Q. Xiao, “A compact L-band broadband 6-bit MMIC phase shifter with low phase error,” in *Proc. 2011 6th European Microwave Integrated Circuit Conference*, Manchester, 2011, pp. 410-413.

[70] B. Cetindogan *et al*., “A 6 Bit Vector-Sum Phase Shifter With a Decoder Based Control Circuit for X-Band Phased-Arrays,” in *IEEE Microw. Wirel. Compon. Lett.*, vol. 26, no. 1, pp. 64-66, Jan. 2016.

[71] J. P. Comeau *et al*., “Silicon-Germanium Receiver for X-Band Transmit/Receive Radar Modules,” in *IEEE Journal of Solid-State Circuits*, vol. 43, no. 9, pp. 1889-1896, Sept. 2008.

[72] M. K. Cho *et al*., “An X-Band 5 bit phase shifter with low insertion loss in 0.18 um SOI Technology,” in *IEEE Microw. Wirel. Compon. Lett.*, vol. 22, no. 12, pp. 648-650, Dec. 2012.

[73] T. Fujiwara and M. Shimozawa, “Broadband and highly accurate X-band vector-sum phase shifter using LC-type power splitter,” in *Proc. 2018 13th European Microwave Integrated Circuits Conference* , Madrid, 2018, pp. 122-125.

[74] W. L. Chan and J. R. Long, “A 58-65 GHz neutralized CMOS power amplifier with PAE above 10% at 1-V supply” in *IEEE Journal of Solid-State Circuits*, vol. 45, no. 3, pp. 554-564, Mar. 2010.

[75] T. B. Kumar *et al*., “A 60-GHz bi-directional variable gain amplifier with microstrip-line interconnect in 65 nm CMOS,” in *Proc. 2016 IEEE iWEM*, Nanjing, 2016, pp. 1-3.

[76] M. K. Cho *et al.*, “A switchless CMOS bi-directional distributed gain amplifier with multi-octave bandwidth,” in *IEEE Microw. Wirel. Compon. Lett.*, vol. 23, no. 11, pp. 611-613, Nov. 2013.

[77] S. Zeinolabedinzadeh *et al.*, “A W-band SiGe transceiver with built-in self-test,” in Proc. *2019 IEEE 19th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Orlando, FL, USA, 2019, pp. 1-4.

[78] C. P. Huang *et al.*, “A multimode 5–6 GHz SiGe BiCMOS PA design powers emerging wireless LAN radio standards,” in *Proc. 2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Miami, FL, 2017, pp. 38-41.

[79] R. S. Hughes, *Logarithmic Amplification with Application to Radar and EW*. Dedham, MA: Artech, 1986.

[80] A. Woroncow and J. Croney, “A true IF logarithmic amplifier using twin-gain stages,” *Radio Electron. Eng*., vol. 32, no. 3, pp. 149–155, Sep. 1966.

[81] K. Kim and Y. Kwon, "A broadband logarithmic power detector in 0.13-μm CMOS," in *IEEE Microwave and Wireless Components Letters*, vol. 23, no. 9, pp. 498-500, Sep 2013

[82] J. Wang *et al*, “A wide band CMOS radio frequency RMS power detector with 42-dB dynamic range,” in *Proc. 2015 IEEE International Symposium on Circuits and Systems*, Lisbon, 2015, pp. 1678-1681.

[83] P. Stärke *et al.*, “A wideband square-law power detector with high dynamic range and combined logarithmic amplifier for 100 GHz F-Band in 130 nm SiGe BiCMOS,” in *Proc. 2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Miami, FL, 2017, pp. 118-121.

[84] Y. Zhou and M. Y. Chia, “A low-power ultra-wideband CMOS true RMS power detector,” in *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 5, pp. 1052-1058, May 2008.

[85] S. Qayyum and R. Negra, “0.16 mW, 7–70 GHz distributed power detector with 75 dB voltage sensitivity in 130 nm standard CMOS technology,” in *Proc. 2017 12th European Microwave Integrated Circuits Conference*, Nuremberg, 2017, pp. 13-16.

[86] E. Ozeren *et al*., “A high dynamic range power detector at X-band,” in *IEEE Microw. Wirel. Compon. Lett*., vol. 26, no. 9, pp. 708–710, Sep. 2016.

[87] K Lam *et al*., "Wideband millimeter wave pin diode SPDT switch using IBM 0.13µm SiGe technology," in *Proc. 2007 European Microwave Integrated Circuit Conference*, Munich, 2007, pp. 108-111.

[88] J. He *et al.*, "Analysis and design of 60-GHz SPDT switch in 130-nm CMOS," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 10, pp. 3113-3119, Oct. 2012.

[89] M. Uzunkol and G. Rebeiz, "A low-loss 50–70 GHz SPDT Switch in 90 nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 45, no. 10, pp. 2003-2007, Oct. 2010.

[90] R. Shu and Q. J. Gu, "A transformer-based V-band SPDT switch," in *IEEE Microw. Wirel. Compon. Lett.*, vol. 27, no. 3, pp. 278-280, March 2017.

[91] M. Parlak and J. F. Buckwalter, "A 2.5-dB insertion loss, DC-60 GHz CMOS SPDT switch in 45-nm SOI," in *Proc. 2011 IEEE Compound Semiconductor Integrated Circuit Symposium*, Waikoloa, HI, 2011, pp. 1-4.

[92] M. Davulcu *et al.*, "A new 5-13 GHz slow-wave SPDT switch with reverse-saturated SiGe HBTs," in *IEEE Micro. Wireless Compon. Lett.*, vol. 27, no. 6, pp. 581-583, June 2017.

[93] J. A. Qayyum *et al.*, "A 20–60 GHz ultra-wideband SPDT switch for multi-band transceivers," in *Proc. 2020 IEEE 20th Topical Meeting on Silicon Monolithic Integr. Circuits in RF Systems*, San Antonio, TX, USA, 2020, pp. 16-18.

[94] K. Kibaroglu et *al.*, "A low-cost scalable 32-Element 28-GHz phased array transceiver for 5G communication links based on a 2×2 beamformer flip-chip unit cell," in *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1260-1274, May 2018.

[95] M. Davulcu *et al.*, "A 7-Bit Reverse-Saturated SiGe HBT Discrete Gain Step Attenuator," in *IEEE Trans, Circuits Syst., II, Exp. Briefs*, vol. 67, no. 4, pp. 665-669, April 2020.

[96] P. Asbeck and H. Krishnaswamy, "Stacked-transistor mm-wave power amplifiers," in *mm-Wave Silicon Power Amplifiers and Transmitters,* H. Hashemi and S. Raman, Ed. Cambridge CB2 8BS, UK: Cambridge University Press, 2016, pp. 207-256.

[97] Y.-H. Hsiao *et al*., "Millimeter-wave CMOS power amplifiers with high output power and wideband performances," in *IEEE Trans. Microw. Theory Techn*, vol. 61, no. 12, pp. 4520–4533, Dec. 2013.

[98] E. Wagner and G. M. Rebeiz, "Single and power-combined linear E-band power amplifiers in 0.12- μm SiGe with 19-dBm average power 1-GBaud 64-QAM modulated waveforms," in *IEEE Trans. on Microw. Theory Techn.*, vol. 67, no. 4, pp. 1531-1543, April 2019.

[99] R. Ben *et al.*, "A 21 dBm 60 GHz SiGe power amplifier using modified Wilkinson combiner," in *Proc. 2016 11th European Microw. Integr. Circuits Conf.* (EuMIC), London, 2016, pp. 409-412.

[100] W. Sun and C. Kuo, "A 19.1% PAE, 22.4-dBm 53-GHz Parallel Power Combining Power Amplifier with Stacked-FET Techniques in 90-nm CMOS," in *Proc. 2019 IEEE MTT-S Int. Microw. Symp.* (IMS), Boston, MA, USA, 2019, pp. 327-330.

[101] C. Chou *et al.*, "Design of a V -Band 20-dBm Wideband Power Amplifier Using Transformer-Based Radial Power Combining in 90-nm CMOS," in *IEEE Trans. Microw. Theory Techn*, vol. 64, no. 12, pp. 4545-4560, Dec. 2016.

[102] H. T. Nguyen *et al.*, "A 60GHz CMOS power amplifier with Cascaded asymmetric distributed-active-transformer achieving watt-level peak output power with 20.8% PAE and Supporting 2Gsym/s 64-QAM Modulation," in *Proc. 2019 IEEE Int. Solid- State Circuits Conf.*, San Francisco, CA, USA, 2019, pp. 90-92.

[103] J. Zhao *et al.*, "A 15 GHz-bandwidth 20dBm PSAT power amplifier with 22% PAE in 65nm CMOS," in *Proc. 2015 IEEE Custom Integr. Circuits Conf.* (CICC), San Jose, CA, 2015, pp. 1-4.

[104] J. Yeh *et al.*, "MMW Ultra-Compact N-Way Transformer PAs Using Bowtie-Radial Architecture in 65-nm CMOS," in *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 7, pp. 460-462, July 2015.

[105] F. Shirinfar *et al.*, "A fully integrated 22.6dBm mm-Wave PA in 40nm CMOS," in *Proc. 2013 IEEE Radio Freq. Integr. Circuits Symp*. (RFIC), Seattle, WA, 2013, pp. 279-282.

[106] Kaizhe Guo *et al.*, "A 60-GHz 1.2 V 21 dBm power amplifier with a fully symmetrical 8-way transformer power combiner in 90 nm CMOS," in *Proc. 2014 IEEE MTT-S Int. Microw. Symp.* (IMS), Tampa, FL, 2014, pp. 1-3.

[107] Y. Chang *et al.*, "A V-Band Power Amplifier With 23.7-dBm Output Power, 22.1% PAE, and 29.7-dB Gain in 65-nm CMOS Technology," in *IEEE Trans. on Microw. Theory Techn.*, vol. 67, no. 11, pp. 4418-4426, Nov. 2019.

[108] H. T. Nguyen and H. Wang, "A Coupler-Based Differential mm-Wave Doherty Power Amplifier With Impedance Inverting and Scaling Baluns," in *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1212-1223, May 2020.

[109] D. Pepe *et al*., "1.29-W/mm2 23-dBm 66-GHz power amplifier in 55-nm SiGe BiCMOS with in-line coplanar transformer power splitters and combiner," in *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 12, pp. 1146-1148, Dec. 2017.

[110] Y. Zhao and J. R. Long, "A Wideband, Dual-Path, Millimeter-Wave Power Amplifier With 20 dBm Output Power and PAE Above 15% in 130 nm SiGe-BiCMOS," in *IEEE J.of Solid-State Circuits*, vol. 47, no. 9, pp. 1981-1997, Sept. 2012.

[111] H. Park *et al.*, "Millimeter-Wave Series Power Combining Using Sub-Quarter-Wavelength Baluns," in *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2089-2102, Oct. 2014.

[112] S. Daneshgar and J. F. Buckwalter, "Compact Series Power Combining Using Subquarter-Wavelength Baluns in Silicon Germanium at 120 GHz," *in IEEE Trans.Microw. Theory Techn*., vol. 66, no. 11, pp. 4844-4859, Nov. 2018.

[113] B. Rabet and J. Buckwalter, "A high-efficiency 28GHz outphasing PA with 23dBm output power using a triaxial balun combiner," in *Proc. 2018 IEEE Int. Solid - State Circuits Conf.*, San Francisco, CA, 2018, pp. 174-176.

[114] S. Kim *et al.*, "A High-Dynamic-Range W-Band Frequency-Conversion IC for Microwave Dual-Conversion Receivers," *in Proc. 2016 IEEE CSICS*, Austin, TX, 2016, pp. 1-4.

[115] S. Li *et al.*, "A multi-feed antenna for antenna-level power combining," in *Proc. IEEE International Symposium on Antennas and Propagation (APS/URSI)*, June 2016.

[116] S. Li *et al.*, "A millimeter-wave dual-feed square loop antenna for 5G communications," *IEEE Trans. Antennas Propag*., vol. 65, no. 12, pp. 6317–6328, Dec. 2017.

[117] S. Li *et al.*, "Multi-feed antenna and electronics co-design: an E-band antenna-LNA front-end with on-antenna noise-canceling and gm-boosting", IEEE *J. Solid-State Circuits*, to be published. doi: 10.1109/JSSC.2020.3024592.

[118] S. Li *et al.*, "A 28-GHz flip-chip packaged Chireix transmitter with on-antenna outphasing active load modulation," IEEE *J. Solid-State Circuits*, vol. 54, no. 5, pp. 1243-1253, May 2019.

[119] W. L. Stutzman and G. A. Thiele, Antenna Theory and Design, 3rd ed. New York, NY, USA: Wiley, 2012.

[120] N. Marchand, "Transmission-line conversion transformers," Electronics, vol. 17, pp. 142–145, Dec. 1944.

[121] K. Sachse, "The scattering parameters and directional coupler analysis of characteristically terminated asymmetric coupled transmission lines in an inhomogeneous medium," *in IEEE Trans. Microw. Theory Techn.*, vol. 38, no. 4, pp. 417-425, April 1990.

[122] K. Sachse and A. Sawicki, "Quasi-ideal multilayer two- and three-strip directional couplers for monolithic and hybrid MICs," in *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 9, pp. 1873–1882, Sep. 1999.

[123] K. Wincza and S. Gruszczynski, "Asymmetric Coupled-Line Directional Couplers as Impedance Transformers in Balanced and n-Way Power Amplifiers," in *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 7, pp. 1803-1810, July 2011.

[124] K. Wincza *et al.*, "Approach to the Design of Asymmetric Coupled-Line Directional Couplers With the Maximum Achievable Impedance-Transformation Ratio," in *IEEE Trans. Microw. Theory Techn*., vol. 60, no. 5, pp. 1218-1225, May 2012.

[125] R. Smolarz *et al.*, "Impedance Transforming Tandem Couplers With Increased Bandwidth and Transformation Ratio," in *IEEE Microw. Wirel. Compon. Lett*., vol. 28, no. 4, pp. 299-301, April 2018.

[126] M. Abbasi *et al.*, "Q-, V-, and W-band power amplifiers utilizing coupled lines for impedance matching," in *2008 IEEE MTT-S Int. Microw. Symp. Dig*., Atlanta, GA, USA, 2008, pp. 863-866.

[127] D. M. Pozar, *Microwave Engineering*, 4th ed. New York, NY, USA: Wiley, 2005.

[128] Jae-Sung Rieh *et al.*, "Structure optimization of trench-isolated SiGe HBTs for simultaneous improvements in thermal and electrical performances," in *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2744-2752, Dec. 2005.

[129] I. Ju *et al.*, "Highly Linear High-Power 802.11ac/ax WLAN SiGe HBT Power Amplifiers With a Compact 2nd-Harmonic-Shorted Four-Way Transformer and a Thermally Compensating Dynamic Bias Circuit," in *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2356-2370, Sept. 2020.

[130] S. Alluri *et al.*, "Simulation Technique for Thermal Resistance in CMOS-SOI Power Amplifier Integrated Circuits," in *Proc. 2020 IEEE Topical Conf. RF/Microw. Power Amp. Radio and Wirel. App.*, San Antonio, TX, USA, 2020, pp. 9-11.

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