A 13.56 MHz Bidirectional IPT System with Wirelessly Synchronised Transceivers for Ultra-Low Coupling Operation

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***Abstract*—This paper presents a high-frequency inductive power transfer (HF-IPT) system with bidirectional capability employing a new wireless synchronisation method. Synchronisation is achieved by transmitting a reference ultra high frequency tone (433.92 MHz) that is stepped down to 13.56 MHz in each transceiver. This allows the operating frequency to be locked across the two sides of the system. Afterwards, a phase search is performed looking for maximum power throughput, determining the phase at the point of resonance (i.e., no reflected reactances). The experimental implementation is achieved with two back-to-back Class EF coil-drivers driven by independent synchronisation circuits. In the experimental setup a constant input voltage is set for each of the two coil-drivers by implementing a source-sink configuration, emulating a bidirectional DC-DC conversion stage at each side. Experimental results show successful transceiver synchronisation, and 4 W were transferred from one end to the other and conversely at an ultra-low coupling of 1.6%. This proves that the combination of the load-independent Class EF transceivers and the synchronisation technique introduced herein is suitable for applications that require large tolerance to misalignment and air gaps larger than one coil diameter, such as in micro e-mobility.**

I. Introduction

One of the differences of HF-IPT with respect to systems working in the hundreds-of-kilohertz range is the possibility of designing a system that does not necessarily use magnetically permeable materials. This is due to the improvement in quality factor of low inductance coils ($<5\,\mu\text{H}$) in the megahertz range [1]–[4], which is around 760 in the presented work. A direct consequence of operating in this frequency range is the possibility of integration of compact light-weight systems in a wide number of applications where a high tolerance to misalignment is required. These applications range from consumer electronics to healthcare and military.

Active rectification in IPT allows operation of both tanks at resonance even with varying coupling factors (k) and loads, allowing operation at ultra-low k ($<2\%$). For low k it is challenging to operate at resonance with passive rectifiers because in such conditions it is required to operate at a very low input resistance, and the parasitic capacitance of the diodes tends to dominate and therefore detune the resonant tank. Efficiency can also be improved when using active rectification due to lower conduction losses. Synchronous rectification is a key step to achieve full-control of a transceiver's power flow, enabling implementation of more advanced applications such as bidirectional wireless power transfer.

Bidirectional wireless power transfer is an increasingly growing topic of research, with applications ranging from low-power battery charging for drones [5] to high-power EV-to-grid applications [6]. One of the key aspects in bidirectional IPT systems is synchronisation: for a system to operate either as an inverter or a rectifier, the coil current needs to be respectively at a phase of 0° or 180° with respect to the induced EMF produced by the other coil, and thus operate at unity power factor (i.e. no reflected reactances).

II. Design of bidirectional coil drivers using Class EF Circuits

The Class EF topology (both transceivers in Fig. 1) is a commonly employed HF-IPT coil driver due to its high efficiency at MHz frequencies [7], [8] and its convenience of only comprising one low side transistor. This topology is usually designed to operate at constant duty cycle and frequency (i.e. in open loop), requiring power throughput control to be implemented by cascading an additional stage with the converter. This topology can be employed as an inverter or a rectifier [9], [10], where the direction of the power flow is determined by the relative polarity of the magnetic link and the relative phase ($\pm 90^\circ$) of the coils currents [11]. The angle between coil currents is chosen to achieve an induced voltage in the coil which is in phase (or 180° out of phase) with the coil currents, causing the reflected impedance to be purely resistive:

$$\begin{aligned}\boldsymbol{v_{\mathrm{M}}} &= -2\pi f_{\mathrm{i}_{\mathrm{coil_A}}} k\sqrt{L_{3_\mathrm{A}} L_{3_\mathrm{B}}}\, i_{\mathrm{coil_B}} \sin(\theta_\mathrm{B}) \\ &\quad + \boldsymbol{j}\left[2\pi f_{\mathrm{i}_{\mathrm{coil_A}}} k\sqrt{L_{3_\mathrm{A}} L_{3_\mathrm{B}}}\, i_{\mathrm{coil_B}} \cos(\theta_\mathrm{B})\right] \\ &= 2\pi f_{\mathrm{i}_{\mathrm{coil_A}}} k\sqrt{L_{3_\mathrm{A}} L_{3_\mathrm{B}}}\, i_{\mathrm{coil_B}} \underline{/\theta_\mathrm{B} + 90^\circ}.\end{aligned} \tag{1}$$

Assuming the two resonant tanks are tuned at the same frequency of the currents in the two coils ($f_{\mathrm{i}_{\mathrm{coil_A}}} = f_{\mathrm{i}_{\mathrm{coil_A}}}$), from (1) the imaginary part of the induced voltage in the primary is zero for $\theta_B = \pm 90^\circ$.

In [10] a load-independent design formulation for the Class EF topology was proposed. This is achieved by relaxing

TABLE I: Components values for the Transceivers

Component	Value	Description
C_1 (pF)	156+C_{oss}	Vishay QUAD HIFREQ
C_2 (pF)	176	Vishay QUAD HIFREQ
C_3 (pF)	130	Vishay QUAD HIFREQ
L_1 (μH)	88	Wurth Elektronik WE-PD
L_2 (nH)	234	Coilcraft 2014VS
L_{p} & L_{s} (nH)	1181	IPT PCB coils
Q_1	GS66504B (650 V, 15 A) GaN FET	

the classic zero-voltage-switching (ZVS) and zero-derivative-switching (ZDS) design constraints to ZVS only. Following the design methodology in [10] it is possible to obtain a set of passive components choices for which the transistor drain voltage achieves zero-voltage-switching (the voltage converges to zero at turn-on) independent of the real coupled load. Therefore, as long as the converter remains tuned (with no reflected reactance) the load independent Class EF converter can be employed as an inverter or a rectifier, and it tolerates changes in the direction of the power flow without affecting its switching performance.

The components choice for the work presented in this paper is shown in Table I.

III. Wireless Synchronisation of the HF-IPT Transceivers

A. Background

Some of the most common and practical synchronisation strategies for kilohertz IPT systems revolve around the concept of using a sense-coil at the receiving-end to extract information about the frequency and phase of the primary and derive a driving signal for the secondary after subtracting a portion of the secondary coil current [6], [12] due to its parasitic coupling with the sense coil. A similar approach for HF-IPT is implemented in [13], where the driving signal is derived directly from the secondary current caused by the induced EMF from the primary. One of the major challenges with these approaches is low-power/low-coupling operation: when the induced EMF from the primary is low, the SNR of the signal generating the driving waveform deteriorates, leading to frequency and phase oscillation. In [13] the lowest power for which synchronisation occurs successfully is 4 W.

Alternative techniques in HF-IPT rely on a similar concept: directly exploiting the induced EMF on the secondary to obtain a drain-voltage waveform at the correct relative phase from the primary [14], [15]. When a threshold voltage is crossed, the transistor is switched on, forcing the drain voltage to zero. Since this threshold is higher than zero, the system will always exhibit hard-switching. These techniques are also heavily reliant on load and k: as the induced EMF decreases, the switching noise of the secondary dominates the drain waveform, making it difficult to perform frequency and phase synchronisation reliably for very low k.

From simulations of the technique proposed in [14] it can be observed that changes in k and load from the designed operating point can lead to sub-optimal operation (hard-switching or diode conduction) and in some cases instability. The results in [15] show that system resilience can be improved through a closed loop control by adjusting the duty cycle. While this is an interesting concept, it should be noted that Class EF circuits are designed for a fixed duty cycle. Therefore this approach may lead to loss of advantageous properties such as ZVS, ZDS and load independence.

B. Synchronisation through high-frequency tone

Our approach to synchronisation is to maintain the driving signals independent from the other coil drivers' parameters, allowing correct operation at low couplings. The proposed wireless synchronisation method does not depend on load and coupling factor since it is performed through an additional communication link. While coupling and load play a role in determining the switching losses during different phases of the synchronisation process, the algorithm is designed to minimise the heating during synchronisation at high loads by decreasing the input voltage while phase search is being performed. Further fine tuning of the phase is performed after synchronisation has occurred and the input voltages are stepped up to their nominal values. This is done to account for the variation in the transistor's output capacitance (C_{oss}) with the drain voltage. In our work we showcase a synchronised system with couplings as low as 1.6%.

The proposed technique consists in transmitting a 433.92 MHz tone (a unmodulated sine-wave) through a separate module (TXs) to both Coil driver A and Coil driver B as shown in Fig. 2a. The two sub-modules Sync A and Sync B isolate this high-frequency tone through a signal conditioner (B39431B3782Z810 from RF360) and use a prescaler to step it down to 13.56 MHz (two MC12093DG divide the signal first by 4 and then by 8). In Sync B the signal's duty cycle is adjusted by a monostable circuit. Before getting to this step, the signal in Sync A undergoes a phase adjustment with a programmable delay module (DS1023-50) controlled through a microprocessor (EK-TM4C123GXL) and is fed to a multiplexer together with its inverse. This allows a further phase shit of 180° to be selected through the microprocessor to change the direction of the power flow. Adjusting the phase of a single side comes with the advantages of reduced system complexity and lower cost.

The phase needs to be adjusted because of the inherent random phase injection when a signal is stepped down from high frequency to low frequency: the frequency step-down in Sync A and Sync B will not always occur at the same instant. Therefore, the relative phase of the unadjusted V_{GS_A} to V_{GS_B} will be random and equal to $\frac{n\times 2\pi}{m}$, with m being equal to the frequency division factor (in this case 32) and n being a random integer between 1 and m.

The optimal phase is detected by sweeping the delay in DS1023-50 and tracking the input current i_{DC_A} with the circuit shown in Fig. 2b. For a perfectly tuned system the point at

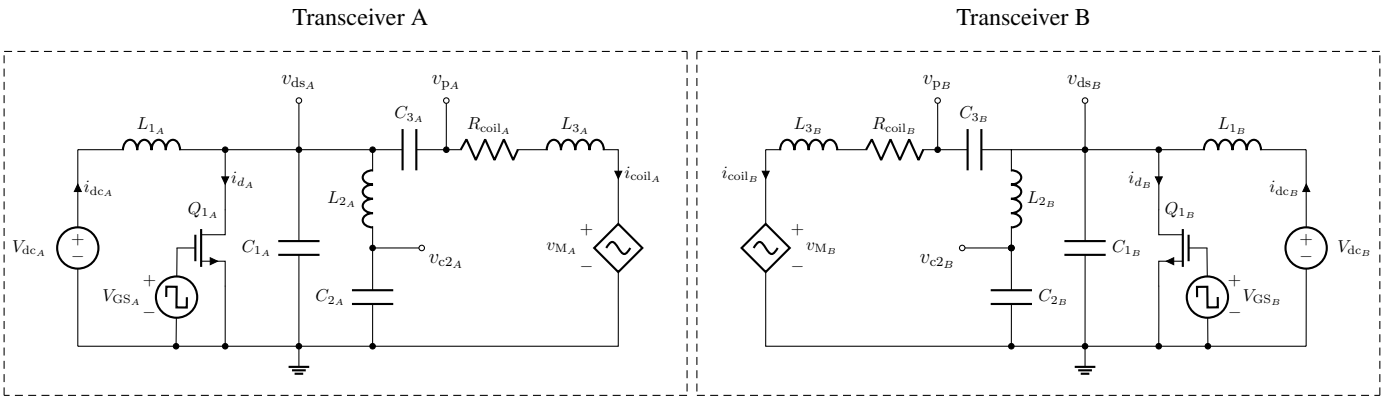
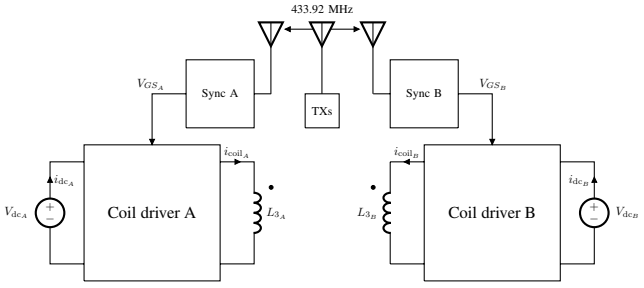
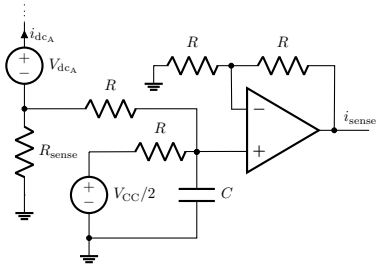


Fig. 1: Circuit diagram of two bidirectional Class EF converters with the loads modelled as dependent voltage sources.



(a) Block diagram of the system



(b) Current sense circuit

Fig. 2: Synchronisation schematics

which $i_{\mathrm{DC_A}}$ is maximised corresponds to the optimal phase for Coil driver A working as a transmitter with unity power factor (the induced EMF from L_{3_B} to L_{3_A} is in phase with the current in L_{3_A}). When $i_{\mathrm{DC_A}}$ is minimised Coil driver A will be working as a receiver with unity power factor (the induced EMF from L_{3_B} to L_{3_A} is 180° out of phase with the current in L_{3_A}). The optimal relative phase in these two cases is $\pm 90°$.

The coil drivers are expected to operate sub-optimally (out of tune) for the synchronisation tracking period due to the reactive reflected impedance produced by the relative phase diversion from $\pm 90°$. It is not recommended to perform the phase search at high k ($> 3\%$) and full power due to the momentarily detuned operation of the transceivers. This can lead to heating of the transceivers because of the additional losses that come with hard-switching or body-diode conduction. It can be observed in Fig. 3 that even at a coupling of 1.6% for $\theta_B \simeq 0°$, the transistor approaches a temperature of 60 °C. This effect is even more prominent when coupling increases, making it necessary to either decrease the load to prevent excessive detuning while the synchronisation process is not complete or perform synchronisation at a very high speed, also decreasing the available time window to perform readings of the input current.

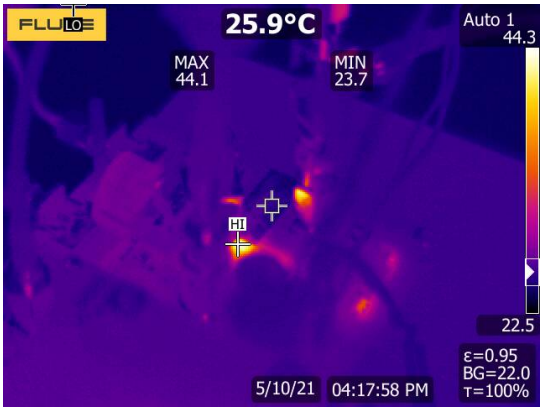
Performing the phase search at low power by reducing the input voltage of the synchronising side is more convenient. Once phase and frequency are locked, the voltage can be stepped-up to its nominal value. This will allow convergence to a phase that is close to optimal, reducing the likelihood of damaging the transceivers. Because the output capacitance of the transistor (C_{oss}) is dependent on voltage, a further fine search to optimise the phase at the nominal voltage will need to be performed: this can be done at an angle of $\pm 30°$ from the initial phase value.

In the presented work we aim to demonstrate the basic principles of synchronisation through a ultra high frequency tone. This can be further improved by using more sophisticated techniques for encoding the synchronisation tone for higher robustness of the communication link, reducing the effect of noise while also addressing constraints related to system bandwidth. One possible solution would be ultra-wideband communication, thanks to the high achievable data-rates and flexibility of this technology for applications such as position localisation [16].

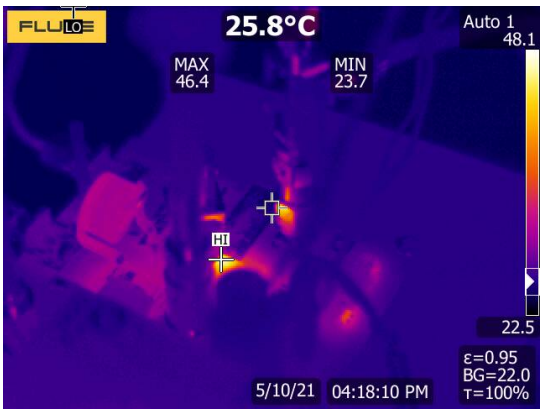
IV. Experimental Demonstration of a Wirelessly Synchronised Bidirectional IPT System at 1.6% Coupling

The test rig is comprised of two identical transceivers as shown in Fig. 4. Labels of Fig. 4a indicate the system blocks presented in Fig. 2a.

Synchronisation is achieved by following the method explained in Section III. The voltage sources $V_{\mathrm{dc_A}}$ and $V_{\mathrm{dc_B}}$ are connected in parallel with two electronic loads operat-



(a) Transistor temperature for $\theta_B \simeq -90°$



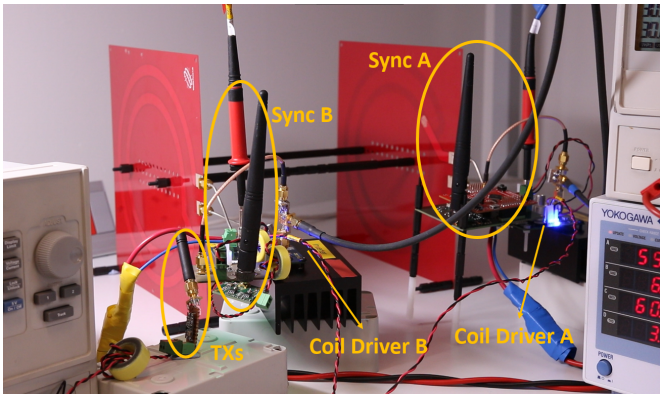
(b) Transistor temperature for $\theta_B \simeq -60°$

(c) Transistor temperature for $\theta_B \simeq 0°$

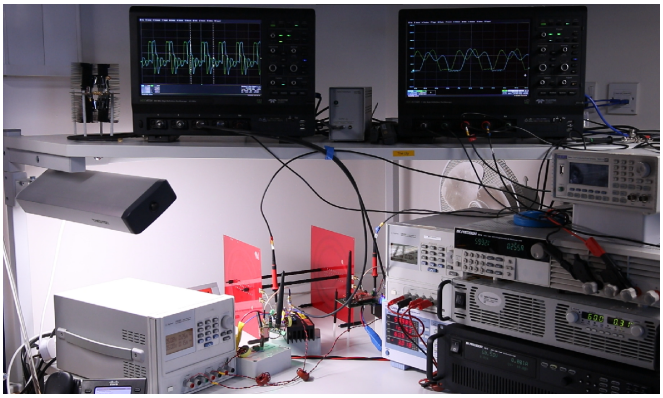
Fig. 3: Transistor temperature in Transceiver A for different points in the synchronisation process at $k = 1.6\%$

ing in constant voltage (CV) mode to obtain a sink-source configuration. This step allows each side to operate under a regulated DC input voltage, granting the transceivers the option of working in bidirectional mode even at power factors different from unity (e.g. full range of relative phases for the gate voltage signals).

In the presented experimental setup there is a $27.4\,\mathrm{cm}$ separation between coils, corresponding to a k of 1.6%. The



(a) IPT Link at 1.6% Coupling



(b) Setup including instrumentation

Fig. 4: Test rig pictures

coupling factor was estimated using an AC load tuned at the frequency of operation (13.56 MHz) and using (2):

$$k = \sqrt{\frac{R_{\mathrm{eq}}(R_{\mathrm{s}} + R_{\mathrm{sec}})}{4\pi^2 f_{i_{coil_A}}^2 L_{3_{\mathrm{A}}} L_{3_{\mathrm{B}}}}}, \tag{2}$$

with R_{s} being the series resistance of the AC load coil, R_{sec} being the resistance of the AC load and R_{eq} the real part of the reflected impedance in the primary coil. These parameters and the primary and secondary coil inductance are measured using an impedance analyser.

The estimation of coupling factor derived using this method was further validated using a CST Studio simulation of the link presented in this work.

A. Tracking Algorithm for Phase Synchronisation with $k < 3\ \%$

The synchronisation algorithm is based on tracking the maximum input current. From (1), the induced voltage in the primary coil is maximised or minimised for $\theta_B = \pm 90°$. This corresponds to the two cases in which the modulus of the load is maximum, requiring the highest input current.

As explained in the Section III, driving the transceivers at a phase different from $\pm 90°$ will lead to sub-optimal operation, with additional lossess in both primary and secondary sides. To reduce the risk of transceiver damage it is necessary to

employ a synchronisation technique that minimises the time of operation in critical regions.

The proposed solution is divided into three steps. In the first step four different values of θ_B, which are $90°$ apart from each other, are tested as shown in Fig. 5. The angle associated with the highest input current is selected for a more detailed search, with the knowledge that the synchronisation has approached a safe region of operation. In Fig. 5 this corresponds to the angle $\theta_2 \simeq 300°$.

The next step narrows down the optimal region of operation by testing two additional angles between θ_2 and the two adjacent operating points from the previous iteration, θ_1 and θ_3.

Once the operating point associated with the maximum current is obtained from the second synchronisation step, an exhaustive search in a range of $\pm 30°$ is performed as illustrated in Fig. 6. This allows convergence to the optimal phase for synchronisation of the two bidirectional transceivers, whose power flow can be reversed by injecting an additional phase of $180°$.

Each measurement of input current is taken five times and averaged to minimise the effect of noise. The average time of each measurement is $24\,\mathrm{ms}$. The duration of the first synchronisation step is $480\,\mathrm{ms}$. As previously mentioned, it is necessary to keep this time-window brief to avoid transceiver damage. The total synchronisation time is 3.6 s.

The accuracy of this method depends on the minimum achievable delay step of DS1023-50, which is $0.50\,\mathrm{ns}$. This corresponds to an accuracy of $2.5°$ for a 13.56 MHz system.

B. Tracking Algorithm for Phase Synchronisation with $k > 3\ \%$

If the magnitude of the input current exceeds a threshold, either because of an increase in coupling or load, the synchronisation strategy explained in Section IV-A is adapted to avoid excessive heating.

The input voltages are stepped down to a safe value of 10 V to perform the first three synchronisation steps. When synchronisation occurs, the input voltages are stepped back up to their nominal values and the third synchronisation step (Fig. 6b) is repeated to account for the detuning derived from a change of the capacitance C_{oss} at lower voltages.

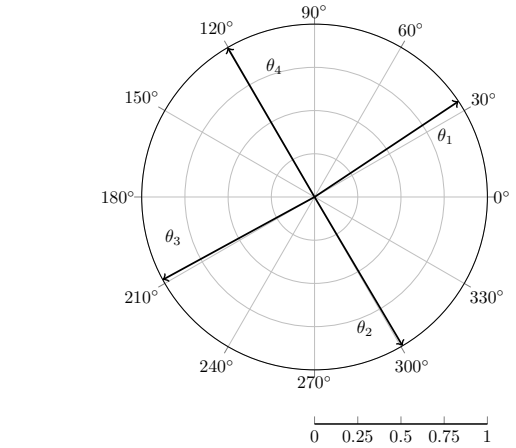
To prove this concept the change in input voltages is programmed using MATLAB to control the electronic loads at both ends, while the rest of the synchronisation algorithm is performed by a microprocessor.

Fig. 8 shows the effect of the input voltage transition on the drain voltage waveform when employing this synchronisation strategy.

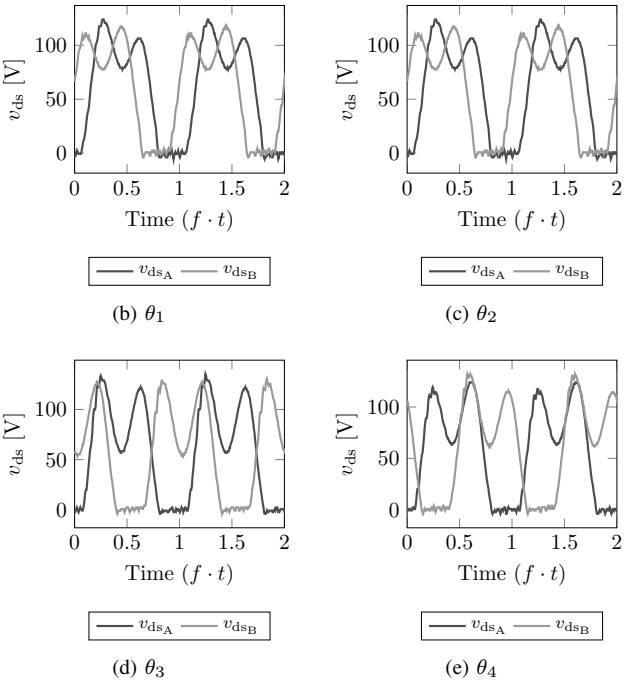
For $k = 3.2\%$ and a load of 11.4 W, the end-to-end efficiency is 54%, while for $k = 4.9\%$ and a load of 14.1 W, the end-to-end efficiency is 58%.

C. System Performance

For $k = 1.6\%$ it is possible to transfer 4 W with 30% efficiency. Once the synchronisation occurs, phase and frequency lock are maintained. Power flow can be reverted by introducing a further phase shift of $180°$.



(a) Phasor diagram of the first synchronisation step



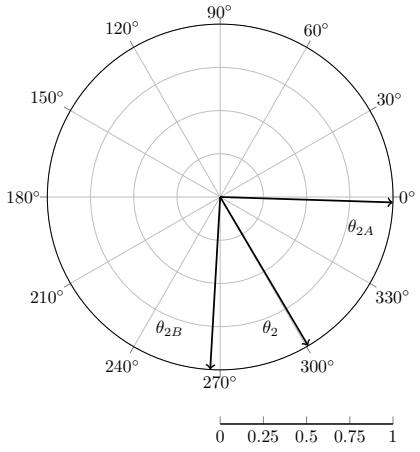
(b) θ_1 (c) θ_2 (d) θ_3 (e) θ_4

Fig. 5: Phasor diagram and drain voltage waveforms of the first synchronisation step for $k = 1.6\%$

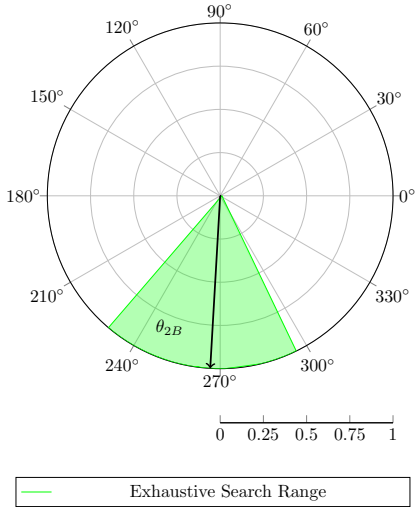
V. Conclusion and Future Work

In this work we present a bidirectional 13.56 MHz IPT system operating at couplings as low as 1.6% by implementing a new synchronisation method.

We have demonstrated the main principles of the proposed synchronisation technique based retrieval of the operating frequency through transmission of a ultra high frequency tone. There is still room for improvement in terms of communication link robustness and system integration: a more



(a) Phasor diagram of the second synchronisation step



(b) Phasor diagram of the third synchronisation step

Fig. 6: Phasor diagram of the second and thirds synchronisation steps for $k = 1.6\%$

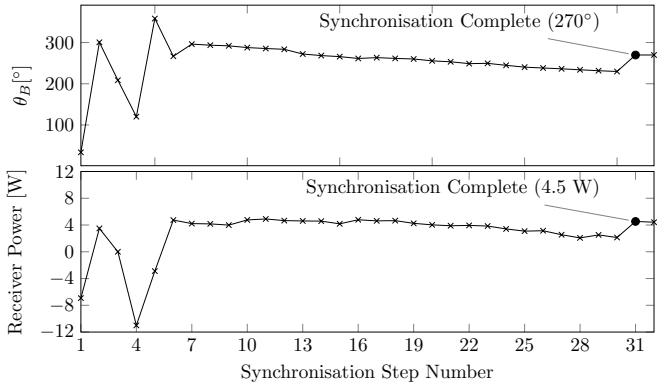
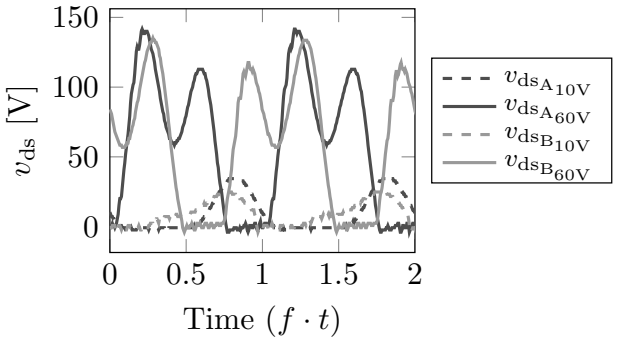
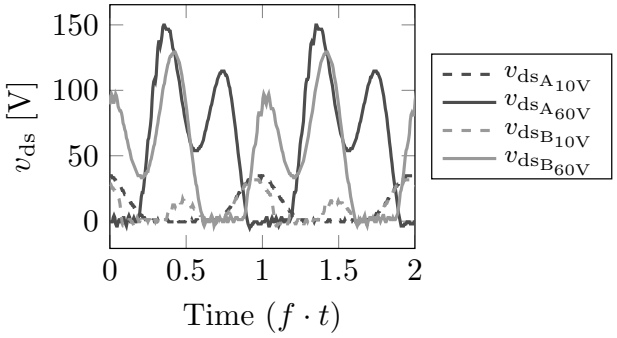


Fig. 7: Receiver power and angle during the synchronisation process for $k = 1.6\%$



(a) $k = 3.2\%$



(b) $k = 4.9\%$

Fig. 8: Drain voltage of transceivers A and B at different input voltages during high-coupling synchronisation; $v_{\mathrm{ds_{A_{10V}}}}$ and $v_{\mathrm{ds_{B_{10V}}}}$ indicate $V_{\mathrm{dc_A}} = V_{\mathrm{dc_B}} = 10\ V$; $v_{\mathrm{ds_{A_{60V}}}}$ and $v_{\mathrm{ds_{B_{60V}}}}$ indicate $V_{\mathrm{dc_A}} = V_{\mathrm{dc_B}} = 60\ V$

sophisticated way of encoding the 433.92 MHz tone (like ultra-wideband) would make this particular synchronization method easier to miniaturise and more resilient to external sources of noise. In addition to the link improvements, it will also be necessary to implement a bidirectional DC-DC converter on each side of the system to allow for changes in input voltage for the high-coupling synchronization method.

The experiments demonstrate that even at ultra low coupling factors ($< 2\%$) it was possible to successfully transfer 4 W with an efficiency of 30% and a synchronisation time of less than 4 seconds. Both low coupling ($< 3\%$) and high coupling ($> 3\%$) synchronisation are possible with a precision of $2.5°$ and minimum risk of transceiver damage in the synchronisation process.

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