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Multi-Objective Design of Single-Phase Differential Buck Inverters With Active Power Decoupling

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ABSTRACT The design of single-phase differential buck inverters has two important considerations, including reducing second-order ripple power using decoupling capacitors and increasing inverter performances. Using larger decoupling capacitors will improve the performance of ripple power reduction and efficiency while reducing power density. Such trade-off has not been fully modeled and investigated, leading to the sub-optimal design of inverters. To address that, in this paper, the trade-off among decoupling capacitance, inverter efficiency and power density are investigated through detailed mathematical modeling and sensitivity study. The trade-off of the volume and power loss of essential inverter components, including power switches, inductors and heatsinks, are also studied to facilitate the inverter design. A fast multi-objective design optimization method based on geometric programming is presented to optimize the inverter efficiency and power density. A 1 kW prototype of a Gallium Nitride (GaN) based inverter has been designed based on the proposed method. A hardware prototype of the inverter has been built and tested, which has an efficiency of 98.02% and power density 4.54 kW/dm^3 and matches 99% to the presented multi-objective design method. This validates the accuracy and effectiveness of the presented design approach considering detailed trade-off analysis.

INDEX TERMS Multi-objective design, single-phase differential inverter, power decoupling, efficiency, power density, geometric program.

I. INTRODUCTION

The instantaneous power on the DC-link of single-phase inverters have inherent second-order ripple components that significantly affect the performance of the systems. Conventional solutions to minimize the effects of ripple power is to deploy large electrolytic capacitors at DC-link of inverters [1]. However, the high failure rate of such capacitors utterly threatens the reliability and lifetime of the inverters [2]. Film capacitors can be used instead, which have a much longer lifetime. However, they cannot be used to directly replace electrolytic capacitors due to the reason of their large volume and high cost [3].

Recently, wide band-gap (WBG) power devices such as silicon carbide (SiC) and gallium nitride (GaN) have attracted great attention in the power electronics industries. Using WBG devices, higher switching frequencies can be achieved without compromising the system efficiency compared to silicon (Si) devices [4]. As a result, the size of passive components in the inverters can be reduced considerably. However, the WBG devices cannot help to address the aforementioned problem of DC-link capacitors because such capacitors are sized according to the low-frequency second-order ripples [5], instead of switching-frequency ripples. On the other hand, active power decoupling is a promising method to minimize the

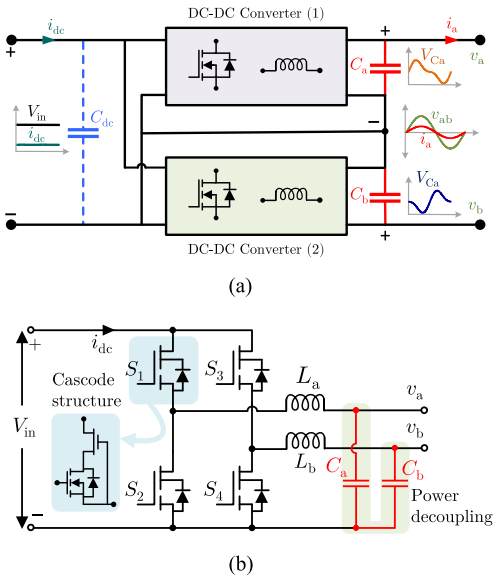


FIGURE 1. (a) Single-phase differential inverter with power decoupling function. (b) Buck-type topology under investigation.

total value of the DC-link capacitance [6]. The main objective of this method is to divert the ripple power to other capacitors, which are smaller and not directly connected to the DC-link. As a result, small-sized and long-lifetime film capacitors can be used [7]. However, this method needs extra active and or passive components, which will inevitably increase the control complexity and volume of the inverters [8], [9].

Compared to many other solutions, the differential inverter can achieve the active power decoupling function without adding extra active or passive components. It has been classified into the buck, boost, or buck-boost inverter, developed of two identical DC/DC converters [10]. The output capacitor of the DC/DC converters is used for the power decoupling function. Fig. 1(a) shows the concept of differential inverter with power decoupling function. In [11], a buck type inverter was used to reduce the ripple from the DC-link using a decoupling control method. It proved that the amplitude of second-order ripple in the DC-link current was reduced by more than seven times. The same inverter was used for grid-connected PV applications by applying a common-mode conducting loop to reduce the leakage current caused by parasitic capacitance and to minimize the second-order pulsating power. It was confirmed that ground leakage current and the pulsating power problems are solved without adding extra active components [12]. In [13], a waveform control-based ripple mitigation method was introduced for a boost type inverter to eliminate the instability in the fuel-cell system. In [14], the waveform control method was extended into a rule-based controller for a boost inverter-based grid-connected battery storage systems. In [15], an energy-based power decoupling control method was introduced for a buck-boost type inverter to mitigate the second-order ripple in the input DC current. As a result, the low-frequency ripple was eliminated, which enables using film capacitors over electrolytic capacitors. In [16], the mismatch of the decoupling capacitors of differential buck inverters was resolved by using a comprehensive common-mode control method. However, the efficiency and power density of the differential inverters are not considered while reducing the size of the decoupling capacitors. In practice, these are the essential parameters which need to be considered to enhance the design.

Existing research focuses on advancing power decoupling methods to decrease the size of the capacitor, hence to further reduce the volume. These methods rely on either improving the control strategy of inverters or adding other supplementary components [7]. However, the use of a smaller decoupling capacitor will sacrifice the efficiency of inverters as the capacitance and efficiency are mutually and inversely coupled [17]. Conversely, a few work contributes to increase the efficiency while the volume of capacitor is less considered [11]. Either way, the design of such inverters will not be optimized unless both the performance parameters–volume and efficiency are considered for the inverter design. Some attempt to achieve both high efficiency and power density by adding extra converter units [18]. Others are focused on the multi-objective design for other types of converters [19], [20].

Despite the significant contributions presented in existing literature, a detailed analysis of the trade-off between the inverters power loss and decoupling capacitance has not been presented. Also, multi-objective design focused on single-phase differential inverters with power decoupling capacitors has yet to be developed. To bridge the gap, this paper introduces the detailed modeling of the trade-off between the inverters power loss and the decoupling capacitor. A multi-objective design approach is proposed for maximizing the efficiency and power density of single-phase inverters. The differential buck inverter is considered an example for this study, shown in Fig. 1(b). The outcome of the design approach can be used for the optimal selection of decoupling capacitors associated with other components, including inductors, heatsinks, and power switches. A mathematical model of power loss and volume of each component within the inverter are developed to achieve this. The relation between the efficiency and power density of the decoupling capacitor is analyzed in-depth. GaN field-effect transistors (FETs) are adopted for the design approach to ensure the high efficiency and high power density of the designed inverters.

This paper is organized as follows. In Section II, the mathematical model of power loss and volume of each component within the inverter is derived by considering the second-order ripple current. In Section III, the trade-offs among the decoupling capacitance, power loss and power density are addressed in-depth using the mathematical models. Section IV, a multi-objective optimization method based on geometric programming (GP) is introduced to optimize the efficiency and power density. The proposed design approach is based on the detailed modeling of power loss and volume by considering the dominant design parameters of the inverter. In this paper, the dominant design parameters are selected based on

the direct approach [21]. Firstly, the power loss and volume model equations of all the components were derived. Then, the tunable parameters in the equations are identified. Next, the values of the parameters are adjusted within the acceptable range, and the parameters that have a higher impact on the power loss and volume are identified. Based on this approach, the design variables, including the switching frequency, the inductor ripple, the switch area, and the junction temperature, are selected. Using these parameters, the power loss and volume are calculated. In Section V, the outcome of the design approach is used for the optimal selection of decoupling capacitors associated with other components, including inductors, heatsinks, and power switches. The presented design approach has been practically used to develop a GaN-based 1 kW prototype. The obtained efficiency and power density are high (98.02% and 4.54kW/dm^3), and the results are 99% matches to the proposed multi-objective optimization method, which in turn shows the effectiveness of the design method.

II. MODELING OF POWER LOSS AND VOLUME OF THE INVERTER

In this section, detailed modeling of the differential buck inverter topology is presented. The mathematical model is essential to explore the efficiency and power density of the inverters. In general, the models of power electronics components included different design variables. For example, the switching loss depends on the switching frequency design variable. This component-level model will only give the power loss of an individual component. The total losses can be calculated by aggregating the individual component-level losses. However, this will reduce the efficacy of the modeling approach. Therefore, an accurate system-level modeling approach is required, which needs to consider all of the design variables.

In this paper, the detailed system-level power loss and volume models of each component are derived based on the active power decoupling approach. From this, the efficiency and power density are further determined. The design variables including switching frequency f_{sw}, the inductor ripple $\triangle i_L$, the switch area A_{sw}, and the junction temperature $\triangle T_j$ are used to calculate the power loss and volume. With this paper, four major components are considered, including the power GaN FETs, inductors, capacitors, and heat sinks. The modeling approch is following broadly the methodology of [19]–[22].

A. POWER GaN FETs

The power loss models of the GaN FETs are derived based on the on-state resistance $R_{DS,on}$, the output capacitance C_{oss}, and the thermal junction-to-case resistance $R_{\theta JC}$ of the switches. These variables are scaled by their reference values with respect to the area of the switch. The switching losses of the inverter are the sum of the turn-on and turn-off loss of all the switches. The switching losses of the higher side switch $P_{S_{H,sw}}(H = 1, 3)$ (see Fig. 1) are obtained as,

$$P_{S_{H,sw}} = \frac{V_{in} f_{sw}}{2} \left\{ \left(I_{out} \sin(\omega t) + i_{comp} - \frac{\triangle i_{L_a}}{2} \right) (t_{CR} + t_{VF}) + \left(I_{out} \sin(\omega t) + i_{comp} + \frac{\triangle i_{L_a}}{2} \right) (t_{VR} + t_{CF}) \right\} \quad (1)$$

where, i_{comp} is the second-order current component and $\triangle i_{L_a}$ is the inductor current ripple. t_{CR} and t_{CF} are the rise and fall times for the current in the switch. t_{VR} and t_{VF} are the rise and fall times for the voltage in the switch.

The switching loss of the lower side switches S_2 and S_4 are lower because it is based on the diode voltage drop V_{SD}. The switching losses of the lower side switch $P_{S_{L,sw}}(L = 2, 4)$ can be derived as,

$$P_{S_{L,sw}} = \frac{V_{SD} f_{sw}}{2} \left\{ \left(I_{out} \sin(\omega t) + i_{comp} + \frac{\triangle i_{L_a}}{2} \right) (t_{CR} + t_{VF}) + \left(I_{out} \sin(\omega t) + i_{comp} - \frac{\triangle i_{L_a}}{2} \right) (t_{VR} + t_{CF}) \right\} \quad (2)$$

From (1) and (2), the total switching losses $P_{tot,sw}$ of the inverter can be calculated as the sum of $P_{S_{H,sw}}$ and $P_{S_{L,sw}}$.

The conduction loss depends on the RMS current flowing through the switch $I_{RMS,sw}$, the on-state resistance $R_{DS,on}$ and the change in junction temperature $\triangle T_j$. It will be varied according to the duty cycle of the switches $S_1 - S_4$. After applying the mathematical simplifications, the total conduction loss $P_{tot,cond}$ can be written as,

$$P_{tot,cond} = \left(\frac{R^*_{DS,on} A^*_{sw}}{A_{sw}} \right) (1 + \triangle T_j) \left\{ \left(I^2_{out} \sin^2(\omega t) + i^2_{comp} + \frac{\triangle i^2_{L_a}}{12} \right) + \left(I^2_{out} \sin^2(\omega t + \pi) + i^2_{comp} + \frac{\triangle i^2_{L_b}}{12} \right) \right\} \quad (3)$$

The power losses of the output capacitance C_{oss}, depend on the input voltage and the switching frequency, which can be expressed as,

$$P_{tot,C_{oss}} = 2 \left(\frac{C^*_{oss} A_{sw}}{A^*_{sw}} \right) V^2_{in} f_{sw} \quad (4)$$

The reverse recovery loss of the lower side switches are not negligible for cascode devices. The total reverse recovery loss $P_{tot,rr}$ is calculated as,

$$P_{tot,rr} = 2 \left(\frac{Q^*_{rr} A_{sw}}{A^*_{sw}} \right) V_{in} f_{sw} \quad (5)$$

The gate losses depend on the switching frequency, the gate-source voltage V_{GS} and the gate charge Q_g. The total gate loss of four switches $P_{tot,g}$ is calculated as,

$$P_{tot,g} = 4\left(\frac{Q_g^* A_{sw}}{A_{sw}^*}\right) V_{GS} f_{sw} \tag{6}$$

The reference values of $R^*_{DS,on}$, A^*_{sw}, C^*_{oss}, Q^*_{rr}, and Q^*_g can be found in the datasheets of GaN FETs. In cascode GaN FETs, the body diode of the lower side switches are incurred by the conduction loss during the reverse recovery time t_{rr} [22]. The total power loss $P_{tot,bd}$ of the body diodes can be written as,

$$P_{tot,bd} = 2V_{SD} f_{sw} t_{rr} \left(I_{out}\left(\sin(\omega t) + \sin(\omega t + \pi)\right) + 2i_{comp}\right) \tag{7}$$

The volume of the switches can be calculated as,

$$vol_{sw} = 4h_{sw}A_{sw} \tag{8}$$

where, h_{sw} is the height of the switch package.

B. OUTPUT INDUCTORS

The inductor power loss consists of the core loss, the AC and DC resistance losses, which can be expressed [23], [24] as,

$$P_{ind} = a_{L1} f_{sw}^{\alpha} \triangle i_L^{\beta} + a_{L2} f_{sw} \triangle i_L^{\gamma} + a_{L3} I_{out}^2 \triangle i_L^{\lambda} \tag{9}$$

where, a_{L1}, α, and β are the Steinmetz coefficients; a_{L2} and a_{L3} are the constants, which are used to approximate the values of DC winding resistance; γ and λ are the real values used to reduce the non-linearity.

The approximated inductor volume is calculated as,

$$vol_{ind} = a_{L4} L\left(I_{peak,a}^2 + I_{peak,b}^2\right) + a_{L5} L\left(I_{peak,a} + I_{peak,b}\right) + a_{L6}\left(I_{peak,a} + I_{peak,b}\right) \tag{10}$$

$$I_{peak,a} = I_{out}\sin(\omega t) + i_{comp} + \frac{\triangle i_{L_a}}{2} \tag{11}$$

$$mI_{peak,b} = I_{out}\sin(\omega t + \pi) + i_{comp} + \frac{\triangle i_{L_b}}{2} \tag{12}$$

where, a_{L4}, a_{L5}, and a_{L6} are the polynomial coefficients of the inductor which must be a positive value. L is the inductor value ($L = L_a = L_b$). $I_{peak,a}$ and $I_{peak,b}$ are the peak current of the inductors.

The inductor selection is associated with the value of the inductor and the maximum output current. The required value of the inductor is calculated by the following expression,

$$L = \frac{rV_{in}}{\triangle i_L f_{sw}} \tag{13}$$

where, r is the ripple coefficient of the inductor and it can be selected between 20% to 35% of the maximum output current. The current flows through the inductor contains switching ripple due to the switches ON and OFF. In (13), the ripple current reduces by increasing the value of the inductor. But, the preferred solution of the inductor is the lower value and smaller size. In order to decrease the inductance value, the switching frequency needs to be optimized accordingly.

C. POWER DECOUPLING CAPACITORS

The power loss of the capacitor is calculated as,

$$P_{cap} = \frac{I_{RMS,C}^2 \tan\delta}{2\pi f_{2\omega} C} \tag{14}$$

where, $I_{RMS,C}$ is the RMS current flow through the capacitor, $\tan\delta$ is the loss factor, $f_{2\omega}$ is the frequency of second-order ripple power and C is the value of the capacitance.

In practical design, the capacitance volume varied by different manufacturers; for that reason, an approximated model is used. The total box volume of the capacitors vol_{cap} are calculated as,

$$vol_{cap} = a_{C1} C\left(V_{C_a}^2 + V_{C_b}^2\right) + a_{C2} C\left(V_{C_a} + V_{C_b}\right) + a_{C3}\left(V_{C_a} + V_{C_b}\right) \tag{15}$$

where, a_{C1}, a_{C2}, and a_{C3} are the polynomial coefficients of the capacitor which must be a positive value. C is the output capacitor ($C = C_a = C_b$). $V_{C_a}$and V_{C_b} are the voltage across the output capacitors. The capacitor voltages V_{C_a} and V_{C_b} are represented as,

$$V_{C_a} = \frac{V_{out}}{2}\left(1 + \sin(\omega t)\right) + v_{comp} \tag{16}$$

$$V_{C_b} = \frac{V_{out}}{2}\left(1 + \sin(\omega t + \pi)\right) + v_{comp} \tag{17}$$

The output capacitor selection is the biggest challenge which have a trade-offs between the second-order ripple, power loss and volume. The details of the output capacitor selection is discussed in Section 3.

D. HEAT SINKS

The volume of the heat sink is calculated [25] as,

$$vol_{heat\ sink} = \frac{V_{\theta SA}}{P_D}\left(\triangle T_j - P_D\left(R_{\theta JC} + R_{\theta CS}\right)\right) \tag{18}$$

where, $V_{\theta SA}$ is the volumetric resistance, P_D is the power dissipated by the GaN FETs, $\triangle T_j$ is the temperature difference between the junction and the ambient, $R_{\theta JC}$ is the thermal resistance from junction to case of the semiconductor, and $R_{\theta CS}$ is the thermal resistance from case to the mounting surface of the semiconductor. The values of $R_{\theta JC}$ and $R_{\theta CS}$ are provided by the manufacturer. In this paper, the value of $R_{\theta JC}$ is considered as one of the design parameters of the heat sink, since it is attached to the heat source. Apart from this, several other parameters need to be considered for selecting heat sinks, such as thermal resistance, volumetric resistance, and fin spacing. The extruded radial fins type heat sink is the better choice for the given design, so that two switches can be mounted in one heat sink.

III. TRADE-OFFS AMONG THE DECOUPLING CAPACITANCE, POWER LOSS AND POWER DENSITY

In this section, the trade-off between the decoupling capacitance and the total power losses of the inverter is analyzed in detail. The impact of capacitance on the switching and conduction loss of GaN FETs are reflected by (1)–(3). Capacitor power loss is calculated by (14). The capacitance will also influence the power loss of inductor by affecting the value of I_{out} in (9). It is then vital to derive the expression of the total capacitance as follows.

The decoupling capacitors reduce the second-order ripples at the DC-link by buffering the second-order power. Hence, the second-order component is processed by the decoupling capacitors. The power balance equation of the decoupling capacitor can be written as,

$$2C\frac{dV_C^2}{dt} = \frac{V_{\text{out}}I_{\text{out}}}{2}\cos(2\omega t) \tag{19}$$

where, V_{out} and I_{out} are the output voltage and current, 2ω is the frequency of second-order ripple. Then, the capacitor voltage can be written as,

$$V_C = \frac{V_{\text{out}}}{2}(1+\cos(\omega t)) + v_{\text{comp}} \tag{20}$$

where, v_{comp} is the second-order ripple compensation voltage. Integrating (19) and substituting V_C into (19) will give the expression of the total required capacitance as,

$$C = \frac{V_{\text{out}}I_{\text{out}}\sin(2\omega t)}{8\omega\left(\frac{V_{\text{out}}}{2}(1+\cos(\omega t)) + v_{\text{comp}}\right)^2} \tag{21}$$

Simplifying the above equation with respect to the peak value is yielded the minimum required capacitance,

$$C_{\text{min}} = \frac{V_{\text{out}}I_{\text{out}}}{4\omega\left(V_{\text{out}} + v_{\text{comp}}\right)^2} \tag{22}$$

From (22), the minimum required capacitance C_{min} is calculated to be 28 μF. A sensitivity analysis is performed to vary the total capacitance from its minimum required value 28 μF (Case I) to 6.6 times larger 185 μF (Case II) to investigate its impact on the power loss of inverter. The results are given in Fig. 2. It can be observed that the power loss reduces nonlinearly with the increase of capacitance. Case I is where the capacitance is minimized and hence results in a large amplitude of second-order ripple in the decoupling capacitors. Such second-order ripple raises the total power loss to 23 W, Fig. 2. Conversely, Case II is where the capacitance is maximized and the total power loss is reduced to only 13.8 W. This is because the large decoupling capacitor buffers the second-order ripple current, which minimizes the effects on the circulating second-order current. However, arguably such a big capacitor is not a good option as the power density of the inverter will be reduced to 2.07 kW/dm^3. Moreover, the amount of change in power loss is less when the capacitance becomes larger. For instance, power loss reduces from 23 W to 17 W when the capacitance increases from 28 μF to 55 μF. The power density is changed from 5.84 kW/dm^3 to 4.61 kW/dm^3. However, the power loss is reduced from 17 W to 13.8 W only when the capacitance increases from 55 μF to 185 μF. A suitable capacitance then would be in the range of 40 μF to 55 μF where the average rate of change in power loss per capacitance is the highest, around 0.22 W/μF; while above 55 μF, the average rate is 10 times less, around 0.025 W/μF. Also, a higher power density can be achieved.

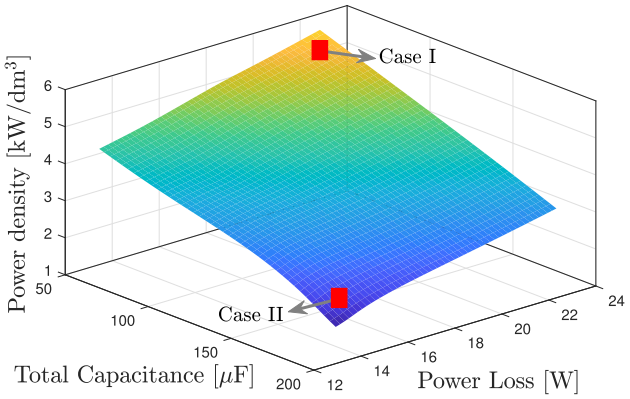


FIGURE 2. Relationship between total capacitance vs. inverter power loss vs. power density.

To further acquire precisely optimized results considering both the total power loss and volume of the inverter, a multi-objective design method needs to be developed. The analysis of the trade-off between power loss and capacitance are integrated as part of the multi-objective design method.

IV. MULTI-OBJECTIVE DESIGN USING GP

GP is one of the mathematical methods, used to solve optimization problems. The advantages of this method are that the global optimum solution always be achievable, and the mathematical operations do not exceed the dimension of the problem. It has been applied to optimize the topology and components of the power electronics converters [26]. This paper uses GP to find the global minimum of power loss and volume for the set of design inputs.

An overview of the proposed multi-objective design approach is presented in Fig. 3. GP formulation can be solved as a convex problem via a logarithmic transformation. The multi-objective design approach is formulated using the monomial and posynomial functions [27]. The objective function of GP can be expressed as follow,

$$\text{minimize}\quad f_i(y) = \sum_{q=1}^{n}\left(a_{iq}y_1^{m_{iq1}}y_2^{m_{iq2}}\ldots y_{\text{n}}^{m_{iqn}}\right)$$

subject to,

$$h_j(y) = \sum_{q=1}^{n}\left(a_{jq}y_1^{m_{jq1}}y_2^{m_{jq2}}\ldots y_{\text{n}}^{m_{jqn}}\right) = 1 \quad j = 1,\ldots,p$$

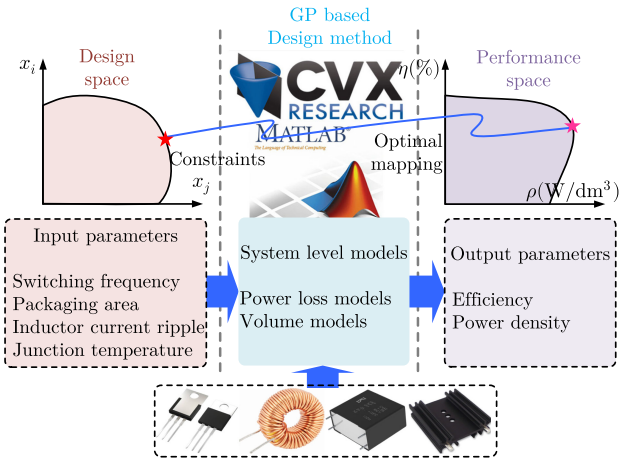


FIGURE 3. Overview of multi-objective design using GP.

$$g_k(y) = \sum_{q=1}^{n} \left(a_{kq} y_1^{m_{kq1}} y_2^{m_{kq2}} \ldots y_n^{m_{kqn}} \right) \leq 1 \quad k = 1, \ldots, r \tag{23}$$

where $y = (y_1, y_2, \ldots y_n)$ is the vector of the design variables, $f_i(y)$ is the objective function to be minimized, and $h_j(y)$ and $g_k(y)$ are the equality and inequality constraints, respectively, that must be satisfied by the solution. Using logarithmic function, $f_i(y)$, $h_j(y)$ and $g_k(y)$ can be transformed into convex functions. The input variables y must be a non-zero real positive numbers and, the coefficients (a_i, a_j, a_k), and exponents (m_i, m_j, m_k) must be a real number.

To formulate the GP for the multi-objective design approach, the total power loss $P_{\text{tot,loss}}$ and volume vol_{tot} are formulated as,

$$\begin{aligned} P_{\text{tot,loss}} &= P_{\text{tot,sw}} + P_{\text{tot,cond}} + P_{\text{tot,C}_{\text{oss}}} + P_{\text{tot,rr}} \\ &\quad + P_{\text{tot,g}} + P_{\text{tot,bd}} + P_{\text{ind}} + P_{\text{cap}} \end{aligned} \tag{24}$$

$$vol_{\text{tot}} = vol_{\text{sw}} + vol_{\text{ind}} + vol_{\text{cap}} + vol_{\text{heat sink}} \tag{25}$$

Using (24) and (25), the objective function and inequality constraints can be obtained as,

$$\begin{aligned} &\text{minimise} \quad f\left(P_{\text{tot,loss}}, vol_{\text{tot}}\right) \\ &\text{subject to} \quad f_{\text{sw,min}} \leq f_{\text{sw}} \leq f_{\text{sw,max}} \\ &\qquad A_{\text{sw,min}} \leq A_{\text{sw}} \leq A_{\text{sw,max}} \\ &\qquad \triangle i_{\text{L,min}} \leq \triangle i_{\text{L}} \leq \triangle i_{\text{L,max}} \\ &\qquad \triangle T_{\text{j,min}} \leq \triangle T_{\text{j}} \leq \triangle T_{\text{j,max}} \end{aligned} \tag{26}$$

From (26), the optimal value of the power loss and volume of the inverters can be determined at the end of iterations. Then, the optimized efficiency and power density of the design is calculated. The outcome of the multi-objective design is the Pareto-front showing the optimized efficiency and power density of the design problem. Also, the selection of components will be known to achieve the optimized solutions.

TABLE 1 Implementation Parameters of the Inverter

Parameter	Value
Input voltage V_{in}	450 V
RMS output voltage v_{ab}	230 V
RMS output current i_{a}	4.35 A
Output capacitor ripple $\triangle v_{\text{c}}$	0.5 V
Ambient temperature $T_{\text{amb.}}$	25°C
Maximum junction temp. $T_{\text{j,max}}$	50°C

TABLE 2 Design Constraints of the Inverter

Design variable	Min. value	Max. value
Switching frequency f_{sw}	10 kHz	200 kHz
Current ripple $\triangle i_{\text{L}}$	$0.1 I_{\text{out,max}}$	$0.45 I_{\text{out,max}}$
Switch area A_{sw}	$0.94 A^*_{\text{sw}}$	$1.07 A^*_{\text{sw}}$
Change in temperature $\triangle T_{\text{j}}$	1°C	25°C

V. RESULTS AND DISCUSSIONS

The proposed design approach was implemented in MATLAB/Simulink and examined with a 1 kW GaN-based inverter. The implementation parameters such as input, output voltage/current and temperature data are given in Table 1. The performance of the inverter was examined in terms of efficiency and power density. The minimum and maximum values of the design variables used for the multi-objective design are given in Table 2. The values of design variables are selected as per the industrial design standards. Four 900 V TP90H180PS GaN FETs were used to build the prototype and the device is manufactured by Transphorm. The simulation of the GaN FETs performed using the SPICE model, and the device data' s are obtained from the datasheet [28]. Two P11T60 series of high current toroid type fixed inductors were used which were designed by MPS Industries. Considering the particular type of inductor does not limit the performance of the proposed design method [23]. Also, the proposed method can be adopted quickly based on the need of any other type of inductor. Two MKP1848 C series of polypropylene film capacitors are used from the Vishay BC Components. The values of the maximum output current $I_{\text{out,max}}$ and reference switching area A^*_{sw} are 6.15 A and 45.6 mm^2. The values of the inductor is $L = 390\,\mu\text{H}$, capacitor is $C = 48\,\mu\text{F}$ and switching frequency is $f_{\text{sw}} = 100\,\text{kHz}$. These are selected according to the outcome of the multi-objective design approach. The coefficients of the inductor and capacitor volume models are give Table 3.

A. PERFORMANCE EVALUATION

The Pareto-front performance of efficiency and power density $(\eta - \rho)$ of the power inverter is generated by the multi-objective design and is given in Fig. 4(a). In comparison, a numerical model is also built to identify the optimal design boundary by scanning all the achievable combinations of efficiency and power density of the inverter. The optimized solutions obtained by both methods are identical. However, the GP based multi-objective design is much faster, taking

TABLE 3 Coefficients of Inductor and Capacitor Volume

$a_{L4}\left(\frac{cm^3}{mH.A^2}\right)$	$a_{L5}\left(\frac{cm^3}{mH.A}\right)$	$a_{L6}\left(\frac{cm^3}{A}\right)$	$a_{C1}\left(\frac{cm^3}{\mu F.V^2}\right)$	$a_{C2}\left(\frac{cm^3}{\mu F.V}\right)$	$a_{C3}\left(\frac{cm^3}{V}\right)$
3.2	7.8	1.09	0.011	0.06	0.03

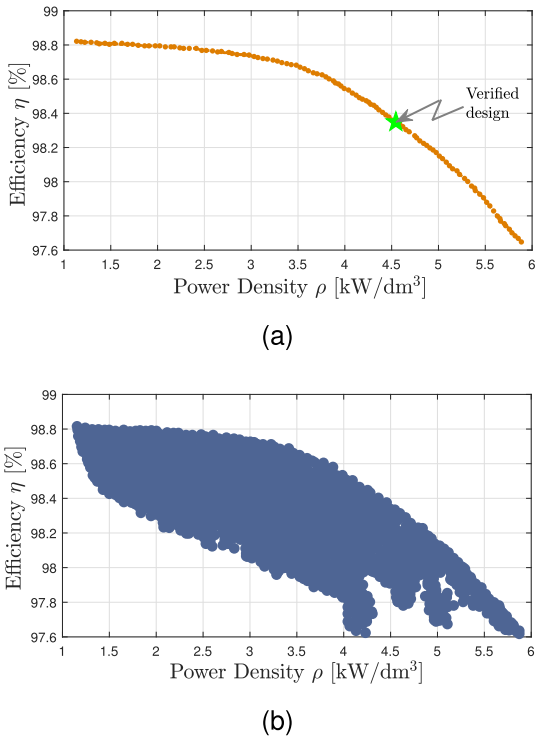


FIGURE 4. Efficiency vs. Power density: (a) Numerical model. (b) Geometric program.

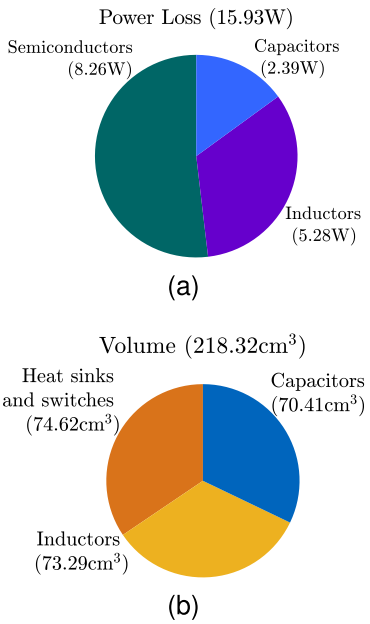


FIGURE 5. (a) Power loss. (b) Volume.

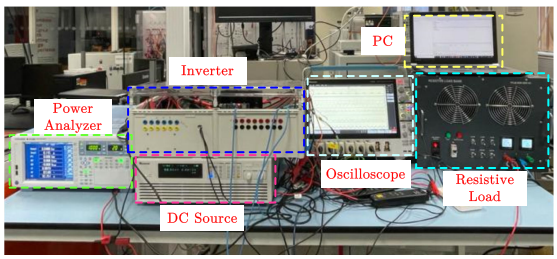


FIGURE 6. Experimental setup.

16 mins, as it has less computational burden and generates only optimized solutions. The numerical model-based method takes 45 mins to scan all combinations, including the optimized solutions and also the suboptimal solutions, as shown in Fig. 4(b), which takes a longer computational time to validate the suboptimal designs. However, the proposed GP-based design scans only the optimal design subject to the constraints and conditions given in equation (23)–(26). Therefore, the proposed method does not compute the suboptimal designs, which cannot provide a feasible solution for the given design problems. Hence, the overall computational time was reduced compared to the numerical model. The computational time is calculated by the processor Intel(R) Core(TM) i7-6500 U CPU @ 2.50 GHz and the installed RAM 16.0 GB.

The next step is to choose one design based on the Pareto-front performance and hence to validate the proposed method. The selected design efficiency and power density are 98.4% and 4.6 kW/dm^3, which are favoured by the current PV inverter market. For the corresponding design, the power loss and volume are obtained as 15.93 W and 218.32 cm^3. The break-down power loss and volume of each component are given in Fig. 5. With the total power losses, semiconductors contributed 51.85%, inductors contributed 33.15%, and capacitors contributed 15%. Likewise, with the total volume, heat sinks and switches occupied 34.18%, inductors occupied 33.57%, and capacitors occupied 32.25%.

B. EXPERIMENTAL VERIFICATION

Fig. 6 shows the experimental setup. The performances of the inverter was tested using the power decoupling control scheme presented in Fig. 7. $G_{v_{ab}}(s)$, $G_{i_{La}}(s)$ and $G_{i_{dc}}(s)$ are the output voltage controller, inductor current controller and second-order ripple controller of the inverter. The voltage controller consists of the fundamental component, the odd and even harmonics compensators. The current controller includes the fundamental component and the odd harmonic compensators. The second-order ripple controller consists of the even harmonic compensators to cancel the even harmonics on the DC-link current. These controllers are designed using the

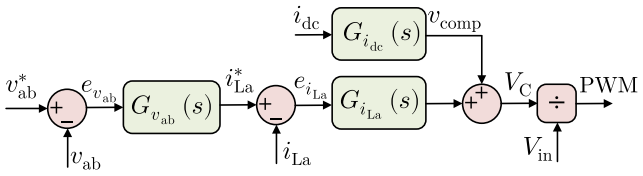


FIGURE 7. Control scheme of the inverter.

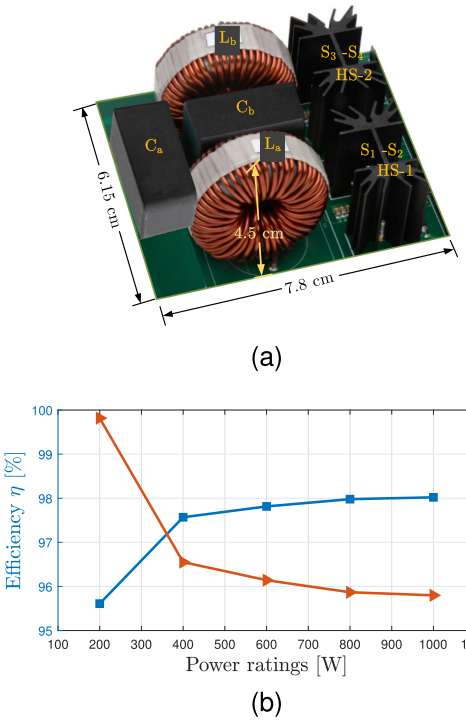


FIGURE 8. (a) Hardware prototype. (b) Efficiency and power loss.

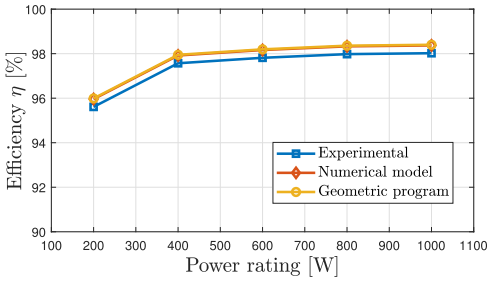


FIGURE 9. Comparisons of efficiency curve.

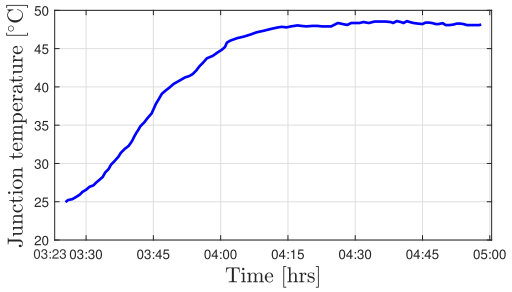


FIGURE 10. Junction temperature of the devices.

Proportional-Resonant (PR) controller. The detailed design of the PR controller can be found in [11], [12], which is not repeated in this paper.

In verification, the prototype of the inverter has been built using the same components obtained by the selected design. Fig. 8(a) shows the hardware prototype of the inverter. The prototype was examined at different output power levels to obtain the response of efficiency vs output power and power loss vs output power, Fig. 8(b). Yokogawa WT1806E precision power analyzer was used to measure the efficiency. It can be observed that the maximum efficiency of the prototype is 98.02%. The power density is obtained as 4.54kW/dm^3 from the volume of the inverter, which is given in Fig. 8(a). To calculate the power density more precisely [9] and [29], Fig. 8(a) does not contain the micro-controller, gate driver and power supply. The reason was that the micro-controller and power supply modules does not have any direct impact with the design parameters. Hence, the volume of these components is always constant. Therefore, the efficiency and power density of the prototype matches to the results of the proposed design approach. Then, the efficiency of the experimental, numerical model and geometric program are compared with each other. Fig. 9 shows the comparisons of the efficiency curve. The efficiency of 98.4% of the proposed design matches with the traditional numerical model. Compared to the experimental efficiency, the error of efficiency obtained from both is only 0.38%. The small error in the efficiency is caused by the PCB, micro-controller, gate driver, power supply and other component losses. The difference in the power density is obtained only 0.06kW/dm^3. Concluding from the above, the accuracy of the proposed design is very high, and its computation speed is much faster than numerical modeling.

The junction temperature of GaN FETs is measured using a TC-08 data logger. The data logger was connected to the computer, and the junction temperatures are monitored. Fig. 10 shows the junction temperature of the devices logged for 70 minutes. It was observed that the steady-state temperature of the device is 48 °C, which is within the range of the change in junction temperature design limits.

Then, the power decoupling capability of the proposed design is verified with and without using the second-order ripple controller. Fig. 11 shows the experimental results of DC-link voltage V_{dc}, DC-link current i_{dc}, output voltage v_{ab}, output current i_a, and decoupling capacitor voltages V_{Ca}, V_{Cb} without second-order ripple controller. Fig. 12 shows the experimental results of DC-link voltage V_{dc}, DC-link current i_{dc}, output voltage v_{ab}, output current i_a, and decoupling capacitor voltages V_{Ca}, V_{Cb} with second-order ripple controller. The ripple elimination capability of the proposed prototype is quantified using the fast fourier transform (FFT) approach. FFTs of DC-link current with and without using the ripple controller is given in Fig. 13(a). From this, the amplitude of second-order ripple in the DC-link current is 2.25 A, which is

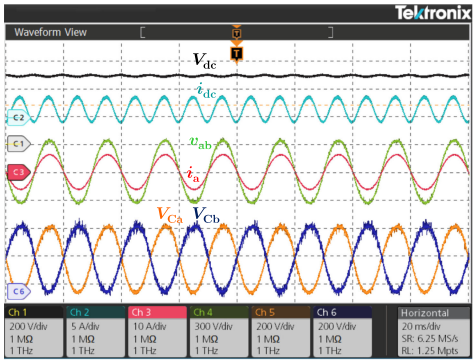


FIGURE 11. Steady-state waveforms at 1kW without second-order ripple controller (V_{dc}, V_{Ca}, V_{Cb}: 200 V/div, i_{dc}: 5 A/div, i_a: 10 A/div, v_{ab}:300 V/div).

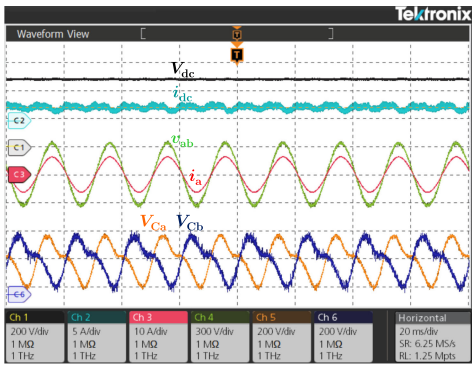
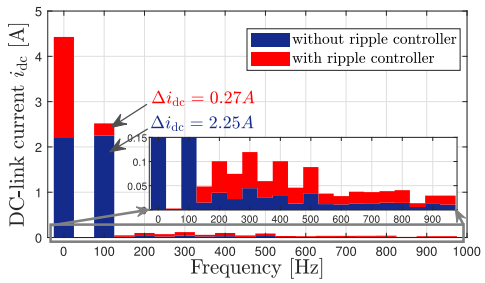
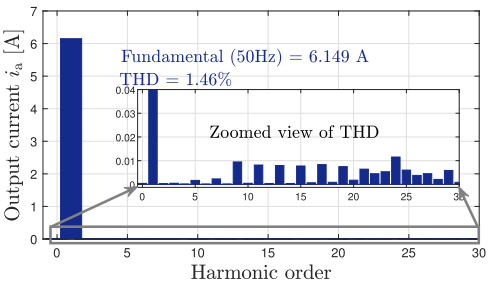


FIGURE 12. Steady-state waveforms at 1 kW with second-order ripple controller (V_{dc}, V_{Ca}, V_{Cb}: 200 V/div, i_{dc}: 5 A/div, i_a: 10 A/div, v_{ab}:300 V/div).



(a)



(b)

FIGURE 13. FFTs of (a) DC-link current with and without second-order ripple controller and (b) output current.

reduced to 0.27 A after using the ripple controller. The residual effects of other order ripple components are not affected the DC-link current after enabling the ripple controller, which can be observed in the zoomed view of Fig. 13(a). Also, THD of the output current is obtained as 1.46%, which is given in Fig. 13(b). The magnitude of other harmonics order is reduced significantly, which is not visible in the figure. The reduction can be visualized in the zoomed view of Fig. 13(b). The FFT results are ensured that the prototype is performed well against the second-order ripple without affecting the output current.

VI. CONCLUSION

This paper investigates the trade-offs between the decoupling capacitor, power loss, and power density of single-phase differential buck inverters. A multi-objective design approach has been proposed to optimize the efficiency, and power density of the inverters. The approach was developed based on detailed mathematical modeling of each component within the inverter. A sensitive analysis was given to select the optimum value of decoupling capacitors. The Pareto-front curve of efficiency versus power density was given for different design requirements, which helps to analyze the trade-offs among the performance measures. This allows the inverter designers to quickly identify the optimum design parameters without compromising much of the inverter total power loss or volume. Compared to the numerical model, the proposed design approach is more effective when the computational complexity, and convergence are concerned. Also, the error of efficiency, and power density obtained from both is only 0.38%, and 0.06kW/dm^3. The experimental results are matched 99% to the proposed multi-objective optimization method. The computational time of the proposed approach is 64.4% faster than the numerical model. Moreover, the second-order ripple in the DC-link current was reduced more than eight times. Employing the proposed design technique, inverter designers can quickly, and accurately draw up the overall optimum system design by balancing trade-offs between efficiency and power density.

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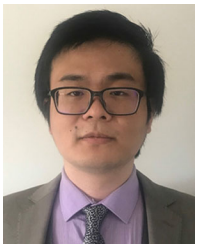

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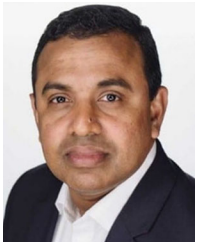

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