Improved Grid Impedance Compensation for Phase-Locked Loop to Stabilize the Very-Weak-Grid Connection of VSIs

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***Abstract*—Voltage source inverters (VSIs) with vector control based on phase-locked loop (PLL) suffer instability when connecting to a very weak AC grid (short circuit ratio (SCR)<1.3). The conventional inductive grid impedance compensation for the PLL by virtually reducing the grid impedance can stabilize this connection. However, the analysis in this paper indicates that its stabilization effectiveness is sensitive to grid impedance variance and, indeed, overcompensation causes the PLL instability. Therefore, in this paper, an improved grid impedance compensation for the PLL is proposed to achieve the same stabilization for very-weak-grid connection and possess a good tolerance of grid impedance variance and overcompensation. A comprehensive small-signal model of the VSI using the proposed PLL's grid impedance compensation is derived for stability analysis and parameter design. The time-domain simulation for this VSI is built to validate the stability analysis. Comparison studies for both proposed and conventional PLL's grid impedance compensation are conducted including the stability effectiveness, VSI performance and grid impedance variance.**

***Index Terms*—PLL-based inverters, vector control, weak grids, stability analysis.**

I. Introduction

VOLTAGE source inverters (VSIs) with PLL-based vector control are widely used for renewable energy integration. Those inverters locating far from the AC grid risk instability due to weak-grid connection [1], which is defined as short circuit ratio (SCR)<3 [2]. Oscillations caused by wind farm inverters connecting to weak grids have been observed in many regional grids [3], such as Texa 4 Hz oscillations, West China 30 Hz oscillations and U.K. 8-9 Hz oscillations. This oscillation can further induce the torsional interaction with synchronization generators [4].

After extensive analysis for this weak-grid connection, it is found that PLL is critical to this VSI instability [5], especially interacting with high grid inductance. Besides, highly-coupled outer loop control [6] and fast-response inner loop control [7] could also cause the instability.

For stable connection to a mildly weak grid (SCR$\in$ [2 3]), many additional stabilization controls are added in the vector control. PLL dynamic compensation is an effective way, by applying in outer loop [8], inner loop [9] and voltage feedforward [10]. Reshaping the VSI impedance via a q-axis compensation can avoid the negative resistance behaviour with weak grid connection [11]. Based on the LC filter, a virtual inductance [12] is added in the vector control to emulate a LCL filter, which can also stabilize the weak-grid connection. However, for connecting to a weak grid such as SCR<2, these stabilization controls are not further validated.

Moreover, it is found that the VSI suffers a critical stability issue when connecting to a very weak grid (SCR<1.3) with rated power injection [13]. Even a great tuning effort is made for the PLL-based vector control, the rated power injection cannot be stabilized and the maximum injected power at SCR = 1 is around 0.7 p.u. [14].

Therefore, to stabilize the rated power injection when connecting to a very weak grid, many solutions have been proposed for the VSI, which can be categorized into two groups: grid-forming control and improved PLL-based control.

Gird-forming control is proposed based on the power synchronization mechanism to effectively support a very weak grid with voltage and rated power. This Power synchronization mechanism can implemented via P [15] droop control or $\omega - P$ droop control with the virtual swing equation of a synchronous generator [16]. Its ability to connect to a very weak grid is further enhanced via robust control design [17] and the transient stability analysis [18]. Although the power synchronization-controlled VSI works well with a weak grid, voltage conflict presents if a strong grid is connected [19], which may cause the VSI instability and sub-synchronous resonance [20].

PLL-based vector control can be improved via adding additional compensation to allow the very weak grid connection with

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rated power injection. Outer loop compensation is an effective way to achieve the desired connection, many methods have been proposed including outer loop decoupling [6], AC voltage compensation [21]. Power compensation [22] by suppressing voltage impact on outer power loop can also effectively stabilize the very weak grid connection.

However, the above-mentioned methods are designed by using the small-signal dynamics of PLL, which increases the control complexity significantly.

The control complexity and stabilization effectiveness are well balanced by the grid impedance compensation in the PLL [23] [24] for the very-weak-grid connection. Only virtual negative impedance is added within the PLL to equivalently advance the synchronized point and strengthen the grid stiffness. Although [24] claims that virtually reducing the grid impedance with negative resistance and inductance helps to stabilize the VSI, its compensation is mainly inductive which $R : Z_L = 1 : 5.6$. More specifically, [23] only using inductive compensation stabilizes the VSI, which proves that the inductive compensation dominates the stabilization effectiveness.

However, in this paper, it is revealed that this inductive compensation highly relies on the information of grid impedance, leading to low tolerance of the grid impedance variance. Furthermore, if the overcompensation occurs because of grid impedance variance or being overestimated, the PLL is likely to lose stability.

In this paper, an improved grid impedance compensation for the PLL is proposed for avoiding above-mentioned drawbacks and stabilizing the very-weak-grid connection (SCR$<$1.3). Differing from the conventional inductive grid impedance compensation by virtually reducing the grid inductance [23], the proposed grid impedance compensation adopts a different mechanism of virtually increasing the grid resistance. Comparing to the conventional PLL's inductive grid impedance compensation, this proposed grid impedance compensation enables good tolerance of grid impedance variance and avoids the instability caused by the overcompensation.

The paper is outlined as follows: Section II introduces the instability mechanism caused by conventional PLL's inductive grid impedance compensation, and presents the feasibility of proposed PLL's grid impedance compensation via interaction analysis between the VSI and a weak AC grid. Section III presents the design of proposed grid impedance compensation for PLL within the VSI's control system, and a small-signal model of this PLL-based vector-controlled VSI using the proposed compensation is derived for parameter design. Section IV demonstrate comprehensive comparison studies between the conventional and proposed PLL's grid impedance compensation including stabilization effectiveness, overcompensation impact, VSI performance and grid impedance variance.

II. Motivation of Improving PLL's Grid Impedance Compensation

The studied VSI with power control based on the PLL is presented in Fig. 1. Besides the active power control at the outer loop, the voltage magnitude of the grid connection point is regulated at the q axis. Current control is necessarily placed in the inner loop to avoid overcurrent. The grid compensation is added in the PLL to adjust grid impedance value equivalently.

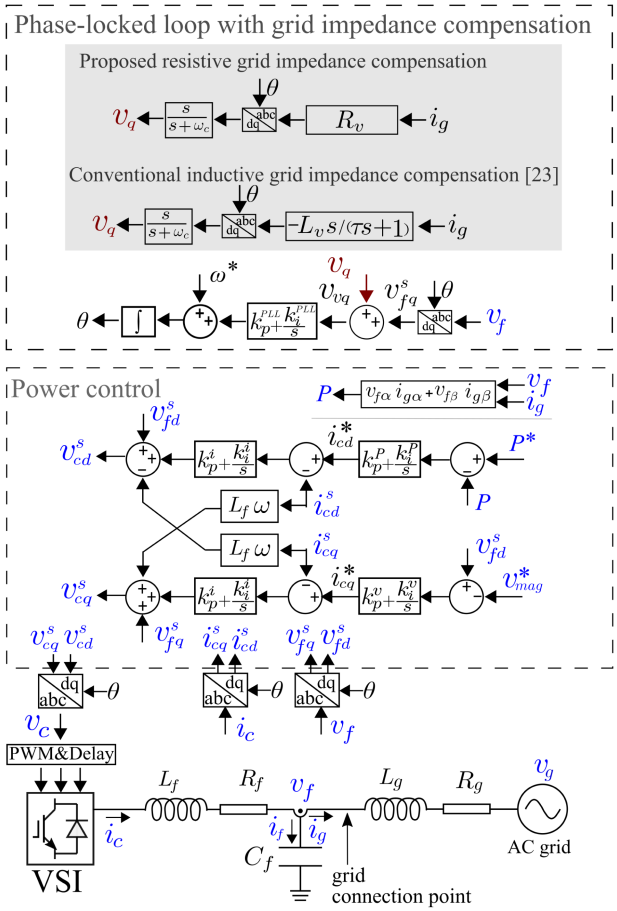

Fig. 1. VSI system: a PLL-based vector-controlled VSI connecting to an AC grid.

Conventional PLL's inductive grid impedance compensation [23] mainly uses virtual negative inductance to equivalently reduce the grid impedance, as shown in Fig. 1. It should be noted that conventional PLL's inductive grid impedance compensation via virtual inductance is a pure derivate, which may cause a significant impact on PLL when i_g varies. Therefore, to avoid this impact, $-L_v s$ is added as $-L_v s/(\tau s+1)$ in the following analysis based on the guidance in [23], where $\tau = 0.01$ ms.

In this section, the motivation of improving grid impedance compensation for the PLL is presented. Firstly, the mechanism of instability caused by the conventional inductive grid impedance compensation is explained and validated in time domain. Secondly, the impedance stability analysis method used in this paper is introduced. Thirdly, the impedance interaction between the VSI and the AC grid is assessed to reveal the stability mechanism by increasing the grid resistance, which is applied for the proposed PLL's grid impedance compensation in the next section.

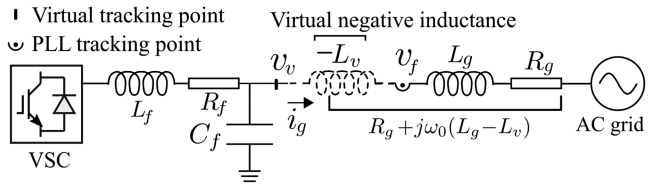

Fig. 2. Equivalent circuit using conventional inductive grid impedance compensation.

A. Instability Caused by Conventional Inductive Grid Impedance Compensation

Conventional inductive grid impedance compensation for PLL was introduced by [23], which can effectively allow the very weak grid connection with rated power injection for VSIs. An equivalent circuit of the VSI system is presented in Fig. 2. By inserting the virtual negative inductance between the tracking point and AC grid, the tracking voltage becomes stiff as the grid impedance is reduced. However, if excessive compensation occurs, this negative inductance compensation will introduce right-plane poles in the PLL, which leads to the PLL instability. This instability mechanism is explained below.

After applying the grid impedance compensation, the tracking voltage becomes v_v as shown in Fig. 2, and the tracking voltage after $abc-dq$ transformation for the PLL is presented below as the small-signal expression:

$$\widetilde{v}_{vq}^{s} = \widetilde{v}_{vq} - V_{vd}\widetilde{\theta} \tag{1}$$

where notation $\widetilde{\ }$ means the small-signal disturbance, capital letter means the steady-state value, such as V_{vd}, superscript s represent the value after the $abc-dq$ transformation.

V_{vd} is calculated as below:

$$V_{vd} = V_{fd} + L_v\omega_0 \underbrace{I_{gq}}_{I_{gq}<0} \tag{2}$$

Based on (1), the relation of PLL presented in Fig. 1 is summarized below:

$$\frac{1}{s}\times\left(k_p^{PLL}+\frac{k_i^{PLL}}{s}\right)\times(\widetilde{v}_{vq}-V_{vd}\widetilde{\theta}) = \widetilde{\theta} \tag{3}$$

Rearranging (3) yields:

$$\frac{k_p^{PLL}s+k_i^{PLL}}{s^2+V_{vd}k_p^{PLL}s+V_{vd}k_i^{PLL}}\widetilde{v}_{vq} = \widetilde{\theta} \tag{4}$$

Compensation ratio for virtual negative inductance is defined as below:

$$L_v = \alpha L_g \tag{5}$$

Excessive compensation, where $\alpha > 1$, may result in $V_{vd} < 0$ in (2). Therefore, positive poles appear in $1/(s^2+V_{vd}k_p^{PLL}s+V_{vd}k_i^{PLL})$, which cause the PLL instability.

A time-domain test for the PLL with negative impedance grid compensation is presented by giving an excessive compensation ratio $\alpha = 1.5$ with SCR $= 2$. The test case is based on the VSI system in Fig. 1, where power control is not included. Its parameters are given in Table I. As shown in Fig. 3, when α is changed to 1.5, the frequency tracked by PLL loses stability.

TABLE I
PARAMETERS OF THE VSI SYSTEM

Symbol	Parameter	Value
	Circuit parameters of VSI system	
S	Power rating	1000 MVA
V_g	rms l-l AC grid voltage	320 kV
L_f	reactor inductance	0.15 p.u.
R_f	reactor resistance	0.05 p.u.
C_f	filter capacitance	0.067 p.u.
v_{mag}^*	d-axis voltage reference	1 p.u.
P^*	active power reference	1 p.u.
T_{del}	control delay and dead time of PWM	5 μs
ω_0	base frequency	2 $\pi\times$ 50
SCR	short-circuit ratio	1 (X_{L_g}:R_g=10)
Z_g ($R_g+jX_{L_g}$)	grid impedance	$0.01+0.995j$ p.u.
	Power control	
ω_c^i	cut-off frequency of closed-loop current control	800 rad/s
k_p^i&k_i^i	PI for current control	0.382&4
k_p^P&k_i^P	PI for power control	$0.1k_p^i$&$0.1k_i^i$
k_p^v&k_i^v	PI for voltage control	$0.1k_p^i$&$0.1k_i^i$
	PLL and grid impedance compensation	
ω_c^{PLL}	phase-locked loop cut-off frequency	210 rad/s
k_p^{PLL}&k_i^{PLL}	PI for PLL	420&44100
ω_c	cut-off frequency of high-pass filter	1000 rad/s
α	gain of virtual inductance	0.8
β	gain of virtual resistance and high-pass filter	0.1
ω_s	cut-off frequency of virtual resistance and high-pass filter	6.28 rad/s
L_v	inserted negative virtual inductance	αL_g
R_v	inserted virtual resistance	< 15

[0] ω_c^i & ω_c^{PLL} are calculated via their PI parameters based on [30] [31]

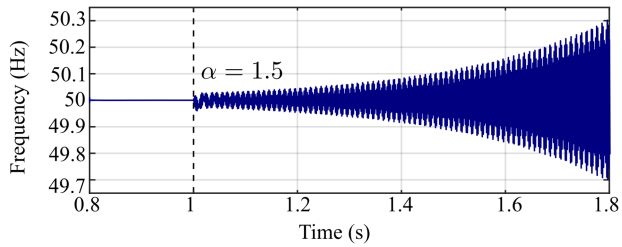

Fig. 3. Frequency tracked by the PLL with conventional inductive grid impedance compensation with SCR $= 2$.

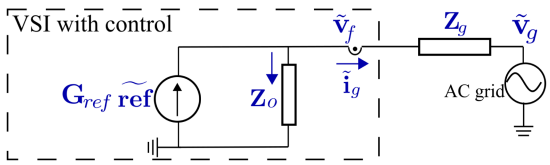

Fig. 4. Equivalent circuit of the VSI system for stability analysis.

B. Stability Analysis Method

To avoid the above-mentioned instability caused by the conventional inductive grid impedance compensation, the impedance stability analysis is introduced for further interaction analysis between the VSI and the ac grid. For impedance stability analysis, a Norton equivalent circuit (Fig. 4) of the VSI system needs to be derived [25] for assessing the stability. $\mathbf{Z}_o$ is the total small-signal impedance of the VSI including the power control (inner and outer loops), PLL, $abc-dq$ transformation, delay of PWM and control system, and LC filter, as shown in Fig. 1. $\mathbf{Z}_g$ is

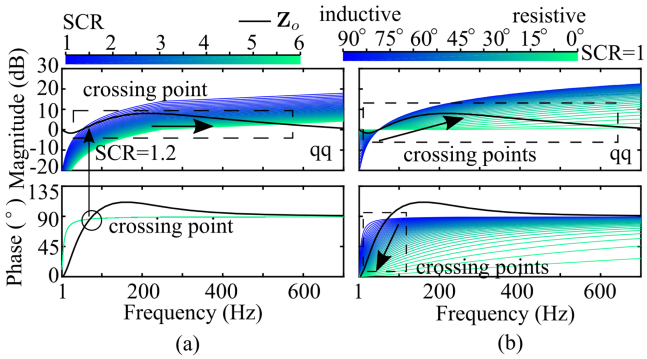

Fig. 5. Impedance interaction analysis of the VSI with various grid impedance. (a) Increasing SCR. (b) Increasing the resistance at SCR = 1.

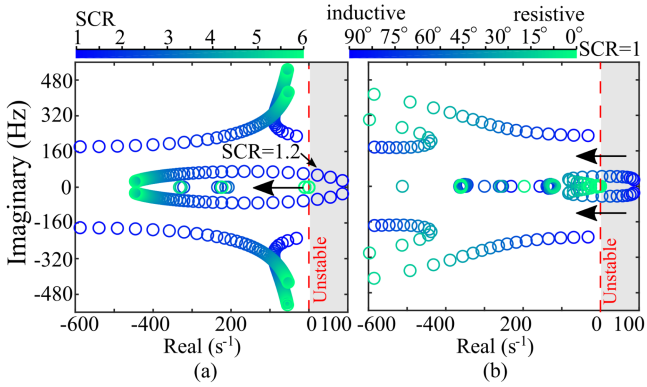

Fig. 6. Stability analysis of the VSI with various grid impedance. (a) Pole locus of increasing SCR. (b) Pole locus of increasing resistance based on inductive grid impedance at SCR = 1.

grid impedance known from R_g and L_g. The following relation is found based on Fig. 4:

$$(\mathbf{Z}_o + \mathbf{Z}_g)\widetilde{\mathbf{i}}_g = \mathbf{Z}_o\mathbf{G}_{ref}\widetilde{\mathbf{ref}} - \widetilde{\mathbf{v}}_g \tag{6}$$

Rearranging (6) with $\mathbf{Y}_o$ yields:

$$\widetilde{\mathbf{i}}_g = (\mathbf{I} + \mathbf{Y}_o\mathbf{Z}_g)^{-1}(\mathbf{G}_{ref}\widetilde{\mathbf{ref}} - \mathbf{Y}_o\widetilde{\mathbf{v}}_g) \tag{7}$$

where $\mathbf{Y}_o$ is the impedance of this VSI and $\mathbf{Y}_o\mathbf{Z}_o = \mathbf{I}$, the impedance ratio matrix is $(\mathbf{I} + \mathbf{Y}_o\mathbf{Z}_g)^{-1}$, and bold capital letter represents the matrix.

This impedance ratio is derived as a 2×2 matrix in dq-frame, which is the key factor [25][26] to analyze the stability of VSI system.

Based on this 2×2 impedance ratio matrix, the determinant-based method [27][28] is applied for stability analysis via only one pole map, as shown below:

$$(\mathbf{I} + \mathbf{Y}_o\mathbf{Z}_g)^{-1} = \mathrm{adj}(\mathbf{I} + \mathbf{Y}_o\mathbf{Z}_g)\underbrace{\det((\mathbf{I} + \mathbf{Y}_o\mathbf{Z}_g)^{-1})}_{\text{factor for stability analysis}} \tag{8}$$

C. Impedance Interaction Analysis Between the VSI and a Weak AC Grid

The small-signal impedance of PLL-based vector-controlled VSI is well derived in [5], which will not be presented in this paper. For a 2×2 VSI impedance $\mathbf{Z}_o$ in dq frame, it is reported that its qq element is critical for the impedance interaction analysis [5]. Therefore, only the qq element is presented. The bode plot of $\mathbf{Z}_o$'s qq element in terms of various SCR are shown in Fig. 5(a). The grid impedance is inductive with $X_{L_g} : Rg = 10 : 1$. When the SCR is low, their magnitude crossing points are close to their phase crossing points, which makes the qq part of $(\mathbf{Z}_o - \mathbf{Z}_g)$ close to 0. This indicates the VSI tends to be unstable. Increasing SCR pushes the magnitude crossing points far from their phase crossing points. Thus, the ultra-small qq element of $(\mathbf{Z}_o - \mathbf{Z}_g)$ is avoided. It is indicated that the VSI gets more stable with high SCRs. The pole map based on determinant-based stability analysis method also proves the findings, as shown in Fig. 6(a). The pole goes into the left plane and move far from $x = 0$ when increasing SCR.

The bode plot of $\mathbf{Z}_o$'s qq element with increasing grid resistance at SCR = 1 is shown in Fig. 5(b). When the grid impedance is highly inductive, the phase of $\mathbf{Z}_o$ and the grid impedance are close at their magnitude crossing point, which results in instability, as shown in Fig. 6(a). With increasing grid resistance, their phases are significantly different at the magnitude crossing points. It is indicated that the VSI is more stable when the grid impedance is mainly resistive. The pole map of the VSI system also proves the finding, as shown in Fig. 6(b). With increasing resistance, the pole goes into the left pane and moves far from $x = 0$.

In sum, if a weak AC grid is connected to a PLL-based vector-controlled VSI, enhancing the grid resistance will effectively stabilize the connection.

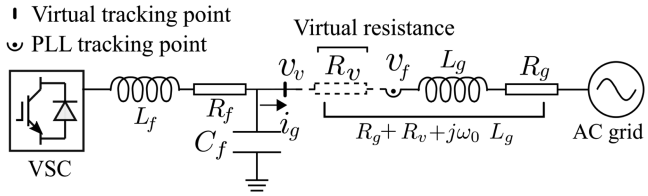

Fig. 7. Equivalent circuit of the proposed grid impedance compensation.

III. Design of Proposed Grid Impedance Compensation for PLL

The previous analysis shows that grid resistance enhancement stabilizes the very-weak-grid connection (SCR=1) with rated power injection. Therefore, differing from the conventional inductive grid impedance compensation by virtually reducing the grid impedance, the proposed grid impedance compensation adopts a different mechanism of virtually increasing the grid resistance, as shown in Fig. 1. The equivalent circuit of the proposed grid impedance compensation is shown in Fig. 7, a virtual resistance is equivalently applied between the tracking point and the AC grid. The total equivalent grid resistance is increased as $R_v + R_g$. Comparing to conventional inductive grid impedance compensation, the virtual negative inductance is replaced, which avoids the instability caused by the overcompensation using virtual negative inductance.

Comparing to the original PLL, an additional v_q is added in the PLL for this compensation. At steady state, it is mandatory for a VSI to synchronize with the grid, which requires v_f being accurately tracked. Therefore, $v_{vq} = v_{fq}$ is requested at steady state even the virtual resistance is applied. To avoid this steady-state error caused by v_q, a high-pass filter $(s/(s+\omega_c))$ is added for the proposed resistive grid impedance compensation, as shown in Fig. 1.

A. Small-Signal Impedance Model of Proposed Grid Impedance Compensation

The small-signal impedance model of PLL-based vector-controlled VSI using resistance grid compensation is derived for its parameter design and stability analysis. This impedance model represents the full VSI system shown in Fig. 1, which includes resistance grid compensation, power control (inner and outer loops), PLL, $abc-dq$ transformation, delay of PWM and control system, and LC filter.

For the dq impedance derivation, the three-phase system is presented as the dq form, such as $\mathbf{v}_c$, $\mathbf{v}_f$, $\mathbf{i}_c$. The bold parameters stand for their dq matrix parameters such as $\widetilde{\mathbf{v}_f} = [\begin{smallmatrix}\widetilde{v}_{fd}\\ \widetilde{v}_{fq}\end{smallmatrix}]$. Notation $\widetilde{\ }$ means the small-signal disturbance. The dq control is based on the synchronized dq frame, their parameters after $abc-dq$ transformation are noted as $\mathbf{v}_c^s$ $\mathbf{v}_f^s$ $\mathbf{i}_c^s$. The dq-formed abc parameters are equal to their dq-synchronized parameters at steady state, but are different when a synchronized phase disturbance $\widetilde{\theta}$ appears at the $abc-dq$ transformation.

For example, $abc-dq$ transformation of v_f is given below:

$$\begin{bmatrix}\widetilde{v}_{fd} + V_{fq}\widetilde{\theta}\\ \widetilde{v}_{fq} - V_{fd}\widetilde{\theta}\end{bmatrix} = \begin{bmatrix}\widetilde{v}_{fd}^s\\ \widetilde{v}_{fq}^s\end{bmatrix} \tag{9}$$

The phase disturbance $\widetilde{\theta}$ comes from the PLL and grid resistance compensation, which is summarized below:

$$(\underbrace{R_v \times \frac{s}{s+\omega_c}}_{Z_v} \times \underbrace{\widetilde{i}_{gq}^s}_{\widetilde{i}_{gq}-I_{gd}\widetilde{\theta}} + \underbrace{\widetilde{v}_{fq}^s}_{\widetilde{v}_{fq}-V_{fd}\widetilde{\theta}}) \times \underbrace{PI_{pll}}_{k_p^{pll}+k_i^{pll}/s} \times \frac{1}{s} = \widetilde{\theta} \tag{10}$$

Rearranging (10) yields:

$$G_{pll}\widetilde{v}_{fq} + Z_v G_{pll}\widetilde{i}_{gq} = \widetilde{\theta} \tag{11}$$

where $G_{pll} = \frac{k_p^{pll}+k_i^{pll}/s}{s+(k_p^{pll}+k_i^{pll}/s)(V_{fd}+R_v s/(s+\omega_c)I_{gd})}$

Substituting $\widetilde{\theta}$ in (9) with (11) given:

$$\mathbf{G}_{fg}\widetilde{\mathbf{v}}_f + \mathbf{H}_{fg}\widetilde{\mathbf{i}}_g = \widetilde{\mathbf{v}}_f^s \tag{12}$$

where $\mathbf{G}_{fg} = [\begin{smallmatrix}1 & V_{fq}G_{pll}\\ 0 & 1-V_{fd}G_{pll}\end{smallmatrix}]$, $\mathbf{H}_{fg} = [\begin{smallmatrix}0 & V_{fq}Z_vG_{pll}\\ 0 & -V_{fd}Z_vG_{pll}\end{smallmatrix}]$.

$\widetilde{\mathbf{i}}_c^s$ and $\widetilde{\mathbf{v}}_c^s$ are found based on a similar derivation:

$$\widetilde{\mathbf{i}}_c + \mathbf{G}_{cf}\widetilde{\mathbf{v}}_f + \mathbf{H}_{cf}\widetilde{\mathbf{i}}_g = \widetilde{\mathbf{i}}_c^s \tag{13}$$

where $\mathbf{G}_{cf} = [\begin{smallmatrix}0 & I_{cq}G_{pll}\\ 0 & -I_{cd}G_{pll}\end{smallmatrix}]$, $\mathbf{H}_{cf} = [\begin{smallmatrix}0 & I_{cq}Z_vG_{pll}\\ 0 & -I_{cd}Z_vG_{pll}\end{smallmatrix}]$.

$$\widetilde{\mathbf{v}}_c^s + \mathbf{G}_{fc}\widetilde{\mathbf{v}}_f + \mathbf{H}_{fc}\widetilde{\mathbf{i}}_g = \widetilde{\mathbf{v}}_c \tag{14}$$

where $\mathbf{G}_{fc} = [\begin{smallmatrix}0 & -V_{cq}G_{pll}\\ 0 & V_{cd}G_{pll}\end{smallmatrix}]$, $\mathbf{H}_{fc} = [\begin{smallmatrix}0 & -V_{cq}Z_vG_{pll}\\ 0 & V_{cd}Z_vG_{pll}\end{smallmatrix}]$.

The linearization of the $abc-dq$ transformation are clarified in (12) (13) (14).

The impedance of the VSI includes the control system and its LC filter. The control system, as shown in Fig. 1, is represented below:

$$\mathbf{PI}_i(\mathbf{PI}_{pv}(\widetilde{\mathbf{ref}} - [\widetilde{P}\ -\widetilde{v}_{fd}^s] - \widetilde{\mathbf{i}}_c^s) + \widetilde{\mathbf{v}}_f^s + \mathbf{G}_{dec}\widetilde{\mathbf{i}}_c^s = \widetilde{\mathbf{v}}_c^s \tag{15}$$

where $\widetilde{\mathbf{ref}} = [\begin{smallmatrix}P^*\\ -v_{mag*}\end{smallmatrix}]$, $\mathbf{G}_{dec} = [\begin{smallmatrix}0 & -L_f\omega_0\\ L_f\omega_0 & 0\end{smallmatrix}]$, $\mathbf{PI}_i = [\begin{smallmatrix}k_p^i + k_i^i/s & 0\\ 0 & k_p^i + k_i^i/s\end{smallmatrix}]$, $\mathbf{PI}_{pv} = [\begin{smallmatrix}k_p^p + k_i^p/s & 0\\ 0 & k_p^v + k_i^v/s\end{smallmatrix}]$.

The linearized active power in dq frame is shown below:

$$\widetilde{P} \approx 1.5(I_{gd}\widetilde{v}_{fd} + V_{fd}\widetilde{i}_{gd} + I_{gq}\widetilde{v}_{fq} + V_{fq}\widetilde{i}_{gq}) \tag{16}$$

Substituting $\widetilde{P}$ and $\widetilde{v}_{fd}^s$ in (15) with (12) (16) yields:

$$\mathbf{PI}_i\mathbf{PI}_{pv}\widetilde{\mathbf{ref}} + \mathbf{G}_{rv}\widetilde{\mathbf{v}}_f + \mathbf{G}_{ri}\widetilde{\mathbf{i}}_g - \mathbf{PI}_i\widetilde{\mathbf{i}}_c^s + \widetilde{\mathbf{v}}_f^s + \mathbf{G}_{dec}\widetilde{\mathbf{i}}_c^s = \widetilde{\mathbf{v}}_c^s \tag{17}$$

where $PI_i = k_p^i + k_i^i/s$, $PI_p = k_p^p + k_i^p/s$, $PI_v = k_p^v + k_i^v/s$, $\mathbf{G}_{rv} = [\begin{smallmatrix}-1.5PI_pI_{gd} & -1.5PI_iPI_pI_{gq}\\ PI_iPI_v & PI_iPI_vV_{fq}G_{pll}\end{smallmatrix}]$ $\mathbf{G}_{ri} = [\begin{smallmatrix}-1.5PI_iPI_pV_{fd} & -1.5PI_iPI_pV_{fq}\\ 0 & PI_iPI_vV_{fq}Z_vG_{pll}\end{smallmatrix}]$.

Substituting $\widetilde{\mathbf{i}}_c^s$, $\widetilde{\mathbf{v}}_f^s$, and $\widetilde{\mathbf{v}}_c^s$ in (17) with (12) (13) (14) and taking the time T_{del} including control delay and the dead time of PWM into account yields:

$$\begin{aligned}\mathbf{G}_{del}\{&\mathbf{PI}_i\mathbf{PI}_{pv}\widetilde{\mathbf{ref}} + [\mathbf{G}_{rv} + (\mathbf{G}_{dec} - \mathbf{PI}_i)\mathbf{G}_{cf}\\ &+ \mathbf{G}_{fg} + \mathbf{G}_{fc}]\widetilde{\mathbf{v}}_f + [\mathbf{G}_{ri} + (\mathbf{G}_{dec} - \mathbf{PI}_i)\mathbf{H}_{cf}\\ &+ \mathbf{H}_{fg} + \mathbf{H}_{fc}]\widetilde{\mathbf{i}}_g + (\mathbf{G}_{dec} - \mathbf{PI}_i)\widetilde{\mathbf{i}}_c\} = \widetilde{\mathbf{v}}_c\end{aligned} \tag{18}$$

where $\mathbf{G}_{del} = [\begin{smallmatrix}(1-0.5T_{del}s)/(1+0.5T_{del}s) & 0\\ 0 & (1-0.5T_{del}s)/(1+0.5T_{del}s)\end{smallmatrix}]$.

The voltage and current relation on the LC filter can be found below:

$$\widetilde{\mathbf{v}}_c = \widetilde{\mathbf{v}}_f + \mathbf{Z}_f\widetilde{\mathbf{i}}_c \tag{19}$$

$$\widetilde{\mathbf{i}}_c = \mathbf{Y}_c\widetilde{\mathbf{v}}_f + \widetilde{\mathbf{i}}_g \tag{20}$$

where $\mathbf{Y}_c = [\begin{smallmatrix}C_f s & -\omega_0 C_f\\ \omega_0 C_f & C_f s\end{smallmatrix}]$, $\mathbf{Z}_f = [\begin{smallmatrix}L_f s + R_f & -\omega_0 L_f\\ \omega_0 L_f & L_f s + R_f\end{smallmatrix}]$.

Substituting $\widetilde{\mathbf{i}}_c$ in (19) with (20) yields:

$$\widetilde{\mathbf{v}}_c = \widetilde{\mathbf{v}}_f + \mathbf{Z}_f\mathbf{Y}_c\widetilde{\mathbf{v}}_f + \mathbf{Z}_f\widetilde{\mathbf{i}}_g \tag{21}$$

Substituting $\widetilde{\mathbf{i}}_c$ $\widetilde{\mathbf{v}}_c$ in (18) with (20) (21) yields:

$$\widetilde{\mathbf{v}}_f + \mathbf{Z}_f\mathbf{Y}_c\widetilde{\mathbf{v}}_f + \mathbf{Z}_f\widetilde{\mathbf{i}}_g = \mathbf{G}_{del}\mathbf{PI}_i\mathbf{PI}_{pv}\widetilde{\mathbf{ref}} + \mathbf{G}_v\widetilde{\mathbf{v}}_f + \mathbf{G}_i\widetilde{\mathbf{i}}_g \tag{22}$$

As shown in Fig. 4, $\mathbf{G}_{ref}$ is the gain factor function of the VSI reference. $\mathbf{G}_{ref}$ is the desired admittance of the VSI. $\mathbf{Y}_o$ and $\mathbf{G}_{ref}$ are defined via rearranging (22) based on Fig. 4:

$$\begin{aligned}\widetilde{\mathbf{i}}_g = &\underbrace{(\mathbf{Z}_f - \mathbf{G}_i)^{-1}(\mathbf{G}_v - \mathbf{Z}_f\mathbf{Y}_c - \mathbf{I})}_{-\mathbf{Y}_o}\widetilde{\mathbf{v}}_f\\ &+ \underbrace{(\mathbf{Z}_f - \mathbf{G}_i)^{-1}(\mathbf{G}_{del}\mathbf{PI}_i\mathbf{PI}_{pv})}_{\mathbf{G}_{ref}}\widetilde{\mathbf{ref}}\end{aligned} \tag{23}$$

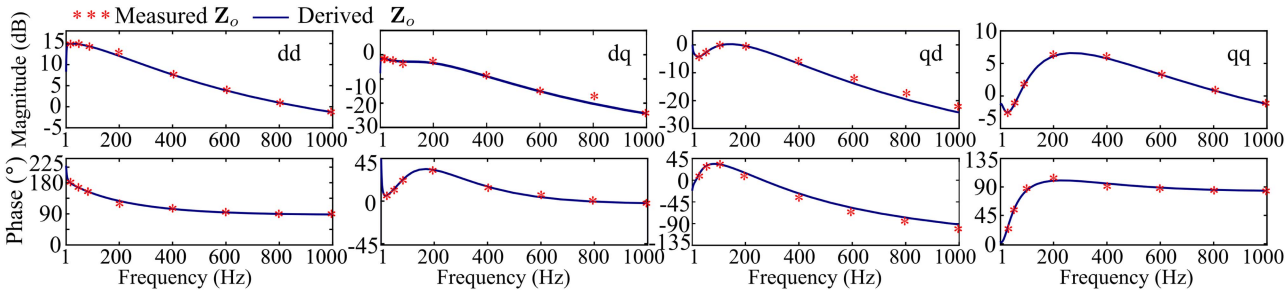

Fig. 8. Validation of derived VSI impedance $\mathbf{Z}_o$ including the proposed grid impedance compensation within the PLL.

where $\mathbf{G}_v = \mathbf{G}_{del}[\mathbf{G}_{rv} + (\mathbf{G}_{dec} - \mathbf{PI}_i)\mathbf{G}_{cf} + \mathbf{G}_{fg} + \mathbf{G}_{fc} + (\mathbf{G}_{dec} - \mathbf{PI}_i)\mathbf{Y}_c]$, $\mathbf{G}_i = \mathbf{G}_{del}[\mathbf{G}_{ri} + (\mathbf{G}_{dec} - \mathbf{PI}_i)\mathbf{H}_{cf} + \mathbf{H}_{fg} + \mathbf{H}_{fc} + \mathbf{G}_{dec} - \mathbf{PI}_i]$.

Therefore, the whole VSI admittance $\mathbf{Y}_o$ and impedance $\mathbf{Z}_o(= \mathbf{Y}_o^{-1})$ are fully derived for the VSI system with the proposed grid impedance compensation within the PLL, as shown in Fig. 1.

B. Validation of Derived Small-Signal Impedance

After deriving the dq VSI admittance and impedance, its validation is carried out via the measurement method [29]. Normally, the derived $\mathbf{Z}_o$ is used to compare to the measured VSI impedance. Two sets of 0.05 p.u. dq-independent AC current, which are essential for calculating 4 unknown impedance elements (Z_{odd} Z_{odq} Z_{oqd} Z_{oqq}), are injected at the grid connection point (Fig. 1) between the VSI and the AC grid. The parameters of the VSI system are presented in Table I. The measured and derived impedance matrices are drawn in Fig. 8. It shows good accuracy of the derived impedance matrix comparing to the measured impedance, which proves that the derived VSI impedance is accurate for stability analysis.

C. High-Pass Filter Design for Proposed Grid Impedance Compensation

To keep the balance between avoiding the steady-state error v_v at 0 Hz in the dq frame and maintaining the proper low-frequency effectiveness of virtual resistance. It is assumed that the total gain of the virtual resistance and the high-pass filter at ω_s is β. The following relation is given below:

$$\frac{s}{s+\omega_c} \times R_v \widetilde{i}_{gq}|_{\omega_s} = \beta \tag{24}$$

In normal operation $\widetilde{i}_{gd} \ll 1$, which simplifies (24) as:

$$\left|\frac{\omega_s j}{\omega_s j + \omega_c}\right| \times R_v < \beta \tag{25}$$

Rearranging (25) for finding R_v yields:

$$R_v < \beta\sqrt{1 + (\frac{\omega_c}{\omega_s})^2} \tag{26}$$

IV. Comparison Studies

The VSI system, as shown in Fig. 1, is used to present the comparison study between the proposed grid impedance compensation and the conventional inductive grid impedance compensation for the PLL. This comparison study includes the stability effectiveness, consequences of excessive compensation, VSI performance and robustness with various grid impedance. The advance of the proposed grid impedance compensation will be presented via the comparison study.

A very weak AC grid (SCR $= 1$) is connected. The small-signal impedance model of the conventional inductive grid impedance compensation is also derived for stability analysis and comparison. The cut-off frequency w_s and its gain β of the proposed grid impedance compensation are set at 6.28 rd/s and 0.1. Therefore, the virtual resistance in this compensation complies with $R_v < 15$ based on (26). All Parameters of this VSI system are presented in Table I.

Static power limitation of a VSC is different, which depends on the rectifier operation or inverter operation. When operating as a rectifier, the static power limitation is -0.85 p.u. at SCR $= 1$. When operating as an inverter, the static power limitation is 1.1 p.u.. It is reported [13][14] that instability occurs when VSC operates as an inverter with rated power injection to the weak grid. Therefore, in our analysis, the inverter operation is analyzed.

A. Stability Effectiveness

For validating the effectiveness of the proposed grid impedance compensation using virtual resistance, the pole map of the VSI system and its time-domain validation are shown in Fig. 9. As shown in Fig. 9(a), the poles close to $x = 0$ are presented. $R_v = 0$ indicates the VSI system using original PLL, and the VSI system is unstable when SCR $= 1$. With increasing the value of virtual resistance, the poles move to the left-half plane, which indicates that VSI is getting stable. For validating the analyzed results in the time domain, two poles ($R_v = 8.5$ and 9.5), that identify the unstable and stable conditions of this VSI, are simulated. The analyzed resonant frequency is 66 Hz as shown in Fig. 9(a) when $R_v = 9.5$.

The time-domain validation is shown in Figs. 9(b). When $R_v = 8.5$ is applied at 1 s, VSI loses stability. this VSI is recovered after $R_v = 9.5$ is applied at 1.4 s. It is validated that the analyzed unstable and stable conditions match the time-domain

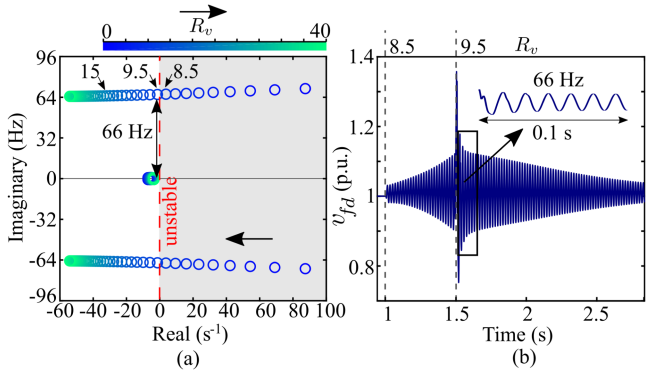

Fig. 9. Stability analysis and time-domain validation for the proposed resistive grid impedance compensation within the PLL. (a) Pole map of the inverter system with increasing R_v. (b) Time-domain validation of virtual resistance.

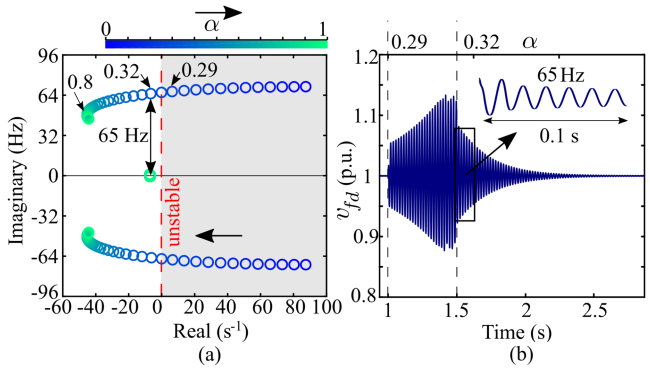

Fig. 10. Stability analysis and time-domain validation for the conventional inductive grid impedance compensation within the PLL. (a) Pole map of the inverter system with increasing α. (b) Time-domain validation of virtual negative inductance.

result. During 1 s to 1.5 s, the resonant frequency, as shown in Fig. 9(b), also matches the analyzed frequency. Moreover, the proposed grid impedance compensation can effectively stabilize the very-weak-grid connection.

This very-weak-grid connection (SCR = 1) can also be stabilized by the conventional inductive grid impedance compensation using virtual negative inductance, as shown in Fig. 10(a). Compensation ratio α is defined in (5). The time-domain validation is shown in Fig. 10(b). When α is changed to 0.29 at 1 s, v_{fd} start to oscillate which becomes unstable gradually. When α is changed to 0.32 at 1.5 s, v_{fd} stop oscillating gradually and return to the stable condition. It is found that the analyzed unstable and stable conditions match the time-domain results. The oscillation frequency is 65 Hz as shown in Fig. 10(b), which matches the analyzed frequency.

Comparing to the conventional inductive grid impedance compensation above, the proposed one can do the similar continuous stabilization for a VSI when connecting to a very weak grid.

B. Power Injection Improvement and Performance Analysis

A PLL-based vector-controlled VSI suffers instability when injecting full power to a very weak AC grid (such as SCR = 1)

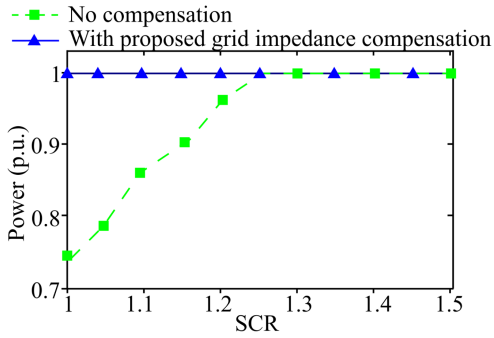

Fig. 11. Power injection capability of the VSI.

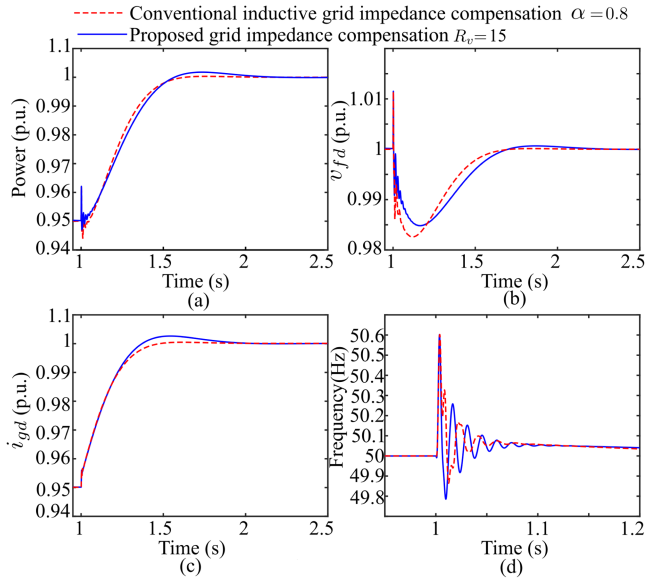

Fig. 12. Power step change comparison. (a) Active power. (b) *d*-axis voltage of connection point. (c) *d*-axis grid current. (d) Frequency.

which has been demonstrated in section IV-A. The maximum injected power of this VSI is identified based on the stability analysis, as shown in Fig. 11. When SCR = 1, only 0.75 p.u. power can be injected to the grid. By using the proposed grid impedance compensation, it is found that the full power injection is maintained even with SCR = 1, as shown in Fig. 11.

This power injection improvement is demonstrated via the performance test, which is a power step-change test with SCR = 1. Optimized parameters of both compensation are selected based on the stability analysis in section IV-C, where $R_v = 15$ and $\alpha = 0.8$. Both compensation enable a smooth power step change from 0.95 to 1 p.u., as shown in Fig. 12(a). Their grid currents and voltages of the connection point, respectively, have similar and smooth dynamics during the power step change, as shown in Fig. 12(b), (c). For both compensation, the disturbances on the frequency are damped in a similar time period, as shown in Fig. 12(d).

In a sum, the proposed grid impedance compensation enables a full power injection with very-weak-grid connection, and its performance is similar to the conventional inductive grid impedance compensation.

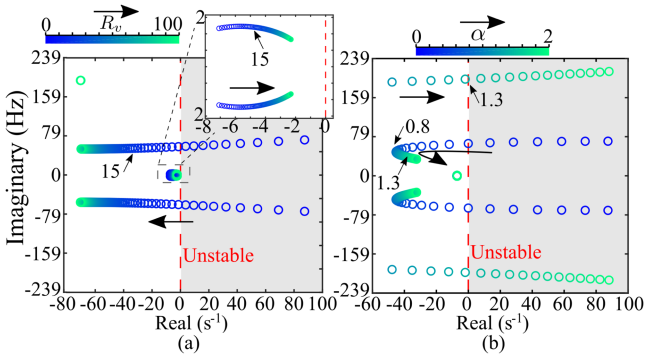

Fig. 13. Overcompensation analysis on VSI stability. (a) Virtual resistance. (b) Virtual negative inductance.

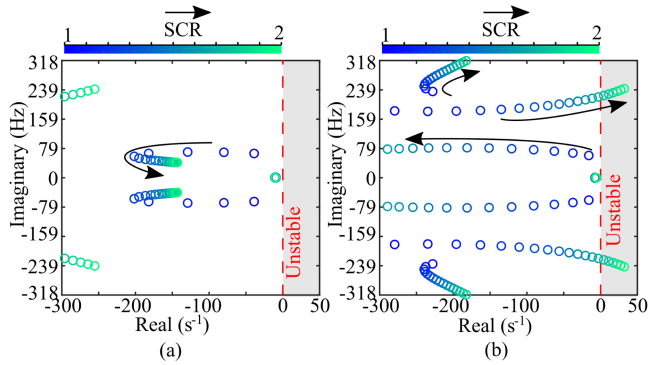

Fig. 14. Impact of grid impedance variance on PLL's grid impedance compensation. (a) Porposed resistive grid impedance compensaton. (b) Conventional inductive grid impedance compensation.

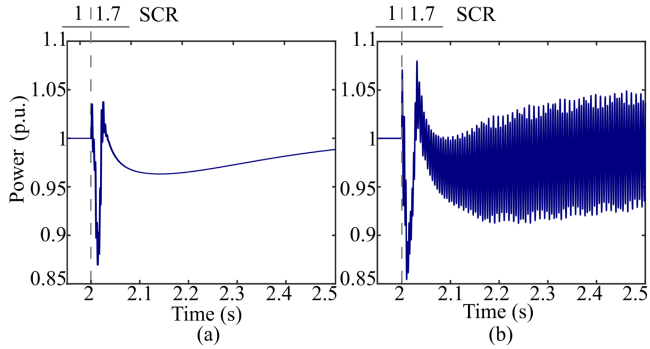

Fig. 15. Time-domain validation of grid impedance variance impact. (a) Porposed resistive grid impedance compensaton. (b) Conventional inductive grid impedance compensation.

C. Overcompensation Impact

The parameters of R_v and α are analyzed based on the small-signal impedance model. Values of the virtual resistance and the virtual negative inductance are extended widely to explore their overcompensation impact on the VSI. The stability analysis of this VSI system with $R_v \in [0\ 100]$ and $\alpha \in [0\ 2]$ are presented in Fig. 13.

For the proposed grid impedance compensation within the PLL, as shown in Fig. 13(a), when R_v increases to 15, the poles are effectively moved to the left from 90 to $-50\ s^{-1}$. However, the rest of $R_v \in [15\ 100]$ moves poles to the left from -50 to $-70\ s^{-1}$. The poles in the mid of Fig. 13(a) are moved slight toward the right-half plane with increasing R_v, which makes the VSI system slightly less stable. Based on the stability analysis of the VSI system above, $R_v = 15$ puts the VSI system in a good stable position. Furthermore, overcompensation of R_v does not cause a significant unstable impact.

For the conventional inductive grid impedance compensation within the PLL, as shown in Fig. 13(b), when α increases to 0.8, the poles are moved to the left significantly. However, when $\alpha \in$ increases from 0.8 to 2, some poles move to the right-half plane and lead to the instability at $\alpha = 1.3$. Based on the stability analysis of the VSI system above, $\alpha = 0.8$ puts the VSI system in a good stable position. However, the virtual negative inductance cause the instability if the overcompensation occurs ($\alpha > 1.3$).

D. Influence of Grid Impedance Variance

For the SCR of a grid >1, the overcompensation will occur If the conventional inductive grid impedance compensation is applied based on the worst case SCR = 1. This case is likely to occur if the grid impedance varies or not be measured accurately. Therefore, the effectiveness of both grid impedance compensation are assessed considering grid impedance variance from 1 p.u. to 0.5 p.u., which is equivalent to SCR = 1 to 2.

VSI system stability is presented in Fig. 14 with grid impedance variance. With increasing SCR, poles of the inverter system using the proposed grid impedance compensation further moves to the left, which enables a consistently stable grid connection, as shown in Fig. 14(a). With increasing SCR, some poles of the VSI system using conventional inductive grid impedance compensation move to the right-half plane, and the VSI loses stability when the SCR is above 1.7, as shown in Fig. 14(b). It proves that the proposed grid impedance compensation is more robust against the grid impedance variance compared to the conventional inductive grid impedance compensation.

Time-domain validation is also presented based on the SCR variance from 1 to 1.7 at 1 s. The results are shown in Fig. 15 . The proposed grid impedance compensation enables a stable power injection, which power is maintained at 1 p.u. after 1 s, as shown in Fig. 15(a). On the contrary, after SCR variance occurs, the conventional inductive grid compensation is overcompensated for the grid, which results in instability, as shown in Fig. 15(b).

V. Conclusion

An improved grid impedance compensation for the PLL using virtual resistance is proposed in this paper to stabilize the very-weak-grid connection (SCR<1.3) for vector-controlled VSIs with rated power injection.

The drawbacks of the conventional inductive grid impedance compensation for the PLL are revealed and validated, which are sensitive to the grid impedance variance and cause the PLL instability if overcompensation occurs.

By comparing to the conventional inductive grid impedance compensation, it is validated that the proposed grid impedance compensation has the similar performance during VSI power

regulation with SCR = 1 and possesses the excellent tolerance against a wide range of grid impedance variance. Furthermore, by stability analysis and time-domain validation, the instability caused by overcompensation is avoided by the proposed grid impedance compensation.

The small-signal impedance model of VSI system using the proposed grid impedance compensation is derived and validated via the impedance measurement. After the time-domain test for VSI system, this small-signal impedance model can effectively involve the parameter design for VSI connecting to a very weak grid.

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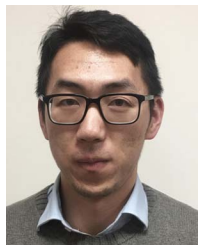

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