This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification

SiC-Based Improved Neutral Legs with Reduced Capacitors for Three-phase Four-wire EV Chargers

Peng Yang, *Student Member, IEEE,* Wenlong Ming, *Member, IEEE,* Jun Liang, *Senior Member, IEEE,* Carlos E. Ugalde-Loo, *Senior Member, IEEE,* Rukshan Navaratne, *Member, IEEE,* Omar Ellabban, *Senior Member, IEEE,* and Ingo Lüdtke

***Abstract*—An electric vehicle (EV) charger can operate in an autonomous mode to create its own grid by utilizing the EV batteries during grid blackouts. This requires three-phase four-wire inverters as the grid-side ac/dc port of the EV charger to supply unbalanced loads. Although silicon carbide (SiC) MOSFETs can be adopted to increase the power density of these inverters, the second order ripples exhibited on the dc bus caused by unbalanced loads need to be mitigated by a large dc capacitance—increasing the size of inverters. In this paper, an improved neutral leg for three-phase four-wire inverters is presented, which not only provides the neutral current for unbalanced loads like a conventional neutral leg, but also reduces the second order ripples on the dc bus without the need for additional hardware components. Furthermore, it can reduce by 50% the dc capacitance compared to its conventional counterpart. A control strategy featuring power decoupling capability is included for the improved leg. It was built with SiC MOSFETs and experimentally assessed with a three-phase inverter, with results verifying its effectiveness. For completeness, the performance of the improved neutral leg is also evaluated through simulations in PLECS and compared to a conventional neutral leg.**

***Index Terms*—Neutral leg, three-phase four-wire inverter, second order ripple, SiC MOSFET, electric vehicle.**

NOMENCLATURE

p_{ac}	Instantaneous ac output power.
P_o	Average output power.
$p_{2\omega}$	Second-order ripple in output power.
$P_{2\omega}$	Amplitude of second order ripple in output power.
δ	Imbalance factor.
v_{DC}	DC bus voltage.
V_{avg}	Average value of dc bus voltage.
V_{max}	Peak value of dc bus voltage.
ΔV	Amplitude of dc bus voltage ripple.
V_{rms}	RMS value of phase-to-ground ac voltages.
$V_{C\_}$	Voltage on neutral capacitor $C_{\_}$.
$V_{2\omega}$	Amplitude of second-order ripple on $V_{C\_}$.
$I_{DC\_2\omega}$	Second order current ripple in dc bus.
I_{de}	Decoupling current injected to $C_{\_}$.

This work was supported by the European Commission's Horizon 2020 Research & Innovation Programme (Marie Skłodowska-Curie Actions) through the project "Innovative Tools for Offshore Wind and DC Grids (InnoDC)", under Grant 765585, and the EPSRC "Sustainable urban power supply through intelligent control and enhanced restoration of AC/DC networks", under Grant EP/T021985/1. (Corresponding author: Wenlong Ming)

P. Yang, J. Liang, C. E. Ugalde-Loo and R. Navaratne are with School of Engineering, Cardiff University, Cardiff, CF24 3AA, United Kingdom. (e-mail: yangp6, liangj1, ugalde-looc, navaratner@cardiff.ac.uk).

W. Ming is with School of Engineering, Cardiff University, Cardiff, and also with Compound Semiconductor Applications Catapult, Newport, United Kingdom. (e-mail: mingw@cardiff.ac.uk)

O. Ellabban and I. Lüdtke are with the Compound Semiconductor Applications Catapult, Newport, NP10 8BE, UK. (e-mail: omar.ellabban, ingo.ludtke@csa.catapult.org.uk).

A preliminary version of this paper was presented at the IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, under the title "A SiC-based Neutral Leg for the Three-phase Four-wire Inverter".

I. INTRODUCTION

THREE-phase inverters have been widely used as an interface between active distribution networks and distributed energy resources [1], such as solar photovoltaics, energy storage systems and electric vehicles (EVs). The increased penetration of distributed energy resources into conventional centralized power systems is shifting them to become decentralized [2], where a grid-tied inverter can work in an autonomous mode to form its own grid [3]. For example, due to the rapidly increasing deployment of EVs, the use of their batteries as energy storage media has enabled flexible power management of decentralized distribution networks, including concepts such as vehicle-to-grid, grid-to-vehicle, vehicle-to-home and vehicle-to-load [4]. In particular, vehicle-to-grid/load applications require EVs to work in an autonomous mode so that an independent grid is formed during power outages [5].

In an autonomous mode of operation, EVs must use the on-board or off-board chargers (i.e. dc/ac converters) to build the independent grid. Such a grid can either be single-phase ac for a single home or three-phase ac for a large community [6]. When a three-phase ac grid is formed by EVs, the EV chargers may be potentially exposed to unbalanced loads. Three-phase four-wire inverters are required to provide a neutral wire for unbalanced load currents [7].

There are various topologies of three-phase four-wire inverters. The simplest one is the conventional three-phase three-leg inverter with split dc bus capacitors (split-link topology) proposed in [8], which connects the neutral point of the ac loads to the mid-point of the dc bus. This topology uses the least number of semiconductors (six switches only). However, the voltage balancing of the split capacitors is difficult [9] and a large capacitance is required to attenuate voltage variations exhibited by them [10]. Another topology is the three-phase four-leg inverter (four-leg topology) proposed in [11], which includes an additional fourth leg to provide a neutral current. A three-dimensional space vector modulation is proposed in [12] for this topology, which enables a 15% higher utilization of the dc bus voltage compared to a split-link topology. In

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification

[13], a neutral current minimization control is proposed for the four-leg topology. One of the main drawbacks of the four-leg inverter is the electromagnetic interference problems caused by the high-frequency operation of the neutral leg [14]. Also, the control loops of the neutral leg and of the three-phase inverter are coupled, which requires more complex control algorithm compared to its counterpart. A third topology is the three-phase inverter with an independently controlled neutral leg (neutral-leg topology) proposed in [15]. This topology is a combination of the aforementioned two configurations, where the mid-point of the split dc bus is connected to the neutral leg. In [16] , a paralleled PI and H infinity control method is proposed to provide the neutral current through the neutral leg and the neutral inductor instead of doing so through the split capacitors. As a result, voltage balancing of the split capacitors can be maintained and the capacitance value reduced. Moreover, this topology also allows an independent control of the neutral leg and avoids the electromagnetic interference problems exhibited by the four-leg inverter [17]. In [18], the dc bus voltage utilization of the independent-neutral-leg topology is increased by 15% through injecting a third-order harmonics to the neutral point.

The structure of an EV charger in an autonomous mode is shown in Fig. 1. It consists of an isolated dc/dc converter and, the aforementioned third topology of three-phase four-wire inverters, which has an independently controlled neutral leg, and LC filters. In this system, besides the need to supply neutral current, another challenge is the second order current and voltage ripples on the dc bus caused by unbalanced loads [19], which is not addressed in the aforementioned literature. In [6], the relation between these ripples and the unbalanced load currents is analyzed. It is reported in [20] and [21] that these ripples should be addressed with care as they can propagate to the EV batteries which, consequently, might deteriorate their performance and decrease their lifetime. In [22], an adaptive sliding mode control scheme is proposed to reduce the voltage ripples by storing them in the dc bus. However, bulky dc capacitors are still required for power decoupling and to limit the overall voltage ripple on the dc bus to a suitable range, which reduces the power density of the converter.

To increase the power density of EV chargers, wide bandgap semiconductors, such as silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) and gallium nitride (GaN) high-electron-mobility transistors (HEMTs) have been widely adopted for on board battery chargers [23] and fast EV charging station [24]. In [25], SiC MOSFETs are adopted in the ac/dc converter to increase the switching frequency to 250 kHz which, in turn, reduces the required inductance of the grid-side filter. However, the capacitance of the dc bus is related to the second order ripples and its value cannot be reduced by increasing the switching frequency. To reduce the dc capacitance, a compensator is presented in [26] so that the ripples are mitigated. However, such a compensator requires additional semiconductors and passive components. Other solutions available in the open literature also require additional active power decoupling circuits in series [27] or in parallel [28] with the dc bus, which inevitably increase the total cost and losses of the system.

In this paper, an improved neutral leg for three-phase four-wire EV chargers including its operation principles is presented. This topology provides neutral current and reduces second order ripples on the dc bus while simultaneously enables an adequate operation under unbalanced loads. The dc capacitance requirements of a conventional neutral leg and of the improved neutral leg to mitigate the second order ripples on the dc bus are analyzed and compared. Since the dc bus ripples are reduced, it is shown that the adoption of the improved neutral leg can reduce by 50% the dc capacitance value compared to when a conventional neutral leg is used. This, in turn, further reduces the overall size of the neutral leg. For completeness, the control strategy of the three-phase four-wire inverter incorporating the improved neutral leg is included. To highlight its benefits, the improved neutral leg is compared with its conventional counterpart in terms of efficiency, size of neutral inductors, and fault tolerance capabilities. Simulation results obtained using PLECS and experimental results obtained through a laboratory test rig are provided to verify the operation of the improved topology. The main contributions of this paper are summarized as follows:

1) The second-order ripples on the dc bus of three-phase four-wire inverter are reduced by the improved neutral leg without additional hardware cost.
2) Control strategy for the improved neutral leg is proposed to ensure that the improved neutral leg can provides neutral current and reduces second-order ripples simultaneously.
3) Due to the reduced second-order ripples, the improved neutral leg can reduce by 50% the dc capacitance value compared to a conventional neutral leg.

II. DC Capacitance Requirements in Conventional SiC-based Neutral Legs

Fig. 2a shows the conventional neutral leg for a three-phase four-wire inverter. To calculate the size of its dc capacitor, a volume comparison of the main passive components of the neutral leg is carried out. A 10 kW three-phase four-wire inverter is used as an example to facilitate the comparison.

A. Total DC Capacitance Requirements

For three-phase four-wire inverters supplying unbalanced loads, the instantaneous output power at the ac side p_{ac} is given as

$$p_{ac} = P_o + p_{2\omega} = P_o + P_{2\omega}\cos\left(2\omega t + \phi\right) \tag{1}$$

where P_o is the average value of the output power; and $P_{2\omega}$, ω and ϕ are the amplitude, angular frequency and phase angle of the second order power ripple $p_{2\omega}$, respectively. Detailed derivation of (1) and values of P_o, $P_{2\omega}$, ω and ϕ can be found in [29]. An imbalance factor δ is defined as

$$\delta = \frac{P_{2\omega}}{P_o}. \tag{2}$$

The larger the value of δ is, the more unbalanced the operation of the inverter will be.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification

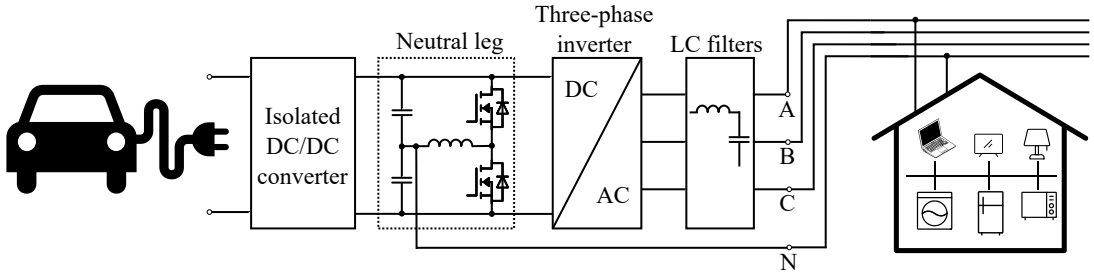
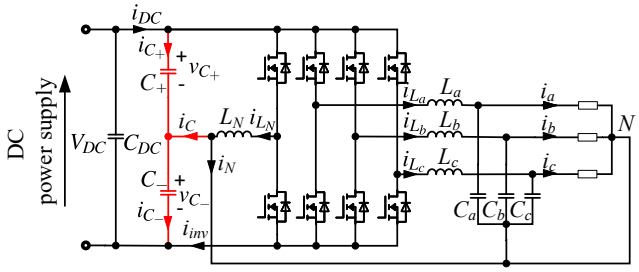
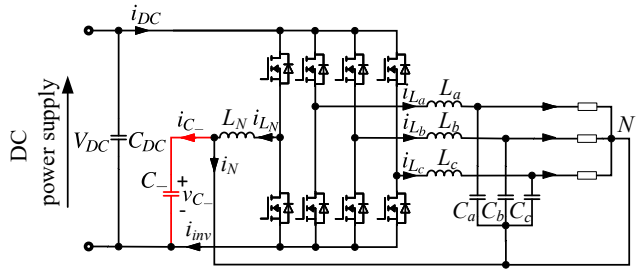


Fig. 1. Structure of a three-phase four-wire EV charger in an autonomous mode with an independently controlled neutral leg.



(a) With the conventional neutral leg.



(b) With the improved neutral leg by removing C_+.

Fig. 2. Three-phase four-wire inverter with neutral legs.

Due to power balance between the ac and dc sides, the second order power ripple $p_{2\omega}$ inevitably propagates from the ac to the dc side, which leads to second order ripples in the dc bus voltage. It is often required to limit such ripples because they can compromise system performance [30]. For example, a large voltage ripple on the dc bus may lead to a high voltage stress on switches, thereby deteriorating the power quality of output voltages and currents of the inverters [31].

To achieve smooth dc bus voltage and current, large dc capacitors are often required to limit the ripple within a required range. For conventional neutral legs (see Fig. 2a), C_+ and C_- are used for this purpose, while C_{DC} is a very small film capacitor representing the sum of the film capacitors placed close to power switches for filtering out switching noises. Here, C_{DC} is neglected when calculating the total dc capacitance. Assuming that $C_+ = C_- = C_N$, the dc bus voltage and the amplitude of the second order voltage ripple on the dc bus are respectively given as [32]:

$$v_{DC} = V_{avg} + \Delta V \sin(2\omega t + \theta) \tag{3}$$

$$\Delta V = \frac{P_{2\omega}}{\omega C_N V_{avg}} = \frac{\delta P_o}{\omega C_N V_{avg}} \tag{4}$$

where V_{avg} is the average dc bus voltage, and ΔV and θ are the amplitude and phase angle of the second order voltage ripple on the dc bus, respectively. The voltages across C_+ and C_- are balanced by regulating i_C to zero; that is,

$$v_{C_+} = v_{C_-} = \frac{1}{2} v_{DC} \tag{5}$$

where v_{C_+} and v_{C_-} are the voltages across the capacitors C_+ and C_-, respectively.

For three-phase four-wire inverters, the capacitance of C_+ and C_- must be large enough so that the following conditions are met [18]:

$$\begin{cases} v_{C_+} \geq \sqrt{2} V_{rms} \\ v_{C_-} \geq \sqrt{2} V_{rms} \end{cases} \tag{6}$$

where V_{rms} is the RMS value of phase-to-ground ac voltages. Substituting (3), (4) and (5) into (6) yields

$$V_{avg} + \frac{\delta P_o}{\omega C_N V_{avg}} \sin(2\omega t + \theta) \geq 2\sqrt{2} V_{rms}. \tag{7}$$

The required V_{avg} can be obtained by solving (7),

$$V_{avg} \geq \sqrt{2} V_{rms} + \sqrt{2V_{rms}^2 + \frac{\delta P_o}{\omega C_N}}. \tag{8}$$

The peak value of dc bus voltage V_{max} can be then calculated as

$$V_{max} = V_{avg} + \Delta V \geq \sqrt{8V_{rms}^2 + \frac{4\delta P_o}{\omega C_N}}. \tag{9}$$

Since a higher V_{max} implies a higher voltage stress, C_N should be large enough to limit V_{max}, that is,

$$C_N \geq \frac{\delta P_o}{\omega \left(V_{max} - 2\sqrt{2} V_{rms}\right)} \cdot \frac{4}{\left(V_{max} + 2\sqrt{2} V_{rms}\right)}. \tag{10}$$

Since $C_+ = C_- = C_N$, the total capacitance required in the conventional neutral leg is given by

$$C_{total,con} \geq \frac{\delta P_o}{\omega \left(V_{max} - 2\sqrt{2} V_{rms}\right)} \cdot \frac{8}{\left(V_{max} + 2\sqrt{2} V_{rms}\right)}. \tag{11}$$

$C_{total,con}$ is often large so bulky and vulnerable electrolytic capacitors are required. However, this leads to a low power density and a reduced reliability of neutral legs [33].

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification

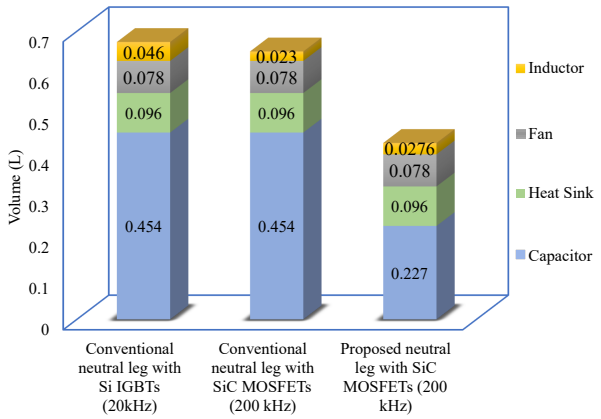


Fig. 3. Volume comparison of main passive components of conventional neutral legs with Si IGBTs, SiC MOSFETs and the improved neutral leg with SiC MOSFETs for a 10 kW three-phase inverter. The total volumes of the components are 0.674 L, 0.651 L, 0.429 L, respectively. Detailed calculations are provided in the Appendix.

B. Volume Considerations

The volume of the main components of the neutral leg for a 10 kW three-phase four-wire inverter is shown in Fig. 3. The detailed calculation method is presented in the Appendix. It can be seen that the volume of the dc capacitors accounts for 70% of the total volume of the main passive components in the conventional neutral leg based on Si IGBTs. The size of the inductor can be significantly reduced with an increased switching frequency by replacing the Si IGBTs with SiC MOSFETs. However, this marginally contributes to the total volume reduction since large dc capacitors are still required to mitigate the second order power ripple due to unbalanced loads (as shown in Fig. 3). To reduce the total volume of the neutral leg, the dc capacitance should be reduced. As it will be shown in Section III, this can be achieved with an improved neutral leg configuration.

III. Improved Neutral Leg with Reduced Capacitance

A. Topology and Operation Principles

To reduce the required dc capacitance, a novel improved topology of neutral legs is presented. This is shown in Fig. 2b. Compared to the conventional one (see Fig. 2a), the improved neutral leg is achieved by either removing the upper capacitor C_+ or the lower capacitor C_- from the dc bus. The first option is adopted in this paper. Although such a modification seems minor, it is important as it enables the reduction of second order ripples on the dc bus by diverting them from the dc bus to capacitor C_-. As a result, a significant reduction of the required dc capacitance is achieved.

The improved neutral leg is operated in the same manner as its conventional counterpart, i.e. by switching on and off the two switches in a complementary way to provide neutral current. The improved configuration can also be controlled independently from the three-phase inverters.

By removing C+, the equivalent capacitor of the dc bus is reduced. Compared to the large neutral leg capacitors designed for low-frequency second-order ripples, the remaining dc bus capacitor only need to filter out the switching harmonics and thus can be quite small. The voltage controller of the isolated dc/dc converter should be redesigned according to the reduced dc bus capacitor to achieve stability according to [34].

B. Capacitance Reduction through the Injection of Second Order Currents

In the improved neutral leg, the second order power ripple $p_{2\omega}$ on the dc bus can be compensated by injecting second order decoupling current to C_-:

$$i_{de} = I_{de} cos\left(2\omega t + \theta_{2\omega}\right). \tag{12}$$

The voltage of C_- is regulated to $\frac{V_{DC}}{2}$, but it will exhibit second order ripples due to the injected current. The voltage V_{C_-} and instantaneous power p_{C_-} of C_- can be respectively calculated as:

$$\begin{aligned} v_{C_-} &= \frac{V_{DC}}{2} + \frac{I_{de}}{2\omega C_-}\sin\left(2\omega t + \theta_{2\omega}\right) \\ &= \frac{V_{DC}}{2} + V_{2\omega}\sin\left(2\omega t + \theta_{2\omega}\right) \end{aligned} \tag{13}$$

$$\begin{aligned} p_{C_-} &= v_{C_-} i_{C_-} = \omega C_- V_{2\omega} V_{DC}\cos\left(2\omega t + \theta_{2\omega}\right) \\ &+ \omega C_- V_{2\omega}^2 \sin\left(4\omega t + 2\theta_{2\omega}\right) \\ &= p_{C\_2\omega} + p_{C\_4\omega}. \end{aligned} \tag{14}$$

where $p_{C\_2\omega}$ and $p_{C\_4\omega}$ represent the second order and fourth order components in the expression for p_{C_-}, respectively.

If the instantaneous power of the neutral inductor L_N is neglected, the second order power ripple on the dc bus can be compensated if $p_{C\_2\omega}$ in (14) is equal to $p_{2\omega}$ in (1). Therefore, term $V_{2\omega}$ presented in (14) can be calculated as

$$V_{2\omega} = \frac{P_{2\omega}}{\omega C_- V_{DC}} = \frac{\delta P_o}{\omega C_- V_{DC}}. \tag{15}$$

The second-order decoupling current I_{de} can be calculated as:

$$I_{de} = 2\omega C_- v_{2\omega} = \frac{2P_{2\omega}}{V_{DC}} = 2i_{DC\_2\omega} \tag{16}$$

where $v_{2\omega} = V_{2\omega}\sin\left(2\omega t + \theta_{2\omega}\right)$; $i_{DC\_2\omega}$ is the second-order current ripple on the dc bus.

Like the conventional neutral leg, v_{C_-} should fulfill (6) to have an undistorted ac output, thus

$$v_{C_-} = \frac{V_{DC}}{2} + \frac{\delta P_o}{\omega C_- V_{DC}}\sin\left(n\omega t + \theta_{n\omega}\right) \geq \sqrt{2}V_{rms}. \tag{17}$$

Therefore, the capacitance requirement of C_- can be calculated according to the maximum value of the dc bus voltage V_{max}

$$C_- \geq \frac{\delta P_0}{\omega\left(V_{max} - 2\sqrt{2}V_{rms}\right)} \cdot \frac{2}{V_{max}}. \tag{18}$$

The total capacitance in the improved neutral leg is the value C_- since only one capacitor is used. Therefore,

$$C_{total,pro} = C_- \geq \frac{\delta P_0}{\omega\left(V_{max} - 2\sqrt{2}V_{rms}\right)} \cdot \frac{2}{V_{max}}. \tag{19}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification

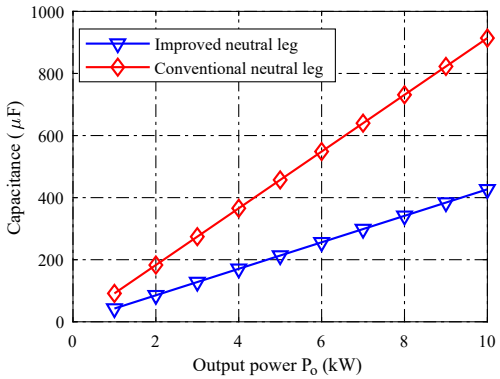


Fig. 4. Comparison of total dc capacitance ($V_{max} = 750$ V, imbalance factor $\delta = 0.5$).

The minimum total capacitance in the improved and conventional neutral legs can be compared using (11) and (19) as

$$\frac{C_{total,pro}}{C_{total,con}} = \frac{\left(V_{max} + 2\sqrt{2}V_{rms}\right)}{4V_{max}} < \frac{1}{2}. \tag{20}$$

According to (20), the improved neutral leg reduces the total dc bus capacitance of a conventional neutral leg by at least 50%. The capacitance requirements of both neutral leg configurations are compared in Fig. 4, with their volume comparison shown in Fig. 3. With a 50% reduction of dc capacitance, the total volume of the improved neutral leg is significantly reduced by 34%.

C. Impact of the Injected Second Order Currents

1) Impact on Provision of Neutral Current Provision: Although one capacitor has been removed in the improved neutral leg, it has the same capability as the conventional neutral leg to provide a neutral current to unbalanced loads. This is achieved through active control. The current provided by the neutral inductor L_N consists of two parts, namely

$$i_{L_N} = i_N + i_{C_-} \tag{21}$$

where i_N is the neutral current required by the unbalanced loads and i_{C_-} is the compensation current injected to C_- to reduce second order ripples on the dc bus. Two independent controllers can be adopted to regulate i_N and i_{C_-} so that the improved neutral leg provides the required neutral current. The overall control strategy is presented in Section IV.

2) Impact on Three-Phase Output Currents i_{La}, i_{Lb} and i_{Lc}: In the conventional neutral leg, the neutral point is regulated to a value $\frac{V_{DC}}{2}$. However, harmonic currents will be introduced to the three-phase output currents due to the existing second order ripples on the dc bus [32]. Compensators should thus be designed to eliminate the harmonics [35]. In the improved neutral leg, although the second order ripples are compensated, the neutral point contains a second order voltage ripple instead. Therefore, the three-phase current controllers should be designed to compensate the harmonic currents induced by the neutral point variation.

3) Impact on the DC Bus Voltage V_{DC}: According to (14), although the second order power ripple on the dc bus is compensated, an additional fourth order power ripple $p_{C-\_4\omega}$ is introduced by C_- which will cause, in turn, fourth order ripples on the dc bus. However, the amplitude of $p_{C-\_4\omega}$ is much smaller than that of $P_{2\omega}$. This may be guaranteed if $V_{2\omega}$ is limited to less than 10% of V_{DC} by properly choosing the capacitance value of C_- to reduce the dc bus voltage stress. On the other hand, to further reduce the fourth order ripples, a fourth order voltage component can be added on C_-

$$v_{C_-} = \frac{V_{DC}}{2} + V_{2\omega}\sin\left(2\omega t + \theta_{2\omega}\right) + V_{4\omega}\sin\left(4\omega t + \theta_{4\omega}\right). \tag{22}$$

The instantaneous power of C_- can be calculated accordingly as

$$p_{C_-} = p_{C-\_2\omega} + p_{C-\_4\omega} + p_{C-\_6\omega} + p_{C-\_8\omega} \tag{23}$$

where

$$p_{C-\_2\omega} = \omega C_N V_{2\omega} V_{DC}\cos\left(2\omega t + \theta_{2\omega}\right) \tag{24}$$
$$+ \omega C_N V_{2\omega} V_{4\omega}\cos\left(2\omega t - \theta_{2\omega} + \theta_{4\omega}\right) \tag{25}$$

$$p_{C-\_4\omega} = \omega C_N V_{2\omega}^2\sin\left(4\omega t + 2\theta_{2\omega}\right) \tag{26}$$
$$+ 2\omega C_N V_{4\omega} V_{DC}\cos\left(4\omega t + \theta_{4\omega}\right) \tag{27}$$

$$p_{C-\_6\omega} = \omega C_N V_{2\omega} V_{4\omega}\sin\left(6\omega t + \theta_{2\omega} + \theta_{4\omega}\right) \tag{28}$$

$$p_{C-\_8\omega} = 2\omega C_N V_{4\omega}^2\sin\left(8\omega t + 2\theta_{4\omega}\right). \tag{29}$$

To compensate both the second order and fourth order ripples, the following equation should be fulfilled:

$$\begin{cases} p_{C-\_2\omega} = p_{2\omega} \\ p_{C-\_4\omega} = 0. \end{cases} \tag{30}$$

A collateral effect of this compensation is that sixth and eighth order ripples are introduced. However, their amplitudes are even smaller than the fourth order power ripple, as shown in Fig. 5. This implies that the total ripples on the dc bus are further reduced and the dc bus capacitance can be much smaller.

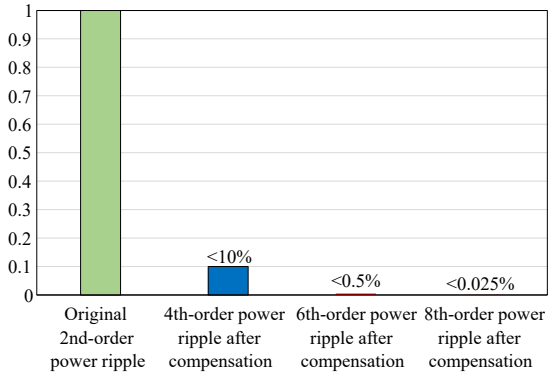


Fig. 5. Amplitude of the remaining power ripples on the dc bus after compensation (relative to the original second order power ripple).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification

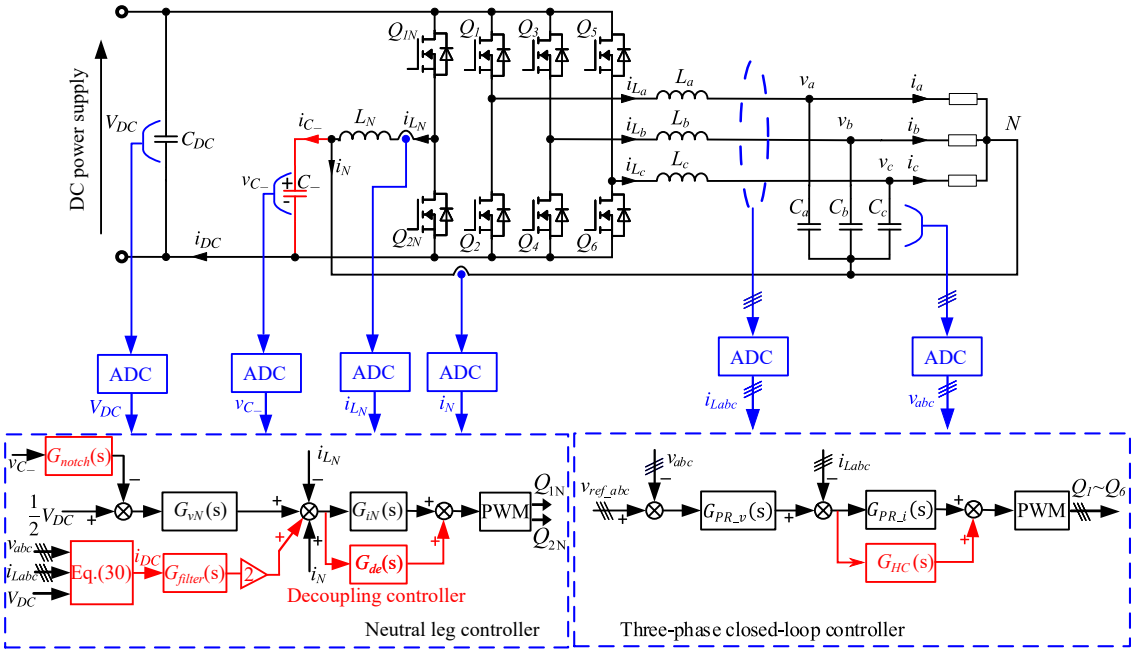


Fig. 6. Control for the improved neutral leg and the three-phase inverter.

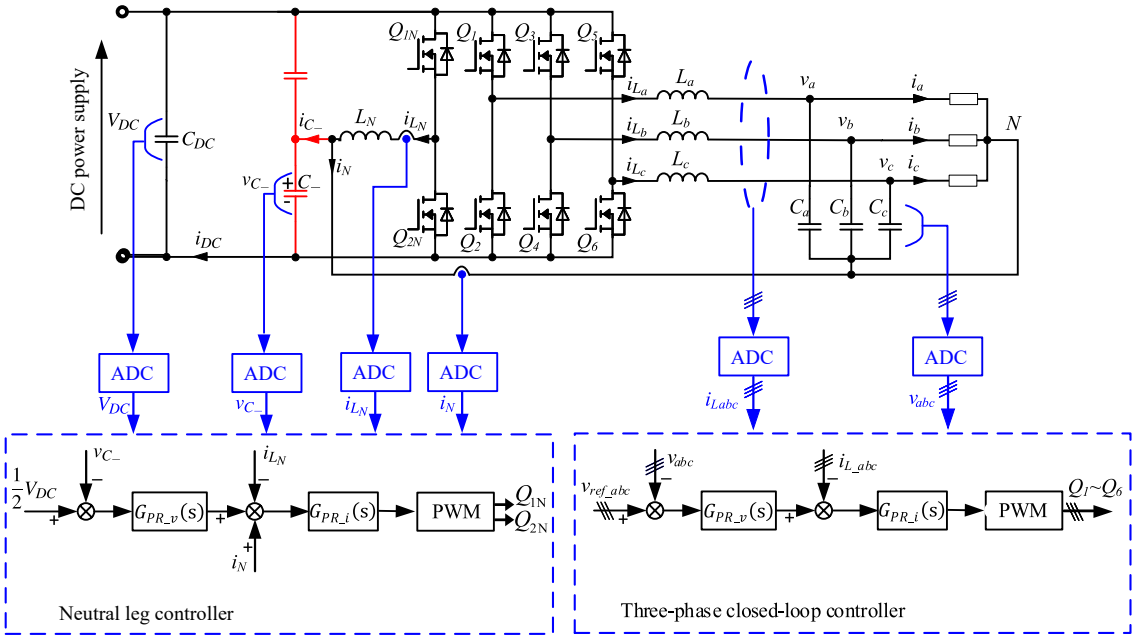


Fig. 7. Control for the improved neutral leg and the three-phase inverter.

IV. Control Design

The control strategy for the three-phase inverter with the improved neutral leg is shown in Fig. 6. This consists of two independent parts as in conventional neutral leg: one for the neutral leg and another one for the three-phase four-wire inverter. As a comparison, the control strategy for the inverter with the conventional neutral leg is shown in Fig. 7. The differences between two control systems are highlighted in red color, including:

1) In the improved neutral leg, the dc-bus current is calculated based on the measured three-phase voltages and currents. A resonant filter $G_{filter}(s)$ is adopted to extract the second-order ripple from the dc-bus current.
2) A resonant controller $G_{de}(s)$ is used in the current loop of the improved neutral leg to remove the second order ripples from the dc bus.
3) A notch filter $G_{notch}(s)$ is adopted in the voltage loop of the improved neutral leg to remove the second-order ripples from the feedback signal of $V_{C\_}$.
4) $G_{HC}(s)$ is included in the three-phase current loop to compensate second order harmonics in output ac currents.

It can be seen that the control system of the improved neutral leg does not need any extra hardware compared to conventional neutral legs. It is worth mentioning that the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification

proposed control scheme only considers a single grid-forming inverter with fixed amplitude and phase angle of output three-phase voltages like [36]. For multiple grid-forming inverters in parallel operation, the widely-used droop control methods, such as the method presented in [37], can be adopted to generate the references of voltage amplitude and phase angle. The control design is detailed next.

A. Control Scheme of the Improved Neutral Leg

This consists of two control loops: inner current loop and outer voltage loop.

1) Inner Current Loop:

Like the conventional neutral leg, the inner current loop of the improved neutral leg receives output signal of the voltage loop and the measured neutral current as reference signals to control the average voltage on C_- and provide neutral current to the load. A simple proportional-integral (PI)-resonant controller is used:

$$G_{iN}(\mathrm{s}) = K_{iN}(1 + \frac{1}{\tau_{iN}s} + \frac{1}{\tau_{riN}}\frac{s}{s^2+\omega_0^2}) \tag{31}$$

where K_{iN} is the proportional gain; τ_{iN} and τ_{rN} are the time constants of the integrator and the resonant term; ω_0 is the fundamental angular frequency.

To achieve power decoupling (i.e. to reduce second-order ripples on the dc bus), a decoupling current is added as another reference signal for the current loop. The dc-bus current i_{DC} is firstly calculated:

$$i_{DC} = \frac{v_a i_{La} + v_b i_{L_b} + v_c i_{L_c}}{V_{DC}} \tag{32}$$

The second-order ripple in i_{DC} is extracted using a resonant filter $G_{filter}(s)$:

$$G_{filter}(s) = \frac{2\xi_1(2\omega_0)s}{s^2 + 2\xi_1(2\omega_0)s + (2\omega_0)^2} \tag{33}$$

where $\xi_1 = 0.3$ defines the cutoff frequency of the resonant filter.

According to (16), the extracted second-order ripple of i_{DC} is multiplied by 2 as shown in Fig. 6 to obtain the decoupling current i_{de}. A second-order resonant controller is used as the decoupling controller to provide the decoupling current through the improved neutral leg:

$$G_{de}(\mathrm{s}) = \frac{K_{iN}}{\tau_{de}}\frac{s}{s^2+(2\omega_0)^2} \tag{34}$$

where τ_{de} is the time constant of the resonant controller.

The block diagram of the current loop for the improved neutral leg is shown in Fig. 8, where e^{-sT_d} represents the delay caused by the PWM and digital computation processes [38]. The forward open loop transfer function of the block diagram can be derived as:

$$\begin{aligned} G_{FW\_iN}(s) &= (G_{iN}(s) + G_{de}(s))e^{-sT_d}\frac{V_{DC}}{2(sL_N + R_p)} \\ &= \frac{K_{iN}V_{DC}}{2(sL_N+R_p)}e^{-sT_d}(1 + \frac{1}{\tau_{iN}s} + \frac{1}{\tau_{rN}}\frac{s}{s^2+\omega_0^2} \\ &\quad + \frac{1}{\tau_{de}}\frac{s}{s^2+(2\omega_0)^2}) \end{aligned} \tag{35}$$

The cross-over angular frequency ω_{c_iN}, proportional gain K_{iN} and time constants (τ_{iN}, τ_{rN}, τ_{de}) can be calculated according to [39]:

$$\begin{cases} \omega_{c\_iN} = \frac{\pi/2 - \phi_{m\_iN}}{T_d} \\ K_{iN} = 2\omega_{c\_iN}L_N/V_{DC} \\ \tau_{iN} = \tau_{rN} = \tau_{de} = 30/\omega_{c\_iN} \end{cases} \tag{36}$$

where ϕ_{m_iN} is the desired phase margin of the current loop. The controller parameters are summarized in Table II. The bode plot of the current loop for the improved neutral leg is shown in Fig. 9, which shows that the current loop is stable with a phase margin of 57°.

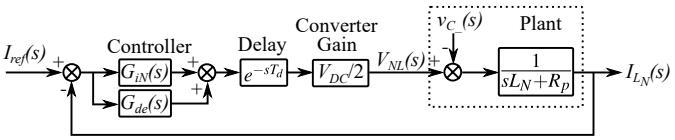


Fig. 8. Block diagram of the current loop for the improved neutral leg.

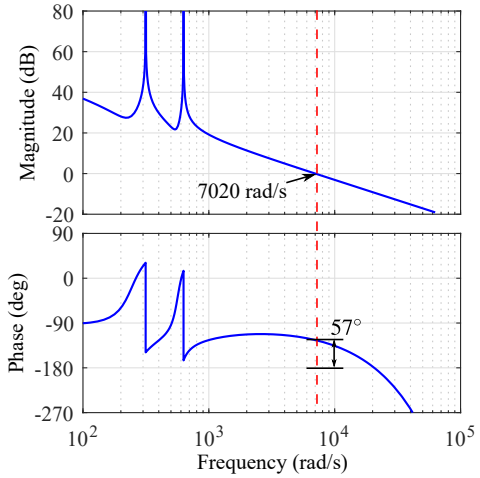


Fig. 9. Bode plot of the current loop for the improved neutral leg.

2) Outer Voltage Loop:

The outer voltage loop of the improved neutral leg aims to control the average dc voltage on C_- to be $\frac{V_{DC}}{2}$. The block diagram of the outer voltage loop is shown in Fig. 10. Since second-order decoupling current is injected into C_-, second-order voltage ripple exists on $V_{C\_}$. Therefore, a notch filter $G_{notch}(s)$ is added in the feedback path to remove the second-order ripple from the measured $V_{C\_}$:

$$G_{notch}(s) = \frac{s^2 + (2\omega_0)^2}{s^2 + 2\xi_2(2\omega_0)s + (2\omega_0)^2} \tag{37}$$

where $\xi_2 = 0.3$ defines the cutoff frequency of the notch filter.

A PI controller $G_{vN}(s)$ is used in the voltage loop:

$$G_{vN}(\mathrm{s}) = K_{vN}(1 + \frac{1}{\tau_{vN}s}) \tag{38}$$

The close-loop transfer function of current loop can be derived from the (35):

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification

$$G_{cl\_N}(s) = \frac{G_{FW\_iN}(s)}{G_{FW\_iN}(s)+1} \tag{39}$$

The open loop transfer function of the voltage loop can be derived as:

$$\begin{aligned} G_{FW\_vN}(s) &= \frac{G_{vN}(s)G_{cl\_N}(s)G_{notch}(s)}{sC_{-}} \\ &= \frac{K_{vN}}{sC_{-}}(1+\frac{1}{\tau_{vN}s}) \times \frac{G_{FW\_iN}(s)}{G_{FW\_iN}(s)+1} \\ &\times \frac{s^2+(2\omega_0)^2}{s^2+2\xi_2(2\omega_0)s+(2\omega_0)^2} \end{aligned} \tag{40}$$

The controller parameters K_{vN} and τ_{vN} are tuned based on the frequency response of the open loop transfer function to ensure a stable system with sufficient phase margin [40]. The controller parameters are summarized in Table II. The bode plot of the voltage loop for the improved neutral leg is shown in Fig. 11, which shows that the voltage loop is stable with a phase margin of 23°.

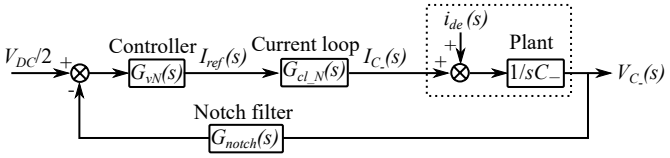


Fig. 10. Block diagram of the current loop for the improved neutral leg.

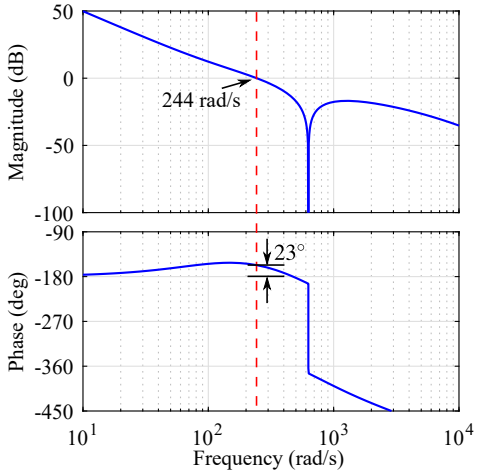


Fig. 11. Bode plot of the voltage loop for the improved neutral leg.

B. Control of the Three-phase Inverter

The three-phase four-wire inverter operates in an autonomous mode to provide balanced three-phase voltages for unbalanced three-phase loads. Thus, the three-phase currents are unbalanced. A cascaded controller is used with an outer ac voltage loop and an inner current loop. The three phases are independently controlled using proportional-resonant (PR) controllers for both current and voltage to improve power quality. The structure of these PR controllers is given as

$$G_{vph}(s) = K_{vph}(1+\frac{1}{\tau_{rvph}}\frac{s}{s^2+\omega_0^2}) \tag{41}$$

$$G_{iph}(s) = K_{iph}(1+\frac{1}{\tau_{riph}}\frac{s}{s^2+\omega_0^2}) \tag{42}$$

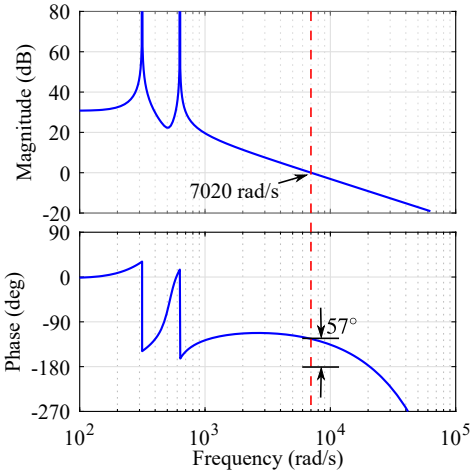
where K_{vph} and K_{iph} are the proportional gains of the voltage and current controller, respectively; τ_{rvph} and τ_{riph} are the time constants of the resonant integrator in the voltage and current controllers, respectively.

In addition, the second order harmonics need to be compensated by the current controller due to the voltage variation of the neutral point caused by the power decoupling controller $G_{de}(s)$. Therefore, as shown in Fig. 6, a harmonic compensator is connected in parallel with $G_{i\_ph}(s)$ to compensate the current harmonics at 100 Hz

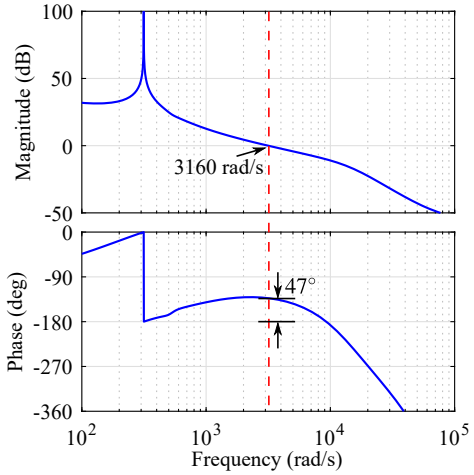
$$G_{HC}(s) = \frac{K_{iph}}{\tau_{HC}}\frac{s}{s^2+(2\omega_0)^2} \tag{43}$$

where τ_{HC} defines the time constant of the resonant integrator of the controller.

The tuning of the parameters for the controllers of the three-phase inverter is the same as that of the conventional three-phase inverter [41]. The parameters of the controllers are summarized in Table. II. The bode plots of the current and voltage loops of the three-phase inverter are presented in Fig. 12.



(a) Current loop.



(b) Voltage loop.

Fig. 12. Bode plots of the three-phase inverter.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification

TABLE I
PARAMETERS OF THE SIMULATION MODEL AND THE EXPERIMENTAL TEST-RIG.

Parameter	Value	Parameter	Value
AC filter inductor L_a, L_b, L_c	2.5 mH	AC filter capacitor C_a, C_b, C_c	20 μF
Neutral inductor L_N	2.5 mH	Neutral capacitor C_+ and C_-	100 μF
DC-bus voltage V_{DC}	750 V	Output phase voltage V_{abc}	230 Vrms
Maximum phase current I_{abc}	5 Arms	Maximum output power P_o	3 kW
Output frequency f_0	50 Hz	Switching frequency f_{sw}	20 kHz

TABLE II
PARAMETERS OF CONTROLLERS FOR SIMULATION AND EXPERIMENT.

	Controller	Parameter	Value
Neutral leg controller	Current controller $G_{iN}(s)$	K_{iN}	0.0465
		τ_{iN}	0.0042
		τ_{riN}	0.0042
	Decoupling controller $G_{de}(s)$	τ_{de}	0.0042
	Voltage controller $G_{vN}(s)$	K_{vN}	0.0260
		τ_{vN}	0.00980
Phase leg controller	Current controller $G_{iph}(s)$	K_{iph}	0.0465
		τ_{iph}	0.00280
	Harmonic compensator $G_{HC}(s)$	τ_{HC}	0.00280
	Voltage controller $G_{vph}(s)$	K_{vph}	0.0621
		τ_{vph}	0.000966

V. SIMULATION AND EXPERIMENTAL RESULTS

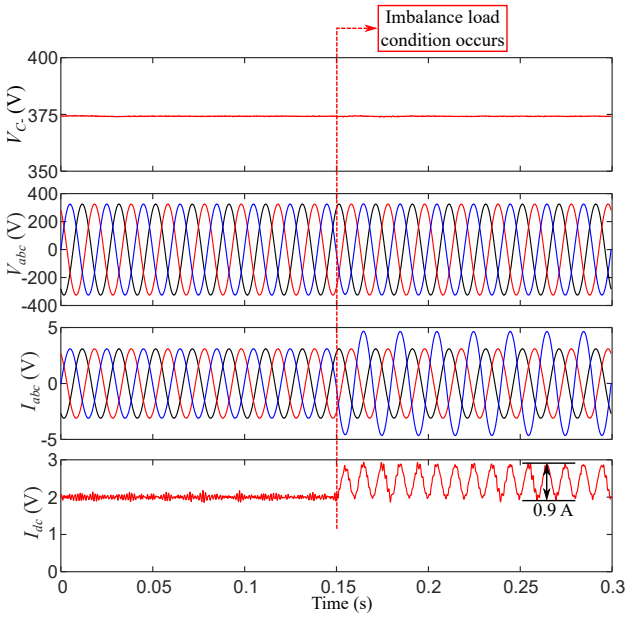
A. Simulation Results

1) Transient Simulation:

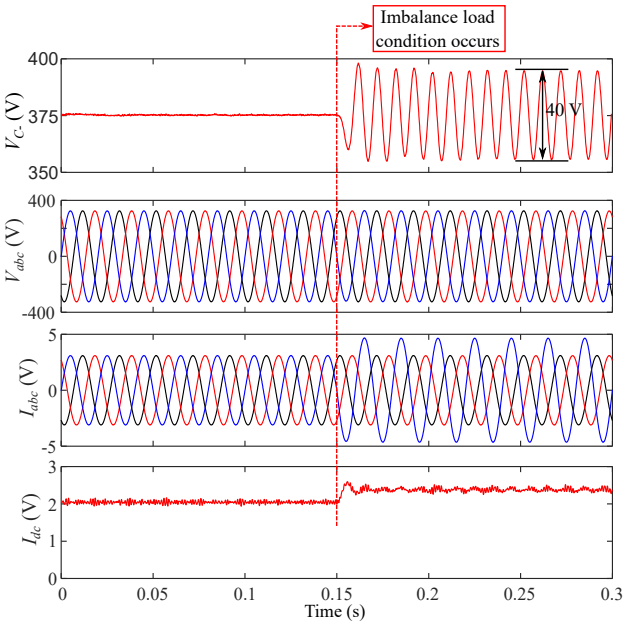
The capabilities of the improved neutral leg to provide neutral current and to reduce the second order current ripple in the dc bus were verified by transient simulation using PLECS. Performance was compared against that exhibited by a conventional leg. The simulation parameters are presented in Table I. The parameters of the controllers presented in Section IV and Fig. 6 are summarized in Table II. Simulation results are presented in Fig. 13.

Fig. 13a presents the simulated transient response of the conventional neutral leg when the load changes from balance condition ($R_a = R_b = R_c = 105\,\Omega$) to imbalance condition ($R_a = R_b = 105\,\Omega$, $R_c = 70\,\Omega$) at 0.15 s. It can be observed in the simulation result that the three-phase load currents I_{abc} respond to the step change instantly and smoothly to provide unbalance loads with neutral current. The three-phase voltages V_{abc} remain balance and the neutral point voltage $V_{C\_}$ remain constant at 375 V when the step change occurs. Due to the imbalance load condition, second-order current ripple can be observed in the dc bus current I_{dc} after the imbalance load condition occurs. The amplitude of the second-order dc-bus current ripple in simulation is 0.9 A.

Fig. 13a presents the simulated transient response of the improved neutral leg when the load changes from balance condition ($R_a = R_b = R_c = 105\,\Omega$) to imbalance condition ($R_a = R_b = 105\,\Omega$, $R_c = 70\,\Omega$) at 0.15 s. The transient responses of the three-phase currents I_{abc} and voltages V_{abc} are the same as those of the conventional neutral leg, which proves that the improved neutral leg has the same capability as the conventional one to provide the imbalance loads with neutral current. Differences between the improved neutral and conventional neutral legs can be observed from the waveforms of neutral point voltage $V_{C\_}$ and dc bus current I_{dc}. In Fig. 13a, after the imbalance condition occurs, the second-order ripples are transferred from the dc bus to the neutral capacitor C_- through active decoupling control of the improved neutral leg. As a result, the second-order ripples in the dc bus current are significantly reduced and second-order voltage ripple can be observed in $V_{C\_}$. The amplitude of the second-order voltage ripple in $V_{C\_}$ is 40 V in simulation.



(a) With conventional neutral leg.



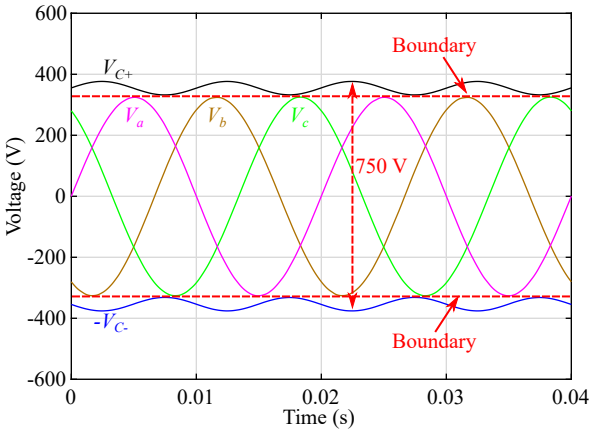
(b) With improved neutral leg.

Fig. 13. Simulation results of inverters with conventional and improved neutral legs.

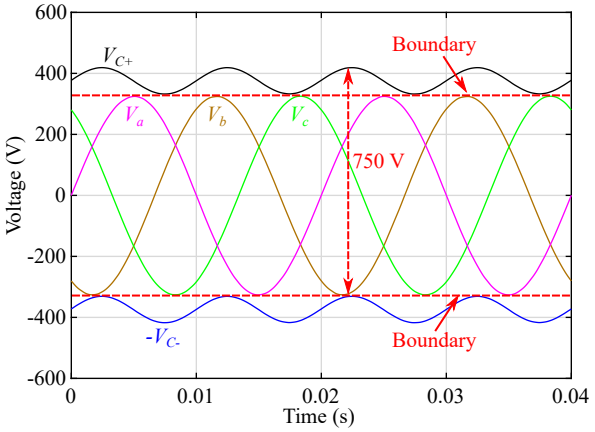
2) Verification of Capacitance Requirement:

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification

The capacitance requirements for the conventional and improved neutral legs have been calculated by (11) and (19), respectively. The equations are verified by simulation in PLCES. The output power P_o is set as 2 kW with an imbalance factor of 0.5. The maximum dc bus voltage V_{max} is set as 750 V. Three-phase load voltages are set as 230 Vrms. The output frequency is 50 Hz. According to (11) and (19), the minimum required total capacitance is 183 μF for the conventional neutral leg and 85 μF for the improved neutral leg under this scenario. The improved neutral leg requires 54% less capacitance. The calculated capacitance were used as the simulation parameters for the conventional and improved neutral legs in PLECS. The simulation results of the voltage ripples on the neutral capacitors V_{C_+} and V_{C_-} are presented in Fig. 14. It is shown that both the conventional and improved neutral legs reach the voltage boundary defined by (6), which verified the effectiveness of the calculated capacitance requirement in (11) and (19). According to Fig. 14, it is relevant to mention that the capacitor voltage V_{C_-} in the improved neutral leg has larger second-order ripple compared to that in the conventional neutral leg. The selection of the voltage rating for the capacitors needs to consider enough safe margin for the second-order ripple.



(a) Conventional neutral leg.



(b) Improved neutral leg.

Fig. 14. Verification of capacitance requirement in Simulation.

TABLE III
SPECIFICATIONS OF NEUTRAL-LEG CAPACITORS.

Type	Polypropylene capacitor
Part No.	C4AQLBW6100A3MK
Manufacturer	KEMET
Dimension (W × L × H, mm)	30 × 57.5 × 45
Capacitance	100 μF
Rated DC voltage	500 V

B. Experimental Results

The capabilities of the improved neutral leg to provide neutral current and to reduce the second order current ripple in the dc bus were experimentally verified using an 3-kW experimental platform. Performance was compared against that exhibited by a conventional leg. The experimental setup is presented in Fig. 15. The three-phase inverter with the improved neutral leg was built with SiC MOSFETs (C2M0080120D) and SiC Schottky diodes (C4D20120D). It was controlled by a DSP (Xilinx Zynq 7030 SoC) with a switching frequency of 20 kHz. Parameters of the experimental test-rig are summarized in Table I. The inverter was operated at autonomous mode to supply three-phase balanced voltage to loads. The ac output voltage was restricted to 230 Vrms at 50 Hz. Three resistors were connected to the ac output terminals as the loads. The maximum output power was 3 kW. The dc bus voltage is supplied by a dc voltage source to ensure it is constant and only the second order current ripple is exhibited on the dc bus. As shown in Fig. 6 and Fig. 7, the three-phase four-wire inverter with the improved neutral leg requires the same number of sensors (5 voltage hall sensors [42] and 5 current hall sensors [43]) as the inverter with the conventional neutral leg. Therefore, the improved neutral leg does not increase the cost of sensors. The voltage and current signals were measured by hall sensors and sent to the ADC channel of DSP through RJ45 cables.

Fig. 16 shows the capacitors used in the conventional and improved neutral legs. In the conventional leg, two 100 μF capacitors are connected in series while the improved leg only requires one 100 μF capacitor. This is consistent with the discussion in Section III, where it was shown that a 50% reduction of capacitance can be afforded in the improved configuration without compromising the capabilities to provide neutral current. The specifications of the capacitors are summarised in Table III.

Although the capacitor used in the experiment is small for a 3-kW inverter, larger capacitors will be required for inverters with a higher power rating and the significance of the improved neutral leg for reducing capacitance will be more obvious. As shown in Fig. 3, the volume of the dc capacitors accounts for 70% of the total volume of the main passive components in the conventional neutral leg. In this case, the 50% reduction of dc capacitors brought by the improved neutral leg have a significant contribution to the total volume reduction. It is shown in Fig. 3 that the improved neutral leg can reduce the volume of the passive components by 34% for a 10-kW inverter.

1) Steady-State Performance:

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification

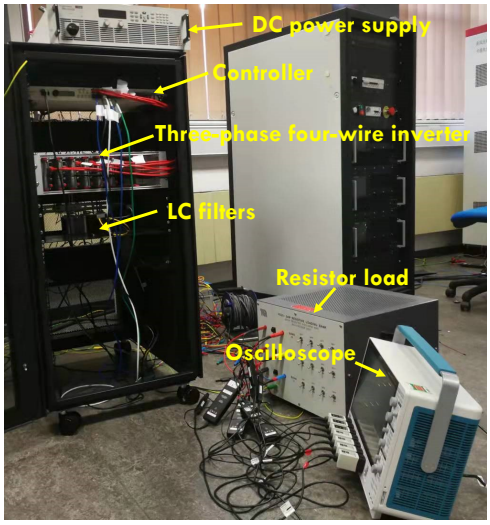


Fig. 15. Experimental setup of the three-phase four-wire inverter.

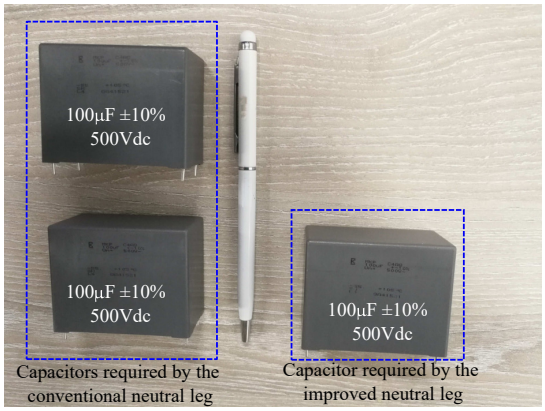
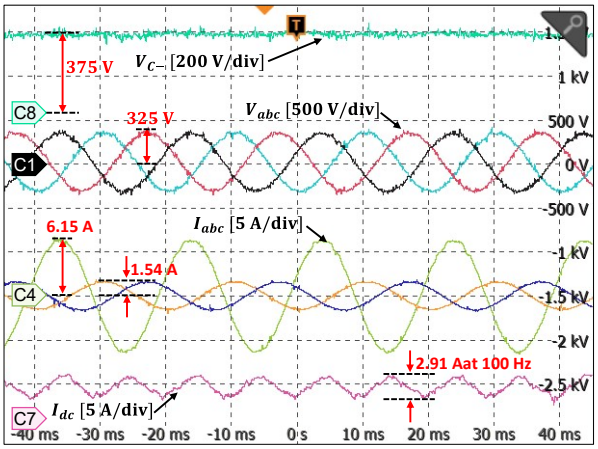
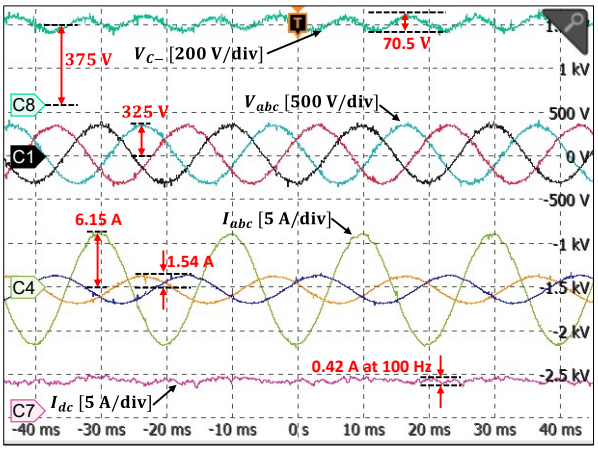


Fig. 16. Size comparison of the capacitors used in the conventional (left) and improved (right) neutral legs.



(a) Experimental results of the conventional neutral leg.



(b) Experimental results of the improved neutral leg.

Fig. 17. Steady-state performance of three-phase four-wire inverters under imbalance load condition ($R_a = 51\,\Omega$, $R_b = R_c = 210\,\Omega$).

Firstly, the steady-state waveforms of the three-phase four-wire inverter with the conventional neutral leg were measured and presented in Fig. 17a. The voltages and currents were measured with a Tektronix MSO58 oscilloscope. The load condition is $R_a = 51\,\Omega$, $R_b = R_c = 210\,\Omega$. The imbalance factor is 0.5 and output power is 1.5 kW. It is shown that, the load voltages were balanced due to the close-loop control of three-phase voltage. The load currents were unbalanced due to unbalanced loads. The neutral current I_N was provided by the neutral inductor L_N instead of the neutral capacitors because there is no 50 Hz voltage ripple on $V_{C\_}$. This is apparent from the FFT spectrum in Fig. 18, which exhibits a negligible 50 Hz component in $V_{C\_}$. As shown in Fig. 17a and Fig. 19, the dc source current I_{DC} features large second order harmonics due to the unbalanced load currents.

Secondly, the steady-state waveforms of the three-phase four-wire inverter with the improved neutral leg were measured and presented in Fig. 17b under the same load condition. It is shown that the improved neutral leg can provide the same functions as the conventional neutral leg: 1) the inverter with the improved neutral leg can provide the same balanced three-phase voltages and imbalance three-phase currents to the loads; 2) the neutral current is still provided by the improved neutral leg instead of the neutral capacitor because there is no 50 Hz voltage ripple on $V_{C\_}$ as shown in the FFT spectrum in Fig. 18. In addition to the above functions, the improved neutral leg can provide a new function to reduce the second-order ripples in the dc bus. It is shown that the dc source current ripples in Fig. 17b were significantly reduced, compared to waveforms in Fig. 17a. In turn, the FFT analysis in Fig. 19 shows that the second order harmonics in the dc source current are reduced by 86% when the improved neutral leg is adopted. However, as a consequence, the capacitor voltage $V_{C\_}$ in the improved neutral leg contained second order voltage ripples, as shown in Fig. 17b and Fig. 18. Despite this shortcoming, the load voltages and currents were not affected. As shown in Fig. 20, the total THD of the load voltage of Phase C was 0.874% without power decoupling control and 0.864% with power decoupling control.

2) Transient Performance:

Fig. 21 presents the transient response of the decoupling controller in the improved neutral leg. The load condition is $R_a = 51\,\Omega$, $R_b = R_c = 210\,\Omega$. The decoupling controller is described is Fig. 6, which is responsible for the reduction of second-order ripples in the dc bus. It is shown that before

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification

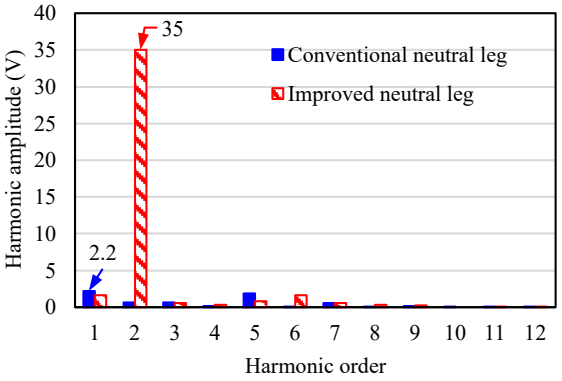


Fig. 18. FFT analysis of capacitor voltage $V_{C\_}$.

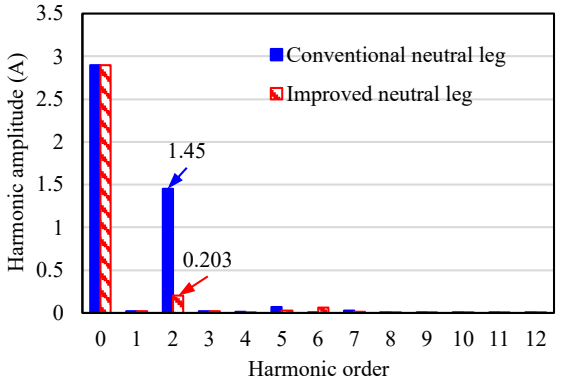


Fig. 19. FFT analysis of I_{dc}.

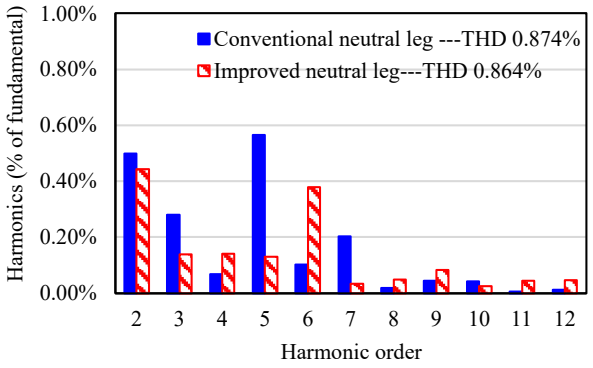


Fig. 20. FFT analysis of load voltage V_a.

the decoupling controller is enabled, the improved neutral leg works exactly as the conventional neutral leg, i.e., second-order ripples can be observed in the dc bus current. After the improved neutral leg is enabled, second-order ripple in the dc bus current is significantly reduced and the three-phase output voltages and currents are not affected. It is shown that the transient response is very fast (within one fundamental cycle).

Fig. 22a presents the transient response of the conventional neutral leg when the load changes from balance condition ($R_a = R_b = R_c = 105\,\Omega$) to imbalance condition ($R_a = R_b = 105\,\Omega$, $R_c = 70\,\Omega$) in experiment. The experimental performance is the same as the simulation performance presented in Fig. 13a. Second-order current ripple can be observed in the dc bus current I_{dc} after the imbalance load condition occurs. The amplitude of the second-order dc-bus

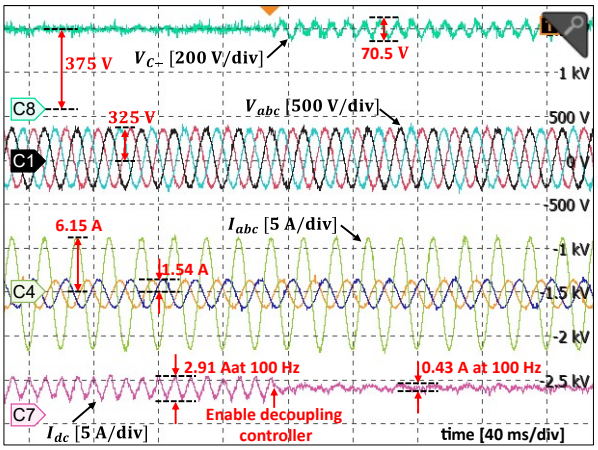
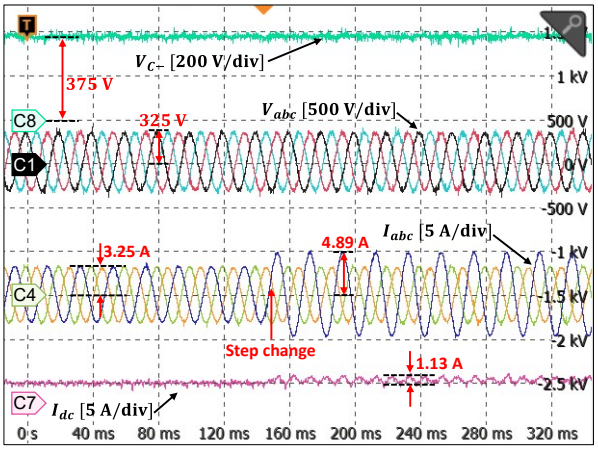
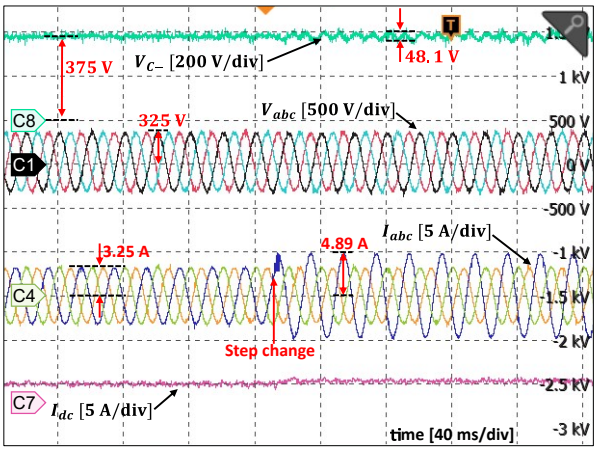


Fig. 21. Transient response of the decoupling controller in the improved neutral leg.



(a) With conventional neutral leg.



(b) With improved neutral leg.

Fig. 22. Transient response of inverters with conventional and improved neutral legs in experiment. Step load change from balance condition ($R_a = R_b = R_c = 105\,\Omega$) to imbalance condition ($R_a = R_b = 105\,\Omega$, $R_c = 70\,\Omega$).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification

current ripple in experiment is 1.13 A. This is slightly higher than the simulation result (0.9 A) in Fig. 13a. The difference is caused by the noises and nonlinearity of the experimental system.

Fig. 22b presents the transient response of the improved neutral leg when the load changes from balance condition ($R_a = R_b = R_c = 105\,\Omega$) to imbalance condition ($R_a = R_b = 105\,\Omega$, $R_c = 70\,\Omega$) in experiment. The experimental performance is the same as the simulation performance presented in Fig. 13b. Second-order ripple is transferred from the dc bus to C_- by the active decoupling control of the improved neutral leg. The amplitude of the second order voltage ripple observed from C_- is 48.1 V. This is slightly higher than the simulation result (40 V) in Fig. 13b. The difference is caused by the noises and nonlinearity of the experimental system.

VI. Comparisons between Conventional and Improved Neutral Legs

In this section, a comparative study is made between the improved and the conventional neutral legs in terms of efficiency, size of neutral inductors, and fault tolerance capabilities.

A. Efficiency

The improved neutral leg suffers higher current stress than the conventional neutral leg due to the additional decoupling current. As a consequence, the inverter efficiency will be affected. However, as highlighted in the introduction, all active decoupling methods inherently lead to more power losses because of the additional semiconductors and current stress [44] [45].

For comparison, the efficiencies were measured for three-phase four-wire inverters with conventional and improved neutral legs, respectively. The efficiencies were measured by a Yokogawa WT1806 power analyzer. Note that the power losses of the digital controller, gate drivers and cooling fans were not measured. In order to have a better representation of the efficiency performance, three different scenarios are considered as shown in Fig. 23.

Fig. 23a compares the efficiencies under balance condition, which shows that the inverters with conventional and improved neutral legs have almost the same efficiency. This is because there are no second-order ripples under balance condition and thus the improved neutral leg works the same as the conventional neutral leg.

Fig. 23b compares the efficiencies with fixed output power of 2 kW and different imbalance factors. It is shown that, as the imbalance factor increases, efficiencies of inverters with both conventional and improved neutral legs decrease. However, the inverter with the improved neutral leg presents lower efficiency than the inverter with the conventional neutral leg. As expected, the efficiency of the inverter with the improved neutral leg is lower than that of the inverter with the conventional neutral leg due to additional current stress induced by the decoupling current. As the losses of the neutral leg cannot be measured separately, they were simulated in PLECS. The PLECS models of SiC MOSFETs (C2M0080120D) and SiC diodes (C4D20120D) are provided by Wolfspeed [46]. The simulation results are presented in Fig. 23c, which shows that the improved neutral leg presents higher losses due to higher current stress compared to the conventional neutral leg.

Fig. 23d compares the efficiencies under imbalance condition, with imbalance factor of 0.5. It is shown that the efficiency drop increases with output power due to the increased current stress of the improved neutral leg. However, thanks to the adoption of SiC MOSFETs, the maximum efficiency drop is only 0.6% with imbalance factor of 0.5 and output power of 2 kW. Such a small efficiency drop can be compromised by the benefit of significant capacitance reduction.

The decreased efficiency caused by the improved neutral leg need to be considered for the thermal design of the inverter, such as sizing of the heat sink. Therefore, system-level optimization is required for the converter to achieve optimal power density, efficiency and cost [47]. However, this optimization aspect is out of the scope of the current paper as the main focus of this paper is to prove the viability of the proposed topology and its control strategy. Further development will be focused on to improve the efficiency and optimize the power density of the whole inverter.

B. Current Stresses of Switches and Inductor in the Neutral Leg

The neutral leg switches and the neutral inductor have the same current stress as they are connected in series. Therefore, the current stress is compared in terms of switching ripples and RMS value of neutral inductor current i_{L_N}.

For both the improved and the conventional neutral legs, the ripple of i_{L_N} is given as

$$\Delta i_N = \frac{V_{DC} - V_{C_-}}{L_N} \cdot \frac{D}{f_{sw}} \tag{44}$$

where D is the duty cycle of the upper switch of the neutral legs and f_{sw} is the switching frequency. For the same value of L_N and f_{sw}, the current ripple of the improved leg is almost the same as that of the conventional neutral leg.

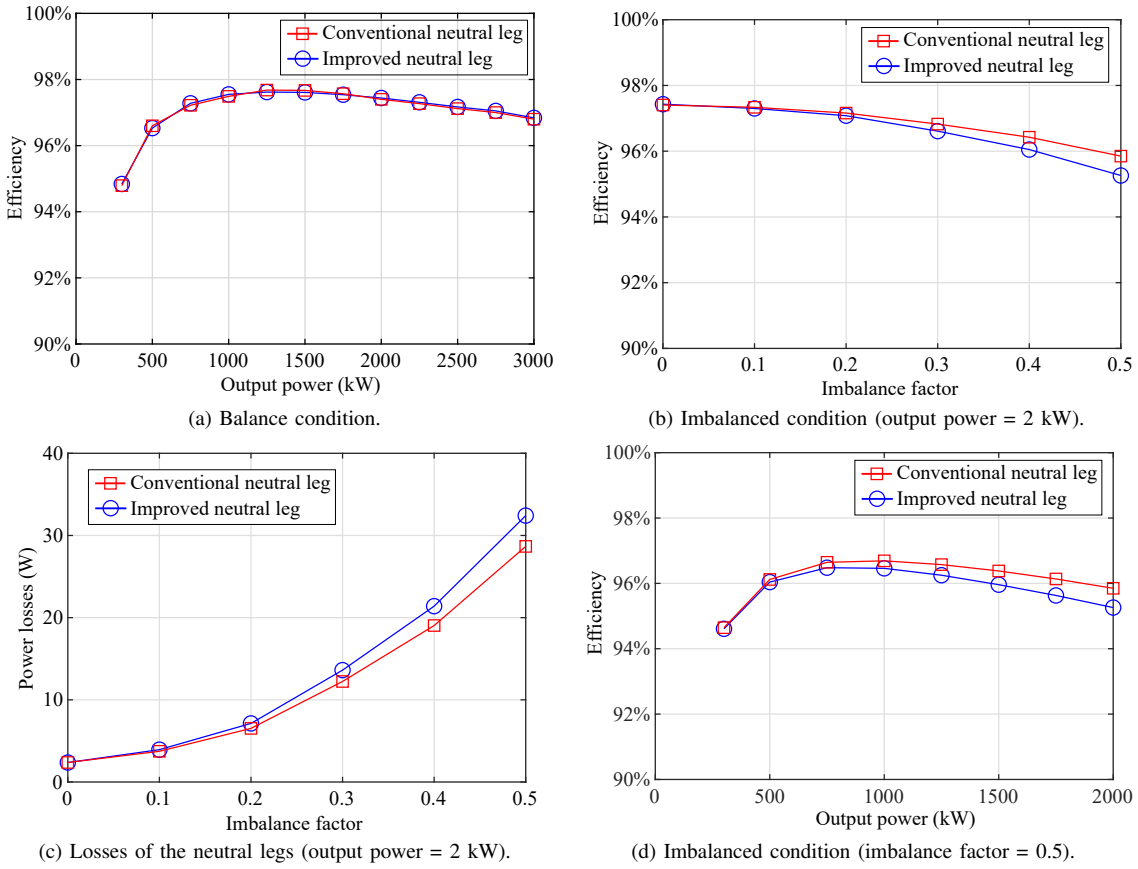
In terms of RMS current, since the improved leg needs to provide additional decoupling current i_{de}, the RMS current in the improved neutral leg is higher than that in the conventional leg. Therefore, the improved neutral leg has higher current stress. This is simulated and shown in Fig. 24 for different imbalance factors. It is shown that the current stress gets higher as the imbalance factor increases. When the imbalance factor is 0.5, the improved leg has 1.2 times higher current stress than the conventional one.

As a result, the neutral inductor in the improved leg should be designed with a higher current rating. The size of the neutral inductor will increase as a result and can be considered proportional to the energy stored in the inductor [48]:

$$S_L \propto L I_{RMS}^2 \tag{45}$$

where S_L represents the size of inductor. Since similar value of neutral inductance is used in both neutral legs, the size of the inductor is determined by the RMS value of the inductor current. As shown in Fig. 24, the RMS value of the inductor current in the improved leg is 1.2 times higher

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification



(a) Balance condition.

(b) Imbalanced condition (output power = 2 kW).

(c) Losses of the neutral legs (output power = 2 kW).

(d) Imbalanced condition (imbalance factor = 0.5).

Fig. 23. Efficiency of three-phase four-wire inverters with conventional and improved neutral legs.

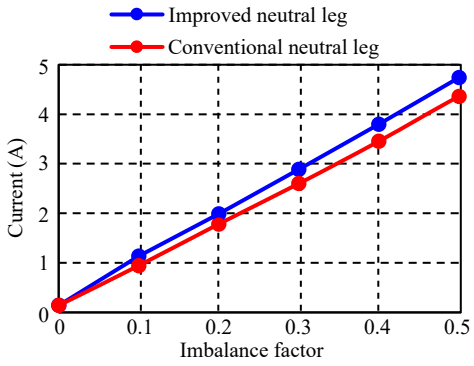


Fig. 24. Current stress of the neutral legs (output power = 2 kW).

than that in the conventional one. Therefore, the size of the neutral inductor in the improved leg should be 1.4 times higher than in its conventional counterpart. However, with the introduction of SiC MOSFETs in the neutral leg, the size of the neutral inductor can be substantially reduced by increasing the switching frequency. As shown in Fig. 3, the size of the inductor is insignificant compared to that of the DC capacitors. Therefore, despite the increased inductor size, the improved leg would still feature a higher power density compared to the conventional neutral leg by reducing the capacitance.

C. RMS Current of Neutral Capacitors

In the proposed neutral leg, second-order decoupling current i_{de} is injected into the neutral capacitor to reduce the second-order ripples on the dc bus. The amplitude of the capacitor current $I_{C\_}$ is equal to I_{de} and can be obtained from (16):

$$I_{C\_} = I_{de} = \frac{2\delta P_o}{V_{DC}} \tag{46}$$

The RMS value of the capacitor current can be calculated as:

$$I_{C\_,RMS} = \frac{I_{C\_}}{\sqrt{2}} = \frac{\sqrt{2}\delta P_o}{V_{DC}} \tag{47}$$

As a result, the capacitor RMS current increases with the output power and imbalance factor of the inverter.

In the conventional neutral leg, since there is no current injected to the neutral capacitors and the neutral current is fully provided by the neutral leg instead of capacitors, the capacitor RMS current is zero if the switching ripples are ignored.

The current waveforms of the neutral capacitors in the improved neutral leg and the conventional neutral leg are measured and presented in Fig. 25 and Fig. 26, respectively. To clearly observe the second-order ripple current injected by the proposed neutral leg, a low pass filter (cutoff frequency = 5 kHz) is applied in the Oscilloscope to remove the switching harmonics from the current waveform. The load condition is $R_a = 52\,\Omega$, $R_b = R_c = 210\,\Omega$. Therefore, the output power and imbalance factor of the inverter are 1.5 kW and 0.5, respectively.

According to (47), the RMS current of the improved neutral capacitor can be calculated as 1.414 A. As shown in Fig. 25, the measured RMS value of the capacitor current of the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification

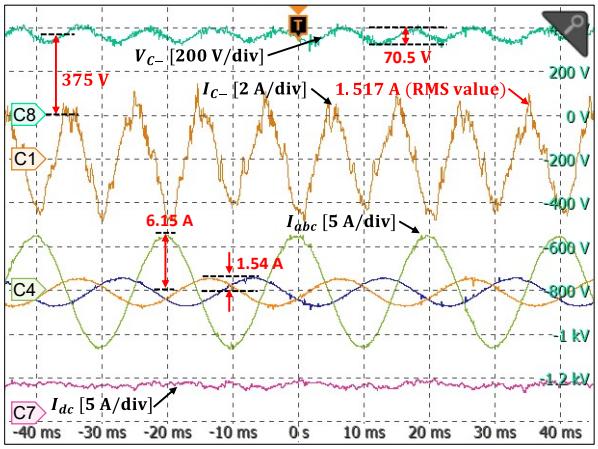


Fig. 25. Capacitor current waveform (C1) of the improved neutral leg.

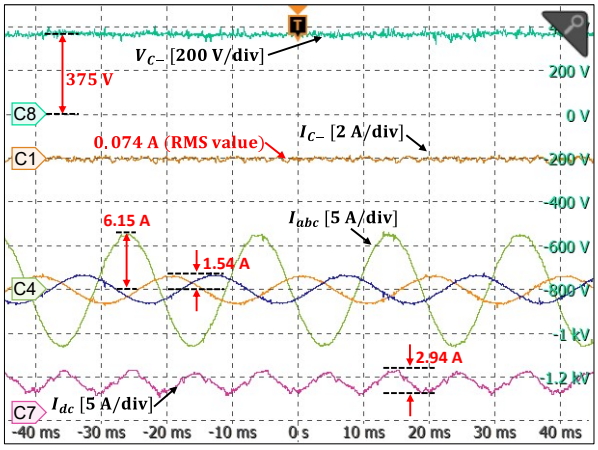


Fig. 26. Capacitor current waveform (C1) of the conventional neutral leg.

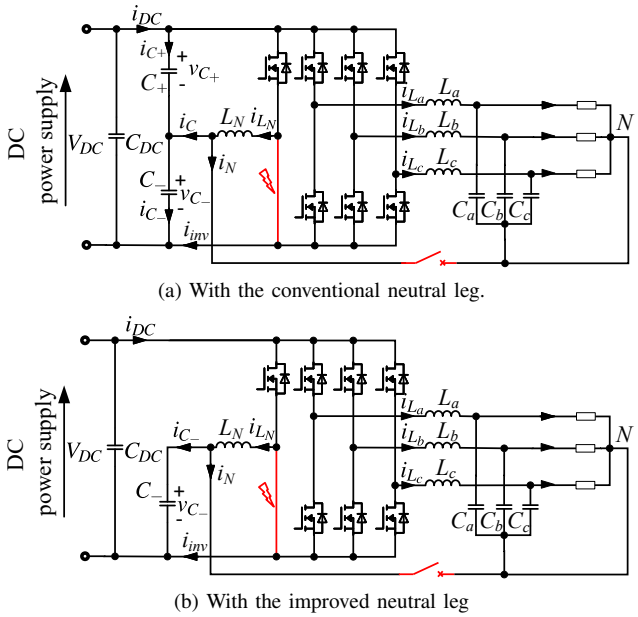
improved neutral leg is 1.517A. The measured results are close to the theoretical result.

As a comparison, the current waveform of the neutral capacitors in the conventional neutral leg is presented in Fig. 26. Because there is no current injected from the conventional neutral leg, the RMS value of the capacitor current is only 0.074 A, which is almost zero. This result is consistent with the theoretical analysis above.

D. Fault Tolerance

The most vulnerable components in neutral legs are the two semiconductor switches [49]. Apart from degradation, these switches mainly exhibit two serious failure modes: short-circuit failure and open-circuit failure.

For a short-circuit failure, the three-phase four-wire inverter with either types of neutral leg cannot operate because the neutral point voltage will be clamped to either the positive or the negative dc bus voltage. Fig. 27 shows the equivalent circuit of the three-phase inverter with two neutral leg configurations when a short-circuit failure occurs on the lower switch. In this case, the neutral point is clamped to the negative dc bus through the neutral inductor for either configuration and the circuit breaker in the neutral wire needs to be immediately



(a) With the conventional neutral leg.

(b) With the improved neutral leg

Fig. 27. Three-phase four-wire inverter with neutral legs in short-circuit failure mode (lower switch).

disconnected. Afterwards, the inverters can still work for balance loads.

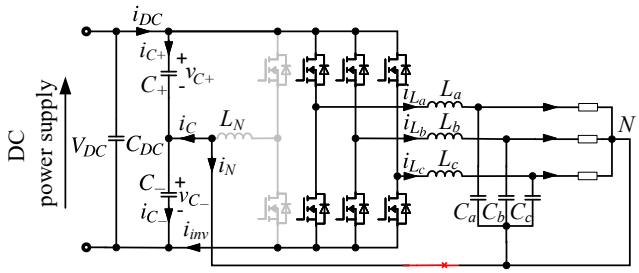
For an open-circuit failure, both the conventional and improved neutral legs are out of service and, thus, would not be able to provide neutral currents. As shown in Fig. 28, the inverter with the conventional neutral leg is equivalent to split-link topology [8]. The voltage potential of the neutral point can be inherently maintained by the series connection of the neutral capacitors. Therefore, it can still work with balanced loads. Under the presence of imbalanced loads, these neutral capacitors are too small to provide sufficient neutral current for unbalanced loads since they are not specially designed for a split-link topology. On the other hand, when an open-circuit failure occurs on the improved neutral leg, the neutral point voltage cannot be maintained. Therefore, the circuit breaker in the neutral wire should be disconnected and the inverter can continue to work in balance condition.

Overall, both neutral legs have limited fault tolerance capability for imbalance operation. And the improved neutral leg need further action of the circuit breaker when the open-circuit failure occurs.

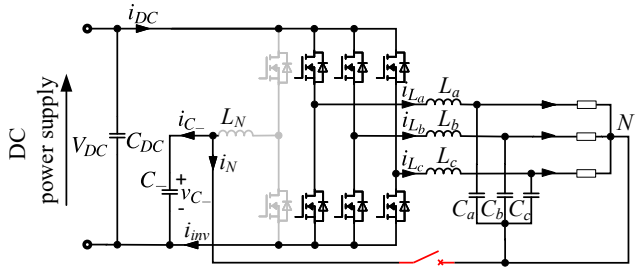
VII. Conclusions

This paper has presented an improved neutral leg, which not only provides the neutral current as its conventional counterpart, but also reduces the second order ripples and dc capacitance on the dc bus. The dc capacitance requirements of the conventional and improved neutral legs to mitigate the dc bus ripples were analyzed and compared. It is shown that due to the reduction of dc bus ripples, the improved neutral leg can decrease by 50% the dc capacitance value compared to the conventional one. Such a benefit is brought by the improved neutral leg without adding any hardware components, so there is no additional cost.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TTE.2021.3138333, IEEE Transactions on Transportation Electrification



(a) With the conventional neutral leg.



(b) With the improved neutral leg

Fig. 28. Three-phase four-wire inverter with neutral legs in open-circuit failure mode.

The aforementioned functions of the improved neutral leg were successfully achieved by two control loops, i.e., the neutral current control loop and the power decoupling control loop. Importantly, the improved neutral leg was controlled independently from the three-phase inverter. The performance of the improved neutral leg was verified by experiments. The improved neutral leg was built with SiC MOSFETs and adopted in a three-phase inverter. Both static and transient performance were evaluated. The experimental results show that the improved neutral leg can reduce the second order current ripples on the dc bus effectively, while simultaneously provides the neutral current.

Due to its satisfactory performance, the improved topology represents a good alternative for EV charger configurations that require operation in an autonomous mode to significantly reduce the dc capacitance and thereby increase the power density. The future work will focus on: i) prototypes with higher power rating and various types of other loads to validate the power density improvement; ii) improvement of efficiency; iii) design optimization of the converter including the heat sink; iv) control and operation strategy under various fault conditions.

APPENDIX

The detailed calculation method of the component size in Fig. 3 is presented in this appendix.

A. Selection of Switching Devices and Switching Frequency

A neutral leg has been designed for a three-phase inverter rated at 10 kW. The output phase-to-neutral voltage is 230 Vrms. The phase current is about 15 A. The neutral leg is designed to have the same current rating as the phase leg. To meet these requirements, the devices shown in Table IV have been adopted.

TABLE IV
DEVICES SELECTED FOR THE NEUTRAL LEG.

	Voltage rating	Current rating ($T_c = 100\,^{\circ}\mathrm{C}$)
Si IGBT (IKW25N120H3)	1200 V	25 A
SiC MOSFET (C2M0080120D)	1200 V	24 A

TABLE V
DEVICE LOSSES UNDER MAXIMUM LOAD CURRENT.

	Si IGBT (IKW25N120H3)	SiC MOSFET (C2M0080120D)
Switching frequency	20 kHz	200 kHz
Switching losses	53.59 W	45.53 W
Conduction losses	13.21 W	12.35 W
Total losses	66.80 W	57.88 W
Junction temperature	111.2 °C	117.0 °C

The switching frequency of the selected Si IGBT is set as 20 kHz, which is normally used for Si IGBTs. The switching frequency of the adopted SiC MOSFETs is selected to achieve the same power losses as the Si IGBT. The power loss model provided by the manufacturers is used to quantify the losses of the two devices under the maximum load current. Simulation results are shown in Table V, which show that with the same power losses, the SiC MOSFET can operate at 200 kHz switching frequency, which is 10 times the switching frequency for the Si IGBT.

B. Calculation of Inductor Size

The calculation of inductor size is based on the inductance value and current stress as in [50]. The inductance value can be calculated according to (44). A 2.5 mH inductance is selected for the Si-based neutral leg and a 0.25 mH inductance is selected for the SiC-based neutral leg. According to Section VI-B, conventional neutral legs with Si IGBT and SiC MOSFETs have the same current stress on the inductor, while the improved leg has around 1.2 times higher current stress on the inductor.

C. Calculation of Capacitor Size

The capacitance of the conventional and the improved neutral legs is calculated using (11) and (19), yielding 914 μF and 426 μF, respectively. Therefore, ten 100 μF film capacitors are used for the conventional and five 100 μF film capacitors for the improved leg. The 100 μF film capacitor is shown in Fig. 16. By measuring the volume of a single capacitor, the total volume is calculated.

D. Selection of Heat Sink and Cooling Fan

The heat sink and cooling fan are selected considering the power losses [51]. As shown in Table V, the power losses from the neutral leg are approximately 120 W. A maximum ambient temperature of 40 °C is considered. The case temperatures of both Si IGBTs and SiC MOSFET are controlled to a value lower than 80 °C. As similar power losses are exhibited in simulations, a similar cooling system is adopted for both neutral legs. The thermal resistance of the cooling system required by the thermal dissipation is:

$$R_{th} = (80^{\circ}\mathrm{C} - 40^{\circ}\mathrm{C})/120\mathrm{W} = 0.33\,\mathrm{K/W}. \quad (48)$$

A heat sink and cooling fan from DYNATRON (Part No. G199) is selected to meet the above requirement and the volume of the heat sink and cooling fan are obtained from the datasheet [52].

REFERENCES

[1] Q. Zhong, "Power-electronics-enabled autonomous power systems: Architecture and technical routes," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5907–5918, 2017.

[2] F. Blaabjerg, Y. Yang, D. Yang, and X. Wang, "Distributed power-generation systems and protection," *Proc. IEEE*, vol. 105, no. 7, pp. 1311–1331, 2017.

[3] S. Ghosh and S. Chattopadhyay, "Three-loop-based universal control architecture for decentralized operation of multiple inverters in an autonomous grid-interactive microgrid," *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1966–1979, 2020.

[4] V. Monteiro, J. G. Pinto, and J. L. Afonso, "Operation modes for the electric vehicle in smart grids and smart homes: Present and proposed modes," *IEEE Trans. Veh. Technol.*, vol. 65, no. 3, pp. 1007–1020, 2016.

[5] Y. Fu *et al.*, "Imbalanced load regulation based on virtual resistance of a three-phase four-wire inverter for EV vehicle-to-home applications," *IEEE Trans. Transp. Electrific.*, vol. 5, no. 1, pp. 162–173, 2019.

[6] ——, "Design methodology of a three-phase four-wire EV charger operated at the autonomous mode," *IEEE Trans. Transp. Electrific.*, vol. 5, no. 4, pp. 1169–1181, 2019.

[7] Y. Fu, Y. Huang, H. Bai, X. Lu, K. Zou, and C. Chen, "A high-efficiency SiC three-phase four-wire inverter with virtual resistor control strategy running at V2H mode," in *Proc. IEEE Wide Bandgap Power Dev. Appl. (WiPDA)*, 2018, pp. 174–179.

[8] M. Aredes, J. Hafner, and K. Heumann, "Three-phase four-wire shunt active filter control strategies," *IEEE Trans. Power Electron.*, vol. 12, no. 2, pp. 311–318, 1997.

[9] P. Verdelho and G. D. Marques, "Four-wire current-regulated PWM voltage converter," *IEEE Trans. Ind. Electron.*, vol. 45, no. 5, pp. 761–770, 1998.

[10] Q.-C. Zhong and T. Hornik, *Control of Power Inverters in Renewable Energy and Smart Grid Integration*. Wiley-IEEE Press, 2013.

[11] C. A. Quinn, N. Mohan, and H. Mehta, "A four-wire, current-controlled converter provides harmonic neutralization in three-phase, four-wire systems," in *Proc. 8th Annu. Appl. Power Electron. Conf. Expo.*, Mar. 1993, pp. 841–846.

[12] R. Zhang, V. H. Prasad, D. Boroyevich, and F. C. Lee, "Three-dimensional space vector modulation for four-leg voltage-source converters," *IEEE Trans. Power Electron.*, vol. 17, no. 3, pp. 314–326, 2002.

[13] J. Chen, T. Yang, C. O'Loughlin, and T. O'Donnell, "Neutral current minimization control for solid state transformers under unbalanced loads in distribution systems," *IEEE Trans. Ind. Electron.*, vol. 66, no. 10, pp. 8253–8262, 2019.

[14] C. Liu, J. Lai, F. Lee, D. Chen, and R. Zhang, "Common-mode components comparison for different SVM schemes in three-phase four-legged converter," in *Proc. 3rd Int. Power Electron. Motion. Control Conf. (IPEMC)*, vol. 2, 2000, pp. 633–638.

[15] Q. Zhong, J. Liang, G. Weiss, C. Feng, and T. C. Green, "H^∞ control of the neutral point in four-wire three-phase DC-AC converters," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1594–1602, 2006.

[16] T. Hornik and Q.-C. Zhong, "Parallel PI voltage–H^∞ current controller for the neutral point of a three-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1335–1343, 2013.

[17] W. Zhao, X. Ruan, D. Yang, X. Chen, and L. Jia, "Neutral point voltage ripple suppression for a three-phase four-wire inverter with an independently controlled neutral module," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2608–2619, 2017.

[18] J. Liang, T. C. Green, C. Feng, and G. Weiss, "Increasing voltage utilization in split-link, four-wire inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1562–1569, 2009.

[19] C. F. Nascimento, O. Diene, and E. H. Watanabe, "Analytical model of three-phase four-wire VSC operating as grid forming power converter under unbalanced load conditions," in *Proc. IEEE 12th Int. Conf. Power Electron. Drive Syst. (PEDS)*, Dec. 2017, pp. 1219–1224.

[20] S. Bala, T. Tengner, P. Rosenfeld, and F. Delince, "The effect of low frequency current ripple on the performance of a lithium iron phosphate (LFP) battery energy storage system," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2012, pp. 3485–3492.

[21] X. Guo, J. Li, and X. Wang, "Impact of grid and load disturbances on electric vehicle battery in G2V/V2G and V2H mode," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 5406–5410.

[22] A. R. Gautam, K. Gourav, J. M. Guerrero, and D. M. Fulwani, "Ripple mitigation with improved line-load transients response in a two-stage DC-DC-AC converter: Adaptive SMC approach," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3125–3135, 2018.

[23] C. Lim, Y. Jeong, and G. Moon, "Phase-shifted full-bridge DC-DC converter with high efficiency and high power density using center-tapped clamp circuit for battery charging in electric vehicles," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10 945–10 959, 2019.

[24] W. Lee, J. Kim, J. Lee, and I. Lee, "Design of an isolated DC/DC topology with high efficiency of over 97% for EV fast chargers," *IEEE Trans. Veh. Technol.*, vol. 68, no. 12, pp. 11 725–11 737, 2019.

[25] B. Whitaker *et al.*, "A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2606–2617, 2014.

[26] D. Patil and V. Agarwal, "Compact onboard single-phase EV battery charger with novel low-frequency ripple compensator and optimum filter design," *IEEE Trans. Veh. Technol.*, vol. 65, no. 4, pp. 1948–1956, 2016.

[27] W. Liu, K. Wang, H. S. Chung, and S. T. Chuang, "Modeling and design of series voltage compensator for reduction of DC-link capacitance in grid-tie solar inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2534–2548, 2015.

[28] C. Ren, X. Han, L. Wang, Y. Yang, W. Qin, and P. Wang, "High-performance three-phase PWM converter with a reduced DC-link capacitor under unbalanced AC voltage conditions," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1041–1050, 2018.

[29] E. H. W. H. Akagi and M. Aredes, *Instantaneous Power Theory and Applications to Power Conditioning*. Wiley-IEEE Press, 2007.

[30] Y. Liu, B. Ge, H. Abu-Rub, and D. Sun, "Comprehensive modeling of single-phase quasi-z-source photovoltaic inverter to investigate low-frequency voltage and current ripple," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4194–4202, 2015.

[31] A. J. Roscoe, S. J. Finney, and G. M. Burt, "Tradeoffs between AC power quality and DC bus ripple for 3-phase 3-wire inverter-connected devices within microgrids," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 674–688, 2011.

[32] C. F. Nascimento *et al.*, "Analysis of noncharacteristic harmonics generated by voltage-source converters operating under unbalanced voltage," *IEEE Trans. Power Del.*, vol. 32, no. 2, pp. 951–961, 2017.

[33] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690–4698, 2012.

[34] X. Zhang, Q.-C. Zhong, and W.-L. Ming, "Stabilization of a cascaded dc converter system via adding a virtual adaptive parallel impedance to the input of the load converter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1826–1832, 2016.

[35] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg, "Evaluation of current controllers for distributed power generation systems," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 654–664, 2009.

[36] Z. Li, C. Zang, P. Zeng, H. Yu, S. Li, and J. Bian, "Control of a grid-forming inverter based on sliding-mode and mixed H_2/H_∞ control," *IEEE Trans. Ind. Electron.*, vol. 64, no. 5, pp. 3862–3872, 2017.

[37] W. Du *et al.*, "A comparative study of two widely used grid-forming droop controls on microgrid small-signal stability," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 963–975, 2020.

[38] D. G. Holmes, T. A. Lipo, B. P. McGrath, and W. Y. Kong, "Optimized design of stationary frame three phase ac current regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2417–2426, 2009.

[39] B. P. McGrath, D. G. Holmes, and L. McNabb, "A signal conditioning antiwindup approach for digital stationary frame current regulators," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 6036–6046, 2019.

[40] S. D'Arco, J. A. Suul, and O. B. Fosso, "Automatic tuning of cascaded controllers for power converters using eigenvalue parametric sensitivities," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1743–1753, 2015.

[41] J. A. Suul, M. Molinas, L. Norum, and T. Undeland, "Tuning of control loops for grid connected voltage source converters," in *2008 IEEE 2nd International Power and Energy Conference*, 2008, pp. 797–802.

[42] Imperix, "Voltage sensor din-800v." [Online]. Available: https://cdn.imperix.com/wp-content/uploads/document/DIN-800V.pdf

[43] Imperix, "Current sensor din-50a." [Online]. Available: https://cdn.imperix.com/wp-content/uploads/document/DIN-50A.pdf

[44] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in pv systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, 2013.
[45] Y. Tang and F. Blaabjerg, "A component-minimized single-phase active power decoupling circuit with reduced current stress to semiconductor switches," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2905–2910, 2015.
[46] Wolfspeed, "LTspice and PLECS models." [Online]. Available: http://go.wolfspeed.com/all-models.
[47] R. M. Burkart and J. W. Kolar, "Comparative η-ρ-σ pareto optimization of Si and SiC multilevel dual-active-bridge topologies with wide input voltage range," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5258–5270, 2017.
[48] A. A. Bento, E. R. da Silva, and E. C. dos Santos, "Reducing the inductor size and current stress by interleaved bidirectional boost rectifiers used for power factor correction," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, March 2006.
[49] T. Dragičević, P. Wheeler, and F. Blaabjerg, "Artificial intelligence aided automated design for reliability of power electronic systems," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7161–7171, Aug 2019.
[50] K. Raggl, T. Nussbaumer, and J. W. Kolar, "Guideline for a simplified differential-mode emi filter design," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1031–1040, 2010.
[51] C. Gammeter, F. Krismer, and J. W. Kolar, "Weight optimization of a cooling system composed of fan and extruded-fin heat sink," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 509–520, 2015.
[52] Dynatron, "Heat sink DYNATRON G199-datasheet." [Online]. Available: https://www.dropbox.com/s/kfcd58xby6u5io9/G199-Specs-Dynatron.pdf?raw=1

Peng Yang (M'16) received the B.Sc and M.Sc degrees in electrical engineering from Tsinghua University, Beijing, China, in 2015 and 2018, respectively. From 2018 to 2021, he was a Marie Curie Early Stage Research Fellow funded by the European Union's InnoDC project. He is currently working toward the Ph.D. degree in electrical engineering at Cardiff University, UK. His research interests focus on characterization, modeling and applications of wide bandgap semiconductors in power electronics.

Wenlong Ming (M'16) received the B.Eng. and M.Eng. Degrees in Automation from Shandong University, Jinan, China, in 2007 and 2010, respectively. He received the Ph.D. degree in Automatic Control and Systems Engineering from the University of Sheffield, Sheffield, U.K., in 2015. He is the winner of the prestigious IET Control & Automation Doctoral Dissertation Prize in 2017. He has been a Senior Lecturer of Power Electronics at Cardiff University, U.K., since August 2020 and a Senior Research Fellow funded by Compound Semiconductor Applications (CSA) Catapult, U.K., for 5 years since April 2020.

He was with the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, USA in 2012 as an academic visiting scholar. He has (co-)authored more than 60 papers published in leading journals or refereed IEEE conferences. His research interests focus on packaging, characterisation, modelling and applications of wide-bandgap semiconductor power devices.

Jun Liang (M'02-SM'12) received the B.Sc. degree from Huazhong University of Science and Technology, Wuhan China in 1992, and the M.Sc. and Ph.D. degrees from China Electric Power Research Institute, Beijing China in 1995 and 1998 respectively. From 1998 to 2001, he was a Senior Engineer with China Electric Power Research Institute. From 2001 to 2005, he was a Research Associate at Imperial College, London, U.K.. From 2005 to 2007, he was a Senior Lecturer at the University of Glamorgan, U.K.. Currently, he is a Professor at the School of Engineering, Cardiff University, U.K.. He is the Chair of IEEE PELS UK&I Chapter. His research interests include DC technologies, power electronics, power system stability control, and renewable power generation.

Carlos E. Ugalde-Loo (M'02-SM'19) was born in Mexico City. He received the B.Sc. degree in electronics and communications engineering from Instituto Tecnológico y de Estudios Superiores de Monterrey, Mexico City, México, in 2002, the M.Sc. degree in electrical engineering from Instituto Politécnico Nacional, Mexico City, México, in 2005, and the Ph.D. degree in electronics and electrical engineering from the University of Glasgow, Scotland, U.K., in 2009. In 2010 he joined the School of Engineering in Cardiff University, Wales, U.K. He is currently Reader in Electrical Power Systems and Deputy Group Leader of the Centre for Integrated Renewable Energy Generation and Supply. His academic expertise includes power system stability and control, grid integration and control of renewables, dc transmission, modelling and control of integrated energy systems and multivariable control.

Rukshan Navaratne obtained his PhD in Aerospace Engineering at Cranfield University and currently working as a Reader and Leading the Aerospace Propulsion Research at Cardiff University. Before joining academia, he has spent much of his career working as an Engineer, Project Manager and Senior Executive in aerospace industry. His current research focuses on the development of novel electric propulsion systems, electrical machine modelling, and design optimisation of advanced novel propulsion systems. Rukshan use variety of numerical and experimental tools and techniques to develop propulsion technologies from initial conception through increasing levels of technology readiness with a constant view towards commercialization and real-world use. Also, he is a consultant to several local and international organisations. Rukshan is a Chartered Engineer and Member of IMechE (UK), ASME, and AIAA.

Omar Ellabban (S'10–M'12–SM'13) is a senior researcher and creative manger with more than 20 years of combined experiences (teaching, research, industrial experience, consulting services and project management) between academia, research institutes, industry and power utility companies in various fields. Dr. Ellabban is conducting and leading many research projects in different areas, such as: power electronics, electric vehicles, automatic control, motor drive, energy management, grid control, renewable energy, energy storage devices, distributed energy systems and their integration into the smart grid. Dr. Ellabban received his B.S. (Hons.) degree in electrical machines and power engineering from Helwan University, Egypt; his M.S. degree in electrical machines and power engineering from Cairo University, Egypt; and his Ph.D. (Hons.) degree in electrical engineering from Free University of Brussels, Belgium, in 1998, 2005, and 2011, respectively. Dr. Ellabban has authored more than 75 journal and conference papers, one book chapter, two books entitled, "Impedance Source Power Electronic Converters, 2016" and "Smart Grid Enabling Technologies, 2021" and many international conference tutorials. His current research interests include renewable energies, grid control, smart grid, automatic control, motor drives, power electronics, and electric vehicles. He is a Senior Member of the IEEE, IET Fellow member and currently serves as an Associate Editor of the IEEE Transactions on Industrial Electronics.

Ingo Lüdtke received the Dipl.-Ing. (FH) degree in Electrical Engineering / Computer Science from Fachhochschule Braunschweig/Wolfenbüttel, Germany in 1990, the Dipl.-Ing. (TH) degree in Electrical Engineering / Automation Technology from Technische Hochschule Zwickau, Germany in 1991 and the Ph.D. degree in Electrical Engineering from the University of Glamorgan, U.K. in 1998. He has received the title of Honorary Visiting Professor from Cardiff University, U.K. in 2020. His current role is Head of Power Electronics at Compound Semiconductor Applications Catapult, U.K. His research interests are in motor control, optimisation, modelling and applications of wide-bandgap compound semiconductor power devices.