E-TCT characterisation of a thinned, backside biased, irradiated HV-CMOS pixel test structure

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Abstract

This paper presents the results of edge-Transient Current Technique (e-TCT) measurements of a test structure of a High Voltage CMOS (HV-CMOS) pixel demonstrator, the H35DEMO. Several high resistivity ($1000\,\Omega\cdot\mathrm{cm}$) samples of the device were thinned to $100\,\mu$m, processed for backside biasing, and irradiated with neutrons to fluences up to $2\cdot10^{16}\,\mathrm{n_{eq}}\cdot\mathrm{cm}^{-2}$. The evolution of effective doping concentration with respect to fluence is studied. Samples irradiated to a fluence of $5\cdot10^{14}\,\mathrm{n_{eq}}\cdot\mathrm{cm}^{-2}$ are fully depleted beyond $-50\,\mathrm{V}$ substrate bias voltage while samples irradiated to the highest fluence reach $30\,\mu$m depletion at $-200\,\mathrm{V}$.

Keywords: particle detector, CMOS, HV-CMOS, e-TCT

1. Introduction

The High Luminosity upgrade for the Large Hadron Collider (HL-LHC) [1], which aims to be operational by the end of 2027, will increase the luminosity of the current LHC by a factor of 10 [2]. As a result, detectors in experiments around the beamline will be subject to much higher doses of radiation, of the order $10^{16}\,1\,\mathrm{MeV}\,\mathrm{n_{eq}}\cdot\mathrm{cm}^{-2}$, throughout their lifetime. Detectors will therefore be required to retain detection efficiency after extended use in these high radiation environments.

Fully monolithic High Voltage CMOS (HV-CMOS) detectors [3] are an extremely attractive option for these future experiments given that they remove the need for the expensive, time-consuming bump bonding process required by the silicon pixel hybrids presently used by experiments at the LHC. In HV-CMOS detectors, the front-end electronics can be directly embedded in the sensor substrate, rather than being bump bonded or glued to a separate sensor.

In addition, compared with standard CMOS detectors HV-CMOS devices can be biased to high voltages for fast charge collection by drift, ensuring the detector can quickly be ready for subsequent events, but also ensuring high radiation tolerances. The H35DEMO is one such HV-CMOS detector, designed as a demonstrator for HL-LHC experiments [4] explained in more detail in section 2.1.

However, HV-CMOS sensors have been irradiated and tested for fluences of the order $10^{15}\,\mathrm{n_{eq}}\cdot\mathrm{cm}^{-2}$, one order of magnitude lower than that of hybrids [5] and required by the HL-LHC. Measurements of irradiated silicon devices show that radiation damage changes the effective doping concentration $\mathrm{N_{eff}}$ of silicon [6]. Which, as a result for high resistivity silicon, decreases the maximum size of the sensitive depletion region, thereby reducing the amount of charge collected by drift and decreasing the signal to noise ratio. Some examples of studies demonstrating this for maximum fluences of the order $10^{15}\,\mathrm{n_{eq}}\cdot\mathrm{cm}^{-2}$ for H35DEMO samples can be found in [7, 8, 9].

In a previous experimental study of high resistivity HV-CMOS devices [10], a comparison of fabricated topside biased and thinned, backside biased samples was carried out. The study shows thinned, backside biased samples collect more charge, therefore showing that despite the change in effec-

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tive doping concentration due to radiation damage, thinning and backside biasing could help to maintain detection efficiency at high fluences. The maximum fluence of samples in this study was $2 \cdot 10^{15}\,\mathrm{n_{eq}} \cdot \mathrm{cm}^{-2}$.

Presented here are results of edge-Transient Current Technique (e-TCT) measurements of test structures on H35DEMO samples, that have been thinned to 100 μm and backside processed to allow backside biasing [11]. Measurements include estimations of the depletion depths of a non-irradiated sample, and samples irradiated to 1 MeV neutron equivalent fluences up to $2 \cdot 10^{16}\,\mathrm{n_{eq}} \cdot \mathrm{cm}^{-2}$ (one order of magnitude larger than in [10]), and study the evolution of effective doping concentration with fluence.

2. Samples and post-processing

2.1. H35DEMO

The H35DEMO (see Figure 1a) is a pixel demonstrator device, measuring 18.49 mm × 24.40 mm, and fabricated in the 0.35 μm HV-CMOS process from ams AG. It uses a p-type substrate, with samples produced with nominal resistivities between 20 Ω·cm and 1000 Ω·cm. This study only includes measurements of the highest resistivity samples. The chip contains four large matrices of pixels and test structures at the top and bottom of the device, which are described in detail in reference [4]. E-TCT measurements in this study have been performed on the test structure (Figure 1b) which is highlighted in red at the bottom of Figure 1a.

This test structure consists of a 3 × 3 matrix of passive HV-CMOS pixels, each measuring 50 μm × 250 μm, which share the same cross-section as the pixels in the larger matrices. The pixel cross-section can be seen in Figure 2a. Each pixel is implemented by means of three deep n-wells (DNWELLs in the diagram) in the p-substrate forming three p-n junctions which are connected in parallel. In the larger matrices, readout electronics are implemented into the central deep n-well (with the exception of one of the matrices which includes logic in all three), which also acts as isolation from the p-substrate. NMOS logic is implemented into shallow p-wells (SPWELLs) inside the deep n-well and pMOS logic is implemented into shallow n-wells (SNWELLs). For simplicity, the pixels in the test structure contain no readout electronics.

The test structure provides two readout channels, one to access the central pixel (highlighted in green in Figure 1b) and the other one to access the outer eight pixels, which are shorted together. The central pixel is the main focus of this study. Since the test structure pixels have no readout electronics, no power is needed for transistors, so the n-wells are biased to 0 V in all measurements. A large reverse bias voltage is applied using the outermost p-implants seen in the cross-section which causes the depletion region to grow mostly into the lightly doped substrate.

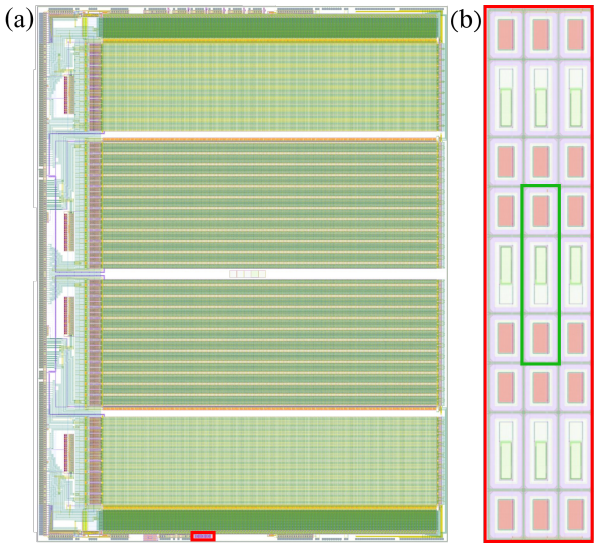

Figure 1: (a) Image of the H35DEMO chip. x and y directions in measurements in this study are horizontal and vertical directions respectively. The test structure used for these measurements is highlighted in red at the bottom of the device. (b) Test structure zoomed and rotated. The central pixel is highlighted in green.

2.2. Backside processing

An undiced 1000 Ω·cm wafer of H35DEMO samples was sent to Ion Beam Services (IBS) for backside processing and dicing. Backside processing included TAIKO thinning to 100 μm using 4000 grade mesh and plasma etching to remove potential defects, p+ implantation, thermal annealing at low temperature to activate the implantation, and backside metallisation to create a contact (see Figure 2b). Initial results on a thinned, backside biased sample can be found in [11].

After dicing, small scratches could be seen on the edges of samples which can refract laser light in the e-TCT measurements described in section 3.2. Therefore, the bottom edges of the samples were polished with 3 μm grit lapping sheet and 1/10 μm

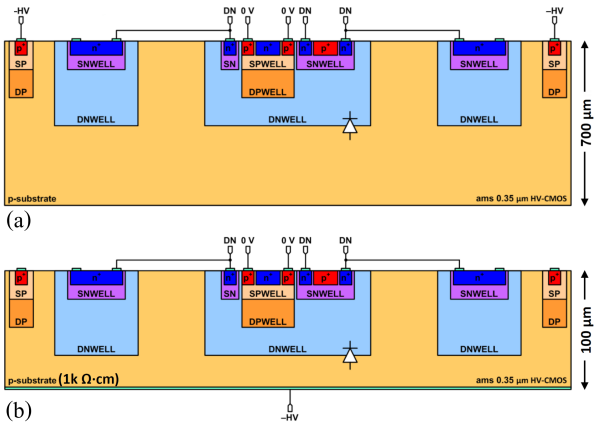

Figure 2: (a) Cross-section diagram of a typical pixel from the H35DEMO. x and z directions in measurements in this study are horizontal and vertical directions respectively. The default substrate thickness is 700 μm. (b) The same cross section after thinning to 100 μm. The topside substrate contacts are left floating and the substrate is now biased to high voltage from the backside.

grade diamond paste to remove the defects. Only the edge of the device illuminated with the laser in the measurements was polished however, since after thinning samples became very brittle and polishing a single edge reduced the likelihood of breakages.

2.3. Irradiation campaign

Six samples were irradiated with neutrons at the TRIGA reactor at the Jožef Stefan Institute (JSI) in Ljubljana [12]. Individual samples were irradiated to different neutron equivalent fluences $\Phi_{\mathrm{eq}} = 1 \cdot 10^{14}$, $5 \cdot 10^{14}$, $3 \cdot 10^{15}$, $5 \cdot 10^{15}$, $1 \cdot 10^{16}$, and $2 \cdot 10^{16}$ 1 MeV $\mathrm{n_{eq}} \cdot \mathrm{cm}^{-2}$ in order to study their performance after suffering effects due to radiation damage. No annealing was performed on the samples, which were kept cold during transport from the JSI facility and during all measurements.

3. Measurements

A Particulars scanning-TCT system [13] was used for the measurements. Using silver conductive paint, samples were glued to a custom PCB, which features a large pad to enable backside biasing. The test structure pads were wirebonded to the PCB in order to process read-out signals. To reduce contributions from noise to the signal and avoid effects of annealing in irradiated samples, PCBs were mounted on a Peltier-cooled stage and kept at $-20\,^{\circ}\mathrm{C}$ for the duration of the measurements.

3.1. Current-voltage

Current-voltage (I-V) measurements were used to determine the reverse breakdown voltages V_{BD} of the samples, and therefore, the safe maximum operating voltages for e-TCT measurements. The pad of the PCB for backside biasing the samples was connected to the negative terminal of a Keithley 2410 source meter and the pad of the central deep n-well was connected to the positive terminal. The supply was ramped to a negative high voltage in 1 V steps, and the current was recorded. Compliance current was set to 10 μA. At this value, the diode was considered to have reached reverse breakdown, and the measurement was stopped. This was repeated for the non-irradiated sample and the irradiated samples (see Figure 3).

The leakage current I_{leak} increases with Φ_{eq}, which is expected due to lattice damage in the bulk [14]. Variations in $\mathrm{V_{BD}}$ of the non-irradiated and low fluence samples can be expected due to initial device-to-device variation, but higher fluence samples ($3{\cdot}10^{15}\,\mathrm{n_{eq}} \cdot \mathrm{cm}^{-2}$ and above) were observed to exhibit a softer breakdown, allowing samples irradiated to higher fluences to be biased to higher voltages in e-TCT measurements (section 3.2). I_{leak} of the non-irradiated sample and sample irradiated to $1 \cdot 10^{14}\,\mathrm{n_{eq}} \cdot \mathrm{cm}^{-2}$ (at low voltages) was too low to measure accurately with the equipment. The increase in leakage current for the sample irradiated to $1 \cdot 10^{14}\,\mathrm{n_{eq}} \cdot \mathrm{cm}^{-2}$ is not understood.

3.2. E-TCT

In e-TCT measurements [15], the edge of the sample is illuminated with a collimated and pulsed

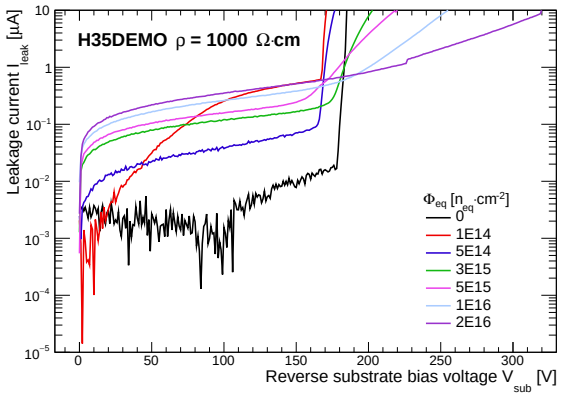

Figure 3: I-V measurements of backside biased irradiated H35DEMO samples.

infrared laser of wavelength 1064 nm. In response to the laser pulse, electron-hole pairs are generated inside the depleted bulk, and drift towards the collecting electrodes due to the electric field. The charge carriers induce a current at the collecting electrodes which is amplified by a discrete amplifier and the signal is read by an oscilloscope.

The stage in the TCT system is capable of submicron movement in two directions x and z (horizontal and vertical directions in Figure 2, respectively), and the focussing optics can be moved in the remaining y direction (vertical direction in Figure 1). By moving the laser optics the waist of the laser beam in the silicon device can be placed below the structure under study. In these particular measurements, the size of the depletion region for a given bias voltage was determined by scanning samples from top to bottom at the centre of the central test structure pixel.

Since each sample was glued to a PCB by hand, there are variations in the position of the pixels relative to the system device to device. Therefore the location of the pixel was first determined by scanning the sample in discrete steps in the x and z directions. A current waveform was recorded at each step (see Figure 4) and the collected charge measured by integration of the signal peak using an integration time of 10 ns, which was kept the same for all samples. Plotting the charge as a function of x and z coordinates in a 3D graph is used to build up an image of the depletion region of the central pixel (see Figure 5). The centre of the pixel (approximately $x = 30275\,\mu$m in the figure) was extracted from this. Optimal optics to sample distance y was chosen using the knife-edge technique i.e., at the fastest increase of collected charge with coordinate z at the top of the sample. A scan in just the z direction at fixed x and y values for different bias voltages was used to characterise the growth of the depletion region. This measurement was repeated for the non-irradiated and all irradiated samples.

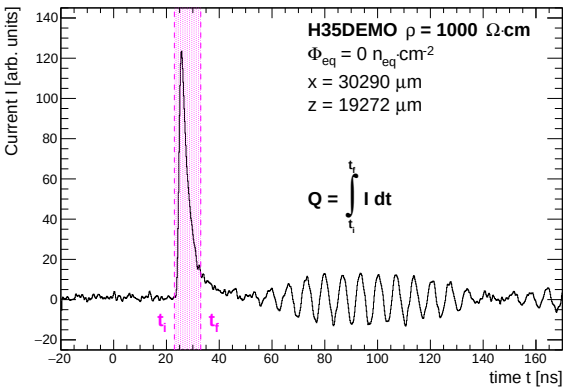

Figure 4: Current waveform recorded at stage position $x = 30290\,\mu$m, $z = 19272\,\mu$m for the non-irradiated device. The waveform is integrated between an initial time t_i and a final time t_f to calculate the collected charge when the laser is focussed at that position.

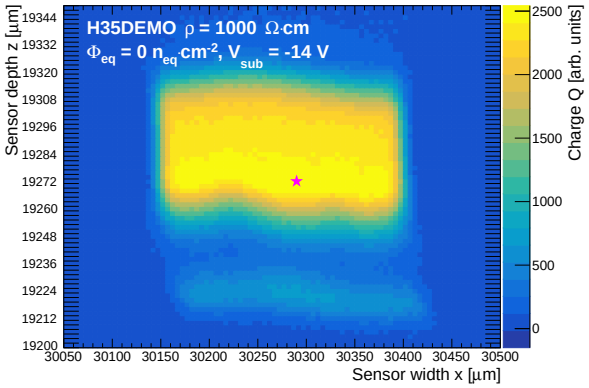

Figure 5: An image of the depletion region of the pixel at substrate bias voltage -14 V. The topside of the device can be seen at approximately $z = 19320\,\mu$m, and the backside of the device at approximately $z = 19220\,\mu$m. The pink star is the location of the waveform in Figure 4.

4. Results and analysis

Figure 6 shows the charge collection profiles and fits for different values of the substrate bias voltage V_{sub} for the non-irradiated sample. It can be seen that by increasing V_{sub}, the sensitive region grows from the top electrode (at approximately $z = 19315\,\mu$m here), to the back electrode (at approximately $z = 19220\,\mu$m). The width of the profile continues increasing until around -30 V where the width of the profile no longer increases. At this point, the sample is considered fully depleted.

Along the charge collection profiles in Figure 6, two peaks in charge collection can be seen. The peak at the backside of the sample, centred at approximately $z = 19225\,\mu$m is due to the electric field created by the highly doped backside p+ implant–low-doped p-substrate interface. The second peak in charge collection can be seen at the boundary of the depletion region. This has been observed in other measurements of the same high resistivity samples [7, 8], explained in [7] to be due to charge sharing between this pixel and the other pixels in the test structure. This can be seen

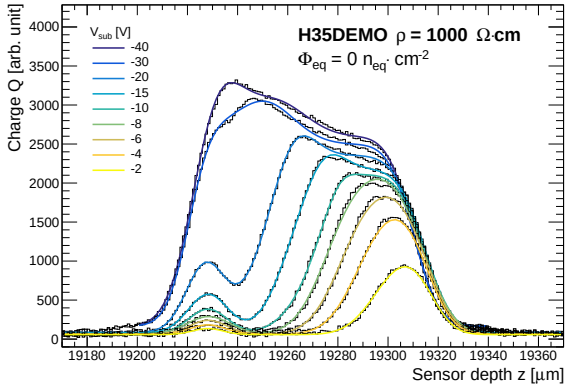

Figure 6: Equation 1 fit to the charge collection profiles of multiple substrate bias voltages for the non-irradiated sample.

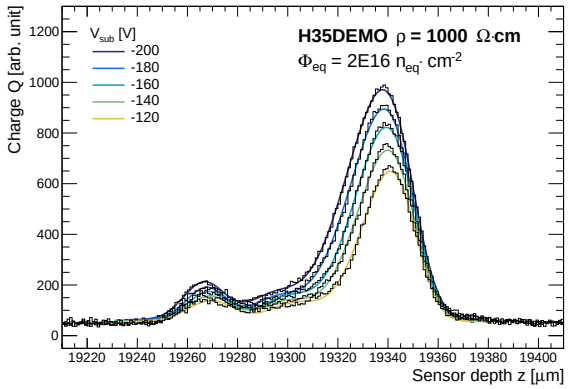

Figure 7: Equation 1 fit to the charge collection profiles of multiple substrate bias voltages of the most highly irradiated sample.

prominently for $V_{sub} = -20\,V$, centered at approximately $z = 19265\,\mu m$. At higher voltages and when full depletion occurs (around $V_{sub} = -30\,V$), the two peaks can be seen to merge, giving the charge collection profile its unusual shape. Figure 7 shows examples of charge collection profiles for the highest fluence sample. It can be seen that the sample never becomes fully depleted, but a charge collection peak at the backside can still be seen.

The width of the depleted region W_D was estimated from the Full Width at Half Maximum (FWHM) of the charge collection profiles (see Figure 8). Equation 1 was fitted to the charge collection profiles for each bias voltage recorded.

$$f(z) = \Big\{A\Big[\mathrm{erf}\Big(\frac{z-k_1}{B_1}\Big) - \mathrm{erf}\Big(\frac{z-k_2}{B_2}\Big)\Big] + a_1 \exp\Big(\frac{(z-\mu_1)^2}{2\sigma_1^2}\Big) + a_2 \exp\Big(\frac{(z-\mu_2)^2}{2\sigma_2^2}\Big)\Big\} + c \tag{1}$$

It consists of a superposition of two error functions and two gaussians (see figure 8), where A and B are vertical and horizontal scale factors respectively, and k is a horizontal translation factor of the error functions. a, μ, and σ are the peak height, mean, and standard deviation of the gaussian distributions, respectively. The subscripts 1 and 2 refer to the first and second functions used of each type. c is a vertical translation factor for the whole function necessary to model the noise for a better fit.

The error functions serve as the fit to the majority of the charge collection profile, created by the pixel depletion region, and the gaussians fit the two observed peaks in charge collection. The gaussian centred at approximately $z = 19225\,\mu m$ (pink in Figure 8) fits the peak at the backside. The second gaussian centred at around $z = 19260\,\mu m$ (green in Figure 8) serves to fit the peak in charge collection at the depletion region boundary.

W_D was evaluated from the FWHM:

$$W_D = z_2 - z_1 \tag{2}$$

where z_1 and z_2 are extracted from the fit when $f(z)$ is equal to the half maximum of the error func-

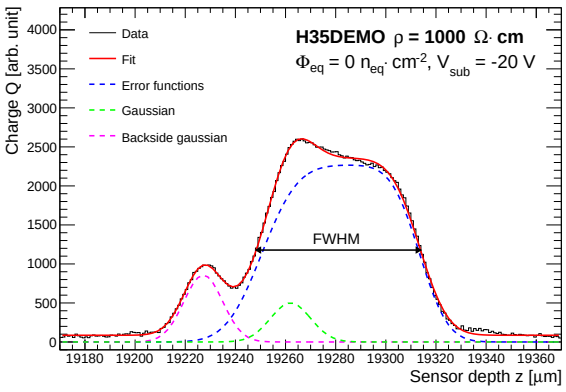

Figure 8: Equation 1 fit to the charge collection profile of the non-irradiated device at a substrate bias voltage of $-20\,V$. Topside of the device is at approximately $z = 19320\,\mu m$. The FWHM is shown with a black arrow.

tions, plus the noise. In this case, z_2 corresponds to the top electrode (approximately $z = 19315\,\mu$m in Figure 8) which is the underside of the deep n-well, close to the topside of the device. This was repeated for each measured substrate bias voltage V_{sub}.

W_D was plotted against V_{sub} to produce Figure 9. V_{sub} on the plot is shown in absolute units. The non-irradiated sample, the sample irradiated to $1 \cdot 10^{14}\,\text{n}_{\text{eq}} \cdot \text{cm}^{-2}$, and the sample irradiated to $5 \cdot 10^{14}\,\text{n}_{\text{eq}} \cdot \text{cm}^{-2}$ are fully depleted at $-24\,\text{V}$, $-30\,\text{V}$, and $-50\,\text{V}$, respectively. At high levels of irradiation samples no longer become fully depleted, and W_D decreases with fluence. At the maximum fluence measured, the device is still able to reach a depletion depth of $30\,\mu$m. Measurements have been taken at higher bias voltages for higher fluence samples as analysis of I-V curves show irradiation increases V_{BD}.

Data points below full depletion are fit with equation 3 in order to extract the effective doping concentration N_{eff} [16]:

$$W_D = W_{D_0} + \sqrt{\frac{2\varepsilon_{\text{Si}}\varepsilon_0}{e_0 N_{\text{eff}}} \cdot V_{\text{sub}}} \tag{3}$$

where ε_{Si} is the relative permittivity of silicon, ε_0 is the vacuum permittivity, e_0 is the elementary charge, and W_{D_0} is a parameter introduced to describe the collected charge measured at $V_{\text{sub}} = 0\,\text{V}$, which is a consequence of non-zero laser beam width, charge collection by diffusion, and built-in depletion. Extracting N_{eff} of the non-irradiated device gives an estimate of the initial substrate resistivty $\rho = 2212 \pm 35\,\Omega\cdot\text{cm}$ [17], which is slightly higher than the range of the possible resistivity of $1000\,\Omega\cdot$cm samples provided by the foundry (600–$2000\,\Omega\cdot$cm) but is confirmed by other studies of this device [7, 8]. The evolution of N_{eff} with Φ_{eq} was studied (see Figure 10) by fitting the data to equation 4 [14]:

$$N_{\text{eff}} = N_{\text{eff}_0} - N_c \cdot (1 - \exp(-c \cdot \Phi_{\text{eq}})) + g_c \cdot \Phi_{\text{eq}} \tag{4}$$

where N_{eff_0} is the initial doping concentration i.e. the doping concentration of the non-irradiated device, N_c is the concentration of acceptors that have been removed, c is the acceptor removal constant, and g_c is the stable damage introduction rate. The extracted values can be seen in table 1.

Since it is known that acceptor removal happens at low fluences in devices with high resistivity, and

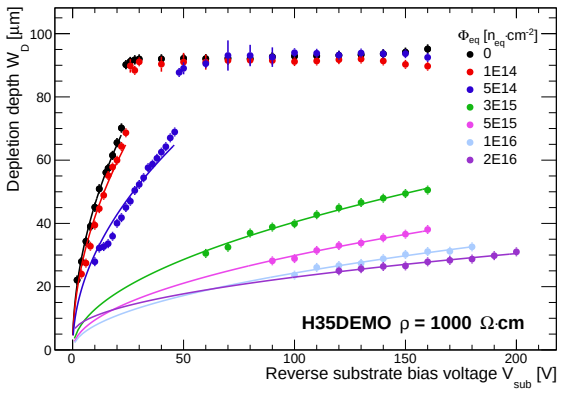

Figure 9: Depletion depth as a function of substrate bias voltage for non-irradiated device and devices irradiated up to $2{\cdot}10^{16}\,\text{n}_{\text{eq}}{\cdot}\text{cm}^{-2}$.

there are no measurements of low fluence devices presented here, N_c and c were set to 0. Therefore it can be seen that N_{eff} increases linearly with an increase in fluence with $g_c = 0.022 \pm 0.001\,\text{cm}^{-1}$, slightly larger than the typical value of $0.020\,\text{cm}^{-1}$ reported in literature, but consistent with high resistivity devices in other technologies [10, 18].

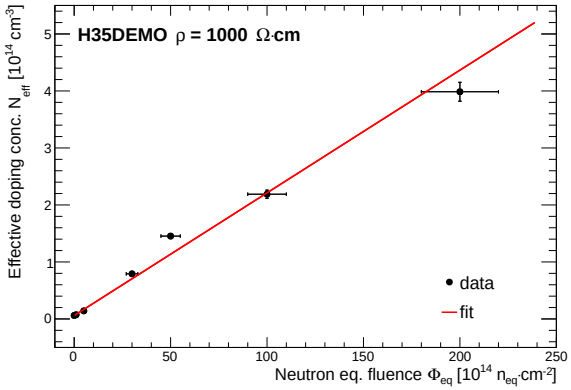

Figure 10: Evolution of effective doping concentration with neutron equivalent fluence.

	H35DEMO
$\rho\,[\Omega\cdot\text{cm}]$	2212 ± 35
$N_{\text{eff}_0}\,[10^{14}\cdot\text{cm}^{-3}]$	0.060 ± 0.001
$g_c\,[\text{cm}^{-1}]$	0.022 ± 0.001

Table 1: Parameters extracted from equation 4 fit to data in Figure 10.

5. Conclusion

High resistivity samples of an HV-CMOS detector prototype, the H35DEMO were thinned to 100 μm, backside processed to create a backside contact, and irradiated to fluences up to $2 \cdot 10^{16}\,\mathrm{n_{eq}} \cdot \mathrm{cm}^{-2}$. E-TCT measurements were used to estimate the depth of the depletion region of pixels in a test structure, which was shown to increase proportionally with the square root of the substrate bias voltage, until the samples reach full depletion. Irradiated devices show decreased depletion depths for the same bias voltage, due to increased effective doping concentration of the substrate, which was shown to increase linearly with fluence. Non-irradiated and lowest fluence samples are fully depleted at substrate bias voltages of -24 V and -30 V respectively and the sample irradiated to maximum fluence reaches a maximum depletion depth of 30 μm at -200 V.

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