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Latest Depleted CMOS Sensor Developments in the CERN RD50 Collaboration

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This contribution summarizes the most recent activities carried out within the CERN RD50 collaboration with regard to Depleted Monolithic Active Pixel Sensors (DMAPS). In particular, these activities have been focused on the characterization of the RD50-MPW2 prototype. RD50-MPW2 is the second DMAPS prototype developed in the 150 nm HV-CMOS technology process from LFoundry. The main characteristics of the RD50-MPW2 design will be reviewed. The leakage current, breakdown voltage and Edge Transient Current Technique (E-TCT) measurements of the RD50-MPW2 test structures will be presented. The characterization of the RD50-MPW2 active matrix and its readout electronics will be also described. Finally, the initial characteristics of the new RD50-MPW3 DMAP sensor prototype being designed at present by the CERN-RD50 collaboration will be shown.

KEYWORDS: semiconductor, sensor, CMOS, DMAPS, ...

1. Introduction

DMAPS using commercial CMOS and High-Voltage CMOS (HV-CMOS) processes are one of the main candidate technologies for future tracking detectors in high luminosity colliders. Their capability of integrating the sensing diode into the CMOS wafer hosting the front-end electronics allows for reduced noise and higher signal sensitivity. They are suitable for high radiation environments due to the possibility of applying high voltage and the availability of relatively high resistivity substrates. The use of a CMOS commercial fabrication process leads to lower costs and allows faster construction of large area detectors. Despite the advantages and good performance demonstrated by DMAPS, these sensors still require further research to improve their time resolution and radiation tolerance to cope with the challenging environment of future particle physics experiments. In this context, the study and development of DMAPS is one of the priorities of the CERN RD50 collaboration.

CERN RD50 is an international collaboration with more than 400 members, which aims at developing and characterizing radiation hard semiconductor devices for high luminosity colliders. Among other research interests, research and development of new sensor structures such as 3D detectors, Low Gain Avalanche Detectors (LGAD) or depleted CMOS sensors are carried out. Due to its potential for future experiments, there is a specific program within the collaboration in order to develop DMAPS covering a variety of topics like TCAD simulations, ASIC design, DAQ development and device characterization. About 36 people from 12 institutes are involved in this program.

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2. CERN RD50 device development roadmap

Two DMAPS have been developed in the RD50 collaboration so far, the RD50-MPW1 and the RD50-MPW2, all of them using Multi-Project Wafers (MPW) in the 150 nm HV-CMOS process from LFoundry. The pixels of both devices have a large collection electrode and have been fabricated with 280 μm silicon wafers.

The RD50-MPW1 [1] was manufactured in April 2018 to gain expertise and test the L-Foundry process and novel designs that were introduced in the submission. It has a size of 5 mm by 5 mm and it was fabricated using substrates with a resistivity of 500 Ω·cm and 1.9 kΩ·cm. The RD50-MPW1 device has test structures for I-V and E-TCT measurements and two independent CMOS pixel matrices. One is a photon counting matrix with 26 by 52 pixels with embedded readout electronics, charge amplifier and discriminator, and a 16-bit counter. The other matrix has 40 by 78 pixels, with a size of 50 μm by 50 μm, with embedded readout electronics following a column drain readout architecture similar to the FE-I3 readout chip [2]. In this device, the measured pixel leakage current was found too high and the breakdown voltage was low [1]. Cross-talk was also detected in some digital lines coming from the in-pixel digital readout of the FE-I3 style matrix [3].

Therefore, RD50 decided to develop a smaller prototype, RD50-MPW2, to improve the pixel and analog readout design. This device was manufactured in February 2020. The main goal was to test new design approaches to minimize leakage current by preventing certain conductive filling layers added by the foundry for fabrication and adding a series of guard rings surrounding the pixel matrix [4]. A new pixel embedded readout electronics design was also implemented to improve the speed of the readout electronics [5]. The main characteristics and the characterization of this device are addressed in the following sections.

Finally, a new DMAPS, the RD50-MPW3, is currently being designed within the RD50 collaboration. It will be a device with a size similar to the RD50-MPW1, with the same pixel design as the RD50-MPW2 and an improved digital readout design to avoid the cross-talk problems detected in the RD50-MPW1. The initial characteristics of this device are introduced in section 6.

3. RD50-MPW2 main characteristics

The RD50-MPW2 [6] has a size of 3.211 mm by 2.120 mm and it was manufactured using resistivity substrates of 10 Ω·cm , 0.5-1.1 kΩ·cm, 1.9 kΩ·cm and $>$ 2 kΩ·cm. Eighty samples of each resistivity were manufactured. The RD50-MPW2 floorplan can be seen in Fig. 1a. It consists of depleted CMOS pixel test structures for I-V and E-TCT measurements, a matrix of 8 by 8 pixels with analog embedded readout, a bandgap voltage reference, a Single Event Upset (SEU) tolerant memory array and test structures with Single-Photon Avalanche Diodes (SPAD). The pixel cross-section of the pixel matrix is depicted in Fig. 1b. It is very similar to the pixel used in the FE-I3 style matrix of the RD50-MPW1 but the electrode spacing is 8 μm instead of 3 μm and the pixel size is 60$\times$60 μm^2 instead of 50$\times$50 μm^2.

The test structures of the RD50-MPW2 used for I-V and E-TCT measurements consist of four test matrices of depleted CMOS pixels without embedded readout electronics. Each matrix has nine pixel diodes with different sizes, shapes and electrode spacing. The first matrix in the top right in Fig. 1a, has rounded square pixels of 50 μm side with electrode spacing of 3 μm while the rest of the matrices have pixels of 60 μm with electrode spacing of 8 μm. The second matrix has rounded square pixels, the third matrix chamfered square pixels and the fourth one square pixels. The pixels of the second test matrix have the same geometry as the ones implemented in the 8 by 8 pixel matrix.

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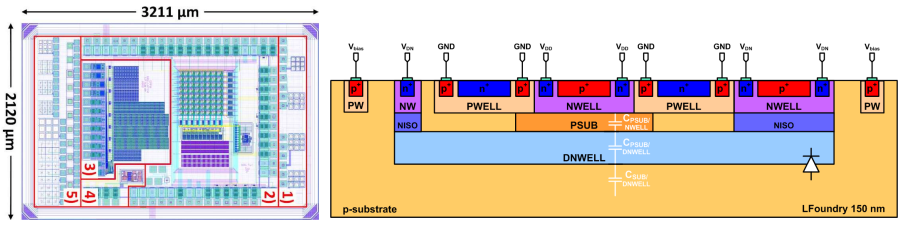
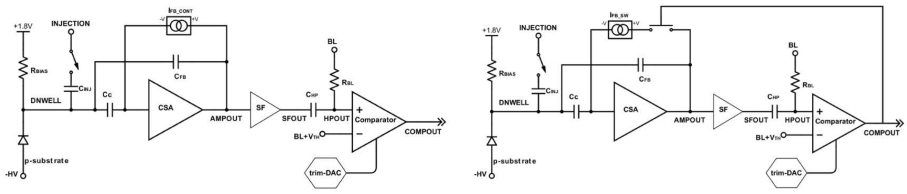


(a) (b)

Fig. 1. Floorplan of the RD50-MPW2 depleted CMOS sensor (a) with its main blocks highlighted: I-V and E-TCT depleted CMOS pixel test structures (1), 8 by 8 pixel matrix (2), SEU tolerant arrray (3), bandgap voltage reference (4) and SPAD test structures (5). Cross-section of the RD50-MPW2 matrix pixel (b).

Two different flavors of analog embedded readout have been implemented in the 8 by 8 pixel matrix. The first four columns have continuous reset readout pixels while the second four columns have switched reset readout pixels. Both types of schematics are showed in Fig. 2a and Fig. 2b, respectively. There is also a bias block close to the pixel matrix, which generates the bias voltages to set the transistors DC operating points for the pixels readout of the matrix. Configuration registers have been included as well in order to control the pixel matrix operation.



(a) (b)

Fig. 2. Schematic of the continuous reset pixel readout (a) and a switched reset readout (b).

4. Measurements of RD50-MPW2 test structures

4.1 I-V measurements

The leakage current versus the bias voltage was measured for the four pixel matrices included in the RD50-MPW2 test structures for several resistivity substrates in both non-irradiated and irradiated devices. The measurements were carried out at room temperature, in complete darkness, in different institutes with a probe station connected to a Source Measure Unit (SMU), placing the bare dies directly on a chuck, contacting the pads of the sensor electrodes with needles. Fig. 3a shows the I-V measurement for a pixel sensor of the first RD50-MPW2 test matrix for a device with a resistivity of 0.5-1.1 kΩ·cm and for the RD50-MPW1 pixel with a resistivity of 0.5 kΩ·cm. The leakage current for an RD50-MPW2 pixel sensor is many orders of magnitude smaller than that measured on RD50-MPW1. Fig. 3b shows the I-V measurements for all the RD50-MPW2 test matrices for the same substrate resistivity (0.5-1.1 kΩ·cm). The leakage current for all matrices is similar while the breakdown voltage increases with electrode spacing, as expected, and it is also lightly influenced by the

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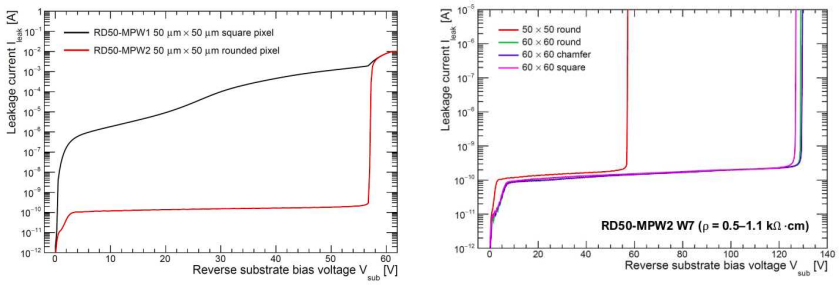
corner shape. The breakdown voltage was measured for the four test matrices in 23 RD50-MPW2 samples with three different resistivity substrates (0.5-1.1 kΩ·cm, 1.9 kΩ·cm and $>$ 2 kΩ·cm). The results of these measurements confirmed the breakdown voltage values seen in Fig. 3b. More precise leakage current measurements were also carried out for the second RD50-MPW2 test matrix with three different resistivity substrates (0.5-1.1 kΩ·cm, 1.9 kΩ·cm and $>$ 2 kΩ·cm) using an additional ammeter for measuring the leakage current of the central pixel while keeping the surrounding pixels connected to ground. The measured leakage current between a bias voltage of -5 and -60 V was well below 1 pA.



(a) (b)

Fig. 3. I-V curve for a pixel sensor of the first RD50-MPW2 test matrix (red line) and for the RD50-MPW1 (black line) (a). I-V measurements for all the RD50-MPW2 test matrices for the 0.5-1.1 kΩ·cm substrate resistivity (b).

Twenty RD50-MPW2 samples of each substrate resistity manufactured were irradiated with neutrons in the TRIGA reactor in Ljubljana to fluences ranging from $1{\cdot}10^{13}$ 1 MeV n_{eq}/cm^2 to $2{\cdot}10^{15}$ 1 MeV n_{eq}/cm^2 [7]. The I-V measurements with irradiated samples were carried out using the second test matrix. Fig. 4a shows the I-V measurements performed on devices of three different resistivity substrates (0.5-1.1 kΩ·cm, 1.9 kΩ·cm and $>$ 2 kΩ·cm) for three different irradiation fluences ($1{\cdot}10^{13}$, $3{\cdot}10^{13}$ and $1{\cdot}10^{14}$ 1 MeV n_{eq}/cm^2). It can be seen that, as expected, the leakage current increases with the irradiation fluence and also that the breakdown voltage decreases with the irradiation fluence similarly for all resistivity substrates. Fig. 4b shows the I-V measurements of a device irradiated with a fluence of $2{\cdot}10^{15}$ 1 MeV n_{eq}/cm^2 and the highest resistivity ($>$ 2 kΩ·cm). The different measurements correspond to different annealing time steps at 60 °C (80, 160, 320, 640 and 1280 min). The plot shows that the leakage current decreases with annealing time, as expected for silicon. The breakdown voltage also tends to increase with the annealing time.

4.2 E-TCT measurements

E-TCT measurements were performed using the second test matrix of the RD50-MPW2 with irradiated and non-irradiated samples to study the depletion region of the sensor [8]. In this measurement technique, the edge of the RD50-MPW2 test matrix is scanned with a movable laser beam of infrared light (λ = 1064 nm), spot size of about 5 μm and pulsed in the sub-nanosecond range to create electron-hole pairs at a known depth. The generated charge can be mapped as a function of the position at which the charge was generated in the pixel sensor bulk as well as the pixel bias voltage, and therefore the depletion depth can be obtained. In particular, the depletion region of the central diode of the matrix was characterized while the outer diodes were connected to ground.

Figure 5a shows the depletion depth as a function of the sensor bias voltage for a resistivity

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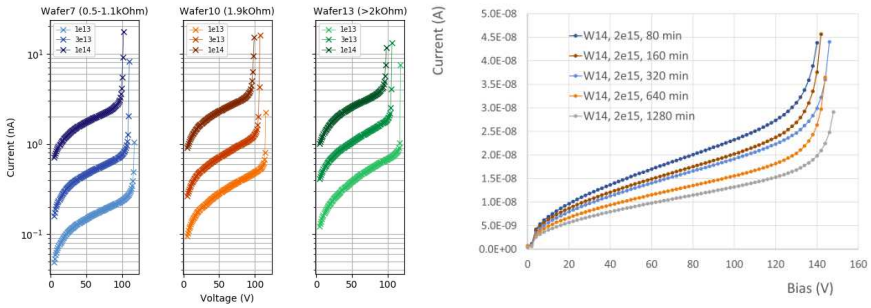

(a) (b)

Fig. 4. I-V curves for different resistivity substrates and neutron irradiation fluences (a) and for different annealing time steps at 60 °C (b).

substrate of 0.5-1.1 kΩ·cm and four different neutron irradiation fluences (ranging from 0 to $2{\cdot}10^{15}$ 1 MeV n_{eq}/cm^2). The depletion depth W_D is defined as the FWHM of the measured charge collection profile and fitted with:

$$W_D = W_{D0} + \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{e_0 N_{eff}} \cdot V_{bias}} \tag{1}$$

where W_{D0} is a parameter that describes the offset at low voltages due to finite laser beam width, collected charge due to diffusion and also due to built-in depletion, ε_0 the dielectric constant, ε_{Si} the relative permittivity of silicon, e_0 the elementary charge, N_{eff} the effective space charge concentration and V_{bias} the bias voltage. The depletion depth grows with the bias voltage before and after irradiation in accordance with Eq. 1. N_{eff} as a function of the neutron fluence can be estimated by fitting the data showed in Fig. 5a using Eq. 1. The plot shown in Fig. 5b reveals that N_{eff} increases with fluence, as expected due to radiation induced deep acceptors. This leads to a decrease in depletion depth at high fluences.

Fig. 5c shows the depletion depth as a function of the sensor bias voltage for a resistivity substrate of 0.5-1.1 kΩ·cm and a neutron irradiation fluence of $2{\cdot}10^{15}$ 1 MeV n_{eq}/cm^2. The different measurements correspond to different annealing time steps at 60 °C. Fig. 5d shows the N_{eff}, estimated from the fit to Eq. 1 corresponding to the data showed in Fig. 5c, as a function of the annealing time at 60 °C. There is a significant effect of the first annealing step but there is not much change after longer annealing times.

5. Characterization of RD50-MPW2 active matrix

The RD50-MPW2 8 by 8 pixel matrix has been characterized for non-irradiated devices. Both the in-pixel calibration circuit implemented in each matrix pixel and an external radioactive source have been used for this purpose. A specific DAQ (Data AcQuisition) system has been developed for the characterization of the RD50-MPW2 active pixel matrix [9].

5.1 Tests with in-pixel calibration circuit

In order to test the readout of the pixels, the first step was injecting a signal through the pixel calibration circuit and reading out the pixel comparator output with the DAQ system. Fig. 6a shows a hitmap of the matrix with the number of hits detected per pixel whereas Fig. 6b shows the mean time over threshold (ToT) maps with the mean pulse width measurement per pixel. It can be seen that the same number of pulses are detected in all pixels and that

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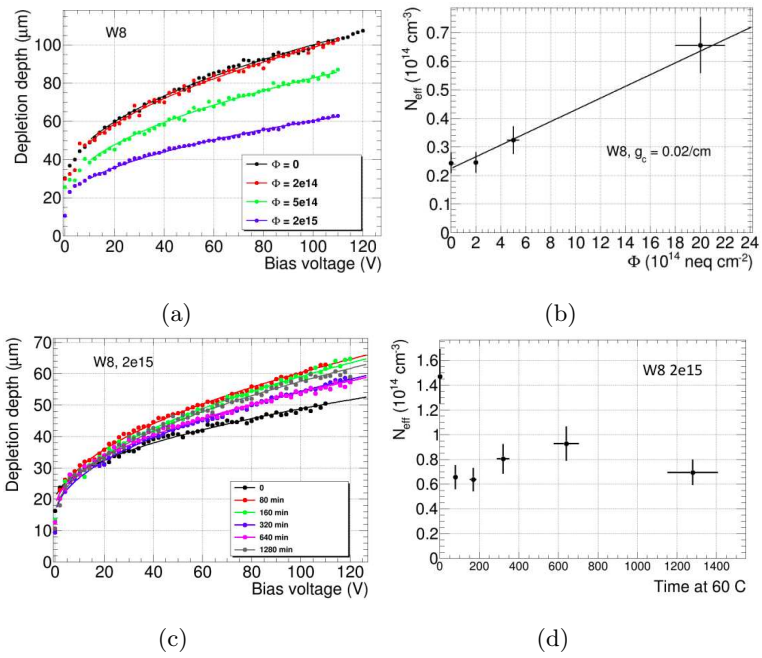

Fig. 5. Depletion depth before and after neutron irradiation of the 0.5-1.1 kΩ·cm sensor (a) and initial doping concentration as a function of 1 MeV neutron equivalent fluences (b). Depletion depth for different annealing time steps at 60 °C (c) and initial doping concentration as a function of annealing time (d).

the mean ToT values are similar for the two different pixel readout types of the matrix.

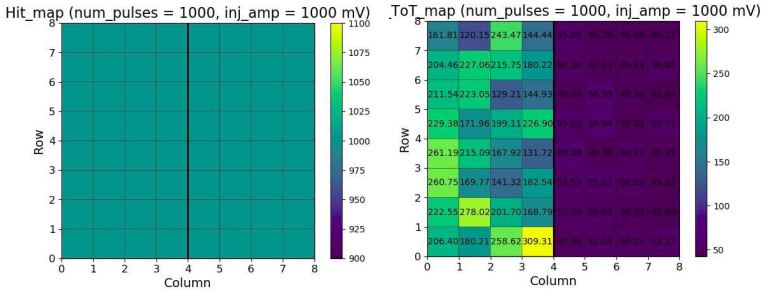

Fig. 6. Full matrix hit map (a) and mean ToT map (b). For both plots the comparator threshold was 990 mV and 1000 pulses of amplitude 1000 mV were injected.

Using the in-pixel calibration circuit, different types of S-curves were computed, such as the number of hits detected per pixel as a function of the injection amplitude variation or versus the comparator threshold variation. The S-curves corresponding to the different Trim DAC values programmable to have a fine variation of the comparator threshold were also computed to verify that this variation is linear. This can be seen in Fig. 7a, where the threshold value at which the 50% of hits are detected (Vt50) is plotted for the different programmable trim DAC values. The optimal trim DAC values for every pixel comparator in order to reduce the width of the S-curves of all pixels could also be found, as it can be

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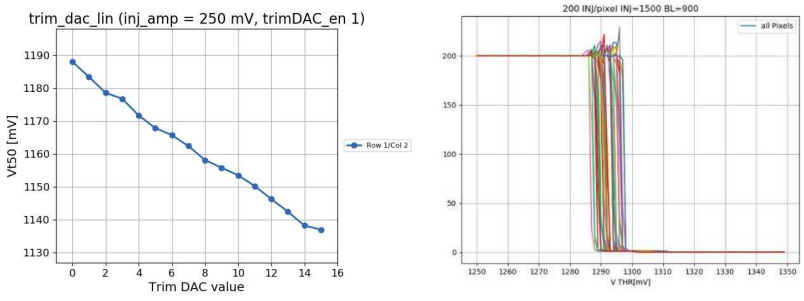
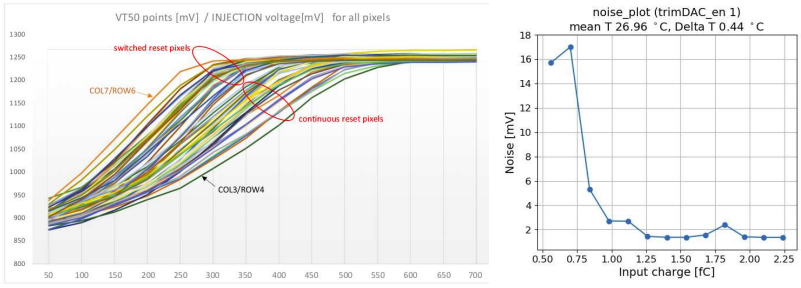
seen in Fig. 7b, demonstrating that the pixel comparator trim DAC worked as expected.



(a) (b)

Fig. 7. Vt50 (mV) versus trim DAC value for a continuous reset pixel (a). S-curves for all matrix pixels (threshold variation) with trim DAC values adjusted to reduce the width of the area where the S-curves change (b).

From the S-curves, gain and noise of the pixel readout chain can also be calculated. Fig. 8a shows the threshold value corresponding to the 50% of hits (Vt50) as a function of the injection signal amplitude for all the pixels. It can be distinguished that the pixel sensors with continuous and switched reset readout have different gain values and the linear range of the gain for each pixel readout type. Fig. 8b shows the noise for switched reset readout pixel (threshold value corresponding to 84% of hits minus threshold values corresponding to 16% of hits) as a function of the input injected charge (with 1fC of input charge corresponding to 257 mV of input signal amplitude). Both the gain and noise measurements agreed with the simulated values.



(a) (b)

Fig. 8. Vt50 (mV) versus injection amplitude (mV) for all pixels (a) and noise (mV) versus input charge (fC) for a switched reset pixel readout (b).

5.2 Tests with a radioactive source

Finally, a ^{90}Sr radioactive source (370 MBq) was used to generate the hits in the active matrix pixels instead of the calibration circuit. Two different RD50-MPW2 samples with a resistivity substrate > 2 kΩ·cm were measured with a shutter time per pixel of 20 s. The number of hits detected per pixel for all pixels as a function of the bias voltage of the pixel for the two different RD50-MPW2 samples were measured. As it can be seen in Fig. 9, the mean value of the number of hits increases with the bias voltage as expected.

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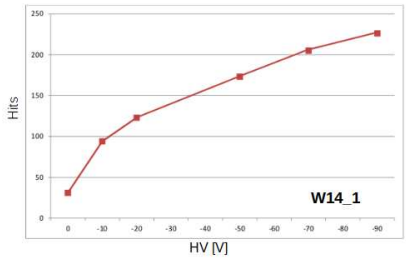

Fig. 9. Mean value of the number of hits detected for all matrix pixels versus the pixel bias voltage with a radioactive source for RD50-MPW2 sample W14-1.

6. RD50-MPW3 device design overview

A new RD50-MPW3 device is currently being designed. It will be manufactured as a MPW in the 150 nm HV-CMOS process from L-Foundry. The device will be bigger than the RD50-MPW2, with a size of 5 mm by 5 mm, in order to accommodate at least one active FE-I3 style matrix and to be able to perform beam tests. Test structures for I-V and E-TCT measurements will be also included. This matrix will have the same pixel and embedded readout as the RD50-MPW2 pixel matrix with capability of masking noisy pixels. However, the matrix layout will be improved. It is foreseen to implement separated analog and digital bias inside each pixel to avoid noise problems. Moreover, it is planned to distribute the matrix columns as double columns with shared digital signals to reduce the routing congestion and cross-talk in the RD50-MPW1 FE-I3 style matrix.

Regarding the chip periphery electronics, there will be an improved FE-I3 style readout to optimize the data transmission. Two end of column (EOC) architectures will be considered to reduce the pixel dead time. There will be one serial data transmission channel with LVDS format. The output data will be transmitted in frames and encoding to keep synchronization will be studied. The slow control for the pixel and bias registers configuration will be based on I2C and Wishbone.

The implementation of the device will be carried out following a digital on top methodology to guarantee timing. We are currently working on the RTL functional model of the pixel, pixel matrix and the periphery electronics and its simulation. We will carry out a post-layout simulation of the double column and the EOC. We will also perform a functional verification of the digital part of the chip in a FPGA using a pixel timing library generated previously.

7. Conclusions

The RD50-MPW2 pixel performance in terms of leakage current and breakdown voltage has improved greatly with respect to the RD50-MPW1. The measurements with irradiated RD50-MPW2 samples show a good device performance as well. The RD50-MPW2 active matrix configuration and readout electronics has been also tested for non irradiated devices with good results. Finally, the new RD50-MPW3 design is currently ongoing. The next steps will be to perform C-V measurements with the RD50-MPW2 test structures, the RD50-MPW2 active matrix characterization of irradiated devices and the finalization of new RD50-MPW3 chip design and its submission in 2021.

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Work performed in the framework of CERN RD50 collaboration.

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