Power Quality Improvement of Electrical Power Systems within More Electric Aircraft

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Abstract

The application of more-electric aircraft concept will see a significant increase of electrical power demands with newly developed electrical loads. This will make it essential to extract electrical power from both high-pressure and low-pressure shafts of an aircraft engine for future aircraft. With each shaft driving one electrical generation subsystem, an advanced dual-channel power generation system can be formed. The dual-generation architecture can significantly reduce the fuel assumption of aircraft engines through power transfer between different engine shafts. In such a system, two permanent magnet synchronisation generators (PMSGs) will supply a common DC bus through their dedicated AC-DC converters.

On the load side, a significant penetration of power electronics is foreseen as they are essential elements to interface load and the DC bus. With an increased number of power electronic converters, harmonics from these converters will impose significant power quality challenges to the electric grid. A capacitor is required to filter the switching harmonics in the DC bus to ensure that its voltage is within the required range. However, due to a high current rating, this capacitor will be bulky and heavy.

This thesis aims to address the power quality issues for the common DC bus electrical power system architecture considering a dual-channel power generation system. To improve the power quality on the DC bus, switching harmonic component cancellation schemes are proposed for different cases. In the first case, two PMSGs are considered to supply the DC bus through AC/DC converters. In this case, the modulation scheme (either SPWM or SVPWM) of one AC-DC converter is controlled to actively cancel one specific harmonic component on the DC bus. After the first case study, the use of a bidirectional buck-boost DC-DC converter as a harmonic absorber with the proposed equal-gate-width (EGW) modulation scheme is considered. The proposed method allows for the active control of the magnitude and phase angle of some specific

harmonic component and thus can be used to suppress the required harmonic component on the DC bus. Simulation and experimental results have demonstrated the high robustness and effectiveness of the proposed methods.

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List of Terms

A_k	Fourier coefficients of $i_{dc}^{[b]}$
C_b	DC-link capacitance
D	Duty cycle
ΔD	Bias duty cycle in EGW PWM
f_0	Fundamental frequency from PMSG
$\hat{f}_0$	Measured fundamental frequency from PMSG
f_c	Switching frequency
$f_c^{[b]}$	Carrier frequency of the DC-DC converter
f_{kf}	Frequency of kfth order harmonic
i, j	Switching and band side orders of DC-side current harmonics
i_d	d-axis current
i_q	q-axis current
i_c^{max}	Maximal phase current
i_{dc}	DC-side current
$i_{dc,i,j}(t)$	DC-side current in the frequency of $if_c + jf_0$
$i_{dc}^{[b]}$	DC-side current from the ESS system
$i_{dc}^{[g]}$	DC-side current from the PMSG system
i_o	Output current for loads
$I_1^{\{1\}}$	Magnitude of the first DC-side switching harmonic from Converter 1
$I_1^{\{2\}}$	Magnitude of the first DC-side switching harmonic from Converter 2
$I_2^{\{1\}}$	Magnitude of the second DC-side switching harmonic from Converter 1
$I_2^{\{2\}}$	Magnitude of the second DC-side switching harmonic from Converter 2
I_{ac}	Amplitude of the fundamental component of AC current

I_{dc}	DC component of the current i_{dc} on DC-bus
$I_{dc,i,j}$	Magnitude of DC-side current harmonics in the frequency of $if_c + jf_0$
$I_{dc,i,j}^{[g]}$	Magnitude of DC-side current harmonics in the frequency of $if_c + jf_0$
$I_{dc,i,j}^{[g1]}$	Magnitude of DC-side current harmonics from PMSG 1 in the frequency of $if_c + jf_0$
$I_{dc,i,j}^{[g2]}$	Magnitude of DC-side current harmonics from PMSG 2 in the frequency of $if_c + jf_0$
I_{dci}	Output current of the converter #i
I_{hf}	Total harmonics on DC capacitor
I_{kf}	Magnitudes of summed kfth order harmonic from all converters connected to the common dc bus
I_L	DC component of the inductor current
k	k=0, 1 and 2 represent phase A, B and C respectively
k_{di}	Droop coefficients of the converter #i
k_{ic}	Integral gain of the current regulator
k_{pc}	Proportional gain of the current regulator
K	Power sharing ratio between the two AC-DC converter
$K_{m,n}$	Harmonic amplitude of switching function
L_d	d-axis inductance
L_q	q-axis inductance
M_{high}	Maximum modulation index
P	Converter power
P_{cpl}	Total power of the CPL
P_{res}	Total power of the resistive load
R	Stator resistance
R_{bat}	Output resistance of battery
R_i	Cable resistance of converter #i
R_{res}	Resistance of the resistive load
$sf(t)$	Switching function of the AC-DC converter

T_0	Dwell time for vector $\overrightarrow{V_0}$
T_1	Dwell time for vector $\overrightarrow{V_1}$
T_2	Dwell time for vector $\overrightarrow{V_2}$
$T_c^{[b]}$	Carrier cycle time of EGW PWM
$T_{con}^{[b]}$	Carrier cycle time of conventional PWM
ΔT	Phase-shift time
T_s	Switching cycle
v_{ab}	Line-to-line voltage
V_{ac}	Magnitude of converter phase voltage
V_b	Voltage of common DC bus
V_{bat}	Open-circuit voltage of the battery
v_c^{max}	Maximal phase voltage amplitude at the fundamental frequency
V_{cr}	Peak values of carrier waves
v_d	*d*-axis stator voltage
v_q	*q*-axis stator voltage
V_{dci}^*	Calculated voltage reference for converter #*i*
V_o	Rated voltage
$\overrightarrow{V_{ref}}$	Reference vector
α	Power factor angle
β	Angle between phase current and its AC side voltage
ζ	Damping ratio
θ_c	Angle of the carrier signal
$\Delta\theta_c$	Phase-shift angle between the two AC-DC converters
$\theta_c^{[b]}$	Carrier angle of EGW PWM
$\theta_c^{[k]}$	Phase angle of the triangular carrier signal for each leg
$\theta_c^{\{1\}}$	Phase angle of carrier signals on converter {1}
$\theta_c^{\{2\}}$	Phase angle of carrier signal on converter {2}
$\sigma_{m,n}^{[k]}$, $\varphi_{m,n}^{[k]}$	Phase angles of components in switching function (3.2)
φ_m	Flux linkage of the permanent magnet

ω_e	Electrical rotor angular velocity
ω_n	Natural bandwidth

Chapter 1

Introduction

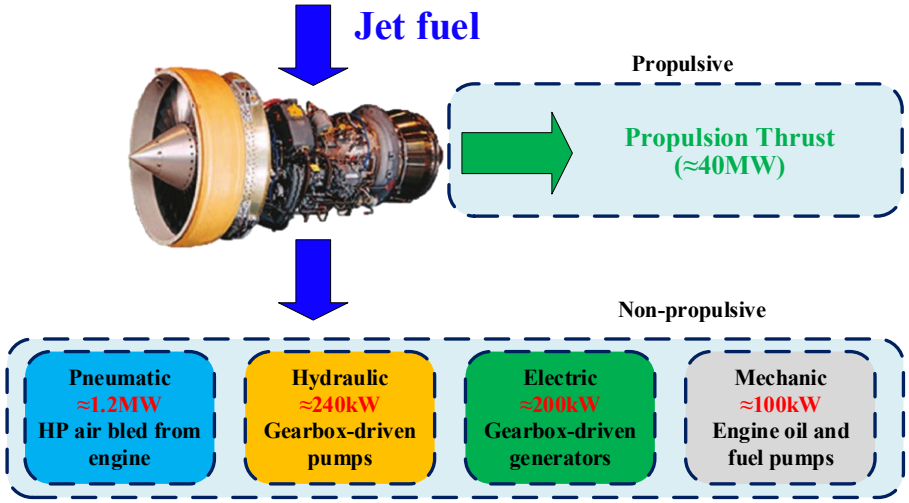
1.1 More Electric Aircraft

In recent years, aircraft have been widely accepted as a convenient way to travel, as they allow long-distance, high-speed and in some circumstances more fuel-efficient travel compared with other commuting methods. Therefore, the aerospace industry is growing at a phenomenal pace. It is estimated that by 2030, approximately 27,000 new aircraft will be in the air. The aerospace industry is therefore considered vital to today's world community, enabling strong annual economic growth worth $425bn in GDP worldwide [1].

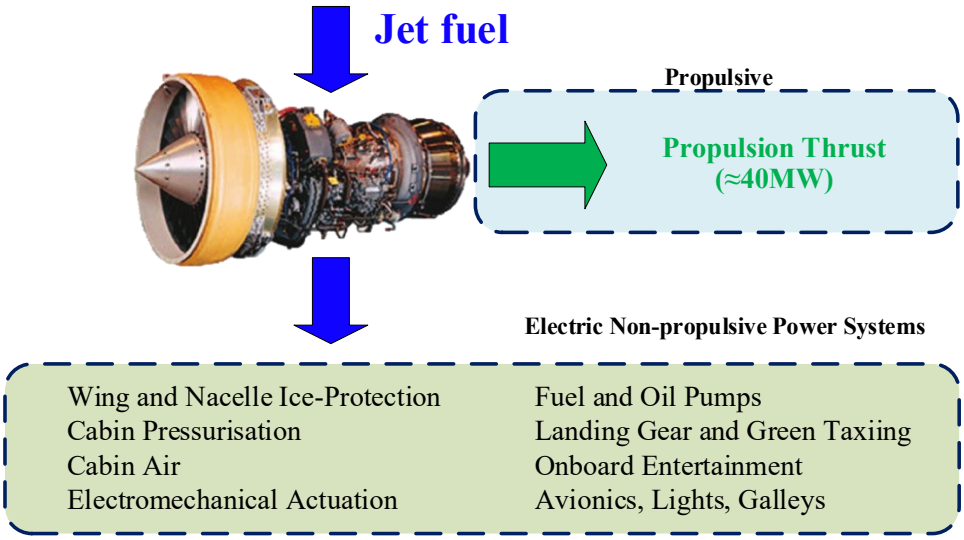
The impact of aircraft on the environment and climate is not negligible, especially the aviation industry is one of the fastest growing sources of greenhouse gas emissions. If expansion trends in the aviation industry progress at the current pace, aircraft will be a big source of pollution for years to come [2]. As a result, the aerospace industry has started to pay more attention to the use of technology to achieve more efficient and environmentally friendly solutions. Due to the rapid development of power electronics, electrical machines and advanced control, the more electric aircraft (MEA) has become the dominant trend in the aerospace industry [3]-[9]. Compared with conventional aircraft, MEA has great potential to reduce fuel burn and CO_2 emissions. Within an MEA, subsystems that used to be driven by hydraulic, mechanical, and pneumatic power are replaced by electrical ones [3], as shown in Figure 1.1a and Figure 1.1b.

Compared with conventional aircraft, the MEA offers significant cost benefits due to fewer parts, integration of key subsystems, and multi-use of components.

It also reduces the overall cost of operation and ownership because its more-electric architecture helps reduce fuel consumption per passenger per mile, increasing overall aircraft performance and energy usage.



(a)



(b)

Figure 1.1: Change in non-propulsive power in conventional aircraft and more electric aircraft. a) Conventional aircraft. b) More electric aircraft.

In conclusion, the implementation of the MEA concept has revolutionised the aerospace industry. With this concept, a significant reduction of weight, cost, and fuel consumption can be achieved.

1.2 Electrical Power Generation Onboard Aircraft

Nowadays, there are three typical generation systems for electrical power onboard aircraft, which are:

- Constant speed constant frequency (CSCF)
- Variable speed constant frequency (VSCF)
- Variable speed variable frequency (VSVF)

The usage of these three types of electrical power generation systems in recent aircraft is listed in Table 1-1.

Table 1-1: AC electric power system in recent civil and military aircraft[31].

Type of power system	**Civil aircraft**	**Military aircraft**
CSCF	B777 2*120kVA A340 4*90kVA MD-12 4*120kVA B747-X 4*120kVA B717 2*40kVA B737NG 2*90kVA B767-400 2*120kVA	Eurofighter Typhoon
VSCF 115VAC	B777 2*20kVA MD-90 2*75kVA	F-18C/D 2*40/45kVA F-18E/F 2*60/65kVA
VSVF 115VAC	Horizon 2*20/25 kVA A380 4*150kVA	Boeing JSF 2*50kVA
VSVF 230VAC	B787 4*250kVA A350 4*100kVA	

1.2.1 Constant speed constant frequency

A constant speed constant frequency (CSCF) generation system is shown in Figure 1.2. There, a constant speed drive (CSD) is used between an engine shaft and an electrical generator. The CSD converts a time-varying rotating speed of an engine shaft to a constant speed and drive a three-phase generator. A fixed frequency of the three-phase generator is thus achieved.

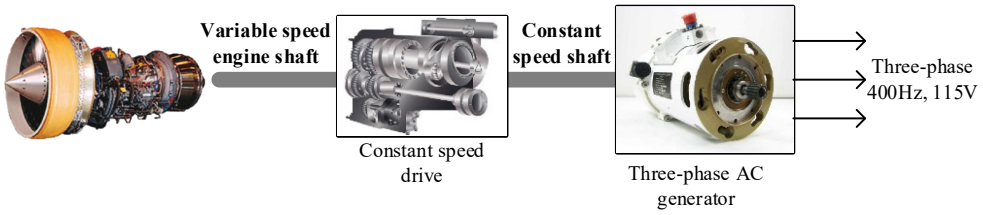


Figure 1.2: Constant speed constant frequency generation system.

The CSCF system provides high reliability and has been well developed over the decades. As shown in Table 1-1, it is still employed in modern aircraft such as the Boeing 777. However, the cost of purchase and maintenance of the CSD can be high due to the complexity of the hydro-mechanical drive system [11]. Besides, the use of CSD reduces the reliability of the system. Hence, this topology is not the best choice for future aircraft.

1.2.2 Variable speed constant frequency

Variable speed constant frequency (VSCF) is shown in Figure 1.3. An AC electrical generator is directly driven by the engine gearbox which produces three-phase AC voltage at variable frequencies. The variable frequency is due to the variable speed of the engine shaft. Three-phase voltages are then fed into an AC-AC converter that converts the variable-frequency power to a constant frequency of 400 Hz.

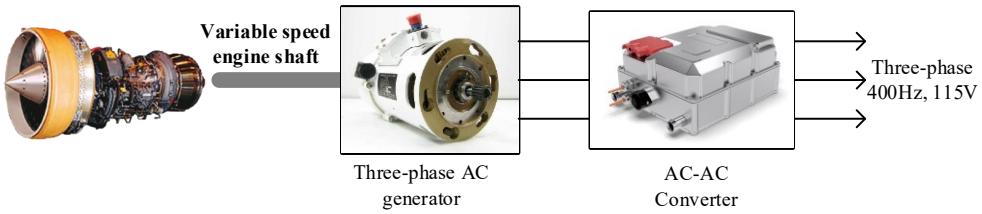


Figure 1.3: Variable speed constant frequency generation system.

In such a VSCF generation system, no CSD is needed between the engine gearbox and the generator. However, the drawback is that this power converter must process all the generated power. Therefore, it must have a full power rating and high reliability to get the required level of safety from the aircraft design.

1.2.3 Variable speed variable frequency

To avoid the reliability issue of the VSCF solution, the power converter can be taken out of the generation system. This results in the variable speed variable frequency (VSVF) configuration as shown in Figure 1.4. The engine shaft directly drives the AC generator and supply to the downstream loads. As the engine speed is not constant, the AC frequency from the generator will thus be changing in the range of 320–800 Hz [12].

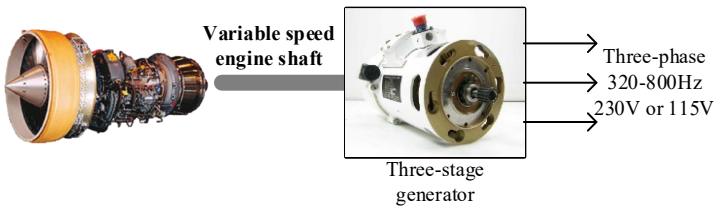


Figure 1.4: Variable speed variable frequency generation system.

To connect this AC power with a variable frequency, nearly all aircraft loads will require power converter based interfaces. As a result, power electronic converters are required locally.

1.2.4 DC Power Generation

Due to the recent development of power electronics, the DC power system has become a potential solution for future aircraft. Indeed, the DC power has been used on military aircraft (F35) and part of the electric power system on Boeing 787. Figure 1.5 shows a DC power generation system with a variable frequency generator supplying an AC-DC converter. The AC electrical power from the generator is rectified to a DC power of 270 V or 540 V [13].

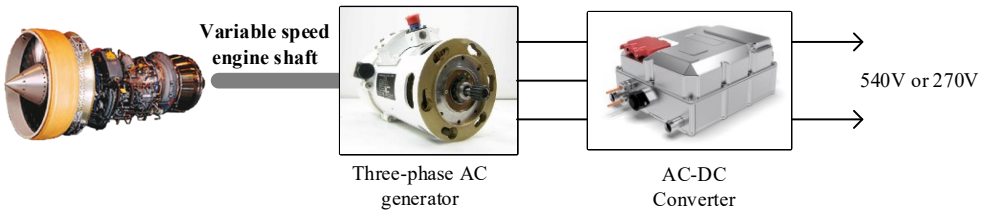


Figure 1.5: DC-voltage generation system

The benefits of such a DC power generation system can be summarised as follows:

- Lower losses in the power transmission cables. This is due to the fact that only two conductors (positive and negative) are required in DC distribution, whereas three conductors (three phases) are required in AC distributions [14].
- The reduction of the skin effect in DC can reduce power loss and also significantly reduce the dielectric losses in the power cables.
- No need for any reactive power compensation equipment: the capacity of wires and devices can be reduced because it does not need to distribute/process the reactive power [14].
- Convenient for parallel power supplying and integrating energy storage system (ESS).

With these potential benefits, the DC power system has attracted great attention in recent years. In addition, such DC generation systems have been widely

considered not only for MEA, but also for hybrid vehicles [15], ships [16] and microgrids [17].

The DC systems are applied in a large variety of applications, and consequently, different architectures have been proposed such as single bus, multi-bus, ring bus configurations. Due to its simplicity, as shown in Figure 1.6, the "single bus" EPS architecture is one of the promising candidates for future MEA.

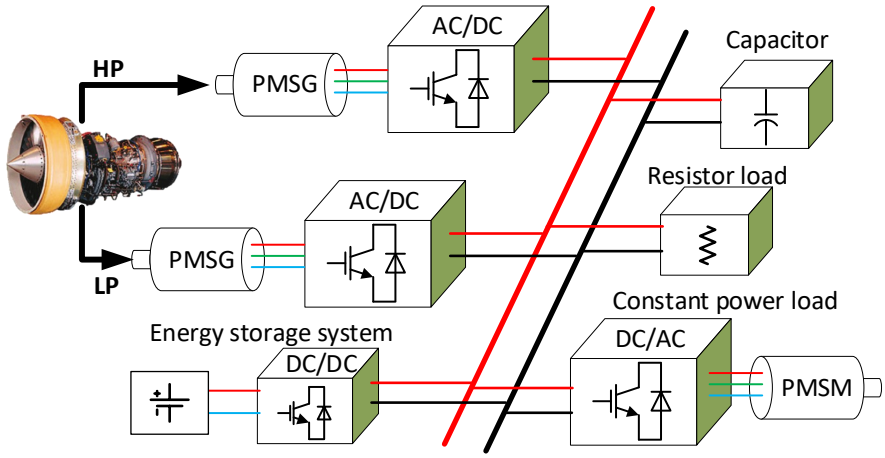


Figure 1.6: "Single bus" EPS structure.

In Figure 1.6, two permanent magnet synchronised generators (PMSGs) supply power to a DC bus through AC/DC converters. An energy storage system (ESS) is connected to the DC bus through a bi-directional DC-DC converter. All kinds of load, i.e., resistive loads and electrical drive loads etc, are supplied by the DC bus. With this structure, the EPS readily permits the paralleling of multiple sources and enables the application of variable-frequency power to be more convenient.

1.2.5 Dual-Channel Power Generation

In recent decades, the turbofan engines are widely used for civil aircraft. In such engines, as shown in Figure 1.7, the air sucked by the turbofan is divided into two parts. Most of the air will go through the bypass channel and the rest will go through the engine core. The air passing through the engine core will be

compressed by a low-pressure compressor and a high-pressure compressor. After two-stage compression, this high-pressure air will be mixed with fuel in the combustion chamber. With ignition, the produced hot air will pass through a high-pressure turbine and then a low-pressure turbine. The high-pressure turbine (HPT) in return will drive the high-pressure compressor (HPC) through the high-pressure (HP) shaft, and the low-pressure turbine (LPT) will drive the fan and low-pressure compressor (LPC) on the low-pressure (LP) shaft [26].

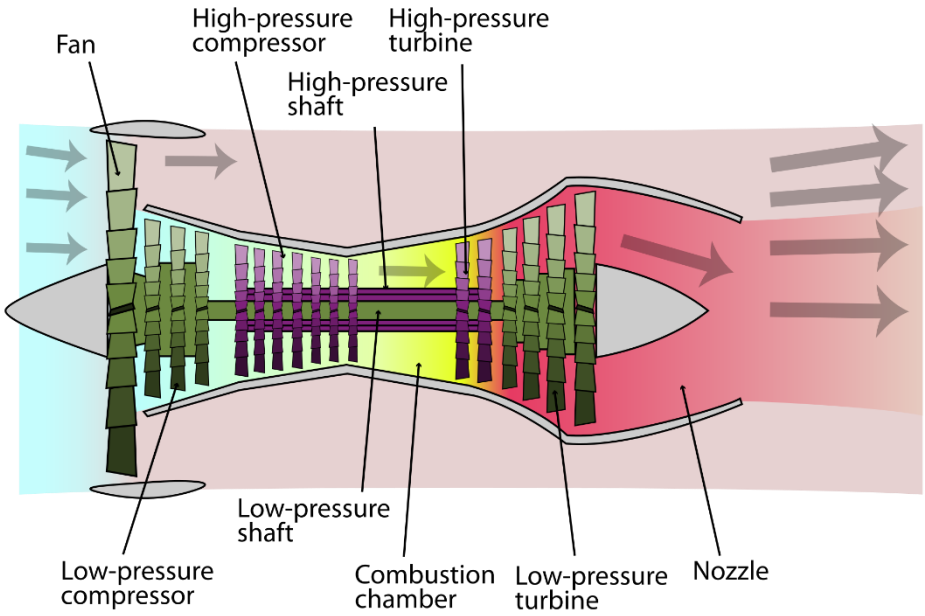


Figure 1.7: Schematic of a twin-spool, high-bypass turbofan engine.

Conventionally, the electric power on an aircraft is extracted from the aircraft high-pressure engine shaft. With increased load onboard the MEA, extracting electrical power from the high-pressure shaft only is not viable as too much power extracted from the high-pressure shaft may result in compressor surges. A compressor surge happens when a downstream blade row cannot utilise the flow delivered by the upstream ones. Surges can lead to mechanical damage to the compressor blades and the thrust bearings due to large fluctuations of airflow and the direction of forces on the rotor [19]. To extract more electrical power from an engine core whist avoiding a compressor surge, it is essential to extract power from both high-pressure and low-pressure shafts. By doing so,

power transfer between the two engine shafts in an electrical way will become feasible and this will improve engine efficiency and further increase engine operation regimes.

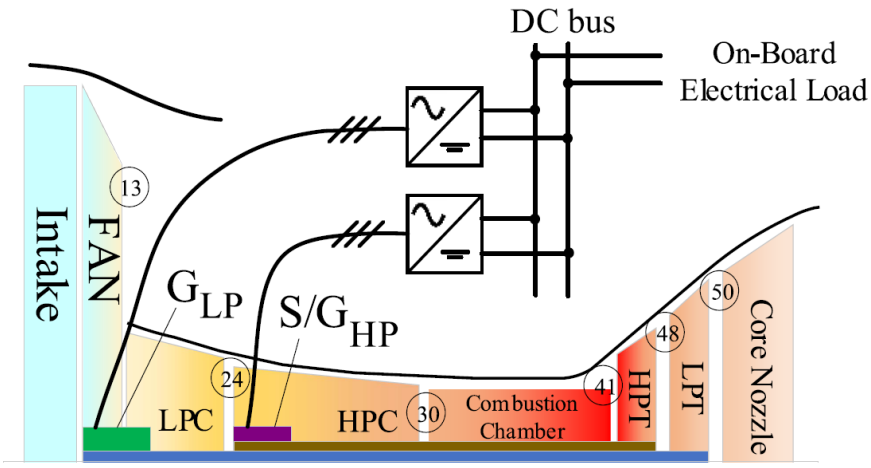


Figure 1.8: Concept diagram of the dual-channel power generation system [18].

In [27], authors proposed an advanced dual-channel electric power generation architecture, as shown in Figure 1.8. In the proposed system, two electrical generators are driven by two engine shafts, i.e., high-pressure shaft and low-pressure shaft, respectively. These two generators supply one common DC bus through the power electronic converters. The authors have concluded that this architecture enables dual-channel power generation and power transferring between two engine shafts. The enabled power transfer between two engine shafts results in improved engine efficiency and stability, as well as compatible thrust with flight mission [27]. At last, the fuel consumption and maintenance cost can be significantly reduced for the aircraft.

1.3 Active Switching Harmonic Suppression of the DC-Link Capacitor Currents

1.3.1 Power quality improvement

One aspect that needs to be considered for the dual-channel generation system is its power quality. In conjunction with a growing number of power electronics devices, more current harmonics will be injected into the DC bus. These harmonics will have short-term and long-term effects on both grids and grid-connected equipment [30].

In a DC power system, capacitors are normally used to filter most of the voltage fluctuations. Capacitors are critical components for power quality improvement. Nowadays, electrolytic capacitors, film capacitors, and ceramic capacitors are widely used as dc-link capacitors. For aircraft applications, the weight and volume are critical design factors and should be minimised during the design process. Moreover, reducing harmonics on a DC bus can potentially extend the lifetime of capacitorsand thus improve the reliability of the entire system [31]-[37].

There are numerous methods proposed recently to actively minimise the current ripple on the capacitors [42]-[48]. However, these papers focused on ripple in the range of the fundamental frequencies and essentially to improve system stabilities when a dc-link is supplying an or multiple electric drive loads. Some of these techniques proved their efficiency in stabilising the dc-link variables even for large disturbances. However, the control bandwidth of these methods is mostly far below the switching frequency. This means that current harmonics due to the switching behaviour of converters are filtered out in the control loop, and these algorithms are not able to mitigate such current harmonics flowing into the DC-bus capacitor. Therefore, this thesis aims to contribute to knowledge in this area and propose simple methods which can suppress the switching harmonics of a dc bus with connected multiple power converters.

1.3.2 Harmonics suppression using additional DC-DC converters

Adding additional circuits is straightforward solution for reducing capacitor harmonics at switching frequencies [49]-[56]. Having the switching frequencies of additional power devices been higher than those of the main converters, the harmonics on the capacitors can be suppressed. Existing methods by using additional switching devices can be classified into two topologies as follows.

- A parallel-connected bidirectional dc–dc converter, terminated by small auxiliary capacitance, replaces the bulk dc-link capacitance, as shown in Figure 1.9. The system reduces the dc-link ripple by diverting the pulsating portion of instantaneous power into the auxiliary capacitance.
- A series-connected bidirectional dc–dc converter, terminated by small auxiliary capacitance, replaces the bulk dc-link capacitance [57][58], utilising the same principle as the previous subgroup.

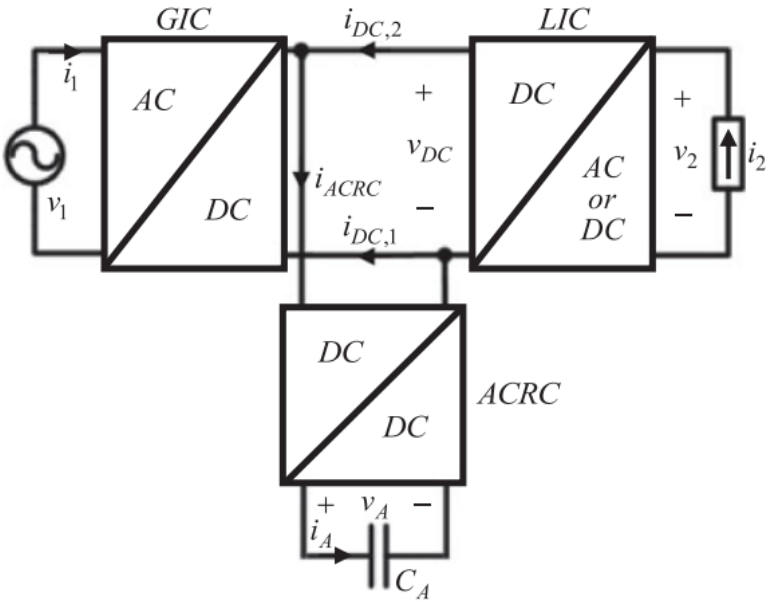


Figure 1.9: Harmonic suppression using additional switches [49].

This concept of suppressing harmonics can be implemented in either AC or DC power system with power electronic devices. However, it requires extra elements and thus increases the cost and complexity of systems.

1.3.3 Harmonic suppression for single AC-DC converters

In recent years, researchers have published several papers on the reduction of switching harmonics for single two-level converter dc-link capacitors [59]-[64]. In [59], a mathematical model of DC-link currents is developed using a Double Fourier solution. It gives researchers an analytical starting point to the current harmonics for a two-level AC/DC converter. In [61], the capacitor current ripple is reduced by applying nonadjacent switching vectors.

Some researchers have investigated suppression methods when one or more DC-DC converter is connected with an AC-DC converter. Modifying switching actions on the DC-DC converter is the critical thought in these papers. In [60], suppressed capacitor harmonics are achieved by implementing a high modulation index on the DC-AC inverter and using an additional DC-DC converter. However, the DC-link voltage becomes variable, which is not the case in the DC power system (The voltage should be controlled at a certain level). In [62]-[64], the researchers investigated minimising harmonics when a boost converter is connected with a two-level DC-AC inverter using time-domain analysis. There, switching actions of the DC-DC converter need to be adjusted in every switching cycle, and this comes with high calculation efforts

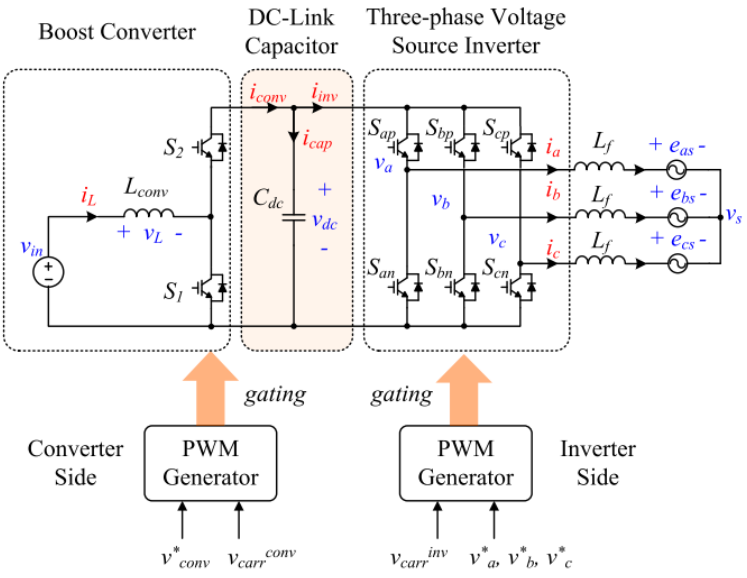


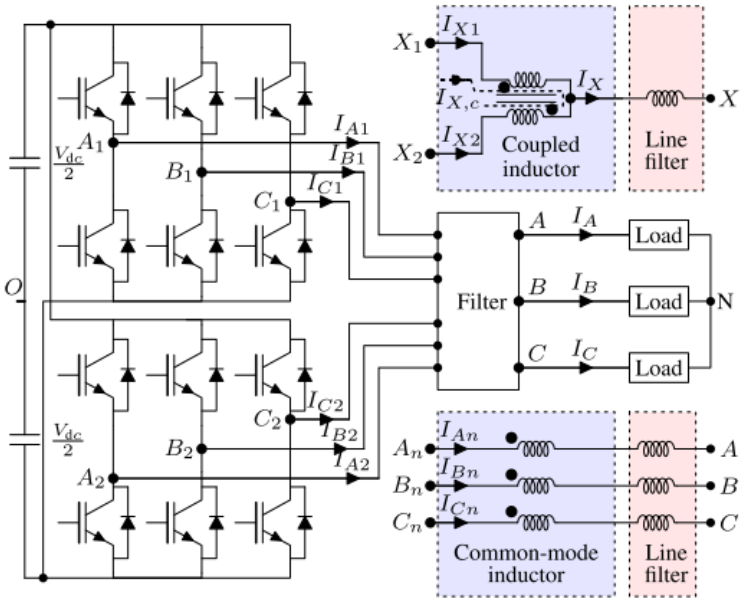
Figure 1.10: DC-DC converter connecting with a three-phase inverter [64].

and thus long calculation times. Hence, they are not suitable for AC-DC converters which are connected to high-speed PMSGs in MEA applications.

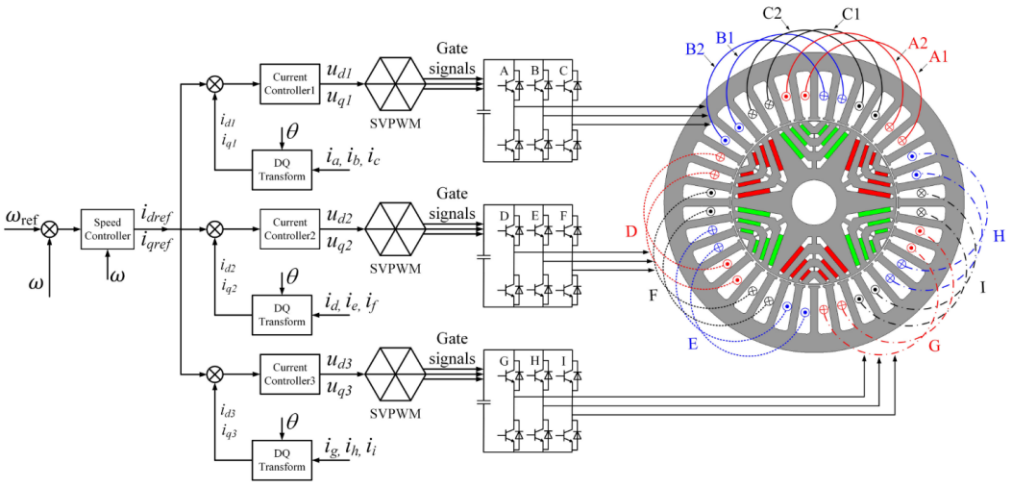
1.3.4 Harmonic suppression for multi-converter systems

For DC electrical power systems with two or more AC-DC converters, the fundamental frequencies of generators are always assumed to be the same in recent publications[65]-[72]. Figure 1.11a and b show two typical systems in these publications. Phase-shift actions among the converters always achieve the switching harmonic minimisation. In Figure 1.11a, the three-phase load is supplied by two parallel-connected converters. The dc-link capacitor-current ripple reduction can be achieved applying a phase shift between the two PWM carriers of the converters, either 0° or 90° depending on the modulation scheme. In Figure 1.11b, windings in the PMSM are split into three channels, and the phase shift methods can also be used to reduce dc-link harmonics where the phase shift angle is dependent on the topology of the multiphase machine.

These two cases in Figure 1.11a and b are different from the dual-channel power generation architecture of the type considered in this thesis. In the dual-channel power generation architecture, the electrical generators are driven by different shafts, thus with different fundamental frequencies. For such a system, shown in Figure 1.8, different fundamental frequencies are applied to their dedicated AC/DC converters. To the best of the authors' knowledge, there are so far very limited publications addressing this issue and illustrating how to minimise the switching harmonics when the fundamental frequencies are different. Although this thesis focuses on the dc-bus supplied by two generators through AC-DC converters, the proposed method and analysing technique can be extended to back-to-back converters or any microgrid with multiple AC-DC or DC-DC converters.



(a)



(b)

Figure 1.11: Multi-converter system with the same fundamental frequency. a) parallel interleaved converters[67]. b) Triple three-phase machine [76].

1.4 Objectives of Thesis and Thesis Structure

1.4.1 Objectives

Following a literature review of the active harmonic suppression methods, this work aims to improve the power quality of DC systems in MEA by suppression of harmonic components at switching frequency levels, as shown in the orange bars in Figure 1.12. In Figure 1.12, f_c is the switching frequency of converters. The harmonics components selected for suppression in this work are those around or above the switching frequency.

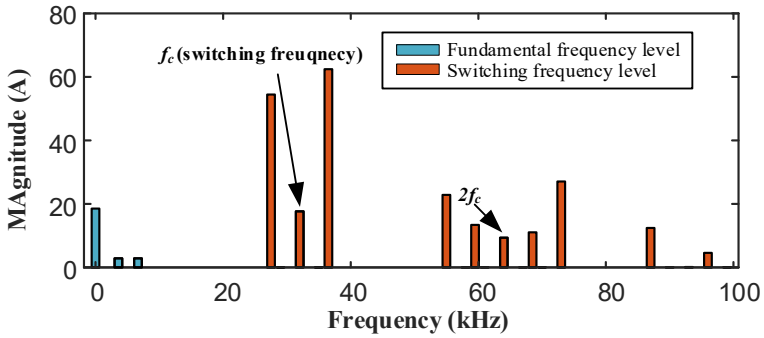


Figure 1.12: Spectrum of DC-side current.

Objectives of this work are listed as follows:

A. Proposal of a method to suppress harmonic component as twice the switching frequency when two PMSG-fed AC/DC converters work under SPWM operation (Chapter 3). harmonic suppression method is proposed based on a simplified mathematical model of the second carrier harmonic from a two-level AC-DC converter developed in Chapter 3. The proposed method can work under any rotor speed and power sharing ratio.
B. Proposal of a method to suppress capacitor harmonics when two PMSG-fed AC/DC converters operate with SVPWM scheme (Chapter 4). The proposed method can suppress both the first and the second order harmonics based on an optimised phase-shift angle.

C. Proposal of a method to suppress first-band switching harmonics when the system augmented with a DC-DC converter (Chapter 5 and Chapter 6). An adjustable PWM method for the DC-DC converter is proposed. Using an optimised phase-shift angle together with a synchronisation approach, the first band switching harmonics are suppressed.
D. Built a new test rig for the experiment (Chapter 7). Develop an interface board based on TI DSP 28379D. Using Matlab/Simulink to generate C code for the controller.

Although the context of the work is based on a dual-channel power generation system, it can be also considered to be a challenging case of multi-converter system with common DC bus, such as back-to-back converters, electric vehicles. Thus, the analysis presented afterwards can further be applied to optimise these applications as well.

1.4.2 Thesis structure

To describe the objectives in this thesis with a logical way, this thesis will be arranged as follows:

Chapter 2 provides the fundamentals of the dual-channel power generation architecture. Models of individual components are introduced, including the PMSG(s), batteries, AC-DC converters, DC-DC converter. Then, this chapter presents the basic control schemes for both local and system-level controller. Finally, the basic theory of SPWM and SVPWM methods are introduced and compared.

Chapter 3 develops a method to suppress capacitor harmonic when two PMSGs works under carrier based PWM operation. A mathematical model to estimate the second carrier current harmonic on the DC-link harmonic of the two-level AC-DC converter is presented. The results show that the magnitude of the harmonic component was only determined by the value of the DC current and modulation index of the converter, while the carrier phase angle results in the phase angle of the DC-side harmonics. Based on a simplified model, a second

carrier harmonic cancellation method was proposed by actively controlling modulation index together with a phase shift angle on the carrier signal. Finally, simulation is implemented to verify the validity of the proposed second carrier harmonic model and cancellation method.

Chapter 4. extends the work from Chapter3 to suppress the current harmonics on DC-link when the PMSGs works under SVPWM operation. SVPWM gives the AC-DC converters higher voltage utilisation ratios. Hence it is suitable for PMSGs operating at high speed. Unlike the proposed method in Chapter 3, in which only the second carrier harmonic is analysed, this chapter will present simplified mathematical models for both the first and second carrier harmonics on capacitors. Based on the simplified models, the active phase-shift angle will be generated to suppress the total harmonic on the DC-link capacitor. The analysis shows that the method will mostly suppress the first switching harmonic under a low output power range but mostly suppress the second carrier harmonic more as the output power increases. Lastly, this chapter validates the proposed mathematical models and suppression method with simulation results.

Chapter 5 describes suppression methods when the system incorporated a battery and a DC-DC converter. Firstly, this chapter presents a harmonic analysis of a two-level AC-DC converter. Harmonics in the first band switching frequency is selected for suppression based on a mathematical comparison. Then, this chapter proposes a new PWM method of a DC-DC converter for adjusting the magnitudes of harmonics. Based on the harmonic analysis of both the AC-DC and the DC-DC converter, a harmonic suppression method is proposed. In this method, synchronsisation action is also considered.

Chapter 6 combines the suppression methods in Chapters 3 and 5 altogether to suppress the first sideband and the second carrier harmonics at the same time. To efficiently suppress the most significant component, a component selection block is designed in the controller of the DC-DC converter.

Chapter 7 deals with the experimental support of the analytical results of the previous chapters. The chapter presents the experimental platform and lab

prototype setup. Experimental results are shown to support the analytical results of previous chapters.

Chapter 8 contains the conclusion of the thesis. It summarises the work and the primary outcome of the PhD research work. It also provides possible future research that can be developed from the work of the thesis. The publications from the research are also given.

Chapter 2

Fundamental Models and Operation of a Dual-Channel Power Generation System

As discussed in Chapter 1, this thesis focuses on power quality improvement of the dual-channel power generation system. Consequently, this chapter will provide the fundamental operation theories for the dual-channel power generation architecture in the MEA. Control methods for permanent magnet synchronised generators (PMSGs) and the energy storage system (ESS) are also discussed. Furthermore, the content of this chapter will serve as the basis for the proposed methods of power quality improvement.

2.1 Introduction

An example architecture of a dual-channel generation system used for the initial study is shown in Figure 2.1. It consists of several components, which are

1) Generators: The power on the DC power system is mainly supplied by two permanent magnetic synchronised generators (PMSGs) which extract power from the HP and LP shafts of the engine. Depending on the flight scenario, the system can be operated with only one active source, or with multiple sources feeding the same DC bus.
2) Energy storage system (ESS): Energy storage system is also integrated for emergency status operation. To achieve a flexible power flow in the

system, a bi-directional DC-DC converter is also implemented. Therefore, the battery can operate under either discharging or charging mode depending on supervision control.

3) DC-bus capacitor: With a capacitor bank, high-frequency fluctuation of current can be filtered, which helps flatten the DC-bus voltage.
4) Power load: The onboard loads are represented by a combination of conventional resistive loads and by constant power load (CPL) typically driven by tightly controlled power electronics. Here, a permanent magnetic synchronised machine (PMSM) is given as an example.

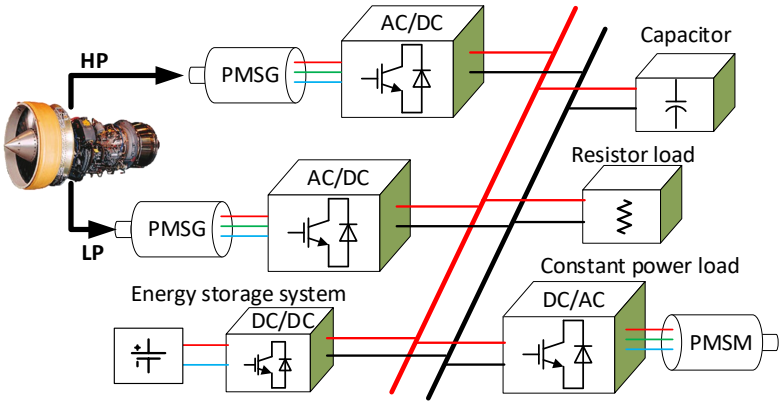


Figure 2.1: Typical dual-generation power system

It is necessary to introduce the characteristics of each part of the electrical power system (EPS) to have a complete understanding of the system.

2.2 Permanent Magnet Synchronised Generator (PMSG) System

2.2.1 PMSG modelling

Three-phase PMSG has been widely used in power generation in recent decades. To avoid the complexity associated with the calculation of three phases, it is widely adopted that PMSG are modelled in synchronously rotating

reference frame (i.e., *dq* frame) [1]. The dynamic equations for PMSG in the *dq* frame are as expressed in (2.1).

$$\begin{cases} v_d = Ri_d + L_d \dfrac{di_d}{dt} - \omega_e L_q i_q \\ v_q = Ri_q + L_q \dfrac{di_q}{dt} + \omega_e L_d i_d + \omega_e \varphi_m \end{cases} \tag{2.1}$$

where v_d, v_q, i_d, i_q, L_d, L_q, R, φ_m, ω_e represent *d*-axis stator voltage, *q*-axis stator voltage, *d*-axis current, *q*-axis current, *d*-axis inductance, *q*-axis inductance, stator resistance, flux linkage of the permanent magnet, and electrical rotor angular velocity respectively. Model diagram based on (2.1) is shown in Figure 2.2 within the orange block.

In this study of the dual-channel power generation system, surface mounted PMSG is assumed to be used because of its mechanical benefit for high-speed operation [1]. Furthermore, the *d*- and *q*-axis inductance are considered to be identical (L_d=L_q=L_s) in the case of the surface-mounted PMSG. Hence, the equation (2.1) can be re-written as the expression in (2.2).

$$\begin{cases} v_d = Ri_d + L_s \dfrac{di_d}{dt} - \omega_e L_s i_q \\ v_q = Ri_q + L_s \dfrac{di_q}{dt} + \omega_e L_s i_d + \omega_e \varphi_m \end{cases} \tag{2.2}$$

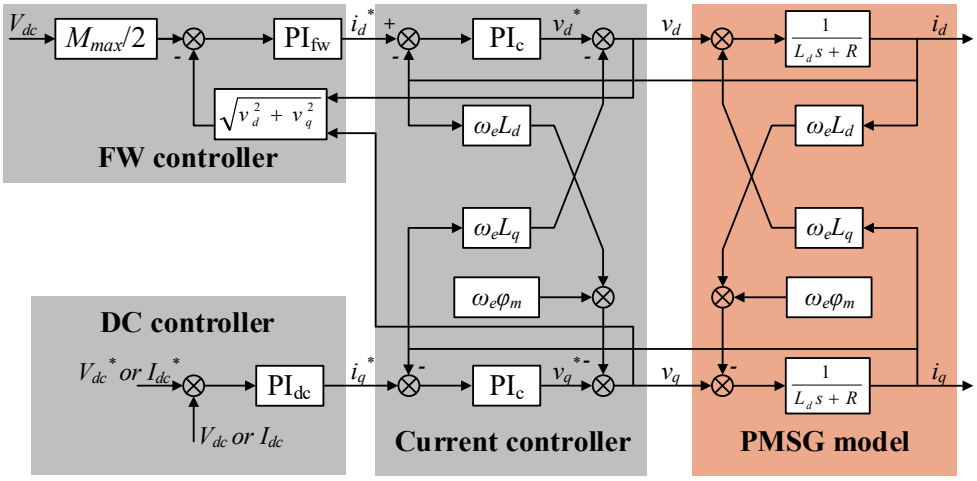


Figure 2.2: Diagram of PMSG system.

Maximum allowable phase currents are determined by the designed rated parameters of the converter and machine. The maximum voltage is dependent on the available DC-link voltage and modulation method. The voltage and current limitations can be written as in (2.3) by neglecting stator resistance and the transient terms.

$$\begin{cases} \sqrt{v_d^2 + v_q^2} \le v_c^{max} \\ \sqrt{i_d^2 + i_q^2} \le i_c^{max} \end{cases} \tag{2.3}$$

where v_c^{max} and i_c^{max} are the maximal phase voltage amplitude at the fundamental frequency and maximal phase current, respectively.

2.2.2 Control of the PMSG system

This section will detail the control design for a single generation system (a single source is considered for simplification) based on models illustrated in the previous subsection. The detailed control scheme for generator mode is also shown in Figure 2.2. The flux-weakening controller and DC controller generate the *dq*-current references which are fed to the current controller.

i Current Control

The first stage is to design the current controllers of the starter generator (S/G) power system. It controls *dq*-current (i_d and i_q) following their reference (i_d^* and i_q^*). Figure 2.2 shows the *dq* current loops and their respective control plant. The feedforward terms within the current control plant are used for compensating coupling terms in the PMSG model. Then the transfer function between the *dq*-current and *dq*-voltage can be reduced to a first-order transfer function as expressed in (2.4) and (2.5) for the *d*-axis and *q*-axis current respectively.

$$\frac{i_d}{v_d^*} = \frac{1}{L_s s + R} \tag{2.4}$$

$$\frac{i_q}{v_q^*} = \frac{1}{L_s s + R} \tag{2.5}$$

Applying a PI controller with feedforward elements [80], a closed-loop transfer function can be derived as

$$\frac{i_d}{i_d^*} = \frac{k_{pc} s + k_{ic}}{L_s s^2 + \left(R + k_{pc}\right) s + k_{ic}} \tag{2.6}$$

$$\frac{i_q}{i_q^*} = \frac{k_{pc} s + k_{ic}}{L_s s^2 + \left(R + k_{pc}\right) s + k_{ic}} \tag{2.7}$$

Where k_{pc} and k_{ic} are the proportional and integral gains of the current regulator. The transfer function is similar to an ideal second-order response $G(s)$, which can be written as

$$G(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{2.8}$$

Where ζ is the damping ratio, and ω_n is natural bandwidth. For the current regulator, ζ and ω_n can be expressed as in (2.9) and (2.10) respectively.

$$\omega_n = \sqrt{\frac{k_{ic}}{k_{pc}}} \tag{2.9}$$

$$\xi = \frac{R + k_{pc}}{2 L_s \omega_n} \tag{2.10}$$

To achieve the desired dynamic and statistic response, the values of ζ and ω_n are always set according to fundamental frequency and switching frequency. Then proportional and integral gain of the current regulator can be calculated.

ii DC-Link Control and flux-weakening control

After designing the current controller, the *dq*-current references are discussed here which are generated from flux weakening controller and DC-link controller as mentioned earlier.

The flux-weakening controller remains active during generator mode in order to maintain the stator voltage ($\sqrt{v_d^2 + v_q^2}$) at the required level and avoid overmodulation of the converter. Here,

$$\sqrt{v_d^2 + v_q^2} \leq \frac{M_{\max} V_{dc}}{2} \tag{2.11}$$

Where M_{max} is the maximum modulation index of the converter. This value depends on the modulation scheme, which will be discussed later in Section 2.2.3.

When the machine is rotating beyond the base speed, the flux-weakening operation is activated, and a negative *d*-axis current (i_d^*) is injected. The *q*-axis current reference is set by the outer DC power loop when the system operates in the generation mode. During the flight, the system operates in the generation mode and the *q*-axis current reference (i_q^*) is set by the dc-link current or voltage demands dictated by the specific power sharing method. For instance, current reference should be implemented when the power sharing method is voltage feedback-based droop control (current-mode droop control method), while voltage reference should be implemented when the power sharing method is current feedback-based droop control (voltage-mode droop control method).

2.2.3 PWM Methods for the Two-Level AC-DC Converter

This section focuses on the implementation of the stator voltage, which is also known as the pulse width modulation (PWM) schemes for the two-level AC-DC converter. A carrier based sinusoidal PWM (SPWM) scheme is reviewed, followed by a detailed analysis of the space vector PWM (SVPWM) algorithm.

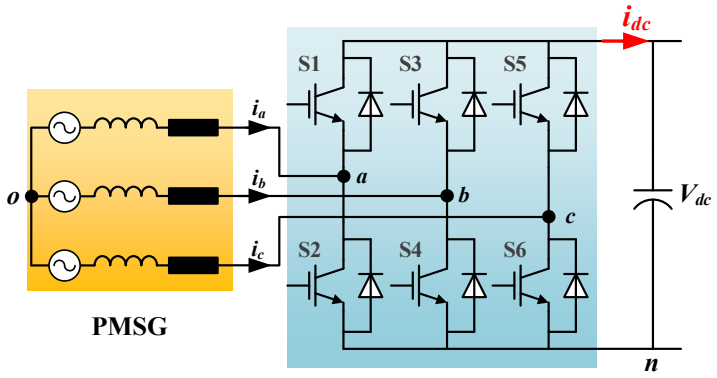


Figure 2.3: PMSG and two-level AC-DC converter.

i Sinusoidal PWM (SPWM)

The principle of the sinusoidal PWM scheme for the two-level AC-DC converter is illustrated in Figure 2.4, where m_a, m_b, and m_c are the three-phase sinusoidal modulating waves which are compared with the triangular carrier wave. The fundamental-frequency component in the converter output voltage can be controlled by modifying m_a, m_b, and m_c. Modulation index of SPWM is

$$M = \frac{V_m}{V_{cr}} \tag{2.12}$$

where V_m and V_{cr} are the peak values of the modulating and carrier waves, respectively. The maximum value of M is

$$M_{spwm,\max} = 1 \tag{2.13}$$

where sinusoidal waveform cannot exceed the magnitude of the triangular carrier wave.

The operation of switches S1 to S6 is determined by comparing the modulating waves (m_a, m_b, and m_c) with the carrier wave. When m_a is higher than the carrier wave, S1 is on and S2 is off in leg A. The resultant converter terminal voltage of phase A (v_{an}) with respect to the negative point of the dc bus (n), is equal to the dc voltage V_{dc}. When m_a is lower than the carrier wave, S1 is off and S2 is on, leading to v_{an}=0, as shown in Figure 2.4. It should be noted that to avoid

possible short circuits during switching transients of the upper and lower devices in an inverter leg, a dead-band time should be implemented, during which both switches are turned off [85]. Dead-band times will distort the switching function of the two-level converter, and thus the AC and DC harmonics. The distortion effect is related to the flow directions of AC currents [106].

The line-to-line voltage v_{ab} can be determined by

$$v_{ab} = v_{an} - v_{bn} \tag{2.14}$$

The waveform of its fundamental-frequency component v_{ab} is also given in Figure 2.4. The magnitude and frequency of v_{ab} can be independently controlled. The fundamental-frequency component v_{ab} increases linearly with M, whose maximum value can be found from

$$V_{ab,\max} = 0.866 V_{dc} \text{ for } M = 1 \tag{2.15}$$

Here, V_{ab} is the amplitude of v_{ab}.

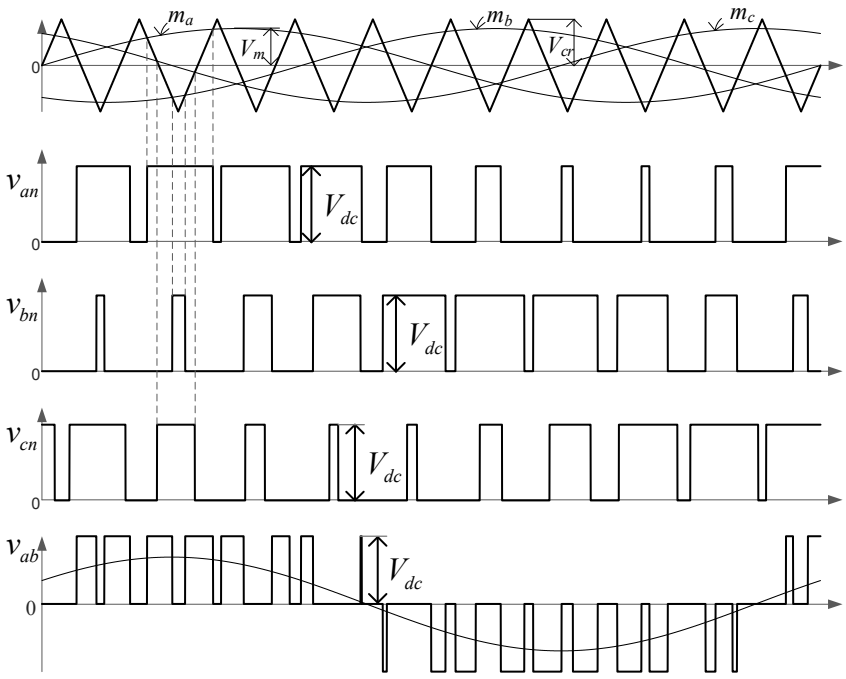


Figure 2.4: Sinusoidal pulse-width modulation (SPWM).

ii Space Vector PWM (SVPWM)

Space vector PWM (SVPWM) is one of the preferred real-time modulation techniques and is widely used for digital control of the AC-DC converters. This section presents the principle and implementation of the SVPWM for the two-level AC-DC converter.

A typical space vector diagram for the two-level AC-DC converter the two-level inverter is shown in Figure 2.5. Six vectors ($\overrightarrow{V_1}$ to $\overrightarrow{V_6}$) split a regular hexagon with six equal sectors (I to VI). The zero vector ($\overrightarrow{V_0}$) lies in the centre of the hexagon. The relationship between the space vectors and their corresponding switching states is given in Table 2-1.

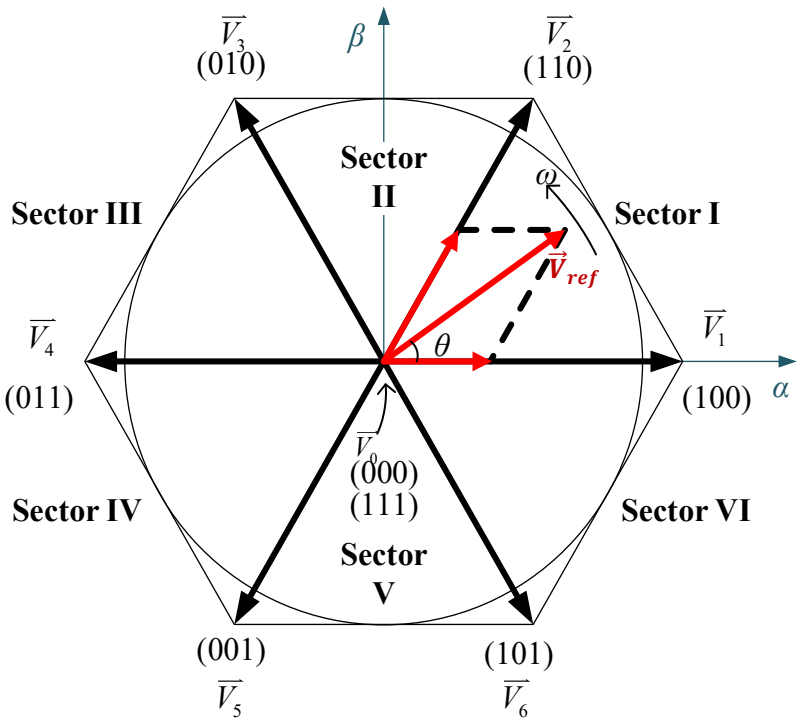


Figure 2.5: Space vector diagram for the two-level converter.

Table 2-1: Space Vectors, Switching States, and On-State Switches

Vector	Switching state	On-state switches
$\overrightarrow{V_0}$	(0, 0, 0) (1, 1, 1)	S2, S4, S6 S1, S3, S5
$\overrightarrow{V_1}$	(1, 0, 0)	S1, S4, S6
$\overrightarrow{V_2}$	(1, 1, 0)	S1, S3, S6
$\overrightarrow{V_3}$	(0, 1, 0)	S2, S3, S6
$\overrightarrow{V_4}$	(0, 1, 1)	S2, S3, S5
$\overrightarrow{V_5}$	(0, 0, 1)	S2, S4, S5
$\overrightarrow{V_6}$	(1, 0, 1)	S1, S4, S5

In Figure 2.5, the reference $\overrightarrow{V_{ref}}$ can be synthesized by three stationary vectors. The dwell time for the stationary vectors essentially represents the duty-cycle time (on-state or off-state time) of the chosen switches during a sampling period T_s of the modulation scheme. The dwell time calculation is based on the 'volt-second balancing' principle, that is, the product of the reference voltage $\overrightarrow{V_{ref}}$ and sampling period T_s equals the sum of the voltage multiplied by the time interval of chosen space vectors.

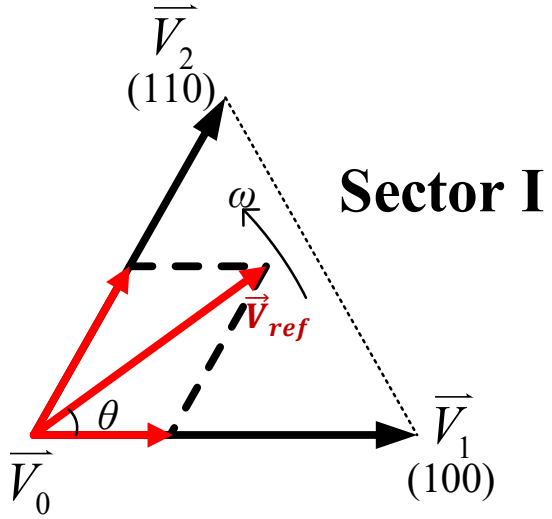


Figure 2.6: Vector synthesisation in Sector I.

Assuming that the sampling period T_s is sufficiently small, the reference vector $\overrightarrow{V_{ref}}$ can be considered constant during T_s. Under this assumption, $\overrightarrow{V_{ref}}$ can be approximated by two adjacent active vectors and one zero vector. For example, when $\overrightarrow{V_{ref}}$ falls into sector I as shown in Figure 2.6, it can be synthesized by $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, and $\overrightarrow{V_0}$. The volt-second balancing equation is

$$\overrightarrow{V_{ref}} = \overrightarrow{V_1}T_1 + \overrightarrow{V_2}T_2 + \overrightarrow{V_0}T_0 \tag{2.16}$$

$$T_s = T_1 + T_2 + T_0 \tag{2.17}$$

where T_1, T_2, and T_0 are the dwell times for the vectors $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, and $\overrightarrow{V_0}$, respectively.

Splitting the resultant equation into the real and imaginary components in the $\alpha\beta$-plane, we have

$$\begin{cases} V_{ref}T_s\cos\theta = \dfrac{2}{3}V_{dc}T_a + \dfrac{1}{3}V_{dc}T_b \\ V_{ref}T_s\sin\theta = \dfrac{1}{\sqrt{3}}V_{dc}T_b \end{cases} \tag{2.18}$$

Solving (2.18) together with $T_s = T_1 + T_2 + T_0$ gives

$$T_1 = \frac{\sqrt{3}T_sV_{ref}}{V_{dc}}\sin\left(\frac{\pi}{3} - \theta\right) \tag{2.19}$$

$$T_2 = \frac{\sqrt{3}T_sV_{ref}}{V_{dc}}\sin(\theta) \tag{2.20}$$

$$T_0 = T_s - T_1 - T_2 \tag{2.21}$$

With the space vectors selected and their dwell times calculated, the next step is to arrange the switching sequence. In general, the switching sequence design for a given $\overrightarrow{V_{ref}}$ is not unique, but the seven-segment switching sequence is the most used one which will be described here.

Figure 2.7 shows a typical and converter output voltage waveforms for $\overrightarrow{V_{ref}}$ in sector I, where $\overrightarrow{V_{ref}}$ is synthesized by vectors $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, and $\overrightarrow{V_0}$. The sampling period T_s is divided into seven segments for the selected vectors.

Table 2-2 gives the seven-segment switching sequences for $\overrightarrow{V_{ref}}$ residing in all six sectors. Note that all the switching sequences start and end with switching state (000), which indicates that the transition for $\overrightarrow{V_{ref}}$ moving from one sector to the next does not require any switching actions.

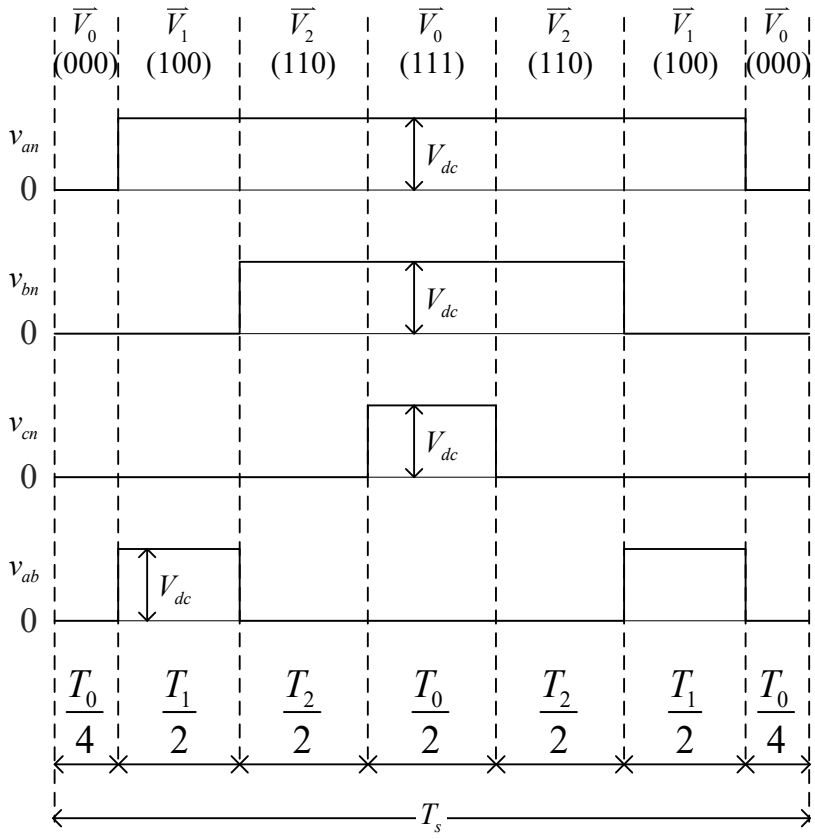


Figure 2.7: Seven-segment switching sequence in Sector I.

Table 2-2: Switching sequence of SVPWM

Sector	**Switching segments**						
	1	**2**	**3**	**4**	**5**	**6**	**7**
I	$\overrightarrow{V_0}$	$\overrightarrow{V_1}$	$\overrightarrow{V_2}$	$\overrightarrow{V_0}$	$\overrightarrow{V_2}$	$\overrightarrow{V_1}$	$\overrightarrow{V_0}$
II	$\overrightarrow{V_0}$	$\overrightarrow{V_3}$	$\overrightarrow{V_2}$	$\overrightarrow{V_0}$	$\overrightarrow{V_2}$	$\overrightarrow{V_3}$	$\overrightarrow{V_0}$
III	$\overrightarrow{V_0}$	$\overrightarrow{V_3}$	$\overrightarrow{V_4}$	$\overrightarrow{V_0}$	$\overrightarrow{V_4}$	$\overrightarrow{V_3}$	$\overrightarrow{V_0}$
IV	$\overrightarrow{V_0}$	$\overrightarrow{V_5}$	$\overrightarrow{V_4}$	$\overrightarrow{V_0}$	$\overrightarrow{V_4}$	$\overrightarrow{V_5}$	$\overrightarrow{V_0}$
V	$\overrightarrow{V_0}$	$\overrightarrow{V_5}$	$\overrightarrow{V_6}$	$\overrightarrow{V_0}$	$\overrightarrow{V_6}$	$\overrightarrow{V_5}$	$\overrightarrow{V_0}$
VI	$\overrightarrow{V_0}$	$\overrightarrow{V_1}$	$\overrightarrow{V_6}$	$\overrightarrow{V_0}$	$\overrightarrow{V_6}$	$\overrightarrow{V_1}$	$\overrightarrow{V_0}$

2.3 Energy Storage System (ESS)

The energy storage system (ESS) provides power for starting PMSG, and it also absorbs the excess power generated by the PMSG. During an emergency (loss of regular electrical power supply from the PMSG(s), the ESS can also provide power to the loads for a limited time through a bidirectional DC-DC converter [81]-[82]. The modelling of ESS will be discussed in this section.

2.3.1 Battery and the DC-DC converter

Figure 2.8 shows a typical ESS. In general, the battery bank module comprises battery cells connected in series and parallel to achieve the desired voltage and power level. As shown in Figure 2.8, a simple model of a constant voltage source V_{bat} in series with a resistor R_{bat} is used to represent the battery.

Bidirectional DC/DC converters are the key equipment in the DC distribution system to provide active interfaces between the DC networks and energy storage

elements [83][84]. Several publications have discussed the topology selection of the DC-DC converter in the MEA applications [86]-[89]. In this thesis, a buck-boost type bi-directional DC-DC converter is chosen here due to its simple structure with high reliability compared to other converters [114].

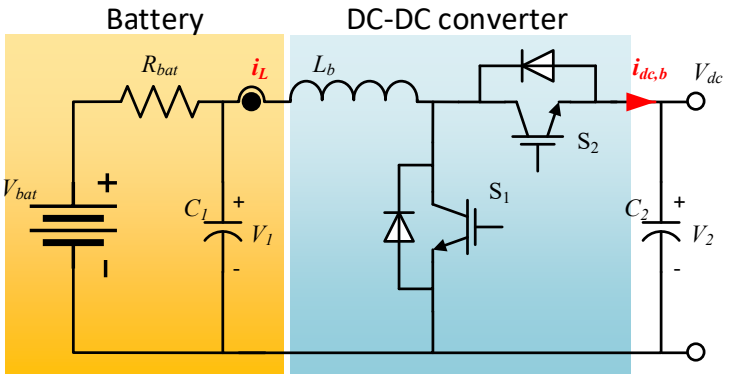


Figure 2.8: Energy storage system

The battery voltage is always determined by the state of charge (SOC) which is shown in Figure 2.9. There have been several computation methods for both SOC and battery voltage. The methods used vary and are dependent on the category of the battery [91]-[93]. However, this is not the topic of this thesis. Therefore, it will not be discussed in detail here.

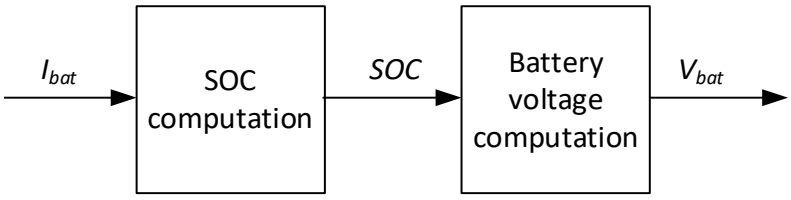


Figure 2.9: Battery model overview.

A Bidirectional DC-DC converter allows both charge and discharge modes of the battery bank by modifying the switching duty cycle of power electronics devices. An average model per switching period is considered here.

The topology of the bidirectional buck-boost converter has been shown in Figure 2.8. When the converter operates in boost mode (discharging mode), the magnitude of the converter's output current at the DC link i_{dc} is positive. In contrast, it is negative when it operates in buck mode (charging). It is assumed that the converter's inductor always operates in continuous conduction mode. Then, the model can be depicted as expressed in (2.22), (2.23) and (2.24).

$$\frac{dV_1}{dt} = \frac{-V_1 + V_{bat}}{C_1 R_{bat}} - \frac{i_L R_{bat}}{C_1} \tag{2.22}$$

$$\frac{dV_{dc}}{dt} = \frac{(1-d)i_L - i_{dc}}{C_2} \tag{2.23}$$

$$\frac{di_L}{dt} = \frac{-V_1 + (1-d)V_{dc}}{L_{bat}} \tag{2.24}$$

where V_{bat} and R_{bat} are the internal voltage and resistance of the battery bank, C_1 and C_2 are the capacitance at the battery bank side and DC link side, V_1 is the voltage on capacitor C_1, L_{bat} is the bi-directional buck-boost inductor and the current through it is i_L.

2.3.2 ESS Control

The controller for a bi-directional DC-DC converter is presented in Figure 2.10. Two PI controllers connected in cascade are used for obtaining duty cycle D for switches.

In practice, the DC-link voltage controller can be eliminated when voltage regulation is done by other sources.

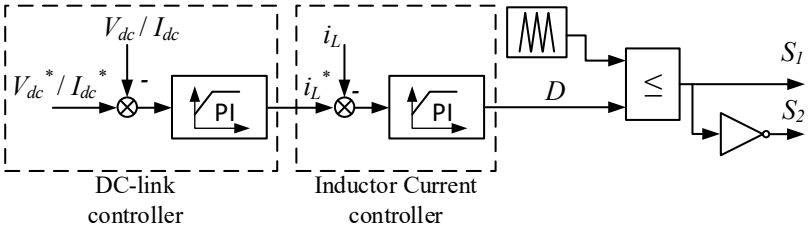


Figure 2.10: Controller of the DC-DC converter .

2.4 Power Sharing Control

After discussing the control of each local controller (LC) in the dual-channel generation system, it is important to manage the power sharing among the multiple sources, i.e., PMSGs and ESS. With power sharing control, system-level optimisation can be achieved such as efficiency improvement, power management etc.

Based on the usage of the communication technique, power sharing control can be divided into 3 categories: centralised control, distributed control, and decentralised control [28][94][95]. These methods will be illustrated, respectively.

2.4.1 Centralised control

As shown in Figure 2.11, centralised control can be implemented in distributed generation (DG) based DC grid by employing a centralised controller [98]. Data from DG are collected in a centralised aggregator, then processed and feedback commands are sent back to them via a digital communication network which is shown as dash lines.

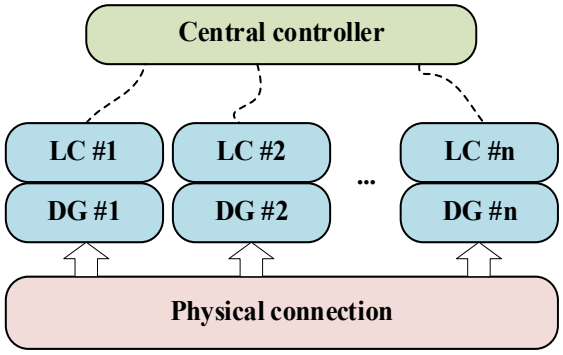


Figure 2.11: Operation principle of centralised control

It is easy to apply a centralised controller in a small scale grid system. Figure 2.12 shows a typical scheme of it. The centralised controller regulates the DC bus, the current references for each power module (PMSGs and ESS) are generated by splitting the total current reference according to the rated power

ratio of sources [28][96]. The algorithm of splitting current reference can be average splitting [28][96] or unequal splitting [97].

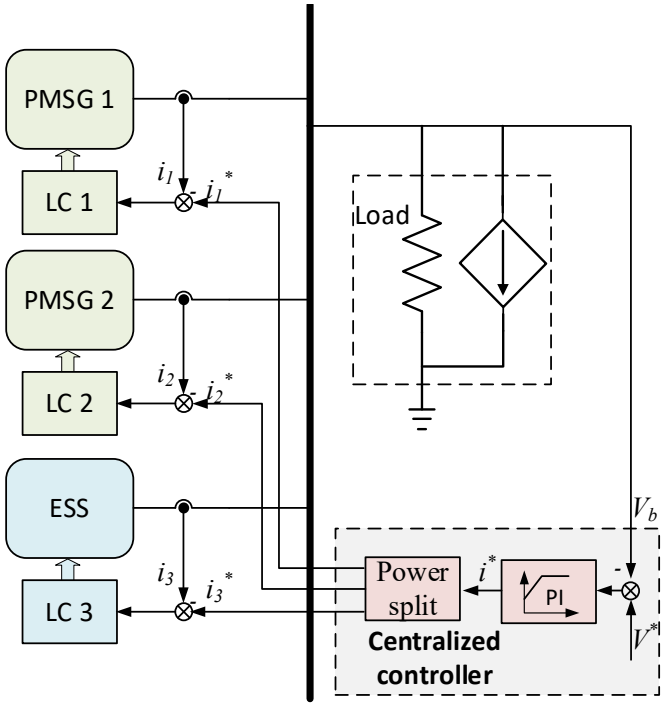


Figure 2.12: Control scheme of centralised control.

In some cases, master-slave control can be implemented as an alternative way of centralised control. It is realised by a module chosen as a "master" and the remaining modules as "slaves" [99][100]. Normally the module which has the largest capacity is the most reliable one, and it can be chosen as the "master". The master module regulates the DC-link voltage and generates the current references for the remaining "slave" modules. The typical block diagram of master-slave control is illustrated in Figure 2.13.

Compared to a centralised controller, master-slave control is more difficult to apply. However, it cuts the use of an extra centralised controller, which helps reduce the system cost.

Although centralised control has much better voltage regulation and current sharing performance, the requirement of communication restricts its application area so that it cannot be used in large-scale systems.

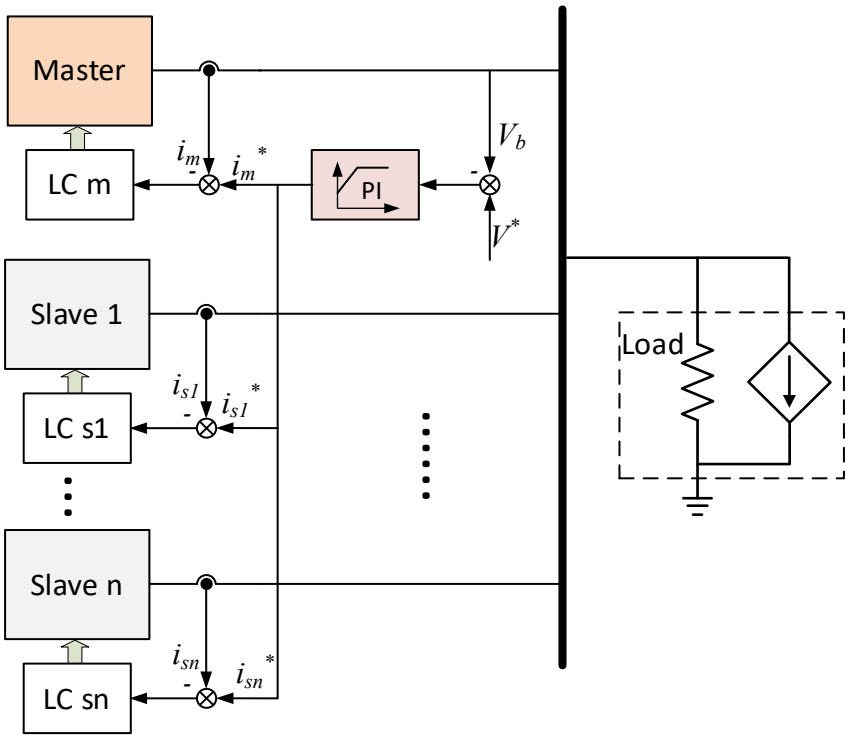


Figure 2.13: Control scheme of master-slave control.

2.4.2 Distributed control

As shown in Figure 2.14, there is no central control unit in a distributed control system. Communication lines only exist between the neighbouring modules [101]-[104].

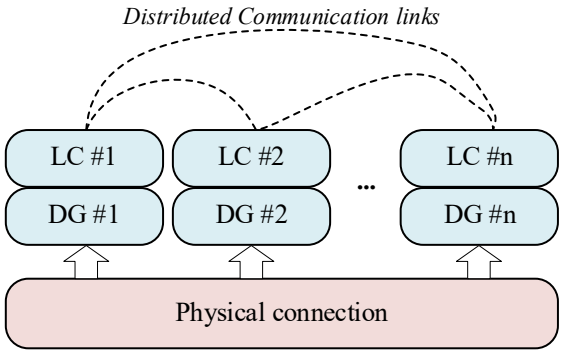


Figure 2.14: Operation principle of distributed control.

The main advantage of this approach is that the system can maintain full functionality, even if the failure of some communication links occurs. Therefore, distributed control is immune to a single point of failure [104].

However, different from the centralised control, the information directly exchanged between the local controllers can contain only locally available variables. In other words, if the two units are not connected directly by the communication link, they do not have direct access to each other's data and their observation of the whole system is limited.

2.4.3 Decentralised control (droop control)

Without external communication among the local controllers, decentralised control uses local measurement to implement local regulation, as shown in Figure 2.15. If the failure of one module occurs, the remaining modules can still contribute to power sharing according to their local droop settings. Thus, the system reliability is increased. Since communication links among the sources and an additional centralised controller are not needed, each parallel module can work independently relying on the local measurements and controllers [105].

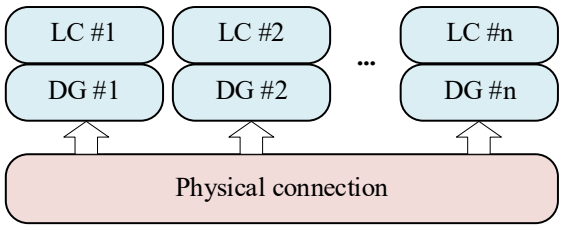
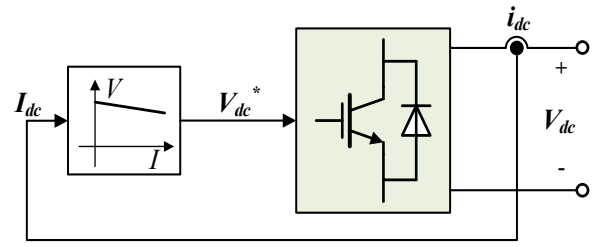


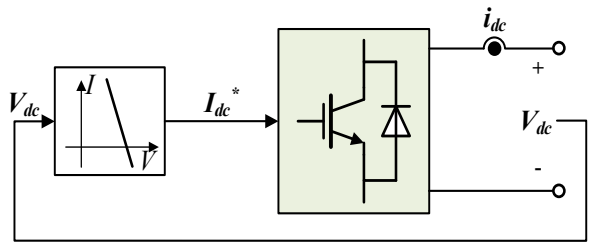
Figure 2.15: Operation principle of decentralised control.

Droop control was firstly employed for AC systems as decentralised control since communication lines are not required. Now, it has been widely accepted for DC systems similarly. It utilises a "virtual resistance" to achieve current sharing. In a DC system, a relationship between current and voltage is built to realise "virtual resistance" character.

Generally, droop control can be classified into voltage (including V-I strategy) and current mode (including I-V strategy) which are shown in Figure 2.16a and b respectively.



(a)



(b)

Figure 2.16: Droop characteristic. a) V-I droop. b) I-V droop.

i Voltage-mode approach

Voltage mode droop control uses measured branch current to generate voltage reference. The calculation of reference for the voltage controller is as follow

$$V_{dci}^* = V_o - k_{di} I_{dci} \tag{2.25}$$

Where *i* represents the index of each converter, V_{dci}^* is the calculated voltage reference for converter #*i*, V_o is the rated voltage, k_{di} is the droop coefficients in voltage-mode droop controllers of the converter #*i*, while I_{dci} is the output current of the converter #*i*.

Figure 2.17 shows the diagram of the V-I droop control curve when three converters are applied. Converters sharing the same DC bus voltage (V_{dci}).

Then, the power sharing between two converters can be seen from Figure 2.17 as

$$I_{dc1} : I_{dc2} : I_{dc3} = \frac{1}{k_{d1}} : \frac{1}{k_{d2}} : \frac{1}{k_{d3}} \tag{2.26}$$

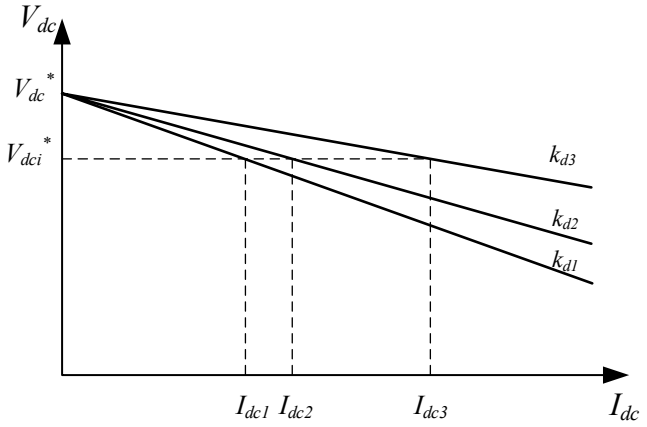


Figure 2.17: Power sharing characters of V-I droop control curve.

However, when considering the voltage drop on cables, the bus voltage in steady-state can be expressed as follows:

$$V_b = V_{dci} - I_{dci} R_i = V_{dc}^* - \left(k_{di} + R_i\right) I_{dci} \tag{2.27}$$

Where V_b is the voltage of common DC bus. R_i is cable resistance of converter #i. Then the current sharing among sources can be rewritten as

$$I_{dc1} : I_{dc2} : I_{dc3} = \frac{1}{k_{d1} + R_1} : \frac{1}{k_{d2} + R_2} : \frac{1}{k_{d3} + R_3} \tag{2.28}$$

It can be inferred that both droop gain and line resistance will influence the power sharing ratio, i.e., increasing the droop gain or line resistance will decrease the power output of the source.

ii Current-mode approach

For current-mode droop control, the output current reference is obtained by the local voltage measurement, which is

$$I_{dci}^{*} = \frac{V_o - V_{dci}}{k_{di}} \tag{2.29}$$

Figure 2.18 shows the current sharing concept when voltage drop on cable is ignored

$$I_{dc1} : I_{dc2} : I_{dc3} = \frac{1}{k_{d1}} : \frac{1}{k_{d2}} : \frac{1}{k_{d3}} \tag{2.30}$$

Where k_{di} is the droop gain for each local controller.

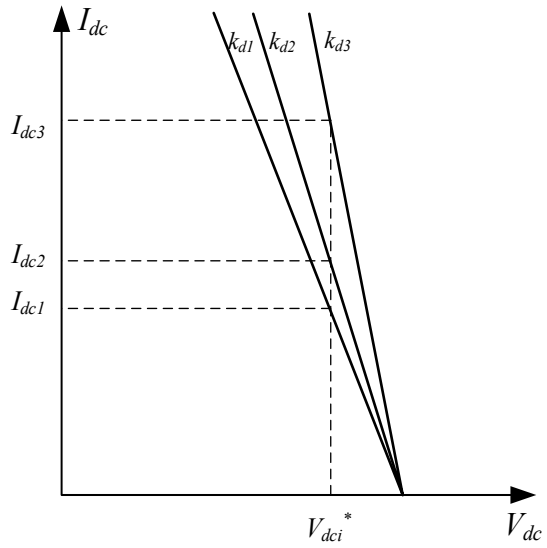


Figure 2.18: Power sharing characters of I-V droop control curve.

When voltage drop on cable considered, current sharing among 3 subsystems can be written as

$$I_{dc1} : I_{dc2} : I_{dc3} = \frac{1}{k_{d1} + R_1} : \frac{1}{k_{d2} + R_2} : \frac{1}{k_{d3} + R_3} \tag{2.31}$$

Based on the aforementioned analysis, in both current-mode and voltage-mode droop-controlled systems the ratio of the source powers is not as desired due to cable resistances.

Seen from (2.28) and (2.31), increasing droop coefficient (k_{d1}, k_{d2}, and k_{d3}) is the way to eliminate power sharing error. However, the voltage regulation performance is poor with it, i.e., the voltage drop is high under high droop gains.

2.5 Load Model

Generally, the load power in the electric aircraft DC grid is made up of a combination of constant impedance load and constant power load as expressed in (2.32).

$$P_L = P_{res} + P_{cpl} = \frac{v_{dc}^2}{R_{res}} + P_{cpl} \tag{2.32}$$

where P_{cpl} and P_{res} are the total power of the CPL and resistive load respectively, R_{res} is the resistance of the resistive load. Then, the voltage-current relationship can be written as in (14).

$$i_o = \frac{v_{dc}}{R_{\text{res}}} + \frac{P_{\text{cpl}}}{v_b} \tag{2.33}$$

In simulation studies, CPL can be represented with a controllable current source. The model diagram of the load combination is, as shown in Figure 2.19.

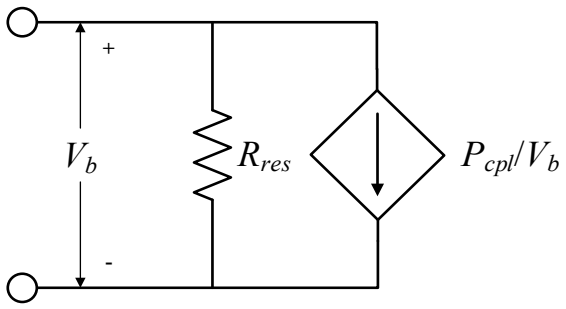


Figure 2.19: Load model

2.6 DC Link Model for Capacitor Bank

The work in this thesis aims to actively suppress harmonic on the DC-link capacitors. The dynamics on the DC-link can be expressed as in (2.34)

$$\frac{dV_{dc}}{dt} = \frac{i_{dc} - i_o}{C_b} \tag{2.34}$$

Here, i_{dc} is the current generated from sources, i_o is output current for loads, C_b is the capacitance of DC-link. If the impedance of the DC cable between the converter and the main DC bus is ignored, V_{dc} is equal to the main bus voltage (V_b). The nominal voltage of the main bus is always defined based on a certain standard. For instance, 270V is the nominal voltage and a range between 250V and 280V is acceptable for the more electric aircraft (MEA) as defined in MIL-STD-704F [41].

2.7 Chapter Summary

A detailed modal analysis of the dual-channel power generation system onboard aircraft has been performed in this chapter. The PMSG based generation system provides the electrical power from the engine shaft to the DC bus. ESS provides extra power when an emergency occurs. Resistive and constant power load are also introduced.

After modal analysis of each component, the control method is discussed. For each subsystem such as PMSG and ESS, the local controller is analysed firstly.

Then power sharing control is introduced to coordinate the dual-channel power generation system. Centralised control and distributed control show better performance because of proper coordination and leadership in small or medium-scale systems. To avoid failure due to communication, decentralised control can achieve high reliability, modularity and only depends on the local variables. However, the droop coefficient should be carefully chosen to balance the trade-off between voltage drop and power sharing accuracy.

Chapter 3

Harmonic Cancellation of Two AC/DC Converters Under Carrier-Based PWM Operations

3.1 Introduction

This chapter will investigate the harmonic suppression method based on the model and control of the dual-channel power system discussed in Chapter 2. In this chapter, the ESS is neglected, and an enhanced cancellation method will be proposed and implemented for the carrier harmonics suppression on the DC bus within the system as shown in Figure 3.1. Two electrical generators are feeding a common dc bus with their dedicated AC/DC converters. As the two generators are directly driven by high-speed shaft and low-speed shaft separately, the fundamental frequencies of these generators are different. In this study, only the steady-state operation is of interest, thus the transient issue associated with CPL can be ignored. A resistive load is connected to the DC bus.

A simplified mathematical model of the second carrier harmonics (components in the twice switching frequency) on DC-bus will be investigated and developed, which helps simplify the calculation procedure of the controller. With the simplified model, a new method to minimise the second carrier harmonic is proposed. With the proposed model and method, significant harmonic minimisation can be achieved under any fundamental frequency and power sharing ratio. Lastly, the proposed method has been validated by simulation.

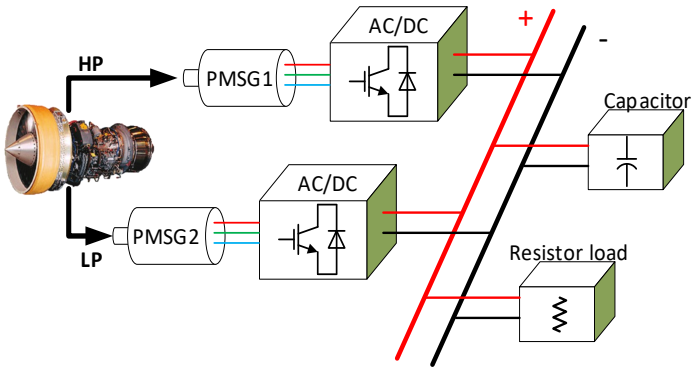


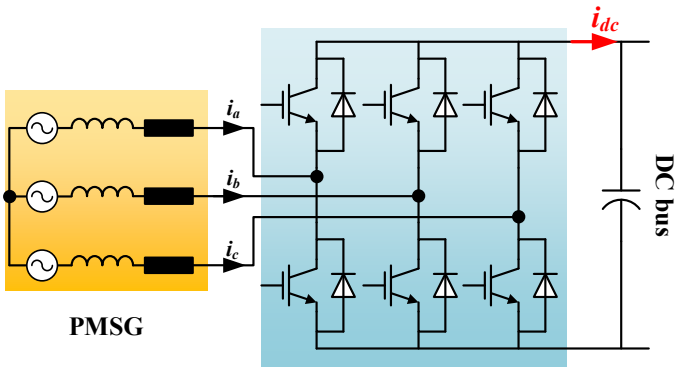
Figure 3.1: Dual-channel enhanced power generation system

3.2 Second Carrier Harmonics Analysis of Single Converter

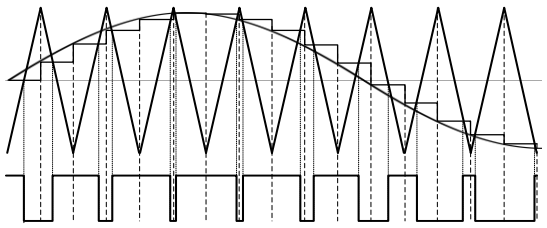
In order to develop a mechanism to suppress harmonics on the dc bus, thorough knowhow of two-level converters and an understanding of how the current harmonics are generated due to PWM method implemented on the power converters are essential. A two-level three-phase converter and asymmetrical regular sampling PWM are shown in Figure 3.2a and b, and the mathematical model of the switching harmonics on the DC-side currents will be based on them.

The two-level converter and asymmetrical regular sampling PWM method have been widely used in AC-DC conversion. Figure 3.2c shows the spectrum of i_{dc} (currents flowing into the capacitor from the converter side). As can be seen, significant components of $f_c \pm 3f_0$ (first band carrier harmonics) and $2f_c$ (second carrier harmonic) can be noticed in the i_{dc} spectrum. Here, f_c is the switching frequency, f_0 is the fundamental frequency from PMSG. For the studied dual-channel generation system, as generators are with different fundamental frequencies. The aim of this chapter is to suppress the harmonics on the DC link by adjusting the switching behaviour of two AC/DC converters. This means harmonics of $f_c \pm 3f_0$ are difficult to suppress because of fixed f_c together with variable f_0. Two components should have a same frequency, i.e.,

$f_c^{\{1\}}+3f_0^{\{1\}}=f_c^{\{2\}}+3f_0^{\{2\}}$. The index {1} and {2} here mean the symbol refers PMSG1 or PMSG2. The switching frequencies of the two converters should be adjusted in real-time according to the fundamental frequencies if $f_c \pm 3f_0$ harmonics are the targeted component.



(a)



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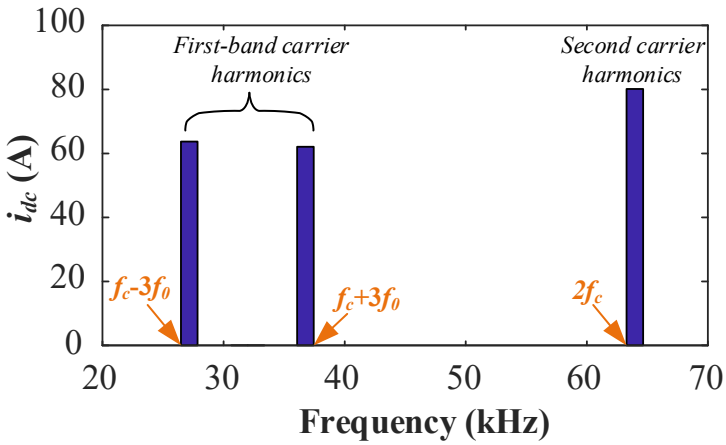


(c)

Figure 3.2: Two-level three-phase converter. a) PMSG and two-level converter, b) asymmetric regular sampling PWM, c) spectrum of i_{dc} (switching frequency f_c=32kHz, fundamental frequency f_0=1.5kHz).

However, comparing to the harmonics in $f_c \pm 3f_0$, harmonic in $2f_c$ has a better potential of suppression since it has no influence from f_0. Using double Fourier solution, analysis of this spectrum will be presented in the following sections.

3.2.1 Mathematical Analysis on DC-Bus Second Carrier Harmonic

Assuming the current on the AC side is ideally sinusoidal for a two-level converter, AC side currents can be written as

$$i_{ac}^{[k]}(t) = I_{ac}\cos\left(2\pi f_0 t + \beta + \frac{2k\pi}{3}\right) \tag{3.1}$$

where I_{ac} is the amplitude of the fundamental component of AC current, f_0 is the fundamental frequency, β is the angle between phase current and its AC side voltage, k=0, 1 and 2 represent phase A, B and C respectively.

Assuming the positive current on DC bus i_{dc} is from the converter to the dc-link capacitor as shown in Figure 3.2. Asymmetrical regular sampling PWM is analysed here because of better voltage output performance compared to symmetric sampling. The switching function of it for each phase leg can be expressed by

$$\begin{aligned} sf^{[k]}(t) &= K_{0,1}\cos\left(2\pi f_0 t + \beta + \alpha + \frac{2k\pi}{3}\right) \\ &+\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} K_{m,n}\cos\begin{bmatrix} m\left(2\pi f_c t + \theta_c^{[k]}\right) \\ +n\left(2\pi f_0 t + \beta + \alpha + \frac{2k\pi}{3}\right)\end{bmatrix} \end{aligned} \tag{3.2}$$

where f_c is the switching frequency, $\theta_c^{[k]}$ is phase angle of the triangular carrier signal for each leg, α is the phase angle between AC fundamental current and AC-side converter voltage (i.e. power factor angle), $K_{m,n}$ is the harmonic amplitude using the Bessel function of the first kind. Based on double Fourier analysis [106], $K_{m,n}$ can be expressed by

$$K_{m,n} = \frac{1}{q_{m,n}} J_n\left(q_{m,n}M\right)\sin\left[\left(m+n\right)\frac{\pi}{2}\right] \tag{3.3}$$

$$q_{m,n} = \left(m + n\frac{f_0}{f_c} \right)\frac{\pi}{2} \tag{3.4}$$

In (3.3) and (3.4), $J_n()$ is Bessel function of the first kind. m and n are orders of switching harmonic and its side bands respectively. For instance, when m=1 and n=3, $K_{m,n}$ means the magnitude of harmonic with a frequency of f_c+3f_0. Using (3.1) – (3.4), the DC-bus harmonic currents generated from one phase leg can be derived as

$$\begin{aligned} i_{dc}^{[k]}(t) &= i_{ac}^{[k]}(t)\, sf^{[k]}(t) \\ &= \frac{I_{ac}}{2}\left\{ \begin{aligned} &K_{0,1}\left[\cos\left(4\pi f_0 t + 2\beta + \alpha + \frac{4k\pi}{3} \right) + cos\alpha \right] \\ &+\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} K_{m,n} \left\{ \begin{aligned} &\cos\left[2\pi\left(mf_c + (n+1) f_0 \right) t + \sigma_{m,n}^{[k]} \right] \\ &+\cos\left[2\pi\left(mf_c + (n-1) f_0 \right) t + \varphi_{m,n}^{[k]} \right] \end{aligned} \right\} \end{aligned} \right\} \end{aligned} \tag{3.5}$$

Where $\sigma_{m,n}^{[k]}$ and $\varphi_{m,n}^{[k]}$ are phase angles of each component, which are

$$\sigma_{m,n}^{[k]} = m\theta_c^{[k]} + (n+1)\left(\beta + \frac{2k\pi}{3} \right) + n\alpha \tag{3.6}$$

$$\varphi_{m,n}^{[k]} = m\theta_c^{[k]} + (n-1)\left(\beta + \frac{2k\pi}{3} \right) + n\alpha \tag{3.7}$$

With (3.5), the current harmonics on DC-bus should be expressed as a sum of three legs' harmonics as

$$\begin{aligned} i_{dc,i,j}(t) &= \frac{I_{ac}}{2} K_{i,j-1} \sum_{k=0}^{2} \cos\left[2\pi\left(if_c + jf_0 \right) t + \sigma_{i,j-1}^{[k]} \right] \\ &+ \frac{I_{ac}}{2} K_{i,j+1} \sum_{k=0}^{2} \cos\left[2\pi\left(if_c + jf_0 \right) t + \varphi_{i,j+1}^{[k]} \right] \end{aligned} \tag{3.8}$$

Where i and j mean switching and band side orders of DC-bus current harmonics. For instance, i and j equal 1 and 3 when harmonic on f_c+3f_0 is analyzed. i and j are different from m and n, because m and n are orders for switching function.

Considering no phase shift on carrier signals among three legs, i.e. $\theta_c^{[1]} = \theta_c^{[2]} = \theta_c^{[3]}$, the phase angle of each component in (3.8) can be given as

$$\sigma_{i,j-1}^{[k]} = i\theta_c^{[k]} + j\left(\beta + \frac{2k\pi}{3}\right) + (j-1)\alpha \tag{3.9}$$

$$\varphi_{i,j+1}^{[k]} = i\theta_c^{[k]} + j\left(\beta + \frac{2k\pi}{3}\right) + (j+1)\alpha \tag{3.10}$$

From (3.8)–(3.10), it can be concluded that current components $i_{dc,i,j}(t)$ are zeros apart from cases with j=0, ±3, ±6, etc. This is due to fact that the three-phase currents are of 2π/3 phase shift and the characteristic of sinusoidal functions that

$$cos\theta + cos\left(\theta + \frac{2k\pi}{3}\right) + cos\left(\theta + \frac{4k\pi}{3}\right) = 0 \tag{3.11}$$

Expression in (3.8) can be divided into two components. The magnitudes of both components can be derived as

$$\frac{I_{ac}K_{i,j-1}}{2} = \frac{I_{ac}}{2q_{i,j-1}} J_{j-1}\left(q_{i,j-1}M\right)\sin\left[(i+j-1)\frac{\pi}{2}\right] \tag{3.12}$$

$$\frac{I_{ac}K_{i,j+1}}{2} = \frac{I_{ac}}{2q_{i,j+1}} J_{j+1}\left(q_{i,j+1}M\right)\sin\left[(i+j+1)\frac{\pi}{2}\right] \tag{3.13}$$

It can be seen from (3.12) and (3.13) that, when i+j are odd numbers (2k+1, k = 0, 1, 2, 3, ….), the magnitudes of these harmonics are zeros. Thus, only cases when i+j are even numbers need to be studied.

In summary, the DC-side current harmonics only appear when

$$j = 0, \pm 3, \pm 6 \ldots \tag{3.14}$$

$$i + j = \text{even number} \tag{3.15}$$

Hence, only components with frequency f_c±3f_0 (i=1, j=±3) and 2f_c (i=2, j=0) harmonics will appear at the dc-link side. The cases when i >2 and j>6 are generally not considered since the magnitudes are small and have little influence

on the DC-link capacitor ripples. This is in line with the diagram shown in Figure 3.2c.

In this chapter, suppression of harmonics with a frequency of $2f_c$ will be focused. From (3.8), substitute i=2 and j=0, the second order carrier harmonic current generated from three-phase converter (with three legs) can be derived as

$$i_{dc,2,0}(t) = \frac{3I_{ac}}{2}\begin{Bmatrix} K_{2,-1}cos\left[4\pi f_c t + 2\theta_c - \alpha\right] \\ +K_{2,1}cos\left[4\pi f_c t + 2\theta_c + \alpha\right] \end{Bmatrix} \tag{3.16}$$

3.2.2 Simplified Model on Second Carrier Harmonic

According to (3.16), two components with the same frequency but different magnitudes and phase angles can be derived as

$$\frac{3I_{ac}}{2}K_{2,-1}cos\left(4\pi f_c t + 2\theta_c - \alpha\right)$$

$$\text{and } \frac{3I_{ac}}{2}K_{2,1}cos\left(4\pi f_c t + 2\theta_c + \alpha\right) \tag{3.17}$$

The coefficient $K_{2,1}$ and $K_{2,-1}$ are written as

$$K_{2,1} = -\frac{2}{\left(2+\frac{f_0}{f_c}\right)\pi}J_1\left(\frac{\pi}{2}\left(2+\frac{f_0}{f_c}\right)M\right) \tag{3.18}$$

$$K_{2,-1} = -\frac{2}{\left(2-\frac{f_0}{f_c}\right)\pi}J_1\left(\frac{\pi}{2}\left(2-\frac{f_0}{f_c}\right)M\right) \tag{3.19}$$

Assuming that $f_c >> f_0$ (in normal cases, f_c is at least 20 times of f_0), the term f_0/f_c can be neglected as it is approximately equal to 0. Substituting f_0/f_c =0 to (3.18) and (3.19) gives

$$K_{2,1} \approx K_{2,-1} \approx -\frac{1}{\pi}J_1(\pi M) \tag{3.20}$$

Substituting (3.20) to (3.16) and using characteristic of sinusoidal functions

$$i_{dc,2,0}(t) \approx -\frac{3I_{ac}cos\alpha}{\pi} J_1(\pi M)\cos(4\pi f_c t + 2\theta_c) \tag{3.21}$$

From (3.21), it can be seen that power factor angle α will have no impact on the phase angle of $I_{dc,2,0}(t)$. This is very important and useful conclusion, since the power factor angle α is always determined by operating conditions of generators, including rotating speed, output power and dc-link voltage etc. Decoupling the power factor and the harmonic phase angle will significantly simplify the development of harmonic cancellation strategies.

For a given output converter power P, the AC-side terminal real power of the two-level converter can be formulated as

$$P = 3\frac{I_{ac}}{\sqrt{2}}\frac{V_{ac}}{\sqrt{2}}\cos\alpha = \frac{3I_{ac}MV_{dc}}{4}\cos\alpha \tag{3.22}$$

where V_{ac} is the magnitude of converter phase voltage, M is the modulation index of the converter. It can be derived from (3.22) that

$$I_{ac}\cos\alpha = \frac{4P}{3MV_{dc}} \tag{3.23}$$

combining (3.23) and (3.21) gives

$$\begin{aligned} i_{dc,2,0}(t) &\approx \frac{4PJ_1(\pi M)}{\pi MV_{dc}}\cos(4\pi f_c t + 2\theta_c) \\ &= \frac{4I_{dc}J_1(\pi M)}{\pi M}\cos(2\times 2\pi f_c t + 2\theta_c) \end{aligned} \tag{3.24}$$

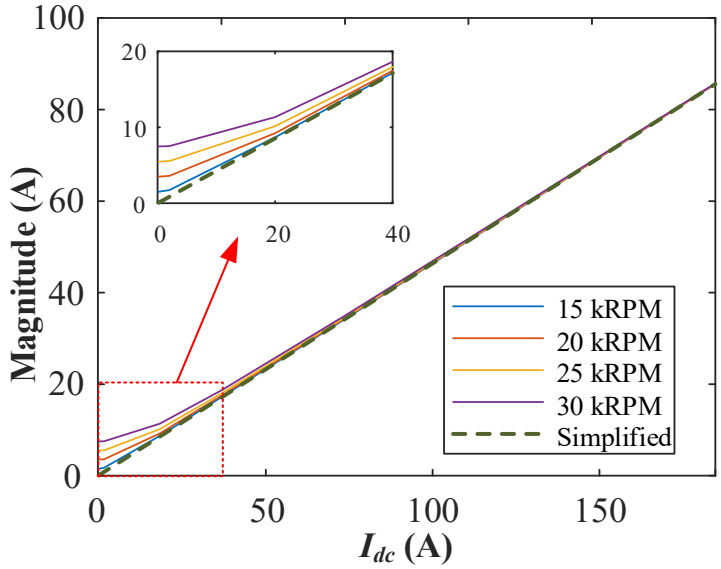
where I_{dc} is the DC component of the current i_{dc} on DC-bus. From (3.24), it is important to note that the magnitude of the second carrier harmonic current is only influenced by DC-side current (I_{dc}) and the modulation index (M) in the simplified model. Meanwhile, the phase angle of this component is determined by the angle of the carrier signal (θ_c) only. This means that the phase angle of second carrier harmonic on the DC-bus current can be controlled by carrier signal θ_c within the AC/DC converter.

3.2.3 Comparison Between the Simplified and Original Model

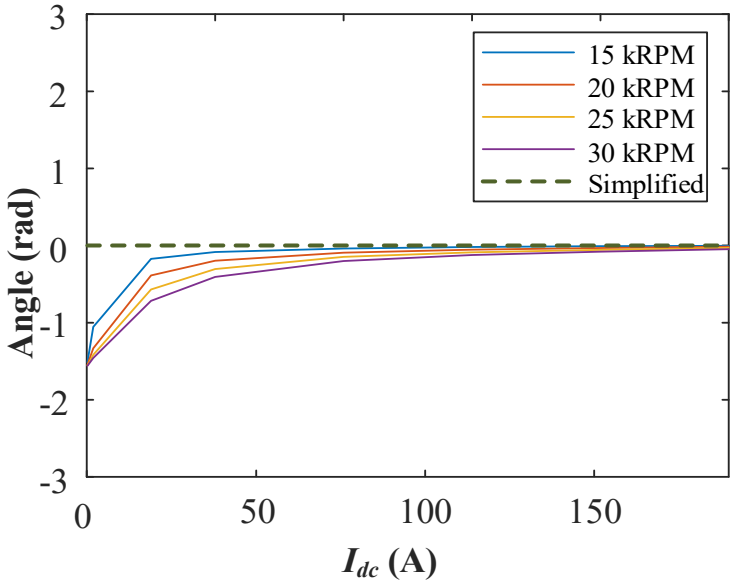
Table 3-1: Simulation Parameters

Category	Parameters	Values
PMSG parameters	Number of poles	6
	Resistance	1.058 mΩ
	Machine inductance	99 μH
	Flux linkage of permanent magnet	0.03644 Vs/rad
	DC link voltage reference	270 V
	Switching frequency	16 kHz
	Maximum modulation index	0.95
	Rated power	45kW
Simulation parameters	DC link capacitance	200 μF
	Load resistance	1.35 Ω
	Rotor speed	From 15 kRPM to 30 kRPM

The comparison between original (3.16) and simplified (3.24) model of DC-bus second carrier harmonics is given in Figure 3.3. The generator parameters are given in Table 3-1 using the AEGART machine [107]. The AEGART system is essentially composed of a permanent magnet generator and a two-level converter. Figure 3.3a compares the magnitude of $I_{dc,2,0}(t)$ between the simplified and original models and Figure 3.3b compares the angle phase difference between results from these two models. The modulation index is set as 0.95 during the calculation. This is reflecting the fact that the generator is always operated at high-speed and a flux-weakening is applied with high modulation index for the converter operations.



(a)



(b)

Figure 3.3: Comparison of second carrier harmonic component ($I_{dc,2,0}(t)$) from original and simplified models with increased generator power and speed. a) Magnitude. b) Phase angle.

In Figure 3.3a and b, a relatively bigger error can be noticed with an increase of the PMSM generator speed. This is due to the fact that the fundamental frequency is increased with fast rotating PMSMs and the assumption of f_0/f_c=0

in (3.19) will produce increased errors. However, accuracy of the simplified model is still acceptable, especially when the power is higher than 10kW (I_{dc} >37A with a 270Vdc).

In addition, when the power is below 10kW, it is obvious that magnitude is not significant. It is understood that the harmonic magnitude under this condition will not be significant due to the smaller current. With the power increase, the power factor α will move towards to zero. This is due to the fact that more active power has been generated by the electrical generator while the reactive power (used for de-fluxing) kept almost the same. From (3.16), two components on the right side of the equation are symmetric, this means improvement of the accuracy of the simplification.

From Figure 3.3a, magnitude is always less than 20A when the power is less than 10kW (I_{dc}<37A, power factor less than 0.21) compared to almost 80A when the power is 45kW (I_{dc}=166.6A, power factor at 0.83). In practice, we are more interested in high-power operation and this is the operation region where power quality issues should be more carefully addressed.

3.3 Proposed Cancellation Method

Using the developed simplified model, a second carrier harmonic cancellation method will be proposed and discussed in this section. In Figure 3.4, the dual-channel generation system is shown in more details. As can be seen, the dual-channel generation system is controlled by a centralised controller. As the permanent magnet generators are directly driven by engine shafts of high-speeds, it is assumed that both PMSG1 and PMSG2 are operated under flux weakening control because of wide rotor speed range.

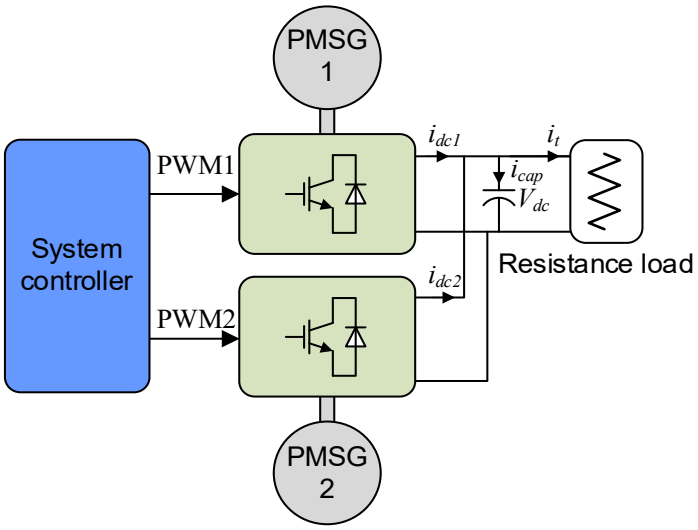


Figure 3.4: System diagram

3.3.1 Method for 1:1 Power Sharing Ratio

When generators supply equal power to the system, and two converters operate under the same modulation index, approximately the same magnitude of their second carrier harmonic components can be achieved using

$$\frac{4I_{dc1}J_1(\pi M)}{\pi M} = \frac{4I_{dc2}J_1(\pi M)}{\pi M} \tag{3.25}$$

where I_{dc1} and I_{dc2} are DC components of current i_{dc1} and i_{dc2}. Considering two sinusoidal currents flowing into one node and these two currents are of the same amplitude and frequency, it can be concluded that these harmonic currents will sum up to zero if they are of 180-degree phase shift. From (3.25), we can conclude that, to make the second carrier harmonics of DC-side currents from two power converters with the same magnitude, the average dc current and the modulation index should be the same for the two power converters, i.e., $I_{dc1}=I_{dc2}$ and $M_1=M_2$. In order to cancel the second carrier harmonics, the phase angle difference ($2\theta_c^{[1]} - 2\theta_c^{[2]}$) should be 180 degrees. This suggests that the phase difference between the two carrier signals ($\theta_c^{[1]} - \theta_c^{[2]}$) should be 90 degrees. Here, superscripts [1] and [2] are the indices of generators.

Based on this fact, a phase shifter with a fixed phase shift angle (90 degrees) is applied within the control system as shown in Figure 3.5. In Figure 3.5, a PI controller adjusts the total DC-link current reference (I_{ref}) to control the DC-link voltage (V_{dc}) as its reference (V_{ref}). Then, I_{ref} is feed to the two local controllers as the reference of each converter with a gain of 0.5. A 1:1 power sharing between the two converters can be achieved. Two AC-DC converters operate under a same modulation index (M). As discussed in the previous content, suppression of the second carrier harmonics can be achieved by a 90-degree phase shift between the two carrier signals, as shown in the orange block in Figure 3.5.

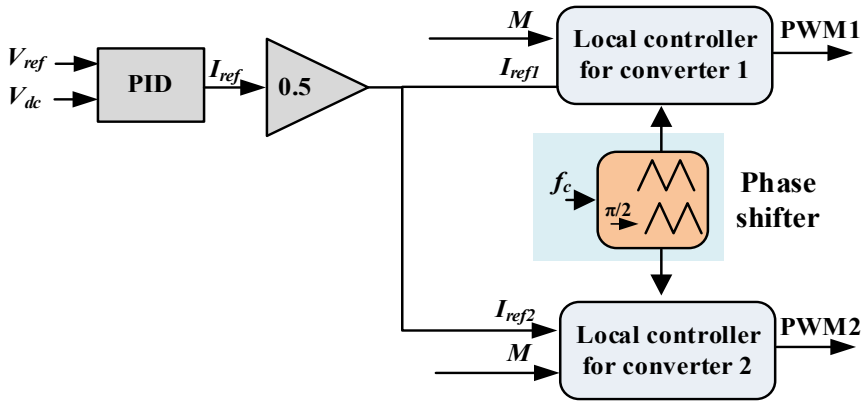


Figure 3.5: System controller when the power sharing ratio between the PMSG1 and the PMSG2 is 1:1.

3.3.2 Method for Unequal Power Sharing Ratios

For optimising fuel consumption and increase surge margin of an aircraft engine, it is very common that the two generation systems are not with the same power. In these cases, applying 90-degree phase shift only may not give expected results with fully eliminated the second carrier harmonics due to different amplitudes from the two AC/DC converters. To overcome this problem, an additional second carrier harmonic magnitude adaptor should be applied as shown in Figure 3.6.

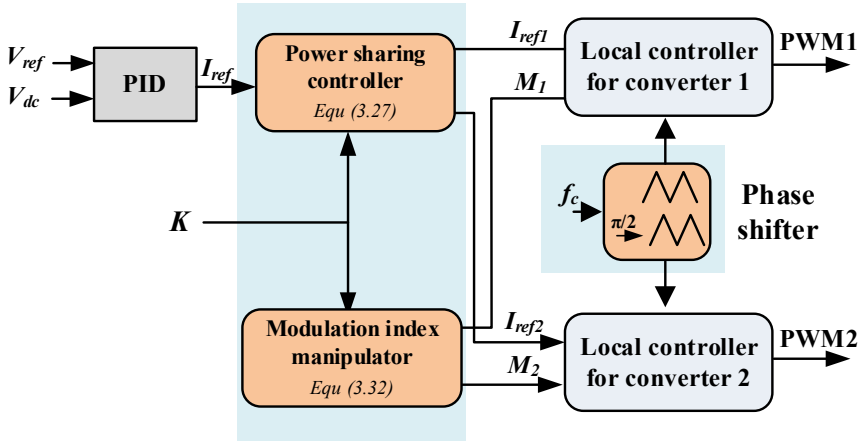


Figure 3.6: System controller when the power sharing ratio between the PMSG1 and the PMSG2 is unequal.

Define K as power sharing ratio between two sources which is

$$K = \frac{I_{ref1}}{I_{ref2}} \tag{3.26}$$

Hence, the current references, i_{ref1} and i_{ref2}, to the two converters can be expressed as

$$\begin{cases} I_{ref1} = I_{ref} \dfrac{K}{K+1} \\ I_{ref2} = I_{ref} \dfrac{1}{K+1} \end{cases} \tag{3.27}$$

The same magnitudes of second carrier harmonics should be achieved with

$$\frac{4I_{ref1}J_1(\pi M_1)}{\pi M_1} = \frac{4I_{ref2}J_1(\pi M_2)}{\pi M_2} \tag{3.28}$$

From (3.28), modulation index (M_1 and M_2) of each converter can be actively controlled to achieve same second carrier harmonic magnitude between two sources. From (3.24), it can be noted that the magnitude of the second carrier harmonic is proportional to the term $J_1(\pi M)/M$. The variation of $J_1(\pi M)/M$. versus M is given as Figure 3.7. It can be observed that smaller modulation index (M) will result in higher $J_1(\pi M)/M$, and thus a higher magnitude of the

second carrier harmonic. Assuming that PMSG1 is driven by the HP shaft and PMSG2 driven by the LP shaft, extracting higher power from LP shaft than HP shaft will help increase surge margin for engine [19], i.e., $I_{ref1}<I_{ref2}$. Hence, K is always less than 1, as derived from (3.26). With $K<1$, PMSG1 will produce less power than PMSG2.

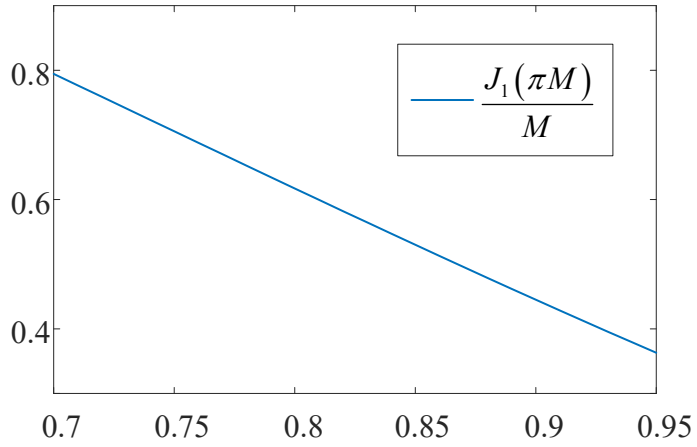


Figure 3.7: Term $J_1(\pi M)/M$ versus M.

As PMSGs operate under flux-weakening control range, the modulation index M is always a fixed value in conventional cases. However, to adjust the magnitudes of the two second carrier harmonics from PMSG1 and PMSG2 to be the same, this work considers M as a control variable in the controller. With the same modulation index between two PMSGs, the second order harmonic from PMSG1 system is lower than that from PMSG 2 because of its lower DC-bus current I_{dc1} (as PMSG1 produce less active power). Reducing modulation index for PMSG 1 system, however, its second order harmonic will be increased according to (3.24). Thus, reducing the modulation index in PMSG1 can compensate the impact of reduced power such that the second carrier harmonic reach the same magnitude of that from PSMG2. Using (3.24) and assuming $M_2=M_{max}$, the relationship between two magnitudes can be expressed as

$$\frac{4i_{ref1}J_1(\pi M_1)}{\pi M_1}=\frac{4i_{ref2}J_1(\pi M_{max})}{\pi M_{max}} \tag{3.29}$$

from (3.29) and (3.26), we have

$$\frac{J_1(\pi M_1)}{M_1} = \frac{J_1(\pi M_{max})}{KM_{max}} \tag{3.30}$$

Define a function

$$f(M) = \frac{J_1(\pi M)}{M} \tag{3.31}$$

The desired modulation index for the PSMG1 system M_1 can be derived as

$$M_1 = f^{-1}\left(\frac{J_1(\pi M_{max})}{KM_{max}}\right) \tag{3.32}$$

The inverse function is hard to calculate in real-time controller due to complicated Bessel function. Hence, a look-up table is applied in practical cases. Figure 3.9 shows the relationship between M and K when M_{max}=0.9 and 0.95 respectively. For a specific power sharing K, the modulation index M of PSGM1 associated converter can be derived using look-up table in Figure 3.9.

Local controller is shown in Figure 3.8. Control parameters set from Figure 3.6 (M, i_{ref}, carrier signal) are highlighted in red. For flux-weakening control under optimised modulation index, the outer voltage control loop provides a negative reference for d-axis current. Meanwhile, an adjustable saturation block is applied. It is to prevent AC side current over the limit i_{max}. This limits the effect of totally eliminating the second carrier harmonic, because the real modulation index cannot be reduced as required.

Using adapted modulation index and 90-degree phase shift on carrier signal, second carrier harmonics of DC-bus capacitor current can be suppressed in different power sharing ratio cases.

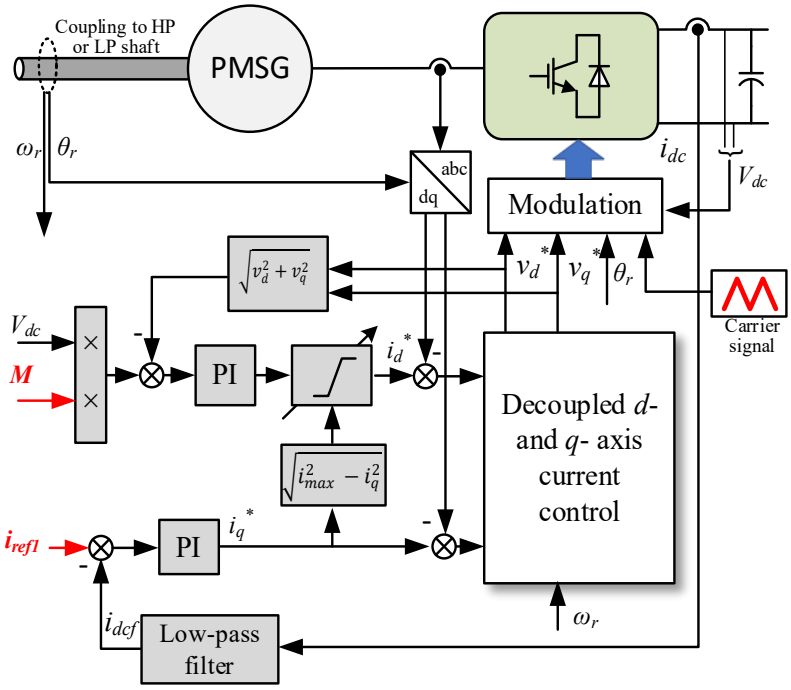


Figure 3.8: Local controller

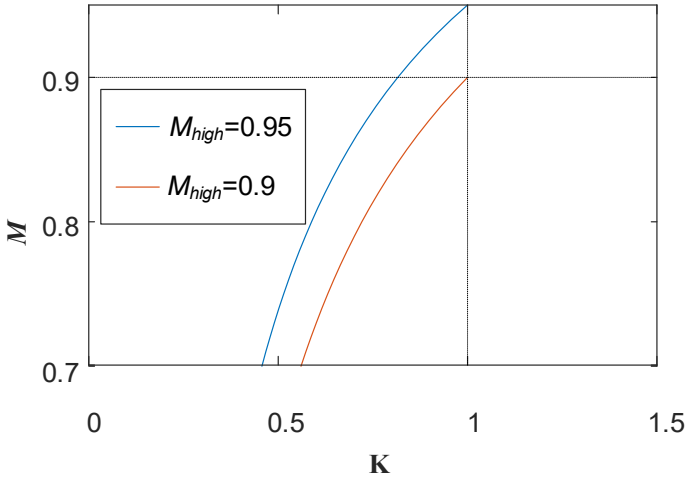


Figure 3.9: *M*-*K* diagram.

3.3.3 First-Band Harmonic

In previous sections, the modulation index of one converter within LP power generation channel is actively controlled, which helps further reduction of the second carrier harmonic. However, the first band harmonics ($f_c \pm 3f_0$) also play

important role in current spectrum. Hence, these two components are investigated in this section.

Firstly, harmonic on f_c+3f_0 is analyzed. Substitute i=1 and j=3 into (3.8) gives

$$\begin{aligned} i_{dc,1,3}(t) &= \frac{3I_{ac}}{2} K_{1,2} cos\left[2\pi\left(f_c + 3f_0\right)t + \sigma_{1,2}\right] \\ &+ \frac{3I_{ac}}{2} K_{1,4} cos\left[2\pi\left(f_c + 3f_0\right)t + \varphi_{1,4}\right] \end{aligned} \tag{3.33}$$

For the coefficient $K_{1,2}$ and $K_{1,4}$, we have

$$K_{1,2} = -\frac{2}{\left(1+2\frac{f_0}{f_c}\right)\pi} J_2\left(\frac{\pi}{2}\left(1+2\frac{f_0}{f_c}\right)M\right) \tag{3.34}$$

$$K_{1,4} = \frac{2}{\left(1+4\frac{f_0}{f_c}\right)\pi} J_4\left(\frac{\pi}{2}\left(1+4\frac{f_0}{f_c}\right)M\right) \tag{3.35}$$

Again, if we assume that $f_c >> f_0$, the term f_0/f_c can be neglected. The equation (3.32) can be approximated as

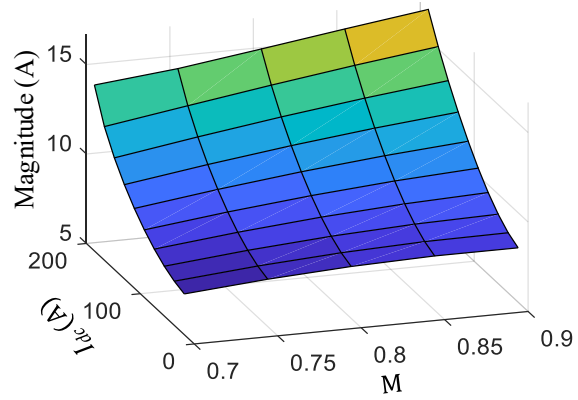
$$\begin{aligned} i_{dc,1,3}(t) &\approx -\frac{3I_{ac}}{\pi} J_2\left(\frac{\pi}{2}M\right)\cos\left[2\pi\left(f_c + 3f_0\right)t + \sigma_{1,2}\right] \\ &+ \frac{3I_{ac}}{\pi} J_4\left(\frac{\pi}{2}M\right) cos\left[2\pi\left(f_c + 3f_0\right)t + \varphi_{1,4}\right] \end{aligned} \tag{3.36}$$

Repeat the same process, the harmonic on f_c-3f_0 can be approximately expressed as

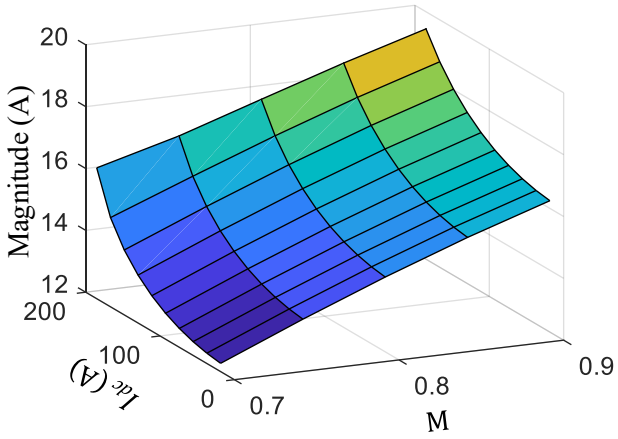
$$\begin{aligned} i_{dc,1,-3}(t) &\approx \frac{3I_{ac}}{\pi} J_4\left(\frac{\pi}{2}M\right)\cos\left[2\pi\left(f_c - 3f_0\right)t + \sigma_{1,-4}\right] \\ &- \frac{3I_{ac}}{\pi} J_2\left(\frac{\pi}{2}M\right) cos\left[2\pi\left(f_c - 3f_0\right)t + \varphi_{1,-2}\right] \end{aligned} \tag{3.37}$$

These formulas (3.36) and (3.37) are difficult to be further simplified. The results are determined by generator parameters and operation points. However,

the first-band harmonic components of DC-link current I_{dc} and the modulation index M can be identified using numeral analysis and are shown in Figure 3.10.



(a)



(b)

Figure 3.10: Magnitudes of first band harmonics related to the modulation and dc-link current. a) f_c-3f_0, b) f_c+3f_0.

Here, PMSM parameters are shown in Table I and the fundamental frequency is assumed f_0=1,200Hz. Systems with other fundamental frequencies can be analysed in a similar way. The change of the fundamental frequency will not have impacts to the conclusions and will not be detailed in this chapter. Analysis

on other PMSM parameters is another future study which will not be illustrated here.

As illustrated in Figure 3.9, modulation of PMSG 1 is less than M_{max} with $K<1$ (i.e. more electrical power is extracted from the LP shaft). From Figure 3.10, magnitudes of $f_c \pm 3f_0$ harmonics decrease if the modulation index decreases. Recalling that reducing modulation index of PMSG1 are used to make its second carrier harmonic component equivalent to that of PMSG2 system. It can be concluded that both first sideband ($f_c \pm 3f_0$) and second ($2f_c$) carrier harmonics can be reduced when adaptively reducing the modulation index of PMSG1. This will be further demonstrated using simulation test below.

3.4 Simulation Results

The simulation was implemented on MATLAB/Simulink and PLECS to evaluate the performance of proposed harmonic model and cancellation method. Some basic control parameters for a multi-source power system are shown in Table I.

Figure 3.11 shows how the proposed method works. With power sharing ratio decrease from 1:1 to 0.8:1, M_1 is adjusted based on (3.32). Moreover, currents before capacitor are controlled where filtered currents change to 89A and 110A respectively under 0.8:1.

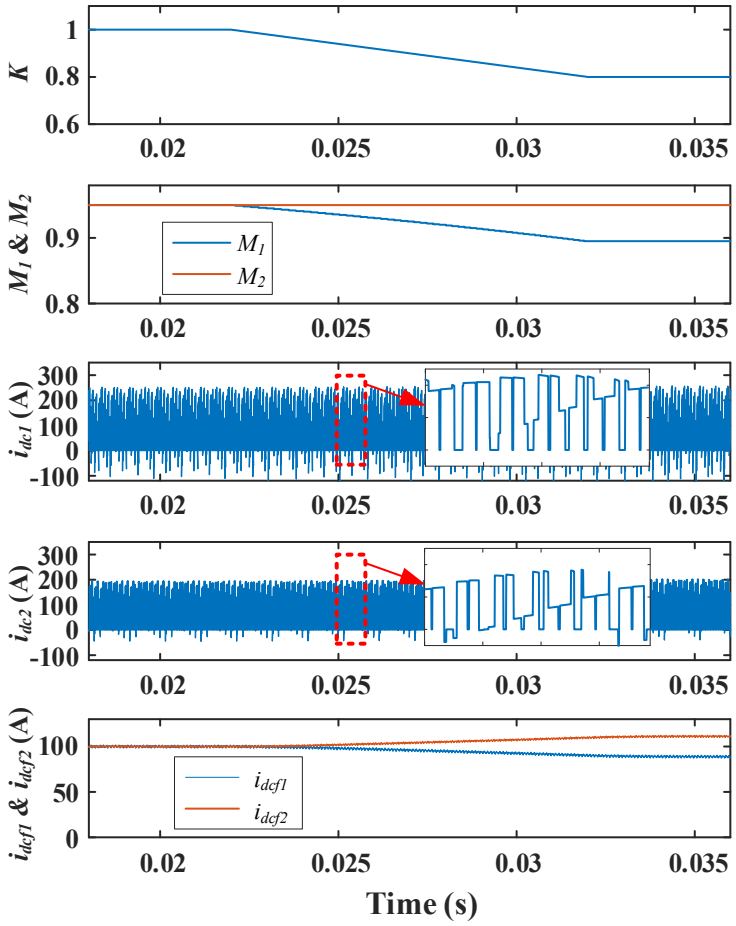
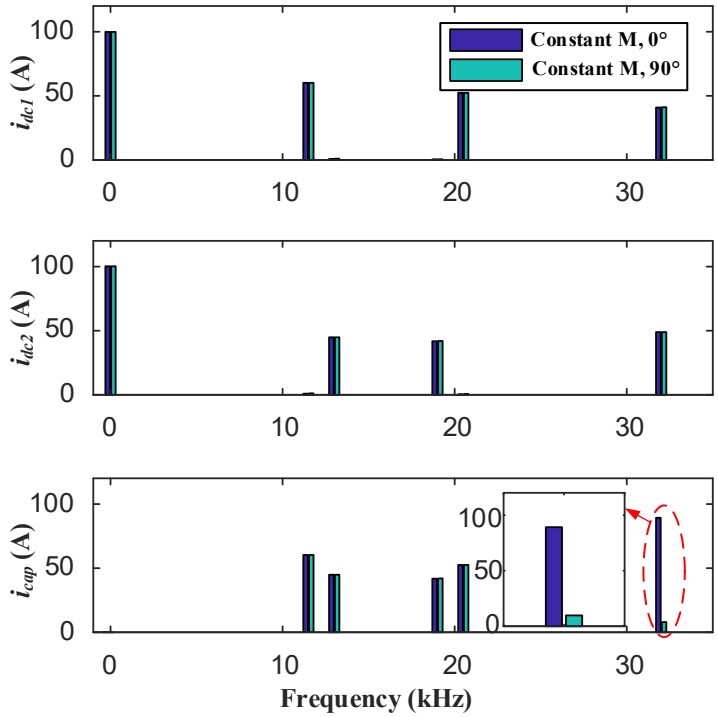
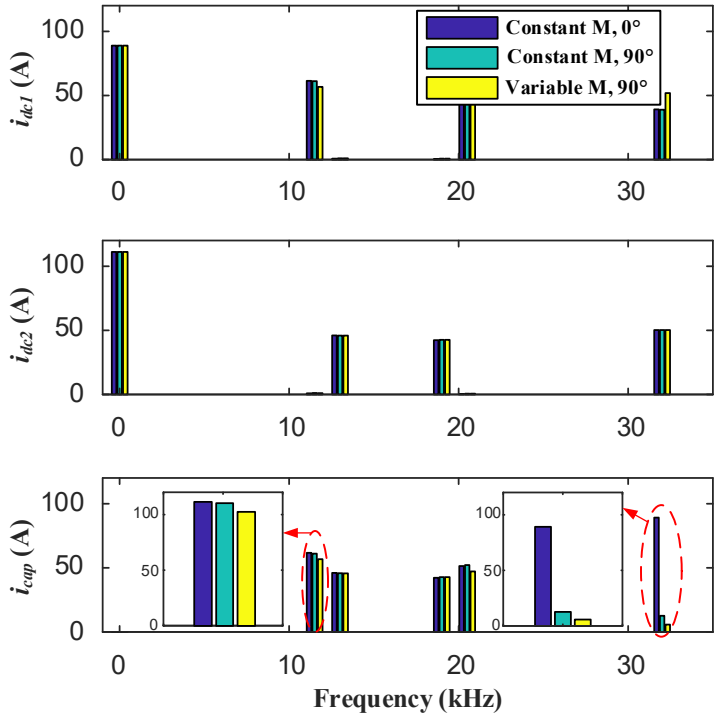


Figure 3.11: Simulation result of adjusting modulation index.

Figure 3.12a and b show the spectrums of currents on converter DC-link and capacitor when power sharing ratio is 1:1 and 0.8:1 respectively. Results under two operations are shown on both spectrums, which are a) constant modulation index (0.95) with no phase shift, b) constant modulation index with 90 degrees phase shift. Another operation of c) optimised modulation index with 90 degrees phase shift (here, M_1=0.895, M_2=0.95) is only shown on Figure 3.12b, because modulation index needs no variation when the power sharing ratio is 1:1. It can be seen that constant modulation index with 90 degrees phase shift has significantly suppressed the second carrier harmonic on the DC-bus capacitor. Moreover, with variable modulation index, the component is further suppressed



(a)



(b)

Figure 3.12: Current spectrums when power sharing ratio changes from 1:1 to 0.8:1. a) Current spectrum when K=1:1. b) Current spectrum when K=0.8:1.

when the power sharing ratio is 0.8:1, which validate the harmonic cancellation under the non-average power sharing ratio. Meanwhile, the first band harmonic in Figure 3.12b has also validated that reducing the modulation index will not increase the first band harmonic using the parameters of PMSG1 as shown in Table 3-1.

3.5 Chapter Summary

In this Chapter, a simplified mathematical model on second carrier current harmonic was investigated. The results show the magnitude of the component was only determined by the value of DC current and modulation index, while the phase angle of it is caused by the carrier phase angle. Based on a simplified model, a second carrier harmonic cancellation method was proposed. By actively controlling modulation index together with 90-degree phase shift on the carrier signal, a cancellation can be realized in a 2-source power system. The method can work under any machine speed and need no communication of harmonic phase angle among sources. The simplified model and cancellation method are basic research of harmonic cancellation. It gives potential approach of harmonic cancellation in not only dual-generator system, but also other multi-converter systems such as microgrid or back-to-back converter. Finally, simulation is implemented to verify the validity of the proposed second carrier harmonic model and cancellation method.

Chapter 4

Harmonic Cancellation of Two AC/DC Converters Under Space Vector PWM Operations

4.1 Introduction

As an extension of the work presented in Chapter 3, this chapter will develop a harmonic cancellation method for the dual-generator system using the SVPWM technique. When compared with SPWM, SVPWM gives higher modulation index limitation, but the harmonic distribution of DC-side current is more complicated. For instance, there is one harmonic component on the first switching frequency when using SVPWM. However, no harmonic exists on this frequency under SPWM operation.

The cancellation scheme proposed in this chapter will be based on detailed mathematic analysis of relation between harmonics and SVPWM modulation. Readers should be reminded that although it requires extensive maths, the developed cancellation scheme can be implemented in a convenient way.

4.2 Mathematical Model of DC-Bus Current Harmonics of Two-Level Converters under SVPWM Operation

In order to develop a scheme to suppress dc voltage/current harmonics within a multi-converter-fed DC grid, it is essential to have detailed information of these

harmonics either through measurement or proper mathematic modelling. In this chapter, we assume that the power converters are standard two-level converter as shown in Figure 4.1a. Although measurement of harmonics can be implemented using band-pass filters, these filters are difficult to extract the required switching frequency harmonics due to the existence of side-band harmonics as shown in Figure 4.2. In this section, relations of DC-link harmonics and SVPWM modulation will be identified, and a mathematical model will be developed.

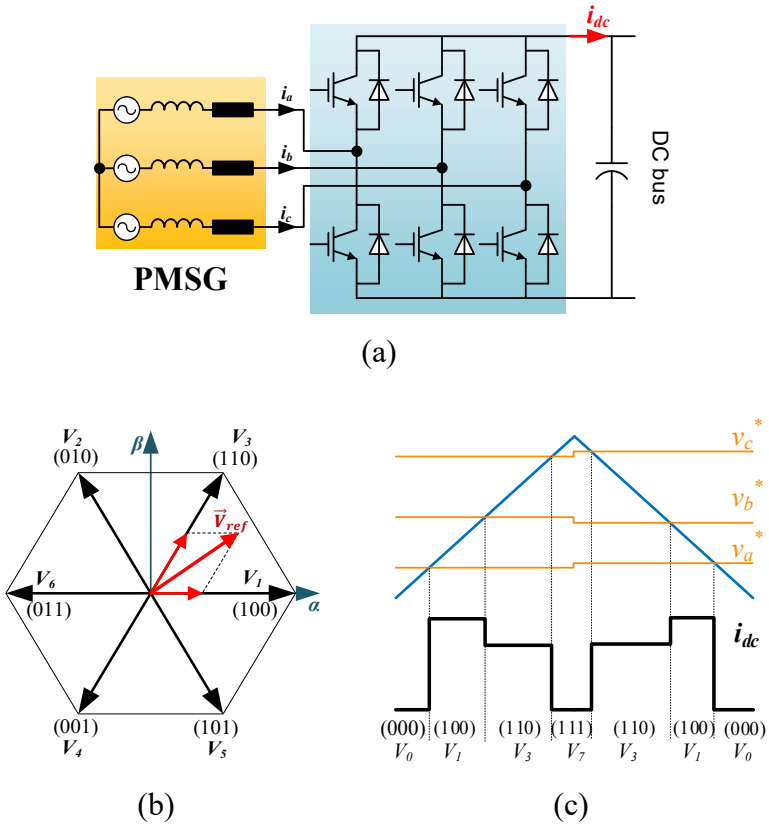


Figure 4.1: Two-level three-phase converter and SVPWM operation. a) Topology, b) Switching vectors and voltage reference, c) Modulation waveform.

Figure 4.1b shows an example of SVPWM operation when a reference voltage (V_{ref}) locates between two adjacent voltage vectors V_1 and V_3. There, V_1, V_3 and two zero vectors V_0, V_7 are used to synthesize the reference V_{ref}. Figure 4.1c illustrates how the reference voltage is transformed into on/off signals for each of the three inverter legs by comparing with a triangular carrier wave. If the

triangular carrier waveform is above the phase voltage reference v_x^* (x=a,b,c), the corresponding leg will be with '1' state, i.e. the upper switch within this leg is "on". Otherwise, the corresponding leg will be with '0' state, i.e., the upper switch within this leg is "off".

Figure 4.2 shows the spectrum of i_{dc} which is the current flowing into the dc-link capacitor from the converter side. f_c is the switching frequency. A few of side band components, $f_c \pm 3f_0$ for instance, can be identified. Here, f_0 is the fundamental frequency of the AC side voltage. Within the dual-channel power generation system, the fundamental frequencies f_0 are normally of different values as generators are driven by different shafts running at different speeds. Considering the fact that a harmonics suppression scheme is essentially to use harmonics from one AC-DC converter to compensate the other, the targeted harmonics should be of the same frequency in two different generation channels. The difference of f_0 makes suppression of the side-band harmonics a very challenging task in that sense as two generators are driven by two different shafts thus with different fundamental frequency f_0. For that reason, this chapter will focus on suppressing components on f_c and $2f_c$ specifically.

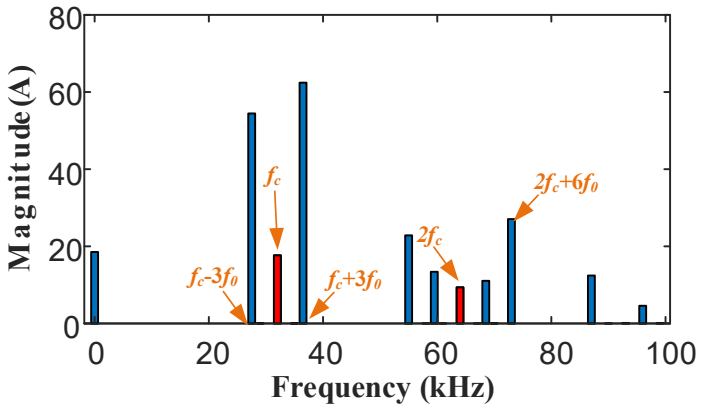


Figure 4.2: i_{dc} spectrum.

Neglecting the switching-frequency harmonics, AC currents for a two-level converter can be written as

$$i_{ac}^{[k]}(t) = I_{ac} cos\left(2\pi f_0 t + \beta + \frac{2k\pi}{3}\right) \tag{4.1}$$

where I_{ac} is the amplitude of AC currents, f_0 is the fundamental frequency, β is the phase angle (with reference to the electrical generator back-EMF in this thesis), k=0, 1 and 2 is to represent phase A, B and C respectively. Assuming the positive direction of current i_{dc} is from the converter to the dc-link capacitor as shown in Figure 4.1a, the switching function for each phase leg can be expressed with Double Fourier expansion [106] as

$$\begin{aligned} sf^{[k]}(t) &= K_{0,1}cos\left(2\pi f_0 t+\beta+\alpha+\frac{2k\pi}{3}\right) \\ &+\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}K_{m,n}cos\left[\begin{matrix} m\left(2\pi f_c t+\theta_c^{[k]}\right) \\ +n\left(2\pi f_0 t+\beta+\alpha+\frac{2k\pi}{3}\right)\end{matrix}\right] \end{aligned} \tag{4.2}$$

where f_c is the switching frequency, $\theta_c^{[k]}$ is phase angle of the triangular carrier signal for each leg, α is the phase angle between fundamental AC currents and voltages (i.e. power factor angle), $K_{m,n}$ is the harmonic amplitude using the Bessel function of the first kind. As discussed in [106], for asymmetrical regular sampling SVPWM, the switching function for a single-phase leg can be expressed by

$$K_{m,n}=\frac{4}{m\pi^2}\left[\begin{matrix} \frac{\pi}{6}\sin\left[\left(q_{m,n}+n\right)\frac{\pi}{2}\right]\left\{J_n\left(\frac{3\pi}{4}q_{m,n}M\right)+2\cos\left(\frac{n\pi}{6}\right)J_n\left(\frac{\sqrt{3}\pi}{4}q_{m,n}M\right)\right\} \\ +\frac{1}{n}\sin\left(\frac{q_{m,n}\pi}{2}\right)\cos\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\pi}{6}\right)\left\{J_0\left(\frac{3\pi}{4}q_{m,n}M\right)-J_0\left(\frac{\sqrt{3}\pi}{4}q_{m,n}M\right)\right\}\Bigg|_{n\neq 0} \\ +\sum_{\substack{k=1\\(k\neq -n)}}^{\infty}\left[\begin{matrix}\frac{1}{n+k}\sin\left[\left(q_{m,n}+k\right)\frac{\pi}{2}\right]\cos\left[\left(n+k\right)\frac{\pi}{2}\right]\sin\left[\left(n+k\right)\frac{\pi}{6}\right] \\ \times\left\{J_k\left(\frac{3\pi}{4}q_{m,n}M\right)+2\cos\left(\left(2n+3k\right)\frac{\pi}{6}\right)J_k\left(\frac{\sqrt{3}\pi}{4}q_{m,n}M\right)\right\}\end{matrix}\right] \\ +\sum_{\substack{k=1\\(k\neq n)}}^{\infty}\left[\begin{matrix}\frac{1}{n-k}\sin\left[\left(q_{m,n}+k\right)\frac{\pi}{2}\right]\cos\left[\left(n-k\right)\frac{\pi}{2}\right]\sin\left[\left(n-k\right)\frac{\pi}{6}\right] \\ \times\left\{J_k\left(\frac{3\pi}{4}q_{m,n}M\right)+2\cos\left(\left(2n-3k\right)\frac{\pi}{6}\right)J_k\left(\frac{\sqrt{3}\pi}{4}q_{m,n}M\right)\right\}\end{matrix}\right] \end{matrix}\right] \tag{4.3}$$

where

$$q_{m,n} = m + n\frac{f_0}{f_c} \tag{4.4}$$

In (4.3) and (4.4), m and n are the order of main and sideband harmonic for a single phase leg respectively. For instance, when m=1 and n=3, $K_{m,n}$ means the magnitude of harmonic component of frequency f_c+3f_0. Using (4.1)–(4.4), the DC-bus currents generated from one phase leg can be derived as

$$\begin{aligned} i_{dc}^{[k]}(t) &= i_{ac}^{[k]}(t)\, sf^{[k]}(t) \\ &= \frac{I_{ac}}{2}\left\{ \begin{aligned} &K_{0,1}\left[\cos\left(4\pi f_0 t + 2\beta + \alpha + \frac{4k\pi}{3}\right) + \cos\alpha\right] \\ &+\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} K_{m,n}\left\{ \begin{aligned} &\cos\left[2\pi\left(mf_c + (n+1)f_0\right)t + \sigma_{m,n}^{[k]}\right] \\ &+\cos\left[2\pi\left(mf_c + (n-1)f_0\right)t + \varphi_{m,n}^{[k]}\right] \end{aligned}\right\} \end{aligned}\right\} \end{aligned} \tag{4.5}$$

where $\sigma_{m,n}^{[k]}$and $\varphi_{m,n}^{[k]}$ (k=0,1,2) are given as

$$\sigma_{m,n}^{[k]} = m\theta_c^{[k]} + (n+1)\left(\beta + \frac{2k\pi}{3}\right) + n\alpha \tag{4.6}$$

$$\varphi_{m,n}^{[k]} = m\theta_c^{[k]} + (n-1)\left(\beta + \frac{2k\pi}{3}\right) + n\alpha \tag{4.7}$$

Thus, the DC-link current (i_{dc}) is essentially to add the contribution from the three-phase legs with (4.5). Components of i_{dc} at the frequency of if_c+jf_0 can be expressed as

$$\begin{aligned} i_{dc,i,j}(t) &= \frac{I_{ac}}{2} K_{i,j-1}\sum_{k=0}^{2} cos\left[2\pi\left(if_c + jf_0\right)t + \sigma_{i,j-1}^{[k]}\right] \\ &+ \frac{I_{ac}}{2} K_{i,j+1}\sum_{k=0}^{2} cos\left[2\pi\left(if_c + jf_0\right)t + \varphi_{i,j+1}^{[k]}\right] \end{aligned} \tag{4.8}$$

where i and j mean orders of main and sideband harmonic of DC-side currents of the converter respectively. The equation (4.8) gives a detailed knowledge of each harmonics. For example, substituting i=1 and j=3 into (4.8), harmonic on f_c+3f_0 can be expressed. Equation (4.6)–(4.8) will be the basis for our harmonic cancellation scheme development.

4.3 Mathematical Analysis of The First and Second carrier Harmonics

As discussed in Section 4.2, harmonics on the first and second carrier frequencies (f_c and $2f_c$) have potential of cancellation. In this section, some simplified models to calculate these two harmonic components are introduced.

4.3.1 Harmonic component of f_c

Using (4.6)–(4.8), the first switching frequency harmonic f_c with SVPWM modulation can be given with i=1, j=0 as

$$\begin{aligned} i_{dc,1,0}(t) &= \frac{I_{ac}}{2} K_{1,-1} \sum_{k=0}^{2} cos\left[2\pi(f_c)t + \theta_c^{[k]} - \alpha\right] \\ &+ \frac{I_{ac}}{2} K_{1,1} \sum_{k=0}^{2} cos\left[2\pi(f_c)t + \theta_c^{[k]} + \alpha\right] \end{aligned} \tag{4.9}$$

Considering no phase shift of carrier signals among three phase legs, i.e. $\theta_c^{[1]} = \theta_c^{[2]} = \theta_c^{[3]} = \theta_c$, the equation (4.9) can be rewritten as

$$\begin{aligned} i_{dc,1,0}(t) &= \frac{3I_{ac}}{2} K_{1,-1} cos\left[2\pi(f_c)t + \theta_c - \alpha\right] \\ &+ \frac{3I_{ac}}{2} K_{1,1} cos\left[2\pi(f_c)t + \theta_c + \alpha\right] \end{aligned} \tag{4.10}$$

where the coefficients $K_{1,-1}$ and $K_{1,1}$ can be obtained according to (4.3) which are

$$K_{1,-1}=\frac{4}{\pi^2}\left[\begin{array}{l}\frac{\pi}{6}\sin\left[\left(q_{1,-1}-1\right)\frac{\pi}{2}\right]\left\{J_{-1}\left(\frac{3\pi}{4}q_{1,-1}M\right)+2\cos\left(\frac{\pi}{6}\right)J_{-1}\left(\frac{\sqrt{3}\pi}{4}q_{1,-1}M\right)\right\}\\ +\sum_{k=3,5,7\ldots}^{\infty}\left[\begin{array}{l}\frac{1}{k-1}\sin\left[\left(q_{1,-1}+k\right)\frac{\pi}{2}\right]\cos\left[\left(k-1\right)\frac{\pi}{2}\right]\sin\left[\left(k-1\right)\frac{\pi}{6}\right]\\ \times\left\{J_k\left(\frac{3\pi}{4}q_{1,-1}M\right)+2\cos\left(\left(3k-2\right)\frac{\pi}{6}\right)J_k\left(\frac{\sqrt{3}\pi}{4}q_{1,-1}M\right)\right\}\end{array}\right]\\ +\sum_{k=1,3,5\ldots}^{\infty}\left[\begin{array}{l}\frac{1}{-1-k}\sin\left[\left(q_{1,-1}+k\right)\frac{\pi}{2}\right]\cos\left[\left(k+1\right)\frac{\pi}{2}\right]\sin\left[\left(-1-k\right)\frac{\pi}{6}\right]\\ \times\left\{J_k\left(\frac{3\pi}{4}q_{1,-1}M\right)+2\cos\left(\left(2+3k\right)\frac{\pi}{6}\right)J_k\left(\frac{\sqrt{3}\pi}{4}q_{1,-1}M\right)\right\}\end{array}\right]\end{array}\right] \tag{4.11}$$

$$K_{1,1}=\frac{4}{\pi^2}\left[\begin{array}{l}\frac{\pi}{6}\sin\left[\left(q_{1,1}+1\right)\frac{\pi}{2}\right]\left\{J_1\left(\frac{3\pi}{4}q_{1,1}M\right)+2\cos\left(\frac{\pi}{6}\right)J_1\left(\frac{\sqrt{3}\pi}{4}q_{1,1}M\right)\right\}\\ +\sum_{k=1,3,5\ldots}^{\infty}\left[\begin{array}{l}\frac{1}{k+1}\sin\left[\left(q_{1,1}+k\right)\frac{\pi}{2}\right]\cos\left[\left(k+1\right)\frac{\pi}{2}\right]\sin\left[\left(k+1\right)\frac{\pi}{6}\right]\\ \times\left\{J_k\left(\frac{3\pi}{4}q_{1,1}M\right)+2\cos\left(\left(2+3k\right)\frac{\pi}{6}\right)J_k\left(\frac{\sqrt{3}\pi}{4}q_{1,1}M\right)\right\}\end{array}\right]\\ +\sum_{k=3,5,7\ldots}^{\infty}\left[\begin{array}{l}\frac{1}{1-k}\sin\left[\left(q_{1,1}+k\right)\frac{\pi}{2}\right]\cos\left[\left(1-k\right)\frac{\pi}{2}\right]\sin\left[\left(1-k\right)\frac{\pi}{6}\right]\\ \times\left\{J_k\left(\frac{3\pi}{4}q_{1,1}M\right)+2\cos\left(\left(2-3k\right)\frac{\pi}{6}\right)J_k\left(\frac{\sqrt{3}\pi}{4}q_{1,1}M\right)\right\}\end{array}\right]\end{array}\right] \tag{4.12}$$

Considering $q_{1,n}=1+\eta f_0/f_c$, the sine function terms in (4.11) and (4.12) can be written as

$$\sin\left[\left(q_{1,n}+k\right)\frac{\pi}{2}\right]=\sin\left[\left(1+k\right)\frac{\pi}{2}+n\frac{f_0}{f_c}\times\frac{\pi}{2}\right] \tag{4.13}$$

Considering the fact that the fundamental frequency is far less than switching frequency, i.e. $f_c \gg f_0$, the equation (4.13) can be approximately expressed using Taylor series with only first order.

$$\sin\left[\left(1+k\right)\frac{\pi}{2}+n\frac{f_0}{f_c}\times\frac{\pi}{2}\right]\approx\sin\left[\left(1+k\right)\frac{\pi}{2}\right]+\cos\left[\left(1+k\right)\frac{\pi}{2}\right]\times n\frac{f_0}{f_c}\times\frac{\pi}{2} \tag{4.14}$$

where k is an odd number (k=1,3,5,…) in (4.11) - (4.13). Thus $\sin(1+k)\pi/2 = 0$. Further considering n=1 and n=-1in (4.14), we have

$$\sin\left[\left(q_{1,-1}+k\right)\frac{\pi}{2}\right] \approx -\cos\left[\left(1+k\right)\frac{\pi}{2}\right]\frac{f_0}{f_c}\times\frac{\pi}{2} \tag{4.15}$$

$$\sin\left[\left(q_{1,1}+k\right)\frac{\pi}{2}\right] \approx \cos\left[\left(1+k\right)\frac{\pi}{2}\right]\frac{f_0}{f_c}\times\frac{\pi}{2} \tag{4.16}$$

Meanwhile, f_0/f_c can be approximately equal to 0 as $f_c \gg f_0$. Thus we have

$$q_{1,1} \approx q_{1,-1} \approx 1 \tag{4.17}$$

Substituting (4.15) - (4.17) into (4.11) and (4.12) gives

$$K_{1,-1} \approx -K_{1,-1} \approx \frac{1}{3}\frac{f_0}{f_c}K_1 \tag{4.18}$$

where

$$\begin{aligned} K_1 &= J_1\left(\frac{3\pi}{4}M\right) + 2cos\frac{\pi}{6}J_1\left(\frac{\sqrt{3}\pi}{4}M\right) \\ &+\frac{6}{\pi}\sum_{k=3,5,7\ldots}^{\infty}\left[\begin{array}{l}\frac{1}{k-1}sin\left[\left(k-1\right)\frac{\pi}{6}\right] \\ \times\left\{J_k\left(\frac{3\pi}{4}M\right)+2cos\left[\left(3k-2\right)\frac{\pi}{6}\right]J_k\left(\frac{\sqrt{3}\pi}{4}M\right)\right\}\end{array}\right] \\ &+\frac{6}{\pi}\sum_{k=1,3,5\ldots}^{\infty}\left[\begin{array}{l}-\frac{1}{k+1}sin\left[\left(k+1\right)\frac{\pi}{6}\right] \\ \times\left\{J_k\left(\frac{3\pi}{4}M\right)+2cos\left[\left(3k+2\right)\frac{\pi}{6}\right]J_k\left(\frac{\sqrt{3}\pi}{4}M\right)\right\}\end{array}\right] \end{aligned} \tag{4.19}$$

From (4.19), it can be noticed that K_1 is dependent on M only. For PMSGs within the MEA power generation system, they are normally running at high speed and thus the flux-weakening control is essentially required. Under these conditions, the modulation index M is always saturated and remains constant. This will make K_1 a constant value as it is only dependant on M.

Using (4.18) and using the sinusoidal sum-to-product formula, equation (4.10) can be simplified to

$$i_{dc,1,0}(t) \approx \frac{f_0}{f_c} I_{ac} K_1 \sin\alpha \cos\left[2\pi f_c t + \theta_c - \frac{\pi}{2}\right] \tag{4.20}$$

where, α is the power factor angle, and is determined by several facts such as machine parameters, output power and so on. For an electrical generator, the term sinα can be obtained from measurements of dq- currents and voltages of electrical generators using the formula of vector product, which is

$$\sin\alpha = \frac{v_q i_d - v_d i_q}{\sqrt{v_d^2 + v_q^2}\sqrt{i_d^2 + i_q^2}} \tag{4.21}$$

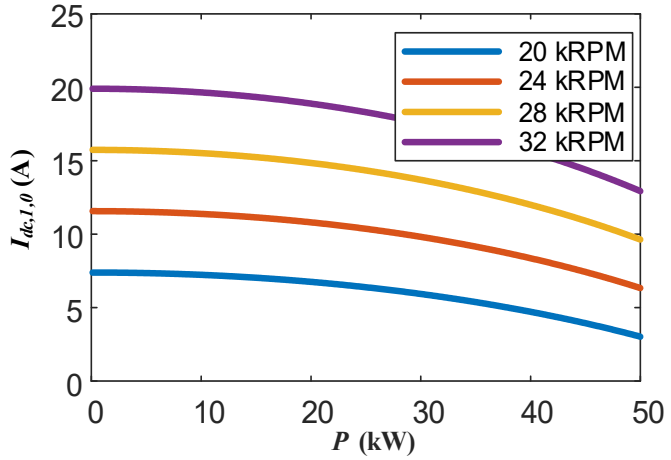
From (4.21), it can be seen that the term sinα can be obtained without requirement of any machine parameters. Substituting (4.21) to (4.20) gives

$$i_{dc,1,0}(t) \approx \frac{f_0}{f_c} K_1 \frac{v_q i_d - v_d i_q}{\sqrt{v_d^2 + v_q^2}} \cos\left[2\pi f_c t + \theta_c - \frac{\pi}{2}\right] \tag{4.22}$$

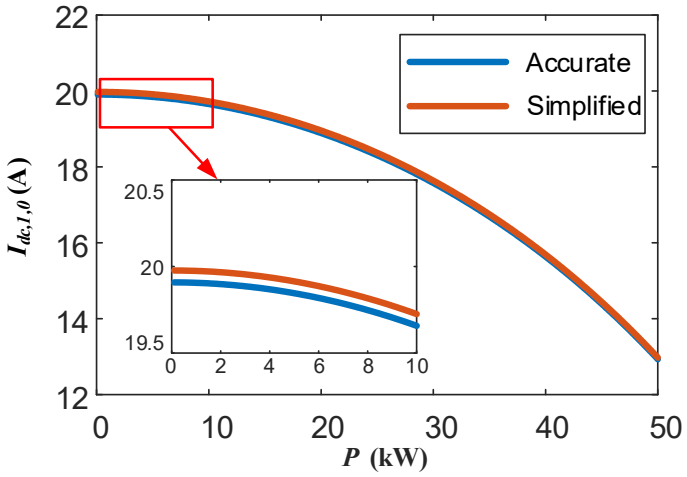
The equation (4.22) shows a simplified model of the first switching harmonic component of the frequency f_c. It can be seen that the phase angle of this harmonic is only determined by phase angle of the carrier signal (θ_c). By shifting the carrier signal phase angle of an AC/DC converter, the component $i_{dc,1,0}(t)$ from different converters can potentially cancel each other.

Figure 4.3 shows the magnitude of $i_{dc,1,0}(t)$ (i.e., $I_{dc,1,0}$) using a permanent magnet generator system developed in the University of Nottingham within the CleanSky AEGART project [107]. As can be seen in Figure 4.3a, the magnitude of harmonic $i_{dc,1,0}$ decreases with an increasing output power. The mathematical proof is given in Appendix A. A higher magnitude can also be noticed with increased rotor speeds. This is because higher rotor speed represents higher fundamental frequency f_0. From (4.22), it can be seen that the magnitude is proportional to fundamental frequency f_0.

Figure 4.3b shows the comparison between detailed model (4.10) and simplified models (4.22). It can be noticed that the discrepancies are less than 0.1A across the entire power range. However, the simplified model is much easier to be implemented in a controller.



(a)



(b)

Figure 4.3: Magnitude of first switching harmonic. a) Magnitudes under different rotor speeds, b) Comparison between simplified model (4.22) and accurate model (4.10) when rotor speed is 32kRPM.

4.3.2 Harmonic component of $2f_c$

The second carrier frequency harmonic also plays a significant role in harmonic spectrum. A simplified model of second carrier harmonic will be introduced in this section. This harmonic component can be derived by substituting i=2, j=0 into (4.8) as

$$\begin{aligned} i_{dc,2,0}(t) &= \frac{I_{ac}}{2} K_{2,-1} \sum_{k=0}^{2} cos\left[2\times 2\pi (f_c) t + 2\theta_c^{[k]} - \alpha \right] \\ &+ \frac{I_{ac}}{2} K_{2,1} \sum_{k=0}^{2} cos\left[2\times 2\pi (f_c) t + 2\theta_c^{[k]} + \alpha \right] \end{aligned} \tag{4.23}$$

Considering no phase shift on carrier signals among three legs, i.e. $\theta_c^{[1]} = \theta_c^{[2]} = \theta_c^{[3]} = \theta_c$, it can be rewritten as

$$\begin{aligned} i_{dc,2,0}(t) &= \frac{3I_{ac}}{2} K_{2,-1} \cos\left[2\times 2\pi (f_c) t + 2\theta_c - \alpha \right] \\ &+ \frac{3I_{ac}}{2} K_{2,1} \cos\left[2\times 2\pi (f_c) t + 2\theta_c + \alpha \right] \end{aligned} \tag{4.24}$$

The coefficients $K_{2,-1}$ and $K_{2,1}$ can be derived with (4.3).

Using similar approximation technique as in the previous section considering f_c is much larger than f_0, we have

$$\begin{aligned} K_2 &\approx K_{2,1} \approx K_{2,-1} \\ &\approx \frac{2}{\pi^2} \left[\begin{array}{l} -\frac{\pi}{6} \left\{ J_1\left(\frac{3\pi}{2} M\right) + 2\cos\left(\frac{\pi}{6}\right) J_1\left(\frac{\sqrt{3}\pi}{2} M\right) \right\} \\ + \sum_{k=1}^{\infty} \left[\begin{array}{l} \frac{1}{k+1} \sin\left[(2+k)\frac{\pi}{2} \right] \cos\left[(k+1)\frac{\pi}{2} \right] \sin\left[(k+1)\frac{\pi}{6} \right] \\ \times \left\{ J_k\left(\frac{3\pi}{2} M\right) + 2\cos\left((2+3k)\frac{\pi}{6}\right) J_k\left(\frac{\sqrt{3}\pi}{2} M\right) \right\} \end{array} \right] \\ + \sum_{k=1}^{\infty} \left[\begin{array}{l} \frac{1}{1-k} \sin\left[(2+k)\frac{\pi}{2} \right] \cos\left[(1-k)\frac{\pi}{2} \right] \sin\left[(1-k)\frac{\pi}{6} \right] \\ \times \left\{ J_k\left(\frac{3\pi}{2} M\right) + 2\cos\left((2-3k)\frac{\pi}{6}\right) J_k\left(\frac{\sqrt{3}\pi}{2} M\right) \right\} \end{array} \right] \end{array} \right] \end{aligned} \tag{4.25}$$

With (4.24) and sum-to-product formula of sinusoidal functions, the magnitude of second carrier harmonic can be expressed as

$$i_{dc,2,0}(t) \approx 3I_{ac}\cos\alpha K_2 \cos\left[2\times(2\pi f_c)t + 2\theta_c\right] \tag{4.26}$$

For a two-level converter, the converter power P at the AC-side terminal can be given as

$$P = 3\frac{I_{ac}}{\sqrt{2}}\frac{V_{ac}}{\sqrt{2}}\cos\alpha = \frac{3I_{ac}MV_{dc}}{4}\cos\alpha \tag{4.27}$$

where V_{ac} is the magnitude of converter phase voltage, M is the modulation index of the converter. From (4.27), we have

$$I_{ac}\cos\alpha = \frac{4P}{3MV_{dc}} = \frac{4I_{dc}}{3M} \tag{4.28}$$

Substituting (4.28) to (4.26) gives

$$i_{dc,2,0}(t) = \frac{4I_{dc}K_2}{M}cos\left(4\pi f_c t + 2\theta_c\right) \tag{4.29}$$

where I_{dc} is the DC component of the current i_{dc} on DC-bus. With (4.22) and (4.29), the switching frequency harmonics can be derived and the implementation of such equations in a generation system is shown in Figure 4.4, where I_1 and I_2 represent $I_{dc,1,0}$ and $I_{dc,2,0}$ respectively.

Comparison between magnitudes of simplified model and original model is given in Figure 4.5. The modulation index is set as 1.10 ($0.95 \times 2/\sqrt{3}$) which reflects the fact that PMSG always works under flux weakening operation conditions. It can be seen that the harmonic component ($I_{dc,2,0}$) from detailed equation (4.24) and simplified one (4.29) matches very well, especially when the power is higher than 10kW. With the power increases, the power factor α will move towards to zero with more active power from electrical generator while the reactive power for de-fluxing kept almost the same. From (4.24), two components on the right side of the equation are symmetric, this means improvement of the accuracy of the simplification. In practice, we are more

interested in high-power operation and this is the operation region where power quality issues should be more carefully addressed.

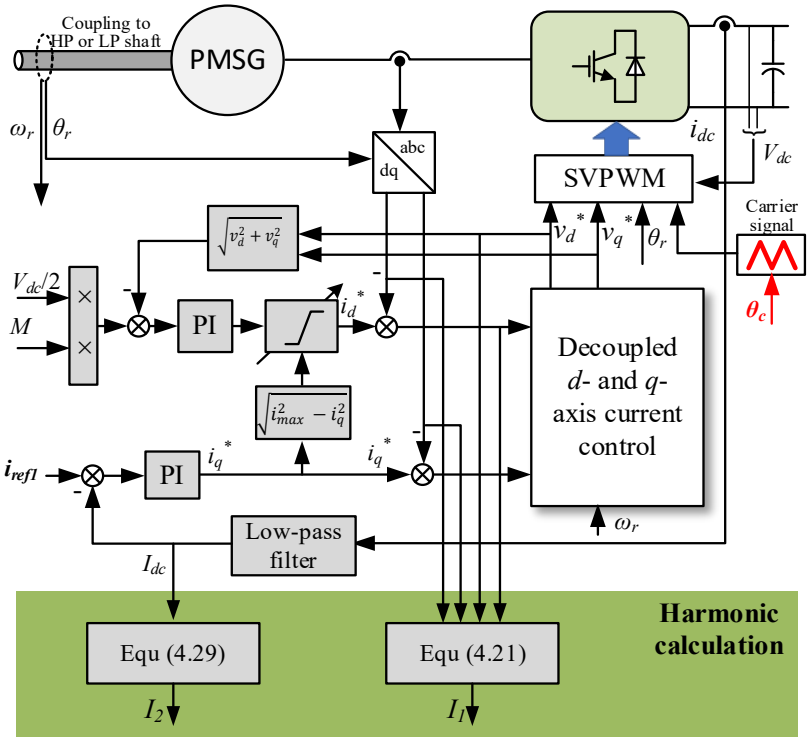


Figure 4.4: Control diagram and harmonic calculation scheme of single PMSG system.

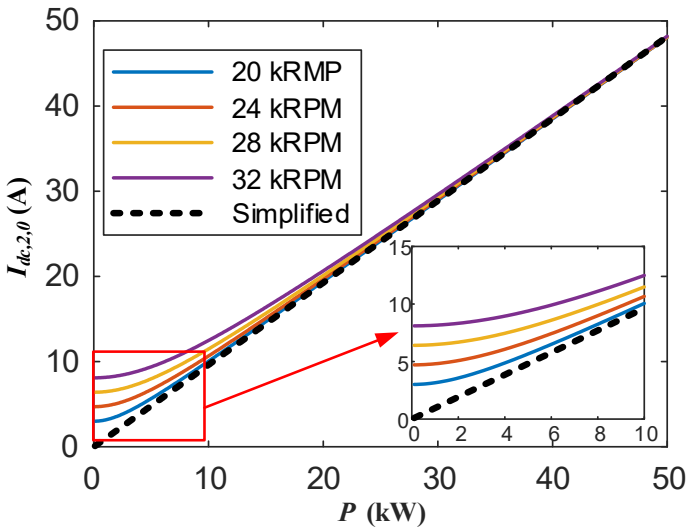


Figure 4.5: Comparison of second carrier harmonic component from accurate (4.24) and simplified (4.29) models with increased generator power and speed.

From (4.29), it is important to point out that the magnitude of the second carrier harmonic current is proportional to DC-link current (I_{dc}) and its phase angle of this component is determined by the angle of carrier signal (θ_c) only. This means that the phase angle of second carrier harmonic on DC-bus current can be controlled by carrier signal θ_c within the AC/DC converter. If the phase angles are shifted by 180^o between two AC/DC converters, the second carrier frequency harmonic will cancel each other fully if they are of the same magnitudes.

From Figure 4.3, we can see that the first switching harmonic $I_{dc,1,0}$ decreases when output power increases. However, from Figure 4.5, we identify that the second carrier harmonic will increase with more power output. This means that the first carrier harmonic tends to be dominant under low power range while the second carrier harmonic tends to be dominant when there is a higher power demand. Although the harmonic cancellation can be achieved by shifting the carrier signal phase angle θ_c for different converters, the first and second carrier frequency harmonics require different phase shift angles. Thus, an optimised trade-off scheme needs to be identified.

4.4 Capacitor Harmonic Minimisation Method

Using models developed in Section 4.3, a harmonic minimisation scheme can be proposed. The aim of this scheme is to achieve an optimal trade-off solution to suppress first and second carrier frequency at the same time. This is achieved using an active phase shift concept. The system to be studied is with two generators with two AC/DC converters as shown in Figure 4.6. The local controller is essentially described in Figure 4.4. The local controller outputs the magnitudes of f_c and $2f_c$ harmonic components to a central phase shift controller and receives carrier phase shift angle from the phase shift controller. The design consideration of this phase shift controller is discussed in this section.

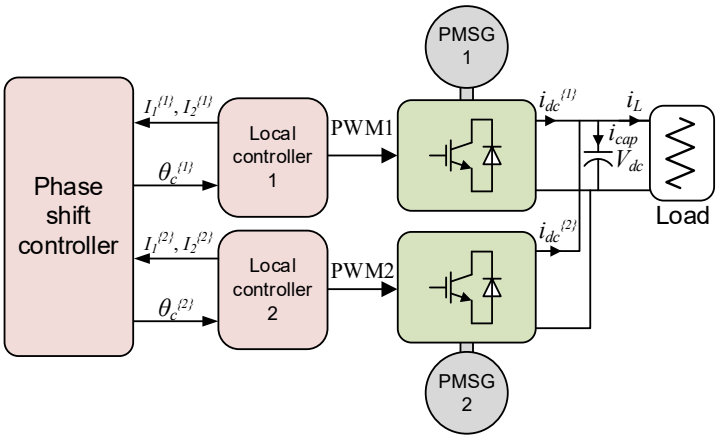


Figure 4.6: Control diagram of a dual-generator power system.

To minimise the voltage ripple on DC capacitor, weighted total harmonic distortion of the capacitor should be analyzed, which is

$$I_{hf} = f_c \sqrt{\sum_{kf=1}^{\infty} \left(\frac{I_{kf}}{f_{kf}} \right)^2} \tag{4.30}$$

where I_{hf} is total harmonics on DC capacitor, f_{kf} is frequency of kfth order harmonic. I_{kf} is the magnitudes of summed kfth order harmonic from all converters connected to the common dc bus. As discussed in Section 4.2, only harmonics on f_c and $2f_c$ have potential of cancelling due to no impacts from the fundamental frequencies. Hence, these two components are extracted from (4.30)

$$I_{hf\_1,2} = f_c \sqrt{\left(\frac{I_{fc}}{f_c} \right)^2 + \left(\frac{I_{2fc}}{2f_c} \right)^2} = \sqrt{I_{fc}^{\,2} + \frac{I_{2fc}^{\,2}}{4}} \tag{4.31}$$

Here, we use subscripts to represent the frequencies of the harmonic for convenience. Using phase angles of the components given from (4.22) and (4.29), (4.31) can be rewritten as

$$
\begin{aligned}
I_{hf\_1,2} &= \frac{1}{2}\sqrt{\begin{matrix}4\left|I_1^{\{1\}}\angle\left(\theta_c^{\{1\}}-\frac{\pi}{2}\right)+I_1^{\{2\}}\angle\left(\theta_c^{\{2\}}-\frac{\pi}{2}\right)\right|^2 \\ +\left|I_2^{\{1\}}\angle\left(2\theta_c^{\{1\}}\right)+I_2^{\{2\}}\angle\left(2\theta_c^{\{2\}}\right)\right|^2\end{matrix}} \\
&= \frac{1}{2}\sqrt{\begin{matrix}4\left(I_1^{\{1\}}\right)^2+4\left(I_1^{\{2\}}\right)^2+8I_1^{\{1\}}I_1^{\{2\}}\cos\Delta\theta_c \\ +\left(I_2^{\{1\}}\right)^2+\left(I_2^{\{2\}}\right)^2+2I_2^{\{1\}}I_2^{\{2\}}\cos 2\Delta\theta_c\end{matrix}} \\
&= \frac{1}{2}\sqrt{\begin{matrix}4I_2^{\{1\}}I_2^{\{2\}}\cos^2\Delta\theta_c+8I_1^{\{1\}}I_1^{\{2\}}\cos\Delta\theta_c \\ +4\left(I_1^{\{1\}}\right)^2+4\left(I_1^{\{2\}}\right)^2+\left(I_2^{\{1\}}\right)^2+\left(I_2^{\{2\}}\right)^2-2I_2^{\{1\}}I_2^{\{2\}}\end{matrix}}
\end{aligned}
\tag{4.32}
$$

Here, $\theta_c^{\{1\}}$ and $\theta_c^{\{2\}}$ are phase angles of carrier signals. $I_1^{\{1\}}$, $I_2^{\{1\}}$, $I_1^{\{2\}}$, and $I_2^{\{2\}}$ are the magnitudes of harmonics from each converter. Here, superscripts in square brackets '{}' are indexes of the converters. $\Delta\theta_c$ is the phase-shift angle between two converters which is

$$\Delta\theta_c = \theta_c^{\{2\}} - \theta_c^{\{1\}} \tag{4.33}$$

In (4.32), variable f_c, $I_1^{\{1\}}$, $I_2^{\{1\}}$, $I_1^{\{2\}}$ and $I_2^{\{2\}}$ are determined by power flow supervised by system level controller. Minimising the total switching frequency harmonics $I_{hf\_1,2}$ can thus be achieved by adjusting $\Delta\theta_c$. Using basic law of quadratic and triangle function, the optimised phase-shift angle can be derived from (4.32) as

$$
\Delta\theta_c = \begin{cases}\cos^{-1}\left(-\dfrac{I_1^{\{1\}}I_1^{\{2\}}}{I_2^{\{1\}}I_2^{\{2\}}}\right), & \dfrac{I_1^{\{1\}}I_1^{\{2\}}}{I_2^{\{1\}}I_2^{\{2\}}}<1 \\ \pi, & \dfrac{I_1^{\{1\}}I_1^{\{2\}}}{I_2^{\{1\}}I_2^{\{2\}}}\geq 1\end{cases}
\tag{4.34}
$$

Based on (4.34), a phase-shift controller can be designed as shown in Figure 4.7.

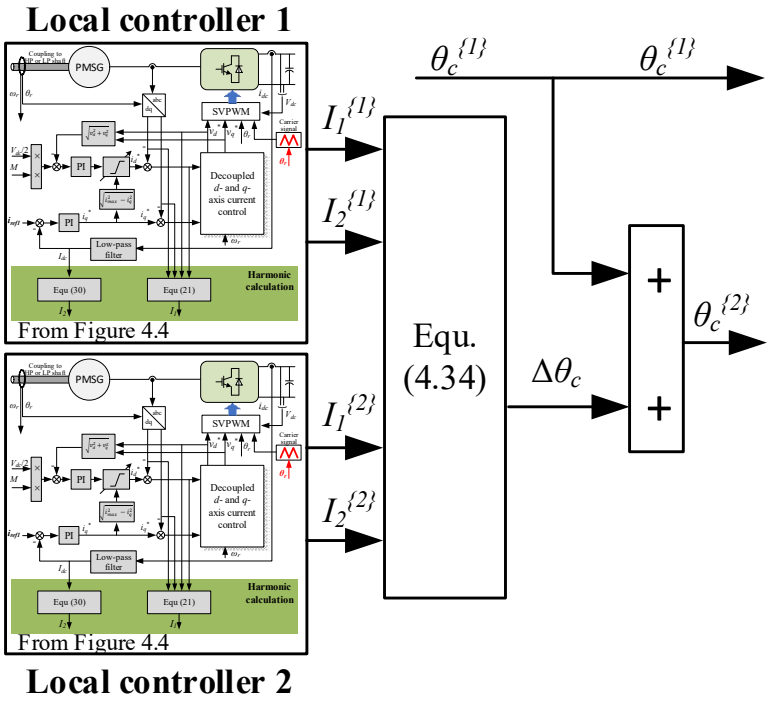


Figure 4.7: Phase-shift controller.

In the implementation, the phase angle of carrier signal of one converter can be fixed (say converter 1), and the carrier signal for the other converter is adjusted using (4.34). According to (4.34), optimised $\Delta\theta_c$ is also determined by magnitudes of the first and second carrier harmonics from each converter.

To give a clear result of how $\Delta\theta_c$ varies, it is assumed that two converters supply the same power to the downstream loads. Figure 4.8 shows the optimised phase-shift angle versus output power of single converter using (4.34). It can be seen that when output power is lower than a barrier (around 10kW in this case), the optimised $\Delta\theta_c$ is 180° constantly. As discussed, under low power region, the first switching component dominates the harmonic spectrum. Thus using (4.22) , phase difference of the first carrier harmonics from two converter is $\theta_c^{\{2\}}$- $\theta_c^{\{1\}}$. Hence, a 180-degree phase difference between carrier signals of two converters can reduce the most of first switching harmonic harmonics.

With higher output power, the second carrier components become dominant. Then the phase-shift angle needs to be adjusted. With higher output power,

optimised $\Delta\theta_c$ keeps dropping down. According to (4.29), phase difference between the second carrier harmonics of two converters is $(2\theta_c^{\{2\}}\text{-}2\theta_c^{\{1\}})$. When output power is high enough to be dominant, it is the equation $(2\theta_c^{\{2\}}\text{-}2\theta_c^{\{1\}}) = 180°$ to be used in the system controller. Then, phase difference between the two carrier signals ($\theta_c^{\{2\}}$- $\theta_c^{\{1\}}$ or $\Delta\theta_c$) should be 90°. This explains why the optimised angle drops approximately to 90°.

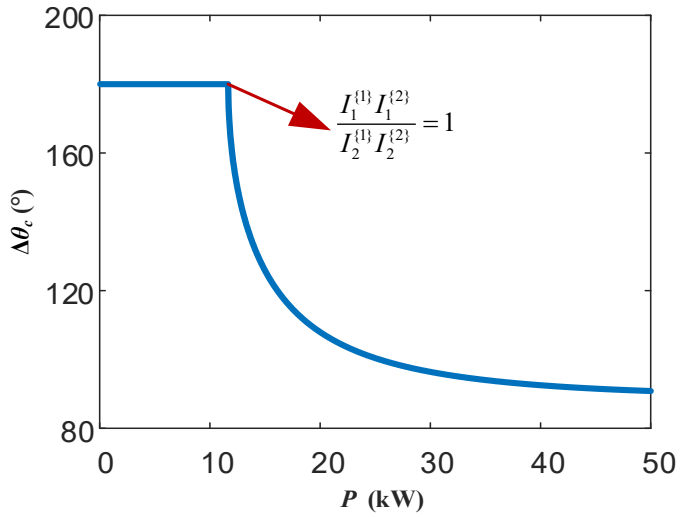


Figure 4.8: Optimised $\Delta\theta_c$ when power sharing ratio between two converters is 1:1.

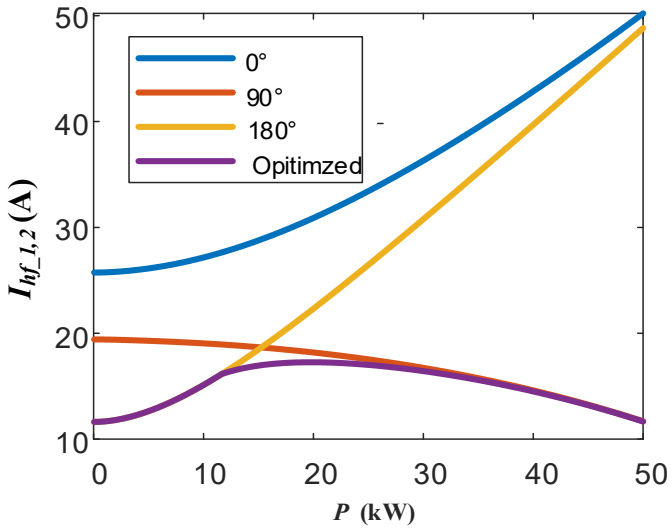


Figure 4.9: $I_{hf\_1,2}$ versus output power of single converter.

The active phase shifting mechanism developed with (4.34) ensures that the $I_{hf\_1,2}$ has been suppressed in its lowest level. Figure 4.9 shows a comparison of $I_{hf\_1,2}$ with different phase-shift strategies. It can be seen that when no phase shift applied, i.e. $\Delta\theta_c$ =0, $I_{hf\_1,2}$ shows highest value across the entire power range. The case with phase shift of 90° works better than that of 180° under high power region, while the case with phase shift angle of 180° works better under low power region. The proposed mechanism combines benefits from both angles and achieves the best $I_{hf\_1,2}$.

4.5 Simulation Results

Simulation is implemented with Matlab/Simulink and PLECS to validate the performance of the proposed harmonic models and cancellation method. Simulation is implemented with Matlab/Simulink and PLECS to validate the performance of the proposed harmonic models and cancellation method. Two PMSGs developed in [107] supply the DC bus, and the phase shift algorithm proposed in previous section is applied, as shown in Figure 4.10.

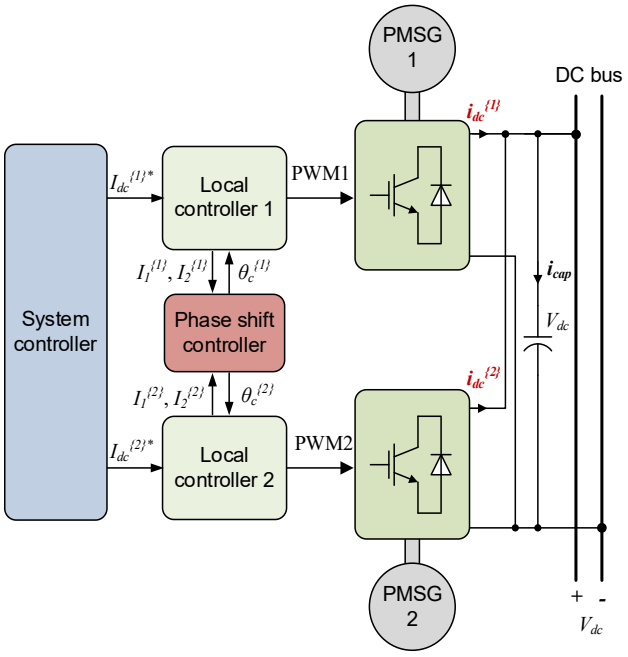


Figure 4.10: Simulation diagram.

Some basic control parameters are given in Table 4-1. The rotor speed of the two PMSG are 20kRPM and 30kRPM, as they are driven by HP and LP shafts of the engine, respectively. Switching frequencies of the two converters are the same, which is 32 kHz. The power load is set as 10kW and 80kW to validate the different phase-shift strategies under low- and high-power ranges.

Table 4-1: Simulation parameters of two AC-DC converters supply the DC-link with SVPWM operation.

Category	Parameters	Values
PMSG parameters	Rotor speed	20kRPM & 30kRPM
	Switching frequency	32kHz
	Maximum modulation index	1.04 ($0.9 \times 2/\sqrt{3}$)
	dq-current controller bandwidth	1000 Hz
DC-link	DC-link capacitance	400μF
	Load power	10kW and 80kW

Figure 4.11a-d show the spectrums of DC bus current from converter 1 and 2 ($i_{dc}^{\{1\}}$ and $i_{dc}^{\{2\}}$), capacitor currents (i_{cap}) under different power output and phase-shift strategies. Converter 1 and 2 generate the power with a sharing ratio of 1:1. Components on f_c and $2f_c$ are highlighted in red.

Figure 4.11a shows the result when power generated from single converter is 5kW and there is no phase-shift angle between two carrier signals. Switching harmonics on both buses just sum up on capacitor, hence significant components show on both the frequencies of f_c and $2f_c$. For $i_{dc}^{\{1\}}$ and $i_{dc}^{\{2\}}$, magnitudes of the first switching harmonics are higher than the second ones. In Figure 4.11b, to mostly supress first switching harmonic, a phase difference of 180° is applied according to Figure 4.8. Compared to Figure 4.11a, the first switching harmonic on capacitor is reduced from 24.92A to 10.41A (58% reduction). However, the second carrier harmonic are with no difference

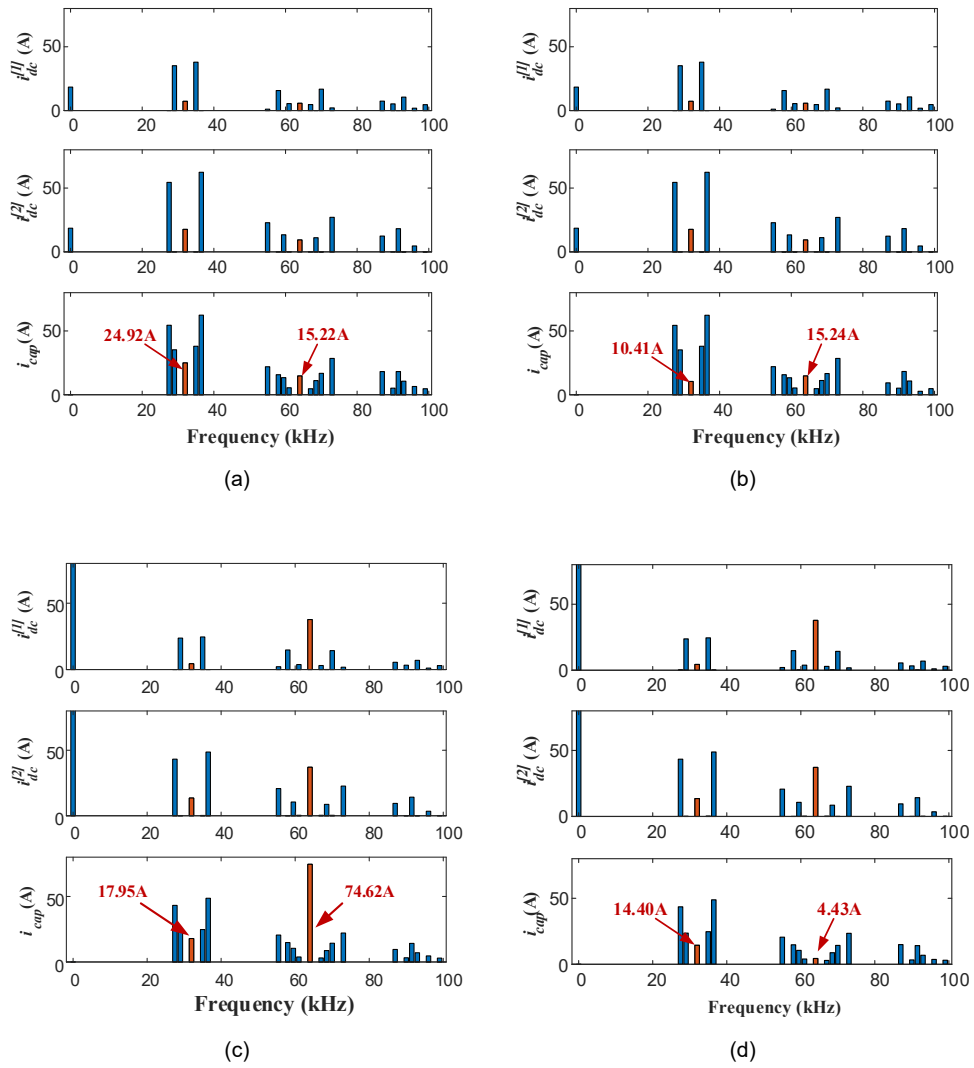


Figure 4.11: Current spectrums of $i_{dc}^{\{1\}}$, $i_{dc}^{\{2\}}$, and i_{cap}. a) 5kW, no phase shift, b) 5kW, optimised phase shift, c) 40kW, no phase shift, d) 40kW, optimised phase shift.

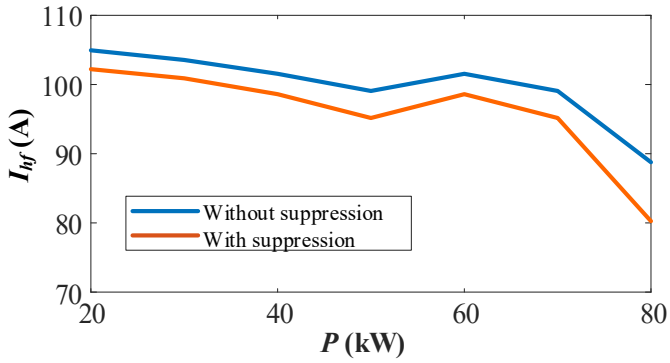
because phase angle of the second carrier harmonic is $2\theta_c$. 180° phase difference on carrier signals results in 360° difference on the second carrier harmonic, which is same as with no phase shift.

In Figure 4.11c and d, output power per converter is increased to 40kW. As analysed in former sections, the second carrier harmonic become more significant compared to the first one. Therefore, a larger second order component shows in Figure 4.11c because there is no phase shift action here.

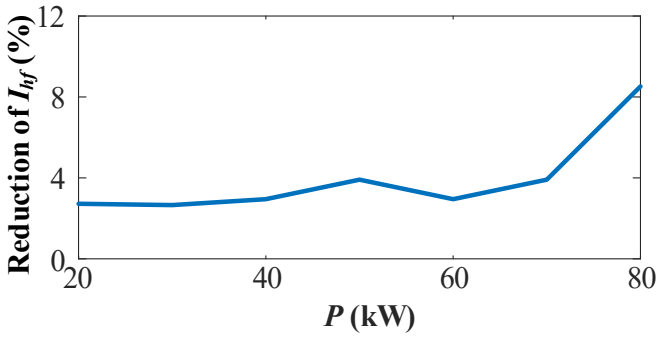
To maximum the suppression on both the first and the second carrier harmonics, optimised phase shift angle is set as 92.2° according to (4.34). The results are shown in Figure 4.11d. The second carrier harmonic on capacitor is significantly reduced from 74.62A to 4.43A (96% reduction). Such an almost 100% suppression is because proportional relationship between the second carrier harmonic and output power, which has been proved in (4.29). When the two sources generate same power, magnitudes of the second carrier harmonics from two converters are almost same. With a nearly 180° (2×90°) phase difference between two components, the suppression is quite effective as shown here.

Apart from the second carrier harmonics, the first switching harmonic is also suppressed as shown in Figure 4.11d. It is reduced from 17.95A to 14.40A (19.8% reduction). Although 90° phase difference is not as good as 180°, it still helps weaken the sum component of this order.

In the simulation study, I_{hf} is calculated under different output power and power sharing ratio of 1:1, as shown in Figure 4.12a. The sideband harmonics show no variation when the proposed method is applied. I_{hf} is suppressed in the whole range. Figure 4.12b shows the percentage reduction in I_{hf} with the variation of the output power after applying the proposed method. A reduction of about 3% is realized when the output power is low (i.e. 20kW). When the output power is higher (i.e. 80kW), the percentage reduction becomes more significant (about 8%). Therefore, the capacitance can be chosen based on the output power range. If the output power is high, a low capacitance can be chosen. On average, a 5% reduction of capacitance can be achieved.



(a)



(b)

Figure 4.12: I_{hf} variation after applying the proposed method.

4.6 Chapter Summary

In this chapter, simplified mathematical models for DC-link harmonics on the AC-DC converter are investigated. The calculation burden of microprocessor is significantly released. For the first switching harmonic, magnitude can be achieved with the measurements of *dq*- voltages and currents. For the second carrier harmonic, the magnitude is proportional to the DC component of the output current.

Based on the simplified models, a cancellation method of DC-link harmonics was proposed. Under low power range, phase-shift angle is set as 180° to suppress the first carrier harmonic mostly. When the output power increases,

the phase-shift angle is adjusted from 180° to 90° actively to suppress both the first and second carrier harmonics.

Finally, simulation was implemented to verify the validity of the proposed harmonic models and the cancellation method.

Chapter 5

Using DC-DC Converters as Harmonic Suppression Device

5.1 Introduction

The previous chapters (Chapter 3 and Chapter 4) focused on harmonic cancellation of switching frequency f_c or double switching frequency $2f_c$ using AC-DC converters. This chapter aims to extend the research and study the potentiality of using buck-boost DC-DC converters as an active harmonic sink to suppress other harmonics. To simplify the analysis, the AC-DC converter is made to operate under SPWM control.

For the DC-DC converter, a new modulation scheme is proposed to actively change the magnitudes and phase angles of its harmonic components. Some specific harmonics on a DC-bus thus can be suppressed by tuning the magnitude and phase angle of this specific harmonic component from a DC-DC converter. In this chapter, although we focus on some specific harmonic component (the first side band harmonic), the proposed method can essentially be used to suppress any harmonic component of interest by simply changing the phase angle and frequency of the carrier signal as well as the position of 'on' switching states of power devices in one cycle within the DC-DC converter.

This chapter is organised in the following manner. Section 5.2 presents a harmonic analysis of the two-level AC-DC converter, specifically on the side-band of first switching frequency harmonic component. Section 5.3 illustrates a new PWM method of a DC-DC converter for adjusting magnitudes of harmonics. Section 5.34 proposes a harmonic suppression method with an

enhanced PWM synchronisation method for implementation considered in Section 5.5. Section 5.6 presents the simulation results. Section 0 introduces suppressing both the second order switching frequency harmonic and the sideband first order switching frequency harmonics at the same time considering two AC-DC converters and one DC-DC converter feeding a common DC-bus. Section 5.7 concludes this chapter.

5.2 Harmonic Analysis of Two-Level AC-DC Converter in The First Order Side Band

As discussed in Chapter 3, the DC-bus harmonic currents generated from one phase leg can be derived as

$$\begin{aligned} & i_{dc}^{[k]}(t) = i_{ac}^{[k]}(t)\, sf^{[k]}(t) \\ & = \frac{I_{ac}}{2} K_{0,1}\left[\cos\left(4\pi f_0 t + 2\beta + \alpha + \frac{4k\pi}{3}\right) + cos\alpha\right] \\ & + \frac{I_{ac}}{2}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} K_{m,n}\left\{\begin{array}{l}\cos\left[2\pi\left(mf_c + (n+1) f_0\right)t + \sigma_{m,n}^{[k]}\right] \\ +\cos\left[2\pi\left(mf_c + (n-1) f_0\right)t + \varphi_{m,n}^{[k]}\right]\end{array}\right\} \end{aligned} \tag{5.1}$$

where $\sigma_{m,n}^{[k]}$ and $\varphi_{m,n}^{[k]}$ are phase angles of each component, which are

$$\sigma_{m,n}^{[k]} = m\theta_c^{[k]} + (n+1)\left(\beta + \frac{2k\pi}{3}\right) + n\alpha \tag{5.2}$$

$$\varphi_{m,n}^{[k]} = m\theta_c^{[k]} + (n-1)\left(\beta + \frac{2k\pi}{3}\right) + n\alpha \tag{5.3}$$

Extracted from (5.1), the DC-side current harmonics in a specific frequency (if_c+jf_0) should be expressed as a sum of components from three legs as

$$\begin{aligned} & i_{dc,i,j}^{[g]}(t) = \frac{I_{ac}}{2} K_{i,j-1}\sum_{k=0}^{2}\cos\left[2\pi\left(if_c + jf_0\right)t + \sigma_{i,j-1}^{[k]}\right] \\ & + \frac{I_{ac}}{2} K_{i,j+1}\sum_{k=0}^{2}\cos\left[2\pi\left(if_c + jf_0\right)t + \varphi_{i,j+1}^{[k]}\right] \end{aligned} \tag{5.4}$$

where i and j mean switching and band side orders of DC-bus current harmonics. For instance, substituting i=1 and j=3 into (5.4) gives the expression of harmonic in the frequency of f_c+3f_0. Here we use a superscript [g] indicating this harmonic is associated with the generator connected the AC-DC converter and is to differentiate it with the DC-DC converter which will be discussed in the later sections.

5.2.1 Harmonics on f_c±3f_0

This subsection will analyse the harmonic in f_c-3f_0 firstly. Considering no phase shift on carrier signals among three legs, i.e., $\theta_c^{[1]}=\theta_c^{[2]}=\theta_c^{[3]}=\theta_c$ and substituting i=1 and j=-3 into (5.4), we have

$$\begin{aligned} i_{dc,1,-3}^{[g]}(t) &= \frac{3I_{ac}}{2}K_{1,-4}cos\left[2\pi\left(f_c-3f_0\right)t+\sigma_{1,-4}\right] \\ &+\frac{3I_{ac}}{2}K_{1,-2}cos\left[2\pi\left(f_c-3f_0\right)t+\varphi_{1,-2}\right] \end{aligned} \tag{5.5}$$

For the coefficient $K_{1,-4}$ and $K_{1,-2}$, we have

$$K_{1,-4}=\frac{2}{\left(1-4\frac{f_0}{f_c}\right)\pi}J_4\left(\frac{\pi}{2}\left(1-4\frac{f_0}{f_c}\right)M\right) \tag{5.6}$$

$$K_{1,-2}=-\frac{2}{\left(1-2\frac{f_0}{f_c}\right)\pi}J_2\left(\frac{\pi}{2}\left(1-2\frac{f_0}{f_c}\right)M\right) \tag{5.7}$$

Assuming that $f_c >> f_0$ (in typical cases, f_c is at least 20 times the frequency of f_0), the term f_0/f_c can be neglected as it is approximately equal to 0. Then, (5.5) can be approximated as expressed in (5.8).

$$\begin{aligned} i_{dc,1,-3}(t) &\approx \frac{3I_{ac}}{\pi}J_4\left(\frac{\pi}{2}M\right)\cos\left[2\pi\left(f_c-3f_0\right)t+\sigma_{1,-4}\right] \\ &-\frac{3I_{ac}}{\pi}J_2\left(\frac{\pi}{2}M\right)cos\left[2\pi\left(f_c-3f_0\right)t+\varphi_{1,-2}\right] \end{aligned} \tag{5.8}$$

Comparing the two terms in (5.8), their magnitudes have different Bessel functions and are given in (5.9).

$$\frac{3I_{ac}}{\pi}J_4\left(\frac{\pi}{2}M\right) \text{ and } -\frac{3I_{ac}}{\pi}J_2\left(\frac{\pi}{2}M\right) \tag{5.9}$$

In (5.9), modulation index (M) is always less than 1, because of the limited output voltage of the AC-DC converter. Comparison between the two Bessel function terms when M<1 is shown in Figure 5.1.

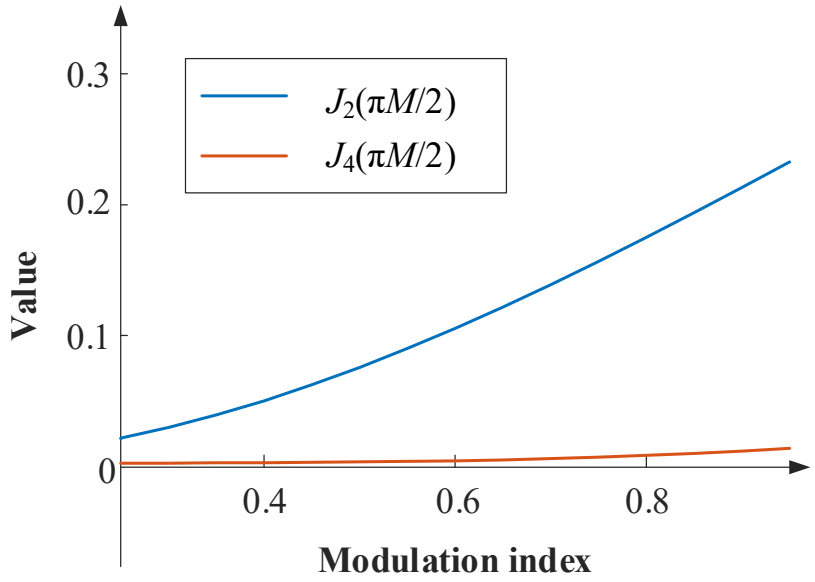


Figure 5.1: Comparison between $J_2(\pi M/2)$ and $J_4(\pi M/2)$ with increased modulation index.

It can be seen that $J_4(\pi M/2)$ is almost zero, and $J_2(\pi M/2)$ is more than 20 times of $J_4(\pi M/2)$. Hence, the first term $J_4(\pi M/2)$ is neglectable in (5.8). Therefore, the expression in (5.8) becomes as in (5.10).

$$i_{dc,1,-3}^{[g]}(t) \approx \frac{3I_{ac}}{\pi}J_2\left(\frac{\pi}{2}M\right)\cos\left[2\pi\left(f_c-3f_0\right)t+\varphi_{1,-2}+\pi\right] \tag{5.10}$$

With (5.10), the magnitude of dc-current first-side band f_c-3f_0 component $I_{dc}^{[g]}{}_{,1,-3}$ can be derived. There, M will be a fixed value if PMSG works under

flux-weakening operation (which is a normal case for aerospace application). I_{ac} is measured by current sensors which is

$$I_{ac} = \sqrt{i_d^2 + i_q^2} \tag{5.11}$$

where i_d and i_q are the d- and q-axis currents of the PMSG. Apart from magnitude, the phase angle of the component in (5.10) can be derived from (5.3) which gives the expression as

$$\varphi_{1,-2} + \pi = \theta_c - 2(\alpha + \beta) - \beta + \pi \tag{5.12}$$

where β is the angle between phase current and its AC side voltage (back-emf in PMSG), α is the power factor angle. Both of them can be achieved from voltages and currents in dq-frame which are

$$\alpha + \beta = \text{atan2}\left(v_q, v_d\right) \tag{5.13}$$

$$\beta = \text{atan2}\left(i_q, i_d\right) \tag{5.14}$$

Here, the function atan2(y, x) gives the angle of complex value (x+iy). Therefore, the magnitude ($I_{dc,1,-3}^{[g]}$) and phase angle ($\theta_{dc,1,-3}^{[g]}$) of the harmonic in f_c-3f_0 can be summarized from (5.11) to (5.14) as

$$I_{dc,1,-3}^{[g]} \approx \frac{3\sqrt{i_d^2 + i_q^2}}{\pi} J_2\left(\frac{\pi}{2}M\right) \tag{5.15}$$

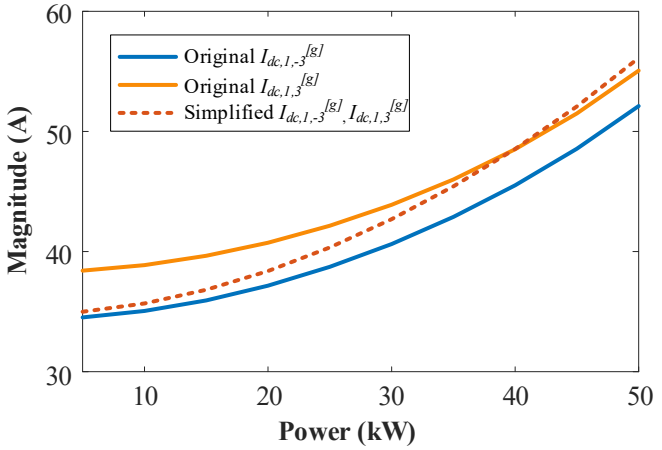
$$\theta_{dc,1,-3}^{[g]} \approx \theta_c - 2\text{atan2}\left(v_q, v_d\right) - \text{atan2}\left(i_q, i_d\right) + \pi \tag{5.16}$$

Following the same process, the magnitude and phase angle of the harmonic in f_c+3f_0 harmonic component can be calculated and simplified as

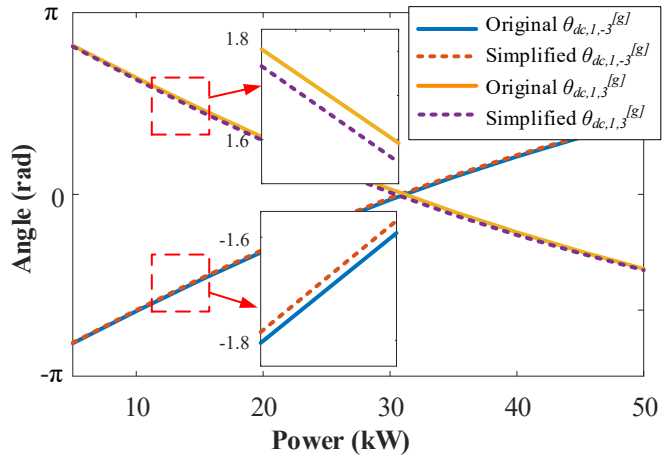
$$I_{dc,1,3}^{[g]} \approx \frac{3\sqrt{i_d^2 + i_q^2}}{\pi} J_2\left(\frac{\pi}{2}M\right) \tag{5.17}$$

$$\theta_{dc,1,3}^{[g]} \approx \theta_c + 2\text{atan2}\left(v_q, v_d\right) + \text{atan2}\left(i_q, i_d\right) + \pi \tag{5.18}$$

From (5.15) and (5.17), it is important to notice that the simplified magnitudes of these two components of frequencies f_c-3f_0 and f_c+3f_0 are essentially the same. A comparison between the simplified models and original models is given in



(a)



(b)

Figure 5.2: Comparison between magnitudes of the simplified and original model on f_c-3f_0 and f_c+3f_0. a) Magnitudes. b) Angles.

Figure 5.2. The magnitude errors are always less than 3A, which is less than 10% of the original model. The angle errors are less than 0.02 rad, which is marginal. Therefore, the simplified model can be adopted and used for the harmonic suppression technique development.

5.2.2 Component selection for suppression

It has been discussed before that another significant harmonic exists in the frequency of $2f_c$. From Chapter 3, the magnitude of this component is analyzed and simplified as

$$I_{dc,2,0}^{[g]} \approx \frac{3I_{ac}\cos\alpha}{\pi} J_1(\pi M) \tag{5.19}$$

With (5.19) and dividing the magnitude of this second ($2f_c$) switching frequency component by that of the first-order side band component in (5.15) or (5.17) gives

$$\frac{I_{dc,2}^{[g]}}{I_{dc,1}^{[g]}} \approx \frac{I_{dc,2,0}^{[g]}}{I_{dc,1,-3}^{[g]}} \approx \frac{I_{dc,2,0}^{[g]}}{I_{dc,1,3}^{[g]}} \approx \left| \frac{J_1(\pi M)}{J_2\left(\frac{\pi}{2}M\right)} \cos\alpha \right| \tag{5.20}$$

where $I_{dc,2}^{[g]}$ is the simplified magnitude of harmonics in $2f_c$. $I_{dc,1}^{[g]}$ is the simplified magnitude of harmonics in $f_c \pm 3f_0$.

Due to the cosine value is always less than 1, it can be obtained from (5.20) that

$$\frac{I_{dc,2}^{[g]}}{I_{dc,1}^{[g]}} \approx \left| \frac{J_1(\pi M)}{J_2(\pi M/2)} \cos\alpha \right| < \left| \frac{J_1(\pi M)}{J_2(\pi M/2)} \right| \tag{5.21}$$

Considering the fact that the AC-DC power converter is connected to PMSGs which always work under flux-weakening conditions in MEA (because of wide shaft speed range of engine), the modulation index (M) will always higher than 0.9. Therefore, the $|J_1(\pi M)/J_2(\pi M/2)|$, which will enclose the division $I_{dc,2}^{[g]} / I_{dc,1}^{[g]}$ in (5.21) can be presented in Figure 5.3.

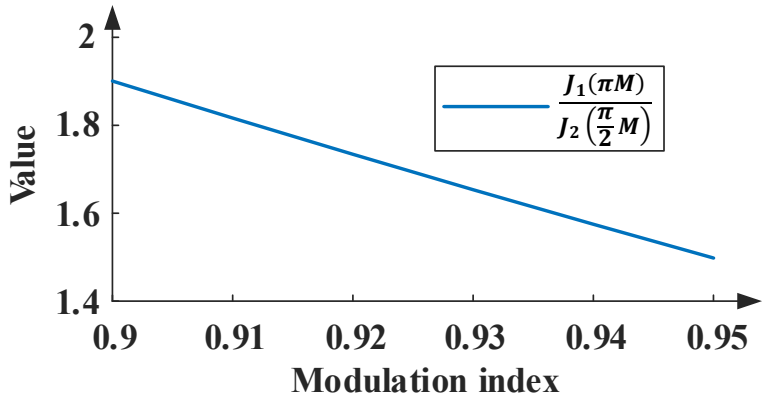


Figure 5.3: $J_2(\pi M)/J_2(\pi M/2)$ with modulation index increases.

Seen from Figure 5.3, the ratio between $I_{dc,2}$ and $I_{dc,1}$ is always less than 2 when the modulation index is higher than 0.9. Hence, we can conclude that

$$\frac{I_{dc,2}^{[g]}}{I_{dc,2}^{[g]}} < \left| \frac{J_1(\pi M)}{J_2\left(\frac{\pi}{2}M\right)} \right| < 2 \tag{5.22}$$

To minimise the voltage ripple on the DC capacitor, total capacitor harmonics of switching frequencies should be analysed as follows

$$I_{hf} = \sqrt{\sum_{k=1}^{\infty}\left(\frac{I_k}{f_k}\right)^2} \tag{5.23}$$

where I_{hf} is total harmonics on DC capacitor, f_k is the frequency of kth order harmonic, I_k is the magnitudes of summed kth order harmonics. In (5.22), $I_{dc,2}$ and $I_{dc,1}$ divide by f_c and rearrange the equation, we have

$$\left(\frac{I_{dc,2}^{[g]}}{2f_c}\right)^2 < \left(\frac{I_{dc,1}^{[g]}}{f_c}\right)^2 \tag{5.24}$$

Meanwhile, f_c-3f_0<f_c<f_c+3$f_0$we have

$$\left(\frac{I_{dc,2}^{[g]}}{2f_c}\right)^2 < \left(\frac{I_{dc,1}^{[g]}}{f_c}\right)^2 < \left(\frac{I_{dc,1}^{[g]}}{f_c - 3f_0}\right)^2 \tag{5.25}$$

$$\left(\frac{I_{dc,1}^{[g]}}{f_c+3f_0}\right)^2 < \left(\frac{I_{dc,1}^{[g]}}{f_c-3f_0}\right)^2 \tag{5.26}$$

From (5.25) and (5.25), it can be seen that component in f_c-$3f_0$ contributes more on DC-link fluctuation compared to that in $2f_c$ and f_c+$3f_0$. Hence, this chapter focuses more on the harmonic suppression in the frequency of f_c-$3f_0$ if only one DC/DC converter is connected to a DC bus.

5.3 Equal Gate Width (EGW) PWM of a Bi-Directional Buck-Boost Converter

This section will discuss harmonic generated from a typical buck-boost DC-DC converter. As shown in Figure 5.4, the bidirectional buck-boost DC-DC converter consists of two power switches (S1 and S2) with anti-parallel diodes and a filtering inductor L_b. The port on the left is connected to a battery with a voltage V_b, and the port on the right is connected to a DC-bus with voltage V_{dc}. This DC-DC converter allows the battery to work under both charging and discharging modes. However, in this chapter, we focus on the discharging mode only.

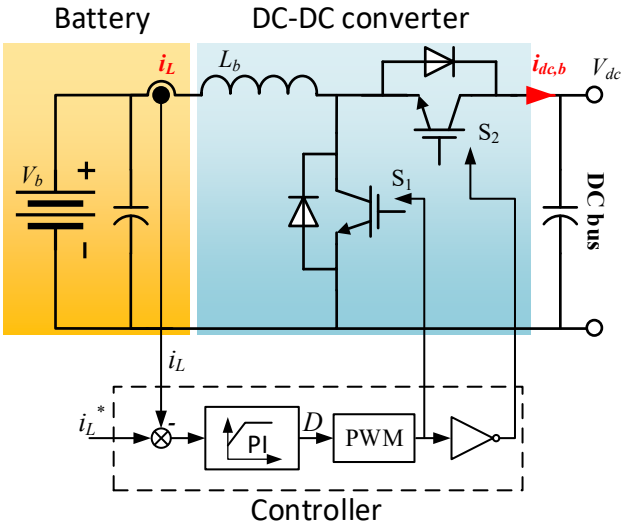


Figure 5.4: Bidirectional buck-boost converter.

5.3.1 Conventional DC-DC converter control and PWM operation

Within the studied hybrid electric power generation centre, a secondary level supervision unit is used to provide the reference power (thus defines inductor current i_L) of the DC-DC converter local controller. A typical control diagram of a DC-DC converter is shown in Figure 5.4. PWM signals are generated to control switches S1 and S2. The switching behaviour of these switches will cause the DC-side current harmonics.

The conventional PWM of the buck-boost DC-DC converter is shown in Figure 5.5. It can be seen that switching signals are generated by comparing the duty cycle reference and carrier signal with a triangle waveform. The period of a carrier signal is defined as $T_{con}^{[b]}$. The average of DC-side current $i_{dc}^{[b]}$ and its contained harmonics are dependent on the power reference (and thus i_L). Similar to AC-DC converters, the $i_{dc}^{[b]}$ harmonics phase angle can be controlled by shifting the phase angle of the carrier signal. However, since the power reference is given by the upper-level controller (at the secondary level) and dependent on load requirements within the hybrid power generation centre, the power reference (and thus i_L^* value) is thus an input value and not be able to be determined by a local controller of a DC-DC converter. Thus, for $i_{dc}^{[b]}$ harmonics, although their phase angles are controllable, this is not the case for their magnitudes for a local controller. This makes the conventional modulation technique with phase-shifting of carrier signals not that effective to cancel harmonics from AC-DC converters, as the $i_{dc}^{[b]}$ harmonic magnitudes is not controllable in this case. Thus, a new modulation technique is required and will be discussed.

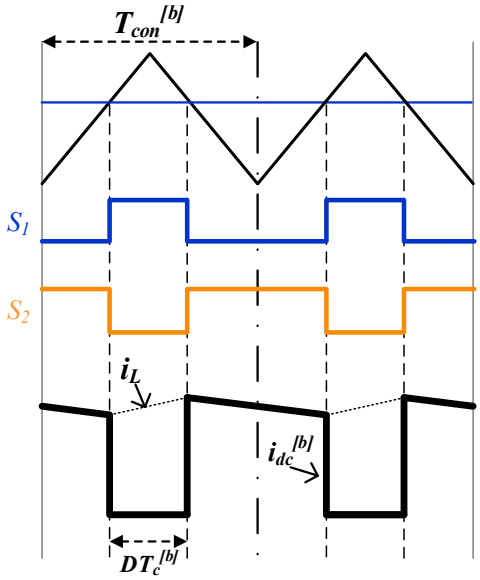


Figure 5.5: Conventional PWM strategy.

5.3.2 Equal-Gate-Width PWM

In this section, a new modulation scheme will be developed to enable an active control of the dc-side current $i_{dc}^{[b]}$ harmonic magnitudes as well as their phase angles. The new PWM method is named as equal-gate-width (EGW) PWM method and is shown in Figure 5.6. There, one cycle time of a carrier signal is defined as $T_c^{[b]}$. The switch S_1 turns on twice within one cycle $T_c^{[b]}$ and each time is on for a period of $DT_c^{[b]}/2$. Here D is the duty cycle of the gate signal from the PI controller output. These two turn-on periods are symmetrical from the half cycle $T_c^{[b]}/2$. The offset referred to its centre is defined as $\Delta D \cdot T_c^{[b]}$. Since S_1 switches on twice for one carrier signal cycle, for the same switching frequency, the carrier signal of proposed EGW will be with a doubled period compared with that of conventional PWM, i.e., $T_c^{[b]} = 2T_{con}^{[b]}$. Using the proposed ESW technique, the first order harmonics will be located at $1/T_c^{[b]}$ frequency.

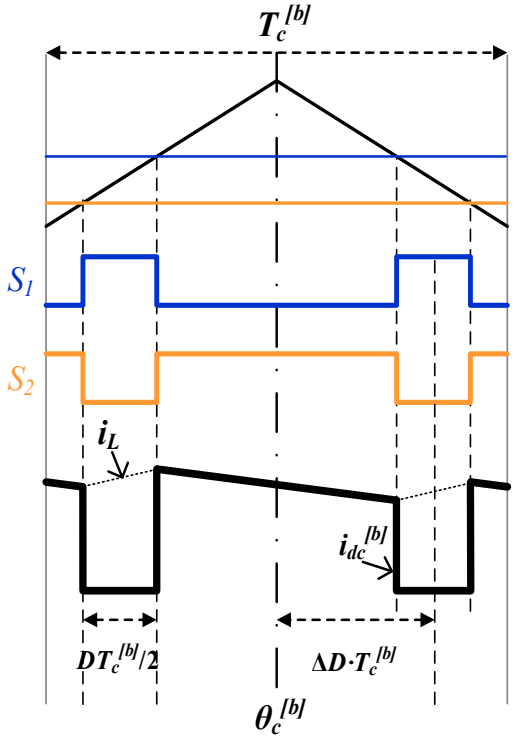


Figure 5.6: Equal-Gate-Width (EGW) PWM

To simplify the analysis, the inductor current is assumed to be constant as I_L, and the converter works under continuous current modes. In this case, the battery model will be simplified as a controllable DC current source. Then, the current flowing into the dc-bus capacitor, $i_{dc}^{[b]}$, can be expressed as

$$i_{dc}^{[b]} = \begin{cases} I_L, & -\dfrac{T^{[b]}}{2} < t < -\dfrac{(4\Delta D + D)T^{[b]}}{4} \\ I_L, & -\dfrac{(4\Delta D - D)T^{[b]}}{4} < t < \dfrac{(4\Delta D - D)T^{[b]}}{4} \\ I_L, & \dfrac{(4\Delta D + D)T^{[b]}}{4} < t < \dfrac{T^{[b]}}{2} \\ 0, & \text{else} \end{cases} \tag{5.27}$$

Considering its symmetry and using Fourier expansion, the current $i_{dc}^{[b]}$ can be expressed as

$$i_{dc}^{[b]} = A_0 + \sum_{k=1}^{\infty} A_k \cos\left(2k\pi f_c^{[b]} t + k\theta_c^{[b]}\right) \tag{5.28}$$

where

$$f_c^{[b]} = \frac{1}{T_c^{[b]}} \tag{5.29}$$

From (5.28), it can be seen that the phase angle of current $i_{dc}^{[b]}$ harmonics are related to the carrier signal phase angle θ_c. The Fourier coefficients A_k in (5.28) are derived as

$$A_0 = I_L\left(1 - D\right) \tag{5.30}$$

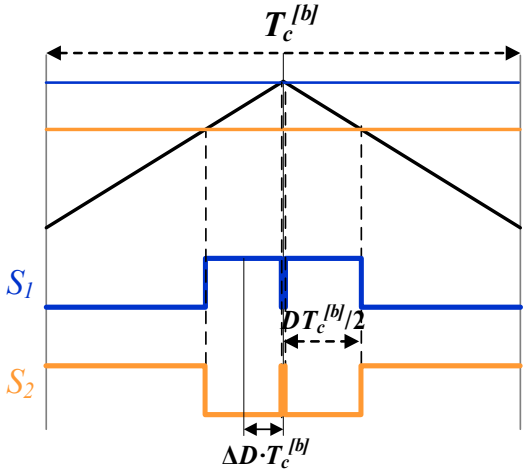
$$\begin{aligned} A_{k(k\neq 0)} &= 2f_c^{[b]} \int_{-\frac{1}{2f_c^{[b]}}}^{\frac{1}{2f_c^{[b]}}} i_{dc}^{[b]}(t) \cos\left(2k\pi f_c^{[b]} t\right) dt \\ &= \frac{4I_L}{k\pi} \sin\left(\frac{k\pi D}{2}\right) \cos 2k\pi \Delta D \end{aligned} \tag{5.31}$$

From (5.31), it can be noticed that the magnitudes of harmonic components A_k can be controlled with ΔD. This is very useful to find, as adjusting this variable will only change the location of the turn-on pulse of S_1 but have no impact on the duty cycle D from the controller. Combining with (5.28), we can come to a conclusion that the proposed EGW PWM scheme can achieve active control of magnitudes and phase angle of current $i_{dc}^{[b]}$ harmonics.

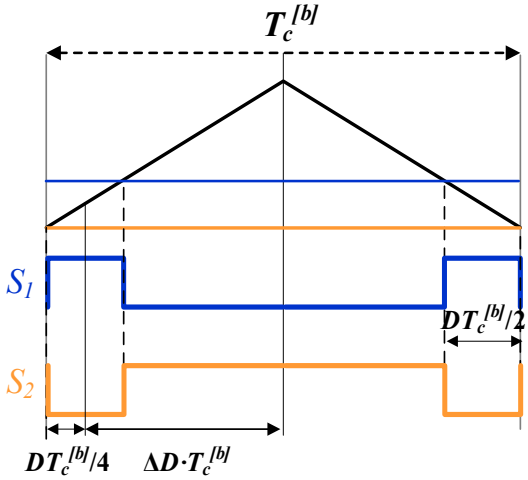
The adjustable range of ΔD is limited by D and defined as

$$\frac{D}{4} < \Delta D < \frac{1}{2} - \frac{D}{4} \tag{5.32}$$

This limitation is essentially considering the fact that if ΔD exceeds the range defined in (5.32), the two gate signal pulses of S_1 in Figure 5.6 will overlap each other or go beyond $T_c^{[b]}$, as shown in Figure 5.7.



(a)



(b)

Figure 5.7: EGW operation when the two gate signal pulses of S_1 are going to overlap each other. a) $\Delta D = D/4$. b) $\Delta D = 1/2 - D/4$.

Considering DC-DC converter works under a steady state, the duty cycle of the DC-DC converter is given as

$$D = 1 - \frac{V_b}{V_{dc}} \tag{5.33}$$

Substituting (5.33) to (5.32) gives

$$\frac{V_{dc}-V_b}{4V_{dc}} < \Delta D < \frac{V_{dc}+V_b}{4V_{dc}} \tag{5.34}$$

Figure 5.8 shows the amplitudes of the first and second order of switching harmonics of $i_{dc}^{[b]}$ (A_1 and A_2) for a DC-DC converter with the proposed EGW PWM scheme. There, we assumed the battery voltage is 200V with the dc bus voltage to be 270V. The current I_L is set to be at 50A. Harmonics higher than the second order are not considered here due to their low impact on DC-link capacitors. From Figure 5.8, it can be seen that magnitudes of the first and second carrier harmonic vary when ΔD changes. Since the harmonic component phase angle can be controlled by changing the carrier signal angle θ_c, we can conclude that the proposed EGW has potential to cancel harmonics from AC-DC converters on the DC bus. This will be discussed in more details in the next section.

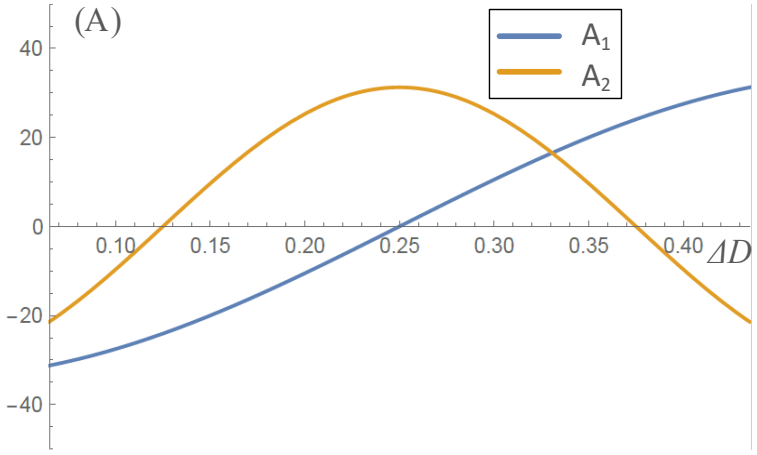


Figure 5.8: Magnitudes of the first and second carrier harmonic with ΔD changing ($f_c^{[b]}$ and $2f_c^{[b]}$).

5.4 Proposed Harmonics Cancellation Method

In this section, an enhanced harmonic suppression method will be proposed using harmonics generated from DC-DC converter to cancel some specific harmonics from AC-DC converters. We will focus on f_c-$3f_0$ harmonic component from AC-DC converter as this component is more significant

compared to ones in f_c+3f_0 and 2f_c as discussed in Section 5.2.2. Without losing generality, similar methods can be developed to suppress other components.

A hybrid generation centre with one AC/DC converter and one DC/DC converter is shown in Figure 5.9. Within such a system, a PMSG supplies power to an HVDC bus through an AC-DC converter. A high-voltage battery supplies power to HVDC bus (270V) via a DC-DC converter. The two converters share a common DC-link capacitor. The AC-DC converter and the DC-DC converter are controlled with their local primary controller. A system controller is used for high-level supervision (secondary) control. The system-level control is to define power sharing between PMSG and the battery by defining their power references ($I_{dc}^{[g]*}$ and I_L^*). The local controllers thus control converters of the PMSG and the battery to inject the required DC currents to the HVDC bus.

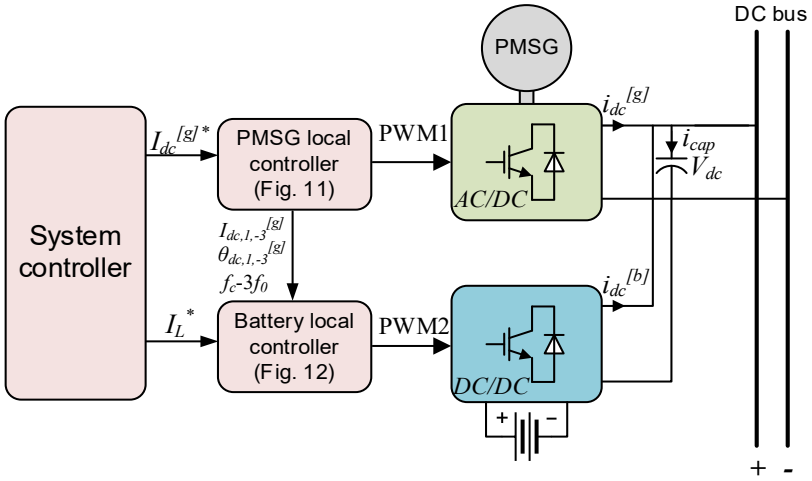


Figure 5.9: Control architecture of the hybrid generation system.

The local control diagram of PMSG is shown in Figure 5.9. Similar to previous chapters, a cascaded control structure has been used, with current control being the inner loop. A flux-weakening control is applied in the outer control loop. This is due to the fact that in MEA applications, PMSG is driven by the high-speed shaft of an aircraft engine. The stator output voltage $\sqrt{v_d^2 + v_q^2}$ is controlled by injecting a negative flux current component i_d. The output current

i_{dc} of the AC-DC converter is also controlled with its reference $i_{ref}^{[g]}$ given by the system-level controller. With measured currents i_d, i_q, voltage references v_d and v_q modulation index M, the information of harmonic component f_c-3f_0 can be derived, with its magnitude $I_{dc1,-3}^{[g]}$ and its phase angle $\theta_{dc1,-3}^{[g]}$ from (5.15) and (5.16) respectively. The fundamental frequency (f_0) can be obtained from a machine speed sensor. These features of f_c-3f_0 component, i.e., magnitude, frequency, and phase angle are then sent to the controller of the controller of the DC-DC converter.

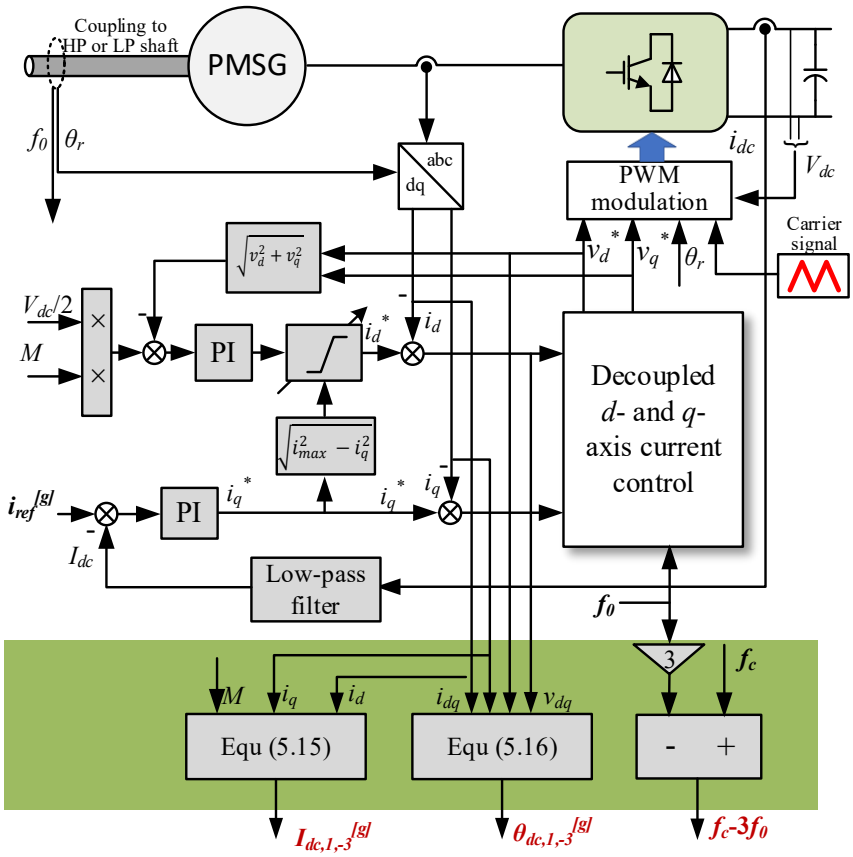


Figure 5.10: Control diagram of the PMSG system.

The cancellation scheme of the harmonic component of f_c-3f_0 from the AC-DC converter is essentially based on the fact that two sinusoidal currents of the same magnitude will cancel each other if they are 180° phase shift to each other. With this fact, we can use a DC-DC converter as an active harmonic injection source

to cancel the f_c-3f_0 harmonic component from an AC-DC converter. To achieve that, the frequency of the carrier signal ($f_c^{[b]}$) of the DC-DC converter should be set to f_c-3f_0 i.e.

$$f_c^{[b]} = f_c - 3f_0 \tag{5.35}$$

To achieve the phase angle difference of 180° between two harmonics, with (5.16), the phase angle of the EGW PWM carrier signal should be set as

$$\theta_c^{[b]} = \theta_{dc,1,-3}^{[g]} - \pi = \theta_c - 2\text{atan2}\left(v_q, v_d\right) - \text{atan2}\left(i_q, i_d\right) \tag{5.36}$$

where $\theta_c^{[b]}$ is the phase angle of carrier signal of DC-DC converter. Based on the expression in (5.36), the phase-shift angle of π is achieved between components on f_c-3f_0 from both the PMSG and battery.

Combining $I_{dc,1,-3}$ in (5.15) and A_1 in (5.31) will give the required harmonic amplitude of the first order harmonic ($A_1^* = I_{dc,1,-3}$) and thus ΔD in the DC-DC converter is derived as

$$\Delta D = \frac{\cos^{-1}\dfrac{A_1^*\pi}{4I_L \sin\left(\dfrac{k\pi D}{2}\right)}}{2\pi} \tag{5.37}$$

where A_1* is the required harmonic requirement which is limit to

$$A_{1max} = \frac{4\sin\dfrac{\pi D}{2}}{\pi} I_L \tag{5.38}$$

Therefore, the carrier signal frequency ($f_c^{[b]}$), magnitude (A_1), and the phase angle $\theta_c^{[b]}$ can be selected based on harmonic information sent from PMSG controller with (5.37) and (5.38) as shown in Figure 5.11.

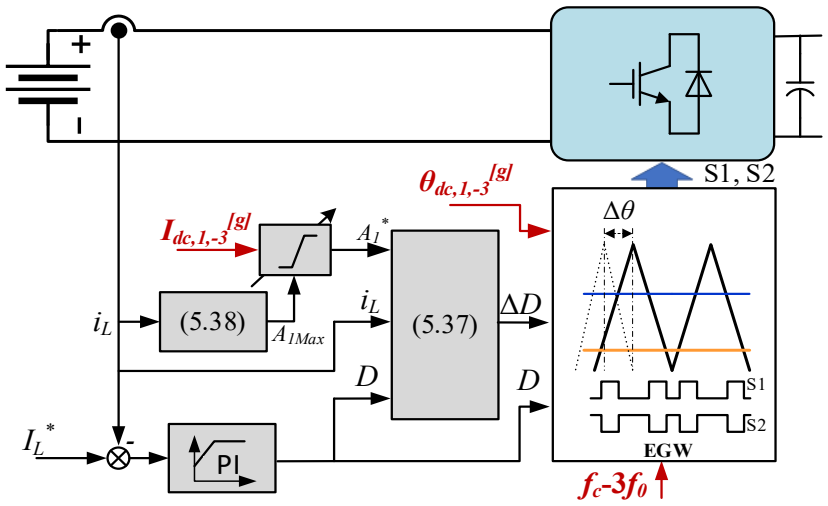


Figure 5.11: Control diagram of battery system.

It can be seen from (5.38) that with a higher inductor current I_L (positive or negative), the adjustable range of A_1 can be wider. Hence, the EGW PWM is more capable of eliminating harmonic when the DC-DC converter operates under higher power. The minimum I_L to fully eliminate $I_{dc,1,-3}$ from the AC-DC converter ($I_{L,full}$) can be derived from (5.38) as

$$I_{L,full} = \frac{\pi I_{dc,1,-3}}{4\sin\frac{\pi D}{2}} \tag{5.39}$$

Comparing to Figure 5.2a, this value shows a similar changing trend with $I_{dc,1,-3}$ when the output power of PMSG increases, as shown in Figure 5.12.

Meanwhile, when the DC-DC converter works under the charging mode, the inductor current (I_L) becomes a negative value. In this case, (5.37) and (5.38) are still applicable, and thus the proposed method is also effective when the DC-DC converter works under the charging mode.

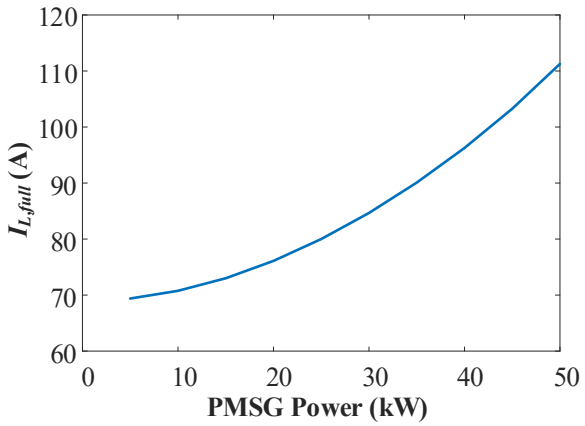


Figure 5.12: $I_{L,full}$ when the output power of PMSG varies.

5.5 PWM Compensation Technique

5.5.1 Impact of measured fundamental frequency Errors

In the previous section, we have pointed out that setting the carrier frequency $f_c^{[b]} = f_c\text{-}3f_0$ and $\theta_c^{[b]} = \theta_{dc,1,-3}^{[g]} + \pi$, the first sideband harmonic of $f_c\text{-}3f_0$ from an AC-DC converter can be suppressed using the first carrier harmonic component from a DC-DC converter. However, during implementation, setting $f_c^{[b]} = f_c\text{-}3f_0$ is not that straightforward. This is due to the fact that although the modulation frequency f_c for the AC-DC converter is set by the controller, the frequency f_0 is a measured value $\hat{f}_0$ and is normally derived from a PMSG speed resolver. Since the measured frequency $\hat{f}_0$ is subject to some degree of errors because of the resolution of the position sensor, it can be concluded that using this measured $\hat{f}_0$ can potentially result in discrepancies between $f_c^{[b]}$ and the desired value $f_c\text{-}3f_0$ (with $f_c^{[b]} = f_c\text{-}3\hat{f}_0$). This, in return, will undermine the performance of harmonic suppression since this error (which can be tiny) will be accumulated and resulted in significant difference between $\theta_c^{[b]}$ and $\theta_{dc,1,-3}^{[g]} + \pi$. As a result, the effectiveness of harmonic suppression cannot be achieved at all.

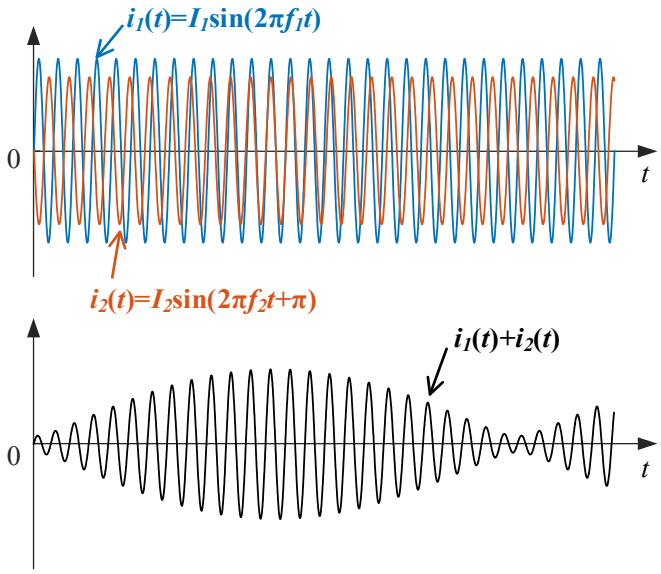


Figure 5.13: Sum up of two un-synchronised components.

Figure 5.13 illustrates a scenario of this case when $f_c^{[b]}$ and f_c-$3f_0$ are not equal due to measurement errors. There, two components, i.e., $i_1(t)$ and $i_2(t)$ are used to represent harmonic components of $f_c^{[b]}$ (assumed to be f_1) and f_c-$3f_0$ (assumed to be f_2) from a DC-DC and an AC-DC, respectively. Due to the measured error in f_0, the carrier frequency $f_c^{[b]}$ is set to $f_c - 3\hat{f}_0$ instead of f_c-$3f_0$. Assuming that f_1:f_2 ($f_c - 3\hat{f}_0$: $f_c - 3f_0$) = 0.96:1 and these two harmonic components have a phase difference of π initially. These two components counteract each other fully at the beginning. However, due to the discrepancy of the two frequencies, the phase difference between these two is actually fluctuating instead of being a constant value of π. Thus, the two components are essentially modulating each other rather than suppressing each other. To mitigate the impact of such f_0 measurement error and achieve an effective suppression in a consistent way, compensation of such error is essential. This will be discussed in the next section.

5.5.2 Applying compensation to avoid the accumulated error

As discussed in previous section, the measurement error of f_0 will lead to a situation that the phase angle difference of the targeted harmonics from the AC-DC converter and the DC-DC converter are fluctuating rather an of π phase shift. To mitigate the impact of this error, compensation should be applied before this error becomes significant. One way to mitigate such accumulated error is simply resetting the phase angles as shown in Figure 5.14. There, to avoid situation in Figure 5.13, compensation is applied when the accumulated error is not significant (π/6 in Figure 5.14). The compensation essentially is to reset the phase angle of $i_2(t)$ to be with a π phase difference again compared to that of $i_1(t)$. After each compensation, although the error between $i_1(t)$ and $i_2(t)$ will start to accumulate again, the error can be always kept within a tolerable range by taking compensation actions in every a few cycles.

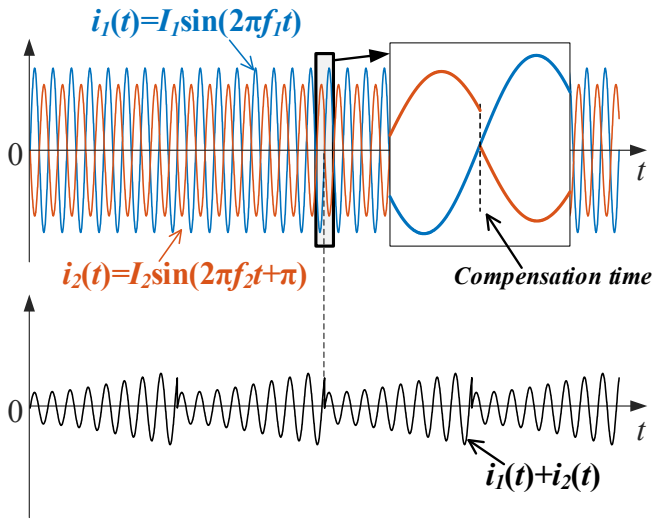


Figure 5.14: Compensation actions on accumulated errors.

The same concept shown in Figure 5.14 can be used to mitigate the errors of the measured frequency $\hat{f}_0$ when setting the frequency of PWM carrier signal within the DC-DC converter $f_c^{[b]}$ to be f_c-$3f_0$ (in reality it is f_c-$3\hat{f}_0$). One of the key implementation aspects of the compensation is to identify the time instant when to apply such compensation.

Considering the fact that f_0 varies according to the rotor speed of PMSG, the carrier frequency of the DC-DC converter (f_c-3f_0) is thus not fixed. On the other hand, the carrier signal of the AC-DC converter is a triangle waveform with a fixed frequency and phase angle. In that case, we can take the carrier signal of the AC-DC converter (of frequency f_c) as the reference signal. The carrier signal of the DC-DC converter (of frequency f_c-3$\hat{f}_0$) needs to be compensated every a few cycles to avoid accumulated error as it should be with a frequency of f_c-3f_0. One potential good choice is to select the compensation time instant to be when the PMSG rotor position is detected "Zero". It is a very logical selection as a fundamental cycle of the PMSG is a reasonable small amount of time and the zero-detection signal from rotor position is convenient to derive in practice.

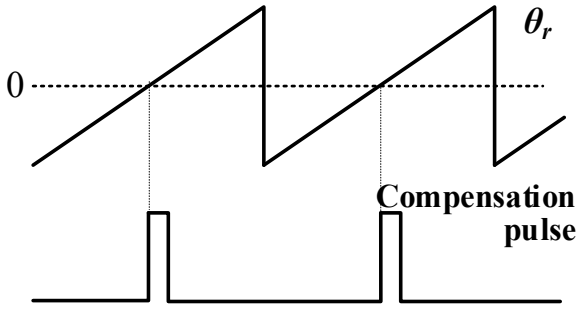


Figure 5.15: Compensation pulse generation.

As shown in Figure 5.15, a compensation pulse is generated when the rotor position θ_r hits zero. The controller of the AC-DC converter sends this pulse together with information for phase-shift angle calculation, i.e., i_{dq}, v_{dq}, M, θ_c, to the controller of the DC-DC converter, as shown in Figure 5.16.

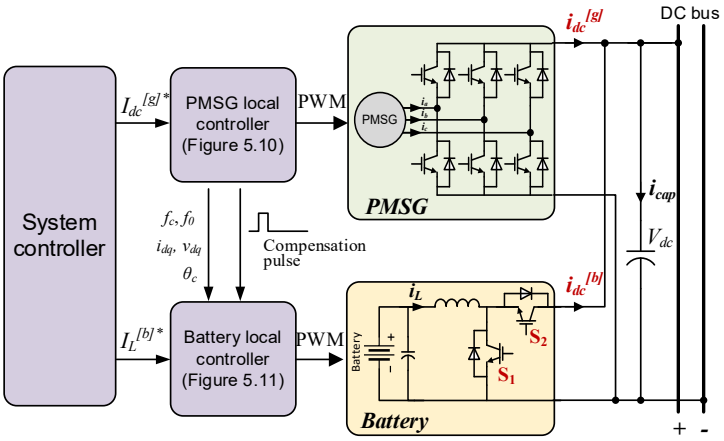


Figure 5.16: Control architecture of the hybrid generation system considering PWM compensation.

After the DC-DC controller receives the pulse, compensation will be applied immediately. At that time instant, the frequency of the DC-DC converter carrier signal will be refreshed to a new f_c-$3\hat{f}_0$ at that time instant. A time shift (ΔT) of the carrier signal will also be applied to the DC-DC converter microcontroller as shown in Figure 5.17. This time shift ΔT is given as

$$\Delta T = \frac{\theta_c^{[b]}}{2\pi\left(f_c - 3\hat{f}_0\right)} \tag{5.40}$$

In the digital controller we used during experiment (TI DSP TMS320F28379D), the carrier signal is generated from a time-base counter. The desired time shift ΔT is achieved by setting the proper counting direction and the initial counting value when the compensation pulse comes.

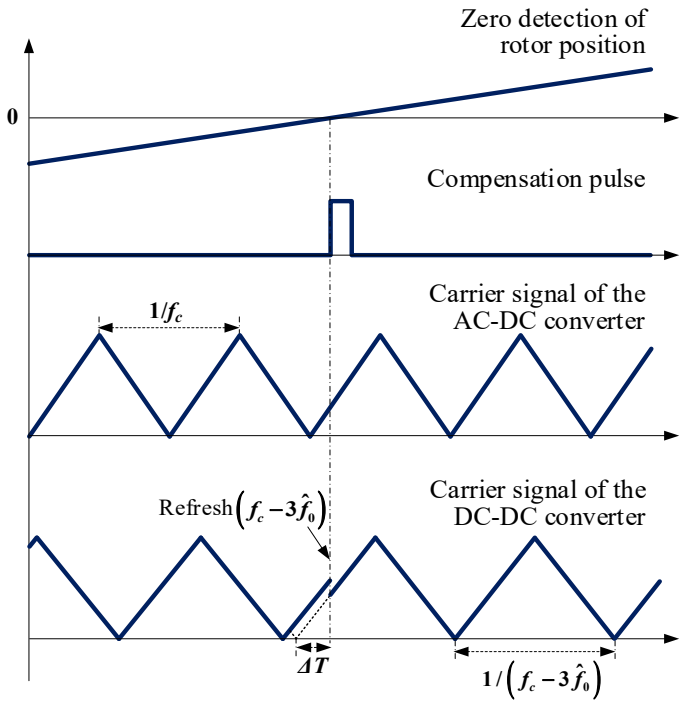


Figure 5.17: Compensation actions on carrier signals from PMSG and battery.

5.6 Simulation Studies

To validate the proposed method of suppressing f_c-3f_0 harmonic, simulation is implemented with Matlab/Simulink and PLECS. The simulation diagram is the same as Figure 5.16, and Table 5-1 lists the simulation parameters.

The rotor speed of the PMSG is 20 kRPM (1000 Hz). The output power of the AC-DC converter ($P^{[g]}$) and the DC-DC converter ($P^{[b]}$) are 20kW. Power sharing ratio is 1:1. The equal power sharing ratio is chosen for convenience to validate the proposed method. However, it is important to mention that in practice, the output powers of the two converters can be unequal according to the system requirements. The switching frequency of the AC-DC converter, f_c, is set at 16 kHz. To cancel the first side band harmonic from the AC-DC converter, the carrier frequency ($f_c^{[b]}$) is set at f_c-3f_0 (13 kHz) for the converter using the EGW PWM scheme. Thus, using the EGW PWM method, the switching frequency is 26kHz (within one carrier signal cycle, there will be two

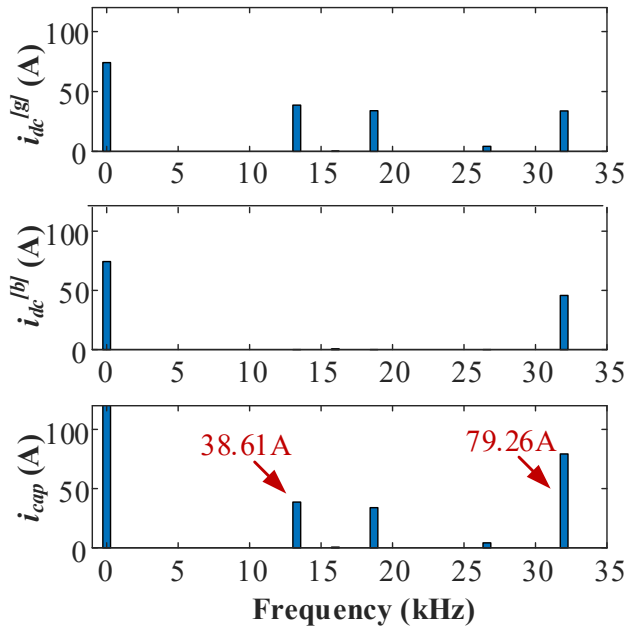
switching actions of S_1 or S_2). As mentioned before, conventionally, the carrier signal frequency for a DC-DC converter $f_{c1}^{[b]}$ is set to be doubled of that of the AC-DC converter, i.e. $2f_c$, i.e. 32 kHz [59]. Thus, we select 32kHz for the DC-DC converter with the conventional modulation technique for comparison studies. This will make it more reasonable to compare harmonics on the DC bus with and without active suppression.

Table 5-1: Simulation parameters for AC-DC and DC-DC converters

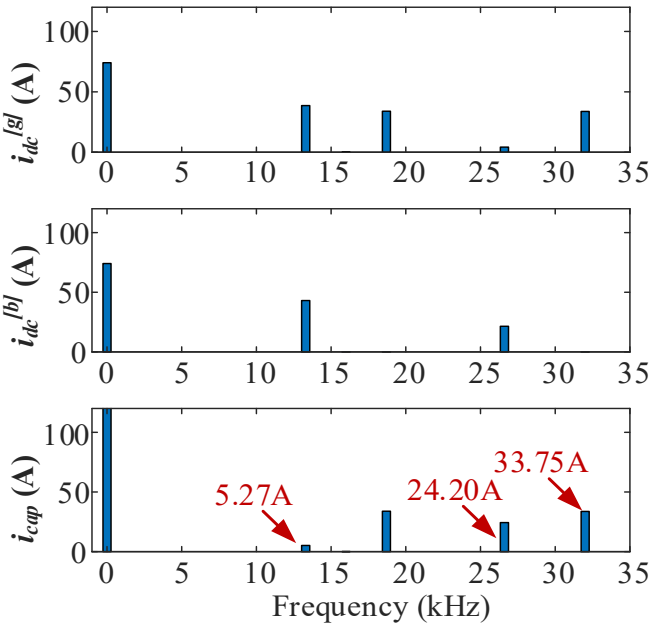
Category	Parameters	Values
PMSG	Rotor speed	20kRPM
	Switching frequency	16kHz
	Maximum modulation index	0.9
	Output power $P^{[g]}$	20kW
Battery	Battery voltage	200V
	Inductance	500μH
	Carrier frequency $f_{c1}^{[b]}$	32kHz (conventional)
	Carrier frequency $f_c^{[b]}$	13kHz (EGW)
	Output power $P^{[b]}$	20kW
	Inductor current I_L	100A
DC-link	DC-link capacitance	400μF
	DC bus voltage	270V

When the DC power system works without harmonic suppression scheme, Figure 5.18a shows the spectrums of the DC-bus currents from the AC-DC converter and the DC-DC converter ($i_{dc}^{[g]}$ and $i_{dc}^{[b]}$). The spectrum of the current flowing into the capacitor i_{cap} is also shown in this figure. The AC-DC converter generates harmonics on $f_c \pm 3f_0$ and $2f_c$, and the DC-DC converter generates

harmonics on f_c and $2f_c$. These components are summed up together on the DC-link capacitor current.



(a)



(b)

Figure 5.18: Current spectrums of $i_{dc}^{[g]}$, $i_{dc}^{[b]}$, and i_{cap}. When $P^{[g]}=P^{[b]}$=20kW. a) No optimisation, b) With the EGW PWM operation.

To suppress the f_c-3f_0 harmonic, the EGW PWM is implemented on the DC-DC converter, as shown in Figure 5.18b. The carrier frequency of EGW PWM is set as f_c-3f_0, i.e., 13 kHz. Comparing with Figure 5.18b, the harmonic in the frequency of f_c-3f_0 is suppressed from 38.61A to 5.27A (86.2% reduction). It is also interesting to notice the change of the second carrier harmonics of i_{cap}. With the proposed scheme, there are two components on the second band, i.e. 2f_c and 2f_c-6f_0. The 2f_c is from the AC-DC converter, the 2f_c-6f_0 component is from the DC-DC converter. This does not mean that the proposed scheme will generate more harmonics at the second carrier frequency level. Actually, without using the harmonic suppression scheme, both the AC-DC and the DC-DC converters will generate 2f_c components and these two components will add on each other at 2f_c in the spectrum.

To further illustrate the mechanism of the EGW PWM, the waveform of $i_{dc}^{[g]}$, $i_{dc}^{[b]}$, and i_{cap} are given in Figure 5.19. In Figure 5.19, the carrier frequency of the EGW PWM is adjusted as 13kHz (f_c-3f_0), ΔD is 0.153. The current pulses on $i_{dc}^{[b]}$counteract with $i_{dc}^{[b]}$, and then a harmonic suppression on i_{cap} can be achieved.

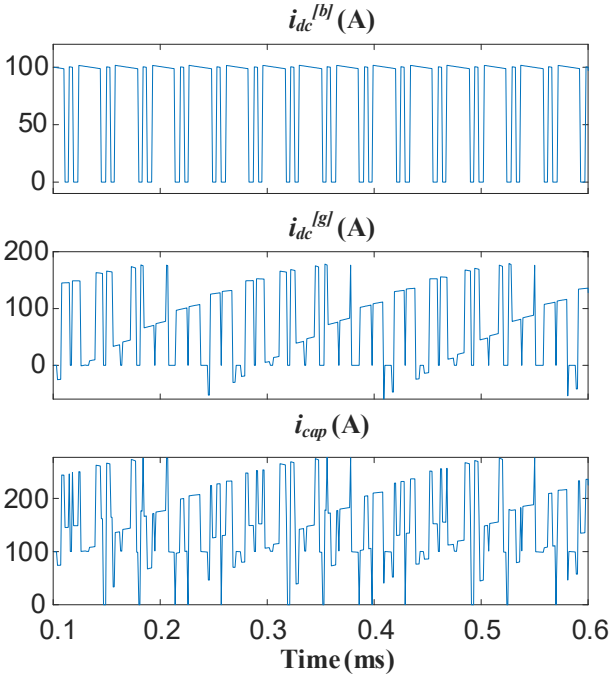


Figure 5.19: Simulation results of EGW PWM operation.

5.7 Chapter Summary

This chapter proposed a new EGW modulation scheme for DC-DC converters which enables active damping of harmonics generated from AC-DC converters. This chapter focuses on f_c-3f_0 harmonic cancellation, but similar methods can be used to suppress other components. An enhanced PWM synchronisation method is also proposed to handle the challenge of non-integer multiple relation between two carrier frequencies. Simulation results verify the validity of the proposed harmonic models and suppression method. The proposed work is extremely useful to improve power electronic dominated DC grid and can achieve improved power quality with no extra cost.

Chapter 6

Harmonic Cancellation of Both The First Sideband and The Second carrier harmonics within A Dual-Channel Power Generation System

6.1 Introduction

In a typical dual-generation power system, two PMSGs and one ESS supply the DC bus through their converters, as shown in Figure 6.1. The previous chapters have discussed the possibility of suppressing DC-link harmonics when two AC-DC converters operate (Chapter 3 and 4) and one AC-DC converter and one DC-DC converter operate (Chapter 5). However, those methods only focus on one specific frequency, i.e., Chapter 3 for $2f_c$ component and Chapter 5 for f_c-$3f_0$ component.

This chapter is to discuss the potential of combining the phase-shift strategy proposed in Chapter 3 and the EGW PWM proposed in Chapter 5 altogether to suppress the both the second order and first sideband order harmonics at the same time.

The chapter is organised in the following manner. Section 6.2 presents the harmonic suppression method. Section 6.3 presents the simulation results. Section 6.4 concludes this chapter.

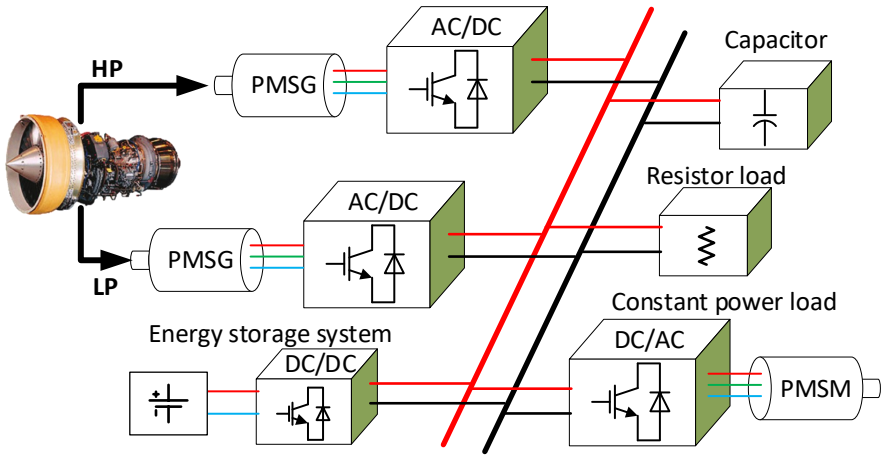


Figure 6.1: Typical dual-generation power system

6.2 Proposed Harmonics Cancellation Scheme

The system diagram has been shown in Figure 6.1. Two PMSGs are driven by the high-pressure and low-pressure shafts of the engine, respectively. An energy storage system (with battery) is also integrated. These three sources share a common DC-bus and supply the power to the whole electric system together. Local controllers for the PMSGs and the battery are applied to control the PMSGs and the battery system, as shown in Figure 6.2.

As discussed in Chapter 3, the second carrier harmonics ($2f_c$) on the DC-link can be suppressed with a 90-degree phase shift between the two AC-DC converters. Therefore, in the system shown in Figure 6.2, there is no change on the PMSG local controllers. Moreover, the second carrier harmonics from DC side can be totally cancelled if the power sharing ratio between the two AC-DC converters is 1:1, as discussed in Chapter 3.

The difference is mainly on the controller of the ESS. There are two pairs of first side-band harmonics on the DC-link, which come from the AC-DC converters of PMSG1 and PMSG2. The frequencies of them are $f_c \pm 3f_0^{[g1]}$ and $f_c \pm 3f_0^{[g2]}$. $f_0^{[g1]}$ and $f_0^{[g2]}$ are the fundamental frequencies of the PMSG1 and PMSG2, respectively.

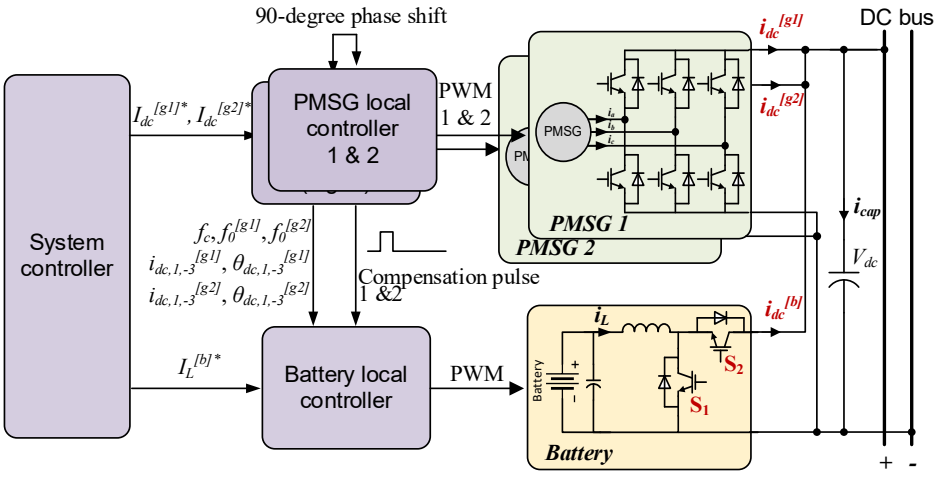


Figure 6.2: Control diagram of the dual-generator system together with a battery system.

To fully use the effectiveness of the EGW PWM, the DC-DC converter should suppress the most significant component. Therefore, there is a component selection block in the local controller of the DC-DC converter, as shown in Figure 6.3.

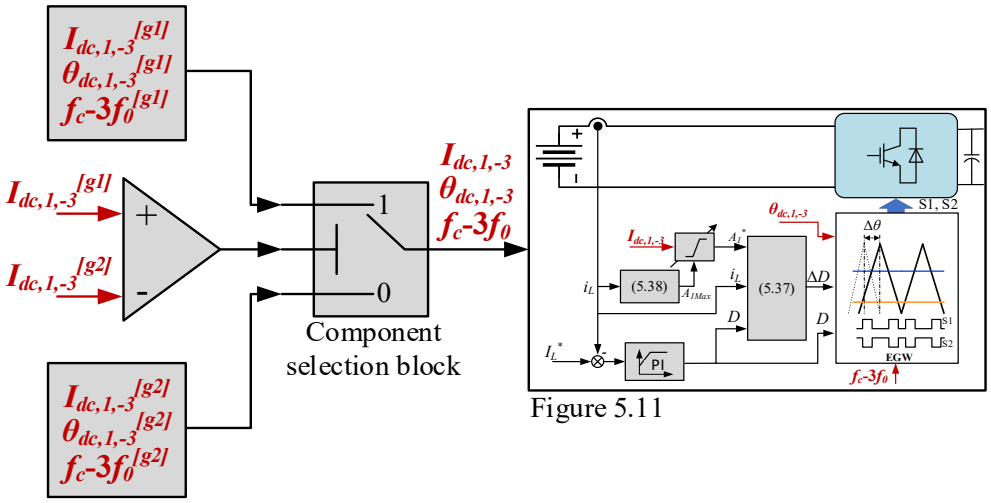


Figure 5.11

Figure 6.3: Modified local controller of the DC-DC converter.

The magnitudes of the f_c-3f_0 harmonics from the PMSG1 and PMSG2 are compared. If $I_{dc,1,-3}^{[g1]} > I_{dc,1,-3}^{[g2]}$, the harmonic information from the PMSG1

should be sent to the controller of the DC-DC converter. On contrary, if $I_{dc,1,-3}^{[g1]}<I_{dc,1,-3}^{[g2]}$, the harmonic information from the PMSG2 should be sent. The harmonic information sent to the controller is selected based on the expressions in (6.1) to (6.3), which include magnitude, phase angle, and frequency.

$$I_{dc,1,-3}=\begin{cases} I_{dc,1,-3}^{[g1]} & I_{dc,1,-3}^{[g1]} \geq I_{dc,1,-3}^{[g2]} \\ I_{dc,1,-3}^{[g2]} & I_{dc,1,-3}^{[g1]} < I_{dc,1,-3}^{[g2]} \end{cases} \tag{6.1}$$

$$\theta_{dc,1,-3}=\begin{cases} \theta_{dc,1,-3}^{[g1]} & I_{dc,1,-3}^{[g1]} \geq I_{dc,1,-3}^{[g2]} \\ \theta_{dc,1,-3}^{[g2]} & I_{dc,1,-3}^{[g1]} < I_{dc,1,-3}^{[g2]} \end{cases} \tag{6.2}$$

$$f_c-3f_c=\begin{cases} f_c-3f_0^{[g1]} & I_{dc,1,-3}^{[g1]} \geq I_{dc,1,-3}^{[g2]} \\ f_c-3f_0^{[g2]} & I_{dc,1,-3}^{[g1]} < I_{dc,1,-3}^{[g2]} \end{cases} \tag{6.3}$$

Then the EGW PWM block will operate accordingly to suppress the corresponding component.

6.3 Simulation Study

To validate the proposed method in Section 6.2, simulation is implemented with Matlab/Simulink and PLECS. The simulation diagram is the same as Figure 6.2, and Table 6-1 lists the simulation parameters.

The rotor speeds of the two PMSGs are 20 kRPM (1000 Hz) and 15kRPM (750 Hz). The output power of the two AC-DC converters ($P^{[g1]}$ and $P^{[g2]}$) and the DC-DC converter ($P^{[b]}$) are all 20kW, and thus power sharing ratio among the three sources is 1:1:1. In practice, the power sharing ratio could be unequal depending on the operation status of the dual-generator DC power system. The switching frequency of the AC-DC converters, f_c, is set at 32kHz. In practice, such a high switching frequency can be achieved by SiC devices. With the proposed method, the EGW PWM on the DC-DC converter is to suppress the first sideband harmonic from PMSG1, and thus the carrier frequency ($f_c^{[b]}$) of the EGW PMW is set at f_c-$3f_0^{[g1]}$ (29 kHz) for the converter using the EGW

PWM scheme. Thus, using the EGW PWM method, the switching frequency is 58kHz (within one carrier signal cycle, there will be two switching actions of S_1 or S_2). As mentioned before, conventionally, the carrier signal frequency for a DC-DC converter $f_{c1}^{[b]}$ is set to be doubled of that of the AC-DC converter, i.e. $2f_c$, i.e. 64 kHz [59]. Thus, we select 64kHz for the DC-DC converter with the conventional modulation technique for comparison studies. This will make it more reasonable to compare harmonics on the DC bus with and without active suppression.

Table 6-1: Simulation parameters for AC-DC and DC-DC converters

Category	Parameters	Values
PMSGs	Rotor speed	20kRPM and 15kRPM
	Switching frequency	32kHz
	Maximum modulation index	0.9
Battery	Battery voltage	200V
	Inductance	500μH
	Carrier frequency $f_{c1}^{[b]}$	64kHz (conventional)
	Carrier frequency $f_c^{[b]}$	29kHz (EGW)
DC-link	DC-link capacitance	400μF
	DC bus voltage	270V

The two AC-DC converters and the DC-DC converter generate currents on the DC-link ($i_{dc}^{[g1]}$, $i_{dc}^{[g2]}$ and $i_{dc}^{[b]}$), as shown in Figure 6.4. The capacitor filters out the high frequency ripple, and the capacitor current (i_{cap}) reflects the summed ripple of the three currents. With no harmonic suppression scheme, as shown in Figure 6.4a, the ripple on i_{cap} shows a significant fluctuation, and the maximum fluctuation is about 350A.

With the proposed method, as shown in Figure 6.4b, a 90-degree phase shift is applied on the AC-DC converter of PMSG2. $i_{dc}^{[g2]}$ also shows time difference with that in Figure 6.4a. According to the discussion in Chapter 3, the $2f_c$ components in i_{cap} can be suppressed.

Meanwhile, the EGW PWM is applied on the DC-DC converter. The switching frequency is reduced compared to that in Figure 6.4a, and $i_{dc}^{[b]}$ shows a symmetric waveform in each carrier cycle (29kHz, 0.034ms). According to the discussion in Chapter 5, the f_c-$3f_0^{[g1]}$ components in i_{cap} can be suppressed. Comparing Figure 6.4b to Figure 6.4a, a significant suppression of ripple can be observed on i_{cap}.

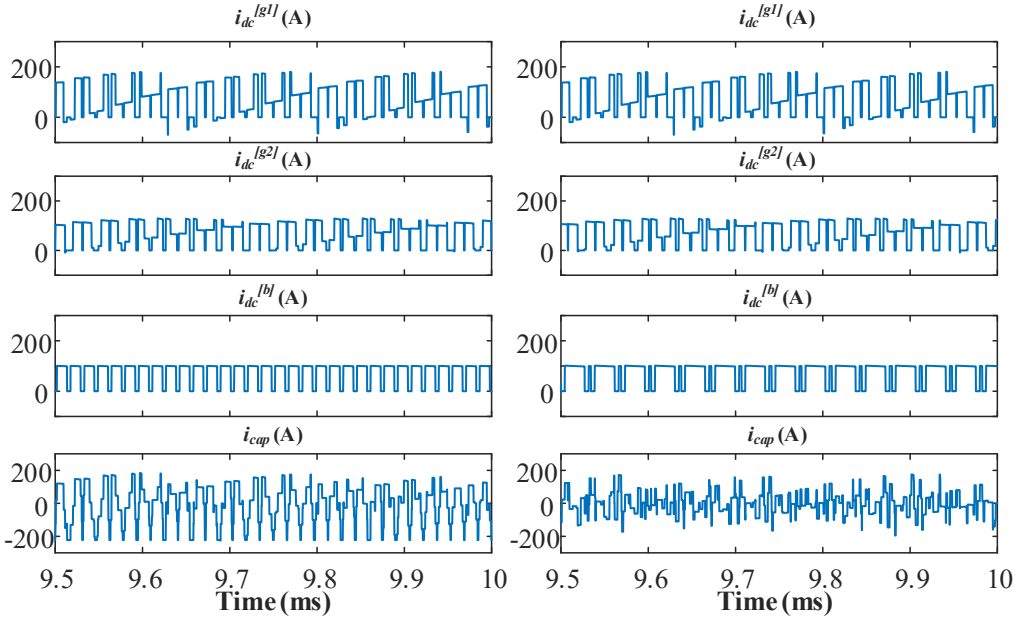


Figure 6.4: Simulation results of $i_{dc}^{[g1]}$, $i_{dc}^{[g2]}$, $i_{dc}^{[b]}$, i_{cap}. a) Without suppression. b) With suppression.

Comparing to the current waveforms, the FFT results can more clearly illustrate the suppression effect of the proposed method in frequency domain, as shown in Figure 6.5a and b.

The AC-DC converters generate harmonics on $f_c \pm 3f_0^{[g1]}$, $f_c \pm 3f_0^{[g2]}$ and $2f_c$, and the DC-DC converter generates harmonics on f_c and $2f_c$. Without harmonic

suppression scheme, these components are summed up together on the DC-link capacitor current (i_{cap}), as shown in Figure 6.5a.

To suppress the first sideband harmonic from the AC-DC converters, the EGW PWM is implemented on the DC-DC converter, as shown in Figure 6.5b. The AC-DC converter 1 generates a component with the magnitude of 39.6A in the frequency of f_c-3$f_0^{[g1]}$. Meanwhile, the AC-DC converter 2 generates a component with the magnitude of 28.0A in the frequency of f_c-3$f_0^{[g2]}$. Because 39.6A>28.0A, the EGW PWM of the DC-DC converter tends to suppress the f_c-3$f_0^{[g1]}$ component, as shown in Figure 6.3. The carrier frequency of EGW PWM is set as f_c-3$f_0^{[g1]}$, i.e., 29 kHz. Comparing Figure 6.5b with Figure 6.5a, the harmonic in the frequency of f_c-3$f_0^{[g1]}$ is suppressed from 39.6A to 3.8A (96.4% reduction).

Furthermore, the proposed method also applies a 90-degree phase shift on the AC-DC converter of PMSG2. The 2f_c components from the two AC-DC converters will counteract each other on the DC-link. The component in the frequency of 2f_c is suppressed from 115.0A to 2.0A (98.3% reduction) when comparing Figure 6.5b to Figure 6.5a. Such an almost 100% suppression is because of the proportional relationship between the 2f_c harmonic and the output power, which has been proved in Section 3.2. When the two sources generate a same power, magnitudes of the second carrier harmonics from the two converters are almost same. With a nearly 180° (2 × 90°) phase difference between the two components, the summed component can be suppressed effectively.

It is also interesting to notice the change on the second carrier harmonics of i_{cap}. With the proposed scheme, there are two components on the second carrier frequency band, i.e. 2f_c and 2f_c-6$f_0^{[g1]}$. The 2f_c-6$f_0^{[g1]}$ component is actually from the DC-DC converter. This does not mean that the proposed scheme will generate more harmonics at the second carrier frequency level. Actually, without using the harmonic compensation scheme, both the AC-DC and DC-

DC converters will generate $2f_c$ components and these two components will add on each other at $2f_c$ in the spectrum.

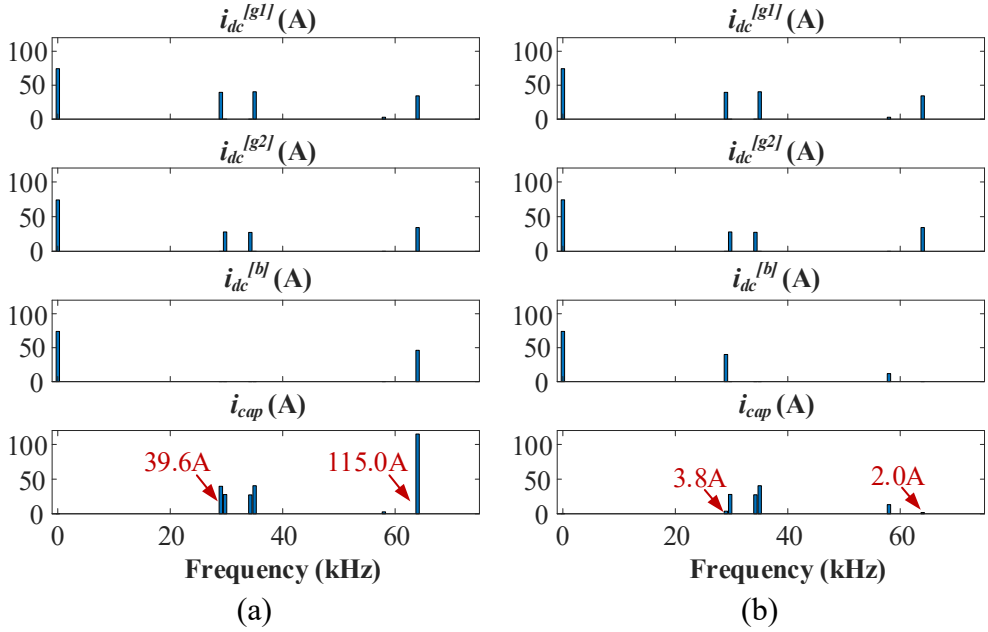


Figure 6.5: Simulation results of the spectrums. a) Without suppression. b) With suppression.

6.4 Chapter Summary

This chapter discusses the potential of combining the 90-degree phase shift strategy proposed in Chapter 3 and the EGW PWM method of DC-DC converters proposed in Chapter 5 altogether to suppress both the second and the first sideband harmonics on the DC-link.

The second carrier harmonics ($2f_c$) on the DC-link can be suppressed with a 90-degree phase shift between the two AC-DC converters. To suppress the most significant first sideband component (f_c-$3f_0^{[g1]}$ or f_c-$3f_0^{[g2]}$), a component selection block is created in the controller of the DC-DC converter. Then the EGW PWM method is applied on the DC-DC converter to suppress the selected components.

Finally, simulation was implemented to validate the effectiveness of the proposed harmonic cancellation method.

Chapter 7

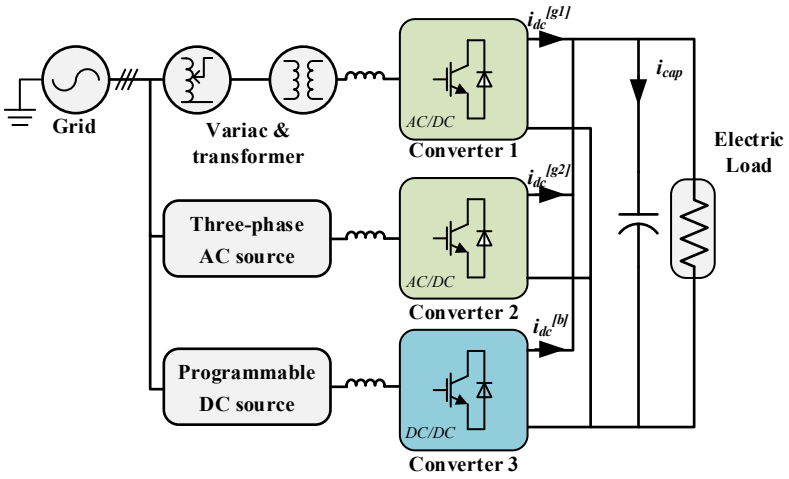
Experimental Rig Setup and Validation

After introducing the proposed harmonic suppression methods in the previous chapter, this chapter is to describe the test platform in the lab and present the experimental results to validate the proposed methods.

7.1 Experimental Setup

An overview of the experimental setup is shown in Figure 7.1a. In the experiment, due to the availability of high-speed test rigs within the University of Nottingham, one PMSG is replaced with a grid-connected variac and an isolating transformer. The isolating transformer has been used between the variac transformer and the AC-DC converter to avoid circulating currents among the converters. The variac transformer allows increasing the input voltages gradually to avoid any inrush currents. The other PMSG is replaced with a programmable AC source. It gives a variable frequency AC voltage to represent a variable rotor speed of PMSG. A programmable DC source is used to represent the battery with a controlled DC voltage.

The test rig in the lab is given in Figure 7.1b, and the detail view of the converters are given in Figure 7.1c. The three converters supply the DC-link altogether, and a capacitor bank is located on the DC-link to filter the current ripple from the converters.



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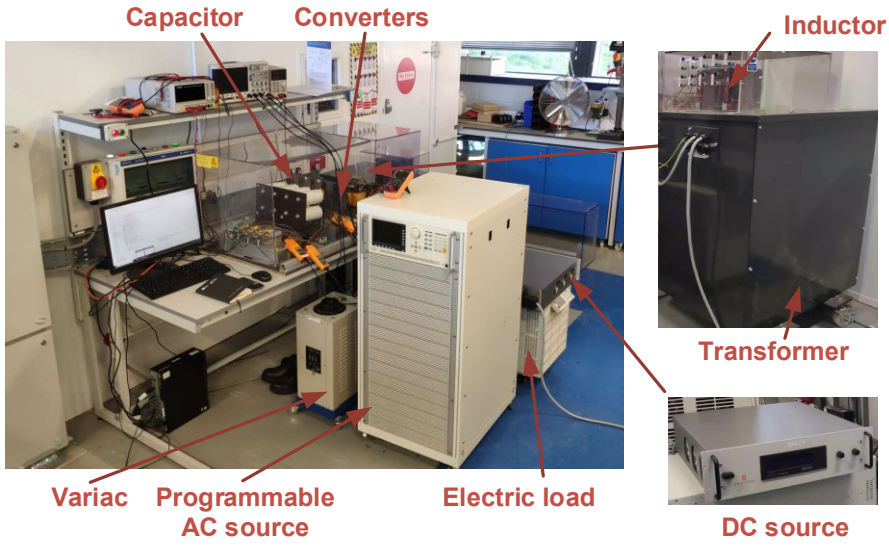
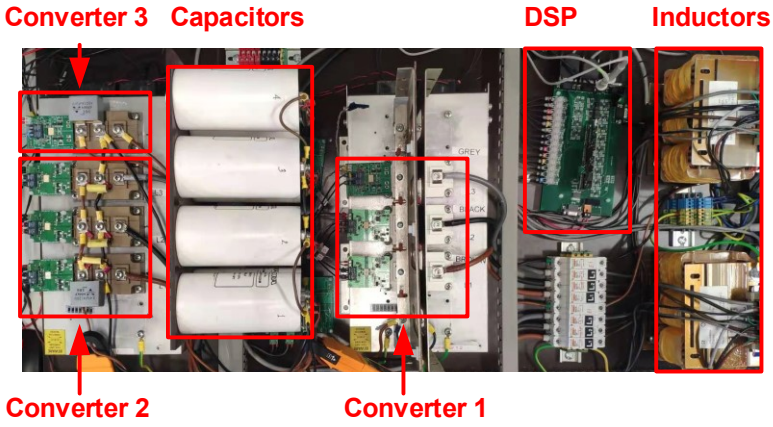


(b)



(c)

Figure 7.1: Experiment setup. a) Experiment diagram. b) Test rig. c) Converters and the controller.

7.1.1 Control Platform

For the control platform, the Texas Instruments F28379D controlCARD is used as shown in Figure 7.2. The controlCARD is based on DSP F28379D which is a 32-bit floating point dual-core microcontroller chip developed by Texas Instruments. Some useful peripherals, such as the ADC module and ePWM module, are embedded in the chip. An xds100v2 emulator is amounted in the controlCARD, which provides a convenient interface to the software Code Composer Studio Software (CCS) without any other additional hardware [107].

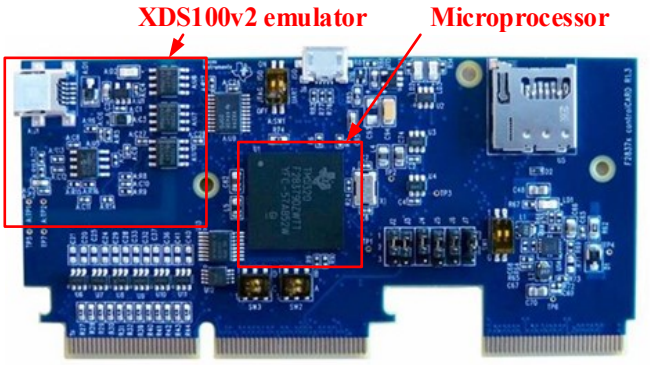


Figure 7.2: Texas Instruments F28379D controlCARD.

An interface board for conditioning sensor signals is developed to receive analogue signals from the voltage and current sensors, proceed these signals and send the conditioned signals to DSP ADC pins (15 channels). With the F28379CARD plugged in, the interface board also receives PWM signals from the DSP. These signals will be transferred to the optic signals and sent to the gate drivers of the power electronic device through fibre optic cables (14 channels), as shown in Figure 7.3.

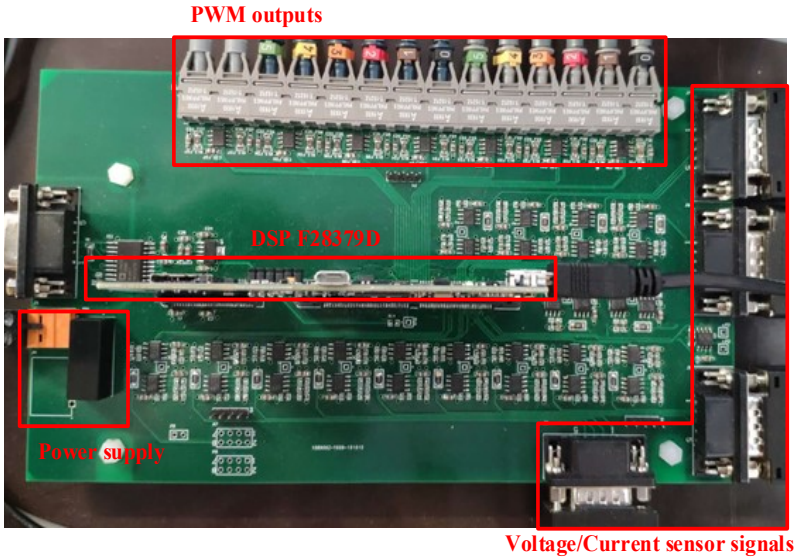
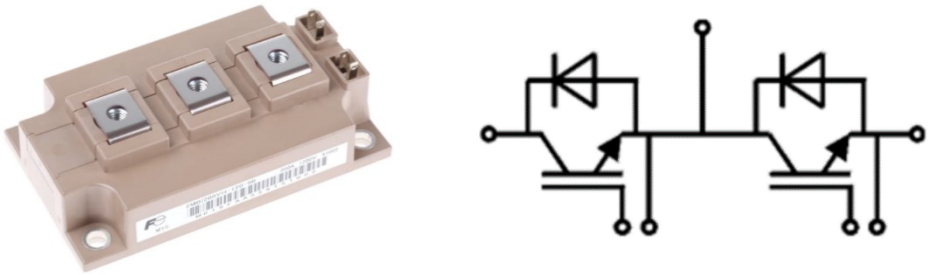


Figure 7.3: DSP Interface board.

7.1.2 Power Electronic Converters

The AC-DC converter used in this research is a typical two-level converter using the module Fuji Electrics 2MBI200VH-120-50 [109] as shown in Figure 7.4. The same power module is also sued for the buck-boost DC-DC converter.

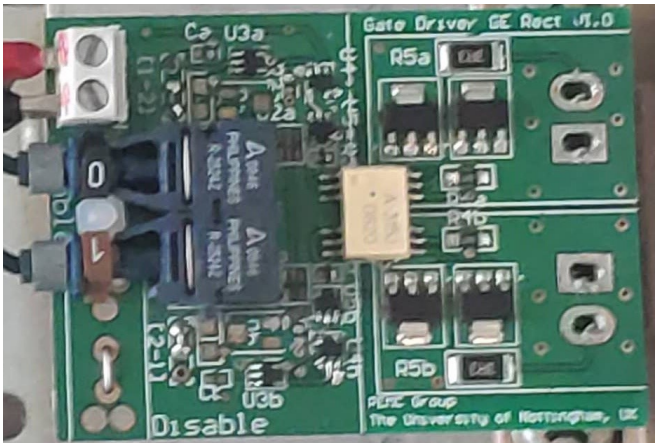


(a) (b)

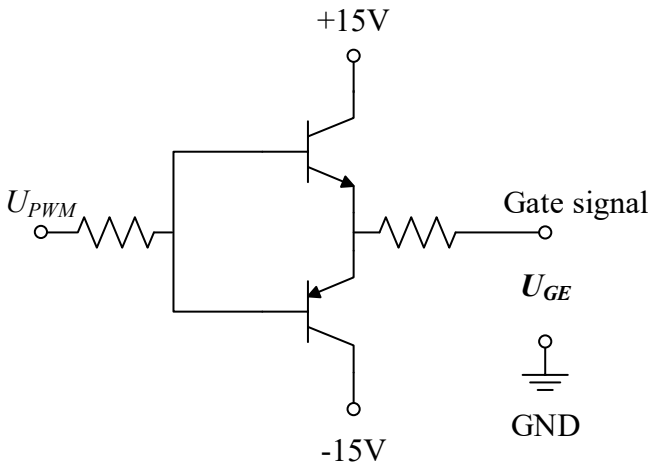
Figure 7.4: IGBT module (2MBI200VH-120-50). a) Prototype. b) Schematic.

To drive a semiconductor power device, the gate driver is an essential element. An IGBT driver board is developed within this project and shown in Figure 7.5a. This gate driver board will receive PWM signals from the control board through

optical fibres. Then, an opto-coupler chip (HCPL-315J) isolates the signals and converts the voltage level to ±15V. With push-pull circuits, as shown in Figure 7.5b, one driver board will drive one Fuji Electrics 2MBI200VH-120-50 power module.



(a)



(b)

Figure 7.5: Driver board. a) PCB board. b) Push-pull circuit.

7.1.3 Sensor Board

The sensor boards shown in Figure 7.6 and Figure 7.7 are used to measure the currents and the voltages of the three phases AC sources, battery, and the DC-link. The voltage transducer LEM LV 25-P [110] and current transducer LA 55-P [111] are used for the voltage and current measurements, respectively. The

measurement range of the voltage transducer LV25-P is 10V to 500V. The response time of 90% maximum measured voltage is 40μs. The measuring range of the current transducer LA 55-P is -70A to 70A, and the bandwidth is 20kHz at -1dB.

The output of the sensors are current signals to reduce noise on the signal cables. With sample resistors on the DSP interface board, as shown in Figure 7.3, the current signals are converted into voltage signals. The conditional circuits will further condition them to the required voltage range of the analog-to-digital converter (ADC) module on the DSP.

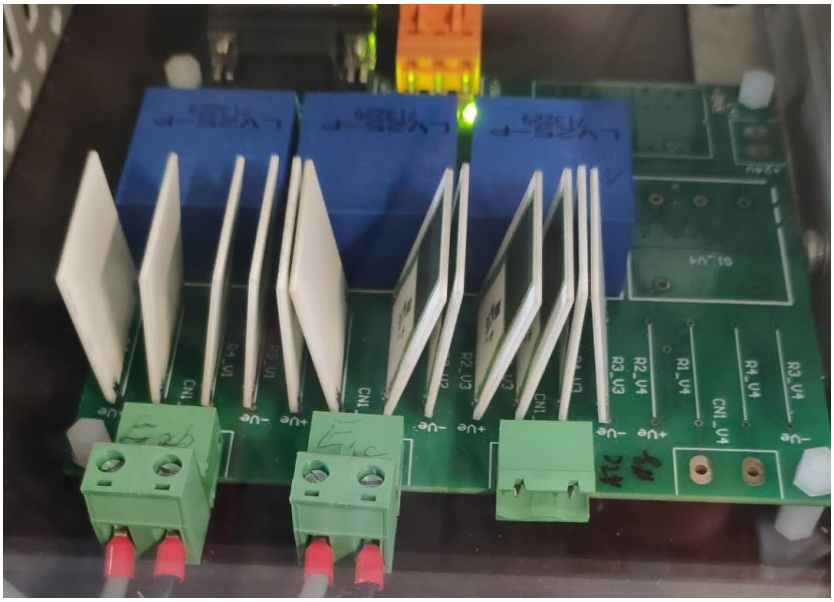


Figure 7.6: Voltage sensor board.

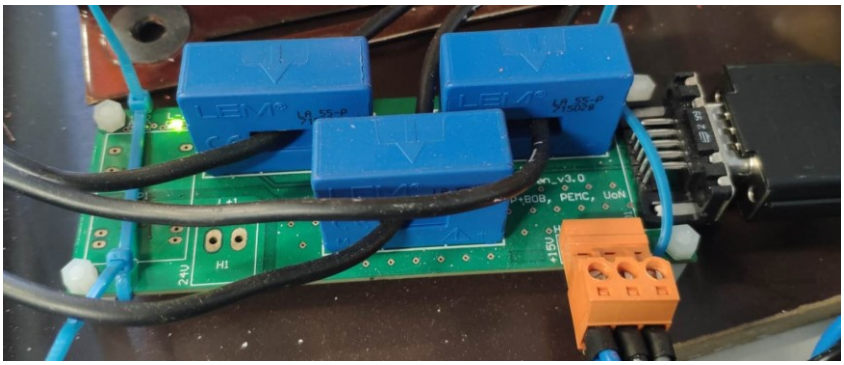


Figure 7.7: Current sensor board.

7.1.4 Power Load

A programmable DC electronic load (EL600VDC19800W) from the APM Technologies Company is used here to give an adjustable load, as shown in Figure 7.8. The maximum power of the electronic load is 20kW. By different settings, the electronic load can work under constant resistance or constant power load. In this thesis, we used constant resistance load mostly.

Figure 7.8: Programmable DC electronic load (EL600VDC19800W)

In the following sections, we will introduce the experimental test results using the developed test rig to validate our proposal harmonic cancellation scheme. Section 7.2 presents the power quality improvement when the two AC-DC converters work under carrier based SPWM operation, which refers Chapter 3. Sections 7.3 presents the power quality improvement when two AC-DC converters work under SVPWM operation, which refers Chapter 4. Section 7.4 deals with the power quality improvement when an energy storage system (with a DC-DC converter) is involved in the system, which refers Chapter 5 and Chapter 6.

7.2 Power Quality Improvement of Dual-Generator System under SPWM Operation

This section will deal with the experimental study of the power quality improvement when two AC/DC converters work under SPWM operation, as discussed in Chapter 3.

When only one AC-DC converter operates under SPWM modulation, the DC-side current is measured to validate the simplified harmonic models proposed in Section 3.2. Then, with a 90-degree phase shift between the two AC-DC converters and adjusting the modulation properly, a suppression of the second carrier harmonic can be achieved on the capacitor current. The experiment refers the suppression method proposed in Section 3.3.

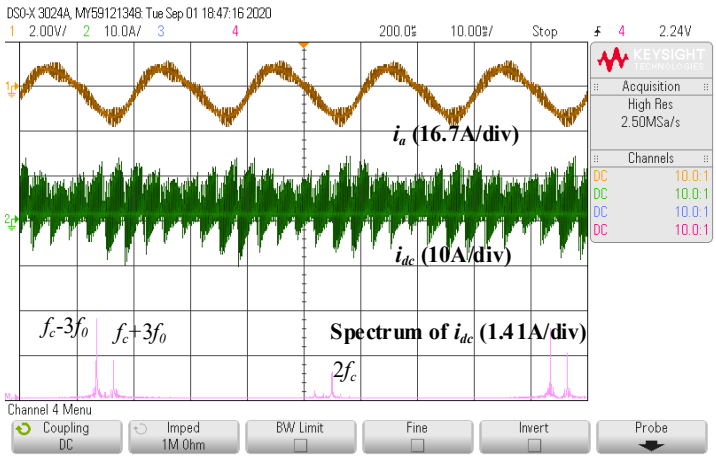
7.2.1 Single generator operation

Mathematical model of one single AC-DC converter under SPWM modulation needs to be properly validated before we implement the developed harmonic cancellation scheme for two AC-DC converters in Section 3.3. Within the DC-link setting at 270V, we increase the power demand from 400W to 2kW with a 400W step increase. The phase A currents (i_a), DC-bus currents (i_{dc}) are recorded. The spectrum of i_{dc} is also given to analyse the magnitude of each component. As discussed before, the permanent magnet machines is assumed to be working under flux-weakening control in MEA and thus the modulation index of an AC-DC converter is controlled within 0.9 and 0.95. The cases with modulation index (M) of 0.9 and 0.95 are tested and the experimental results are shown in Figure 7.9. Some detailed experimental parameters are shown in Table 7-1.

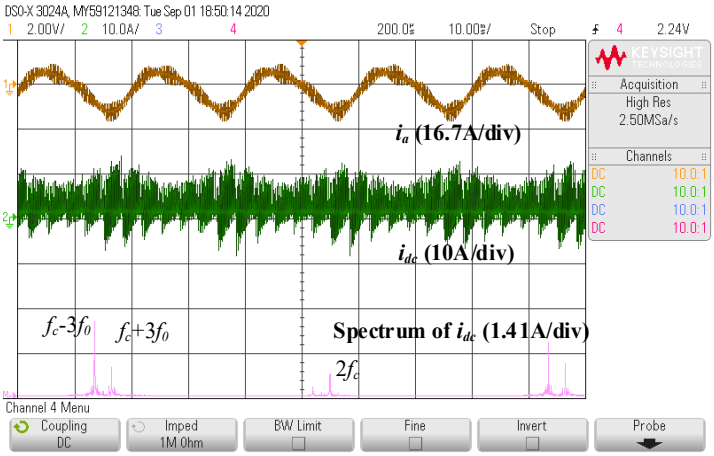
Table 7-1: Experiment parameters for single generator under SPWM operation.

Parameters	**Values**
DC link capacitance	4.4 mF
Line inductance	1 mH
DC bus voltage	270V
DC output power	400W-2000W
Frequencies of AC side	50 Hz
AC voltage magnitude (line to line)	215 V
Switching frequency	4 kHz
Modulation index	0.95 and 0.9

From Figure 7.9(a)-(j), we can see that only components on $f_c \pm 3f_0$ and $2f_c$ are noticeable. As discussed in Section 3.2.1, when M increases from 0.9 to 0.95, magnitude of harmonic on $2f_c$ decreases as illustrated in Section 3.3.2. Meanwhile, with a higher output power, the magnitude of the harmonic in the frequency of $2f_c$ increases proportionally.



(a)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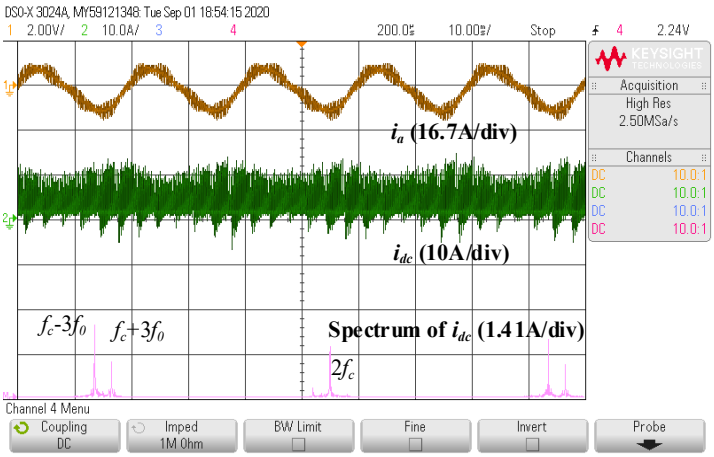
(b)


DSO-X 3024A, MY59121348: Tue Sep 01 18:54:15 2020
i_a (16.7A/div)
i_{dc} (10A/div)
f_c-3f_0
f_c+3f_0
Spectrum of i_{dc} (1.41A/div)
2f_c
Channel 4 Menu
Coupling DC
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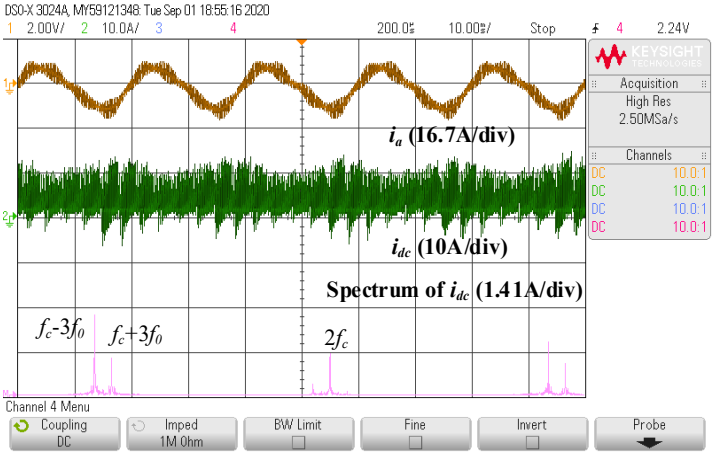
(c)


DSO-X 3024A, MY59121348: Tue Sep 01 18:55:16 2020
i_a (16.7A/div)
i_{dc} (10A/div)
Spectrum of i_{dc} (1.41A/div)
f_c-3f_0
f_c+3f_0
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Coupling DC
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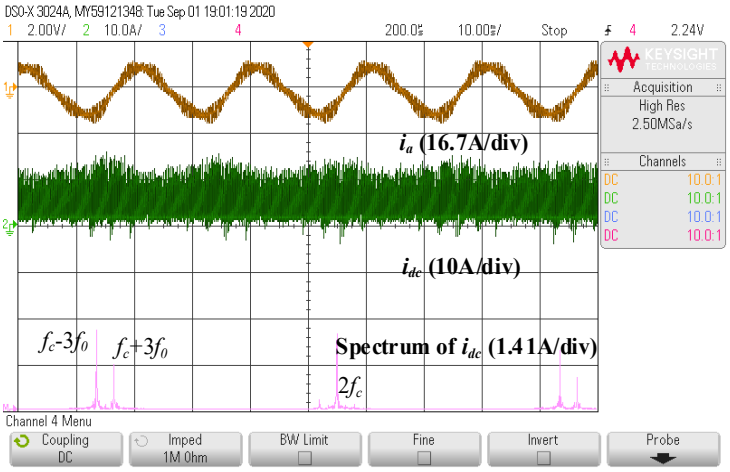
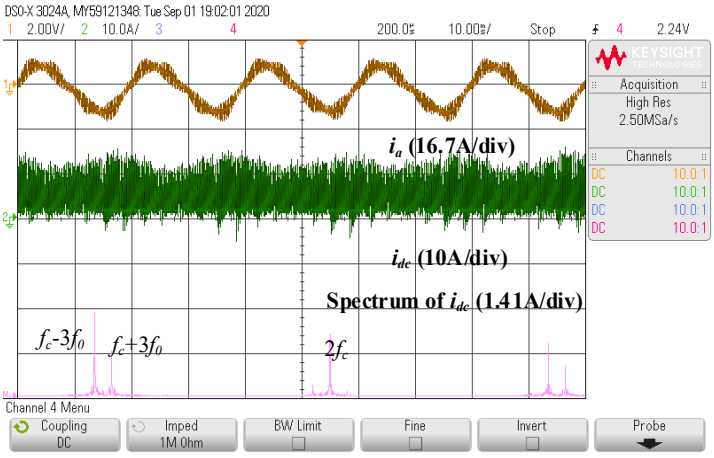
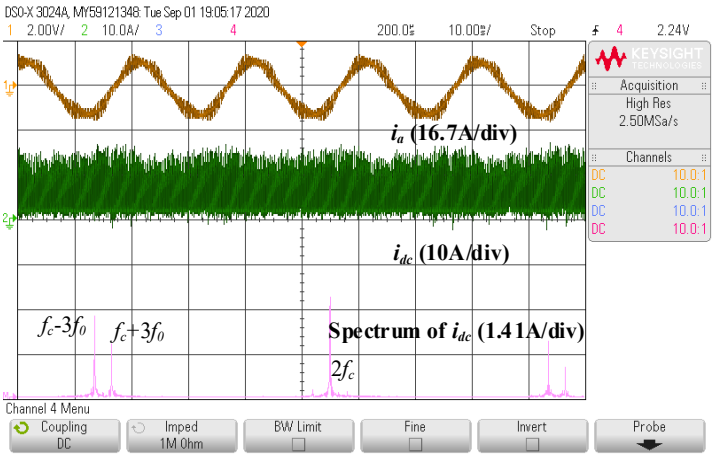

DSO-X 3024A, MY59121348: Tue Sep 01 19:01:19 2020
i_a (16.7A/div)
i_{dc} (10A/div)
f_c-3f_0
f_c+3f_0
Spectrum of i_{dc} (1.41A/div)
2f_c

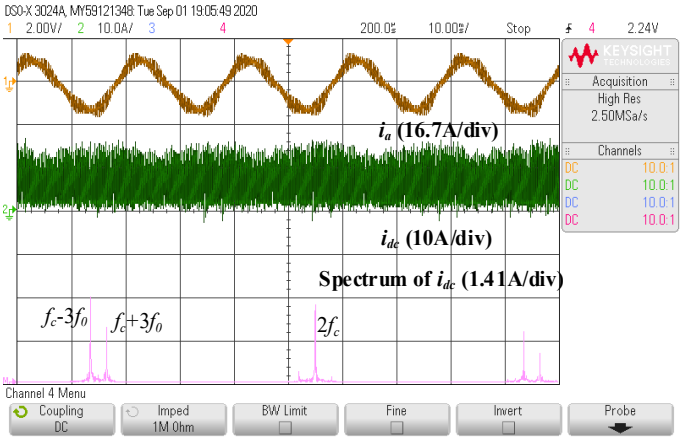
(e)


DSO-X 3024A, MY59121348: Tue Sep 01 19:02:01 2020
i_a (16.7A/div)
i_{dc} (10A/div)
Spectrum of i_{dc} (1.41A/div)
f_c-3f_0
f_c+3f_0
2f_c

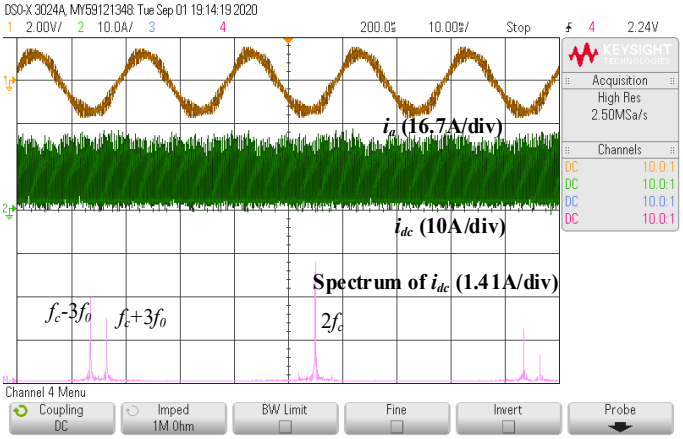
(f)


DSO-X 3024A, MY59121348: Tue Sep 01 19:05:17 2020
i_a (16.7A/div)
i_{dc} (10A/div)
f_c-3f_0
f_c+3f_0
Spectrum of i_{dc} (1.41A/div)
2f_c

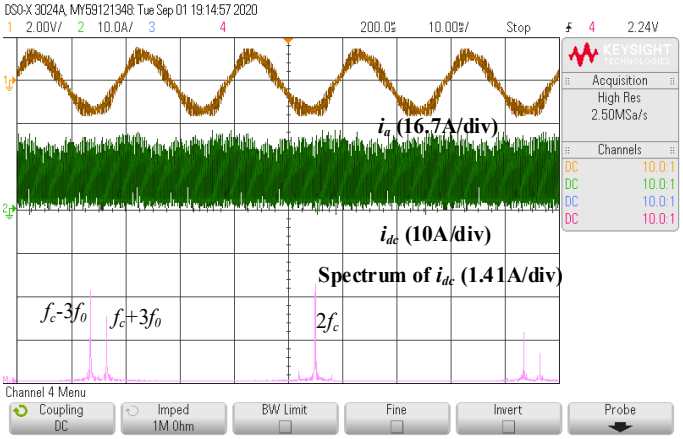
(g)



(h)



(i)



(j)

Figure 7.9: Phase current, DC bus current and its spectrum under different power (P) and modulation index (M). a) P=400W, M=0.9. b) P=400W, M=0.95. c) P=800W, M=0.9. d) P=800W, M=0.95. e) P=1200W, M=0.9. f) P=1200W, M=0.95. g) P=1600W, M=0.9. h) P=1600W, M=0.95. i) P=2000W, M=0.9. j) P=2000W, M=0.95.

Using FFT, the magnitudes of second order harmonics when M=0.95 and M=0.9 can be extracted from experimental results shown in Figure 7.9(a)-(j) and are listed in Table 7-2. These harmonic magnitudes can also be calculated using the simplified model from equ. (3-24). The comparison between the analytically simplified models and experimental results is shown in Figure 7.10. The two results match well with each other and the differences between them are within 6%. From this, we can conclude that the simplified models can be used for our harmonic suppression mechanism development.

Table 7-2: Experiment results of second order harmonics under SPWM operation.

Output power (W)	***M*=0.95, I_2 (A)**	***M*=0.9, I_2 (A)**
400	0.652	0.840
800	1.346	1.593
1200	2.013	2.433
1600	2.544	3.132
2000	3.251	3.972

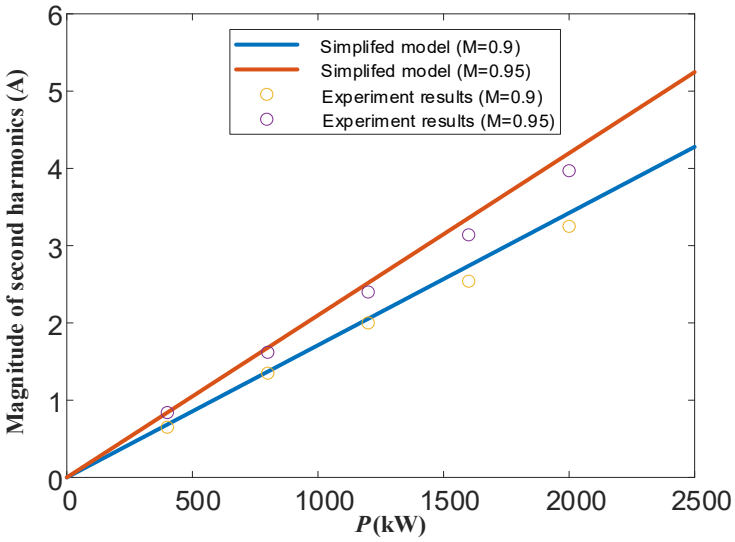


Figure 7.10: Comparison of second carrier harmonic components ($2f_c$) between experiment results and simplified model.

7.2.2 Dual-generator operation

After validating the mathematical model, harmonic cancellation method propose in Section 3.3 will be validated in this section. In this case, the battery and the DC-DC converter will not be involved, and the experiment diagram is as shown in Figure 7.11.

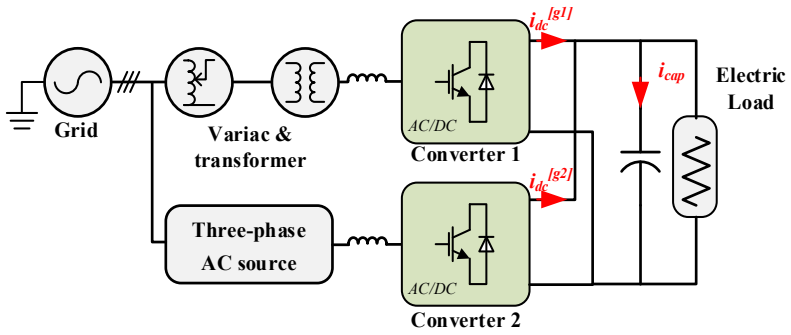


Figure 7.11: Experiment diagram of the dual-generator system under SPWM operation.

The experiment parameters are shown in Table 7-3. Output frequencies of the grid and programmable AC source are 50Hz and 70Hz respectively to represent different fundamental frequencies between the two PMSGs. The switching

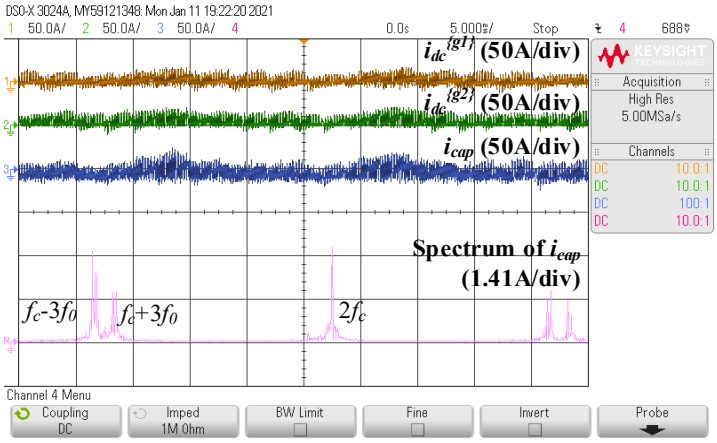
frequency is 4kHz which is much higher than fundamental frequencies. As the permanent magnet machines are running at high-speed, it is assumed that the machines are under flux-weakening control. Thus, the modulation index of the connected converter can be actively controlled.

In the proposed method, a 90-degree phase shift is applied, and thus the second carrier harmonics generated from the two converters counteract with each other. When the power sharing ratio between the two converters is 1:1, the two components show a same magnitude, and thus the second carrier harmonic can be suppressed completely on the capacitor current, as shown in Figure 7.12.

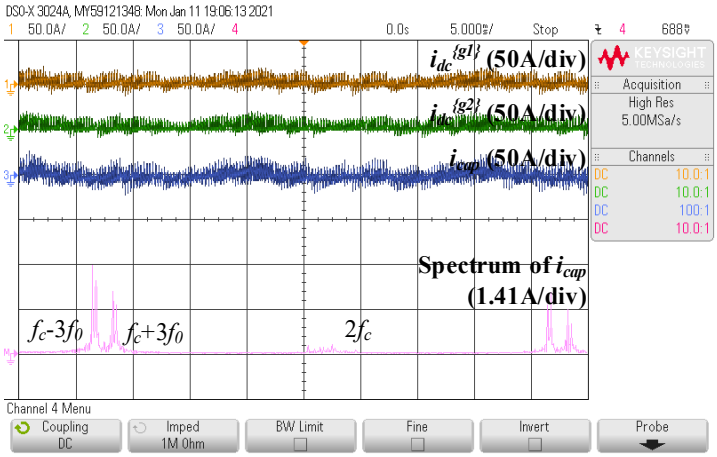
Table 7-3: Experiment parameters for dual-generator under SPWM operation.

Parameters	**Values**
DC link capacitance	4.4 mF
Line inductance	1 mH
DC bus voltage	270V
Output power	2 kW
Frequencies of AC side	50 Hz and 70 Hz
AC voltage magnitude (line to line)	215V
Switching frequency	4 kHz
Maximum modulation index	0.95

The DC-bus currents ($i_{dc}^{\{g1\}}$ and $i_{dc}^{\{g2\}}$) and the capacitor current (i_{cap}) are given in Figure 7.12. When no phase shift was implemented on carrier signals, as shown in Figure 7.12a, the magnitude on $2f_c$ is 3.1A. With a 90-degree phase shift, there is no difference happening on the first band harmonics (i.e., f_c-$3f_0$). However, magnitude on $2f_c$ is almost suppressed to 0A.



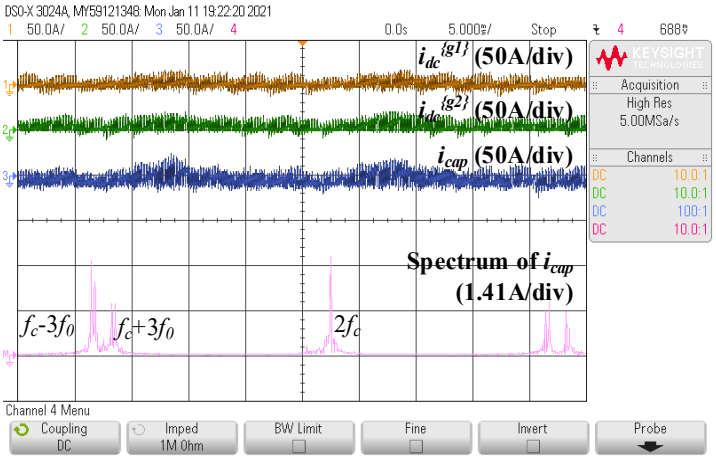
(a)



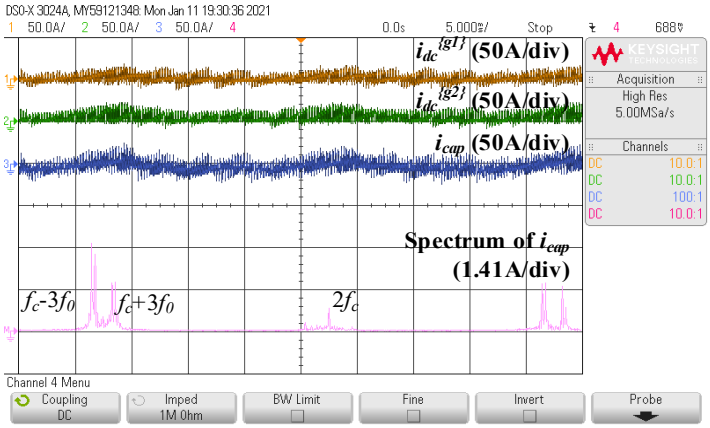
(b)

Figure 7.12: DC-bus and capacitor current when power sharing ratio is 1:1. a) Without phase shift. b) With 90-degree phase shift.

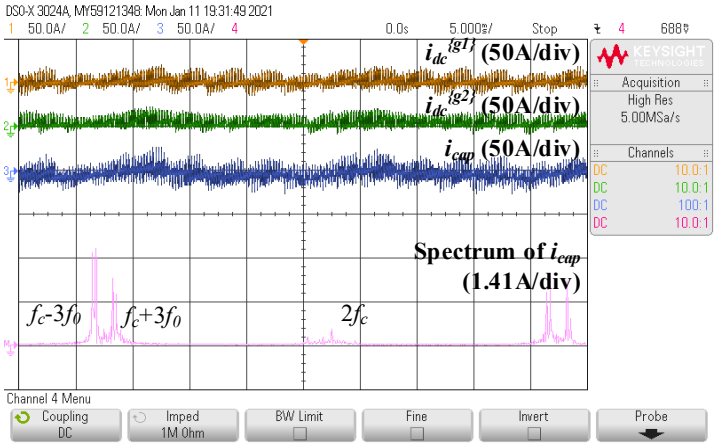
However, when the two converters generate unequal output power, the magnitudes of the second carrier harmonics from the two converters become unequal too. The 90-degree phase shift is not able to suppress the component completely. As discussed in 3.3, with an adjustment of modulation index on one converter, the magnitudes of the two components can be the same. Therefore, an complete suppression of the second carrier harmonic can be achieved on the capacitor current.



(a)



(b)



(c)

Figure 7.13: DC-bus and capacitor currents when power sharing ratio is 0.8:1. a) No phase shift and no optimised modulation index. b) With 90-degree phase shift without optimised modulation index. c) 90-degree phase shift together with optimised modulation index.

When the power sharing ratio between two converters is 0.8:1. The results are under a) constant *M* (0.95) with no phase shift, b) constant *M* with a 90-degree phase shift, c) variable *M* with 90 degrees phase shift, are analysed, as shown in Figure 7.13a-c. Comparing Figure 7.13b with Figure 7.13a, the second carrier harmonic is suppressed from 3.0A to 0.8A when only applying a 90-degree phase shift on the carrier signal. A 73.3% suppression ratio was achieved. Then, this magnitude was further suppressed to 0.1A (a further 23% reduction) when optimised modulation index applied, as shown in Figure 7.13c .

Comparing Figure 7.13b and c, there is a little increase on the first band harmonic. The is due to the fact that experiment is not based on PMSM because of limitation of test rig. Meanwhile, the study has not considered about the power loss on converter, which will also cause increase on first band harmonics. These issues can be further studied in the future.

7.3 Power Quality Improvement of Dual-Generator System under SVPWM Operation

This section will deal with the power quality improvement when the two AC-DC converters work under space vector PWM (SVPWM) operation. This is related to Chapter 4.

When only one AC-DC converter operates under SVPWM modulation, the DC-side current is measured to validate the simplified harmonic models proposed in Section 4.3. Then, an adjustable phase-shift angle between the two AC-DC converters is applied, and a suppression of the total harmonic of both the first and the second carrier harmonics can be achieved on the capacitor current. The experiment refers the suppression method proposed in Section 4.4.

7.3.1 Single generator operation

Same as carrier based SPWM operation, the single generator experiment is also investigated for SVPWM modulation. The experiment parameters are shown in

Table 7-4. Here fundamental frequency is 50 Hz, and switching frequency is 2kHz. Here, f_c/f_0=40, harmonic on f_c is more visible compared with higher switching frequency. The modulation index is fixed as 1.04, which equals $0.9 \times \frac{2}{\sqrt{3}}$. This value is suitable for flux-weakening operation.

Table 7-4: Experiment parameters for single generator under SPWM operation.

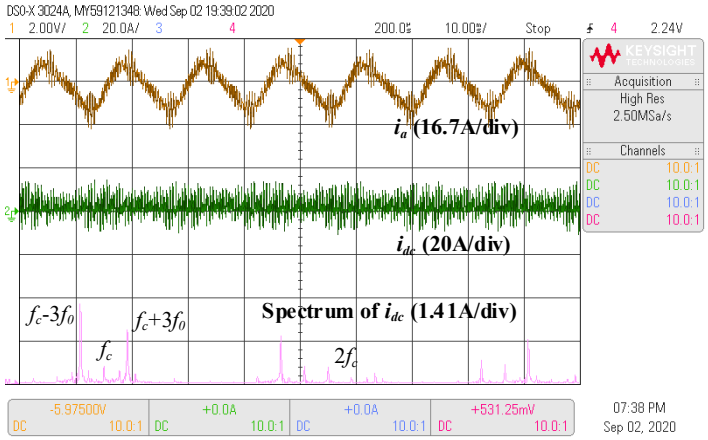
Parameters	**Values**
DC link capacitance	4.4 mF
Line inductance	1 mH
DC bus voltage	270V
Output power	400W-2000W
Frequencies of AC side	50 Hz
AC voltage magnitude (line to line)	245 V
Switching frequency	2 kHz
Modulation index	1.04 (=$0.9 \times \frac{2}{\sqrt{3}}$)

Current of phase A (i_a), DC-side current (i_{dc}) and the spectrum of i_{dc} are observed firstly, as shown in Figure 7.14. From Figure 7.14a to e, the output power is increased from 400W to 2kW with steps of 400W.

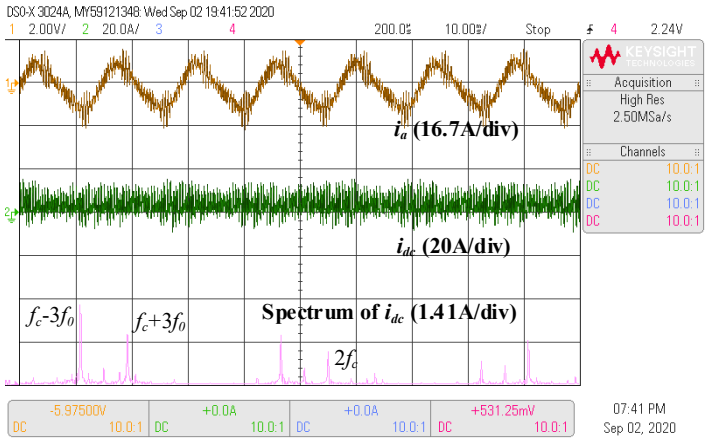
Derived from Figure 7.14a-e, magnitudes of harmonics on both f_c and $2f_c$ are listed in Table 7-5 and shown in Figure 7.15. Meanwhile, simplified models of proposed in Section 4.3 are also drawn in Figure 7.15. Compare between experiment results and simplified model, errors between them are always less than 5%, which validate the effectiveness of mathematical model.

Harmonic on f_c slightly decreases with higher output power. The mathematical proof has been provided in Appendix A. Meanwhile, the magnitudes on $2f_c$

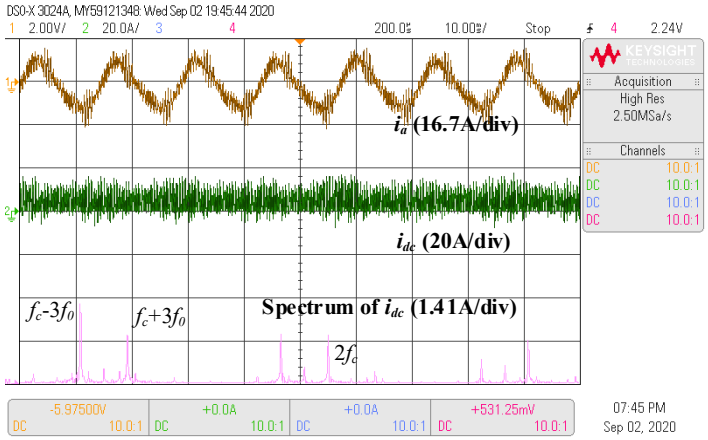
components increase significantly when the output power increases, and a proportional relationship between the magnitude and the output power can be observed. In summary, harmonic on f_c is always higher than that on $2f_c$ under low power region. However, harmonic on $2f_c$ becomes higher than that on when the power increases.



(a)



(b)



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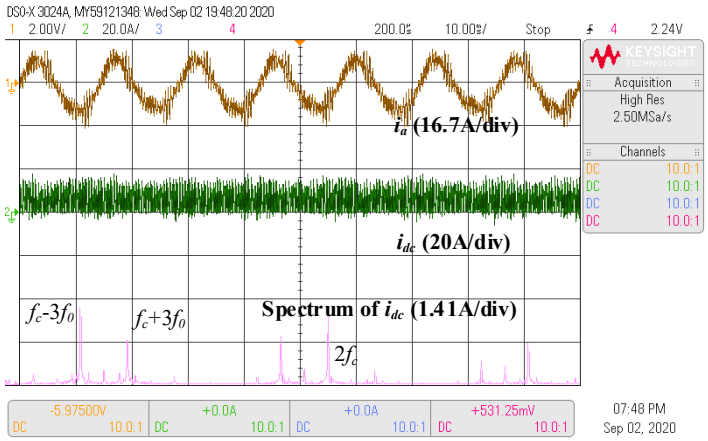

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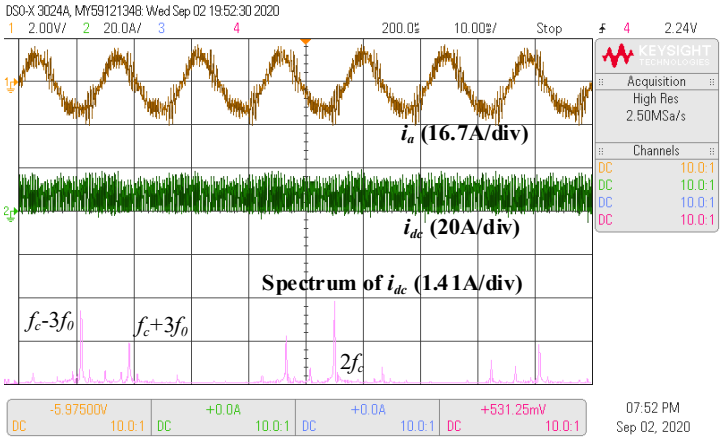


(e)

Figure 7.14: Phase current, DC bus current and its spectrum under different power (P) and fixed modulation index (M=1.04). a) P=400W. b) P=800W. c) P=1200W. d) P=1600W. e) P=2000W.

Table 7-5: Experiment results of harmonic magnitudes under SVPWM operation

Output power (W)	I_1 **(A)**	I_2 **(A)**
400	0.549	0.536
800	0.518	1.051
1200	0.479	1.555
1600	0.457	2.149
2000	0.420	2.672

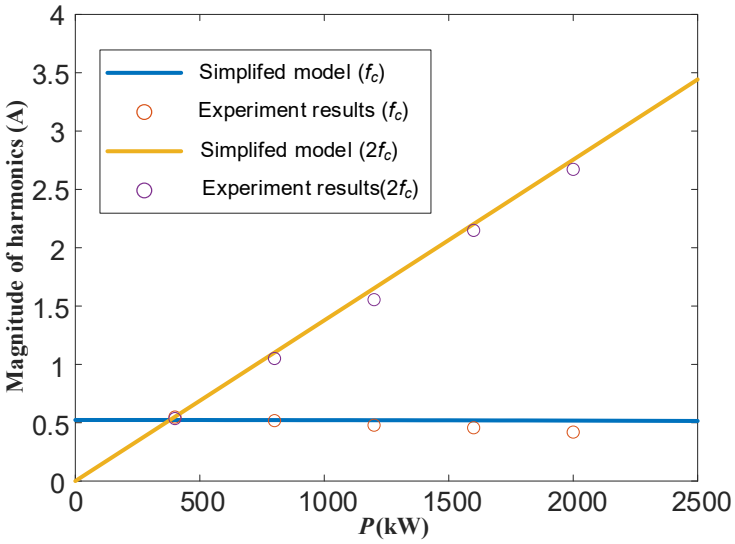


Figure 7.15: Comparison between simplified model and experiment.

7.3.2 Dual-generator operation

To validate the harmonic suppression method under SVPWM operation in a dual-generator system, the experimental diagram is the same as Figure 7.11. The difference is only in the control side, which SVPWM is applied in this case. Some basic experimental parameters are given in Table 7-6. Output frequencies

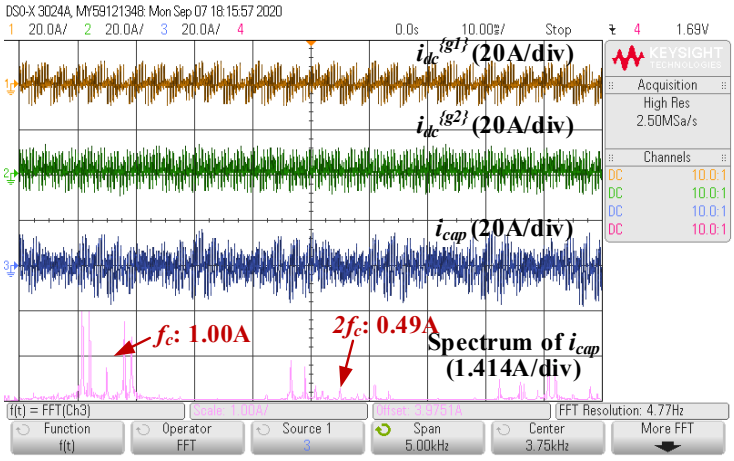
of the grid and programmable AC source are 50Hz and 70Hz respectively to represent different fundamental frequencies among PMSGs. The switching frequency is 2kHz where the carrier-fundamental frequency ratios for both converters are 40:1 and 28.6:1. The line-to-line voltages of the AC side are 246V. Converters must operate under flux-weakening control in this case. The maximum modulation index is set as 1.04. Power sharing ratio is 1:1 between converters.

Table 7-6: Experiment parameters for single generator under SPWM operation.

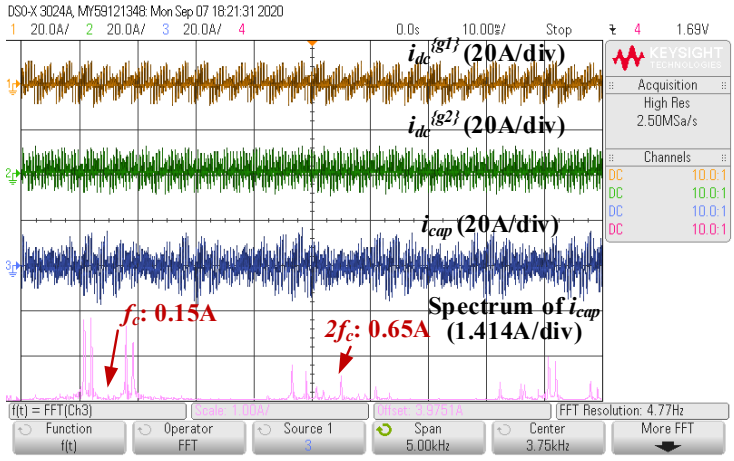
Parameters	**Values**
DC link capacitance	4.4 mF
Line inductance	1 mH
DC bus voltage	270V
AC voltage magnitude (line to line)	246V
Frequencies of AC side	50 Hz & 70 Hz
Switching frequency	2 kHz
Modulation index	1.04 ($=0.9 \times \frac{2}{\sqrt{3}}$)

When the output power of the dual-generator system is 400W and the power for each converter are the same which is 200W, the currents on DC bus from the two converters ($i_{dc}^{\{g1\}}$ and $i_{dc}^{\{g2\}}$) and the capacitor current (i_{cap}) are provided, as shown in Figure 7.16. In Figure 7.16a, no phased shift is applied. Harmonics in the frequencies of f_c and $2f_c$ are 1.0A and 0.36A, respectively. Here, the f_c component is not neglectable compared to the $2f_c$ one. According to the discussion in Section 4.4, a 180-degree phase shift should be applied to mainly supress first carrier harmonic. The result is shown in Figure 7.16b. Harmonic on f_c is supressed to 0.15, which has 85% suppression. Meanwhile, harmonic on $2f_c$ is almost same.

When the output power of dual-generator system increases to 4kW, the second order harmonic become more dominant in capacitor current spectrum which is shown in Figure 7.17a. Where harmonics on f_c and 2 f_c are 0.74A and 4.54A. With a 90-degree phase shift, the second order harmonic is supressed to 0.26A (94.3% suppression). Meanwhile, first order harmonic is also reduced from 0.74A to 0.58A (21.6% suppression). The result is shown in Figure 7.17b. Both the first and second carrier harmonic are supressed, which is as same as simulation shown in Section 5.6.

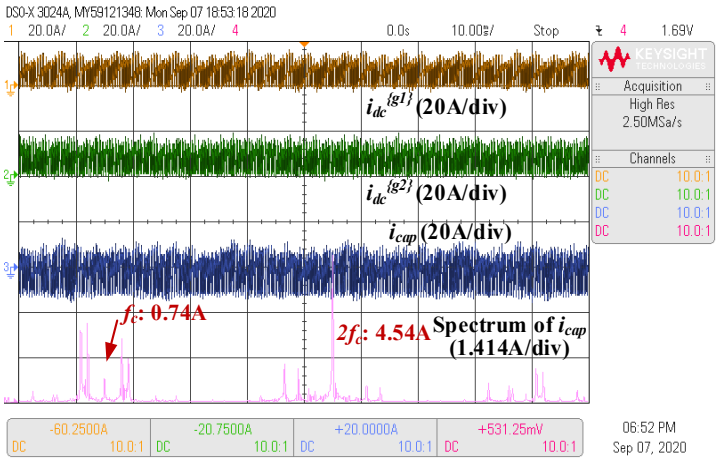


(a)

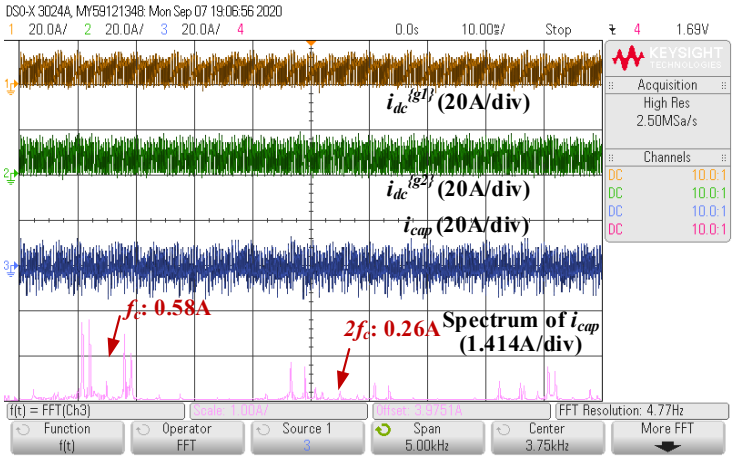


(b)

Figure 7.16: DC-bus and capacitor current when output power is 400W. a) Without phase shift. b) With an optimised phase shift angle (180°).



(a)



(b)

Figure 7.17: DC-bus and capacitor current when output power is 4kW. a) Without phase shift. b) With optimised phase shift angle (93°).

7.4 Power Quality Improvement of Dual-Generator System with an Energy Storage System Involved

This section will deal with the power quality improvement when an energy storage system (ESS) with a DC-DC converter involved in the system. This is related to Chapter 5 and Chapter 6.

7.4.1 One AC-DC converter and one DC-DC converter

The experimental study starts from the simplest case, in which only one AC-DC converter and one DC-DC converter are involved in the system. The experimental diagram is given in Figure 7.18.

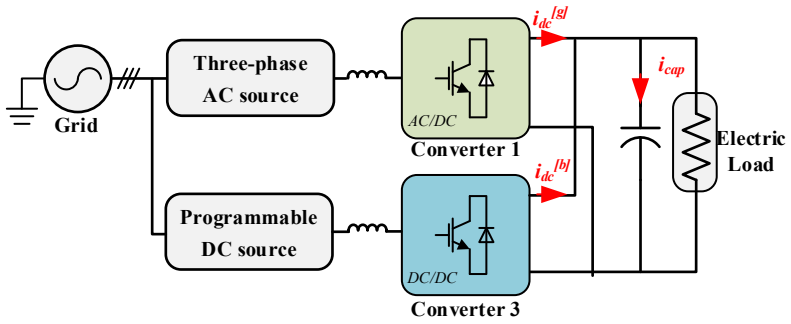


Figure 7.18: Experimental diagram when only one AC-DC converter and one DC-DC converter are involved in the system.

In Section 5.3, a new PWM modulation method of the DC-DC converter (EGW PWM) is proposed to actively adjust the magnitude of the harmonic in a specific frequency. With the EGW PWM, the first-band harmonic (i.e., f_c-3f_0) can be suppressed by the coordination between the AC-DC converter and the DC-DC converter, as discussed in Section 5.4.

The parameters of the experiment are shown in Table 7-7. The AC fundamental frequency is 50Hz. The switching frequency of the AC-DC converter, f_c, is set at 4kHz. The carrier signal frequency for conventional PWM $f_{c1}^{[b]}$ is set to be 2f_c, i.e. 8kHz, which is a typical value for such a DC-DC converter. For the EGW PWM method, the carrier frequency ($f_c^{[b]}$) is set at f_c-3f_0 (3.85kHz). Thus, using EGW PWM method, the switching frequency is 7.7kHz, which is a little lower than that in the conventional PWM. This makes the comparison between the harmonics before and after active suppression reasonable.

The system is controlled using TI DSP TMS320F28379D, which is embedded with an ePWM module. The EGW PWM of the DC-DC converter can be achieved by properly configuring the PWM actions in the ePWM module

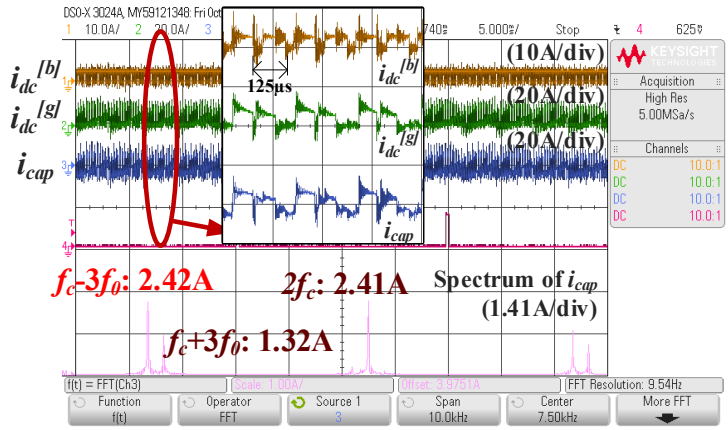
according to the counting direction. The extra computation for harmonic suppression is mainly on f_c-3f_0 harmonic estimation and phase shift angle calculation. This computation time is tested in the software which is 16μs. In the experiment, these calculations are implemented in every 20ms which is the sample time of the DC-side current ($i_{dc}^{[g]}$) control. 20ms is much longer than 16μs, and thus the extra computation will not affect system performance.

Table 7-7: Experiment parameters for AC-DC and DC-DC converters

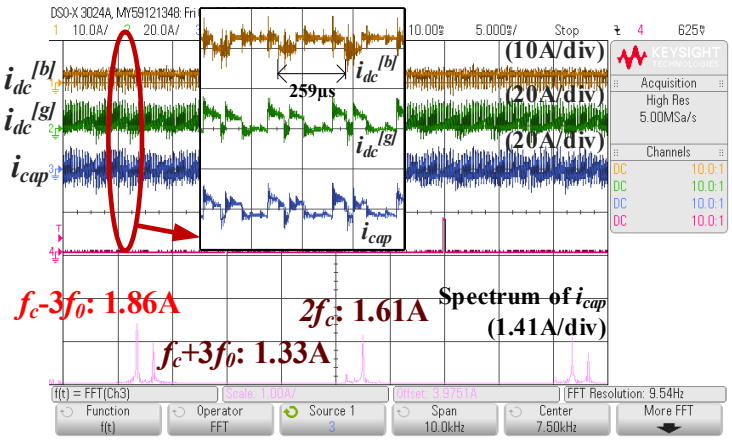
Category	Parameters	Values
DC-link	DC link capacitance	4.4 mF
	DC bus voltage	270V
AC-DC	Line inductance	1 mH
	Frequencies of AC side f_0	50 Hz
	Voltages of AC side	215 V
	Switching frequency f_c	4 kHz
	Modulation index	0.90
DC-DC	Inductance	30 mH
	Carrier frequency $f_{c1}^{[b]}$	8kHz (conventional PWM)
	Carrier frequency $f_c^{[b]}$	3.85 kHz (EGW PWM)

In the first case, the output power of the PMSG and the battery are set as 1kW and 0.5kW, respectively. The DC-bus currents from the AC-DC converter and the DC-DC converter ($i_{dc}^{[g]}$ and $i_{dc}^{[b]}$) are observed, and the current flowing into the capacitor (i_{cap}) and its spectrum are also analysed, as shown in Figure 7.19. The DC-DC converter is firstly driven by the conventional PWM, and the results are shown in Figure 7.19a. Then, the DC-DC converter is driven by the proposed EGW PWM scheme, and the results are shown in Figure 7.19b. By

comparing these two results, the harmonic component of f_c-3f_0 is suppressed from 2.42A to 1.86A (23.1% reduction). Although with over 20% reduction, this component is not completely cancelled as expected. This is because the power from the battery (thus current $i_{dc}^{[b]}$) is much smaller than that of PMSG (thus current $i_{dc}^{[g]}$). In that case, the amplitude of f_c-3f_0 is even higher than A_{1max} which is the maximum value that the DC-DC converter can generate on this component. The two gate signal pulses in one carrier cycle of the EGW PWM overlap each other. This is equivalent to halving the switching frequency. Thus, the switching cycle is increased from 125μs ($f_{c1}^{[b]}$=8kHz) to 259μs ($f_c^{[b]}$=3.85kHz), as shown in the zoom-in views of Figure 7.19a and b.



(a)



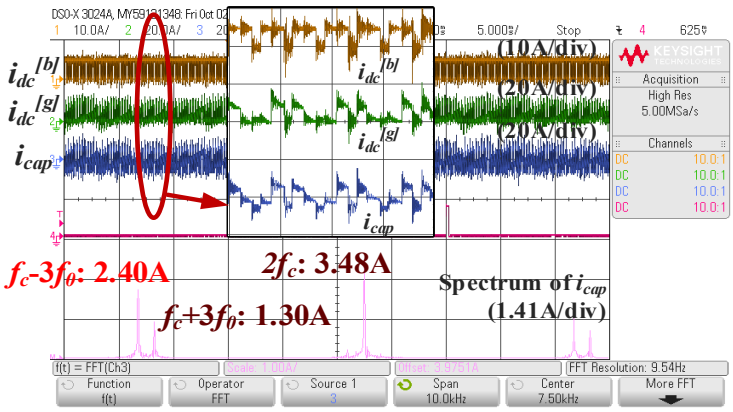
(b)

Figure 7.19: Harmonic suppression when $P^{[g]}$=1kW, $P^{[b]}$=0.5kW. a) Without suppression. b) With EGW suppression.

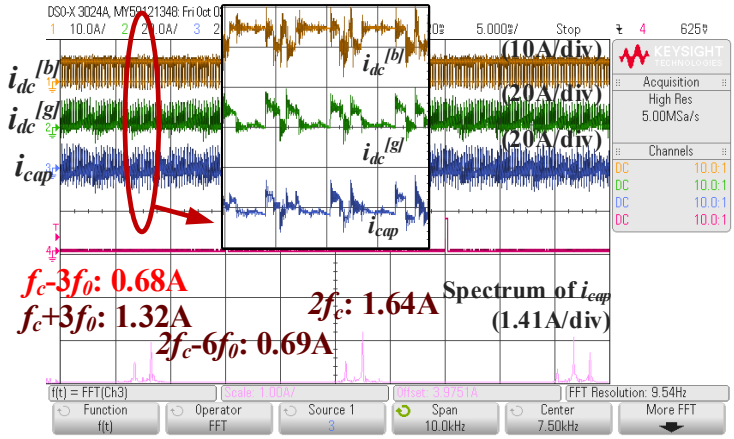
However, if we increase the battery power, the harmonic of f_c-3f_0 can be further suppressed. When the output power of the DC-DC converter is increased to 1kW, the DC-DC converter should have the capability to fully cancel the f_c-3f_0 component. Results, in this case, are shown in Figure 7.20a and b. The harmonic component of f_c-3f_0 frequency has been suppressed from 2.44A to 0.68A (73.8% reduction). The error is due to the fact that the magnitude of f_c-3f_0 component from AC-DC converter is an approximately estimated value. Comparing Figure 7.20b to Figure 7.19b, the two gate signal pulses in one carrier cycle do not overlap each other, as shown in the zoom-in view of Figure 7.20b. In this view, $i_{dc}^{[b]}$ counteracts pulses on $i_{dc}^{[g]}$ and the harmonic on the capacitor (i_{cap}) can be suppressed.

It is also interesting to notice the change on the 2f_c (f_c=4kHz) component of i_{cap}. When the DC-DC converter operates with conventional PWM ($f_{c1}^{[b]}$=8kHz), the current harmonics will be adding to the 2f_c component. However, with EGW PWM, the carrier signal has a frequency of 3.85 kHz and there will be no harmonic component at 2f_c. Therefore, it can be noticed from Figure 7.20a and Figure 7.20b that the harmonic in 2f_c is reduced from 3.48A to 1.64A (52.9% reduction).

In practice, the battery voltage varies according to its working status, i.e., state of charge (SoC). Therefore, an experiment results when the battery voltage is 180V (10% variation compared to the nominal voltage) is given, as shown in Figure 7.21. In this view, $i_{dc}^{[b]}$ counteracts pulses on $i_{dc}^{[g]}$ and the harmonic on the capacitor (i_{cap}) can be suppressed. This validates the effectiveness of the proposed method when the battery voltage varies.



(a)



(b)

Figure 7.20: Harmonic suppression with EGW suppression when $P^{[g]}$=1kW, $P^{[b]}$=1kW. a) Without suppression. b) With EGW suppression.

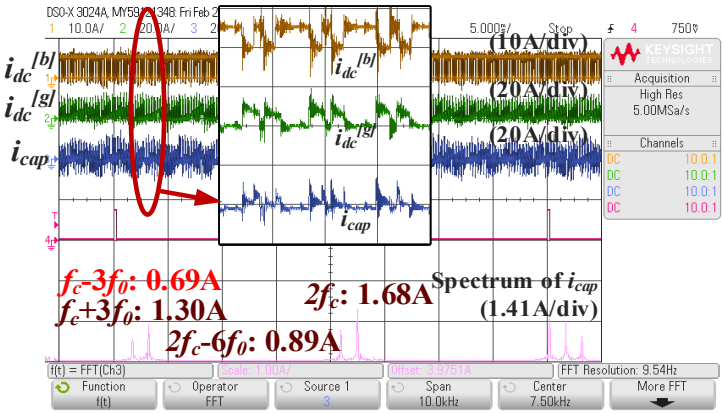


Figure 7.21: Harmonic suppression with EGW suppression when $P^{[g]}$=1kW, $P^{[b]}$=1kW, V_{bat}=180V.

The proposed method can be extended to other harmonic components on the DC-link, i.e., in f_c+3f_0. By simply adjusting the carrier frequency (to f_c+3f_0) and the phase angle of the EGW PWM, a suppression of f_c+3f_0 harmonic can be achieved, as shown in Figure 7.22. The output power of the AC-DC and DC-DC converters are 1kW, and the experimental result without harmonic suppression has been given in Figure 7.20a. Comparing Figure 7.22 to Figure 7.20a, the harmonic in f_c+3f_0 is reduced from 1.30A to 0.34A (73.8% reduction).

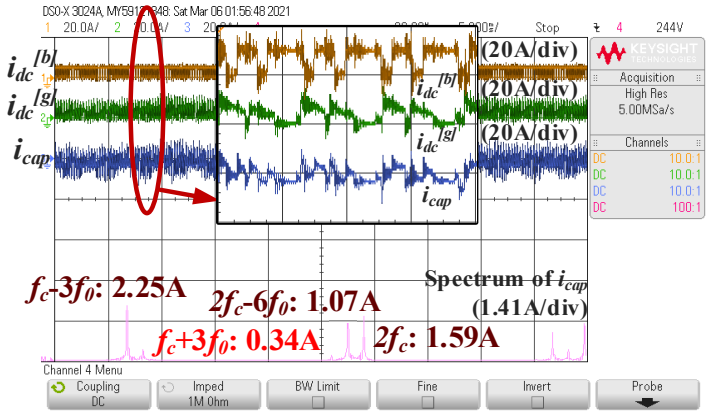


Figure 7.22: Harmonic suppression on f_c+3f_0 with EGW suppression when $P^{[g]}$=1kW, $P^{[b]}$=1kW.

7.4.2 Two AC-DC converters and one DC-DC converter

To validate the concept proposed in Chapter 6, this section will discuss the experimental results of harmonic suppression when two AC-DC converters and one DC-DC converter supply the DC bus altogether, as shown in Figure 7.23.

The parameters of the experiment are shown in Table 7-8. The AC fundamental frequencies of the two converters ($f_0^{[g1]}$ and $f_0^{[g2]}$) are 50Hz and 70Hz, respectively. This is to emulate the LP and HP shafts of the engine which are with different rotation speeds. The switching frequency of the two AC-DC converters, f_c, is set at 4kHz. The carrier signal frequency for conventional PWM $f_{c1}^{[b]}$ is set to be 2f_c, i.e. 8kHz, which is a typical value for such a DC-DC converter. For the EGW PWM method, the carrier frequency ($f_c^{[b]}$) is set at f_c-3$f_0^{[g2]}$ (3.79kHz) because converter 2 generates a higher component in f_c-3$f_0^{[g2]}$ compared to f_c-3$f_0^{[g1]}$ component from the converter 1. Thus, using EGW PWM

method, the switching frequency is 7.79kHz, which is a little lower than that in the conventional PWM. This makes the comparison between the harmonics before and after the active suppression reasonable.

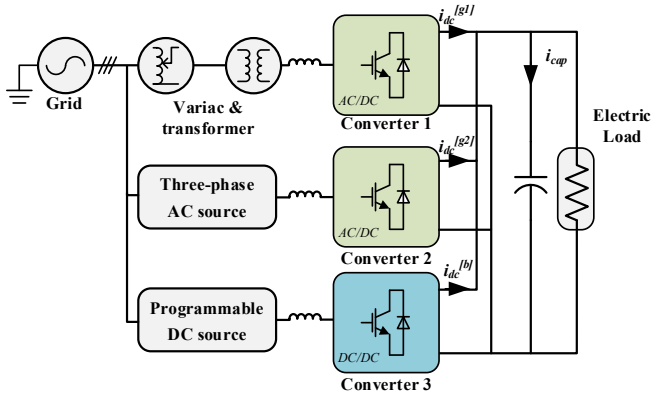
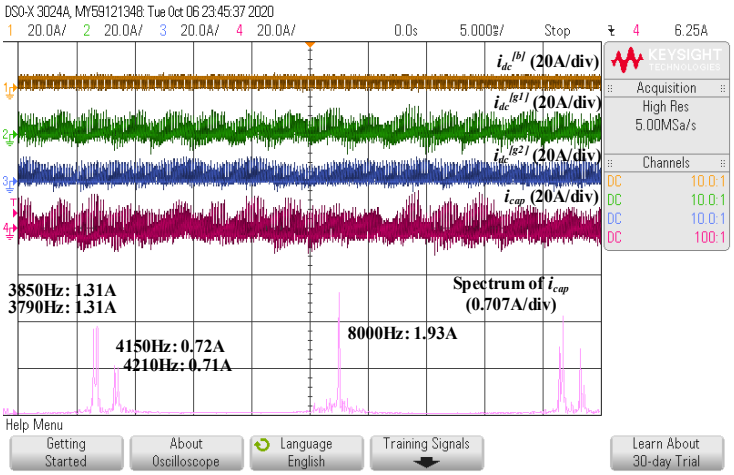


Figure 7.23: Experiment diagram.

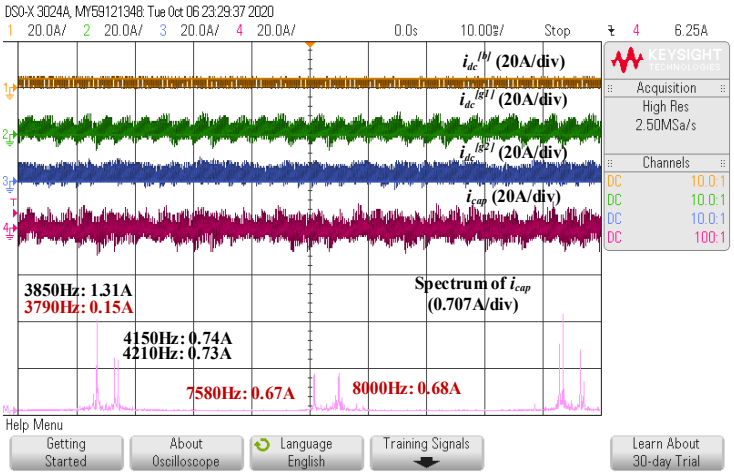
Table 7-8: Experiment parameters for AC-DC and DC-DC converters

Category	Parameters	Values
DC-link	DC link capacitance	4.4 mF
	DC bus voltage	270 V
	DC load	2.5 kW
AC-DC	Line inductance	1 mH
	Frequencies of AC side $f_0^{[g1]}$ and $f_0^{[g2]}$	50 Hz & 70 Hz
	Voltages of AC side	210 V
	Switching frequency f_c	4 kHz
	Modulation index	0.90
	Output power $P^{[g1]}$ and $P^{[g2]}$	1 kW & 1kW
DC-DC	Inductance	30 mH
	Carrier frequency $f_{c1}^{[b]}$	8 kHz (conventional PWM)
	Carrier frequency $f_c^{[b]}$	3.79 kHz (EGW PWM)
	Output power $P^{[b]}$	1 kW

In experimental validation, the output power of the two AC-DC converters and the DC-DC converter ($P^{[g1]}$, $P^{[g2]}$, and $P^{[b]}$) are all 1kW. The AC-DC converter of PMSG1 generates the components in the frequencies of $f_c \pm 3f_0^{[g1]}$ (3850Hz and 4150Hz) and $2f_c$ (8000Hz). The AC-DC converter of PMSG2 generates the components in the frequencies of $f_c \pm 3f_0^{[g2]}$ (3790Hz and 4210Hz) and $2f_c$ (8000Hz). The DC-DC converter generates the components in the frequencies of f_c(4000Hz) and $2f_c$ (8000Hz). These components are summed up on the capacitor current (i_{cap}), as shown in Figure 7.24a.



(a)



(b)

Figure 7.24: Experimental results when $P^{[b]}$=1kW, $P^{[g1]}$=1kW, $P^{[g2]}$=1kW. a) Without optimisation. b) With optimisation.

A 90-degree phase shift is applied between the carrier signals of the two AC-DC converters to suppress the harmonic in $2f_c$. Comparing to Figure 7.24a, the $2f_c$ components on i_{cap} is suppressed from 1.93A to 0.68A (64.8% reduction), as shown in Figure 7.24b. The component is not suppressed completely, because there is some nonnegligible error when calculating the $2f_c$ harmonic if the PMSG operates under low power range.

EGW PWM is applied on the DC-DC converter to suppress one of the first band harmonics (f_c-$3f_0$[g2], 3790Hz in this case). The carrier frequency of the EGW PMW is set as f_c-$3f_0$[g2] (3790Hz). This component is suppressed from 1.31A to 0.15A (88.5%), as shown in Figure 7.24b.

With such a comprehensive optimisation, both the first-band and the second carrier harmonics on i_{cap} are suppressed.

7.5 Chapter Summary

This chapter describes the test platform in the lab and presents experimental results. The harmonic suppression when two AC-DC converters operate under SPWM (Chapter 3) and SVPWM (Chapter 4) has been validated. The mathematical models of DC-side current under these two PWM methods are also proved. In addition, the feasibility and effectiveness of the proposed suppression methods using DC-DC converter (Chapter 5 and Chapter 6) have been proved.

Summarising, the reported experimental results in this chapter have confirmed all the key theoretical findings of this thesis.

Chapter 8

Conclusion and Future Work

8.1 Conclusion and Discussion

This thesis aims to address the power quality issues of the dual-channel power generation system, specifically focuses on the reduction of harmonics on a common dc bus. This, in return, will extend the lifetime and reduce the weight of the dc-bus capacitor. The main contributions of this thesis are summarized as:

A. Development of simplified mathematical models of the switching harmonics from the AC-DC converter and the DC-DC converter on the DC-link. The information of harmonics, such as the magnitudes and the phase angles, are essential for harmonic suppression. With some simplification of the mathematical process, the controller can achieve such information with a lower calculation burden and without additional hardware.

B. Analysis and establishment of the methodologies of new adjustable PWM methods. Conventional PWM methods give a fixed harmonic distribution on the DC-link. With the aim to modify the spectrum distribution of DC-side current, an adjustable PWM method is proposed in this research.

C. Investigation of solutions for actively suppressing capacitor harmonic with system-level coordination. There are more than two sources amounted in the dual-channel electric power generation systems. System-level coordination is essential among sources to suppress harmonic with the same frequency. With the target of suppressing total

harmonics on the DC-link capacitor, system-level control is developed under different operations from each source, including information transfer and phase-shift angle assignment.

In **Chapter 3**, a simplified mathematical model on second carrier current harmonic was investigated. The results show the magnitude of the component was only determined by the value of DC current and modulation index, while the phase angle of it is caused by the carrier phase angle. Based on a simplified model, a second carrier harmonic cancellation method was proposed. By actively controlling modulation index together with 90-degree phase shift on the carrier signal, a cancellation can be realized in a 2-source power system. The method can work under any machine speed and need no communication of harmonic phase angle among sources. The simplified model and cancellation method are basic research of harmonic cancellation. It gives potential approach of harmonic cancellation in not only dual-generator system, but also other multi-converter systems such as microgrid or back-to-back converter.

In **Chapter 4**, simplified mathematical models for DC-link harmonics on the AC-DC converter are investigated. The calculation burden of microprocessor is significantly released. For the first switching harmonic, magnitude can be achieved with the measurements of *dq*- voltages and currents. For the second carrier harmonic, the magnitude is proportional to the DC component of the output current. Based on the simplified models, a cancellation method of DC-link harmonics was proposed. Under low power range, phase-shift angle is set as 180° to suppress the first carrier harmonic mostly. When the output power increases, the phase-shift angle is adjusted from 180° to 90° actively to suppress both the first and second carrier harmonics. Finally, simulation was implemented to verify the validity of the proposed harmonic models and the cancellation method.

In **Chapter 5** proposed a new EGW modulation scheme for DC-DC converters which enables active damping of harmonics generated from AC-DC converters. This chapter focuses on fc-3f0 harmonic cancellation, but similar methods can be used to suppress other components. A enhanced PWM synchronisation

method is also proposed to handle the challenge of non-integer multiple relation between two carrier frequencies. Experiment results verify the validity of the proposed harmonic models and suppression method. The proposed work is extremely useful to improve power electronic dominated DC grid and can achieve improved power quality with no extra cost.

Chapter 6 combines the suppression methods in Chapter 3 and 5 altogether to suppress the first sideband and the second carrier harmonics at the same time. To efficiently suppress the most significant component, a component selection block is designed in the controller of the DC-DC converter.

Chapter 7 describes the test platform in the lab and presents experimental results. The harmonic suppression when two AC-DC converters operate under SPWM (Chapter 3) and SVPWM (Chapter 4) has been validated. The mathematical models of DC-side current under these two PWM methods are also proved. In addition, the feasibility and effectiveness of the proposed suppression method using DC-DC converter (Chapter 5 and Chapter 6) have been proved.

Although the context of the work is based on a dual-channel power generation system, it can be also considered to be a challenging case of multi-converter system with common DC bus, such as back-to-back converters, electric vehicles. Thus, the analysis presented afterwards can be applied to optimise them as well.

8.2 Future Work

This thesis has introduced the power quality improvement for dual-channel power generation system. Some future work can be carried out based on the theories in this thesis, which are listed as follow:

1. First-band harmonic suppression for SVPWM: In this thesis, the harmonics on the frequencies of $f_c \pm 3f_0$ have not been studied when the PMSG works under SVPWM operation. In the first switching harmonic band, there are three

significant components (f_c, $f_c \pm 3f_0$), which is different from the spectrum of SPWM operation. Therefore, some trade-off will happen when selecting one of them to suppress.

2. Expand the suppression method when the starter-generator works under i_d=0 control: In this thesis, the PMSG always works under flux-weakening control because of the high-speed operation. However, the PM machine works under i_d=0 control in starting mode. The proposed mathematical models and the suppression methods in this thesis can be expanded to such operation.

3. Harmonic analysis when considering dead-time effect. Dead-band times will distort the switching function of the two-level converter, and thus the AC and DC harmonics. The distortion effect is related to the flow directions of AC currents [106]. When dead-band times are not neglectable in some applications, the distortion of DC-side harmonics can be further studied.

4. System with more than two PMSGs: Distributed propulsion is one of the research trends in the future MEA. Hence, the power system in such MEA is with more than two generators. How to suppress DC-link harmonic with more than two AC-DC converters is a challenge for such a system. Moreover, artificial intelligence technology is an interesting solution that is worth trying.

5. Power quality improvement when the PMSGs are controlled using the three-level converters: Compared to the two-level converter, the three-level converter provides a lower switching frequency which will benefit the system efficiency. When the three-level converters work in parallel, the power quality issue is an interesting topic. The research can not only for switching harmonic suppression, but also balancing neutral points voltage with active coordination among converters.

8.3 Publications

The research given in the thesis has resulted in 1 conference paper [112], 3 journal papers on IEEE transactions [113]-[115], and we are currently drafting more journal and conference papers from the work of the thesis.

Appendix A

Mathematical Proof of The Decreasing Trend of $I_{dc,1,0}$

Using field oriental control (FOC), PMSG can be easily controlled. Equations of the *dq*- model for a PMSM are as follow.

$$\begin{cases} v_d = Ri_d + L_d \dfrac{di_d}{dt} - \omega_e L_d i_q \\ v_q = Ri_q + L_q \dfrac{di_q}{dt} + \omega_e L_d i_d + \omega_e \psi_m \end{cases} \tag{A1.1}$$

Where v_d, v_q, i_d, i_q, L_d, L_q, R, φ_m, ω_e represent *d*-axis stator voltage, *q*-axis stator voltage, d-axis current, *q*-axis current, *d*-axis inductance, *q*-axis inductance, stator resistance, flux linkage of permanent magnet, electrical rotor angular velocity. In MEA, surface mounted PMSG are always used because of its high mechanical property under high-speed operation. Then, the *d*- and *q*-axis inductance are identical (L_d=L_q=L_s). Neglecting the voltage drop on resistor and transient reaction, (A1.1)former equations of *d*- and *q*-axis can be simplified as

$$\begin{cases} v_d = -\omega_e L_s i_q \\ v_q = \omega_e L_s i_d + \omega_e \varphi_m \end{cases} \tag{A1.2}$$

As illustrated in the paper, the PMSGs in MEA always work in a flux-weakening operation, the magnitude of the output voltage from the AC-DC converter is

$$\begin{aligned} \sqrt{v_d^2 + v_q^2} &= \omega_e \sqrt{(L_s i_q)^2 + (L_s i_d + \psi_m)^2} \\ &= \frac{MV_{dc}}{2} \end{aligned} \tag{A1.3}$$

where M is the modulation index of the converter.

For a given output converter power P, the AC-side terminal real power of the two-level converter can be formulated as

$$P = \frac{3}{2}\omega_e \psi_m i_q \tag{A1.4}$$

Thus, q-axis current (i_q) can be derived as

$$i_q = \frac{2P}{3\omega_e \psi_m} \tag{A1.5}$$

Substitute (A1.5) into (A1.3), and the q-axis current (i_q) can be derived as

$$\begin{aligned} i_d &= \frac{\sqrt{\left(\frac{MV_{dc}}{2\omega_e}\right)^2 - \left(L_s \frac{2P}{3\omega_e \psi_m}\right)^2} - \psi_m}{L_s} \\ &= \sqrt{\left(\frac{MV_{dc}}{2L_s\omega_e}\right)^2 - \left(\frac{2P}{3\omega_e \psi_m}\right)^2} - \frac{\psi_m}{L_s} \end{aligned} \tag{A1.6}$$

Substitute (A1.5) and (A1.6) into (A1.2), the d- and q-axis voltages (v_d and v_q) can be obtained as

$$v_d = -\omega_e L_s i_q = -\frac{2L_s P}{3\psi_m} \tag{A1.7}$$

$$v_q = \omega_e L_s i_d + \omega_e \psi_m = \sqrt{\left(\frac{MV_{dc}}{2}\right)^2 - \left(\frac{2L_s P}{3\psi_m}\right)^2} \tag{A1.8}$$

In this sentence, the decrease of $I_{dc,1,0}$ is observed visually in Fig. 4.a. The author that such a decrease is difficult to be proved in mathematical way. In this paper, the harmonic on f_c ($i_{dc,1,0}$) has been derived as

$$i_{dc,1,0}(t) \approx \frac{f_0}{f_c} K_1 \frac{v_q i_d - v_d i_q}{\sqrt{v_d^2 + v_q^2}} \cos\left[2\pi f_c t + \theta_c - \frac{\pi}{2}\right] \tag{A1.9}$$

Substitute (A1.5) ~ (A1.8) into (A1.9) gives

$$\begin{aligned} I_{dc,1,0} &\approx \frac{f_0}{f_c} K_1 \frac{v_q i_d - v_d i_q}{\sqrt{v_d^2 + v_q^2}} \\ &= \frac{f_0}{f_c} K_1 \left(-\frac{MV_{dc}}{2\omega_e L_s} + \frac{\sqrt{9M^2\psi_m^2 V_{dc}^2 - 16P^2 L_s^2}}{3ML_s V_{dc}^2} \right) \end{aligned} \tag{A1.10}$$

where $I_{dc,1,0}$ is the magnitude of the DC-link harmonic in the frequency of f_c. If we increase the output power of the AC-DC converter (P), the term $\sqrt{9M^2\psi_m^2 V_{dc}^2 - 16P^2 L_s^2}$ in (A1.10) will decrease because of the minus symbol. Thus, $I_{dc,1,0}$ will show a decreasing trend when increasing the output power P.

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