PROTECTION OF LVDC NETWORKS INTEGRATING SMART TRANSFORMERS: THE CASE OF LV ENGINE FALKIRK TRIAL SITE

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Abstract

To enhance the adaptability of low voltage (LV) networks and release additional network capacity towards enabling the wider uptake of low carbon technologies, SP Energy Network's (SPEN) LV Engine project aims to design and trial the first UK solid state transformer (SST) for deployment within secondary substations (11/0.4kV). The trial site at Falkirk Stadium that is aimed to be completed in the near future will form the first LVDC trial at a utility scale in the UK. The SST and the introduction of low voltage DC (LVDC) supplies will present fundamental changes in the operation of existing secondary substations and will introduce new LV fault profiles for the associated LVDC distribution networks. This paper presents the results of joint work between the University of Strathclyde, SPEN and WSP with the primary objectives to understand the impact of SST deployment on the fault behaviour of LVDC networks and develop adequate protection strategies for LV Engine LVDC trial sites.

1 Introduction

The SPEN LV Engine project is an innovative project with the objective to exploit the enhanced functionalities offered by SSTs towards increasing network flexibility and releasing additional capacity within the LV network infrastructure [1]. The SST deployment will be trialled within five different schemes, two of which aim to provide LVDC supply mainly for rapid electric vehicle (EV) charging applications. The performance of these trials will be technically and financially compared with conventional secondary substations.

The trial site at Falkirk Stadium that is aimed to be completed in the near future will form the first LVDC trial by a distribution network operator (DNO) in the UK [2]. By virtue of their power electronic components, SSTs will have limited short-circuit capabilities, and their deployment, in addition to the introduction of LVDC, will fundamentally change the protection requirements of the associated distribution network [3]. The vast majority of existing LV distribution feeders in the UK are protected by simple fuse-based overcurrent protection. Adoption of the same approach in LVDC networks integrating SSTs is challenging as the limited fault current contributions of such converters are expected to render overcurrent protection less reliable [4]. Therefore, it is important to understand the impact of SST deployment on the fault behaviour and the protection strategies of LVDC distribution networks, and identify what arrangements need to be made to provide adequate protection with minimal cost impact and minimal disruption to protection arrangements already in place. This paper reports the findings of the protection studies carried out on the Falkirk LVDC network prior to SST deployment within the site, based on which a fit for purpose protection strategy is designed.

2 Falkirk Trial Network

2.1 LVDC Network Characteristics

A trial site selection process was undertaken by SPEN and WSP as part of the LV Engine project [5], through which an LVDC trial site has been identified and secured at the Falkirk Stadium, where development is currently taking place for providing rapid EV charging facilities. The Falkirk trial network aims to demonstrate the functionalities of LV Engine Scheme 4 [1], and will operate in a bipolar configuration with ± 475 VDC and will comprise of a 167 kVA SST, an ultra-rapid EV charger rated at 150 kW, and an LVDC feeder that interconnects the two main system components.

The Falkirk network will use a TN-S earthing arrangement with solidly earthed mid-point/neutral. An LVDC switchboard will be installed between the SST and the EV charger, which will comprise of an incoming circuit (connection with the SST) and one outgoing circuit (LVDC feeder connecting DC customers). The switchboard is planned to be fitted with DC Moulded Case Circuit Breakers (MCCBs) to provide a combined circuit breaker and disconnector function, along with undervoltage release (UVR) units for undervoltage protection. Moreover, for earth fault detection a DC earth fault leakage relay (EFLR) will be used. An electrical schematic for the entire LVDC substation is shown in Fig. 1.
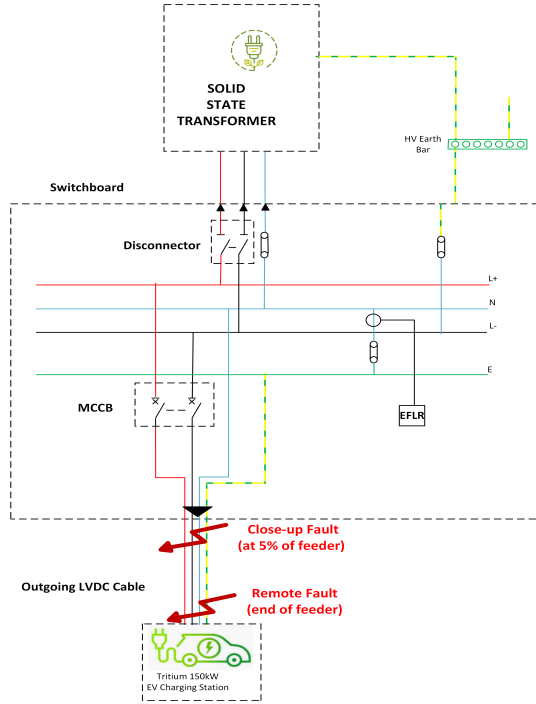
Fig. 1. Diagram of Falkirk trial network.

2.2 LVDC Network Modelling

In consultation with technology vendors, a representative model of the Falkirk network has been developed using the MATLAB/Simulink software platform. The complete model can be divided into four main components: the SST model, the EV charger model, the LVDC feeder model, and the model for the protection devices of the LVDC switchboard (accounting for the switch disconnector, the MCCB and the EFLR).

A representative behavioural model has been provided by the SST manufacturer, which encapsulates the required characteristics and functionalities of the SST which are of interest for carrying out LVDC fault studies. Considering the fast response of the power electronics-based converter and the high control bandwidth, both the detailed circuit and the control algorithms have been simplified for fast simulation speed. Pole voltages below 425 V and above 500 V trigger the undervoltage and overvoltage alarms respectively (incorporated in the model), and the SST shuts down. Furthermore, a representative EV charger model has been developed in which the module converter topology is represented by a single-phase phase shift converter [6]. The input and output filter arrangements and their parameters have been provided by the EV charger manufacturer. Overcurrent and/or undervoltage (between +/- supplies) alarms at the converter input are also included for the protection of the module in the event of faults. When any of these alarms is triggered, the charger is terminated within microseconds. For the $\pm$475 VDC circuit, a four-core SWA 185mm^2 stranded copper 0.6/1kV is planned to be installed for connecting the EV charger to the LVDC substation. The cable is represented by placing resistors and inductors in series to simulate the impedance of each feeder core. The technical characteristics

of the SST, EV charger and LVDC feeder are summarised in Table 1.

Table 1 Network component characteristics.

Component	Parameter	Value
SST	Power capacity	167 kW
	DC output voltage	$\pm$475V
	Output capacitance per pole	300 μF
	Maximum output current	185 A
	Undervoltage threshold	425 V
EV charger	Power capacity	150 kW
	Output voltage	425-500 V
	Input filter capacitor	840 μF
	Undervoltage threshold	760 V
DC feeder	Length	60 m
	Resistance	0.98 Ω/km
	Reactance	0.155 Ω/km

In the context of this study, all relevant DC MCCBs available from manufacturers that may be selected for supplying the LVDC switchboard have been considered. Indicative examples of commercially ready LV DC circuit breakers are the Tmax family of ABB [7] and the Compact NSX range of Schneider [8] that offer suitable MCCBs for DC applications providing both protection and isolation functions in DC circuits. Both MCCB families can be equipped with thermomagnetic trip units, which allow for protection against overloads with a thermal device based on thermal bimetallic strips, and protection against short-circuits using a magnetic device (overcurrent element). In addition, both breakers can be fitted with UVR units. The MCCBs satisfying the desired voltage/current ratings and the switchboard specifications [9] are the ABB Tmax T4V 250, and the Schneider NSX200 TM DC PV. The specifications of both MCCBs are cited in Table 2.

Table 2 MCCB characteristics.

Parameter	T4V 250	NSX 200
Rated voltage (U_n)	1000 V	1000 V
Current rating (I_n)	200 A	200 A
Thermal trip settings	70-100% of I_n	70-100% of I_n
Magnetic trip settings	5...10xI_n	5...10xI_n
Trip time (magnetic)	15 ms	< 20 ms
UVR opening threshold	35-70% of U_n	35-70% of U_n
UVR closing threshold	85% of U_n	85% of U_n
UVR response time	<30 ms	<50 ms

The complete MCCB model in MATLAB/Simulink comprises of the control and logic components for implementing the trip characteristics with freely adjustable settings, based on which a trip command is generated for triggering the isolation function of the MCCB. The trip characteristics have been obtained by the corresponding manufacturers' datasheets [7, 8] using graph scanning and data extraction software. The opening of the MCCB was modelled using ideal elements (switch,

resistor, diodes, and voltage sources) to represent the idealised (smothered) voltage waveform shown by the manufacturers.

The main purpose of the switch-disconnector in the Falkirk trial is to isolate the LVDC supply for any planned work within the substation, and it is not required to perform any protection functions or break a current in excess of the rated value. Therefore, for the conducted DC fault studies an ideal switch has been assumed for the modelling of this device. Finally, the function of the EFLR is achieved by measuring the earth-to-neutral link and generating an alarm signal when the selected residual operating current setting ($I\Delta n$) is exceeded (200 mA selected in these studies).

3 Falkirk Trial Network Fault Studies

The aim of the studies is to perform a DC fault characterisation of the LVDC system and use the findings to inform the LVDC strategy design process of potential issues that may arise by recommending/identifying potential solutions. In detail, the fault studies in this section will assess the behaviour of voltage and current over time for faults along the LVDC feeder (fault locations shown in Fig. 1), Moreover, the performance of the SST and the EV charger during DC faults will be reviewed. Pole-to-pole (PTP), pole-to-ground (PTG) and pole-to-neutral (PTN) DC faults are considered for the analysis. Faults at the customer side (EVs) are not investigated as during such faults the EV charger that is an isolated DC/DC converter topology, is terminated within microseconds and consequently, the rest of the network upstream of the charger is not affected.

Current traces are captured at the starting end of the LVDC feeder (at the MCCB location) for all cable poles. The positive, negative and neutral core currents of the cable are denoted as I_{L+}, I_{L-} and I_N, respectively. This point of measurement is selected in order to inspect the current traces observed by the MCCB during DC faults and to assess their impact on the MCCB protection logic. The system pole voltages are captured at the SST output and the corresponding positive and negative terminal voltages are denoted as V_{SST+}, and V_{SST-}. Furthermore, the input voltage of the EV charger (denoted as V_{EV}) is monitored, as well as the current flowing through the neutral-to-earth link to which the EFLR is attached (I_{earth}).

3.1 Pole-to-pole Faults

A fault between the two poles of an LVDC network is the most severe failure condition as in such a case all system converter smoothing capacitors are subjected to the fault resulting in the highest possible transient fault currents in both poles of the system. Therefore, PTP fault conditions need to be carefully examined in LVDC networks. The voltage and current traces for a solid PTP fault at the end of the LVDC feeder are shown in Fig. 2. The results show that the EV charger voltage collapses almost instantaneously, while although the fault is situated at maximum fault distance from the SST, the SST voltages fall rapidly below the undervoltage protection threshold leading to the SST shutting down its output.

Similarly, in Fig. 3, which illustrates the corresponding results for a solid PTP fault at 5% distance along the feeder (closer to the SST), the SST voltages fall below the 425 V threshold almost instantaneously followed by the collapse of EV charger voltage less than half a millisecond later. Collectively, these voltage signatures suggest that both the SST and EV charger are disconnected due to undervoltage protection very early in the fault stage for any PTP fault along the feeder.
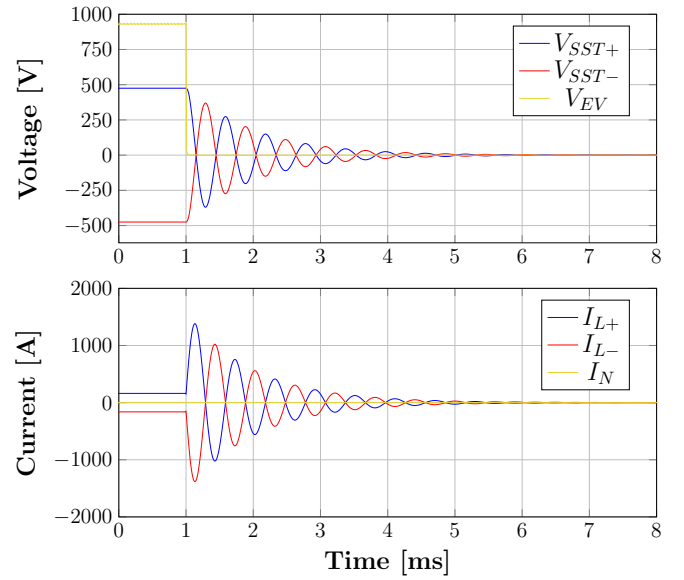

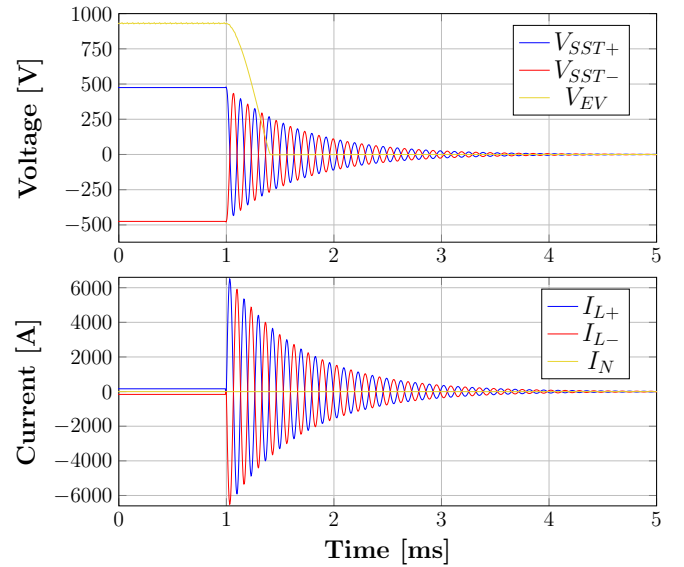Fig. 2 Voltage and current traces for a close-up solid PTP fault.

Fig. 3. Voltage and current traces for a remote solid PTP fault.

When the SST is disconnected, its current contribution is completely interrupted, and the system fault response is then dictated by the LVDC feeder and converter filter capacitors characteristics. The resulting RLC circuits lead to highly oscillatory behaviours in both voltages and currents as seen from

Fig. 2 and Fig. 3. For the close-up DC fault the oscillations become more prominent due to the smaller cable inductive components in the fault path. The peak transient current (same for both I_{L+} and I_{L-}) is equal to 6.48 kA and 1.38 kA for the remote and close-up fault, respectively. Such peak transient currents can theoretically exceed the magnetic trip threshold of the MCCB if the lower setting is applied (1 kA). However, in both cases the currents decay to zero within 4-6 ms.

3.2 Pole-to-ground Faults

In contrast to PTP faults that result in symmetrical fault voltage and current profiles, PTG faults lead to different fault signatures in each pole of the LVDC network. This can be observed in Fig. 4 that displays the system voltages and currents for a positive close-up PTG fault. The faulted positive pole voltage and current show similar trends with those observed for PTP faults, with both V_{SST+} and I_{L+} experiencing severe oscillations until they decay to zero within 4ms (with a 6.45kA fault current peak for I_{L+}). Current I_{L-} also exhibits an oscillatory behaviour but at a significantly lower frequency and magnitude than I_{L+}. Furthermore, there is an overvoltage in the healthy pole. Under these conditions, the part of the SST DC/DC stage regulating the positive pole voltage is disconnected based on its associated undervoltage protection, whereas the part of the SST DC/DC stage controlling the negative pole is disconnected due to its overvoltage protection.
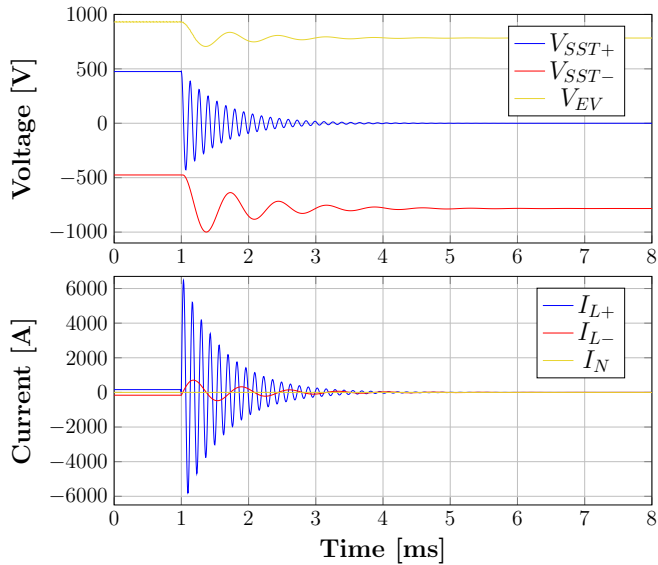

Fig. 4 Voltage and current traces for a close-up solid PTG fault.

Similar trends are observed for the remote PTG fault shown in Fig. 5 (1.37 kA peak current in this case). The above examples demonstrate that the voltage of the faulted pole of the system always collapses to zero. On this basis, use of under-voltage detection as the main protection element of the strategy has been confirmed as a suitable approach, as long as it is implemented for each pole separately in order to accommodate detection of PTG faults.
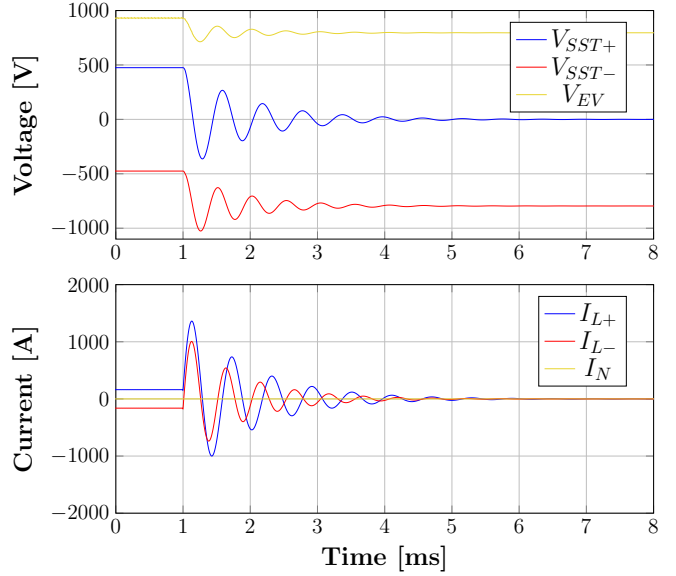

Fig. 5. Voltage and current traces for a remote solid PTG fault.

3.3 Pole-to-neutral Faults

The voltage and current waveforms for a solid positive PTN fault at the end of the LVDC feeder are illustrated in Fig. 6. The voltage profiles for both faults are virtually identical with those observed for PTG faults. In both cases, the faulted-pole voltage V_{SST+} collapses to zero and an overvoltage is presented on the healthy pole voltage V_{SST-}. The peak currents in the positive and negative poles are significantly smaller than the minimum possible overcurrent threshold of the MCCB (i.e., 1 kA). Furthermore, since there is no current flowing through the ground, the EFLR will not be able to detect PTN faults that may occur at any point in the network. Therefore, undervoltage protection is the only option for detecting PTN faults.
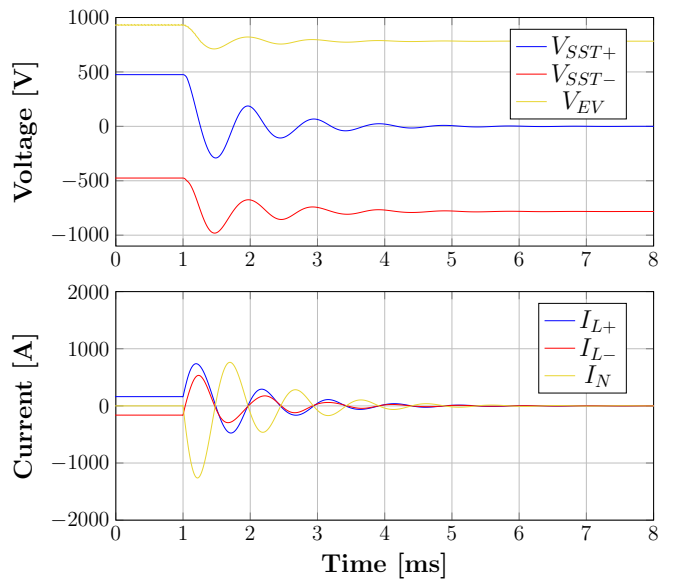

Fig. 6 Voltage and current waveforms during a solid PTN fault.

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3.4 Highly Resistive Faults

Fig. 7 illustrates the corresponding voltage and current traces for a resistive PTP fault at the end of the feeder. The fault resistance in this scenario has been set to 5 Ω, which corresponds to an amount of power consumed in the fault that is comparable to the maximum demand of the EV charger. For resistive DC faults, the rate of descent of converter voltages is more gradual, and during the early DC fault stage the converter attempts to regulate its output current by employing the constant current mode control. When the SST voltages hit the 425 V threshold, the converter is commanded to switch off causing a rapid decrease in currents I_{L+} and I_{L-}. The amplitude of current oscillations is much lower in this case due to the damping caused by the fault resistance. The observed collapse of SST voltages for both solid and resistive PTP faults suggests that the UVR unit is suitable to be used as the primary protection function for opening the MCCB in case of PTP faults.
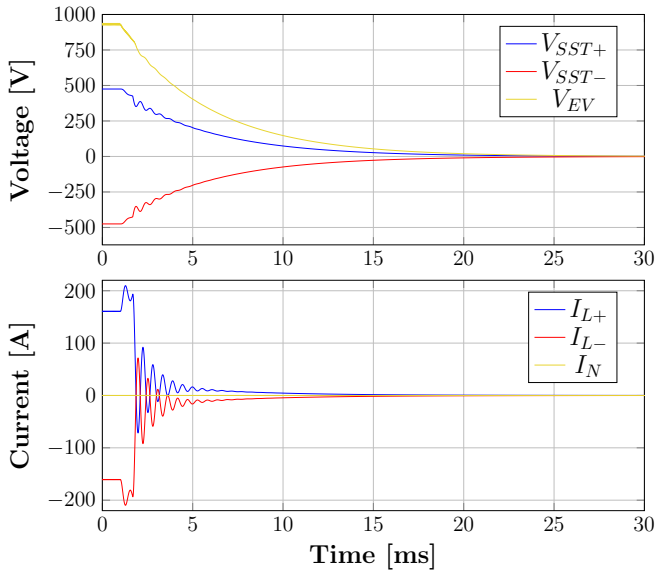

Fig. 7 Voltage and current traces for a remote highly resistive (5 Ω) PTP fault.

For the extreme scenario of a remote PTG fault with 20 Ω fault resistance (see Fig. 8), the undervoltage on the faulted pole is not adequate to trigger the SST undervoltage alarm. In fact, both SST pole voltages remain within the normal operation range and the converter retains its operation. The EV charger also retains its normal operation since it has a lower undervoltage protection threshold than the SST (the charger trips once the SST has tripped first). Eventually, both system converters converge to new operating points at reduced DC voltages. If only undervoltage is used as the main protection element, such high-resistance faults will not be detected. However, Fig. 8 shows that the earth current monitored by the earth fault relay can be in the range of several tens of amperes even for the 20 Ω resistive fault. This suggests that the EFLR can be used as a complementary means of PTG fault detection.
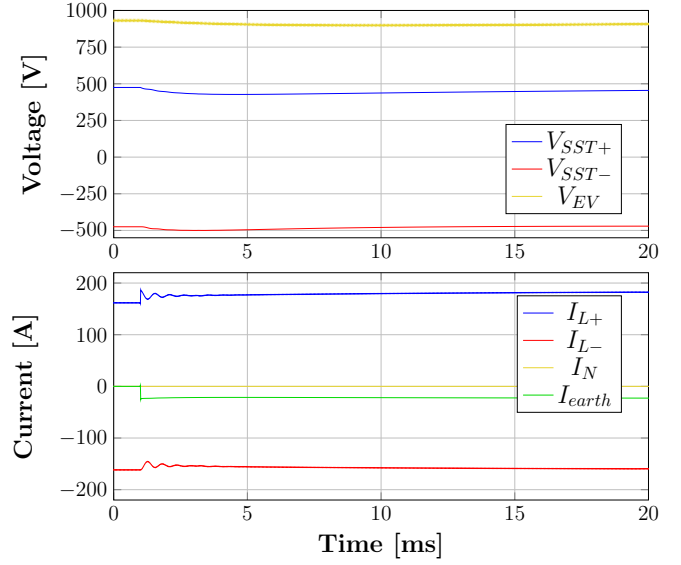

Fig. 8 Voltage and current traces for a remote highly resistive (20 Ω) PTG fault.

3.5 Discussion

Due to the current limiting capabilities of the SST, in most fault cases the peak fault current is not sustained for a sufficient period to guarantee tripping of the MCCB. Hence, overcurrent protection is not appropriate to be used as the main element of the protection strategy, but it is suggested to be included as an additional backup layer of protection and for protecting the power electronic components of the SST against high current stresses in case of converter malfunction. To achieve this, the lowest possible overcurrent setting can be used for the selected MCCB to be placed in the outgoing circuit of the switchboard.

Based on the voltage waveforms observed for solid and resistive PTG/PTN faults, it is evident that undervoltage is always presented on the faulted pole. Nevertheless, the full pole-to-pole system voltage during low-resistance PTG faults will remain very high and above the opening threshold of the UVR unit (0.7 p.u. or 665 V). Consequently, to ensure the effective operation of the UVR, both pole voltages should be measured, and the 0.7 p.u. threshold should be enforced on each pole voltage individually (equivalent to 332.5 V threshold). Owing to its higher undervoltage protection threshold (425 V), the SST trips first before the UVR opening threshold is violated. Once DC voltage controllability of the SST is completely lost, the voltage of the faulted pole drops further and activates the UVR.

4 LVDC Protection Strategy

An flow diagram of the proposed LVDC protection strategy for the Falkirk trial site is shown in Fig. 9. Building on the outcomes of the fault studies, the primary protection consists of undervoltage detection achieved through the UVR unit, and the overcurrent protection offered by the MCCB. When any of the SST voltages falls below the undervoltage threshold as a result of a DC fault on the LVDC network, the SST will temporarily

shut off its LVDC output causing the faulted pole voltage to collapse and the UVR trip coil to release and trip the MCCB. The overcurrent element of the MCCB further supports primary protection and ensures SST protection and faster fault isolation for more severe faults with increased fault current levels. The EFLR acts as complementary protection for less severe faults that may not be detected by the primary protection. This is achieved by sending a trip signal from the EFLR to the control systems of the SST when the residual operating current is exceeded, indicating that an earth fault condition has been detected, and resulting in the SST shutting down its output.
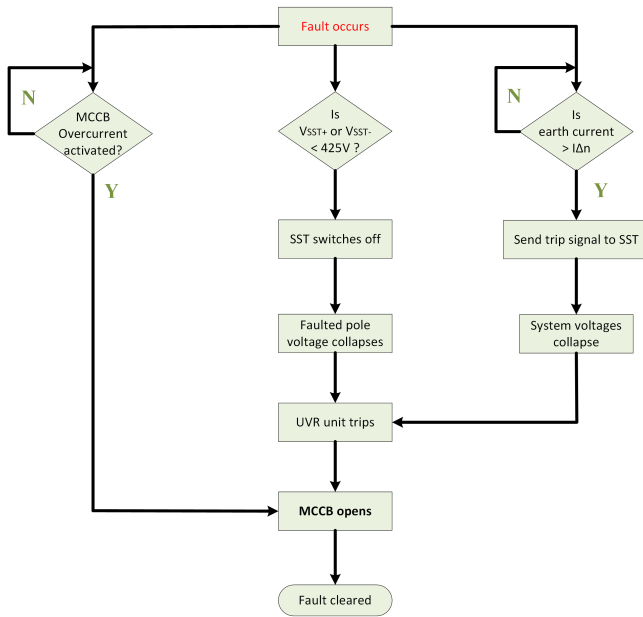

Fig. 9. Flowchart of the LVDC protection strategy.

The LVDC protection strategy also includes a DC fault discrimination stage (not shown in Fig. 9), which aims to determine the faulted zone (LVDC feeder or LVDC switchboard) after the MCCB has opened through its protection functions. This is achieved by ramping up the SST voltages to check if a current is observed on the SST output. This will indicate whether the fault is situated upstream or downstream of the MCCB. In the former case, the SST output current should be zero, while in the latter a fault current should be presented on the output. To execute this action, it is not necessary for the SST to ramp-up directly to full voltage. Instead, ramping up to a voltage value within the Extra Low Voltage (ELV) region (<50V) as defined in [10] is initially performed. If a fault current is not seen on the output, then the SST can continue ramping up the DC voltage to the nominal system voltage.

5 Conclusion

This paper has presented the main findings of the protection study for the LV Engine LVDC trial network that will be deployed at the Falkirk Stadium. The SST, EV charger, LVDC feeder and protection equipment comprising the LVDC network have been implemented within a representative model

and several fault studies have been conducted to firstly analyse and understand the fault response of the Falkirk LVDC network, and secondly to develop a fit-for-purpose and industry approved protection strategy, which can be replicated for similar future applications. The LVDC protection strategy proposed for the Falkirk trial network may operate in two main steps: a) main protection and b) DC fault discrimination. Apart from the inherent MCCB overcurrent protection, the main protection primarily uses the undervoltage shunt release coil to directly trip the MCCB if any of the two pole voltages falls below the UVR threshold. UVR protection can be successfully used to detect PTP faults as well as PTG/PTN low-resistance faults. Backup protection is provided by the earth fault relay, which can detect high-resistance PTG faults. Finally, the DC fault discrimination process achieved by restarting the SST to an extra low voltage level, assists the identification of the zone in which the DC fault has occurred.

6 Acknowledgements

7 References

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