Thermo-optic phase shifters for integrated photonics at low temperatures

Gerardo E. Villarreal Garcia

A dissertation submitted to the University of Bristol in accordance with the requirements for award of the degree of Doctor of Philosophy in the Faculty of Science.

.

November 2017

Abstract

Quantum information processing can provide tools to tackle problems beyond the capacity of classical computers, sensors and communication systems. Quantum photonics is one of the most promising quantum technologies that aim to implement systems that harness the quantum mechanical properties of nature. Such technologies can be implemented using photonic integrated circuits, a scalable solution compatible with the long-established CMOS fabrication technologies that benefit from developing telecommunication applications.

The maturity level of silicon photonic technology offers vast libraries of standard components that can be used to design integrated quantum photonic devices. Single-photon detectors (SPD) are the only critical component essential for any quantum photonic device that is not readily available yet. SPDs based on superconducting nanowires offer the best performance currently and can be integrated into photonic devices but require operation temperatures below 4K. This conflicts with another essential building block, optical phase-shifters, used for routing single photons in the circuits that introduce local temperature shifts of several hundred degrees Kelvin.

This thesis studies the viability of the operation of thermo-optic phase shifters in cryogenic environments. It analyses the optical and electrical properties of matter in a range of temperatures and the combined effect of the specific heat with the thermo-optic coefficient. It presents simulation results on integrated photonic devices' electrical and optical properties. It also presents measurement protocols for low-temperature characterisation using different cryogenic systems. Finally, it shows that standard

thermo-optic phase-shifters can be used at low temperatures with a slight increase ($< 10\%$) in power consumption. This validates the route towards the scalability of integrated quantum photonic systems.

Acknowledgements

I would like to thank Dr. Damien Bonneau for his support on the design of the integrated circuit used for the collection of experimental data, to Dr. Pisu Jian for helping with the deposition of additional contact pads required for the electro-optical measurements. This research was funded the Consejo Nacional de Ciencia y Tecnologia (CONACYT, CVU:409778).

Author's Declaration

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

SIGNED:..... DATE:.....

Contents

1 Introduction **15**

1.1 Quantum Information and Quantum Computing 15

1.2 Photonic Quantum Computing 19

1.3 Silicon Integrated Photonics 20

1.4 Superconducting Single Photon Detectors 21

1.5 Silicon's Thermo-Optic Coefficient 24

2 Theory and Methods **27**

2.1 Silicon-on-Insulator platform 27

2.1.1 Waveguides 28

2.1.2 Grating couplers 29

2.1.3 Phase shifters 30

2.2 Matter at low temperature 31

2.2.1 Specific heat 31

2.2.2 Thermal expansion 34

2.2.3 Thermal conductivity 34

2.2.4 Electrical conductivity 37

2.3 Electrical properties of semiconductors at low temperatures 38
2.3.1 Electrical conductivity 38
2.3.2 Band gap 39
2.3.3 Density of states 40
2.3.4 Carrier density 43
2.3.5 Mobility models 46
2.4 Experimental set-up 54
2.4.1 Variable Temperature Insert 55
2.4.2 Sample Stage 59
2.4.3 Cryogenic Probe Station 62

3 Multiphysics Simulations **68**

3.1 Introduction to COMSOL 68
3.2 Mesh convergence 70
3.3 Thermal phase shifter at cryogenic temperatures 71
3.3.1 Description of the geometry 72
3.3.2 Boundary conditions 74
3.3.3 Results 76
3.3.4 Discussion 87
3.4 Thermal contraction of optical/electrical probe holder 89
3.4.1 Description of the geometry 91
3.4.2 Boundary Conditions 93
3.4.3 Results 94

4 Thermal phase shifters in a cryogenic environment **96**

4.1 Mask design 97

4.2 VTI electrical connections 97

4.3 Experimental data 99

4.3.1 Frequency response 99

4.3.2 Resistance measurement and doping level estimation 100

4.3.3 Optical characterization 104

4.4 Discussion 107

5 Conclusions and outlook **111**

List of Figures

1.1 Nonlinear effects used for single photon generation in centrosymmetric (SPDC) and non-centrosymmetric media (SFWM) 21

1.2 Thermo-optic coefficient for silicon and silica measured between 5 K and 300 K. Data extracted from work published by Komma 25

2.1 Cross-sections of a collection of SOI waveguides. 29

2.2 Temperature dependency of silicon's band gap using model proposed by Green [66]. 40

2.3 Temperature dependence of density of states effective mass of electrons and holes in intrinsic silicon [66] 42

2.4 **a)** Intrinsic silicon lattice **b)** Silicon lattice doped with n-type impurities (Phosphorus), providing additional electrons **c)** Silicon lattice doped with p-type impurities (Boron) increasing the number of potential holes in the system. 45

2.5 Temperature-dependent carrier density function (Eq. 2.30) for a p-type non-degenerate semiconductor doped with an impurity density $Na = 4 \times 10^{15}\,\mathrm{cm}^{-3}$. 46

2.6 Logarithm of the hole mobility contribution due to scattering by the lattice 49

2.7 Logarithm of the hole mobility contribution due to scattering with major impurities (acceptors). 50

2.8 Logarithm of the hole mobility contribution due to minor impurities (donors). 52

2.9 Logarithm of the electron-hole scattering contribution to mobility. 53

2.10 Diagram of silicon lattice for a **a)** low and **b)** high impurity density. Carriers moving through a lattice like in b) would not "observe" three impurity atoms with a single hole each, but a bigger cluster with three times the electrical charge. 54

2.11 a) Diagram of the liquid He Crogenic® dewar. b)Radiation shield used to reduce evaporation of liquid He bath inside the dewar. The central orifice allows the VTI to go through down to the bottom of the dewar, the other three were designed to fit the electrical connections of the heater at the bottom of the dewar, the He level meter and to fit the transfer line used during liquid He transfers. 56

2.12 a) Cross-section of the vacuum chamber and how the indium seal is applied around the inside groove. b) Cracks in the indium seal can be avoided by cutting the indium wire in diagonal at both ends in such a way that they approximately form a complete ring that keeps its shape when a uniform vertical force is applied. 57

2.13 Sample holder used for cryogenic tests using the variable temperature insert. The DUT is connected to the PCB via wire bonding. The sample stage is separated from the 1k-pot by a low thermally conductive rod made of G10. A heater made of nichrome was installed under the sample stage as excitation for the temperature controller. 58

2.14 Sample stage for optical and electrical characterization of PICs in the VTI. 61

2.15 a) VGA's front view. b) VGA's top and lateral view. (images are not to scale). 62

2.16 Diagram of the Lake Shore® Probe Station for characterization of PICs in a cryogenic environment. The probe shown in the figure is a single DC electrical problem, although a similar arrangement is present for different kind of probes. 63

2.17 Diagram of the circulation lines for the liquid cryogen (either liquid helium or liquid nitrogen). Image extracted from Lake Shore® Cryotronics's documentation. 65

2.18 Cryogenic Probe Station (CPX) used for the optical and electrical characterization of integrated photonics circuits at cryogenic temperatures . 66

3.1 a) Waveguide's effective refractive index at 1550 nm and T= 293 K as a function of the number of mesh elements used in the parametric sweep b) Magnitude of the relative difference of the effective refractive index for every number of mesh elements and the value obtained for a mesh with maximum resolution 72

3.2 Geometry #1 with a single heater deposited on top of a waveguide. 73

3.3 Geometry #2 with two heaters at both sides of the waveguide. 74

3.4 **a)** Specific heat and **b)** thermal conductivity for materials used in mutiphysics simulation. Figure **c)** shows the ratios between silicon and silica for both their specific heats and thermal conductivities as a function of temperature. **d)** Thermal expansion coefficient for some relevant materials. Data extracted from [61, 78–82]. 75

3.5 Temperature profile $\Delta T = T - T_0$ for Geometry #1 at $T_0 = 4\,\mathrm{K}$ and $T_0 = 300\,\mathrm{K}$ in the **a)** xy-plane underneath the heater at z=110 nm above the BOX layer and **b)** in the xz-plane at the middle of the waveguide and the heater. 77

3.6 Temperature increase profiles in the **a)** transversal and **b)** longitudinal direction for a silicon waveguide in a SOI wafer for using a thermal phase shifter dissipating 1mW of heat. Points in **c)** shows a comparison between profile widths in both directions. 79

3.7 COMSOL simulation of the change in effective refractive index for a 500 by 220 µm^2 SOI waveguide at 1550 nm assuming a change in refractive index due to the thermo-optic effect and thermal expansion of the silicon structure. The inset shows the difference (in %) in n_{eff} due to the contribution of the thermal expansion. 80

3.8 Temperature-dependent refractive index for silicon and silica at 1550 nm obtained from [51]. 81

3.9 Temperature profiles in the **a)** transversal and **b)** longitudinal direction at $T_0 = 4\,\text{K}$ for different dissipated powers by the heater. Points in **c)** shows a comparison between profile widths in both directions. 83

3.10 Change in refractive index for Si and SiO2 as a function of temperature with respect to their value at room temperature. A similar function for the corresponding effective refractive index is also shown. Curves were calculated from data points in [51] 84

3.11 **a)**Accumulated phase-shift (in π-rad) along the 500 μm silicon waveguide for powers dissipated by the thermal modulator from 1 mW to 60 mW. **b)** P_π^{4K}=49.46 mW at $T_0 = 4\,\text{K}$, P_π^{300K}=24.03 mW at $T_0 = 300\,\text{K}$. 85

3.12 **a)** 2D visualization of the xy plane at a z-coordinate at the middle of the waveguide. **b)** Temperature distribution in the XZ plane at a y-coordinate at the middle of the waveguide and both thermal modulators which dissipate 10 µW. 86

3.13 **a)** Longitudinal and **b)** transversal temperature profiles for both geometries with a single and double heater, at 4 K and 300 K. 87

3.14 **a)** Accumulated phase-shift as a function of the power dissipated by the heat sources in both geometries. **b)** Power required to achieve a $\pi-$phase shift at $T_0 = 4\,\mathrm{K}$ and $T_0 = 300\,\mathrm{K}$ for both geometries 88

3.15 Variable temperature insert (VTI) and location of the sample stage for cryogenic characterization of photonic devices. 90

3.16 **a)** Sample stage designed for characterization of integrated devices in a variable temperature cryostat. **b)** Displacement if the fibre array due to thermal contraction. Variables to be estimated include displacement vector and change in the angle of incidence. 91

3.17 Three different variations of the arch that hold the fibre array. 92

3.18 Deformation components for Geometry #1 in x, y and z direction. 93

3.19 Deformation components for Geometry #2 in x, y and z direction. 93

3.20 Deformation components for Geometry #3 in x, y and z direction. 94

4.1 Integrated Mach-Zehnder interferometer used for the characterization of the highly doped silicon thermal phaser shifter. The set up has 6 I/O optical channels via grating couplers, two multi-mode interference structures and an additional waveguide connecting port 1 and 6 with a ring resonator, designed for a different experiment. 97

4.2 Microscope image (a) and mask layout (b) of the integrated MZI used in the experiment. 98

4.3 Diagram with connections and interfaces between the chip installed at 1K-pot and the manganin wires connected to the VTI's multi-DC port. A printed circuit board (PCB-01) with 40 fine-pitch contacts (100 µm) and a FFC connector serve as electrical interface with the wire bonding soldered to the AlCu contact pads. A second PCB (PCB-02) links the signal from PCB-01 with the manganin DC lines. 99

4.4 Frequency response of the VTI's electrical connections measured from the multi-DC connection through the 1.6 m 100

4.5 Resistivity of p-type silicon as a function of the impurity density at room temperature (line). The spot shows the experimental value for resistivity measured at the heater at room temperature. Interpolated data points from [93] 101

4.6 Numerical simulations in COMSOL of the carrier density, total hole mobility and resistivity for p-type silicon with a impurity level of $4.95 \times 10^{19}\,\mathrm{cm}^{-3}$, according to theory presented in Sec. 4.6, for the silicon strip heaters. . . . 102

4.7 Resistance measured at the heater with respect to the temperature measured at the VTI'S 1K-pot. 103

4.8 Silicon heater's resistance measured by 4-probe technique in the cryogenic probe station for a range of input powers from 0 to 160 mW. 104

4.9 Extended contact pads added in in-house post-process lithography by Dr. Pisu Jiang to allow the electrical probes and fibre array get to their probing/coupling position. 105

4.10 **a)** Transmission scan on an integrated MZI between port 1 and port 4 (Fig.s 4.1) as a function of the power dissipated by the thermal phase shifter for different base temperatures ranging from 10 K to 260 K **b)** Dissipated power required to obtain a π-phase shift in the MZI interference pattern. 108

List of Tables

1.1 Examples of quantum gates to perform operations on one (2-by-2 matrices) and two qubits that can form a set for universal quantum computation. . . 18

2.1 Sommerfeld constant and Fermi temperature for some relevant materials [61, 62]. 33

2.2 Parameters required to calculate the density of states effective masses. Transversal and longitudinal electron effective mass extracted from [66]. . . 43

2.3 Parameters for lattice and majority carriers scattering models 48

2.4 Numerical values for the constants s_i in equation 2.41 and r_i in equation 2.44 51

3.1 Maximum and minimum limits for the variation of mesh elements setting for all the domains in the geometry 71

3.2 Results of simulation of thermal expansion in COMSOL Multiphysics for all the different arch geometries simulated in this section. The result with the smaller deformation for each category is written in **bold**. 94

Chapter 1

Introduction

1.1 Quantum Information and Quantum Computing

The invention of the transistor and the later appearance and popularisation of modern computers gave us new tools to create new technologies, enabling access to new knowledge and innovation. These tools became essential in our constant quest for answering fundamental questions about our universe.

After a few decades of constant development, the increase in the processing power of modern computers has followed the trend predicted by Intel's co-founder Gordon Moore. Moore's Law states that the number of transistors per square inch would be doubled every two years. The increase in the number of operations that a processor can handle is partly determined by the number of transistors it contains and scales with the degree of miniaturisation provided by the available technology. However, the miniaturisation process can not continue indefinitely without technological and fundamental obstacles, firstly due to available fabrication techniques, and secondly due to the quantum mechanical nature of electrons, i.e. electrical currents can not be completely confined by the structures inside the processor because of quantum tunnelling. The fabrication issue might be overcome since there is a possibility that said technological problems could be solved at some point in the

future. However, the quantum mechanical nature of electrons establishes a fundamental limit to the size of any component. Anticipating this scenario, chip manufacturers study new materials that can extend the boundaries of what we can call *classical computers* [1].

How can we keep pushing the limits of what is technologically possible when the barrier to overcome is the very quantum mechanical nature of matter? The answer is that new computing paradigms need to be explored, paradigms that allow us to continue with the trend of producing more and more powerful processors and enable new functionalities other than the increase of operating speed. Optical and DNA computing, together with spin electronics-based technology, are just a few examples of new branches in computing science that are looking to bring a new technological revolution. A strong competitor in this race is quantum computing, which exploits and harnesses the properties of quantum mechanical systems, such as superposition and entanglement, in order to perform operations on data and solve computational problems [2].

While a classical computer encodes information using "macroscopic" observables, a quantum computer uses microscopic systems that can exist in a superposition of at least two different states. Unlike classical computers, where the information is encoded in 0s and 1s, also known as bits, quantum computers encode their information in quantum bits, or qubits, which can exist in a linear superposition of two states:

$$|\psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle \tag{1.1}$$

where α and β are complex numbers representing the probability amplitude for the system to be observed in the state $|0\rangle$ or $|1\rangle$ respectively. The set of states $\{|0\rangle, |1\rangle\}$ is known as *computational basis*. These states are orthonormal to each other and can be defined by a two-state quantum system such as an electron through its spin (up $|\uparrow\rangle$ and down $|\downarrow\rangle$) or the polarization of a photon (vertical $|V\rangle$ and horizontal $|H\rangle$). Both states form a complete basis and the state $|\phi\rangle$ must comply with the normalization condition $|\alpha|^2 + |\beta|^2 = 1$. The

state $|\phi\rangle$ is usually represented in its matrix form as:

$$\alpha\,|0\rangle + \beta\,|1\rangle = \begin{bmatrix} \alpha \\ \beta \end{bmatrix}$$

In classical computing, operations on bits are performed through logical gates such as ANDs, ORs, or NANDs. This last one is known as a universal gate since any other logic gate can be constructed from a combination of NAND gates. A universal set of quantum gates, on the other hand, requires arbitrary single-qubit control gates and at least one non-trivial two-qubit gate (Table. 1.1).

A quantum computer can be classified in different categories based on the way the quantum system processes information: quantum annealers, analogue quantum computers and fault-tolerant universal quantum computers [3]. Quantum annealers are the most restrictive implementation of a quantum computer since they are designed to solve specific optimisation problems, showing no particular advantage with respect to classical computing [4]. Analogue quantum computers will simulate many-body quantum systems, just as Richard Feynman once proposed in 1982, and implement their Hamiltonian. On the other side, fault-tolerant universal quantum computers are the most powerful and broadly applicable kind of quantum computer, with the potential of being fully reconfigurable and capable of implementing any type of algorithm.

Regardless of the kind of physical system chosen for the implementation of the components required for universal quantum computing, a set of minimum requirements need to be fulfilled according to the work presented by DiVincenzo in 2000 [5], known as DiVincenzo's criteria:

1. Scalable physical system with "well characterised" qubits.
2. The ability to initialise a qubit to a known reproducible state.
3. Decoherence times longer than gate operation times.

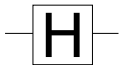
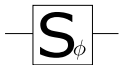
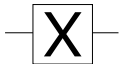
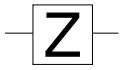
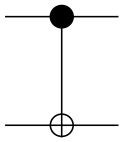
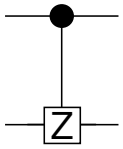
Quantum gate	Circuit block	Transformation matrix
Hadamard		$\frac{1}{\sqrt{2}}\begin{bmatrix}1 & 1\\ 1 & -1\end{bmatrix}$
Phase		$\begin{bmatrix}1 & 0\\ 0 & e^{i\phi}\end{bmatrix}$
Pauli-X		$\begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix}$
Pauli-Y		$\begin{bmatrix}0 & -i\\ i & 0\end{bmatrix}$
Pauli-Z		$\begin{bmatrix}1 & 0\\ 0 & -1\end{bmatrix}$
Controlled-NOT		$\begin{bmatrix}1 & 0 & 0 & 0\\ 0 & 1 & 0 & 0\\ 0 & 0 & 0 & 1\\ 0 & 0 & 1 & 0\end{bmatrix}$
Controlled-Z		$\begin{bmatrix}1 & 0 & 0 & 0\\ 0 & 1 & 0 & 0\\ 0 & 0 & 1 & 0\\ 0 & 0 & 0 & -1\end{bmatrix}$

Table 1.1: Examples of quantum gates to perform operations on one (2-by-2 matrices) and two qubits that can form a set for universal quantum computation.

4. A universal set of quantum gates.

5. An effective way of measuring the qubit's final states.

1.2 Photonic Quantum Computing

Nowadays, several platforms have shown progress in the process of developing the components and conditions required for the implementation of quantum technologies, e.g. superconducting qubits [6], quantum dots [7], dopants in Si [8], ion traps [9], optomechanical [10], nuclear spin in nitrogen-vacancies [11], photonics [12], etc. On one side, due to the strong interaction between matter-based qubits such as trapped ions or quantum dots, quantum gates are relatively easy to implement. Nonetheless, they are difficult to isolate from the environment, which leads to decoherence.

On the other side, the matured developed field of quantum optics, and the scarce interaction of photons with the environment and their compatibility with current telecommunication technologies make photonics an ideal candidate for QIP applications. Manipulation of photons by using linear optics components results in easily realisable single-qubit quantum gates, enabling information to be encoded in different degrees of freedom such as polarisation, time bin, or path [13].

Photons interact weakly with the environment but do with other photons, which represents a significant challenge for realising two-qubit quantum gates, e.g. the CNOT gate. Nonetheless, this restriction was circumvented in 2001 by Knill, Laflamme and Milburn, who showed that such interaction could be induced by making projective measurements using ancilla photons [14], which opened up the way for the implementation of quantum gates using only single-photon sources, single-photon detectors and beam splitters.

As the number of input qubits and quantum gates increases, the number of optical components becomes large enough to be unpractical in terms of phase stability and losses, reasons why the use of integrated photonics has attracted attention in the past few

years [15].

1.3 Silicon Integrated Photonics

Information processing using photonic integrated circuits (PIC) provides additional advantages with respect to bulk optics in terms of system stability and scalability. Single-photon generation in bulk optics, for example, uses expensive nonlinear crystals that need to be carefully aligned and thermally stabilised. On the other hand, in the case of PICs, single photons can be simply generated along the waveguide, which is possible due to the high confinement of the electric field inside the structure and the optical nonlinearity of the waveguide material.

Integrated photonic components for quantum photonic applications are currently being fabricated using different platforms such as: InP [16], GaAs [17], Ge-doped SiO_2 [18], Si_4N_3 [19], $LiNbO_3$ [20] and Silicon-On-Insulator (SOI) [21]. Among those alternatives, silicon-based platforms have the advantage of being compatible with CMOS fabrication technology, which has the perk of being supported by decades of investment in R&D by the microelectronics industry. [22]. Furthermore, silicon has some regions of transparency in its absorption spectrum, one of them in particular known as *telecom band* or *C-band*, covers wavelengths between 1530 nm and 1565 nm, a spectral range that coincides with silica's transmission peak and best performance of erbium-doped fibre amplifiers [23]. This makes silicon compatible with fibre optic telecommunication technology.

Since silicon is a centrosymmetric material, it shows no second-order nonlinear effects (χ^2) like SPDC or the electro-optic effect [24] which is often used as a modulation mechanism. Nonetheless, silicon does possess strong third-order nonlinearities (χ^3), including the Kerr effect, which produces self-phase modulation [25] and cross-phase modulation [26], and could even play a role in generating an induced χ^2 effect according to recent studies [27]. Additionally, parametric processes such as spontaneous four-wave mixing (SFWM) have been used successfully for heralded single-photon generation (see Fig.

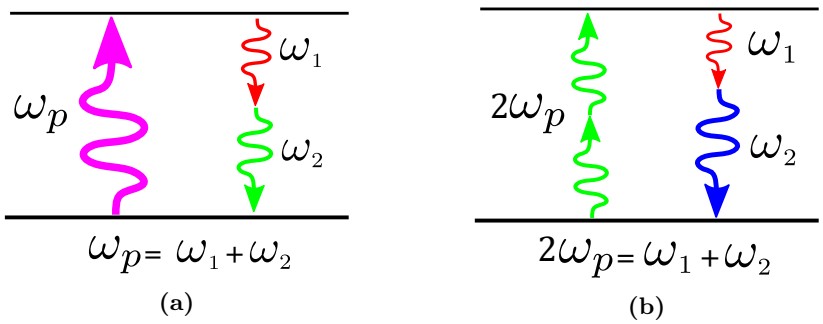


Figure 1.1: Nonlinear effects used for single photon generation in centrosymmetric (SPDC) and non-centrosymmetric media (SFWM)

1.1) [28].

The platform used to fabricate integrated silicon photonics is commonly known as "silicon-on-insulator" (SOI). SOI wafers consist of a ∼725 µm silicon substrate, 2 µm of buried oxide (BOX) for minimising parasitic capacitance between electrical connections and the substrate, and 220 nm of crystalline silicon. This has become the standard for photonic semiconductor foundries, although other thickness combinations are also used [29].

Both the BOX and cladding layers are formed of silicon oxide (silica SiO_2). Silicon and silica are not only compatible in terms of fabrication technology and wavelength operation but also have a high index contrast, which gives the potential to fabricate sub-micron waveguides, which leads to a higher component density with respect to other platforms, reducing the device footprint [30].

1.4 Superconducting Single Photon Detectors

The last building block required for a universal photonic quantum computer is a scalable technology for single-photon detection. An effective way of measuring the presence of a single photon requires a technology that allows high detection efficiencies, low timing jitter, low dead time, and in this particular case, a technology compatible with the integration of silicon photonics [31].

Efficiency is simply defined as the probability that a signal is generated in the presence

of a single photon. Nonetheless, the system efficiency η can usually be decomposed in other efficiencies that describe different subsections of the detection apparatus [31]:

$$\eta = \eta_{\text{loss}}\eta_{\text{abs}}\eta_{\text{det}} \tag{1.2}$$

where η is the system detection efficiency, η_{loss} is the coupling efficiency into the single-photon detector's (SPD) input, η_{abs} is the probability of absorption, and η_{det} is the *quantum efficiency*, which is the probability that an absorption event triggers a measurable signal heralding the presence of a single photon.

The dark count rate (DCR), the rate of *clicks* triggered without an absorption event, is typically measured in Hz. The timing jitter is the uncertainty or expected error between an absorption event and its corresponding click. The recovery time, or dead time, represents the time it takes the SPD to recover from a detection event and be ready for the next one. An additional desirable characteristic is a photon-number resolution that determines the number of photons in the multi-photon state that triggered the click.

Among the technologies currently available or under development for single-photon detection, four will be highlighted and briefly described: photomultipliers tubes (PMT), single-photon avalanche photodiodes (SPAD), transition-edge sensors (TES), and superconducting nanowire single-photon detectors (SNSPDs). Extensive reviews and descriptions of the properties and applications of these technologies can be found in the literature [31, 32].

Both PMTs and SPADs rely on creating a later amplified electrical current triggered by an initial electron excited by photon absorption, resulting in small SDEs, particularly for low energy single photons.

PMTs are a long-established photon-counting technology, commercially available but with relative large active areas (diameters $> 10\,\text{mm}$) and are therefore not a scalable solution. Commercial PMTs offer efficiencies of $\sim$2% at 1550 nm with DCR of 200 kHz, although efficiencies as high as 40% can be obtained for shorter wavelengths [31], with a

fairly good counting rate of 10 MHz and low jitter in the order of 300 ps.

SPADs are P-N or P-I-N junctions operated with a reversed bias above the breakdown voltage, also known as Geiger mode. Carriers generated by photon absorption unleash an avalanche of carriers, amplifying the current and triggering a macroscopic breakdown of the diode junction [33]. SPADs offer low dark count rates (generally tens of Hz, but DCR at 1 Hz has been shown [34]), relatively low timing jitters (between tens and hundreds of ps) [35,36], high count rates (up to 100 MHz) at infrared wavelengths, and SDE up to 30% in InGaAs SPADs at 1550 nm [37].

A well known platform for SPADs in the range of wavelengths around 1550 nm is InGaAs/InP which has shown detection efficiencies above 55% [38], with DCR mostly due to tunnel-assisted generation of carriers in the absorption layer [35] and trap-assisted excitations [39]. Compared to other SPD alternatives, SPADs are characterised by lower power consumption and for being compatible with integrated technology, [40,41].

While SPADs may require refrigeration below room temperature to reduce thermally-assisted dark currents, their cooling system is not as expensive as technically specialised as what can be found in superconducting devices. Germanium, for instance, must be cooled down to liquid nitrogen temperatures ($\sim$ 77 K), but moderate cooling is enough for InGaAs/InP, which can operate between 150 K and 220 K.

Within the category of superconducting SPDs, two solutions are particularly important: TESes and SNSPDs. TESes are thermal sensors made of films of a superconducting material that operate at very low temperature (hundreds of µK) right at the edge between the superconducting and normal state so that a small change in temperature triggered by the absorption of a single photon creates an abrupt change in the resistance [42]. Since the output signal provided by the sensor is proportional to the heat absorbed, TESes can discriminate the number of photons, assuming a known wavelength [43]. SDEs as high as 95% at 1500 nm [44] has been demonstrated, nonetheless extremely low temperatures in the order of 100 µK are required for their operation. The timing jitter is relatively poor at around 100 ns at FWHM, and dead times around the

same order of magnitude limit their counting rate at about 100 kHz due to the reliability of the detection mechanism on thermal effects [31].

SNSPDs, on the other side, consist of nanowires made of thin films of a superconducting material, e.g. NbN or NbTiN. The nanowire operates below its critical temperature and is biased with a bias current just below its critical current. A simplified version of visualising the detection mechanism is thinking on the absorption of a single photon breaking Cooper pairs [45], creating a region of high-resistivity in a small region of the wire, which leads to the transition from the superconducting state to the normal state in the whole nanowire. SNSPDs offer not only high detection efficiencies and broad spectral photon sensitivity (from visible to mid-infrared) but also low jitter (tens of ps), low dark counts (~ 10 Hz), and unlike TES sensors, short dead times leading to high count rates up to ~ 1 GHz [31].

SNSPDs have the potential for being integrated on PICs. Integrated SNSPDs or Waveguide SNSPDs (WSNSPDs) are nanowires deposited on top of photonic waveguides. Due to the presence of a non-zero evanescent field outside the waveguide, there is a non-zero probability of single-photon absorption, which scales with the length of the nanowire and that can also be enhanced by the presence of a cavity [46, 47]. Fabrication compatibility between superconductor materials used in SNSPDs and integrated photonic platforms has been demonstrated for GaAs [48] and SOI using NbN films with detection efficiencies as high as 91% [49].

1.5 Silicon's Thermo-Optic Coefficient

SNSPDs and WSNSPDs require circuits to be kept at low temperatures. The goal of building more complex PICs with a scalable architecture that can send feedback to a set of reconfigurable quantum gates invites to weigh up the idea of having a fully integrated quantum processor, which would imply a complete set of photonic components (single-photon sources, switches, phase modulators, etc.) operating at cryogenic temperatures.

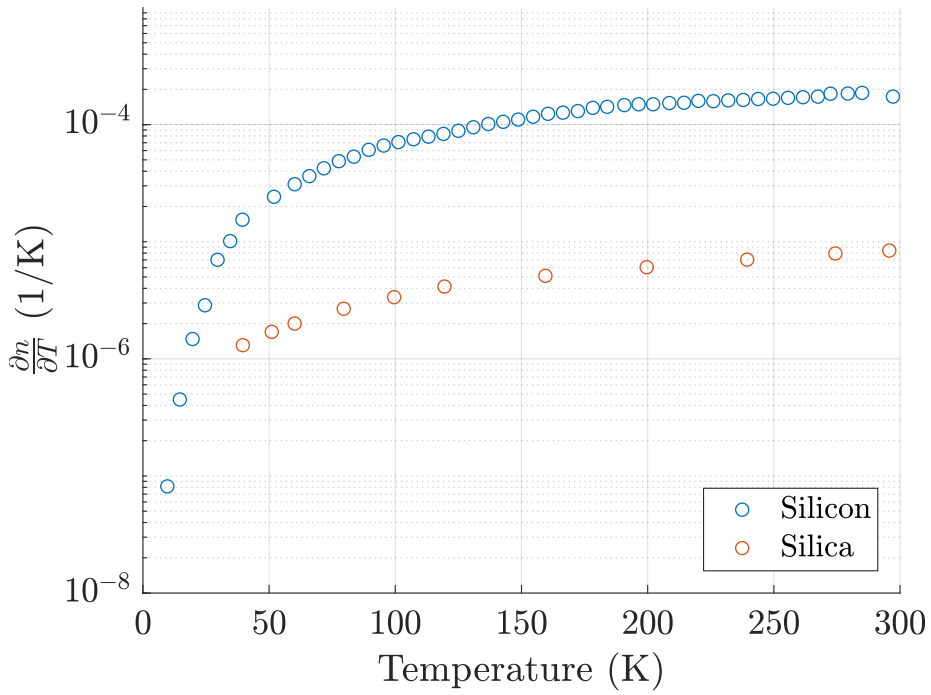


Figure 1.2: Thermo-optic coefficient for silicon and silica measured between 5 K and 300 K. Data extracted from work published by Komma et al. [51]

Material properties change with temperature: atoms' vibrations in a solid's lattice begin to fade, decreasing the effect of anharmonic corrections to the harmonic oscillator approximation [50]. The specific heat and thermal conductivity decrease with temperature as the number of available degrees of freedom declines and the heat transfer mechanisms become less effective.

The temperature dependence of silicon's refractive index, also known as the thermo-optic effect, is commonly used to modulate the optical path length in specific sections of waveguides using heat-dissipating structures. Silicon has a thermo-optic coefficient $\partial n/\partial T$ of $1.8 \times 10^{-4}\,\mathrm{K}^{-1}$ for 1550 nm at room temperature that decreases four orders of magnitude when $T \rightarrow 5\,\mathrm{K}$ [51] (see Fig. 1.2). This result raises questions regarding the viability of using heat-dissipating structures in PICs operating at cryogenic temperatures, particularly in structures such as optical phase shifters.

This work will characterise the performance of thermal phase shifters in an SOI chip

operating at cryogenic temperatures in order to study their viability as a building block for quantum information processing.

Chapter 2

Theory and Methods

In the previous chapter, silicon integrated photonics was presented as a robust candidate platform for a future fault-tolerant universal quantum computer. Likewise, it was mentioned that superconducting detectors are nowadays the best single-photon detection technology available that is also compatible with integration.

This chapter will introduce some key components of the silicon-on-insulator platform and how their material properties change when exposed to a cryogenic environment. It is an expected requirement if a fully integrated silicon-based quantum processor incorporates SNSPDs as detection technology. This chapter will also introduce the cryogenic equipment used to characterise integrated components.

2.1 Silicon-on-Insulator platform

Optical quantum information experiments can be constrained by the limitations of bulk optic components which are inherently non-scalable and a poor solution in terms of stability for situations when the system becomes large and complex [12]. This, by definition, limits the number of elements a system can utilise, such as beam splitters, mirrors, etc., and therefore defines its complexity [30]. It was until Politi et al. [15, 21] showed in 2008

that PICs could overcome said limitations by implementing integrated waveguide circuits, reducing the experiment's footprint, increasing their stability and gaining control of the optical path length more practically compared to bulk optics.

GaAs-, InP- and GaN-based materials have been the dominant platforms for semiconductor diode lasers since their first demonstration in 1962 due to their direct bandgap, leading to a faster and more efficient recombination process [52]. Nonetheless, the technology for fabricating PICs based on III-IV semiconductors is expensive compared to other alternatives such as silicon.

Silicon is not only backed by decades of investment in R&D, which has reduced its costs, but it also provides a transparent medium with low propagation loss. Silicon also offers high index contrast when it is used with silica, which decreases the circuits' footprint and allows for a more confined electric field inside sub-micron waveguides [53].

The Silicon-on-Insulator platform (SOI) is a well-established technology with components that benefit from recent developments in classical applications to be used in quantum photonics and quantum information processing experiments [54].

2.1.1 Waveguides

As it was mentioned in Sec. 1.3, high index contrast between silicon and silica allows the fabrication of sub-micron waveguides, with standard dimensions of typically 500 by 220 nm^2

Although other geometries are also used for different purposes, maximum confinement is achieved with rectangular strip waveguides. Rib waveguides, for example, provide extra space on both sides of the propagation channel for electrical connections on devices such as electro-optical modulators [29] and integrated photodetectors (Fig. 2.1). Typical losses of SOI strip waveguides available in commercial foundries are in the 2.5 dB/cm range [55]

The single-mode condition is met with this high index contrast (3.48/1.44) when the core's width is between 400 and 500nm. Because of the thickness of the SOI layer of 220 nm,

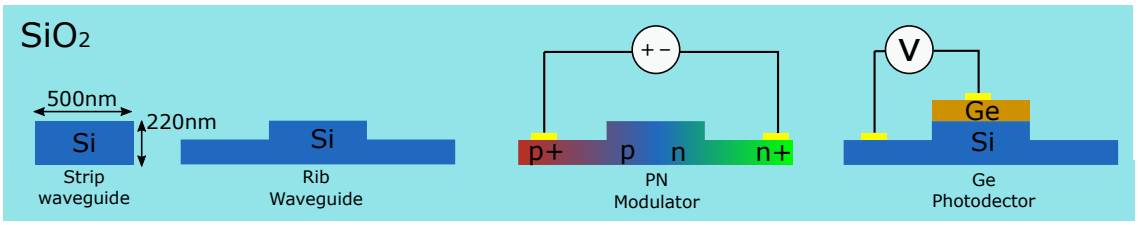


Figure 2.1: Cross-sections of a collection of SOI waveguides.

the core only supports one mode for each polarization (TE and TM). Single-mode operation is required to ensure good interference between different fields propagating through other waveguides [30].

A layer of buried oxide (BOX) with a thickness of 2 μm is required to reduce leakage and therefore reduce the propagation loss for both polarisations. However, TM's leakage is at least three orders of magnitude higher than TE's for 1 μm [56]. Even at this dimension, the core will support two modes, fundamental TE and TM, but TE tends to be more confined, and it is considered the truly fundamental mode.

Optical waveguides are dispersive, primarily because of geometry effects, since the dimensions of the waveguide are close to the value of the wavelengths used, so small changes in the geometry cause a significant change in the mode confinement [56].

2.1.2 Grating couplers

A grating coupler could be defined as a structure with a periodic refractive index modulation that allows free-space propagating light to be coupled and guided by a waveguide. This periodicity is typically achieved in silicon photonics by etching grooves in the silicon waveguide.

Fibre core diameters vary from 8 to 10 um gives an optical mode diameter in the order of 15 µm the mode into a waveguide of 500 nm by 220 nm. Although lensed fibres can be used, alignment requires sub-micron precision, which can definitely be found but increases the costs.

The grating coupler periodicity is designed to slightly mismatch the wavelength of the guided mode to avoid back-propagation caused by second-order diffraction [29]. Because of this mismatch, grating couplers are aligned at an angle θ between the chip's surface and the vertical. In order to get fibres as close as possible to the surface of the grating coupler, fibres and fibre arrays can be polished with an angle θ.

Grating couplers are compatible with SMF-28. They are ideal for wafer-scale testing, are easy to fabricate and show low facet reflections.

2.1.3 Phase shifters

Preparation of an initial path-encoded state or its manipulation to perform an operation using linear optics, require components that allow control of the relative phase difference between different spatial modes. The phase shift between two spatial modes is described in general by:

$$\Delta\phi = \frac{2\pi}{\lambda_0} \int_{\mathrm{x=0}}^{\mathrm{x=L}} \Delta n_{\mathrm{eff}}(x, T) dx \tag{2.1}$$

where $\Delta n_{\mathrm{eff}}(x, L)$ is the change in the effective refractive index in of the spatial modes, which is in general position- and temperature-dependent, L is the length where $\Delta n_{\mathrm{eff}}(x, L)$ is non-zero, and λ_0 is the wavelength of the traveling wave (or single photon) being delayed.

An integrated phase shifter changes the optical path length of a waveguide section by changing its effective refractive index. Silicon shows very weak electro-optic properties due to its centrosymmetric crystalline structure. Still, its refractive index can be tuned by changing its temperature [57] or its carrier concentration [58] in the case of impurity-doped silicon.

The main drawback of modulation by injection of free carriers is increasing the propagation losses due to free carrier absorption (FCA). Nevertheless, they rely on a a much faster mechanism compared to thermal effects, showing up to 70 Gbit/s [59].

2.2 Matter at low temperature

Cryogenic temperatures required for the operation of WSNSPDs impose an additional constraint in building a fully integrated universal reconfigurable quantum computer. Assuming that a cryogenic environment is needed to get good-performing integrated single-photon detectors, understanding how materials behave at low temperatures becomes essential not only to design experiments properly but also to modify photonics components so they behave correctly at this range of temperatures.

The first approach in the study of solids is using the harmonic approximation, where atoms in the crystalline lattice are approximated as perfect harmonic oscillators,

2.2.1 Specific heat

Heat capacity is an extensive property of a substance defined as the amount of energy necessary to increase its temperature in 1K of a certain amount of mass. Depending on whether the heat transfer occurs under constant volume or constant pressure, the heat capacity is defined as follows:

$$C_X = \left(\frac{\partial Q}{\partial T}\right)_X \tag{2.2}$$

where X=V,P for the heat capacity at constant volume and constant pressure, respectively, although an intensive property such as the specific heat, which is independent of the mass, is more convenient.

$$c_x = \frac{C_x}{m} \tag{2.3}$$

where x=v,p same as for the heat capacity. For gases, it makes sense to imagine how it could increase or decrease the pressure it exerts on the walls that contain it while keeping its volume constant. Still, for solids, a small temperature change comes with a change in volume due to thermal expansion, which imposes a huge demand on the strength of

the walls of the vessel [60]. Usually, when dealing with changes in temperature in solids, expansion or contraction happens without this kind of constraint, so c_p makes more sense to use. Furthermore, the relationship between c_v and c_p is:

$$c_p - c_v = \frac{\alpha^2 T}{\rho \kappa} \tag{2.4}$$

where α is the volumetric thermal expansion, ρ is the density, and κ is the isothermal compressibility. At low temperatures, as $T \to 0$, both specific heats approach the same value.

Changes in the thermal properties are significant because they allow refractive index modulation by changing its temperature.

The change in specific heat at low temperatures depends on the microscopic excitation mechanisms for every material. The more the degrees of freedom for the system to store energy, the larger the specific heat.

For non-magnetic, crystalline insulators, the excitations come from the lattice in the form of phonons [61].

$$C_{\text{ph}}(T) \propto \left(\frac{T}{\theta_D}\right)^3 \tag{2.5}$$

where θ_D is the Debye temperature.

Besides the lattice vibrations, conduction electrons also contribute to potentially excitable states for metals. The electronic contribution to the specific heat can be calculated using the "free-electron" model density of states $g_e(E)$ and the Fermi-Dirac distribution as the occupation function for the energy states. The electronic contribution to the specific heat is directly proportional to T [61]:

$$C_e(T) = \frac{\pi^2}{2} N_0 k_B \frac{T}{T_F} = \gamma T \tag{2.6}$$

where N_0 is the total number of electrons in the system, $T_F = E_F/k_B$ is the Fermi

Metal	γ [mJ mol^{-}1 K^{-}2]	$T_F[10^4\text{K}]$
Al	1.35	13.5
Cu	0.691	8.12
Nb	7.79	6.18

Table 2.1: Sommerfeld constant and Fermi temperature for some relevant materials [61, 62].

temperature, and γ is the Sommerfeld constant. Despite the good agreement between Eq. 2.6 and experimental data, electrons in metals are not entirely free and independent from each other. Still, they show some level of interaction that affects their effective masses.

$$C = \gamma T + \beta T^3 \tag{2.7}$$

On the other hand, superconductors experience a change in electronic specific heat when the temperature drops below their critical temperature. At the same time, their lattice contribution to c_p remains independent of the phase change. The electronic specific heat gets a boost when the system goes through a phase change, in this case, the superconducting transition. Below T_c, the electronic heat capacity decreases faster than it would do if the system continued at a non-superconducting state, following an exponentially decaying trend.

Finally, amorphous solids, which have no periodic crystalline structure, have a different degree of freedom which is not present in crystals. In a disordered solid, atoms have "more freedom" to occupy more positions other than the restricted options in a periodic structure. In consequence, heat capacity get an additional contribution, besides C_{ph}, due to phenomena such as tunnelling transitions or structural relaxations [61], and at low temperatures this contribution dominates and is proportional to T^n, where $n > 1$ but close to 1:

$$C_a \propto T^n \tag{2.8}$$

2.2.2 Thermal expansion

Characterisation of multiple integrated components in a cryogenic environment require elements that allow alignment adjustment, particularly for optical I/O.

Thermal expansion is a consequence of the deviation of the atomic potential from the harmonic approximation. A lattice with atoms with parabolic potential would show no sign of thermal expansion. At low temperatures, as the thermal vibration in atoms become smaller, the potential they feel approximates more and more to a true parabola, leading to the extinguishment of the thermal expansion coefficient α as $T \to 0$:

$$\alpha = \frac{1}{L}\left[\frac{\partial L}{\partial T}\right]_p \tag{2.9}$$

Thermal expansion is significant when designing a cryogenic system in general. Soldered junctions that form an interface between two or more different metals with different thermal expansion coefficients should always be considered. At low temperatures, the displacement of said layers might generate stress that could break the solder joint.

The selection of materials that are meant to be in contact should be made considering how said pieces will behave when the temperature changes. If the situation requires that a particular structure keeps its relative position with respect to a certain point, the ideal solution would be using materials with similar α if not the same material.

2.2.3 Thermal conductivity

Thermal conductivity is the property of matter to conduct heat. The transport of heat in a solid is described by Fourier's law of conduction:

$$\dot{q} = -\kappa \nabla T \tag{2.10}$$

Where $\dot{q}$ is the heat flux measured in [W/(m K)], κ is the thermal conductivity coefficient and ∇T is the temperature gradient.

Heat is transported either by electrons or by lattice vibrations (phonons). These *heat carriers* do not move ballistically through the solid. Still, they interact with their surroundings, being scattered either by other electrons, the lattice, or imperfections in the material. A simplification of the heat transport problem is to consider electrons and phonons as a gas diffuses through the material and then apply kinetic gas theory to calculate an effective thermal conductivity coefficient:

$$\kappa = \frac{1}{3} v \lambda \frac{C}{V_m} \tag{2.11}$$

where v is the drift velocity of the *heat carriers*, λ is their mean free-path, and C/V_m is the specific heat per unit of volume. The equation can be interpreted as the ease to *transport* a certain *cargo* (a.k.a. C/V_m) is proportional to the magnitude of said *cargo*, how fast the carriers move and how long they move before they are scattered by other particles.

On one side, the phonons' speed in solids, particularly metals, can be assumed to be the speed of sound v_s. At the same time, for electrons, only those with energies around the Fermi level can be excited to occupy energy states that allow thermal conductivity, so their velocity is associated with their energy E_F and is called Fermi velocity, or v_F, where $v_F \gg v_s$. Both v_s and v_F are temperature independent. In Sec. 2.2.1 temperature dependence of C was already discussed. Therefore, the missing piece of the puzzle is to discuss how T affects the mean free-path λ, which is intrinsically related to scattering mechanisms that limit the *heat carriers'* mobility.

2.2.3.1 Phonon scattering

For insulators, phonon-phonon scattering is the most relevant mechanism affecting the mean free-path λ; therefore, the thermal conductivity is given basically by Eq. 2.11 where $\lambda = \lambda_{ph}$ being the last one the phonons' mean free-path.

$$\kappa_{ph} \propto T^3 \lambda_{ph}(T) \quad \text{at} \quad T < \theta_D/10 \tag{2.12}$$

At this temperature range, $T < \theta/10$, the number of phonons in the lattice decreases with decreasing T, which diminishes the scattering, increasing λ_{ph}. This means thermal conductivity is inversely proportional to temperature at relatively high temperatures below room temperature.

The number of thermally excited phonons in the lattice is very low for even lower temperatures. They become almost irrelevant for scattering, which gives a free pass to other scattering agents whose availability doesn't depend on the temperature as crystal defects or crystal boundaries. Since at very low temperatures λ_{ph} is temperature independent, $kappa_ph$ rely only on the specific heat, which for insulators is proportional to T^3.

Since at high temperatures κ_{ph} is inversely proportional to T, and at low temperatures it is proportional to T^3, somewhere in between those two ranges, there should be a point where κ_{ph} reaches a maximum value.

Consequences of defects and impurities having more influence in the scattering of *heat carriers* include: 1) potential high thermal conductivity for low impurity and low defect density crystals, reaching κ_{ph} even comparable to metals; and 2) low thermal conductivity for amorphous insulators, such as glass, due to the small distance between defects, which are everywhere.

2.2.3.2 Electronic scattering

The thermal conductivity coefficient due to conduction electrons in a metal can be defined using Eq. 2.11 with a velocity equals to the Fermi velocity v_F:

$$\kappa_e = \frac{1}{3} v_F \lambda_e(T) \frac{C_e}{V_m} \tag{2.13}$$

At high temperatures, the presence of thermally excited phonons plays an essential role

in scattering heat-conducting electrons; therefore, similarly to phonon-phonon scattering, the electron-phonon scattering increases with temperature.

At low temperatures, the number of vibrations in the lattice decreases, and so the scattering by impurities and defects start to dominate. Similarly to what happened to λ_{ph}, λ_e becomes temperature independent, so the thermal conductivity becomes proportional only to the specific heat:

$$\kappa_e \propto C_e \propto T \tag{2.14}$$

$$C = \gamma T + \beta T^3 \tag{2.15}$$

And just like happened with κ_{ph}, the different trending for high and low temperatures result in the thermal conductivity going through a maximum value—the more perfect the metal, the lower the temperature of the maximum value of κ_e. As the impurities and defects in the metal increase, the maximum temperature gets pushed to higher temperatures.

2.2.4 Electrical conductivity

Electrical conductivity measures the capacity of a material to transport electrical charge. Consider a medium with electrical charges that are free to move. If an electric field $\vec{E}$ is applied, the charges will feel a Lorentz force creating a current density $\vec{J}$:

$$\vec{J} = \sigma \vec{E} \tag{2.16}$$

where σ is the electrical conductivity and is generally a rank-2 tensor. The expression 2.16 is known as Ohm's law.

While the thermal conductivity κ measures the conduction of energy through the interaction of different *thermal carriers* (i.e. phonons and electrons), electrical conductivity

measures the ability to transport the carriers themselves.

In metals at low temperatures, where lattice vibrations are minimal, and scattering is caused mainly by defects and impurities, $\lambda_e \sim$ constant, thermal conductivity keeps decreasing, leading to a ratio κ/σ proportional to T.

2.3 Electrical properties of semiconductors at low temperatures

Semiconductors constitute a significant portion of silicon photonic devices. A description of the relevant properties and mechanisms required to understand the performance of a silicon PIC in a cryogenic system would be incomplete without a proper discussion on the temperature dependence of the properties of semiconductors. This section will introduce some fundamental concepts of semiconductors, particularly the definitions required to model electrical conductivity based on their carrier density and mobility.

Conductors are materials characterised by their high electrical conductivity, while insulators show high resistance to the flow of electrical charges. Semiconductors, on the other size, are a kind of material with properties somewhere in between these two categories. Semiconductors, in general, have electrical conductivities that are sensitive to external factors such as temperature, illumination, magnetic fields, and injection of impurities [63], which makes them ideal for applications where this modulation can be exploited to sense the environment or process information.

2.3.1 Electrical conductivity

The electrical conductivity in a semiconductor depends not only on the number of free carriers available to form an electrical current but also on how easy it is for the charges to move around the lattice. In general, for a semiconductor where both electrons and holes are present and can contribute to a net electrical current, their conductivity is defined as

follows:

$$\sigma = q_0 \left(n\mu_n + p\mu_p \right)$$

where the q_0 is the elementary charge of an electron, n and p are the electron and hole density respectively, and μ_e and μ_p are their mobilities.

The following pages will discuss the role temperature plays in the concentration of carriers and the scattering processes between them and the lattice.

2.3.2 Band gap

One of the main characteristics that distinguish semiconductors from other kinds of materials is the structure of their energy bandgap. While conductors have a continuous range of available electronic energy levels, insulators and semiconductors have defined ranges of forbidden energy levels that separate bound electrons (valence band) from those free to move around the lattice (conduction band). Semiconductors, unlike insulators, have relatively small band gaps, which allow electrons to be easily excited from the valence band to the conduction band. Intrinsic silicon, for example, has a bandgap of 1.12 eV compared to an insulator such as glass (9 eV).

The energy band gap is the barrier that valence electrons need to overcome to be free to transport charge from one place to another in the semiconductor.

Band gaps in semiconductors change with temperature due to two effects: thermal expansion, which changes the lattice constant, which is explained by the fact that electronic energy bands are created due to overlapping of single electron's discrete energy levels; and due to electron-phonon interactions, which goes against the assumption of a perfect crystal stated in the theory of electronic energy bands [64].

A change in the bandgap modifies the probability a certain electron would be excited to the conduction band. Since temperature changes modify the interaction between atoms in the lattice, a relationship between bandgap and temperature is expected and reported as an empirical expression by Varshni [65]:

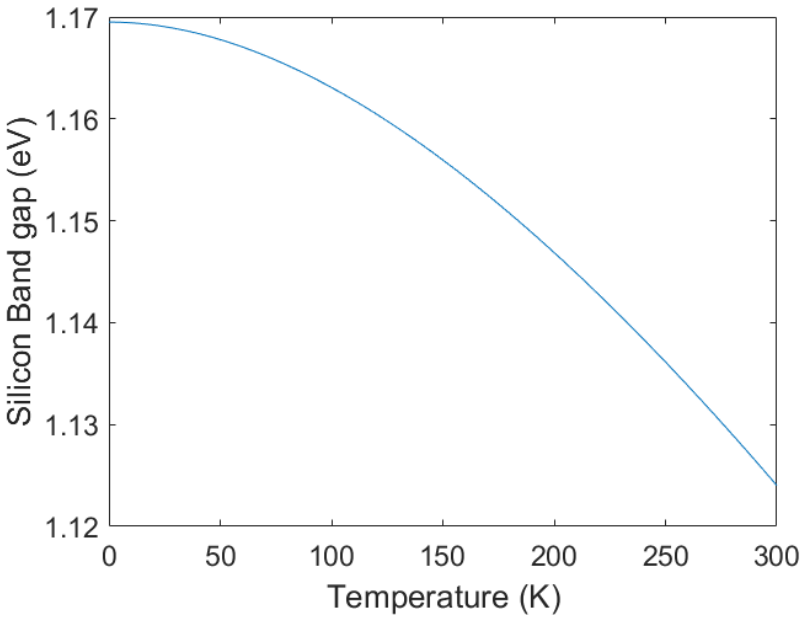


Figure 2.2: Temperature dependency of silicon's band gap using model proposed by Green [66].

$$E_g = E_{g0} - \frac{aT^2}{b+T} \tag{2.17}$$

where a and b are constants proper to the material, and E_{g0} is the band gap at T=0 K. For silicon, said parameters have the following values: a=4.73×10^{-4}, b=636 and E_{g0}=1.1695. The main observation one can notice from Eq. 2.17 is that the band gap becomes wider at lower temperatures, which together with smaller thermal excitation contributes to the reduction of available carriers in the conduction band.

2.3.3 Density of states

However, even if an electron in the valence band absorbed the energy required to overcome the forbidden zone, the conduction band still needs to have available energy levels to be occupied. The density of electrons n (or holes p) in a semiconductor depends both on the density of energy levels $g(E)$ and the probability density function $f(E)$ that a certain energy level within a range dE is occupied, also known as Fermi distribution:

$$
\begin{aligned}
n &= \int_{E_c}^{E_{\text{top}}} g_c(E)\ f(E)\ \ dE \\
p &= \int_{E_{\text{bottom}}}^{E_v} g_v(E)\ (1 - f(E))\ \ dE
\end{aligned}
\tag{2.18}
$$

The density of states, or number of available states within an energy range, depends both on the energy of the conduction and valence bands, and the effective masses of carriers.

$$
\begin{aligned}
g_c(E) &= \frac{m_n^* \sqrt{2m_n^*(E - E_c)}}{\pi^2 \hbar^3} \quad E \geq E_c \\
g_v(E) &= \frac{m_p^* \sqrt{2m_p^*(E_v - E)}}{\pi^2 \hbar^3} \quad E \leq E_v
\end{aligned}
\tag{2.19}
$$

where m_n^* and m_p^* are the density-of-states effective masses of electrons and holes respectively, which are in general temperature dependent. For silicon, the electronic states are not uniformly distributed in the K-space (energy surfaces are ellipsoidal and centred at points along $\langle 100 \rangle$), therefore its density-of-states effective mass in the conduction band is expressed in terms of the components of the inverse mass tensor [66]:

$$
m_n^* = 6^{2/3} \left(m_l^* m_t^{*2} \right)^{1/3} \tag{2.20}
$$

where m_l^* is the longitudinal effective mass and m_t^* is known as the transverse effective mass, and the inverse mass tensor is defined as follows:

$$
\frac{1}{m^*} = \begin{pmatrix} m_{xx}^{-1} & m_{mxy}^{-1} & m_{xz}^{-1} \\ m_{yx}^{-1} & m_{yy}^{-1} & m_{yz}^{-1} \\ m_{zx}^{-1} & m_{zy}^{-1} & m_{zz}^{-1} \end{pmatrix} \tag{2.21}
$$

where $m_{xx} = m_l^*$ and $m_{yy} = m_{zz} = m_t^*$, and the off-diagonal elements are assumed to have a negligible value. In silicon, m_l^* is temperature independent, while m_t^* is inversely proportional to the temperature shrinkage of the energy bandgap:

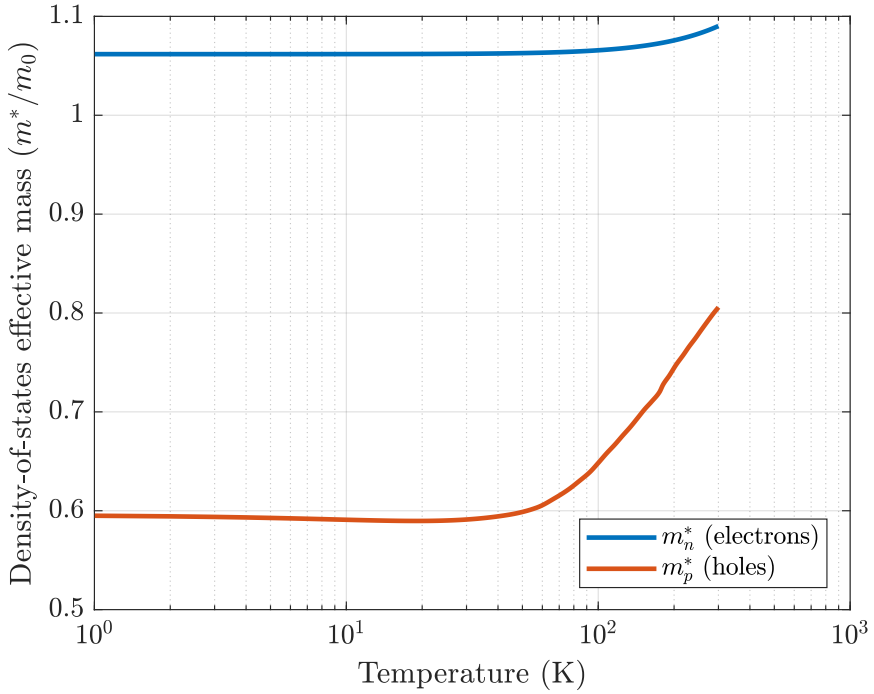


Figure 2.3: Temperature dependence of density of states effective mass of electrons and holes in intrinsic silicon [66]

$$m_l^* = 0.9163 m_0 \tag{2.22}$$

$$m_t^* \cong 0.1905 \left(\frac{E_{g0}}{E_g(T)} \right) \tag{2.23}$$

where m_0 is the electron's rest mass, and both E_{g0} and $E_g(T)$ are the energy gaps discussed in Sec. 2.3.2. Off-diagonal terms

The electronic structure of silicon near the valence band's maximum at the centre of the Brillouin zone has double degenerate hole bands. They are called "light hole", "heavy hole" and "split-off" hole band, which, assuming they all are isotropic and parabolic, contribute to the density-of-states effective mass in the valence band according to the

Effective mass	Value
m^*_{hh}/m_0	0.537
m^*_{lh}/m_0	0.153
m^*_{so}/m_0	0.234

Table 2.2: Parameters required to calculate the density of states effective masses. Transversal and longitudinal electron effective mass extracted from [66].

following expression:

$$m_p^* = \left({m_{lh}^*}^{3/2} + {m_{hh}^*}^{3/2} + \left(m_{so}^* \ \exp\left(-\frac{\Delta}{k_B T} \right) \right)^{3/2} \right)^{2/3} \tag{2.24}$$

where m_{hh} is the heavy hole effective mass, mlh is the light hole effective mass, m^*_{so} is the effective mass of holes in the split-off band and Δ is the energy between the "split-off" band and the other two bands, and has been measured to be 0.0441(3) eV at 1.8 K [66]. Table 2.2 shows a summary of the values reported for silicon's holes effective masses in the valence band.

Substituting equations 2.23 into 2.20, and the values in Table 2.2 into 2.24, an expression for the temperature dependency of the density-of-states effective masses can be obtained (see Fig. 2.3).

2.3.4 Carrier density

The function $f(E)$ in equations 2.18 is the Fermi distribution and describes the probability distribution that a carrier occupies an available energy state within a specific energy range:

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{k_B T} \right)} \tag{2.25}$$

Substituting 2.25 and 2.19 in 2.18 the density of carriers, for both electrons and holes, in terms of their temperature dependent parameters is:

$$\begin{aligned} n &= N_C \frac{2}{\sqrt{\pi}} F_{1/2}(\eta_c) \\ p &= N_V \frac{2}{\sqrt{\pi}} F_{1/2}(\eta_v) \end{aligned} \tag{2.26}$$

with N_C and N_V being the effective density of states of the conduction and valence band respectively:

$$\begin{aligned} N_C &= 2\left(\frac{2\pi m_n^* k_B T}{h^2}\right)^{3/2} \\ N_V &= 2\left(\frac{2\pi m_p^* k_B T}{h^2}\right)^{3/2} \end{aligned} \tag{2.27}$$

and $F_{1/2}(\eta)$ is the Femi-Dirac integral of order 1/2:

$$F_{1/2}(\eta) = \int_0^\infty \frac{x^{1/2} dx}{1 + \exp(x - \eta)}$$

The number of electrons and holes excited by thermal vibrations in the lattice gives the intrinsic carrier density. It depends both on the value of the energy bandgap and the density of energy states in the valence and conduction band:

$$n_i = \sqrt{N_C N_V}\ \exp\left(-\frac{E_g}{2k_B T}\right) \tag{2.28}$$

The carrier density has two different contributions: intrinsic and extrinsic. Extrinsic carriers come from the ionisation of impurities incorporated into the silicon lattice.

Dopants can be classified into two: donors and acceptors. Donors are elements that cede electrons (n-type). At the same time, acceptors have fewer electrons in their valence band than the atoms they displace, so they can "accept" electrons from other atoms. Acceptors can be understood as atoms that take electrons or give holes. Phosphorous and boron are typical materials used as impurities for silicon as donors and acceptors.

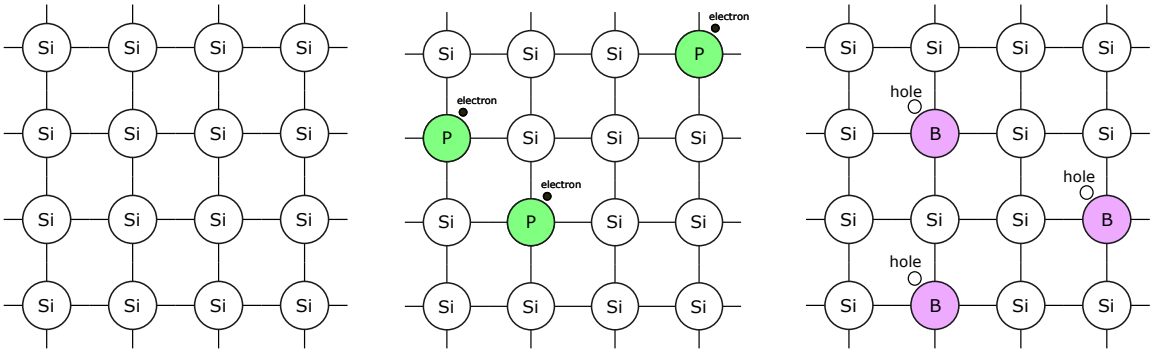


Figure 2.4: a) Intrinsic silicon lattice **b)** Silicon lattice doped with n-type impurities (Phosphorus), providing additional electrons **c)** Silicon lattice doped with p-type impurities (Boron) increasing the number of potential holes in the system.

An expression for the total carrier density (for a nondegenerate* semiconductor in equilibrium) as a function of temperature that includes both intrinsic and extrinsic contributions can be found in the literature [69]:

$$n = -\frac{N^* + N_a}{2} + \sqrt{\frac{(N^* + N_a)^2}{4} + N^*(N_d - N_a)} \tag{2.29}$$

$$p = -\frac{N^* + N_d}{2} + \sqrt{\frac{(N^* + N_d)^2}{4} + N^*(N_a - N_d)} \tag{2.30}$$

where N_a and N_d are the acceptor and donor density respectively, and:

$$N^* = \frac{N_c}{2} \exp\left(\frac{E_d - E_c}{k_B T}\right) \qquad \text{for a n-type semiconductor} \tag{2.31}$$

$$N^* = \frac{N_v}{2} \exp\left(\frac{E_v - E_a}{k_B T}\right) \qquad \text{for a p-type semiconductor} \tag{2.32}$$

*A non-degenerate semiconductor has Fermi level located either within the conduction or valence band or inside the bandgap within $\approx k_B T$ from the edge of one of those bands. Intrinsic semiconductors become degenerate at high temperature when $k_B T$ becomes comparable to the bandgap when the material's bandgap is narrowed or at high impurity concentrations [67]. According to [68] a semiconductor can be considered strongly degenerate above $10^{18}\,\mathrm{cm}^{-3}$.

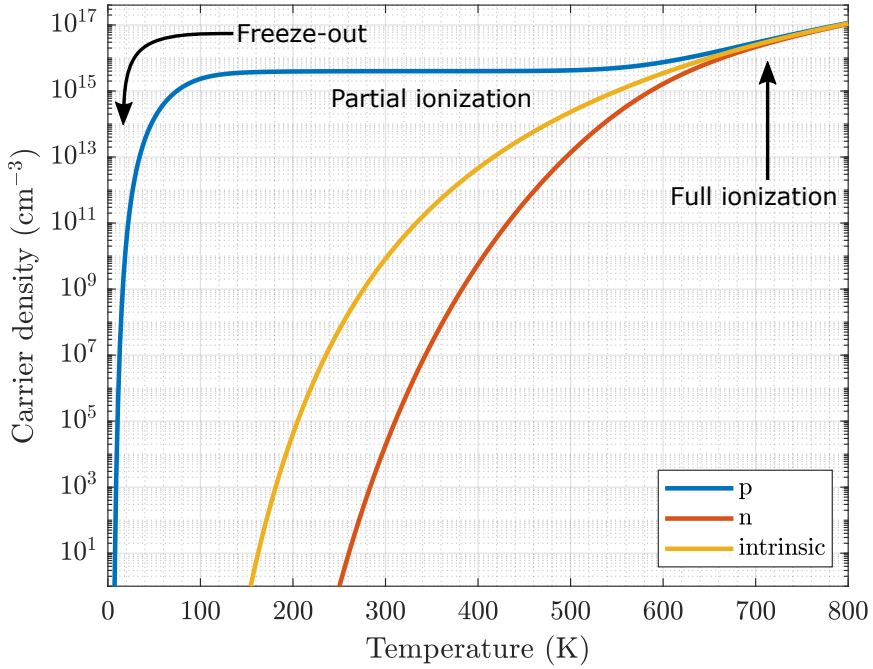


Figure 2.5: Temperature-dependent carrier density function (Eq. 2.30) for a p-type non-degenerate semiconductor doped with an impurity density $Na = 4 \times 10^{15}\,\mathrm{cm}^{-3}$.

As the temperature decreases, carriers start filling lower energy levels, decreasing the number of intrinsic carriers and decreasing the ionisation level of available impurities.

For a low impurity-density semiconductor, the minimum temperature required for full ionisation is lower compared to a semiconductor with a high doping level. As temperature decreases, recombination of carriers becomes more predominant until the total carrier density drops dramatically in a process called "freeze-out" (Fig. 2.5).

On the other hand, a high concentration of impurities increases the temperature where the freeze-out occurs, allowing the operation of electronics at lower temperatures, but compromising the non-degeneracy of the material.

2.3.5 Mobility models

When an electric field is applied to an electrical charge in free scape, a constant Lorentz force will result in a constant acceleration following Newtonian mechanics. Nonetheless,

electrical carriers in solids will experience continuous scattering by other carriers and thermal vibrations from the lattice. These interactions will produce a semi-erratic path on average, resulting in a displacement proportional to the electric field applied.

The mobility is the proportionality constant between the electric field $\vec{E}$ and average velocity, or drift velocity $\vec{v_d}$:

$$\vec{v_d} = \mu \vec{E}$$

Any mechanism that disturbs the perfect periodicity of the lattice can produce scattering of carriers, and every one of them will contribute to the total mobility μ, which can be approximated using Matthiessen's rule:

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \cdots \frac{1}{\mu_N} \tag{2.33}$$

where $\mu_1, \mu_2, \cdot, \mu_N$ are the mobilities due to exclusively one scattering agent such as the lattice, impurities, defects, etc.

The models used to describe and model the temperature dependence of some relevant scattering mechanisms will be presented and discussed in the following sections and are the result of the work published by Klaassen [70–72].

2.3.5.1 Lattice scattering

Experimental data on electron and hole mobility as a function of the impurity concentration N at 300 K has been previously modelled using the following expression [73]:

$$\mu = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + (N/N_{\text{ref}})^{\alpha_1}} - \frac{\mu_1}{1 + (N_{\text{ref},2}/N)^{\alpha_2}} \tag{2.34}$$

The contribution to the total scattering due only to the interaction of carriers with the lattice is obtained from the limit where the scattering by impurities is negligible $N \to 0$:

$$\mu_{i,L} = \mu_{\max}$$

Parameter	electrons	holes
$\mu_{\max}$ $(\mathrm{cm}^2 \cdot V^{-1} \cdot s^{-1})$	1414.0	470.5
$\mu_{\min}$ $(\mathrm{cm}^2 \cdot V^{-1} \cdot s^{-1})$	68.5	44.9
μ_1 $(\mathrm{cm}^2 \cdot V^{-1} \cdot s^{-1})$	56.1	29.0
N_{ref} (cm^-3)	9.20×10^{16}	2.23×10^{17}
$N_{\mathrm{ref},2}$ (cm^{-3})	3.41×10^{20}	6.10×10^{20}
α_1	0.711	0.719
α_2	1.98	2.0

Table 2.3: Parameters for lattice and majority carriers scattering models with electrons and holes for equations in sections 2.3.5.1 and 2.3.5.2

where the subscript $i = e, h$ stands for electrons and holes respectively, $\mu_{\max}$ is reported as 1414.0 for n-type (phosphorus-doped) silicon, and 470.5 for p-type (boron-doped) silicon, both with units of mobility $cm^2 \cdot V^{-1} \cdot s^{-1}$. The difference between both values could be explained by two factors: 1) the scattering between the lattice and the carriers are fundamentally different in magnitude depending on the type of majority carrier since effective masses are different for electrons and holes; 2) injection of different impurities can result in different changes in the lattice constant in the semiconductor [74].

A well known empirical exponential function for the temperature-dependent mobility contribution due to lattice scattering used by [75, 76] is the following:

$$\mu_{i,L} = \mu_{\max} \left(\frac{300}{T} \right)^{\theta_i} \tag{2.35}$$

where θ_i is a parameters that must be obtained experimentally, but for silicon Klassen [71] reports them as $\theta_e = 2.285$ and $\theta_h = 2.247$.

2.3.5.2 Major impurity scattering

The second contribution to the scattering experienced by carriers in a doped semiconductor is the one due to the interaction with the major impurities. If the lattice scattering is

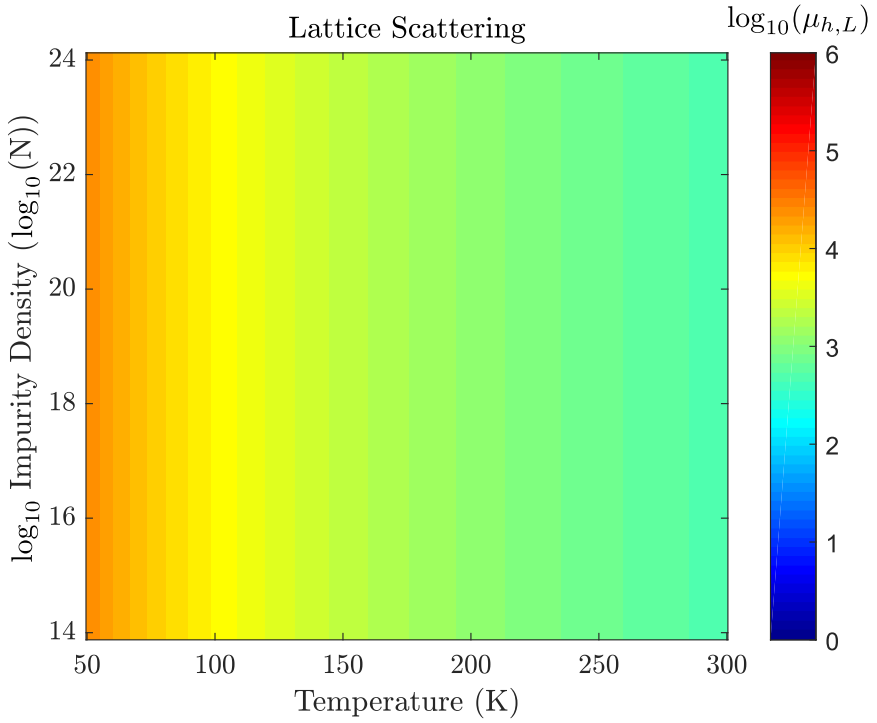


Figure 2.6: Logarithm of the hole mobility contribution due to scattering by the lattice

extracted from Eq. 2.34, then the major impurity contribution is what is left:

$$\mu_{\mathrm{i,I}}(N_I, c) = \mu_{i,N}\left(\frac{N_{\mathrm{ref},1}}{N_l}\right)^{\alpha_1} + \mu_{i,c}\left(\frac{c}{N_I}\right) \tag{2.36}$$

where I=D, A stands for donors and acceptors respectively, and c is the total number of carriers $c = n + p$. The temperature dependency of this scattering mechanism is implicit in the coefficients $\mu_{i,N}$ and $\mu_{i,c}$:

$$\mu_{i,N} = \frac{\mu_{\max}^2}{\mu_{\max} - \mu_{\min}}\left(\frac{T}{300}\right)^{3\alpha_1 - 1.5} \tag{2.37}$$

$$\mu_{i,c} = \frac{\mu_{\min}\mu_{\max}}{\mu_{\max} - \mu_{\min}}\left(\frac{300}{T}\right)^{0.5} \tag{2.38}$$

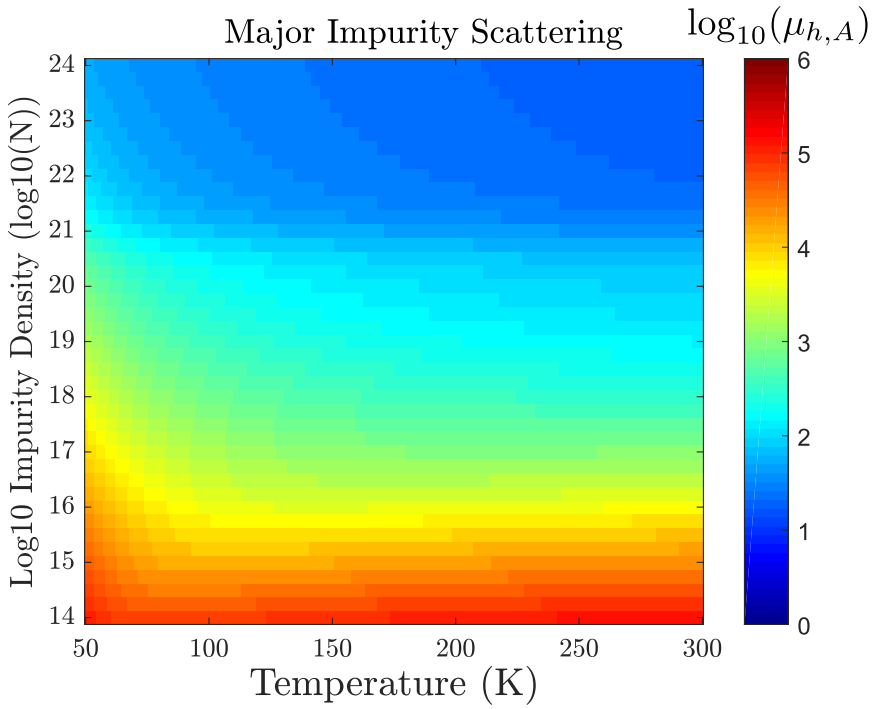


Figure 2.7: Logarithm of the hole mobility contribution due to scattering with major impurities (acceptors).

i	s_i	r_i
1	0.89233	0.7643
2	0.41372	2.2999
3	0.19778	6.5502
4	0.28227	2.3670
5	0.005978	-0.01552
6	1.80618	0.6478
7	0.72169	

Table 2.4: Numerical values for the constants s_i in equation 2.41 and r_i in equation 2.44

2.3.5.3 Minor impurity scattering

A third scattering mechanism models the collisions between carriers and minority impurities, i.e. acceptor scattering for electrons ($\mu_{e,A}$) and donor scattering for holes ($\mu_{h,D}$):

$$\mu_{e,A}(N_A, c) = \frac{\mu_{e,D}(N_D = N_A, c)}{G(P_h)} \tag{2.39}$$

$$\mu_{h,D}(N_D, c) = \frac{\mu_{h,A}(N_A = N_D, c)}{G(P_h)} \tag{2.40}$$

where G(P) is the "ratio between the collision cross-sections for repulsive ($\sigma_{\text{rep}]}$) and attractive (σ_{attr}) screened Coulomb potentials" [71] which is also equal to the ratio between scattering coefficients between majority and minority impurities, i.e. $G(P) = \frac{\sigma_{\text{rep}}}{\sigma_{\text{attr}}} = \frac{\mu_{e,D}}{\mu_{e,A}}$ or $\frac{\mu_{h,A}}{\mu_{h,D}}$. The ratio G(P) can also be expressed in terms of a function P in the following way:

$$G(P) = 1 - \frac{s_1}{\left(s_2 + \left(\frac{m_0}{m}\frac{T}{300}\right)^{s_4} P\right)^{s_3}} + \frac{s_5}{\left(\left(\frac{m}{m_0}\frac{300}{T}\right)^{s_7} P\right)^{s_6}} \tag{2.41}$$

The coefficients s_i can be obtained from Table 2.4 and P depends on temperature T, the total carrier density c and the effective carrier mass m according to the following expression:

$$P = \frac{1.36 \times 10^{20}}{c}\left(\frac{m}{m_0}\right)\left(\frac{T}{300}\right)^2 \tag{2.42}$$

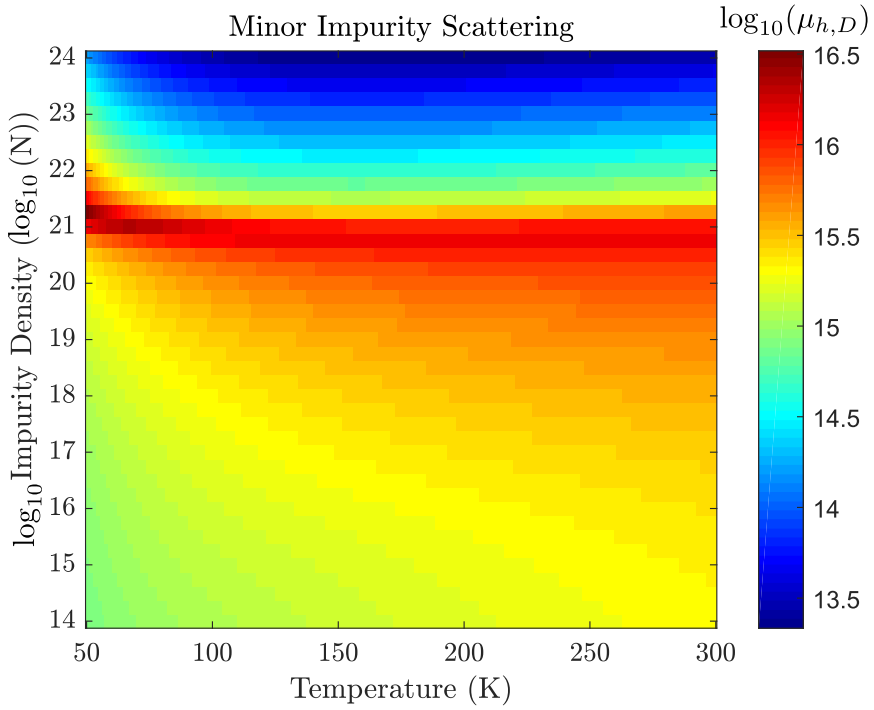


Figure 2.8: Logarithm of the hole mobility contribution due to minor impurities (donors).

2.3.5.4 Electron-hole scattering

Finally, under the assumption that in terms of electrical forces, holes can be considered as acceptors, and electrons as donors, the Eq. 2.38 can be used to model electron-hole interactions by applying a correction $F(P)$ that compensates the differences between moving carriers and stationary impurities:

$$\begin{aligned} \mu_{e,h}(p,c) &= F(P_e)\mu_{e,D}(N_D = p,c) \\ \mu_{h,e}(n,c) &= F(P_h)\mu_{h,A}(N_A = n,c) \end{aligned} \tag{2.43}$$

where $F(P_i)$ is fitted by the following analytical expression:

$$F(P) = \frac{r_1 P^{r_6} + r_2 + r_3 \frac{m_1}{m_2}}{P^{r_6} + r_4 + r_5 \frac{m1}{m2}} \tag{2.44}$$

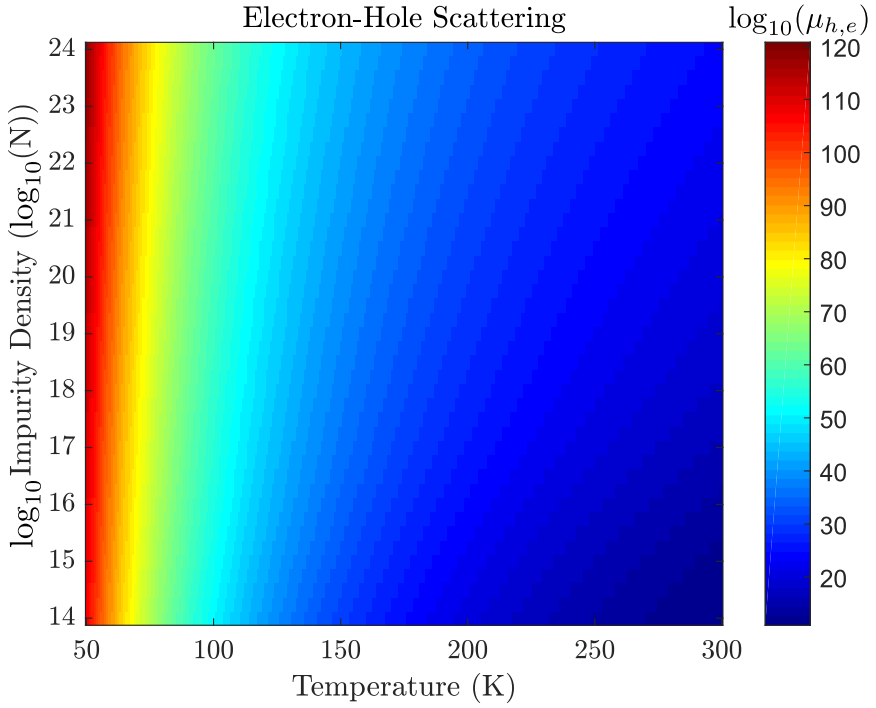


Figure 2.9: Logarithm of the electron-hole scattering contribution to mobility.

and the coefficients r_i can also be found in Table 2.4 and $\{m_1, m_2\}$ are the masses of both electrons and holes.

2.3.5.5 High Concentration effects

Besides the scattering mechanisms mentioned in previous sections, additional contributions to the total mobility arise when semiconductors are doped with a high dose of impurities. Above impurity concentrations in the order of $10^{20}\,\mathrm{cm}^{-3}$, carriers are no longer scattered by impurities with a single charge and a concentration N_I, but by impurities with Z charges forming a "cluster" concentration defined by $N_I' = N_I/Z$ (Fig. 2.10).

$$Z_I(N_I) = 1 + \frac{1}{c_I + \left(\frac{N_{\mathrm{ref,I}}}{N_I}\right)^2} \tag{2.45}$$

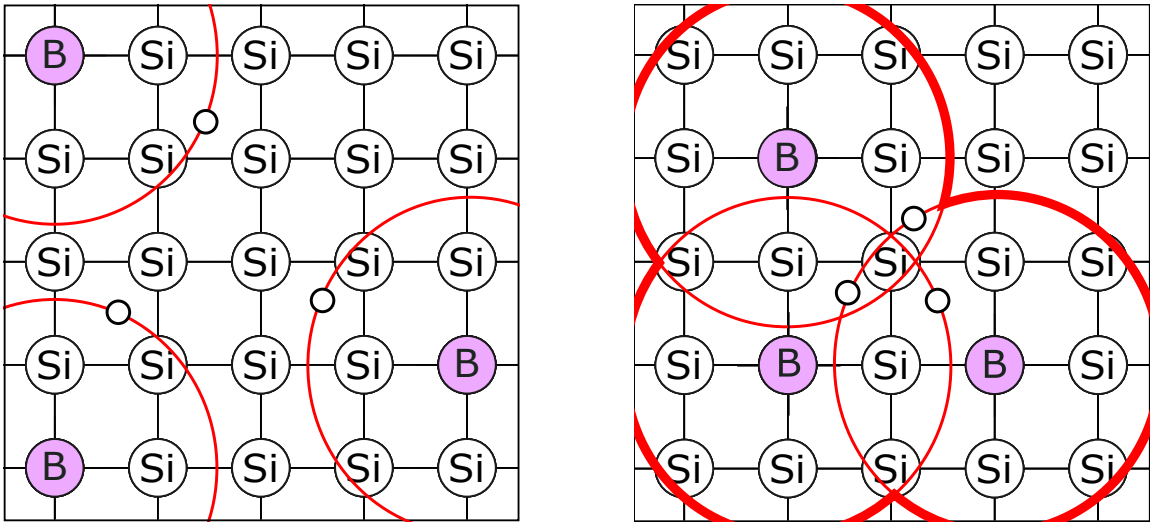


Figure 2.10: Diagram of silicon lattice for a **a)** low and **b)** high impurity density. Carriers moving through a lattice like in b) would not "observe" three impurity atoms with a single hole each, but a bigger cluster with three times the electrical charge.

where the required parameters for phosphorus are $c_I = 0.21$ and $N_{\mathrm{ref,D}} = 4.0 \times 10^{20}\,\mathrm{cm}^{-3}$, while for boron are $c_A = 0.50$ and $N_{\mathrm{ref,A}}$

2.4 Experimental set-up

This section will introduce the cryogenic equipment used to characterise integrated photonic structures at temperatures near absolute zero. The system used should not only be able to provide stable temperatures within the range of typical SNSPDs' critical temperature ($\sim$2 K), but it should also provide enough cooling power capable of dissipating all the heat generated by the sample.

Cryogenic systems can be categorized based on several characteristics: wet/dry system, open/closed-cycle, continuous/single-shot operation, evaporation cryostats, dilution refrigerators, etc [61]. From the alternatives mentioned above, the evaporation cryostat is the most accessible and economical option assuming a collection mechanism for the evaporated cryogen is in place. The University of Bristol has the required infrastructure

to collect, liquefy and store the liquid helium (L^4He or LHe) used among all different departments in the School of Physics.

A Lake Shore® cryogenic probe station (CPX) compatible with high-vacuum and under-4 K applications were also used for direct electrical and optical probing of integrated devices without requiring any kind of wire bonding.

The following pages will provide the most relevant details on the design and operation of both cryogenic systems and the design of the sample stage.

2.4.1 Variable Temperature Insert

The first cryogenic system to be discussed is an in-house manufactured variable temperature insert (VTI), also referred to as a dipstick, formed by a single oxygen-free copper (OFCu) cold head protected by a vacuum chamber and designed to be submerged in a cryogenic liquid bath (Fig. 2.11a), typically LHe.

When the chamber is completely submerged, the LHe bath constantly provides liquid cryogen at 4.2 K to the cold head (here referred to as 1k-pot), which maintains it at the boiling temperature of He. The exhaust line connects the cold head to a pump which extracts the most energetic He molecules, lowering its temperature.‘

The container for the cryogenic bath is a Cryogenic® stainless steel dewar with a capacity of 43 litres with an insulating optimised multilayer protection maintained under vacuum. The top plate is also made of stainless steel and has three openings: the main and bigger one for inserting the VTI and two smaller ones for attaching the liquid level meter and the exhaust line connected to the return line.

The aluminium shields shown in Fig. 2.11a have layers of reflective aluminised mylar and nylon netting. Three additional radiation shields (Fig. 2.11b) were installed at the top of the access to the bath to reduce the thermal losses on the liquid He bath due to convection and radiation. The shields were made of 16 cm-diameter PCB disks which were stripped of their solder layer, so the copper layer was exposed.

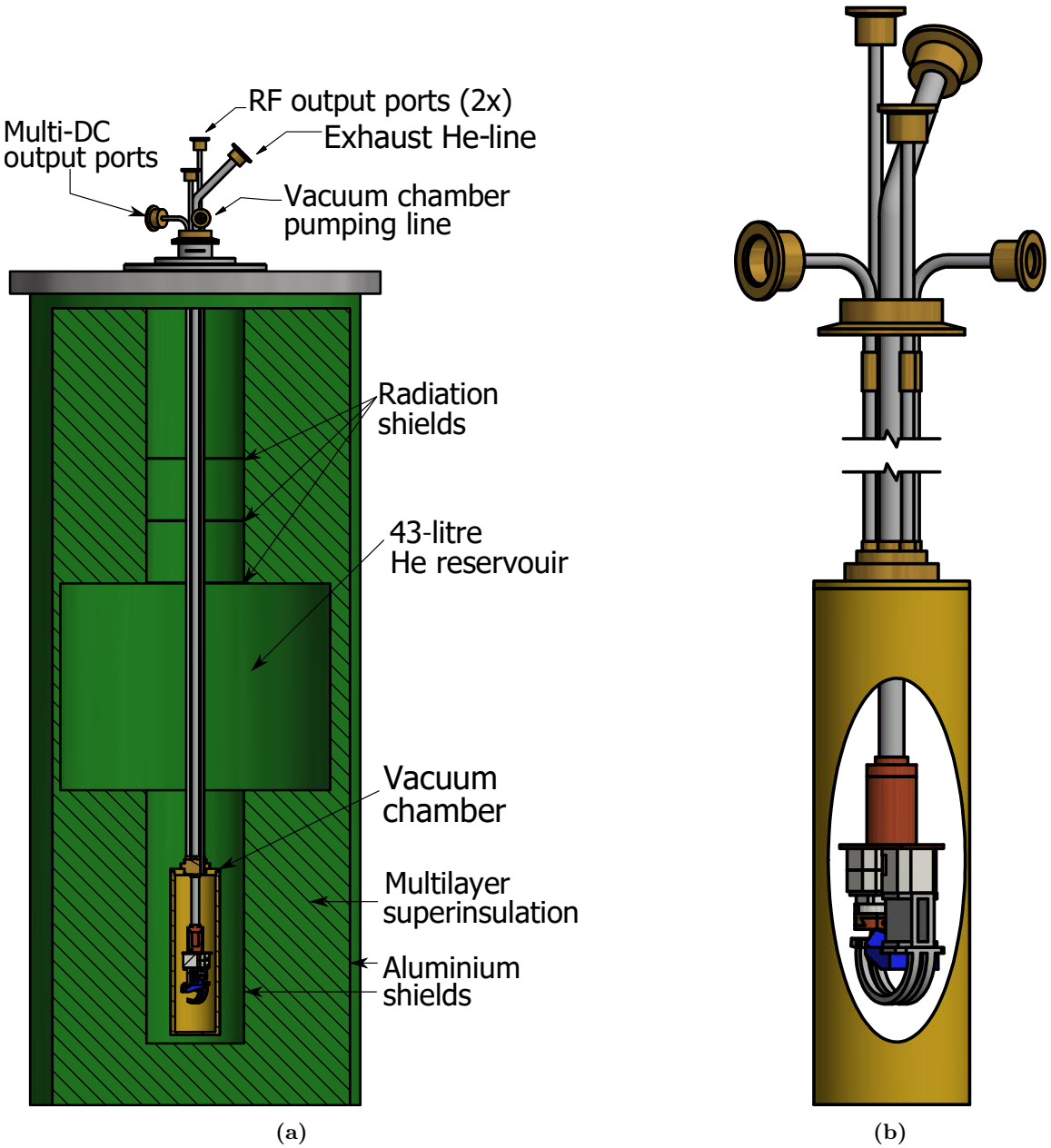


Figure 2.11: a) Diagram of the liquid He Crogenic® dewar. b)Radiation shield used to reduce evaporation of liquid He bath inside the dewar. The central orifice allows the VTI to go through down to the bottom of the dewar, the other three were designed to fit the electrical connections of the heater at the bottom of the dewar, the He level meter and to fit the transfer line used during liquid He transfers.

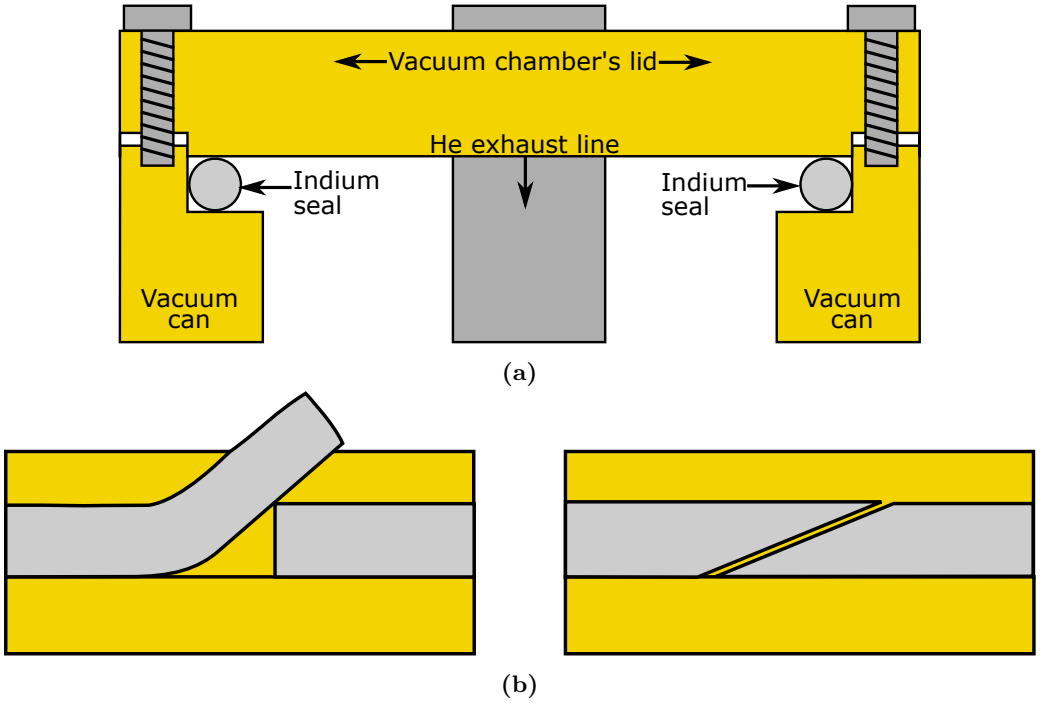


Figure 2.12: a) Cross-section of the vacuum chamber and how the indium seal is applied around the inside groove. b) Cracks in the indium seal can be avoided by cutting the indium wire in diagonal at both ends in such a way that they approximately form a complete ring that keeps its shape when a uniform vertical force is applied.

The vacuum chamber was made of brass due to its machinability. It was designed to fit the size of the sample stage, minimising its volume and weight as much as possible. The chamber consists of two structures, the main body and a lid.

To have a proper connection between the lid and the vacuum can and secure a good vacuum, a seal is made of indium wire with a diameter of $\sim 1\,\mathrm{mm}$, cut to a length equal to the inner perimeter of the vacuum chamber inside a groove specially machined for that purpose. Both edges of the indium wire are trimmed at an angle and spliced together (Fig. 2.12b) to get a homogeneous seal and avoid cracks once the lids are screwed into position. Before fitting the seal in the groove, a thin layer of Dow Corning ® high vacuum grease can be applied to improve the effectiveness of the seal and reduce the probability of leaks.

Four independent stainless steel tubes connect the vacuum chamber to the top of the VTI, where they connect to the multi-DC ports, the two SMA connectors used for RF

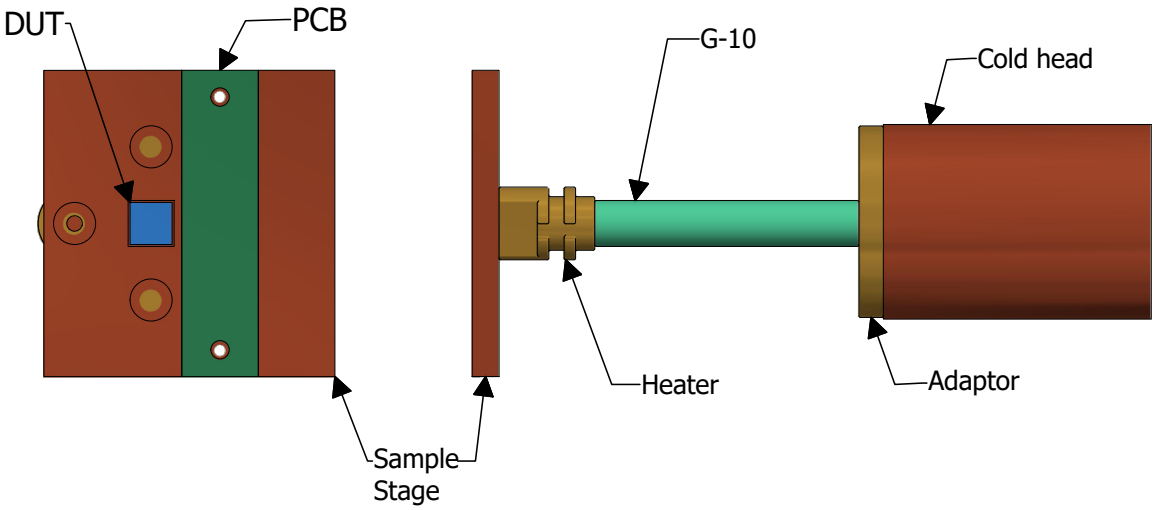


Figure 2.13: Sample holder used for cryogenic tests using the variable temperature insert. The DUT is connected to the PCB via wire bonding. The sample stage is separated from the 1k-pot by a low thermally conductive rod made of G10. A heater made of nichrome was installed under the sample stage as excitation for the temperature controller.

measurements and the vacuum chamber's pumping line. The multi-DC interface is an 18-pin Fischer® connector Core Series attached to a machined KF25 brass stub.

The cold head, or 1K-pot, is a small reservoir made of oxygen-free copper, connected to the liquid He bath through a small stainless steel capillary with an inner and outer diameter of 0.5 mm and 0.8 mm respectively, with a length of approximately 16 cm. The 1K-pot is also connected to an exhaust line used to extract He-gas via a two-stage oil-sealed rotary pump with a pumping speed of $12\,\mathrm{m^3\,h^{-1}}$ and an ultimate pressure at around 2×10^{-3} mbar.

The sample holder consists of a 40-by-40 $\mathrm{mm^2}$ of oxygen-free copper with two indentations to allow the DUT and PCB to be close to the sample stage's surface and facilitate the wire bonding. Two Cernox® sensors CX-1050 were used to monitor the temperature of the sample stage and the 1k-pot through an SRS cryogenic temperature controller (CTC100).

The He bath is prepared inside a 43-litre capacity dual shielded stainless steel dewar, which feeds the 1K-pot with a continuous supply of liquid He through a stainless steel 0.5 mm-diameter. As was mentioned before, five stainless steel tubes are soldered to the

vacuum chamber: one for DC lines, two for RF cables, one for pumping the chamber and one exhaust line, which is connected directly to the 1K-pot. The DC lines were made of twisted low-thermally conductive manganin ($Cu_{83}Mn_{13}Ni_4$) wires, connected to an 18-pin Fischer Core Series Brass connector.

The 1K-pot reaches base temperature (^{4}He's boiling temperature = 4.2K) through thermalisation with the cryogenic bath, which is helped by the constant supply of liquid helium from the capillary.

The liquid He^4 in the 1K-pot is cooled down to its boiling temperature of 4.2 K by pumping it through the exhaust line using a rotary pump. Liquid from the bath flows through the capillary, experiencing a throttling process, also known as Joule-Thompson expansion, which is an isenthalpic process [77]. The variation in temperature can be expressed in terms of the relevant thermodynamics variables:

$$\left(\frac{\partial T}{\partial p}\right)_H = \frac{1}{C_p}\left(T\left(\frac{\partial V}{\partial T}\right)_p - V\right) = \frac{V}{C_p}\left(-T\alpha + 1\right) \tag{2.46}$$

where C_p is the constant-pressure heat capacity, and α is the volumetric expansion coefficient of liquid helium at 4.2 K.

2.4.2 Sample Stage

Characterisation of an integrated device shows some particular difficulties when the test is done inside a cryostat. Firstly, since the cryogenic system should be suitable for SNSPD testing, the cryostat must have no windows, limiting the ability to get any visual feedback during the alignment of the sample. This prompts not only active components for alignment adjustment, which is required in standard photonic setups anyway but also a feedback-loop control that optimises the position of the sample during its cooling down process.

The sample stage designed for the cryogenic characterisation of PICs is shown in Fig. 2.14. The position and orientation of the sample are controlled by four closed-loop

Attocube® Premium Line positioners designed to operate under extreme conditions such as cryogenic temperatures and ultra-high vacuum.

The sample is located in a dismountable oxygen-free copper base attached to a fixed brass adaptor. Underneath both pieces, a rotary stepper (ARN101) controls the orientation angle of the sample with a resolution in the order of µ° with a travel range of 14 m° at $T = 4\,\mathrm{K}$. Two linear steppers (ANP101) control the sample's position in the horizontal plane, both with sub-nm resolution, travel range of 5 mm and 0.8 µm-fine positioning range. A V-Groove array (VGA) of fibres for optical I/O is held in position by an aluminium arch attached to a second stack of elements, including an electrical probe, a third linear vertical positioner and an aluminium pedestal.

The VGA consists of a linear array of single-mode fibres with a separation of 127 µm between channels (Fig. 2.15). The base is silicon, while the lid is made of Pyrex. The VGA is polished at an angle of 8° to coincide with the specifications of the gratings couplers to avoid back-reflection caused by second-order diffraction (Sec. 2.1.2). The electrical probe, on the other side, is a Cascade Microtech® |Z| Dual Probe®, designed for low temperature and high vacuum applications.

Both the VGA and the electrical probe are linked together via an aluminium arch that not only provides a separation between both elements but also allows the VGA to have its polished facet be parallel to the surface of the sample, allowing it to get closer to it, improving optical coupling.

After the VGA and the electrical probe are aligned at room temperature, the relative distance changes as the temperature decreases inside the cryostat due to thermal contraction. Although the deformation process is slow and can be compensated in real-time using an optimisation routine that maximises the optical coupling (assuming that the effective contact area available for the electrical probe is big enough), a multiphysics simulation was performed to estimate the magnitude of the relative displacement between the optical and electrical I/O (see Sec. 2.2.2).

The two stacks of components are screwed to an oxygen-free copper baseplate, attached

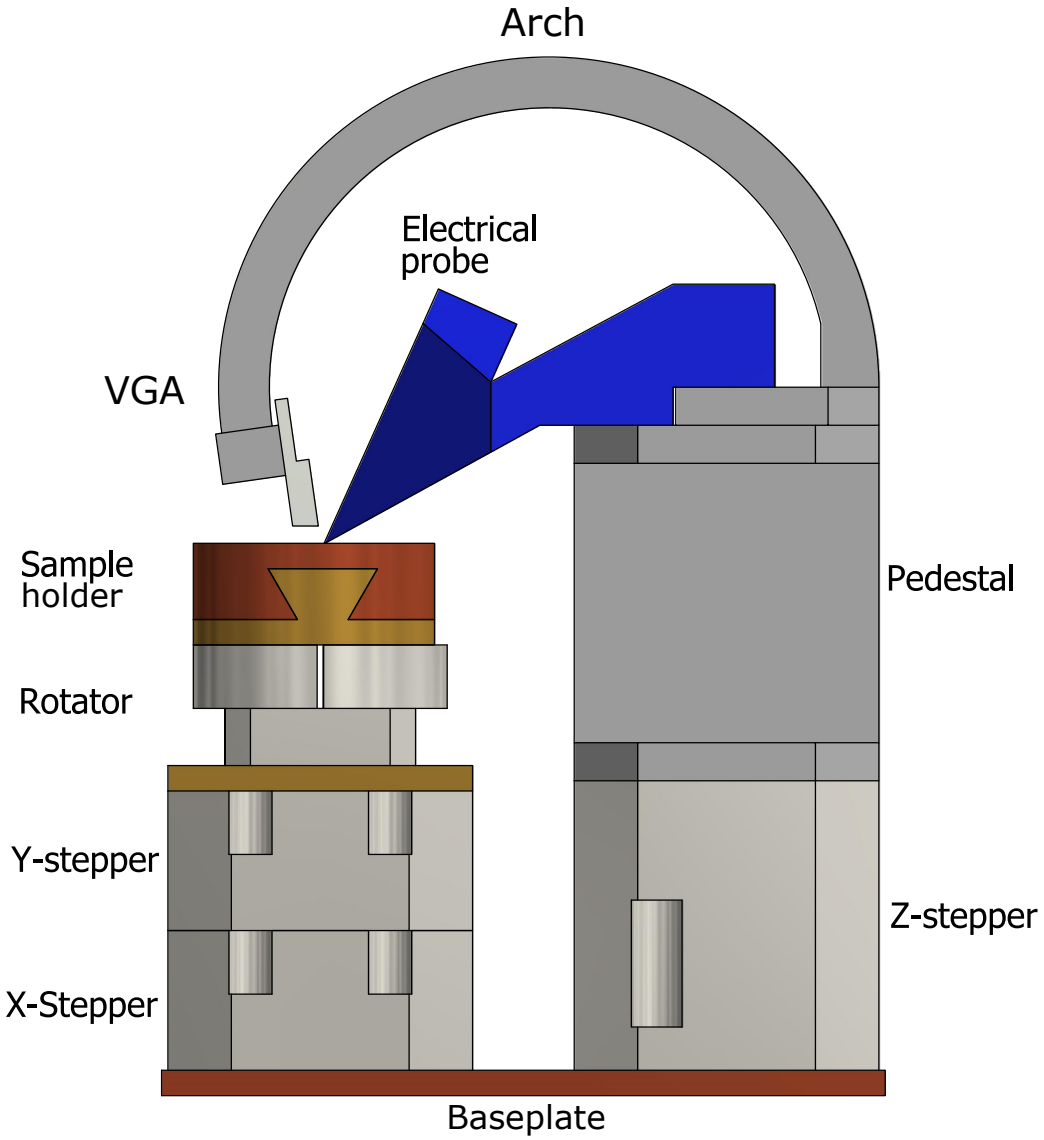


Figure 2.14: Sample stage for optical and electrical characterization of PICs in the VTI.

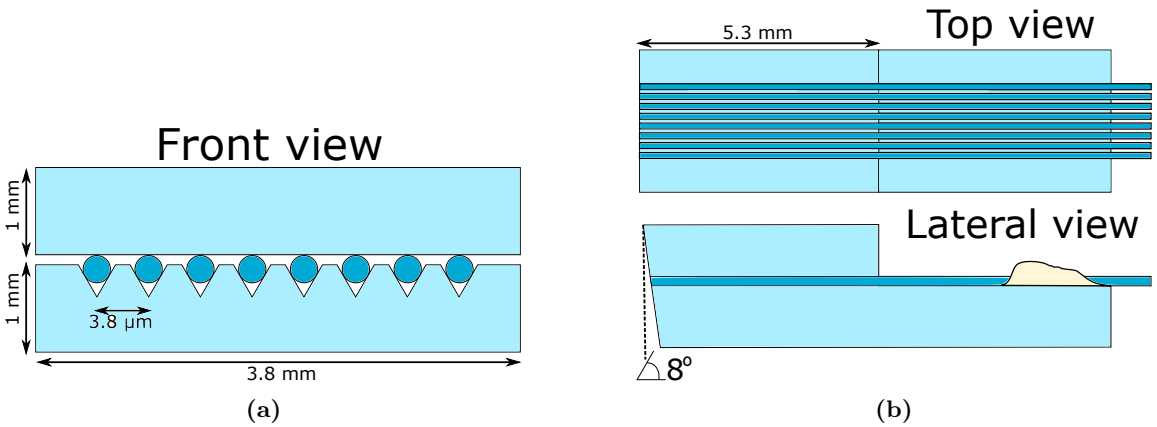


Figure 2.15: a) VGA's front view. b) VGA's top and lateral view. (images are not to scale).

to the cryostat's cold head. Since several elements are separating the sample from the direct contact to the heat sink, a silver wire is connected to both the sample holder and the baseplate.

2.4.3 Cryogenic Probe Station

When the characterisation of a PIC does not involve single-photon detection, then the task can be accomplished by using a cryogenic probe station such as the Lake Shore® CPX (Fig. 2.16).

The probe station is a modular system that allows customisation by installing different probing tools such as DC-, RF-probes, and optical fibre. The system used for this work has five probing arms: two single DC probing arms with BeCu and W probe tips (ZN50R-CVT), one 12-channels multi-contact DC, one microwave probe with ground-signal-ground geometry (MMS-09) and one V-groove Assembly of fibre array with eight single-mode channels.

The microwave probe has a pitch of 127 µm between signal and grounds, which match the current standard in microelectronics. The probe has a bandwidth of 40 GHz which is more than enough for modulators with slow switching mechanism as the thermo-optic ones (¡1 GHz), but it also allows the possibility of working with other technologies such as

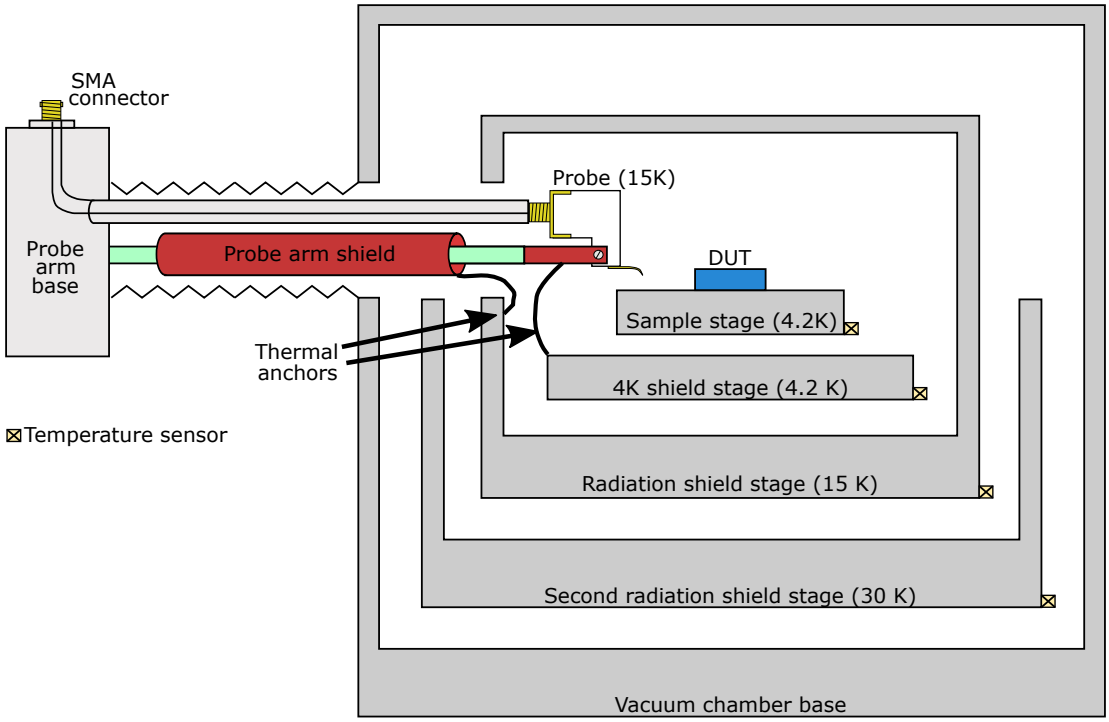


Figure 2.16: Diagram of the Lake Shore® Probe Station for characterization of PICs in a cryogenic environment. The probe shown in the figure is a single DC electrical problem, although a similar arrangement is present for different kind of probes.

plasma-induced and electro-optic modulators.

The sample stage is located on top of a cold head that is cooled through a heat exchanger connected to an open circuit for the continuous flow of a cryogenic liquid (either liquid helium or nitrogen). The sample is kept under a vacuum in a stainless steel chamber and protected by three radiation shields. Each radiation shield has a temperature sensor and a heater connected to one of two Lake Shore® Cryogenic Temperature Controller Model 336.

The sample stage reaches temperatures as low as 2.0 K by using the same Joule-Thomson effect utilised in the VTI, obstructing the flow into the sample stage with a needle valve that can be controlled manually through a micrometre at the bottom of the station. The constrained flow of liquid helium will eventually balance with the helium-gas extracted through the exhaust line (using a rotary pump), resulting in a flow of cryogenic liquid with the least energetic molecules, and therefore with a lower temperature.

The DUT is usually glued to the sample stage using a cryogenic varnish (GE 7031, CMR-Direct) that does not require UV light to cure. After the sample is in position, the chamber is pumped with an HV turbopump down to a pressure of 1×10^{-3} mbar before any cryogenic liquid can enter the circuit. Once the pressure is low enough, and the probe station is being cooled down to temperatures below 100 K, the pressure drops down to 1×10^{-6} mbar due to cryopumping, which is caused by the cold walls trapping and freezing the few molecules of air floating in the chamber.

Once the pressure in the chamber is near 3×10^{-6} mbar, the valve that connects the chamber to the pump must be closed to avoid air going from the pump into the chamber due to cryopumping. Suppose the valve is not closed on time. In that case, the remaining gas inside the chamber begins to transfer heat between the external walls and windows of the chamber and the cold head, which generates unwanted condensation that limits the visibility of the sample through the camera.

While the system was designed to be mechanically and thermally stable within hundreds of nm and tens of mK, respectively, optical coupling at 4.2 K is usually more

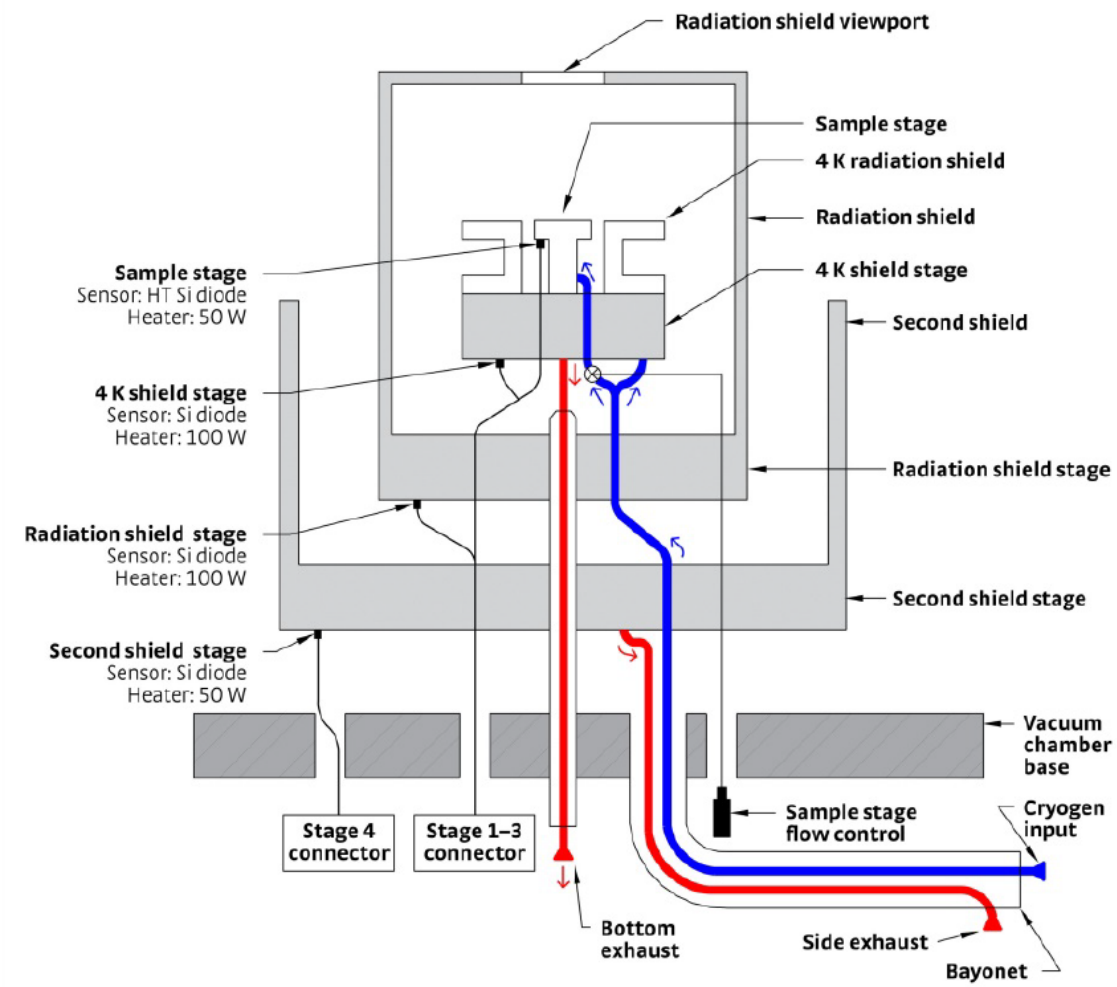


Figure 2.17: Diagram of the circulation lines for the liquid cryogen (either liquid helium or liquid nitrogen). Image extracted from Lake Shore® Cryotronics's documentation.

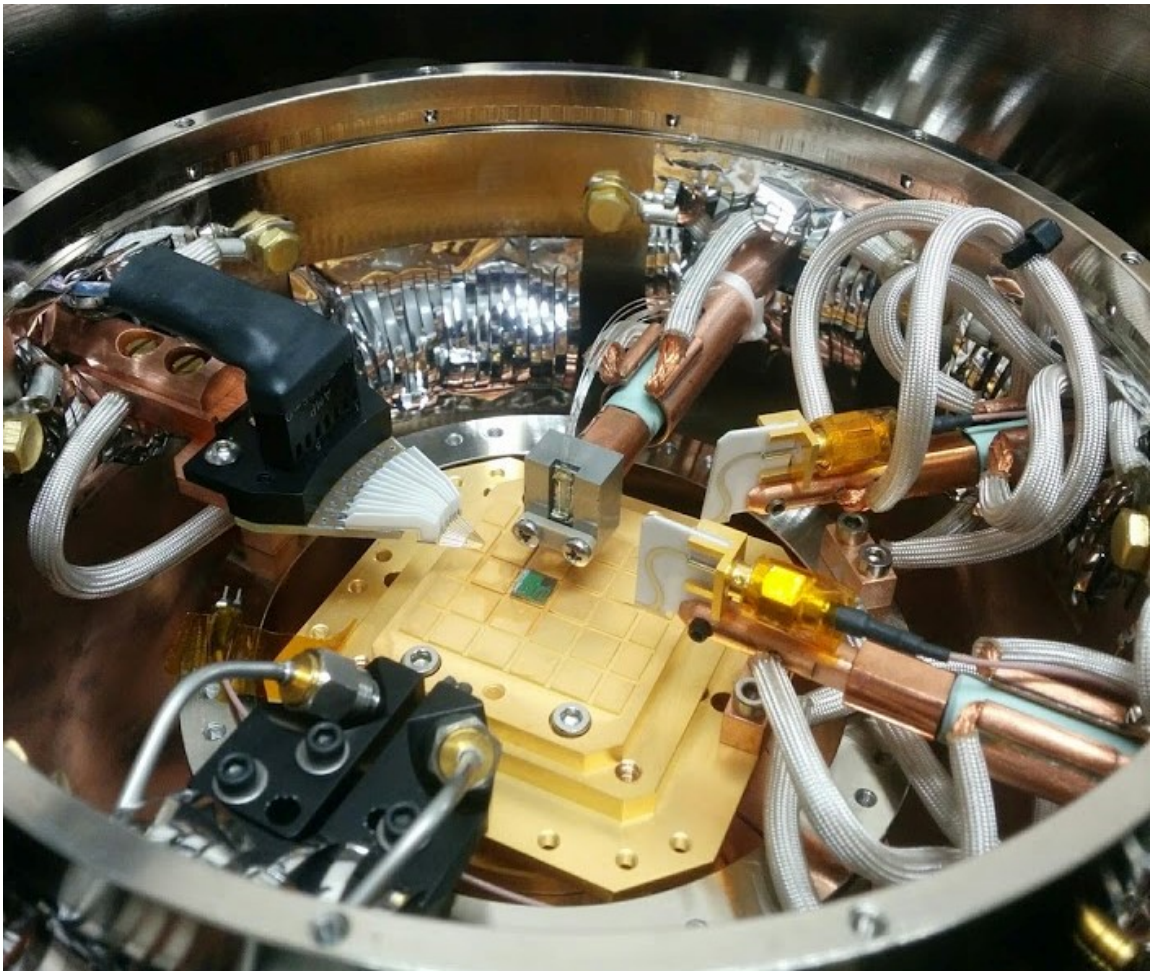


Figure 2.18: Cryogenic Probe Station (CPX) used for the optical and electrical characterization of integrated photonics circuits at cryogenic temperatures

challenging since no temperature controller is not used to stabilise it. The cold head is kept at 4.2 K by maintaining a continuous and strong flow of liquid helium. That means keeping a pressure above 4 psi and a constriction valve wide open (at least 4 turns), so the cold head has enough cryogen to cool down every single probe anchored to it.

Once the measurements have concluded, all probes should be lifted a few millimetres at least before the probe station begins to warm up. In order to increase the temperature of the cryogenic system back to room temperature, it is necessary to stop the transfer of liquid helium (by releasing all the pressure in the transport vessel) and set the temperature to room temperature for every stage in the CPX using the temperature controllers. Once every stage has reached room temperature, the chamber can be vented and opened.

Chapter 3

Multiphysics Simulations

First, the software used for the studies will be introduced, including all the pertinent modules used to define and solve the appropriate equations system. Then, the problem of heat dissipation at cryogenic temperatures by thermal phase shifters will be discussed, followed by a practical example of how to use multiphysics simulations to provide valuable data in the process of coupling light into a chip with no visual feedback on the position of the optical fibres.

3.1 Introduction to COMSOL

COMSOL® Multiphysics® is a simulation environment based on a finite element (FEM), partial differential equation (PDE) solver capable of modelling different physical phenomena capable of interacting with each other to mimic a real-life device or effect.

COMSOL provides a graphic user interface (GUI) where a geometry can be defined for either 1, 2 or 3-dimension simulation regions. The construction of the geometry can be done by either using the provided set of basic forms and transformation tools or by importing a CAD file from a compatible software package. Continuous regions of a 3D geometry are called *Domains*, the 2D surfaces that limit them are known as *Boundaries*,

which in turn are bounded by 1D *Edges*.

In the case of a 3D simulation, material properties must be assigned to every domain. The required material properties depend on the kind of modules run by COMSOL during the simulation execution. For example, if the Heat Transfer module was to be executed, then all thermal properties for all the materials used to characterise the geometry must be defined.

While the dimensions of every single element of the geometry can be defined individually by typing its value in the appropriate section, it's more convenient to create a Parameter list, where such values can not only be modified automatically either before or during a simulation but also because in that way they can be exported, saved in a text file and potentially be used later in a different simulation.

The initial values and boundary conditions are defined together with the kind of solution that should be found (e.g. stationary, time-dependent, etc.). The COMSOL modules used for these simulations include electromagnetics (AC/DC), heat transfer, structural mechanics, and wave optics.

The geometry is then discretised into small, simple shapes called mesh elements.

The heat transfer equations in solids solved for the stationary state has the following form:

$$\rho C_p \frac{\partial T}{\partial t} - \nabla \cdot (\kappa \nabla T) = Q \tag{3.1}$$

where ρ is the material's density ($\mathrm{kg\,m^{-3}}$), C_p is the specific heat capacity at constant stress ($\mathrm{J\,kg^{-1}\,K^{-1}}$), T is the absolute temperature (K), κ is the thermal conductivity coefficient ($\mathrm{W\,m^{-1}\,K^{-1}}$), and Q is the net volumetric heat source ($\mathrm{W\,m^{-3}}$)

The AC/DC module, for the same kind of solution, solves the current conservation equation:

$$\nabla \cdot \vec{J} = Q \tag{3.2}$$

where the current density $\vec{J} = -\sigma \nabla V + J_e$, σ being the electrical conductivity, V is the

electric potential field and J_e is any external current source.

3.2 Mesh convergence

COMSOL has a tool called parametric sweeps, where a particular study can be executed multiple times for a range of values for one or a set of parameters, which can be used to alter the geometry, its mesh, boundary conditions or even input excitations, and express them as a function or a variable.

Creating a well-defined mesh can provide a better resolution and higher accuracy, but that would come with a cost: more significant computation time and more considerable memory usage. In order to decrease the number of mesh elements, the most common operation is using a coarser mesh, dividing the geometry into smaller sections. Increasing the number of mesh elements usually leads to a more accurate result, unless it does until a certain point, where the increase in accuracy and resolution is not as significant as the increase in the time it takes to the simulation to find a convergent solution.

The mesh was created following two approaches: extrusion of a 2D triangular mesh on one of the faces of the waveguide and a 3D-tetrahedral meshing for all the other domains. The extrusion of a 2D triangular mesh is easier to perform in the waveguide because of its regular shape, and its length is orders of magnitude larger than its cross-section. Once the 2D mesh is created in one of its 220 nm by 550 nm facets, the "Sweep" tool creates regular prisms with faces defined by each element of the 2D mesh. Because the mesh elements in the waveguide are smaller than in the rest of the geometry, this domain must be discretised first so adjacent domains can adapt to the finer mesh of the waveguide.

The parametric sweep of the number of mesh elements was done by firstly linearly varying some key values in the settings window for every domain in the geometry (Table 3.1). For every value of h, each setting (e.g. Max. element size) takes a value according to:

$$y = h \cdot (y_{\max} - y_{\min}) + y_{\min}$$

Domain	Parameter	Min. value	Max. value
Waveguide	Max. triangular face	0.05 µm	0.2 µm
Heater	Min. mesh size	0.1 µm	1 µm
Cladding	Max. mesh element	1 µm	5 µm
BOX	Max. mesh element	1 µm	5 µm
Substrate	Max. mesh element	5 µm	50 µm

Table 3.1: Maximum and minimum limits for the variation of mesh elements setting for all the domains in the geometry

where $y_{\max}$ and $y_{\min}$ are the maximum and minimum value, respectively, for each setting shown in Table 3.1, and h is the the parametrisation factor that varies from 0 to 1.

In order to analyse the effect of the number of mesh elements in future studies, a relevant observable for the geometry analysis must be selected. Since the structures to be simulated will have a direct effect on the waveguide's optical properties, a good option to monitor the model's performance is to look at the effective refractive index.

The results of the parametric study are shown in Fig. 3.1, both for the absolute value of the effective refractive index in the waveguide as a function of the factor h (Fig. 3.1a) and its absolute difference with respect to index obtained with the mesh with the highest resolution (h=0) as a function of the number of mesh elements (Fig. 3.1b). Based on how the effective refractive index varies with h, setting its value to $h = 0.3$ would provide a good level of accuracy without adding unnecessary computational time.

3.3 Thermal phase shifter at cryogenic temperatures

The model that will be described in this section will try to answer the question of whether thermal phase modulators can be used in a cryogenic environment. The target is to obtain a π-phase shift at a wavelength of 1550 nm in an SOI waveguide considering the power limitations associated with cryogenics systems and the idea of scalable technology.

In the following sections, two different geometries will be discussed and compared. The first one consists of a single heater modulating a waveguide from a few microns above

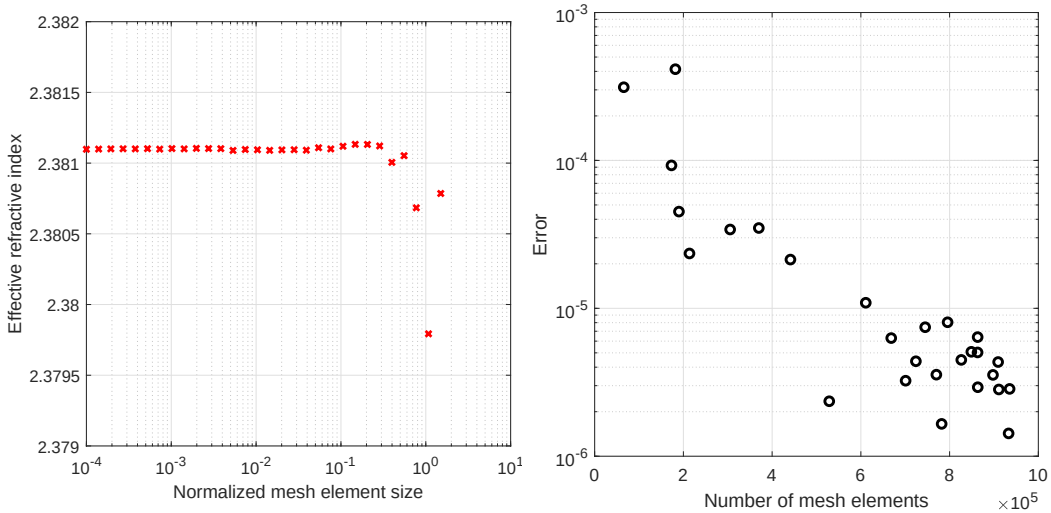


Figure 3.1: a) Waveguide's effective refractive index at 1550 nm and T= 293 K as a function of the number of mesh elements used in the parametric sweep b) Magnitude of the relative difference of the effective refractive index for every number of mesh elements and the value obtained for a mesh with maximum resolution

and a two-heater geometry with two heat sources at both sides of the waveguide. These geometries correspond with standard components in design libraries by photonic foundries IME and IMEC, respectively.

3.3.1 Description of the geometry

Geometry #1 is based on a standard arrangement for a thermal modulator: a straight waveguide with a thin film of resistive material on top, for which dimensions were taken from standard parameters used in the fabrication process by the commercial foundry IMEC: the simulation volume consists on a 100 µm by 500 µm section of a standard SOI wafer with 725 µm of a crystalline silicon substrate, followed by a 2 µm-thick layer of buried oxide (BOX). A silicon waveguide with a cross-section of 500 nm by 220 nm and a length of 500 µm lie on top of the BOX layer, and it is covered by 3 µm of cladding. The heater has a length of 100 µm with a cross-section of 500 nm by 120 nm, and lies right on top of the waveguide at a distance of 2 µm (see Fig. 3.2).

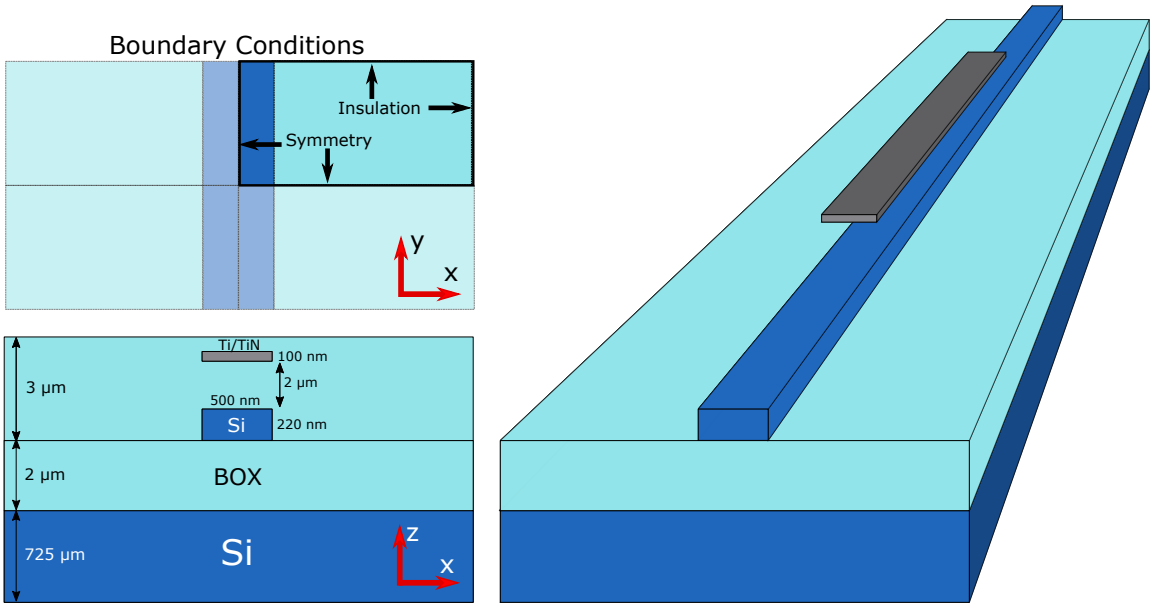


Figure 3.2: Geometry #1 with a single heater deposited on top of a waveguide.

Geometry #2 consists of the same substrate, BOX layer, cladding and waveguide elements of geometry #1, except for the location of the heat source. In this particular case, the modulation is performed by two slabs of resistive material located at both sides of the waveguide, with a thickness of 220 nm, a width of 1.2 µm and a separation gap of 2 µm (See Fig. 3.3).

The material chosen for both the BOX layer and the cladding was silica (SiO_2). The heater's composition will be not discussed now, and it will be assumed that the structure can dissipate the amount of power defined as the input parameter.

The temperature-dependent data of specific heat and thermal conductivity for silicon and silica were extracted from the available literature [78–81] (Fig. 3.4) and introduced to the model as interpolation functions. For values outside the range of the data provided by the references, COMSOL extrapolates for the queried value by the model using a linear approximation.

From Fig. 3.4b it can be seen why silicon is considered a suitable substrate material not only for this work for also for microelectronics applications. The high thermal

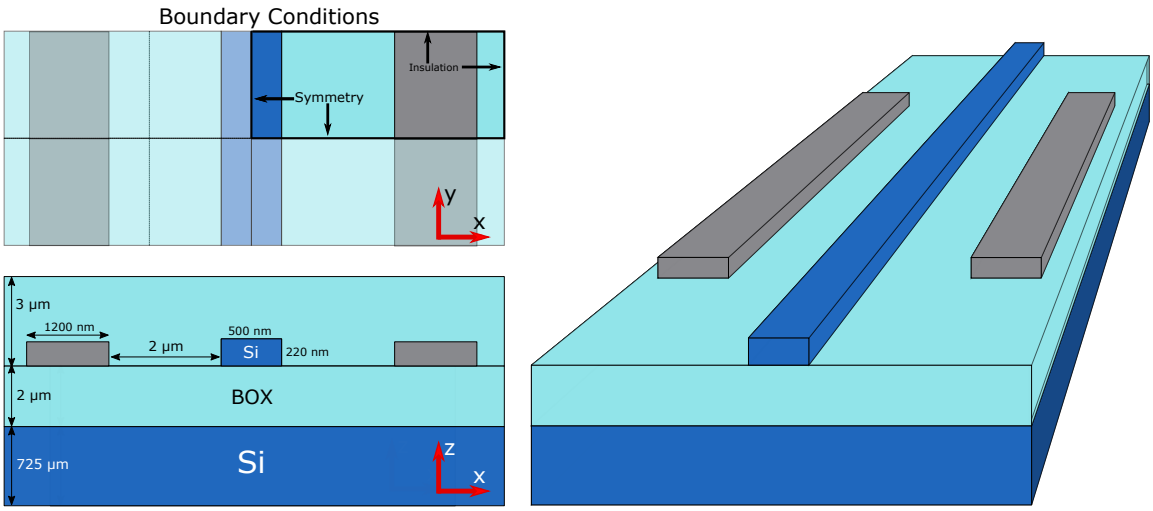


Figure 3.3: Geometry #2 with two heaters at both sides of the waveguide.

conductivity of silicon helps the sample to reach thermal equilibrium with the heat sink quickly. Furthermore, this characteristic also helps to reduce the simulated volume without increasing the border contribution to the final solution since the substrate completely absorbs all dissipated heat.

Since a significant portion of the model consists of silicon and silica, a direct comparison between their thermal conductivities and specific heats is shown in Fig. 3.4c.

3.3.2 Boundary conditions

The boundary conditions for both geometries were defined as follows:

$T = T_0$ at the bottom of the silicon substrate, where T_0 is the base temperature of the heat sink the chip is attached to. T_0 is a constant provided as an input parameter of the model.

Insulating boundary condition (heat flux $\dot{q} = 0$) was chosen for all four lateral and top facets of the model, assuming that the chip being simulated is under vacuum, which discards convection losses, and that radiation losses are small compared to the heat flux through the silicon substrate.

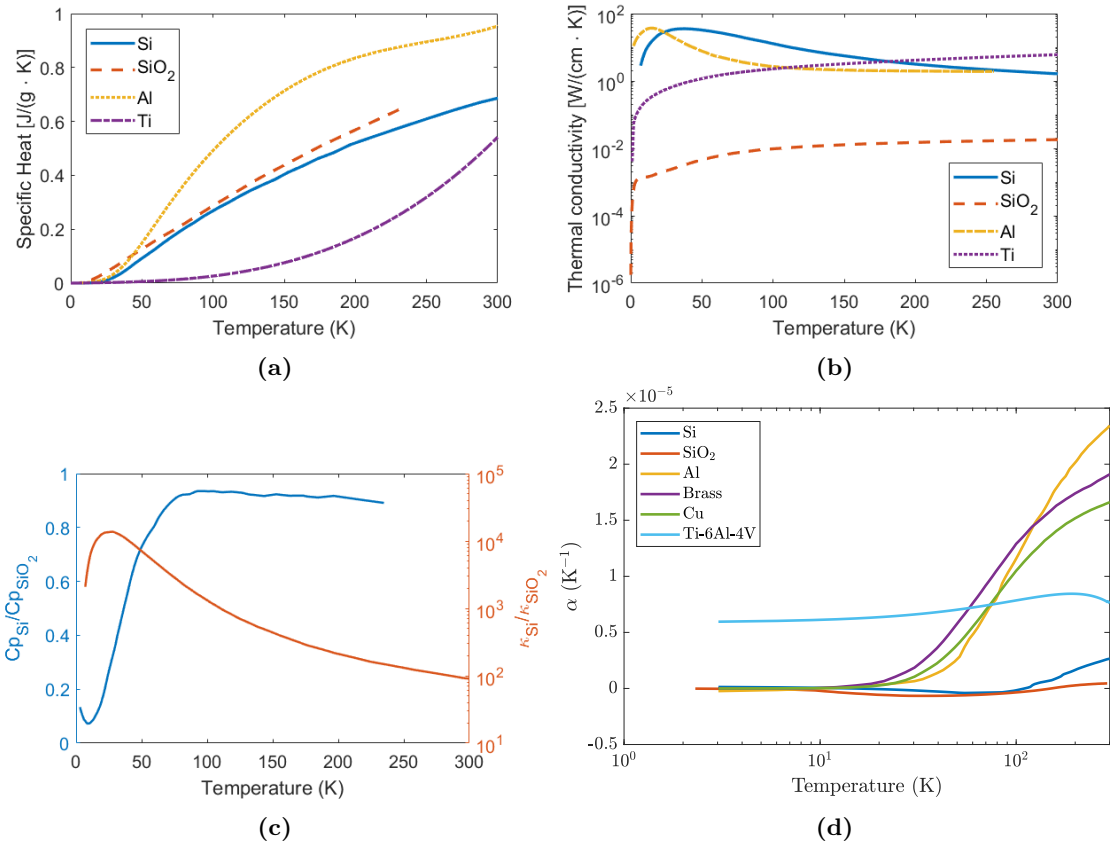


Figure 3.4: **a)** Specific heat and **b)** thermal conductivity for materials used in mutiphysics simulation. Figure **c)** shows the ratios between silicon and silica for both their specific heats and thermal conductivities as a function of temperature. **d)** Thermal expansion coefficient for some relevant materials. Data extracted from [61, 78–82].

Since both geometries share the characteristic of being symmetric about x=0 and y=0, a symmetry boundary condition was applied to said planes to reduce the size of the model and the computational time, solving for only a quarter of the original model.

The heater was defined as a 3D heat source with an overall heat rate transfer of q_0 for each geometry. For Geometry #1, q_0 was dissipated exclusively by one structure, while for Geometry #2 the dissipated power was split equally between the two identical strips.

Both geometries were then discretised by applying different meshing parameters to each domain based on their dimensions. While the waveguide and the heaters where discretized using tetrahedral elements with lengths between 1 nm and 100 nm (high resolution), the BOX and cladding layers have elements with lengths between 100 nm and 10 µm and the silicon substrate with dimensions between 1 µm and 40 µm.

Since the thermal excitation by the heater is small and the hotspots are expected to be localised, T_0 was chosen as the initial value of T for every element of the mesh.

3.3.3 Results

3.3.3.1 Single heater: Geometry #1

The models were run to find a stationary solution for a range of base temperatures T_0 and an initial injected power of 10 mW. The value of the injected power was chosen based on the typical technical specifications of cryogenics systems, such as the one available for future experimentation, which usually presents cooling powers in the order of tens of mW.

The temperature distribution in the stationary state for geometry #1 in the xy-plane intersecting the waveguide at a value of z equal to half the waveguide's thickness is shown in Fig. 3.5 for both T_0= 4 K and $T_0 = 300$ K. The temperature distribution shows the effect of the change in the ratio $\kappa_{\mathrm{Si}}/\kappa_{SiO_2}$ observed in Fig. 3.4c, where at low temperatures, silicon waveguides behave like thermal channels guiding heat more easily than allowing it to be dissipated through the substrate.

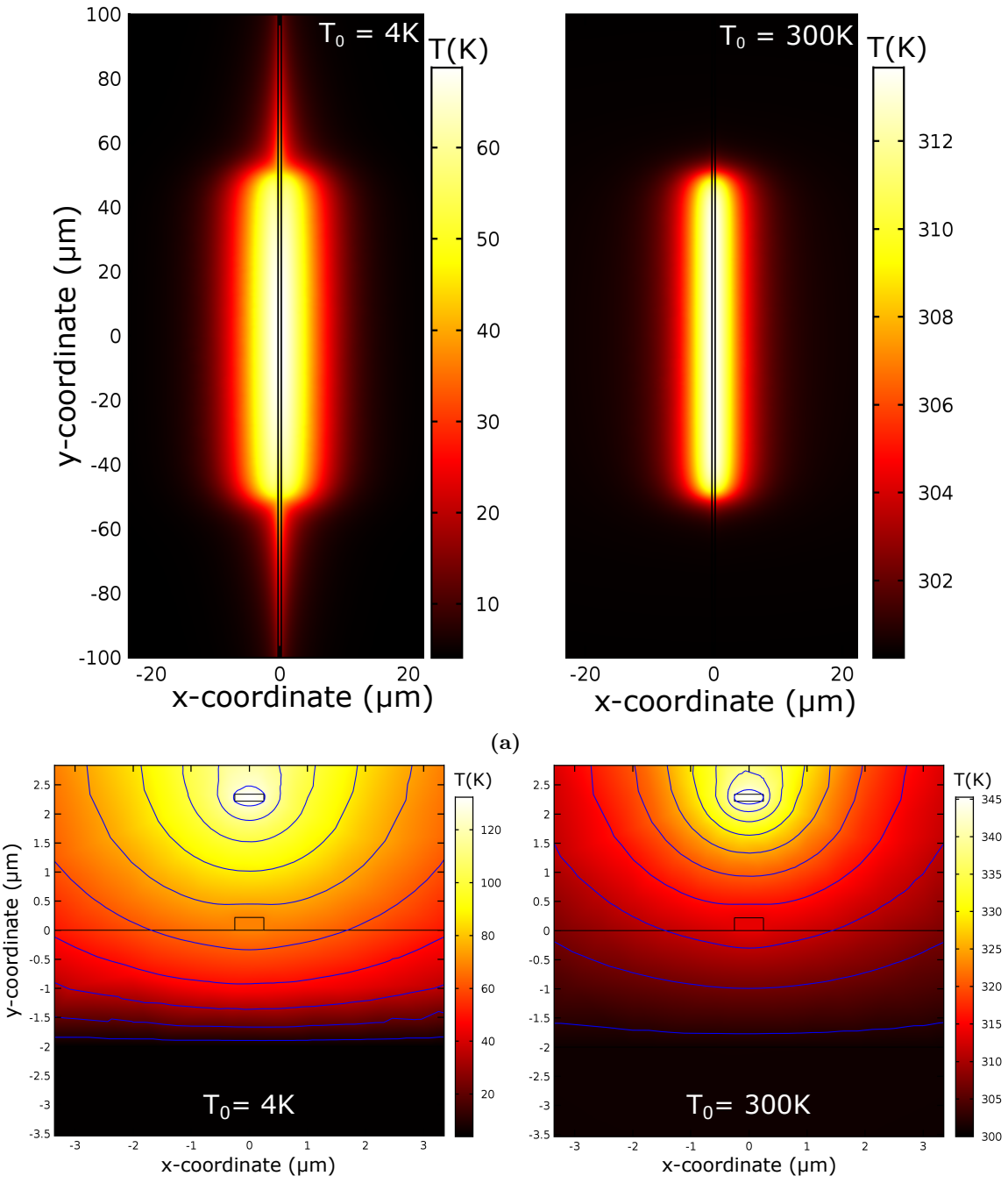


Figure 3.5: Temperature profile $\Delta T = T - T_0$ for Geometry #1 at $T_0 = 4\,\mathrm{K}$ and $T_0 = 300\,\mathrm{K}$ in the **a)** xy-plane underneath the heater at z=110 nm above the BOX layer and **b)** in the xz-plane at the middle of the waveguide and the heater.

The change in the temperature profile along and perpendicular to the waveguide's axis are shown in Fig. 3.6 for different base temperatures T_0. The perpendicular profile (Fig. 3.6a), measured along the x-axis and at the height of 100 nm, provides an insight particularly on the order of magnitude for thermal cross-talk. For Geometry #1, the range of the transversal ΔT profile increases from 20 µm at $T_0 = 300\,\mathrm{K}$ to around 40 µm at $T_0 = 4\,\mathrm{K}$. The local minimum observed at the middle of the waveguide at low T_0 is possibly caused by the diffusion of heat from the region below the heater towards the cold waveguide's boundaries. Since the ratio of thermal conductivities between silicon and silica becomes more pronounced (Fig. 3.4c) at cryogenic temperatures, the waveguide acts as a heat guide that transports energy away from the region near the phase shifter. Because of this effect, thermal cross-talk between heaters and SNSPDs could be enhanced, particularly if both components are located on the same optical channel leading to more dark counts in the detector or even the destruction of the superconducting state of the nanowire.

The curves shown in Fig. 3.6b represent a set of temperature distributions at different values for T_0 along the centre of the waveguide. For values of T_0 close to room temperature, regions with high temperature are sharply delimited at the area underneath the heater, while decreasing T_0 causes the profiles to spread along the waveguide and have smoother temperature transitions.

A description of the full-width at half-maximum (FWHM) values for the curves discussed before is presented in Fig. 3.6c. The longitudinal profiles of ΔT below 50 K show a sudden increase in their width, which coincides with a temperature range where the thermal diffusivity ratio between silicon and silica increases super-exponentially as $T_0 \to 0$ (see Fig. 3.4c).

A comparison between the data for $T_0 > 200\,\mathrm{K}$ and $T < 50\,\mathrm{K}$ shows that at higher temperatures, the direct effect of the heater on the waveguide is more localised with steeper edges and more defined regions of high temperature. An exception in the trend of the steepness can be appreciated between T_0=20 K and T_0=4 K, where even when the distribution at 4K is broader, its edges are more delimited. This behaviour change coincides

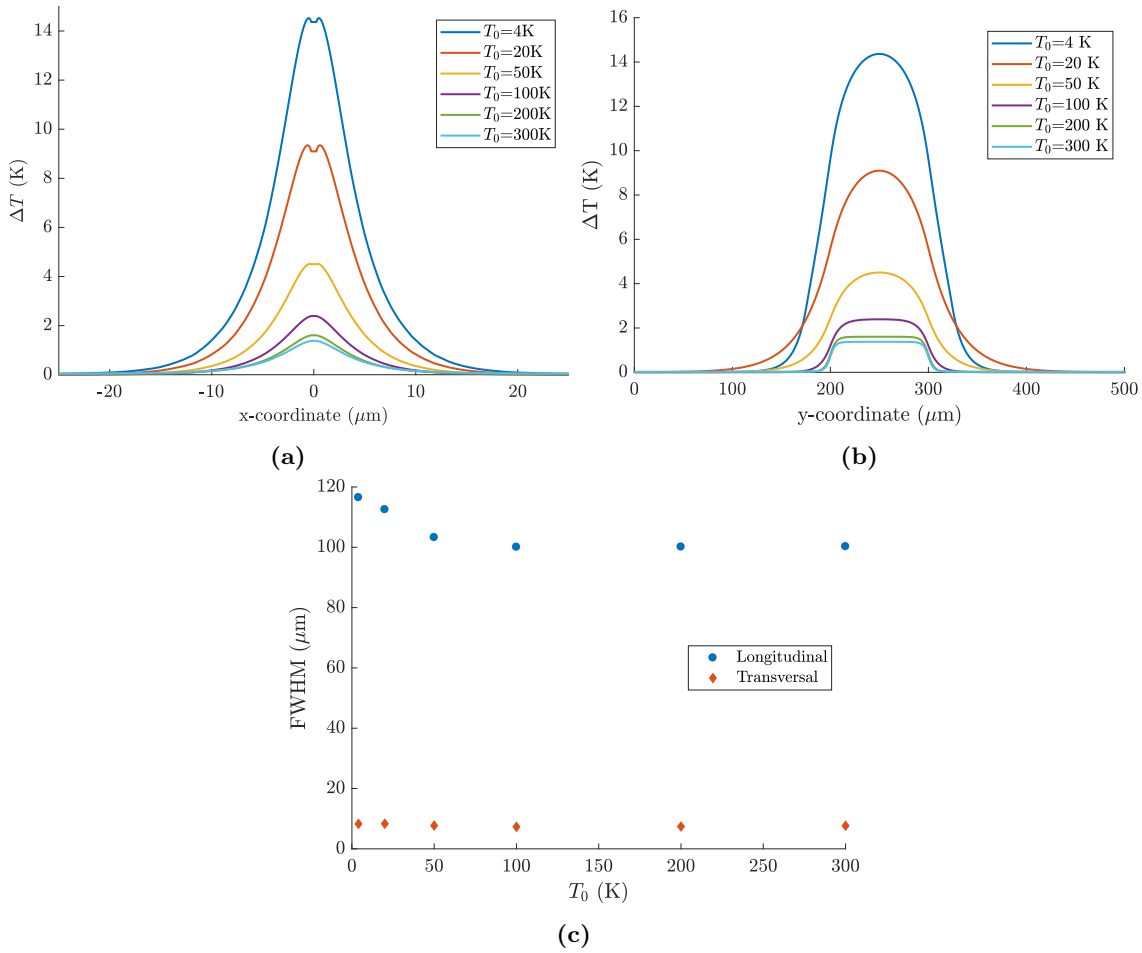


Figure 3.6: Temperature increase profiles in the **a)** transversal and **b)** longitudinal direction for a silicon waveguide in a SOI wafer for using a thermal phase shifter dissipating 1mW of heat. Points in **c)** shows a comparison between profile widths in both directions.

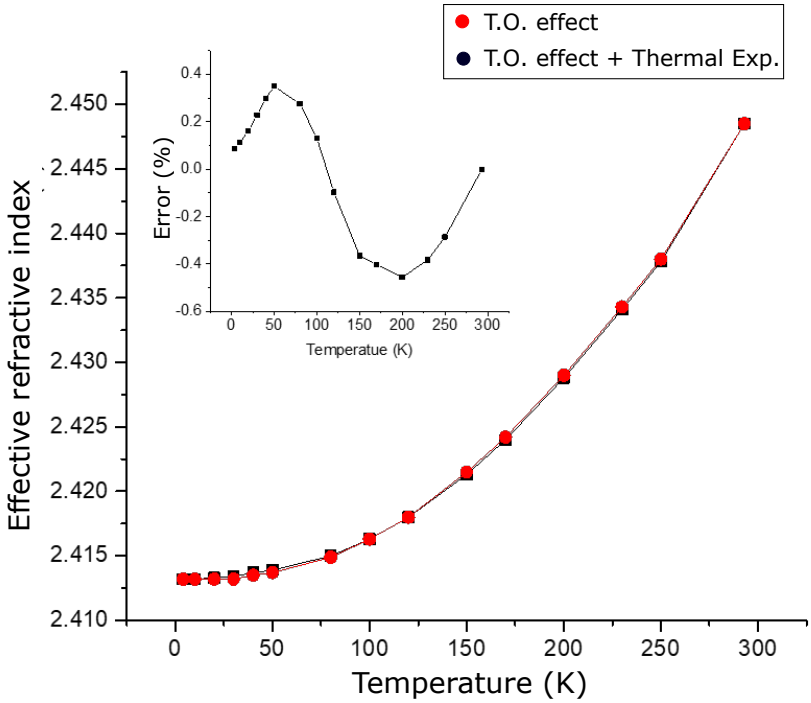


Figure 3.7: COMSOL simulation of the change in effective refractive index for a 500 by 220 µm^2 SOI waveguide at 1550 nm assuming a change in refractive index due to the thermo-optic effect and thermal expansion of the silicon structure. The inset shows the difference (in %) in n_{eff} due to the contribution of the thermal expansion.

with a maximum point for the ratio between the thermal conductivity of silicon and silica (Fig.3.4c) that occurs at around 28 K for the data used in this simulation.

The total phase shift achieved by thermo-optic effect in the simulated spatial mode is calculated by integrating Eq. 2.1 along the waveguide assuming $n_{\text{eff}}(x)$ changes with the distribution of T. An expression can be obtained for n_{eff} via a COMSOL simulation using the Wave Optics module assuming a temperature-dependent refractive index for silicon and silica (Fig. 3.8) obtained from integrating data points for the thermo-optic coefficients data points previously showed [51] (Fig. 3.8). Although changes in the waveguide's dimensions due to thermal expansion could also potentially have a contribution to the dynamics of n, its effect was observed to be negligible compared to the contribution of the change in the refractive indexes (Fig. 3.7).

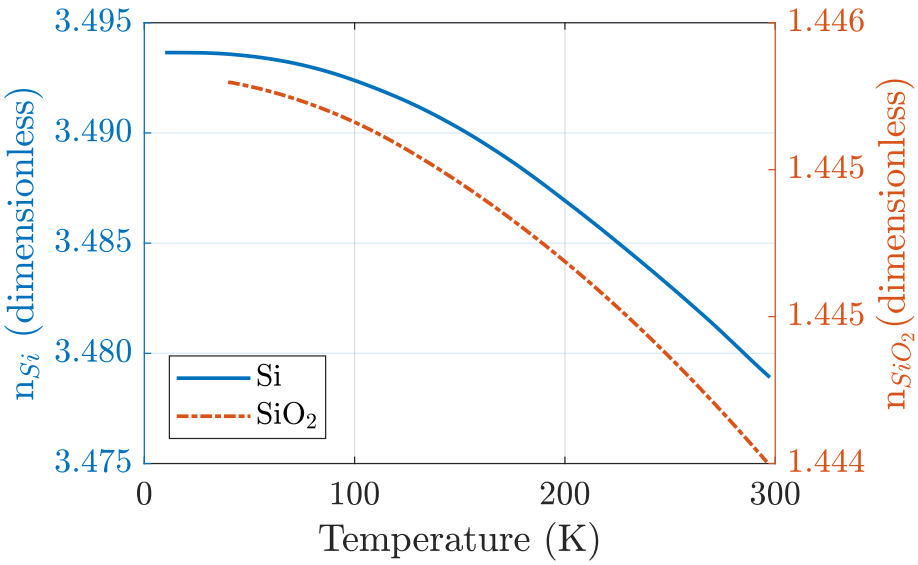


Figure 3.8: Temperature-dependent refractive index for silicon and silica at 1550 nm obtained from [51].

Thermal cross-talk is influenced by the base temperature of the cryogenic system and the amount of heat injected by the modulator. Both transversal and longitudinal ΔT profiles with respect to the dissipated power by the heater are shown in Fig. 3.9a and 3.9b respectively for a base temperature $T_0 = 4\,\mathrm{K}$. Based on the temperature distribution observed along the waveguide's axis, it is possible to estimate an approximate minimum distance required between a source of heat such as the thermal modulator and a superconducting detector to provide enough distance for the heat to be dissipated through the substrate instead of reaching the SPD and destroy the superconducting state. The FWHM was calculated for all previous distributions and plotted against the power dissipated by the phase modulator at a base temperature $T_0 = 4\,\mathrm{K}$ (Fig. 3.9c) is a way of defining said distance. For the range of input powers considered in the simulation, a value around 100 µm seems to be the stationary result the parameter sweep on power points to as more and more energy is applied to the modulators.

Further adjustments can be made to the estimation if more information is provided about the materials used in the superconducting detector and its geometry, which defines

its critical temperature. The destruction of the superconducting state in the detector is not the only effect to consider in terms of thermal cross-talk, but the increase in DCR, which would diminish its performance at even longer distances. The question is if the extra noise is significant enough to motivate to create additional measures to improve the thermalisation of the waveguide.

The dependence of the cross-talk in the direction perpendicular to the waveguide's axis with the dissipated power in Geometry #1 is almost non-existing (Fig. 3.9c), except for a region around 5 mW where the longitudinal cross-talk reaches a maximum. This could again be explained by the peak the ratio $\kappa_{\mathrm{Si}}/\kappa_{SiO_2}$ reaches at low temperature, making it easier for the heat to spread inside the silicon waveguide. e

The temperature-dependent effective refractive index $\mathrm{n_{eff}(T)}$ for a 500 nm by 220 nm waveguide was calculated using the Boundary Mode Analysis study of COMSOL's Wave Optics module (Fig. 3.10). The temperature dependency of silicon's refractive index used in the study was obtained from the available literature [83]. .

The accumulated phase-shift at T_0= 4 K and T_0= 300 K for the 500 µm-long waveguide as a function of the dissipated power by the thermal modulator are shown in Fig. 3.11a. The power required to achieve a phase-shift equal to π are P_π^{4K}=49.5 mW and P_π^{300K}= 24.0 mW for base temperatures of 4K and 300K respectively.

A parametric sweep of P_π over intermediate values of T_0 between 4 K and 300 K is shown in Fig. 3.11b. The non-linear behaviour between P_ϕ and T_0 is probably reminiscent of the non-linear nature of the properties of $\mathrm{Si/SiO_2}$ with temperature.

From Fig. 3.11b at least two conclusions can be discussed. The first one regards the power requirement for the operation of a thermal phase shifter, which increases as the temperature approaches absolute zero. The second remark is that the maximum value for P_π at 4 K does not represent a significant issue for cryogenics systems and their limiting cooling power.

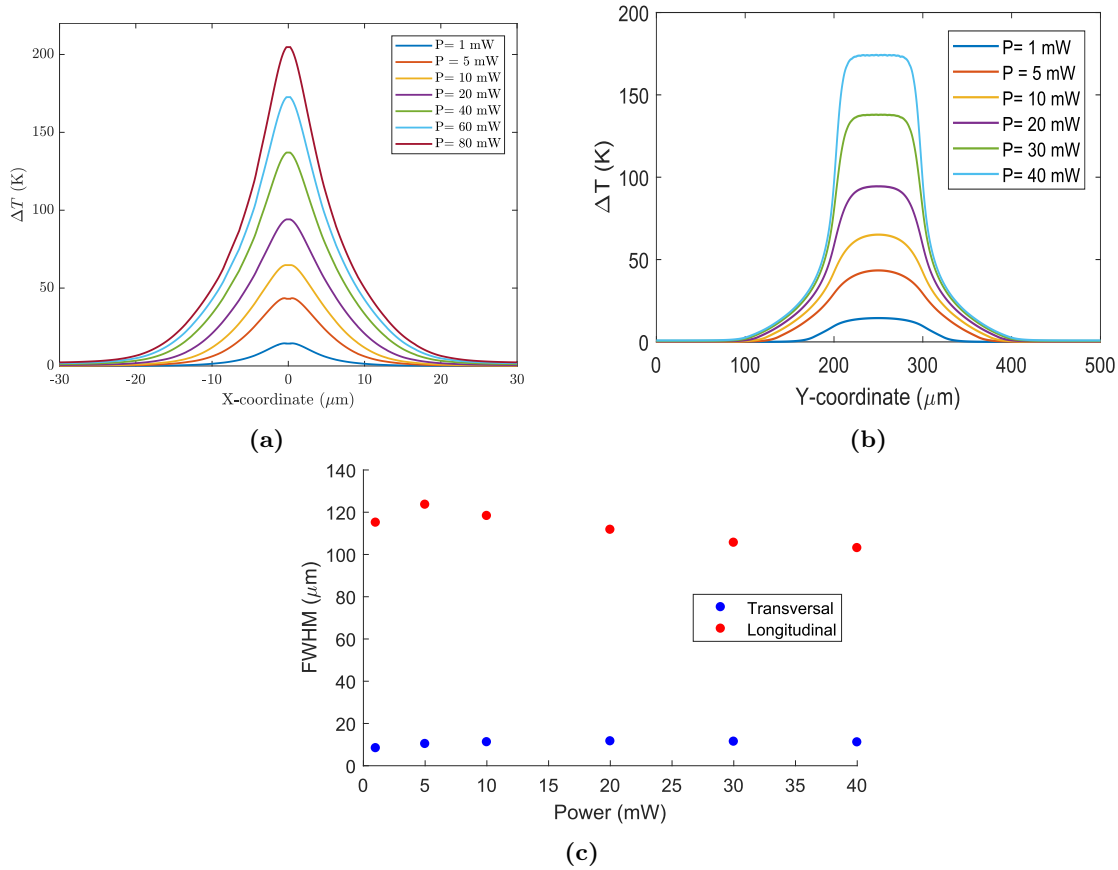


Figure 3.9: Temperature profiles in the **a)** transversal and **b)** longitudinal direction at $T_0 = 4\,\mathrm{K}$ for different dissipated powers by the heater. Points in **c)** shows a comparison between profile widths in both directions.

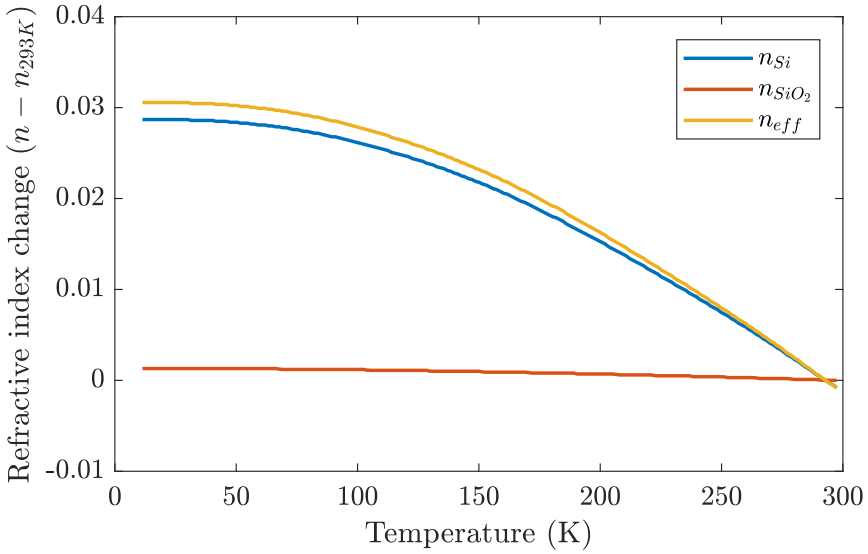


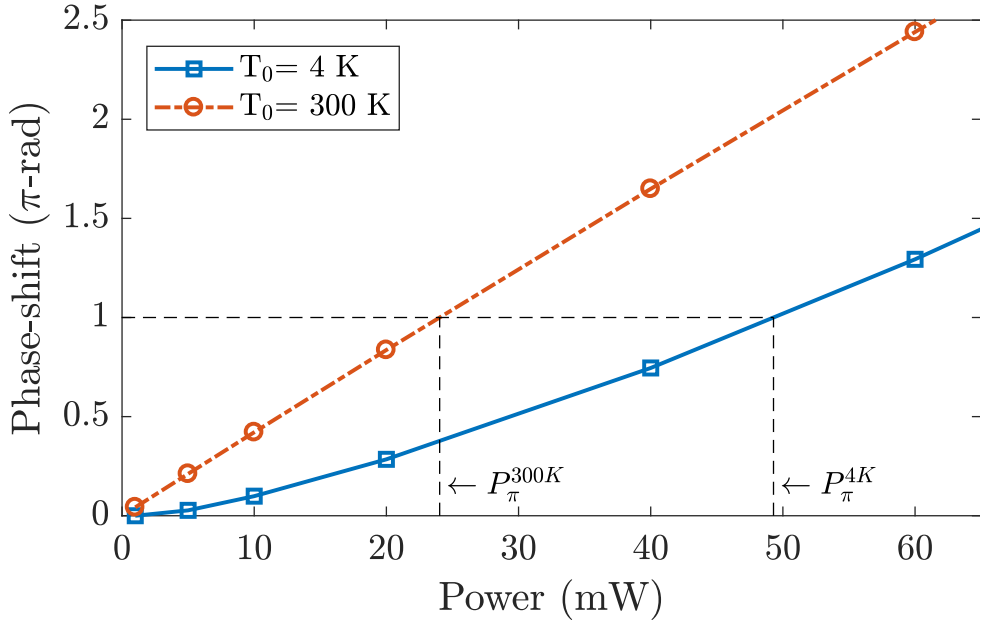
Figure 3.10: Change in refractive index for Si and SiO2 as a function of temperature with respect to their value at room temperature. A similar function for the corresponding effective refractive index is also shown. Curves were calculated from data points in [51]

3.3.3.2 Double-heater: Geometry #2

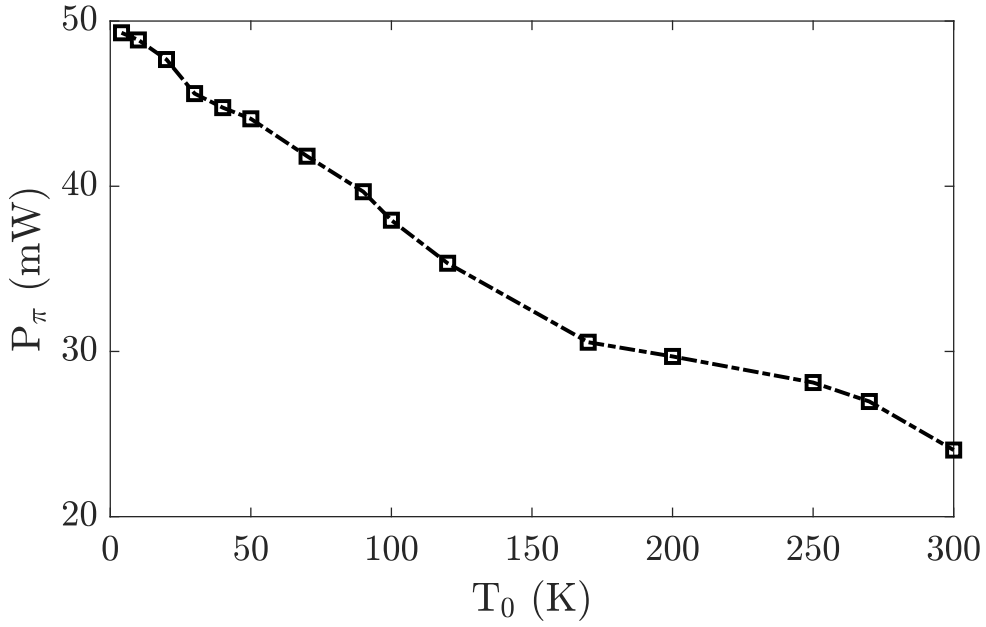
A similar analysis to what was done for Geometry #1 is now presented for Geometry #2, consisting of a double-strip heater.

A temperature increase ΔT distribution for the XY- and XZ- plane are shown in the Fig. 3.12a and 3.12b respectively, for a dissipated power of 10 mW. Unlike what was observed in Fig. 3.5 with the Geometry #1, the profile ΔT does not have an expected spread along the silicon waveguide, which might be caused by the proximity of the heat sources to the silicon substrate, leading to a faster draining of the heat and a more localised area with a relatively high temperature.

In terms of thermal cross-talk, a comparison between the longitudinal temperature distributions along the waveguide for the two geometries at $T_0 = 4\,\mathrm{K}$ and $T_0 = 300\,\mathrm{K}$ is shown in Fig. 3.13. At both base temperatures, the heat sources dissipate 10 mW, resulting in a sharper and more localised distribution for the double-heater design. Even when the dissipated power is equal in both geometries, the maximum temperature reached by the



(a)



(b)

Figure 3.11: a) Accumulated phase-shift (in π-rad) along the 500 μm silicon waveguide for powers dissipated by the thermal modulator from 1 mW to 60 mW. **b)** P_π^{4K}=49.46 mW at T_0 = 4 K, P_π^{300K}=24.03 mW at T_0 = 300 K.

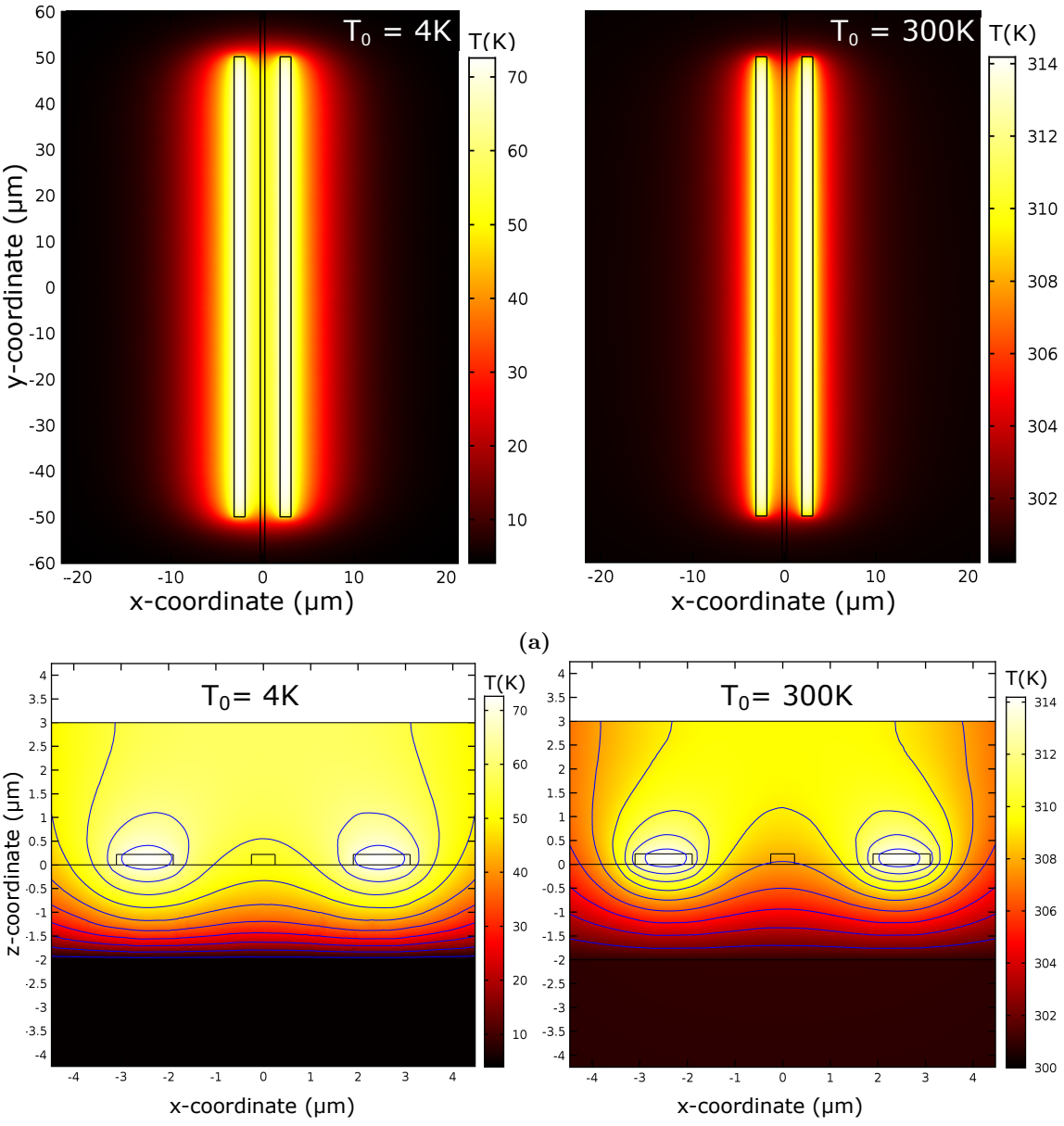


Figure 3.12: a) 2D visualization of the xy plane at a z-coordinate at the middle of the waveguide. **b)** Temperature distribution in the XZ plane at a y-coordinate at the middle of the waveguide and both thermal modulators which dissipate 10 µW.

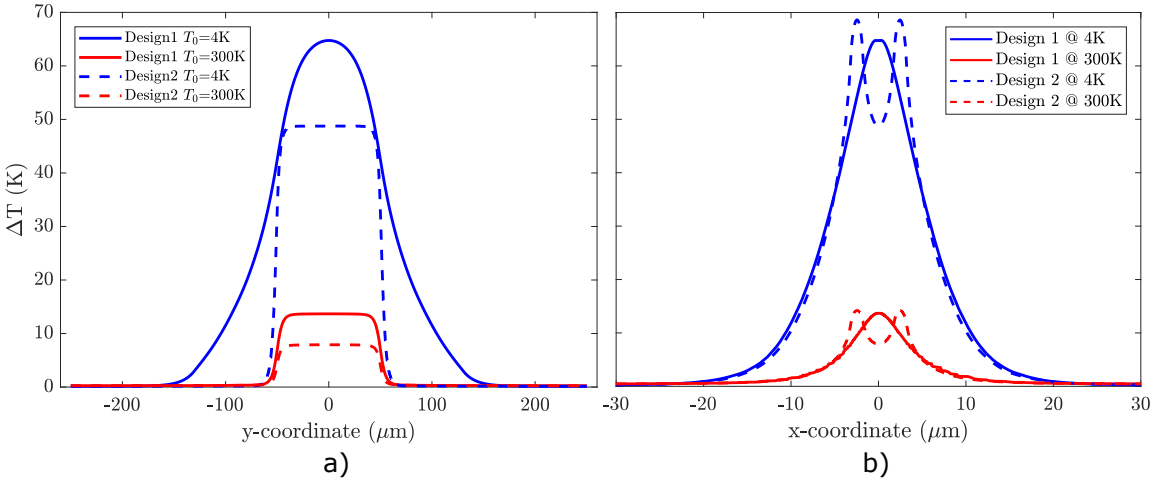


Figure 3.13: a) Longitudinal and **b)** transversal temperature profiles for both geometries with a single and double heater, at 4 K and 300 K.

Geometry #2 is smaller than for Geometry #1.

In terms of the perpendicular cross-talk, Fig. 3.13 shows no particular advantage from any of the geometries simulated.

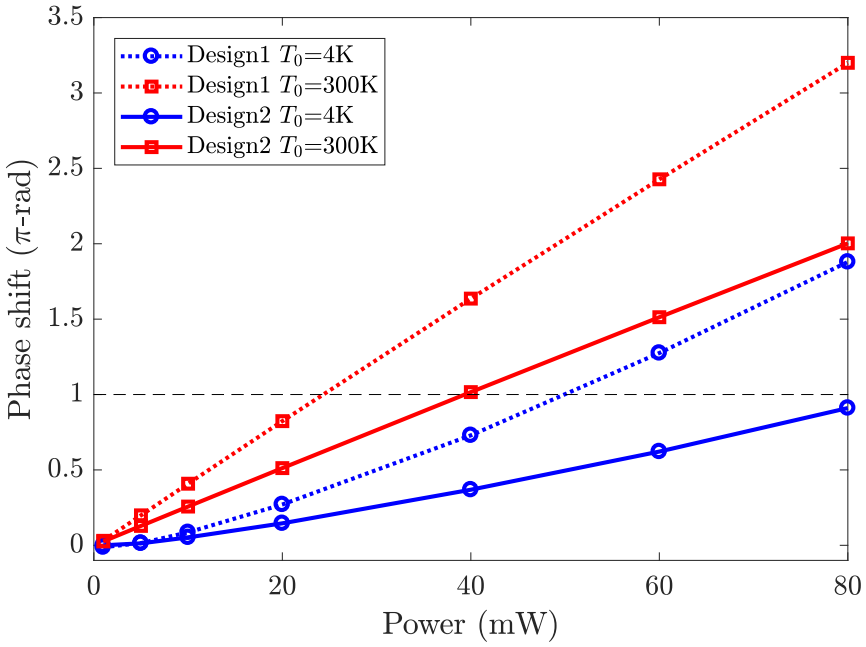
The total phase-shift achieved by the modulator for both geometries and two different temperatures is shown in Fig. 3.14a. About how efficient is the phase modulator to produce a change in phase per unit of power dissipated, higher temperatures are overall more efficient no matter the geometry used. On the other side, in a low-temperature situation, the single heater geometry shows the best performance in rad/mW.

3.3.4 Discussion

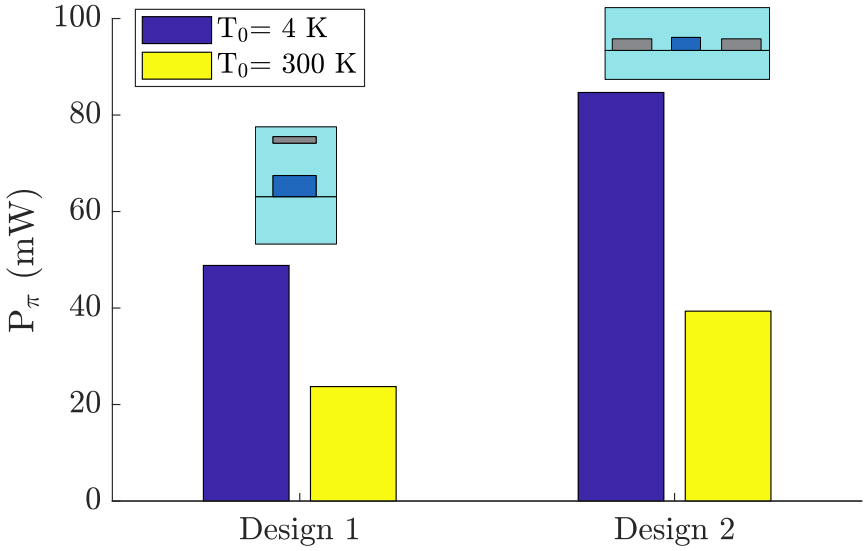
It has been shown that numerical simulations can be a valuable tool to help design and thermal analysis of integrated silicon photonics.

Even when a drop in the silicon's thermo-optic coefficient has been reported, the numerical results shown in this section showed that localised areas of high temperature could be created in specific regions around the phaser shifters.

It is also important to notice how changes in materials' thermal properties play a



(a)



(b)

Figure 3.14: a) Accumulated phase-shift as a function of the power dissipated by the heat sources in both geometries. **b)** Power required to achieve a $\pi-$phase shift at $T_0 = 4\,\mathrm{K}$ and $T_0 = 300\,\mathrm{K}$ for both geometries

significant role in how phenomena such as thermal cross-talk or the appearance of thermal guides.

We showed that the modulator's design and location could play a relevant role in optimising its performance. For example, while a single heater created a more considerable change in phase for the same heater's length and the same power injected, a double heater deposited at the level of the silicon waveguide can provide a more localised region of high temperature, even when its maximum temperature is lower, it can be compensated by having longer double structures.

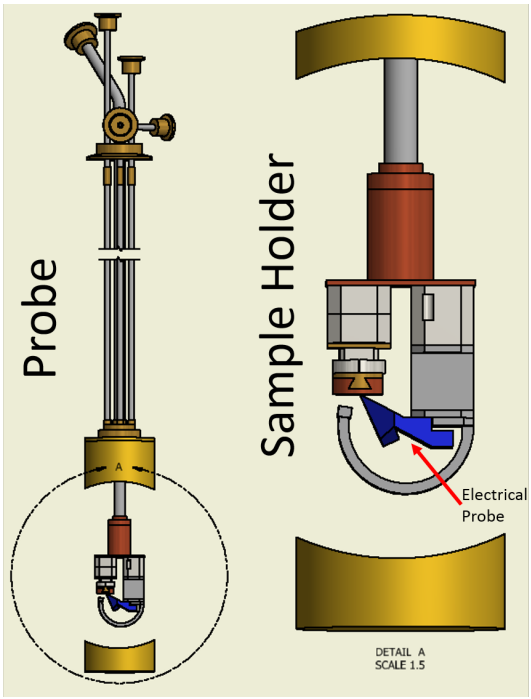
The results of the presented simulations also provide an insight into the behaviour of thermal cross-talk, both along the waveguide and perpendicular to its axis. It was shown that due to change in the thermal conductivity of silicon and silica at low temperatures.

Finally, numerical results showed that obtaining a $\pi-$phase shift in a cryogenic environment using thermal phase shifters is possible by dissipating powers in the order of tens of mW. This range of powers comply with the typical cooling power of cryogenic systems such as the introduced in Sec. 2.4

3.4 Thermal contraction of optical/electrical probe holder

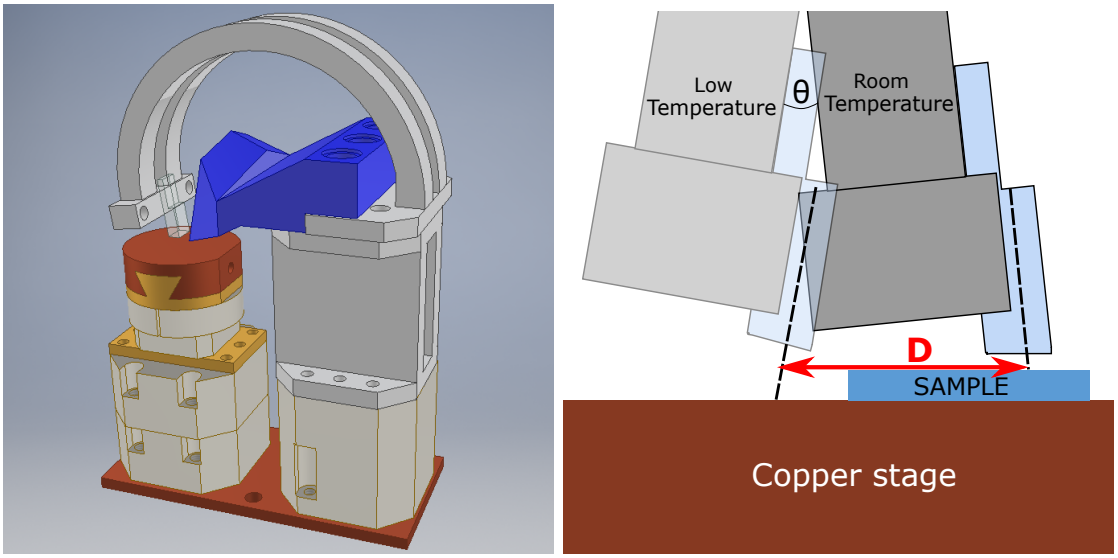
This section will present a simulation of the thermal contraction expected in the sample stage designed for the characterisation of integrated devices in a variable temperature insert (see Sec.2.4.1). The sample stage (shown in Fig. 3.15a) as modelled in Autodesk® Inventor® Professional 2017 and then imported into COMSOL Multiphysics.

Due to the conditions of low temperature and low pressure, the sample stage is subjected to, getting any visual feedback of the alignment of probes to the sample becomes a challenge. Since the sample stage is a complex structure composed of different materials, the dynamics result of the change of temperature are unknown and therefore of interest, particularly for the improvement of alignment protocols.



(a)

Figure 3.15: Variable temperature insert (VTI) and location of the sample stage for cryogenic characterization of photonic devices.



(a) (b)

Figure 3.16: **a)** Sample stage designed for characterization of integrated devices in a variable temperature cryostat. **b)** Displacement if the fibre array due to thermal contraction. Variables to be estimated include displacement vector and change in the angle of incidence.

The sample stage consists of two columns of components held together by a copper baseplate, which improves thermalisation with the 1K-pot. On top of one of the columns, the sample rests on a copper stage, attached to a brass adaptor which is connected to an Attocube® ANR101 rotator with a resolution of $\mu°$. The copper stage was designed to be thermally linked to the cryostat 1K-pot through a thermally conductive material such as a silver wire. Below the rotator, two linear close-loop horizontal stepper positioner Attocube® ANPx101. The second column holds both the electrical probe and the V-Grooved Assembly of optical fibres (VGA) (Fig. 2.15) separated at a fixed distance, with the VGA facing the surface of the opposed copper sample stage at an angle of 8° to the vertical.

3.4.1 Description of the geometry

Despite the complexity of the Attocube® nanopositioners, the model assumes all their volume consists of titanium since that element contributes most of their total weight.

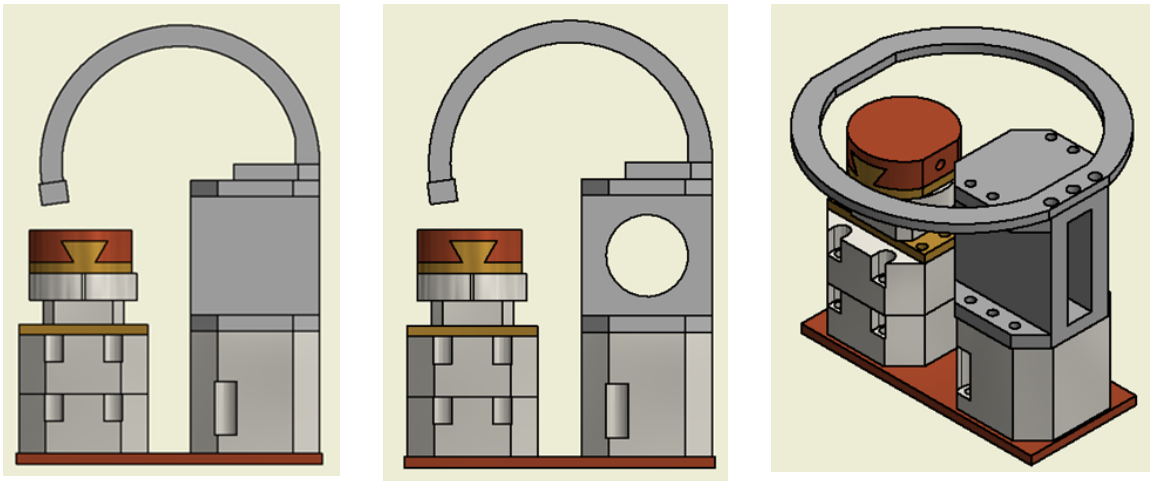


Figure 3.17: Three different variations of the arch that hold the fibre array.

COMSOL provides a material library with physical constants at normal conditions (room temperature and atmospheric pressure), which can be used if the temperature doesn't change drastically. But for studies at low temperature, the temperature dependency for every relevant parameter must be provided as input either as experimentally confirmed data or as a justified approximation . Figure 3.4d shows the thermal expansion coefficient for a temperature range from 0 to 300 K [61, 82].

In terms of the solid mechanics equations, since small deformations are expected, the motion equations (Eq. 3.3) were solved in order to obtain a stationary solution assuming the whole structure stays within the elastic regime:

$$\nabla \cdot S + F_v = 0 \tag{3.3}$$

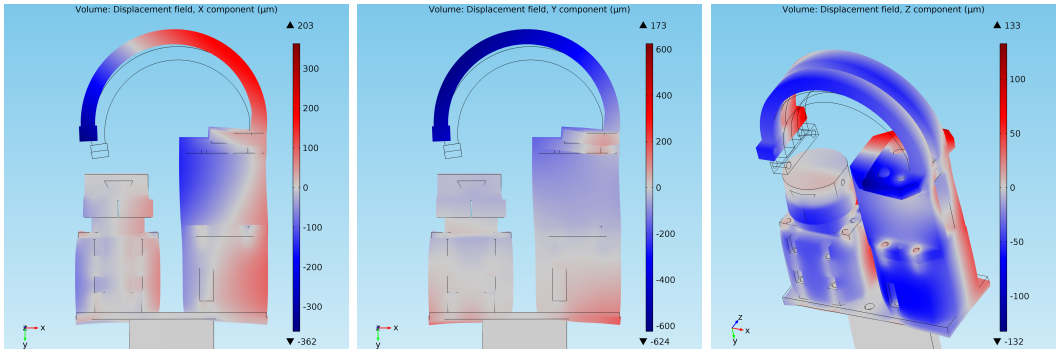
where S is the Cauchy stress and F_v is the volume force vector.

Three different variations for the design of the arch that holds the VGA was tested to identify any potential characteristic that might be beneficial to reduce either the relative displacement of the VGA or its change in orientation (see Fig. 3.17)

3.4.2 Boundary Conditions

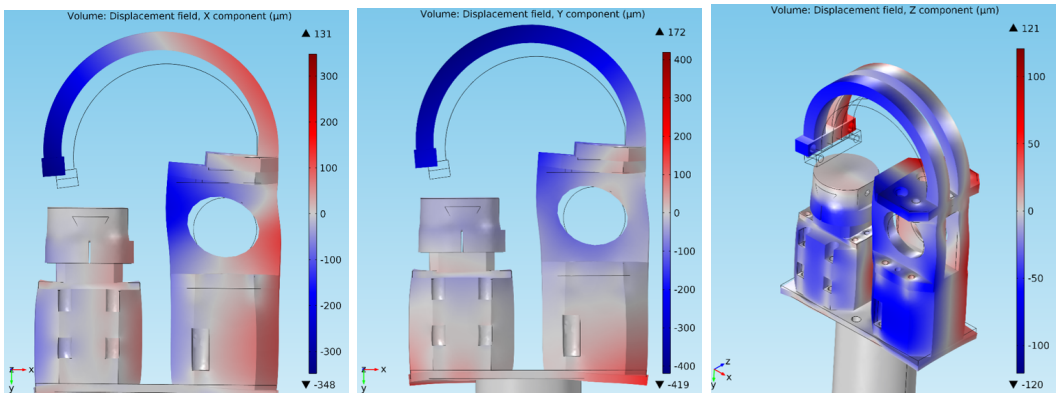
The lower face of the baseplate was defined as the reference point for all the deformation, so a fixed boundary was applied to it. All the junctions corresponding to where the different components are screwed to each other were defined as fixed connectors to restrict their relative displacement in any degree of freedom, either linear or angular.

No equation needed to be solved for the heat transfer solution since the only boundary condition for this module was a constant temperature value for the whole structure, then sent to the Solid Mechanics module to apply the correspondent deformation.



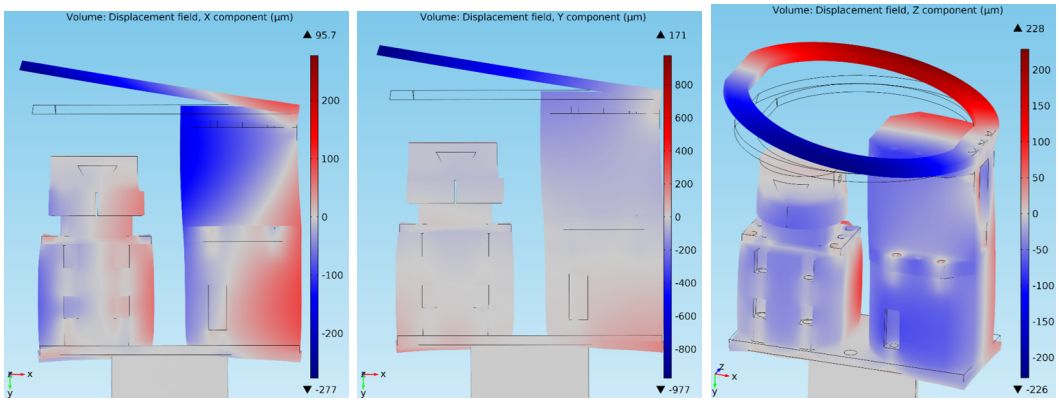
(a) Deflection in x. **(b)** Deformation in y. **(c)** Deformation in z.

Figure 3.18: Deformation components for Geometry #1 in x, y and z direction.



(a) Deflection in x. **(b)** Deflection in y. **(c)** Deflection in z.

Figure 3.19: Deformation components for Geometry #2 in x, y and z direction.



(a) Deformation in x. **(b)** Deformation in y. **(c)** Deformation in z.

Figure 3.20: Deformation components for Geometry #3 in x, y and z direction.

Parameter	Geometry #1	Geometry #2	Geometry #3
Δx (µm)	323	312	**242**
Δy (µm)	464	**258**	880
Δz (µm)	13	6	**2**
$\Delta\theta$ (°)	-0.57	**-0.33**	-0.9
D (µm)	-351	**-306**	-347

Table 3.2: Results of simulation of thermal expansion in COMSOL Multiphysics for all the different arch geometries simulated in this section. The result with the smaller deformation for each category is written in **bold**.

3.4.3 Results

The net deformations in x, y and z after running the study are shown in Fig. 3.18, 3.19 and 3.20. The relative deformation was split into three spatial components for the three geometries analysed. The deformation shown in this figure has an amplification factor of 10x so the reader can perceive the direction of the deformation.

Table 3.2 shows a summary of the relevant quantities obtained from the simulation. The parameters D, Δx, Δy and Δz represent the magnitude and every spatial component of the total relative displacement of the point the fibre array point is projecting on the sample stage. In contrast, $\Delta\theta$ is the change in the angle of the fibre array to the z-axis.

The significance of the results for the deformation of the stack of components should be discussed considering the model's limitations. Some of the variables not included in

the analysis were the complex internal structure of the nanopositioners and the thermal expansion of the thermally conducting varnish using the glue of the DUT on the sample stage.

As it was mentioned before, most of the nanopositioners mass is titanium. It is a fair assumption to model the whole structure as a solid titanium block as a first approximation. Nonetheless, deviations from the simplified model could be observed experimentally if internal components such as electrodes or membranes contribute to the total deformation, either by thermal expansion/contraction or due to a change in the way they interact with other internal components.

Nonetheless, this simulation aims not to predict with high accuracy the dynamic evolution of the structure during the contraction, nor to predict the resulting form of the system with microns of precision. The stack of nanopositioners is meant to be placed in a chamber with no means to establish visual contact with the sample through a window or a camera. The exact position and orientation of the fibre array holder are not as crucial as simply estimating the order of magnitude of the deformation range. This is relevant for two reasons: 1) when light is coupled vertically via optical fibre, the region around the optimal coupling location has a radius $\sim 10\,\mu m$, similar to the fibre core radius, and 2) the nanopositioners have a sub-micron resolution, but a limited travelling range of 5 mm. An estimation for the final deformation due to thermal contraction provides valuable data to program a routine to scan the sample and obtain optimal coupling, even after the initial coupling was lost after cooling the system.

Furthermore, since it is expected that the angle between the polished side of the fibre array and the surface of the sample to change with temperature, a simulation of thermal expansion is also helpful to properly design a fibre holder with optimal optical coupling at cryogenic temperatures.

Chapter 4

Thermal phase shifters in a cryogenic environment

In the previous chapter, numerical simulations showed that, although changes in thermal and optical properties in silicon at low temperatures affect the performance of thermal phase shifters, heaters could modulate the delay of single photons. A $\pi-$phase shift in an integrated interferometer was simulated dissipating powers within the ranges of tens of mW as observed at room temperature.

Commercial foundries typically turn to metallic or ceramic materials, such as aluminium [84], tungsten [85] or titanium [86], to fabricate heat dissipating structures. Alternatively, semiconductor materials such as silicon can dissipate heat via Joule heating if their carrier density is enhanced by doping them with a high dose of impurities.

This chapter will present an experimental work demonstrating the viability of thermal phaser shifters at cryogenic temperatures, mainly focused on their applications for QIP. Firstly, the DUT will be introduced, followed by the relevant connections and adjustments made to the cryogenic system to install the sample, to finally present and discuss the results of the electrical and optical characterisation of the DUT.

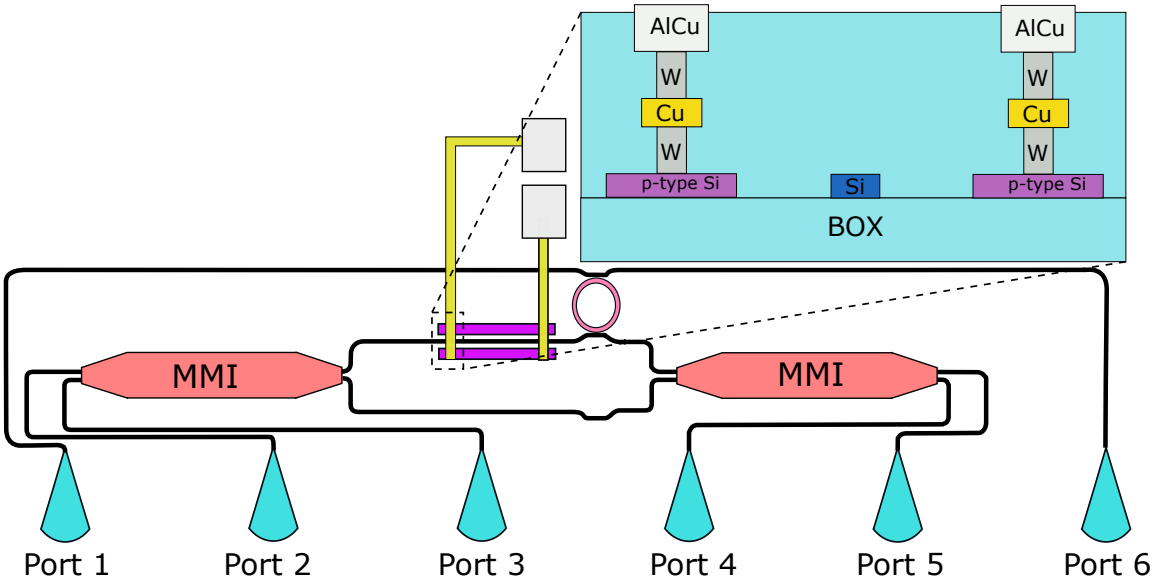


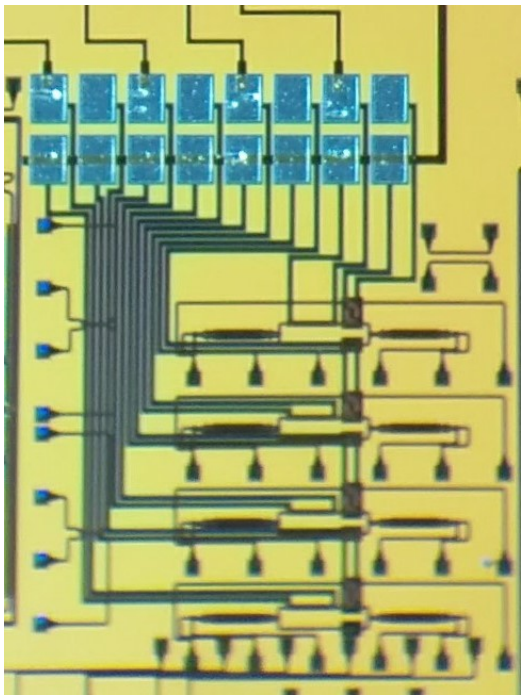
Figure 4.1: Integrated Mach-Zehnder interferometer used for the characterization of the highly doped silicon thermal phaser shifter. The set up has 6 I/O optical channels via grating couplers, two multi-mode interference structures and an additional waveguide connecting port 1 and 6 with a ring resonator, designed for a different experiment.

4.1 Mask design

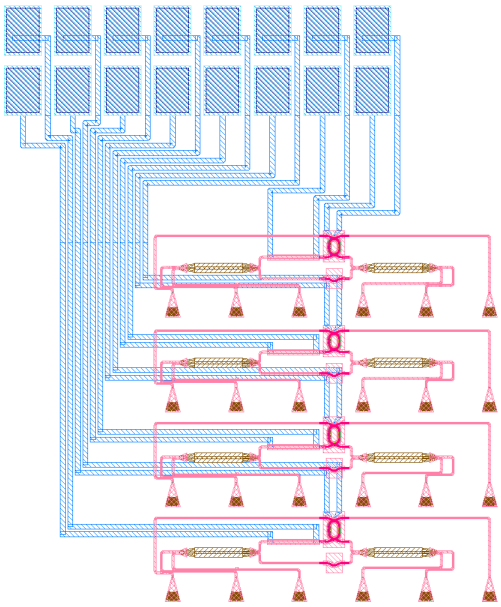
An optical interferometer is optimal for studying the change waveguides' refractive index. A Mach-Zehnder interferometer (MZI) was designed on an SOI device by Dr Damien Bonneau and fabricated by IMEC (Fig. 4.1). Light is coupled into the MZI vertically, via grating couplers optimised for a wavelength of 1550 nm at an angle of 8° and separation between ports of 127 µm. Multimode interference (MMI) structures were used for power splitting instead of directional couplers due to their tolerance to fabrication errors.

4.2 VTI electrical connections

AlCu pads were connected to a 40-pin FR-4 PCB (PCB-01 in Fig. 4.3), with a pitch of 100 µm using 25 µm-diameter gold wires. The PCB was screwed to the 1k-pot. The insert has 16 DC-lines made of twisted AWG 30 manganin wires, which are connected to the exterior via an 18-pin Fischer® connector. The connection between the PCB at the



(a)



(b)

Figure 4.2: Microscope image (a) and mask layout (b) of the integrated MZI used in the experiment.

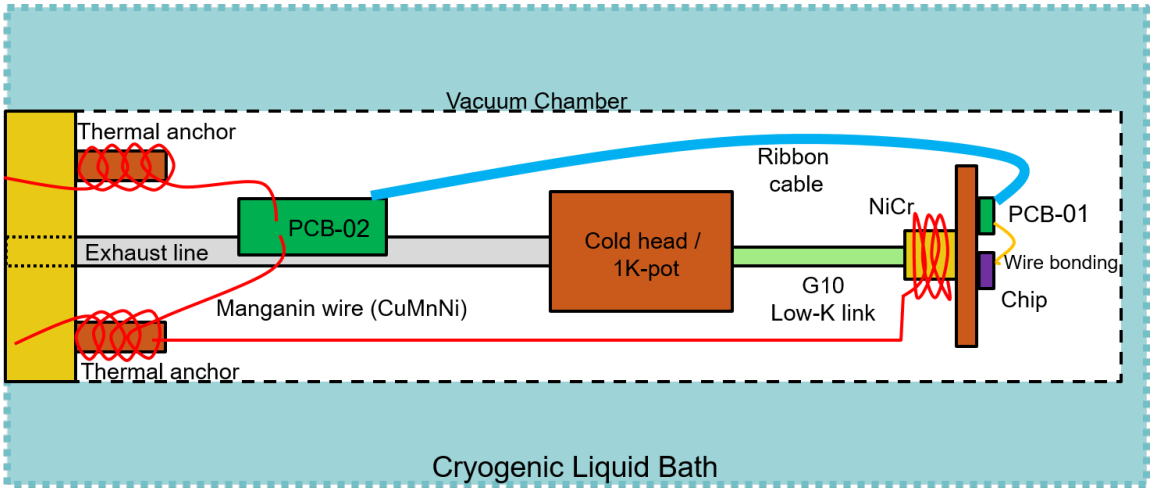


Figure 4.3: Diagram with connections and interfaces between the chip installed at 1K-pot and the manganin wires connected to the VTI's multi-DC port. A printed circuit board (PCB-01) with 40 fine-pitch contacts (100 µm) and a FFC connector serve as electrical interface with the wire bonding soldered to the AlCu contact pads. A second PCB (PCB-02) links the signal from PCB-01 with the manganin DC lines.

sample stage and the manganin wires was made at a second PCB attached to the exhaust line with four 10-pin female header connectors (Fig. 4.3).

All manganin wires were anchored to four different copper rods in contact with the shield to dissipate as much heat as possible from the exterior into the cryogenic bath.

4.3 Experimental data

4.3.1 Frequency response

Thermal modulators are not suitable for high-frequency operations. Thermal processes occur at relatively low speeds, which leads to long recovery times and low bandwidth. Furthermore, the wires that communicate the DUT with the external connections add additional parasitic capacitance that increases the loss dramatically at frequencies in the order of MHz.

In order to confirm the DUT's bandwidth, the S_{21} spectrum was measured between

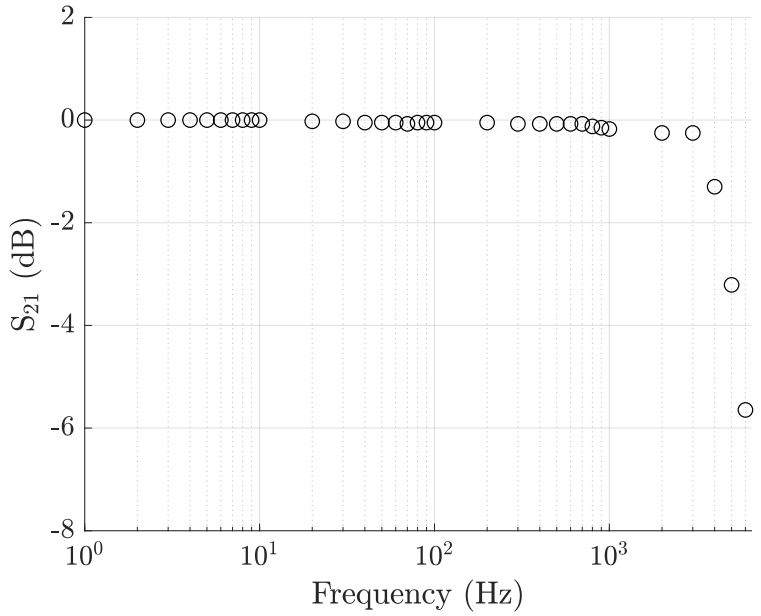


Figure 4.4: Frequency response of the VTI's electrical connections measured from the multi-DC connection through the 1.6 m

the VTI input ports and the sample's PCB (Fig. 4.4). The measured 3 dB bandwidth of ~ 5.3 kHz can be mainly attributed to the 1.6 m twisted manganin wires which serve as a poor transmission line.

Typical response times in thermo-optic phase shifters are usually within the range between 1 and a few hundred µs [87–92] which following a simple rule of thumb, translates into bandwidths between 2 kHz and 1 MHz.

But those bandwidths are ideal cases where the increase in BW is not due to wiring, so we can assume that the intrinsic BW is higher than 5kHz for the case of our device.

4.3.2 Resistance measurement and doping level estimation

The silicon heater's impurity density was estimated by measuring its resistivity and compared to reported data in the literature [93].

The average resistance of the silicon heaters at room temperature was measured to

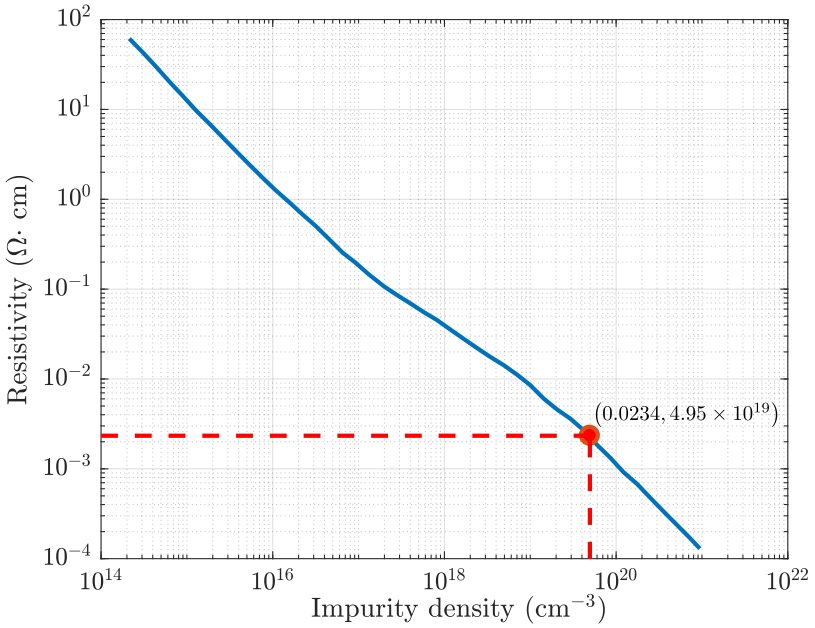


Figure 4.5: Resistivity of p-type silicon as a function of the impurity density at room temperature (line). The spot shows the experimental value for resistivity measured at the heater at room temperature. Interpolated data points from [93]

.

be 9.84 ± 0.01 kΩ using a 4-probe technique with a 6.4 digit multimeter. Based on the geometry of the silicon strip, the structures have an average sheet resistance of 106.41 ± 0.43 Ω/sq and resistivity of $2.34 \times 10^{-2}\,\Omega\,\text{cm}$. The relationship between doping level and resistivity for p-type silicon at room temperature has been reported in the literature [93] (Fig. 4.5), which shows that every silicon heater has an approximate doping level of $4.95 \times 10^{19}\,\text{cm}^{-3}$, which sets it above the limit of doping concentration for non-degenerate silicon.

The change in the heater's resistance at cryogenic temperatures was measured by cooling the VTI down to 77 K* and recording the signal from a temperature sensor attached to the sample stage (Fig. 4.7). The process was recorded on three different occasions, showing a behaviour opposed to what was expected from Fig. 4.5. There are two possible explanations for this:

*Material quality issues limited the performance of the VTI at lower temperatures due to the presence of porosities in the stainless steel tubes.

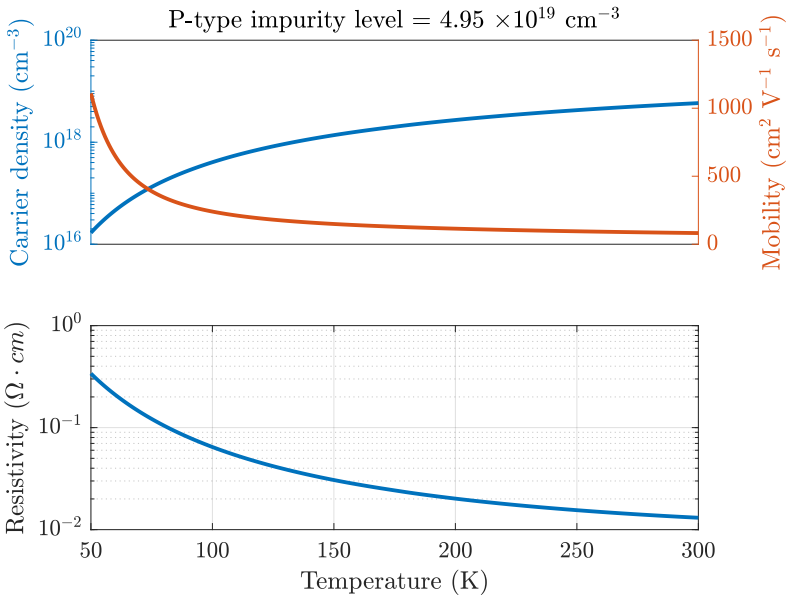


Figure 4.6: Numerical simulations in COMSOL of the carrier density, total hole mobility and resistivity for p-type silicon with a impurity level of $4.95 \times 10^{19}\,\mathrm{cm}^{-3}$, according to theory presented in Sec. 4.6, for the silicon strip heaters.

1. Temperature dependency contribution from the metal wires. Despite the experiment being wired for a 4-probe measurement, the metallic wires on the chip can not be isolated. Metals, unlike semiconductors, show an uninterrupted decrease with lowering the temperature due to a reduction in electronic scattering [94].

2. Self-heating mechanism that increases the temperature of the heater while its resistance is being measured, a temperature change out of the reach of the temperature sensor (see Fig. 4.8)

One of the reasons this could be explained is that the current injected into the heater was not controlled. Therefore, there is no way of knowing if any kind of self-healing process is creating localised areas of high temperature in the areas surrounding the heater.

The silicon heater's resistance was measured first using a 4-probe technique with two single DC probes and two channels from a 12-channel multi-DC probe for a range of input powers (from 0 to 160 mW) in order to observe the effect of self-heating at different temperatures above 10 K. The trending shown in Fig. 4.8 for all different temperatures is

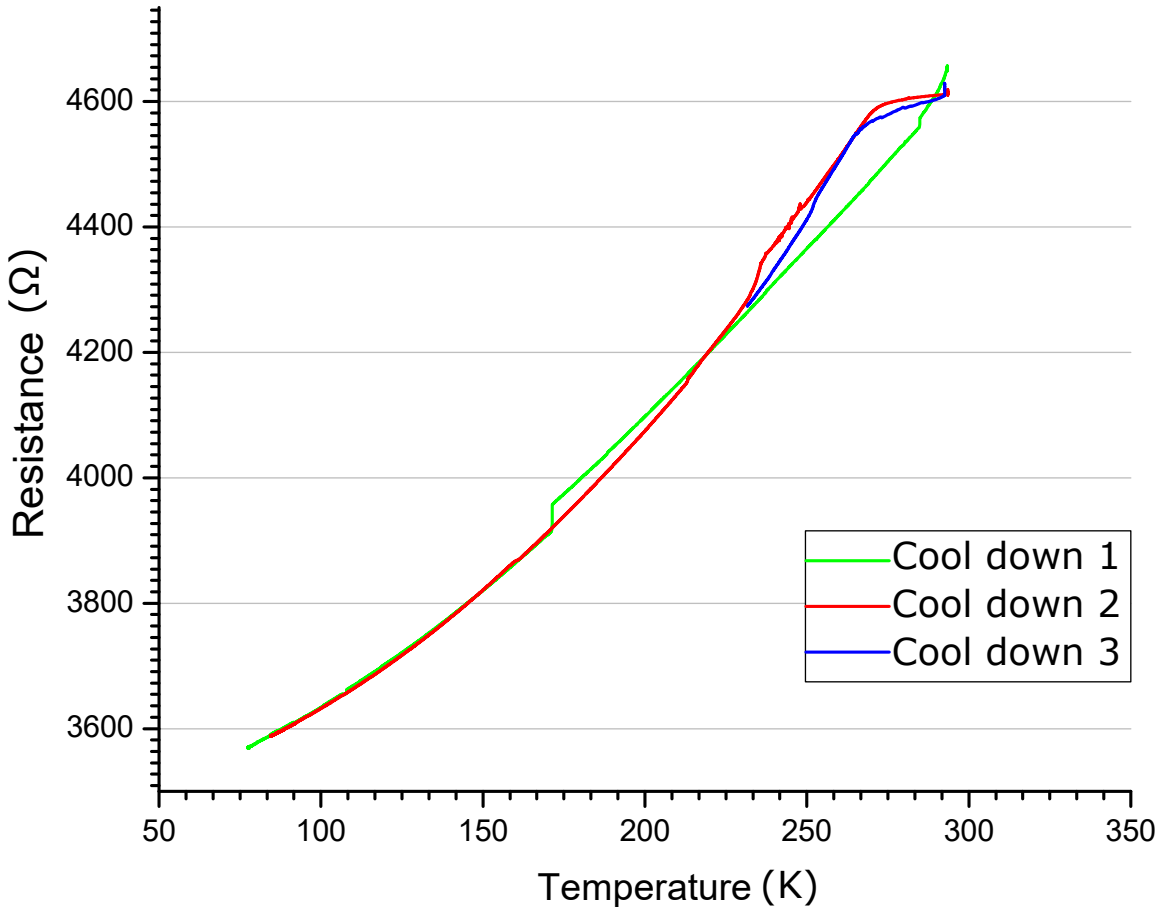


Figure 4.7: Resistance measured at the heater with respect to the temperature measured at the VTI'S 1K-pot.

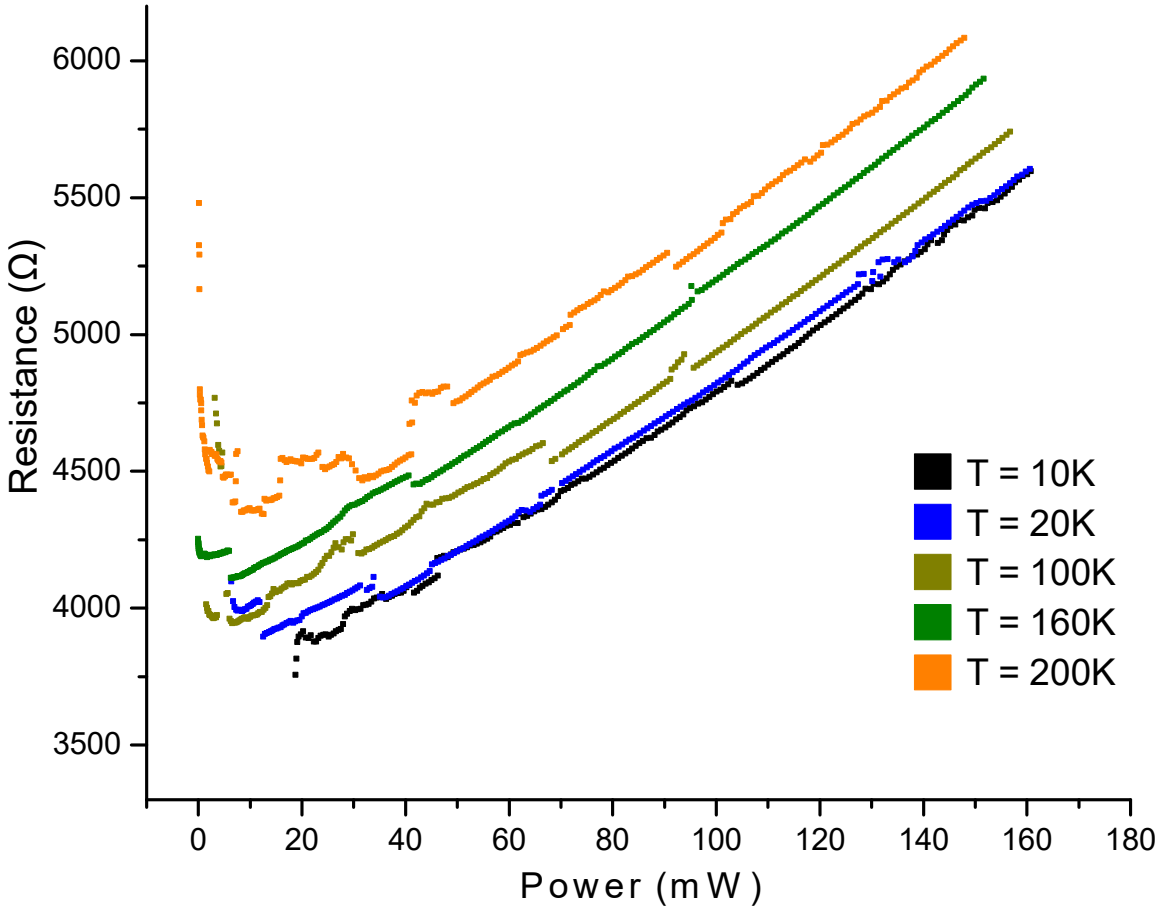


Figure 4.8: Silicon heater's resistance measured by 4-probe technique in the cryogenic probe station for a range of input powers from 0 to 160 mW.

evidence of a self-healing process by Joule heating.

With temperatures as low as 10 K, carriers freeze-out did not stop carriers from acting as ohmic dissipators, probably due to the high level of impurity decreasing the threshold at which freeze-out occurs, leaving some carriers that did not recombine, triggering a process that leads to an increase in temperature in a localised area of the silicon strip.

4.3.3 Optical characterization

The optical characterisation of the MZI was attempted in both experimental set-ups finally performed in the Lake Shore® cryogenic probe station for better reliability.

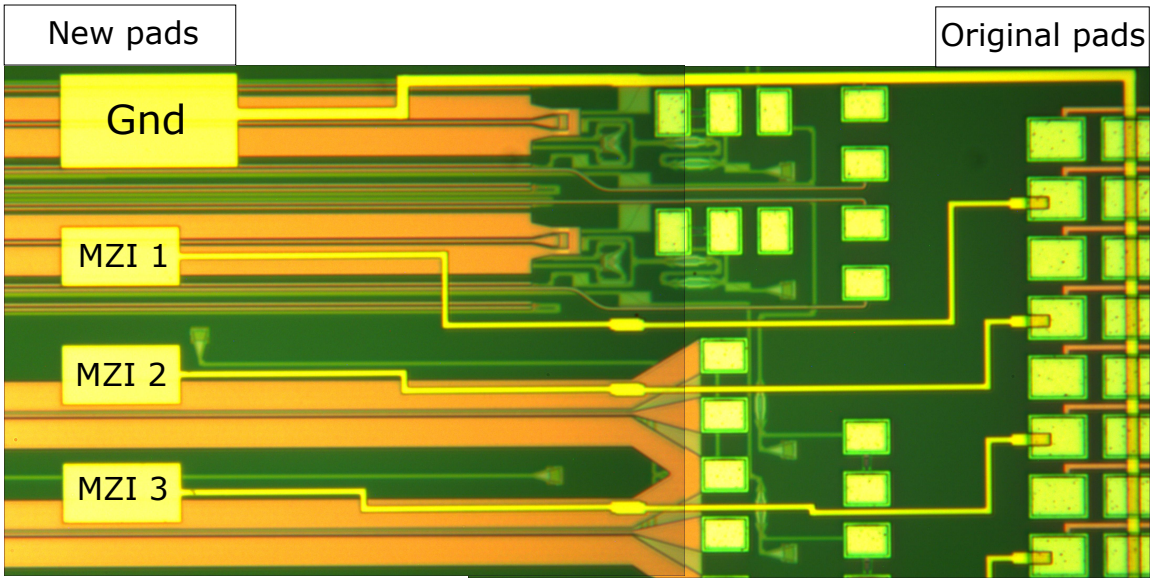


Figure 4.9: Extended contact pads added in in-house post-process lithography by Dr. Pisu Jiang to allow the electrical probes and fibre array get to their probing/coupling position.

In order to bring the electrical probes and the fibre array close enough to make contact with the pads and couple light into the grating couplers, some post-process lithography had to be done on the pads. The contact pads had to be extended further away from the grating couplers in order to allow the 2 mm-thick fibre array's Pyrex lid and silicon substrate to fit in the area above the experiment and the electrical probes to have access to the contact pads.

The camera that provides an image from the top of the sample stage is the only visual feedback one can use to align the fibre array to the grating couplers on the sample. Nonetheless, the view of the position of the individual fibres on top of the sample is limited. This is why right-angle prism mirrors were used to have a lateral view of the alignment process.

In order to align the optical inputs, a 1550 nm CW-laser was used in ports 1, and 6 with a Thorlabs' power meter PM100D and fibre photodiode power sensor S154 is connected to channel six.

The following protocol was designed to speed up and optimise optical and electrical

alignment:

1. Move away from the fibre array from the region of the sample where the grating couplers are to give visibility to the camera and maintain it 2 to 3 mm above the sample.

2. Use the camera's software to mark the spots where the grating couplers from Port 1 and Port 6 are located.

3. Use the lateral mirrors to observe the position of the fibres and begin to move the VGA holder along the axis of the probe station arm with direction towards its coupling position.

4. Use the camera software to estimate the position of the fibres with respect to the edge of the chip (use dimensions from the mask and a reference in the camera, e.g. the VGA's thickness).

5. Scan in the transversal direction with respect to the axis of the probe station arm until a reading is observed in the power meter.

6. Once the VGA is in position with some level of coupling. It is ok to lower the VGA gradually, adjusting its position over the horizontal plane based on the reading in the power meter, trying to maximise it.

7. Once the VGA is in position with optimal coupling; the single DC probe can be positioned on the contact pads. When there are in position, they should be lowered slowly, keeping the camera focused on the surface of the chip. When the probe makes contact with the surface of the sample, small tip deformation will be observed.

8. The CW laser should now change from VGA's channel 1 to channel 2 to have the input light being coupled into one of the arms of the MZI, which is connected to Port 2 (Fig. 4.1). The fibre IR sensor should be connected to either Port 3 or 4.

A set of measurements for a range of powers dissipated by the heater is shown in Fig. 4.10a. The temperature change is reflected on the effective refractive index of the whole circuit, resulting in coupling changes in the structure and effective path-length changes.

The test was repeated for different temperatures, always keeping the VGA and the DC probes away from the surface of the chip while the temperature of the sample stage is changing to avoid damaging any of the components.

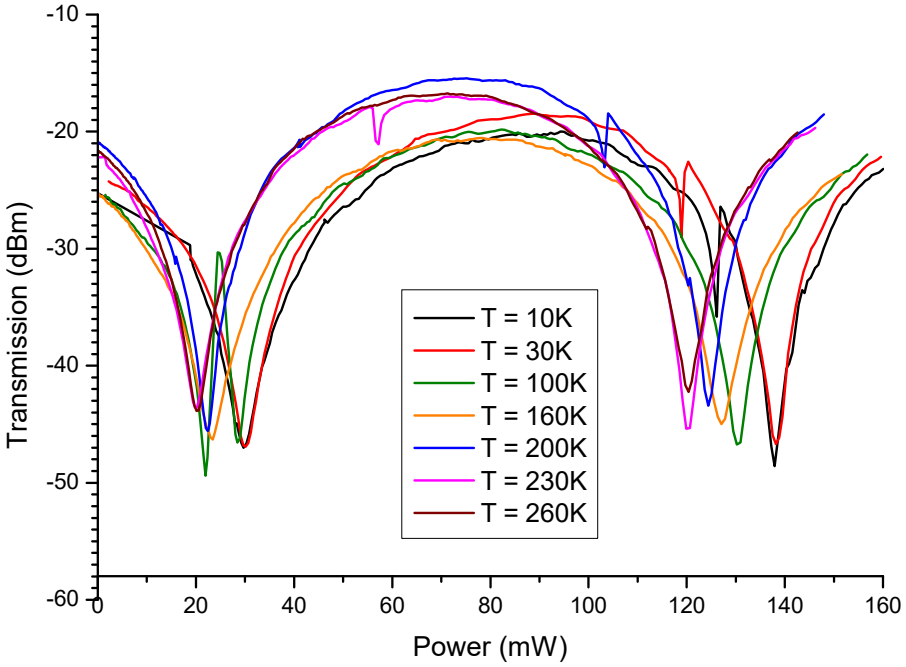
The power required[†] for a π-phase shift was measured from valley to valley in Fig. 4.10a. Those values are presented in Fig. 4.10. One of the characteristics of from Fig. 4.10 is its similarities with Fig. 3.11b: both show a slightly negative correlation between P_π and temperature. In other words, it supports the claim that not much more power is required at cryogenic temperatures to obtain a π-phase shift.

4.4 Discussion

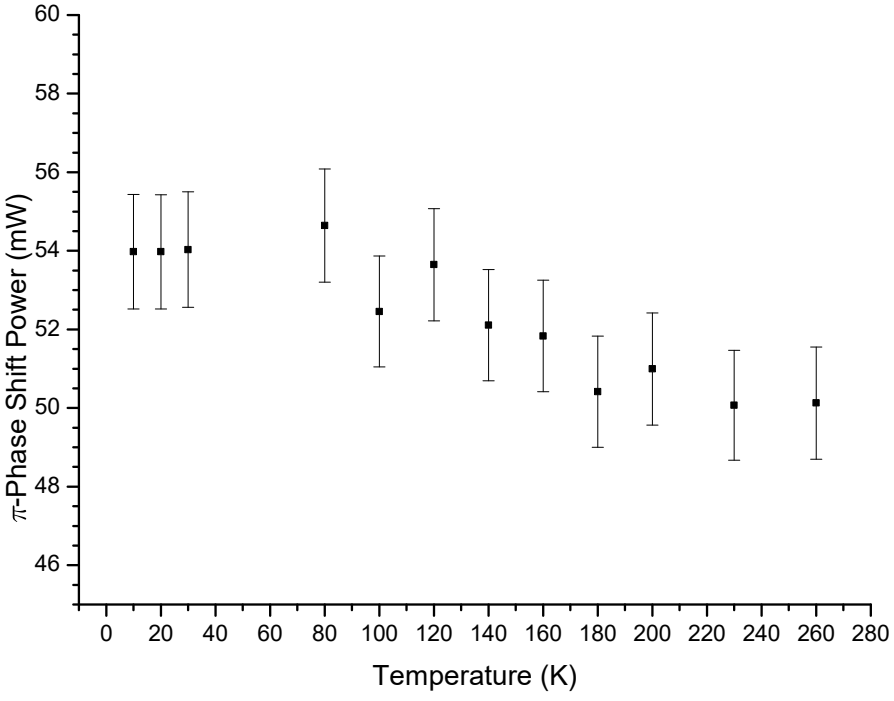
Comparing the results for the power required to achieved a π-phase shift, both theoretical (Fig. 3.11b) and experimental (Fig. 4.10b), it can be noted that they coincide in the order of magnitude. While the numerical estimation for P_π^{300K} is around half the value of P_π^{4K}, the experimental result shows a variation of only 7% between both temperatures.

The uncertainty in the input data is used to characterise the temperature dependency of the material's thermal properties. On the other side, the effect of metallic pads and internal interconnection layers within the chip was considered negligible compared to the contribution of the cladding and substrate in the thermal dissipation process. The electrical probe is thermally anchored to the sample stage, isolated from the high temperature components by a section of G10. This low thermally conductive material limits the thermal load in the sample stage. Nonetheless, the probe arm does not reach a full base temperature when making contact. Even though the temperature difference between probe and sample is not more than 1 K, that connection makes the chip's surface no longer an insulated

[†]The power is calculated from the measured values of injected current and the resistance measured previously



(a)



(b)

Figure 4.10: a) Transmission scan on an integrated MZI between port 1 and port 4 (Fig.s 4.1) as a function of the power dissipated by the thermal phase shifter for different base temperatures ranging from 10 K to 260 K **b)** Dissipated power required to obtain a π-phase shift in the MZI interference pattern.

boundary, which differs from the boundary conditions defined in the numerical model.

The fact that slightly more energy was expected to be dissipated according to the simulations to accomplish a π-phase shift might be associated with one or more assumptions made in the numerical model that are not present in the experimental set-up. For example, the constant temperature boundary condition defined at the bottom face of the geometry implied a non-limited heat flow between the sample and a surface at base temperature $T0$. Nonetheless, the chip and cold head are not in direct thermal contact, but they are linked through a cryogenic vanish. It must be pointed out that the varnish has a high thermal conductivity at low temperatures. Still, since the offset between experimental and numerical data points is not larger than an order of magnitude, the decrease in the effective thermal transmission between the chip and cold head could explain a rise in the resulting stationary temperature for a particular injected power.

It could be expected that at temperatures close to absolute zero, the main contribution to the specific heat would come from vibrations from the lattice and instead of electronic contribution. As the temperature increases and more impurities are ionised, increasing the carrier density in the silicon strip, the heat capacity increases more rapidly than in the case of the intrinsic silicon waveguide, requiring more heat to achieve the same change in temperature. Nonetheless, the opposite is observed since the experimental data refers to a highly doped structure; its specific heat should be higher than the simulated structure, leading to a higher value of absorbed heat between both temperatures.

On the other side, geometry 2 was used for the experimental measurements mainly because of the availability of such kinds of structures in our group's collection of devices. Geometry #1 discussed in chapter 3, is the most common design for thermo-optic modulators. Still, they do not provide any extra perks in terms of fabrication turnaround time, cost or significant improvement in performance.

Finally, it has been shown that thermal phase shifters can be used on photonic circuits at cryogenic temperatures. This is despite the massive decrease in the semiconductors' thermo-optic coefficient and thanks to their decreasing heat capacity. The phenomena

observed are relevant to silicon by can be easily generalised to other material platforms.

Concerning the drop in silicon's thermo-optic coefficient [51], a simple way to understand the reason why phase shifters can operate at low temperature could be explained by the following expression:

$$\frac{\Delta n}{\Delta Q} = \frac{\partial n}{\partial T}\frac{\partial T}{\partial Q} = \frac{\partial n}{\partial T}\left(\frac{1}{C_p}\right) \tag{4.1}$$

where n is silicon's refractive index, T is the temperature and Q is the power absorbed by the material. In simple terms, even when the thermo-optic coefficient $\frac{dn}{dT}$ decreases four orders of magnitude when it goes from room temperature to near 5 K, the specific heat also decreases, which makes it easier for the material to increase its temperature with less energy, and since thermal conductivity also drops for all materials, this increase in temperature tends to be localized.

Chapter 5

Conclusions and outlook

The importance of thermal analysis in silicon integrated photonics and microelectronics is an issue of concern for commercial semiconductor foundries. The increasing number of components in silicon-based microprocessors demands better ways to deal with overheating, challenging to engineer new ways of dissipating heat. Cryogenic applications in silicon photonics have expanded the range of temperatures at which solutions for a thermally efficient performance must be provided.

As long as superconducting technologies such as SNSPDs keep an advantage over other single-photon detection alternatives, cryogenic temperatures will still be required. Therefore, changes in material properties at low temperatures should be considered an additional step in the design process of an integrated device, particularly for those aiming to pave the way towards universal optical quantum computing.

It is no surprise that alternative paths to modulate PIC's optical path length have been developed in the past few years due to the need of having structures to operate on single qubits spatially encoded on integrated waveguides and the observation that silicon's and silica's thermo-optic coefficient tends to vanish at temperatures near absolute zero [51].

Single qubit quantum gates are required to operate a fully integrated quantum processor. Their fundamental components, such as single-photon sources, filters, microring

resonators and optical switches, just to mention a few, will require to be tested and characterized at low temperatures.

Here has been shown through multiphysics simulations that it is possible to use thermal phase shifters to create localized areas of high temperature in well-delimited regions of a waveguide by injecting an amount of power that is compatible with the cooling capacities of cryogenic systems that operate above 1 K. On the other side, the increase in the ratio between thermal conductivities of silicon and silica leads to silicon waveguides behaving as heat channels, concentrating heat more efficiently.

Additionally, thermo-mechanical simulations have been used as a tool for modelling the alignment of optical and electrical components in an environment with difficult access to cameras such as cryostat.s

Geometries such as the standard heaters simulated, tested and discussed previously are far from being an optimal design in terms of how power efficiency or thermal cross-talk they cause. That is an ongoing line of research that is not necessarily concerned about devices' performance at low temperatures but will undoubtedly contribute to the final objective.

Just as the heaters' geometries could be optimized and offer better performance, the structure of the silica layers surrounding the region of interest could also be modified considering how the thermal properties of silicon and silica change at low temperatures. That is, creating regions where heat could have a preferential direction for its propagation, e.g. adding trenches over the silicon oxide cladding around the phase shifters, directing heat dissipation through the silicon substrate.

The relatively small change in power consumed by a thermal phase shifter at low temperatures suggests that bigger and more powerful cryostats are required to host the complex photonic circuits required in quantum information processing.

Nevertheless, there are still open questions such as the dynamic response of these elements at low temperatures. It is still unclear whether metallic or semiconductor-based heating elements will be better at low temperatures, but we believe mobility will play a

key role.

Finally, using the concepts and techniques developed here, it will be possible to engineer the thermal management of photonic circuits at low temperatures to reduce power consumption and thermal cross-talk providing a route to scalability and compatibility with superconducting single-photon detectors.

Bibliography

[1] A. Chen, "Beyond-CMOS Technology Roadmap." `http://www.itrs2.net/itrs-reports.html`, May 2015. International Technology Roadmap for Semiconductors.

[2] T. D. Ladd, F. Jelezko, R. Laflamme, Y. Nakamura, C. Monroe, and J. L. O'Brien, "Quantum computers.," *Nature*, vol. 464, pp. 45–53, mar 2010.

[3] IBM Research, "Which way to a fault-tolerant universal quantum computer?." https://www.research.ibm.com/ibm-q/learn/what-is-quantum-computing/.

[4] B. Heim, T. F. Rønnow, S. V. Isakov, and M. Troyer, "Quantum versus classical annealing of ising spin glasses," *Science*, vol. 348, no. 6231, pp. 215–217, 2015.

[5] D. P. DiVincenzo, "The physical implementation of quantum computation," in *Fortschr. Phys*, Citeseer, 2000.

[6] J. You and F. Nori, "Quantum information processing with superconducting qubits in a microwave field," *Physical Review B*, vol. 68, no. 6, p. 064509, 2003.

[7] J. M. Nichol, L. A. Orona, S. P. Harvey, S. Fallahi, G. C. Gardner, M. J. Manfra, and A. Yacoby, "High-fidelity entangling gate for double-quantum-dot spin qubits," *arXiv preprint arXiv:1608.04258*, 2016.

[8] J. T. Muhonen, J. P. Dehollain, A. Laucht, F. E. Hudson, R. Kalra, T. Sekiguchi, K. M. Itoh, D. N. Jamieson, J. C. McCallum, A. S. Dzurak, *et al.*, "Storing quantum

information for 30 seconds in a nanoelectronic device," *Nature Nanotechnology*, vol. 9, no. 12, pp. 986–991, 2014.

[9] S. Debnath, N. Linke, C. Figgatt, K. Landsman, K. Wright, and C. Monroe, "Demonstration of a small programmable quantum computer with atomic qubits," *Nature*, vol. 536, no. 7614, pp. 63–66, 2016.

[10] M. Schmidt, M. Ludwig, and F. Marquardt, "Optomechanical circuits for nanomechanical continuous variable quantum state processing," *New Journal of Physics*, vol. 14, no. 12, p. 125005, 2012.

[11] F. Jelezko, T. Gaebel, I. Popa, M. Domhan, A. Gruber, and J. Wrachtrup, "Observation of coherent oscillation of a single nuclear spin and realization of a two-qubit conditional quantum gate," *Physical Review Letters*, vol. 93, no. 13, p. 130501, 2004.

[12] J. L. O'Brien, A. Furusawa, and J. Vučković, "Photonic quantum technologies," *Nat. Photonics*, vol. 3, pp. 687–695, dec 2009.

[13] J. L. O'Brien, "Optical quantum computing.," *Science*, vol. 318, pp. 1567–70, dec 2007.

[14] E. Knill, R. Laflamme, and G. J. Milburn, "A scheme for efficient quantum computation with linear optics.," *Nature*, vol. 409, no. 6816, pp. 46–52, 2001.

[15] A. Politi, M. J. Cryan, J. G. Rarity, S. Yu, and J. L. O'brien, "Silica-on-silicon waveguide quantum circuits," *Science*, vol. 320, no. 5876, pp. 646–649, 2008.

[16] P. Sibson, C. Erven, M. Godfrey, S. Miki, T. Yamashita, M. Fujiwara, M. Sasaki, H. Terai, M. G. Tanner, C. M. Natarajan, *et al.*, "Chip-based quantum key distribution," *Nature Communications*, vol. 8, p. 13984, 2017.

[17] G. Reithmaier, M. Kaniber, F. Flassig, S. Lichtmannecker, K. Müller, A. Andrejew, J. Vuckovic, R. Gross, and J. Finley, "On-chip generation, routing, and detection of resonance fluorescence," *Nano letters*, vol. 15, no. 8, pp. 5208–5213, 2015.

[18] J. Carolan, C. Harrold, C. Sparrow, E. Martín-López, N. J. Russell, J. W. Silverstone, P. J. Shadbolt, N. Matsuda, M. Oguma, M. Itoh, *et al.*, "Universal linear optics," *Science*, vol. 349, no. 6249, pp. 711–716, 2015.

[19] C. Xiong, X. Zhang, A. Mahendra, J. He, D.-Y. Choi, C. Chae, D. Marpaung, A. Leinse, R. Heideman, M. Hoekman, *et al.*, "Compact and reconfigurable silicon nitride time-bin entanglement circuit," *Optica*, vol. 2, no. 8, pp. 724–727, 2015.

[20] M. Bazzan and C. Sada, "Optical waveguides in lithium niobate: Recent developments and applications," *Applied Physics Reviews*, vol. 2, no. 4, p. 040603, 2015.

[21] A. Politi, J. C. Matthews, M. G. Thompson, and J. L. O'Brien, "Integrated quantum photonics," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 15, no. 6, pp. 1673–1684, 2009.

[22] E. Ghafar-Zadeh, "Emerging CMOS bio-sensors: A paradigm shift," *Biosens J*, vol. 4, p. 115, 2015.

[23] G. P. Agrawal, "Optical amplifiers," *Fiber-Optic Communication Systems*, pp. 226–278, 2002.

[24] J. Leuthold, C. Koos, and W. Freude, "Nonlinear silicon photonics," *Nat. Publ. Gr.*, vol. 4, 2010.

[25] E. Dulkeith, Y. A. Vlasov, X. Chen, N. C. Panoiu, and R. M. Osgood, "Self-phase-modulation in submicron silicon-on-insulator photonic wires," *Optics Express*, vol. 14, no. 12, pp. 5524–5534, 2006.

[26] R. Dekker, A. Driessen, T. Wahlbrink, C. Moormann, J. Niehusmann, and M. Först, "Ultrafast Kerr-induced all-optical wavelength conversion in silicon waveguides using 1.55 μm femtosecond pulses," *Optics express*, vol. 14, no. 18, pp. 8336–8346, 2006.

[27] E. Timurdogan, C. V. Poulton, and M. R. Watts, "Electric Field-Induced Second Order Nonlinear Optical Effects in Silicon Waveguides," *arXiv preprint arXiv:1603.04515*, mar 2016.

[28] E. Engin, D. Bonneau, and C. Natarajan, "Photon pair generation in a silicon micro-ring resonator with reverse bias enhancement," *Opt. Express*, vol. 21, no. 23, pp. 2201007–2201014, 2013.

[29] L. Chrostowski and M. Hochberg, *Silicon photonics design: from devices to systems*. Cambridge University Press, 2015.

[30] M. Thompson, A. Politi, J. Matthews, and J. O'Brien, "Integrated waveguide circuits for optical quantum computing," *IET Circuits, Devices Syst.*, vol. 5, no. 2, p. 94, 2011.

[31] R. Hadfield, "Single-photon detectors for optical quantum information applications," *Nat. Photonics*, vol. 3, no. 12, pp. 696–705, 2009.

[32] M. D. Eisaman, J. Fan, A. Migdall, and S. V. Polyakov, "Invited review article: Single-photon sources and detectors.," *Rev. Sci. Instrum.*, vol. 82, p. 071101, jul 2011.

[33] R. H. Haitz, "Mechanisms contributing to the noise pulse rate of avalanche diodes," *Journal of Applied Physics*, vol. 36, no. 10, pp. 3123–3131, 1965.

[34] B. Korzh, N. Walenta, T. Lunghi, N. Gisin, and H. Zbinden, "Free-running InGaAs single photon detector with 1 dark count per second at 10% efficiency," *Appl. Phys. Lett.*, vol. 104, no. 8, 2014.

[35] A. Tosi, A. D. Mora, F. Zappa, and S. Cova, "Single-photon avalanche diodes for the near-infrared range: detector and circuit issues," *Journal of Modern Optics*, vol. 56, no. 2-3, pp. 299–308, 2009.

[36] Y. Liang, E. Wu, X. Chen, M. Ren, Y. Jian, G. Wu, and H. Zeng, "Low-timing-jitter single-photon detection using 1-ghz sinusoidally gated ingaas/inp avalanche photodiode," *IEEE Photonics Technology Letters*, vol. 23, no. 13, p. 887, 2011.

[37] A. Tosi, N. Calandri, M. Sanzaro, and F. Acerbi, "Low-noise, low-jitter, high detection efficiency InGaAs/InP single-photon avalanche diode," *IEEE J. Sel. Top. Quantum Electron.*, vol. 20, pp. 192–197, nov 2014.

[38] L. C. Comandar, B. Fröhlich, J. F. Dynes, A. W. Sharpe, M. Lucamarini, Z. Yuan, R. V. Penty, and A. J. Shields, "Gigahertz-gated ingaas/inp single-photon detector with detection efficiency exceeding 55% at 1550 nm," *Journal of Applied Physics*, vol. 117, no. 8, p. 083109, 2015.

[39] J. Zhang, M. A. Itzler, H. Zbinden, and J.-W. Pan, "Advances in ingaas/inp single-photon detector systems for quantum communication," *Light: Science & Applications*, vol. 4, no. 5, p. e286, 2015.

[40] B. Goll, M. Hofbauer, B. Steindl, and H. Zimmermann, "A fully integrated spad-based cmos data-receiver with a sensitivity of- 64 dbm at 20 mb/s," *IEEE Solid-State Circuits Letters*, vol. 1, no. 1, pp. 2–5, 2018.

[41] C. Yu, M. Shangguan, H. Xia, J. Zhang, X. Dou, and J.-W. Pan, "Fully integrated free-running ingaas/inp single-photon detector for accurate lidar applications," *Optics Express*, vol. 25, no. 13, pp. 14611–14620, 2017.

[42] B. Cabrera, R. Clarke, P. Colling, A. Miller, S. Nam, and R. Romani, "Detection of single infrared, optical, and ultraviolet photons using superconducting transition edge sensors," *Applied Physics Letters*, vol. 73, no. 6, pp. 735–737, 1998.

[43] A. J. Miller, S. W. Nam, J. M. Martinis, and A. V. Sergienko, "Demonstration of a low-noise near-infrared photon counter with multiphoton discrimination," *Applied Physics Letters*, vol. 83, no. 4, pp. 791–793, 2003.

[44] A. E. Lita, A. J. Miller, and S. W. Nam, "Counting near-infrared single-photons with 95% efficiency," *Optics express*, vol. 16, no. 5, pp. 3032–3040, 2008.

[45] G. N. Gol'tsman, O. Okunev, G. Chulkova, a. Lipatov, a. Semenov, K. Smirnov, B. Voronov, a. Dzardanov, C. Williams, and R. Sobolewski, "Picosecond

superconducting single-photon optical detector," *Appl. Phys. Lett.*, vol. 79, no. 6, p. 705, 2001.

[46] M. K. Akhlaghi, E. Schelew, and J. F. Young, "Waveguide integrated superconducting single-photon detectors implemented as near-perfect absorbers of coherent radiation," *Nature communications*, vol. 6, 2015.

[47] N. A. Tyler, J. Barreto, G. E. Villarreal-Garcia, D. Bonneau, D. Sahin, J. L. O'Brien, and M. G. Thompson, "Modelling superconducting nanowire single photon detectors in a waveguide cavity," *Opt. Express*, vol. 24, pp. 8797–8808, Apr 2016.

[48] D. Sahin, A. Gaggero, Z. Zhou, S. Jahanmirinejad, F. Mattioli, R. Leoni, J. Beetz, M. Lermer, M. Kamp, S. Höfling, and A. Fiore, "Waveguide photon-number-resolving detectors for quantum photonic integrated circuits," *Appl. Phys. Lett.*, vol. 103, no. 11, p. 111116, 2013.

[49] W. H. P. Pernice, C. Schuck, O. Minaeva, M. Li, G. N. Goltsman, A. V. Sergienko, and H. X. Tang, "High-speed and high-efficiency travelling wave single-photon detectors embedded in nanophotonic circuits.," *Nat. Commun.*, vol. 3, p. 1325, jan 2012.

[50] C. Kittel, *Introduction to solid state physics*. Wiley, 2005.

[51] J. Komma, C. Schwarz, G. Hofmann, D. Heinert, and R. Nawrodt, "Thermo-optic coefficient of silicon at 1550 nm and cryogenic temperatures," *Applied Physics Letters*, vol. 101, no. 4, p. 041905, 2012.

[52] D. Liang and J. E. Bowers, "Recent progress in lasers on silicon," *Nat. Publ. Gr.*, vol. 4, 2010.

[53] D. Bonneau, J. W. Silverstone, and M. G. Thompson, "Silicon quantum photonics," *Top. Appl. Phys.*, vol. 122, no. 6, pp. 41–82, 2016.

[54] R. Soref, "The Past, Present, and Future of Silicon Photonics," *IEEE J. Sel. Top. Quantum Electron.*, vol. 12, no. 6, pp. 1678–1687, 2006.

[55] "imec-ePIXfab SiPhotonics: iSiPP50G." http://www.europractice-ic.com/SiPhotonics_technology_imec_ISIPP50G.php, Aug. 2017.

[56] O. Kononchuk and B.-Y. Nguyen, *Silicon-on-insulator (SOI) technology: Manufacture and applications*. Elsevier, 2014.

[57] F. G. Della Corte, M. Esposito Montefusco, L. Moretti, I. Rendina, and G. Cocorullo, "Temperature dependence analysis of the thermo-optic effect in silicon by single and double oscillator models," *Journal of Applied Physics*, vol. 88, no. 12, pp. 7115–7119, 2000.

[58] R. Soref and B. Bennett, "Electro-optical effects in silicon," *Quantum Electron. IEEE J.*, no. 1, pp. 123–129, 1987.

[59] H. Xu, X. Li, X. Xiao, P. Zhou, Z. Li, J. Yu, and Y. Yu, "High-speed silicon modulator with band equalization," *Opt. Lett.*, vol. 39, no. 16, pp. 4839–4842, 2014.

[60] F. Reif, *Fundamentals of statistical and thermal physics*. Waveland Press, 2009.

[61] F. Pobell, *Matter and methods at low temperatures*. Springer Science & Business Media, 2007.

[62] S. W. Van Sciver, "Helium cryogenics, international cryogenics monograph series," 2012.

[63] S. M. Sze, *Semiconductor devices: physics and technology*. John Wiley & Sons, 2008.

[64] Y. Tsay, B. Gong, S. Mitra, and J. Vetelino, "Temperature dependence of energy gaps of some iii-v semiconductors," *Physical Review B*, vol. 6, no. 6, p. 2330, 1972.

[65] Y. P. Varshni, "Temperature dependence of the energy gap in semiconductors," *physica*, vol. 34, no. 1, pp. 149–154, 1967.

[66] M. A. Green, "Intrinsic concentration, effective densities of states, and effective mass in silicon," *Journal of Applied Physics*, vol. 67, no. 6, pp. 2944–2954, 1990.

[67] C. P. Poole Jr, *Encyclopedic Dictionary of Condensed Matter Physics*. Academic Press, 2004.

[68] B. M. Askerov, *Electron transport phenomena in semiconductors*. World scientific, 1994.

[69] B. Van Zeghbroeck, "Principles of semiconductor devices," *Colarado University*, 2004.

[70] D. Klaassen, "A unified mobility model for device simulation—II. temperature dependence of carrier mobility and lifetime," *Solid-State Electronics*, vol. 35, no. 7, pp. 961–967, 1992.

[71] D. Klaassen, "A unified mobility model for device simulation—I. model equations and concentration dependence," *Solid-State Electronics*, vol. 35, no. 7, pp. 953–959, 1992.

[72] D. Klaassen, "A unified mobility model for device simulation," in *Electron Devices Meeting, 1990. IEDM'90. Technical Digest., International*, pp. 357–360, IEEE, 1990.

[73] G. Masetti, M. Severi, and S. Solmi, "Modeling of Carrier Mobility Against Carrier Concentration in Arsenic-, Phosphorus-, and Boron-Doped Silicon," *IEEE Trans. Electron Devices*, vol. 30, no. 7, pp. 764–769, 1983.

[74] C. G. Van de Walle, "Effects of impurities on the lattice parameters of GaN," *Physical Review B*, vol. 68, no. 16, p. 165209, 2003.

[75] G. Ludwig and R. Watters, "Drift and conductivity mobility in silicon," *Physical Review*, vol. 101, no. 6, p. 1699, 1956.

[76] F. Morin and J. Maita, "Electrical properties of silicon containing arsenic and boron," *Physical Review*, vol. 96, no. 1, p. 28, 1954.

[77] D. S. Betts, *Refrigeration and thermometry below one Kelvin*. Sussex University Press, 1976.

[78] P. Flubacher, A. Leadbetter, and J. Morrison, "The heat capacity of pure silicon and germanium and properties of their vibrational frequency spectra," *Philosophical Magazine*, vol. 4, no. 39, pp. 273–294, 1959.

[79] C. Glassbrenner and G. A. Slack, "Thermal conductivity of silicon and germanium from 3 Ks to the melting point," *Physical Review*, vol. 134, no. 4A, p. A1058, 1964.

[80] R. Zeller and R. Pohl, "Thermal conductivity and specific heat of noncrystalline solids," *Physical Review B*, vol. 4, no. 6, p. 2029, 1971.

[81] D. Mann, "User's manual of property data in graphic format.[cryogenic temperatures]," 1977.

[82] F. Nix and D. MacNair, "The thermal expansion of pure metals: copper, gold, aluminum, nickel, and iron," *Physical Review*, vol. 60, no. 8, p. 597, 1941.

[83] H. Li, "Refractive index of silicon and germanium and its wavelength and temperature derivatives," *Journal of Physical and Chemical Reference Data*, vol. 9, no. 3, pp. 561–658, 1980.

[84] M. Nedeljkovic, S. Stankovic, C. J. Mitchell, A. Z. Khokhar, S. A. Reynolds, D. J. Thomson, F. Y. Gardes, C. G. Littlejohns, G. T. Reed, and G. Z. Mashanovich, "Mid-infrared thermo-optic modulators in SOI," *IEEE Photon. Technol. Lett.*, vol. 26, no. 13, pp. 1352–1355, 2014.

[85] A. Malik, S. Dwivedi, L. Van Landschoot, M. Muneeb, Y. Shimura, G. Lepage, J. Van Campenhout, W. Vanherle, T. Van Opstal, R. Loo, *et al.*, "Ge-on-Si and Ge-on-SOI thermo-optic phase shifters for the mid-infrared," *Opt. Express*, vol. 22, no. 23, pp. 28479–28488, 2014.

[86] M. Pu, L. Liu, W. Xue, Y. Ding, L. H. Frandsen, H. Ou, K. Yvind, and J. M. Hvam, "Tunable microwave phase shifter based on silicon-on-insulator microring resonator," *IEEE Photonics Technology Letters*, vol. 22, no. 12, pp. 869–871, 2010.

[87] M. Kawachi, "Silica waveguides on silicon and their application to integrated-optic components," *Optical and Quantum Electronics*, vol. 22, pp. 391–416, Sep 1990.

[88] N. C. Harris, Y. Ma, J. Mower, T. Baehr-Jones, D. Englund, M. Hochberg, and C. Galland, "Efficient, compact and low loss thermo-optic phase shifter in silicon," *Opt. Express*, vol. 22, no. 9, p. 10487, 2014.

[89] M. R. Watts, J. Sun, C. DeRose, D. C. Trotter, R. W. Young, and G. N. Nielson, "Adiabatic thermo-optic mach–zehnder switch," *Optics letters*, vol. 38, no. 5, pp. 733–735, 2013.

[90] Q. Fang, J. F. Song, T.-Y. Liow, H. Cai, M. B. Yu, G. Q. Lo, and D.-L. Kwong, "Ultralow power silicon photonics thermo-optic switch with suspended phase arms," *IEEE Photon. Technol. Lett.*, vol. 23, no. 8, pp. 525–527, 2011.

[91] J. Song, Q. Fang, S. Tao, T. Liow, M. Yu, G. Lo, and D. Kwong, "Fast and low power michelson interferometer thermo-optical switch on soi," *Optics express*, vol. 16, no. 20, pp. 15304–15311, 2008.

[92] J. Xia, J. Yu, Z. Wang, Z. Fan, and S. Chen, "Low power 2× 2 thermo-optic soi waveguide switch fabricated by anisotropy chemical etching," *Optics communications*, vol. 232, no. 1-6, pp. 223–228, 2004.

[93] W. R. Thurber, R. L. Mattis, Y. M. Liu, and J. J. Filliben, "Resistivity-Dopant Density Relationship for Boron-Doped Silicon," *Journal of The Electrochemical Society*, vol. 127, p. 2291, oct 1980.

[94] L. Wang and J. F. McDonald, *Modeling of High Speed Metal-Insulator–Semiconductor Inter connections: The effect ILD on slow–wave attenuation*. PhD thesis, Rensselaer polytechnic Institute,, 1998.