Development of a Device for On-Die Double-Pulse Testing and Measurement of Dynamic On-Resistance of GaN HEMTs

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Abstract. *On-die testing can accelerate development of semiconductor devices, but poses certain challenges related to high frequency and high current switching. This paper describes design and development of a tester for double-pulse switching test and measurement of dynamic on-state resistance of unpackaged High-Electron-Mobility Transistors (GaN HEMTs). The tester is capable of switching an inductive load at drain-to-source voltage up to 400 V and drain current up to 10 A. Design challenges resulting from specific properties of GaN HEMTs and on-die measurement are explained, and solutions are proposed. Essential parts of the developed device are described, including low inductance gate-driver and measurement methods. Modified drain voltage clamping circuit for accurate on-state drain voltage measurement is described. The tester is constructed as a printed circuit board, integrated into a probe station. Voltage and current waveforms are measured with oscilloscope and used to calculate the on-resistance. Results of a reference measurement with commercially available packaged transistors are presented. Waveforms measured on experimental unpackaged normally-off GaN HEMT samples are also presented and discussed. The proposed tester device proved to be capable of performing the dynamic on-resistance measurement with satisfactory results.*

Keywords

Double-Pulse switching Test, dynamic on-resistance, GaN HEMT, inductive load, on-die measurement, RDSon extraction, tester development, wafer measurement, wide bandgap semiconductor.

1. Introduction

Gallium Nitride based High-Electron-Mobility Transistors (GaN HEMTs) have become a synonym for high-efficiency and high-frequency power switching devices. Modern commercially available lateral GaN HEMTs can provide some interesting advantages over dominant silicon MOSFETs, including significantly lower gate and output charges or negligible reverse recovery time. These characteristics allow for lower switching losses and higher power density of GaN HEMTs particularly at higher switching frequencies [1].

However, a phenomenon known as current collapse, caused by electron trapping in GaN HEMTs can increase the on-state Resistance ($R_{DS(on)}$) in dynamic conditions, i.e. for a short time after the transistor turn-on, particularly at higher blocking voltages (see Fig. 1). This phenomenon has been addressed by many researchers and in the latest generations of GaN devices, and significant reduction of dynamic $R_{DS(on)}$ ($dynR_{DS(on)}$) has been achieved. It has been presented that carbon doping of GaN (AlGaN) has large impact on $dynR_{DS(on)}$, but also impact of passivation and field plate geometry was reported [2], [3], and [4].

To investigate dynamic degradation of $R_{DS(on)}$, it is necessary to accurately measure on-state drain-to-source voltage $V_{DS(on)}$ and drain current ID which are used to calculate $R_{DS(on)}$. The test setup must be able to accurately capture these waveforms starting from the first hundreds of nanoseconds after the transistor turn-on. Double-Pulse switching Test (DPT) is a standard evaluation method of switching properties of semiconductor devices. Several publications focused on DPT of already packaged GaN HEMTs, e.g. [5] and [6]. However, packaging of experimental devices adds more complexity to the development process. Therefore, a reliable wafer-level analysis contributes considerably to acceleration of the development process. A device for on-wafer DPT was developed by [7]. Their setup is used for small experimental structures only which do not require high drain current. Therefore, it is not suitable for testing full-scale power transistors. Their tester is attached to a microscope arm and has wires soldered directly to probes, which makes manipulation with the probes and wafer relatively complicated. Also, there is a mechanical coupling between the microscope and the wafer that can result in damage to the samples.

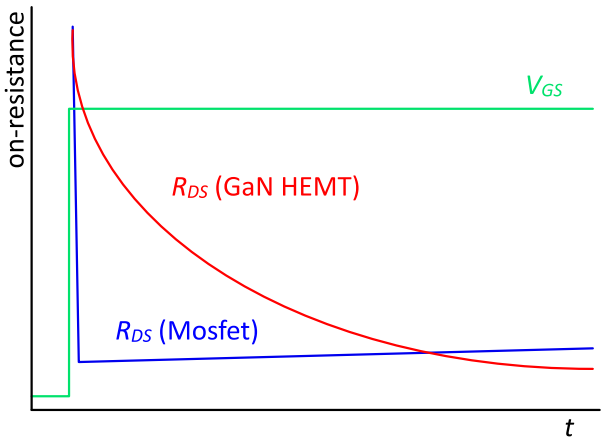


Fig. 1: Typical behavior of GaN HEMT and Si MOSFET on-resistance. While MOSFET curve drops rapidly to static R_{DS} value, HEMT $dynR_{DS(on)}$ is higher after the turn-on due to current collapse.

2. Double-Pulse Test

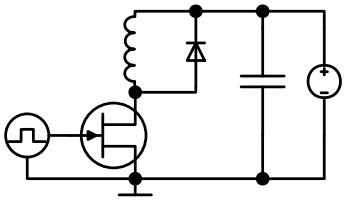
Double-pulse switching test operates on the principle of switching a high-side inductive load using the Device Under Test (DUT) as the switch (Fig. 2(a)). Duration of the first pulse (t_1) is used to set the required inductor current and can be calculated using a formula for a series R-L circuit current. However, since the contributions of the DUT on-resistance and the parasitic resistance are negligible, a simpler formula for inductor current is sufficient for estimation of t_1:

$$i(t) = \frac{1}{L}\int v_L(t)dt. \tag{1}$$

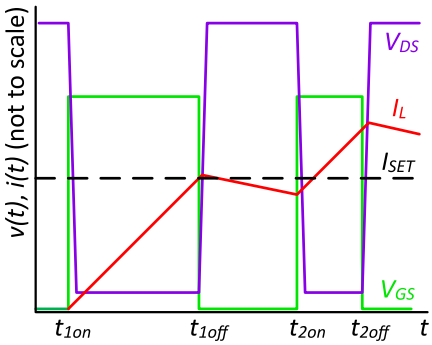
Since the voltage across the inductor is constant and equal to the supply voltage, t_1 can be expressed as:

$$t_1 = L\frac{i_{test}}{V_{in}}. \tag{2}$$

As soon as drain current reaches the specified value, DUT is turned off and after a defined time it is turned on again. In between the pulses, the inductor current is freewheeled through a diode or a complementary switch and there is a slight decrease in the current due to parasitic resistance Turn-off characteristics of DUT are measured at the end of the first pulse and turn-on characteristics at the beginning of 2nd pulse. The 2nd pulse is also the point of interest for observation of $dynR_{DS(on)}$, since there is a quick transition from high drain voltage to high drain current (Fig. 2(b)).

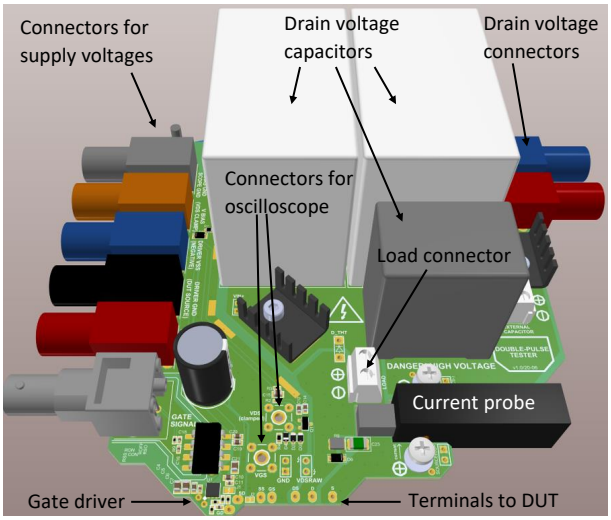


(a)



(b)

Fig. 2: (a) Simplified schematic of a double-pulse test setup. (b) Typical waveforms of gate (V_{GS}) and drain (V_{DS}) voltage, and inductor current I_L. The first pulse lasts until I_L reaches nominal current I_{SET}. Current at t_{2on} should be reasonably close to I_{SET}.



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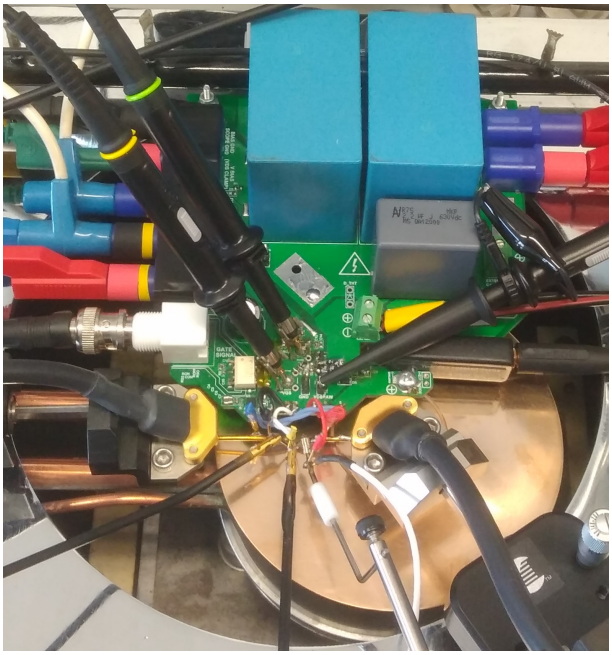
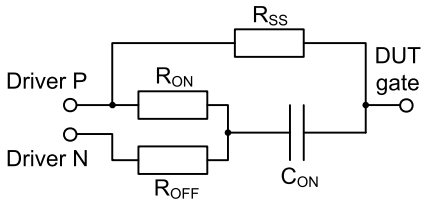


(b)

Fig. 3: (a) 3D model of the tester PCB design. (b) Full test setup with the tester integrated into the probe station.

3. Tester Design

The tester is constructed in a form of a Printed Circuit Board (PCB) without cover that connects to DUT via several wires and probes on a probe station (Fig. 3). This form was chosen to minimize the physical distance from DUT to gate driving circuitry since using any enclosure would complicate the placement of the tester in the probe station. Absence of enclosure poses risks in terms of operator safety, but since the probe station itself needs to be protected from accidental touch during high voltage operation, this solution does not require any additional safety precautions except for a capacitor discharge circuit. The device is capable of tests at a drain-to-source voltage (V_{DS}) up to 400 V. Drain current rating is designed up to 30 A, but in practice, it is limited by an external load inductor saturation and a current probe rating. Gate signal is fed from an external double-pulse signal generator and V_{DS} is provided by on-board capacitor bank, charged by laboratory DC power supply. Voltage and current waveforms are measured with an oscilloscope. The tester is derived from our earlier design of a resistive load switching tester [8]. This device served as a good platform for the development of an improved tester. Due to the fast-switching characteristics of HEMTs, design challenges include elimination of parasitic inductance, particularly in gate-source current loop and oscilloscope probes grounding. Also, the connection between the freewheeling diode's anode and DUT drain terminal should have low inductance to prevent drain voltage spikes after DUT turn-off.



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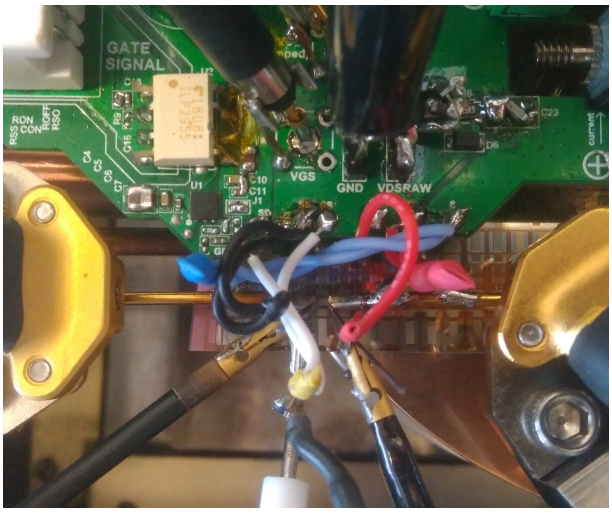


(b)

Fig. 4: (a) Gate R-C network generates negative V_{GS} at turn-off even if the gate driver does not support negative V_{GS}. (b) Detail of tester-to-DUT connection. Keeping wires as short as possible is essential to obtain accurate test results.

In general, this can be achieved by reducing the distance between components and length of connections, which is remarkably challenging in the context of on-die measurement. The physical size of the probes and

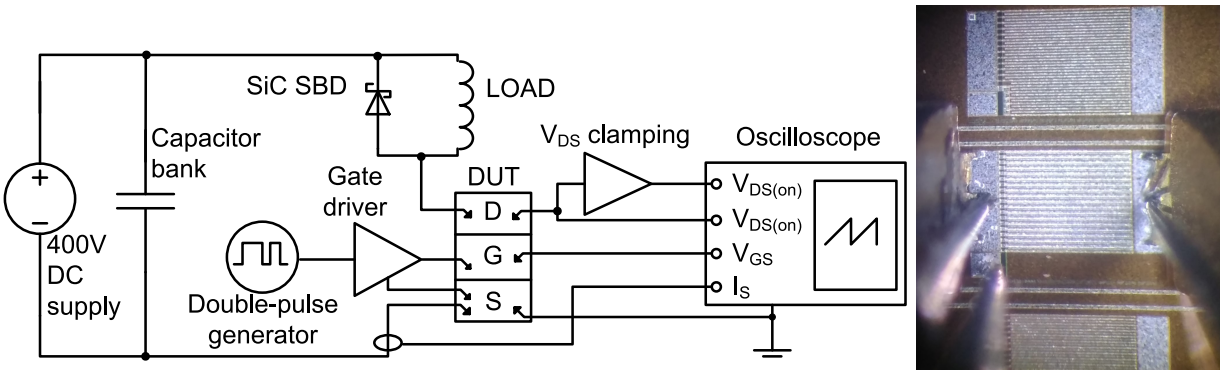


Fig. 5: (a) Simplified block diagram of the tester with sensing connections and probes to DUT. (b) Due to physical dimensions of tested transistors, gate driver G and S contacts had to be merged with oscilloscope V_{GS} and GND probes, therefore only 5-probe DUT connection was used in actual measurement. Charging and discharging of gate capacitances can affect $V_{DS(on)}$ reading due to voltage drop on the shared source probe.

wiring results in increased series inductance and resistance. Accurate measurement of current and voltage is also challenging. To achieve application-like switching conditions, turn-on and turn-off times need to be as low as tens of nanoseconds. Therefore, high $\frac{dV}{dt}$ and $\frac{dI}{dt}$ values are expected and the measurement setup must be capable of relatively high bandwidth and high dynamic range. Particularly for measurement of on-state drain voltage $V_{DS(on)}$, which swings from hundreds of volts in off-state to a few hundred millivolts, all in order of nanoseconds.

Since oscilloscopes are not able to measure precisely through such dynamic range, insertion of drain voltage clamping circuit is necessary to limit maximum voltage on $V_{DS(on)}$ probe and saturation of oscilloscope channel. Several clamping methods have been proposed [9]. Each of them represents a compromise between circuit complexity, accuracy of voltage reading, and measurement bandwidth.

3.1. Gate and Drain Circuits

Gate driver can supply adjustable positive and negative gate-to-source voltage up to 12 V peak-to-peak using dedicated GaN driver IC. Driver output can be fitted with a single gate resistor or with a resistor-capacitor network optimized for driving GaN HEMTs (Fig. 4(a)). This network is widely used in practical GaN HEMT applications and allows for negative gate voltage at turn-off even if the gate driver does not support negative V_{GS} [10] and [11].

The input signal is generated by an external double-pulse generator isolated by an on-board optoisolator. The drain circuit is supplied from a bank of high-frequency polypropylene film capacitors with low Equivalent Series Resistance (ESR) and inductance (ESL) and total capacitance of 82.2 μF. These are charged from an external power supply.

DUT is connected using wafer probes and flexible wires to the tester board in such a manner that the average length of a conductor from PCB to DUT is approximately 30 mm (Fig. 4(b)). Load inductor is physically located at a distance from the rest of the circuit to limit magnetic fields affecting measurement accuracy. SiC power diode is used for inductor freewheeling. Since the diode cannot be placed physically close to DUT, the stray inductance of the wiring may produce V_{DS} spikes. Therefore, an R-C snubber circuit is placed in parallel to DUT to suppress those spikes.

3.2. Sensing Circuits

To prevent gate and drain loop currents affecting measurements by voltage drops on wiring, separate wires and probe tips are used for every connection to DUT (see Fig. 5(a)). Such connection also prevents drain current from affecting V_{GS}, making use of Kelvin source connection.

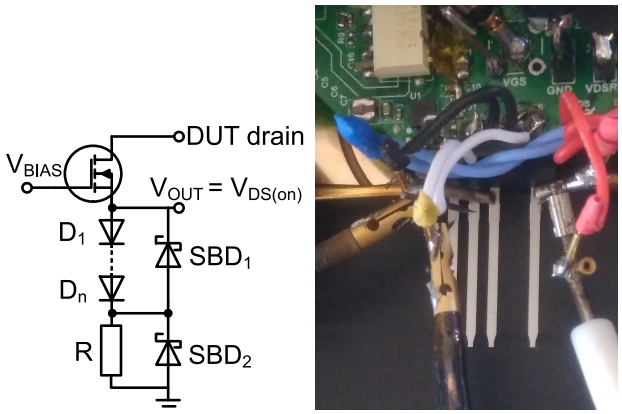
All oscilloscope probes are referenced to a single point (electrically and physically) and utilize a low-inductance grounding connection to reduce current loops. Ferrite rings are placed around oscilloscope probe cables to suppress common-mode voltages. Although great attention was paid to the tester-to-DUT connection, it remains the main source of parasitic resistance and inductance in the most sensitive part of the circuit. DUT current is measured at the source terminal (low side) due to the voltage rating of the current probe.

From different approaches to V_{DS} clamping, a circuit used by [12] was chosen, mainly for its zero-offset output voltage. Transient performance was improved

by selection of components with low current rating, i.e. low capacitance. To further enhance transient performance, a Zener diode was replaced by a series connection of several forward-biased diodes (Fig. 6(a)). In this circuit, the N-MOSFET is biased (partially open) in such a way, that off-state DUT drain voltage is clamped across it to a value slightly higher than the expected $V_{DS(on)}$. When DUT is turned on, the voltage at the N-MOS source terminal follows the drain voltage.

4. Test Results and Discussion

After the developed device was manufactured, it was tested to validate its performance and measurement accuracy.



(a) (b)

Fig. 6: (a) V_{DS} clamping circuit. V_{OUT} is limited to the sum of forward voltages of diodes $D_1 \ldots D_n$. (b) Testing influence of probe tips on the measurement using packaged SiC MOSFET. Only a slight difference compared to a device soldered directly to the tester.

Due to unavailability of a reference on-die tester device, the confirmation measurements were performed using transistors with known characteristics by comparing the measured values to the reference data. In the first step, packaged Si and SiC MOSFETs, and GaN HEMT samples were soldered to the tester connection wires and subjected to DPT switching. Dynamic $R_{DS(on)}$ was calculated from the measured voltage and current in the beginning of the 2nd pulse and compared to the static R_{DS} values.

Results of the MOSFETs measurements were within ±10 % of their static values. Reference GaN HEMTs exhibited some increase in $dynR_{DS(on)}$ at the beginning of the 2nd pulse. Therefore, R_{DS} values from the end of the 1st pulse were compared with the datasheet values. Increase of $dynR_{DS(on)}$ compared with the static values was in a range from 0 to +30 % even at the end of the pulse due to influence of $dynR_{DS(on)}$ and heating of the structure at higher I_D.

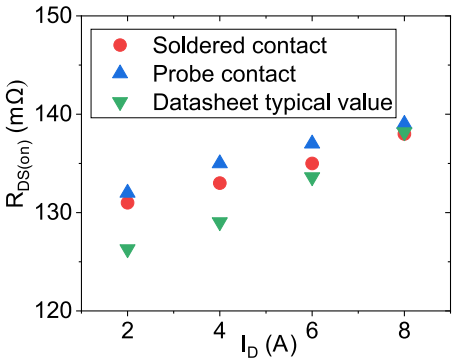
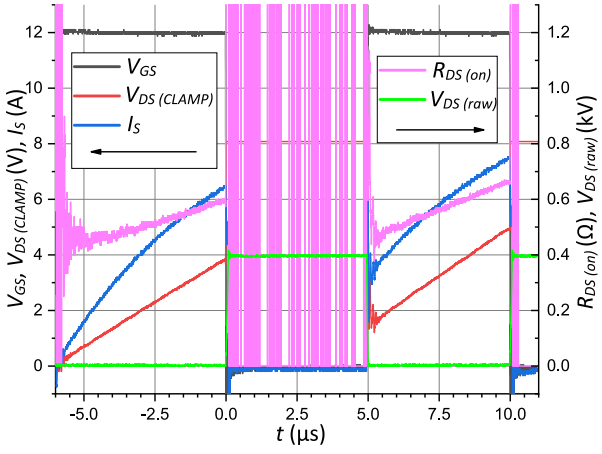
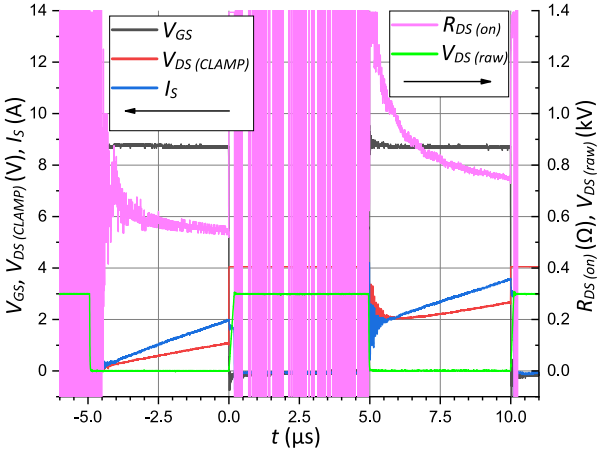


Fig. 7: On-resistance of a reference commercially available Si MOSFET measured at 1 µs of the 2nd pulse compared to datasheet typical values.



(a)



(b)

Fig. 8: (a) Waveforms measured on SiC MOSFET at 400 V and 4 A. The difference between the source current at the end of 1st and the beginning of 2nd pulse is a result of a relatively low inductance of the load. (b) Experimental GaN HEMT at 300 V and 2 A. Significant increase of $V_{DS(on)}$ and $dynR_{DS(on)}$ is at the beginning of 2nd pulse.

In the second step, the same transistors were contacted using wafer probes (needles) to determine the effect of the probes on the circuit (Fig. 6(b)). No significant difference was observed compared with the first validation step at switched current up to 10 A. The results suggest that the added inductance of the probe is negligible and so is the resistance of the probe tip contact. Comparison of on-resistance at the beginning of the 2nd pulse is in Fig. 7.

In the third step, the same measurements were repeated with unpackaged MOSFET devices to validate the connections between the probes and wafer. The results were again consistent with the devices' specifications, and thus the tester is considered to operate and measure accurately in the switching conditions up to $V_{DS} = 400$ V and $I_L = 10$ A.

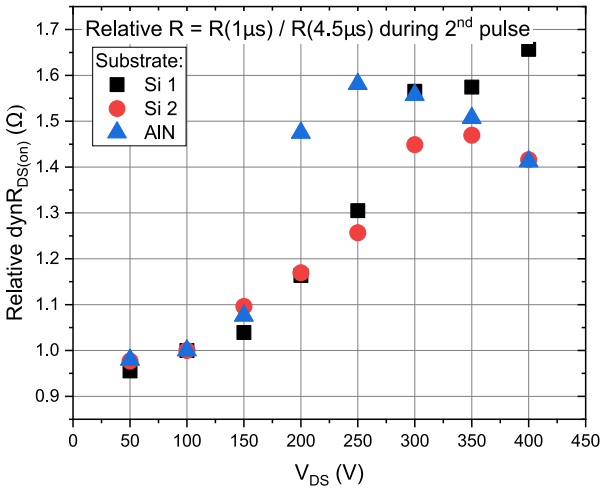
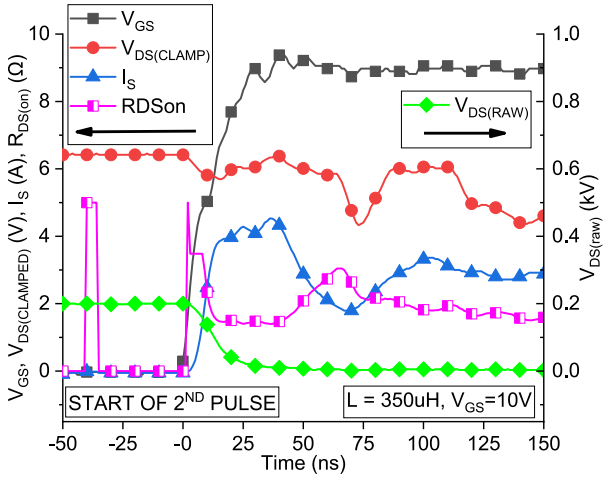


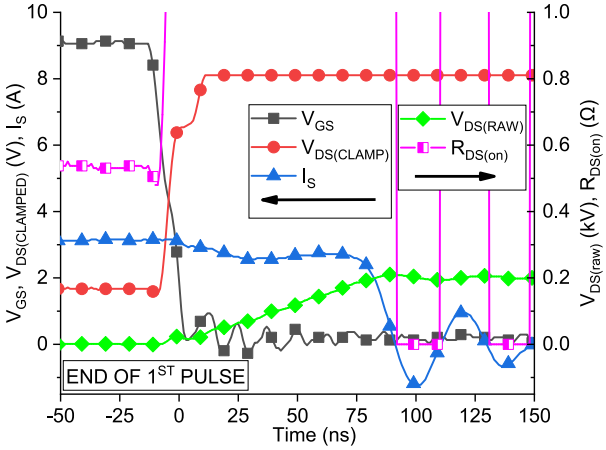
Fig. 9: Comparison of dynamic $R_{DS(on)}$ dependence on off-state V_{DS} of the same transistor structure on different substrates. $I_{SW} = 0.5$ A. At $V_{DS} = 50$ V the effect of heating is more pronounced than the $dynR_{DS(on)}$, thus the lower relative $dynR_{DS(on)}$ value.

Measurements at higher I_D were not performed mostly due to limitations of the inductors used. Typical test waveforms are displayed in Fig. 8. The higher noise in R_{DS} signal at the beginning of 1st pulse is due to the low drain current, which manifests in noise being more significant compared to the desired signal. In between the pulses, clamped drain voltage can overshoot out of the oscilloscope range due to a switching transient, but the overshoot is not high enough to saturate the oscilloscope channel and affect $V_{DS(on)}$ measurement during 2nd pulse.

After the tester was validated to operate properly, several experimental unpackaged 600 V-rated GaN HEMTs were also tested. Some of them exhibited a significant increase of dynamic $R_{DS(on)}$ particularly at higher drain voltages (Fig. 8(b)). Figure 9 compares differences in $dynR_{DS(on)}$ of a single HEMT structure fabricated on different substrates as measured using the tester. Figure 10 shows typical waveforms during turn-on and turn-off events of an experimental GaN-on-Si transistor with switching times in the order of 10^{-8} s. Due to the relatively large physical distance from DUT to the freewheeling diode, a snubber circuit is needed to suppress the turn-off V_{DS} spike and is observable in the measurements (Fig. 10(b)).



(a)



(b)

Fig. 10: (a) Turn-on waveforms of an unpackaged experimental GaN HEMT at the beginning of the 2nd pulse. Note the dynamic $R_{DS(on)}$ value compared to (b). Drain voltage $V_{DS(CLAMP)}$ is measured at the output of the clamping circuit, $V_{DS(RAW)}$ is measured directly at the DUT drain terminal. (b) Turn-off waveforms of the same transistor at the end of the 1st pulse. The gradual increase of $V_{DS(RAW)}$ and the lagging source current (I_S) result from charging of a snubber capacitor parallel to the DUT.

5. Conclusion

On-die measurement and diagnostics are useful tools for rapid development since the experimental semiconductor devices do not need to be diced and packaged

prior to the tests. Dynamic on-state resistance is a typical issue of GaN HEMTs. However, commercial instruments for on-wafer extraction of dynamic on-resistance are not currently available. Therefore, a tester device for double-pulse switching and on-die measurement of dynamic on-state resistance of GaN HEMTs was designed, built, and integrated into a probe station. Design challenges were identified, analyzed and solutions to these challenges were described and used in the design. Measurement methods for accurate capture of waveforms necessary to calculate the value of dynamic on-resistance were described. The device was validated using packaged commercial Si and SiC MOSFETs, GaN HEMTs, and unpackaged experimental transistors with drain voltage set up to 400 V and drain current up to 10 A. On-resistance values measured during double-pulse tests were compared to static $R_{DS(on)}$ measurements and to the respective datasheet values with satisfactory results. The tester is built in such a way that it can be used within various probe stations and it proved to be sufficiently accurate for on-die measurement of $R_{DS(on)}$ of experimental GaN HEMTs.

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Author Contributions

J.M. and J.K. devised the concept, form and specifications of the device. J.K. and M.M. contributed with the hardware schematic design, layout, component selection and instruments connections. K.G. programmed a double-pulse generator, provided 3D-printed parts and helped with device assembly. J.M. and A.C. performed measurements, sample characterization and processed the data. M.J. provided the samples and consulted the hardware design. J.M. acquired funding and supervised the project. J.K. wrote the manuscript in consultation with all authors.

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