Ultra-Thin Chips With ISFET Array for Continuous Monitoring of Body Fluids Ph

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***Abstract*—This paper presents ISFET array based pH-sensing system-on-ultra-thin-chip (SoUTC) designed and fabricated in 350 nm CMOS technology. The SoUTC with the proposed current-mode active-pixel ISFET circuit array is desined to operate at 2 V and consumes 6.28 μW per-pixel. The presented SoUTC exhibits low sensitivity to process, voltage, temperature and strain-induced (PVTS) variations. The silicon area occupancy of each active-pixel is 44.9 $\times$ 33.5 μm^2 with an ion-sensing area of 576 μm^2. The design of presented ISFET device is analysed with finite element modeling in COMSOL Multiphysics using compact model parameters of MOSFET in 350 nm CMOS technology. Owing to thin ($\sim$30 μm) Si-substrate the presented SoUTC can conform to curvilinear surfaces, allowing intimate contact necessary for reliable data for monitoring of analytes in body fluids such as sweat. Further, it can operate either in a rolling shutter fashion or in a pseudo-random pixel selection mode allowing the simultaneous detection of pH from different skin regions. Finally, the circuits have been tested in aqueous Dulbecco's Modified Eagle Medium (DMEM) culture media with 5–9 pH values, which mimics cellular environments, to demonstrate their potential use for continuous monitoring of body-fluids pH.**

***Index Terms*—pH measurement, ultra-thin chip, ion-sensitive field effect transistors (ISFET), COMSOL, CMOS integrated sensors, sensor arrays.**

I. Introduction

WEARABLE microsystems with sensors and integrated signal processing and data transmission capability could boost digital health by providing non-invasive tools for continuous and real-time monitoring of health parameters [1], [2]. This is also aided by recent progress in flexible electronics as they allow such sensor systems to conform to curvilinear surfaces, such as human skin, which is necessary for robust physiological measurements [3], [4]. Some of these technological advances have been already exploited to develop devices for real time monitoring of various health parameters such as heart rate [5], blood oxygen and pressure [6], [7], respiration rate [8], body posture [9], skin stretching [10], skin temperature [11], [12] and brain activity [13]. These existing solutions mainly focus on measurement of physiological parameters. They could be further advanced to develop a complete monitoring and diagnostic tool by adding the devices that monitor complementary biochemical parameters from bio-fluids such as sweat [14], which can be a treasure trove for the detection of several chronic ailments. As a result, a few recent studies have focussed on the wearable epidermal electronics for continuous measurements of electrolytes and metabolites in body fluids [15]–[17].

Among various parameters in body fluids, the pH in sweat is critical as it can reflect metabolic activity, body's exercise intensity and dehydration level. Most of the reported epidermal electronic systems, developed so far to measure pH, have used printed ion-selective electrodes (ISEs) in conjunction with rigid commercial off-the-shelf electronics for signal processing and digitisation [18]–[20]. Whilst printed passive ISEs offer an attractive route for electrochemical measurements, the ion-sensitive field-effect transistors (ISFETs) could be a better alternative, owing to their complementary metal-oxide-semiconductor (CMOS) compatibility and the possibility of having full system on chip. The ISFETs have been mainly used for label-free detection of H^+ ions [21]. However, with a stack of silicon oxide and silicon nitride (deposited primarily as passivation at the surface of the chip) they can be designed for pH measurement. Using pH to current/voltage conversion circuits, integrated analogue-to-digital converters (ADCs) and multiplexing techniques for proper signal-to-noise ratio (SNR), it is possible to obtain a complete ISFET based microsystem. Whilst avoiding off-chip parasitic and interferences, this will also significantly reduce the power consumption, area and overall cost of the system [22]–[24]. However, in the current rigid form-factors, it is challenging to use the CMOS-based ISFETs as an epidermal electronic system, which require conformal contact with curvy skin surface. This challenge could be overcome by using suitable wafer or chip thinning techniques, which can lead to silicon dies to have $<$50 µm thickness [25]–[27]. The bending or strain-induced variations in the devices' performance of such ultra-thin chips (UTCs) could also be exploited to calibrate the instabilities such as drift in ISFETs [26], [28], [29]. Conformal chips are also required for the fabrication of systems deployed on surfaces with a high curvature such as fingertips, biological tissues and electronic pills [30]. Furthermore, ultra-thin chips

Manuscript received August 28, 2021; revised November 16, 2021 and December 28, 2021; accepted January 3, 2022. Date of publication January 10, 2022; date of current version February 16, 2022. This work was supported in part by the Engineering and Physical Sciences Research Council (EPSRC) through Engineering Fellowship for Growth under Grant EP/R029644/1, in part by the Centre for Doctoral Training in Intelligent Sensing and Measurement under Grant EP/L016753/1, and in part by the European Commission (EU) through Marie Skłodowska-Curie Innovative Training Network – INTUITIVE under Grant H2020-MSCA-ITN-2019-861166. This paper was recommended by Associate Editor M. Johnston. *(Corresponding author: Ravinder Dahiya.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TBCAS.2022.3141553.

Digital Object Identifier 10.1109/TBCAS.2022.3141553

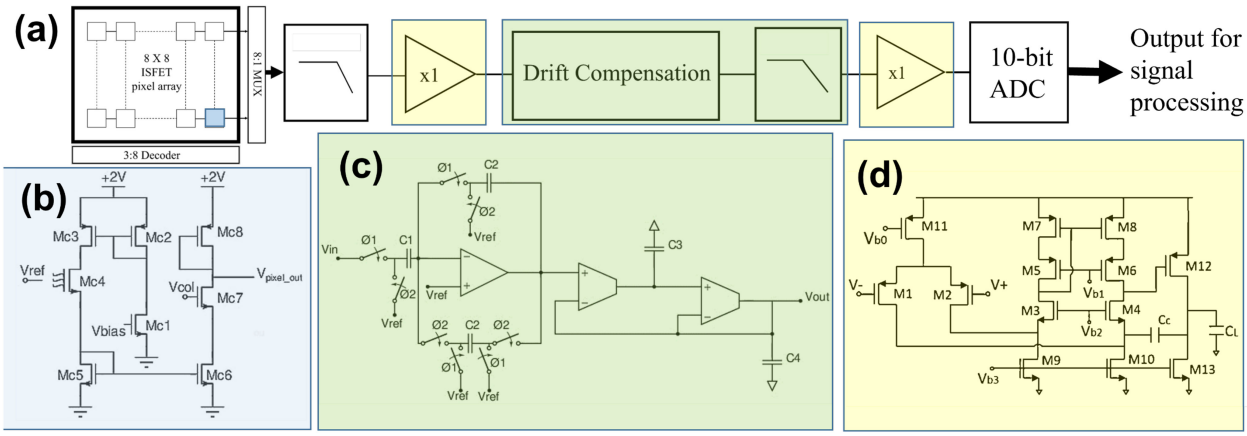

Fig. 1. (a) Signal chain of ISFET array in current-mode readout from pH recording stage to digital conversion for data analysis, (b) individual pixel circuit topology, (c) drift compensation using correlated double sampling (CDS), (d) Folded cascode configuration for settling kickback occurring due to the ADC at the start of the acquisition period.

are utilized for 3D stacking of chips in order to increase device density without occupying larger areas [31].

Considering the above advantages of UTCs, herein we present a pH-sensing system-on-ultra-thin-chip (SoUTC) designed and fabricated in 350 nm CMOS technology. The presented pH-sensing microsystem is realised on ∼30 µm thick UTC using an "unmodified" CMOS process. The chip contains a current-mode in-pixel ISFET readout and a switched-capacitor correlated double sampling (CDS) circuit in the signal-chain to compensate for low-frequency instabilities, such as drift and strain-induced variations [32]. The initial results related to this paper were presented at IEEE ISCAS 2021 [32]. In this extended paper, we present further details and analysis of the ISFET chip, particularly the device analyses with finite element modelling in COMSOL Multiphysics using compact model parameters of MOSFET in 350 nm CMOS technology. The utilisation of numerical simulations paves the way towards physics-oriented design of complex systems comprising of solid-state physics in conjunction with mass transfer and thermodynamic phenomena. The limitations of circuit level simulators such as SPICE render them in-efficient towards ISFET design. Furthermore, intricate systems constituting of multi-ionic species and their transport in fields cannot be captured via complete analytical models most of which require numerical analysis. In addition to simulations targeted towards the ISFET device, system level simulations have been carried out taking into account mechanical bending of the integrated circuit based on our previously published results [27]. The simulation results show good resilience towards PVT variations and small deviations in the SNR and total harmonic distortion (THD) of the active-pixel topology at different strained conditions. The presented ISFET based SoUTC is tested in aqueous Dulbecco's Modified Eagle Medium (DMEM) solution and it shows a sensitivity of ∼10 mV/pH in a 5–9 pH range and a reference electrode voltage bias 1.5–1.7 V. Experimental results also show an acceptable degradation in figures of merit (FoM) constituting of the signal-to-noise ratio (SNR) and total harmonic distortion (THD) of the analogue front-end on the thin die compared to its bulky counterpart with reduced standard deviation in the FoM across all pixels of the ISFET array.

The remainder of this paper is organised as follows. Section II presents the overall design of the ISFET as well as the presented system along with details of the key blocks. Detailed multi-physics simulations of the ISFET are presented in Section III. The fabrication of the SoUTC and the experimental results are described in Section IV. This section also presents the compatibility between the experimental and simulated sensitivity of the ISFET device. Finally, a summary of key outcomes and future prospects are given in Section V.

II. ISFET and System Design

A. Overall System Architecture

The block diagram of the presented pH microsystem, having current-mode readout circuitry interfaced with the ISFET M_c4, is shown in Fig. 1(a). The first block is an 8 × 8 pixel array. Each pixel (shown in Fig. 1(b)) is selected via external column addresses functioning as inputs to a 3:8 decoder for column select via the pixel transistor M_c7. The pixel output is transferred to the next stage via an analog multiplexer consisting of a set of transmission gates utilised for row-select. The transmission gates have been designed to provide low on-resistance, low THD and high SNR. The output of the pixel is filtered using a passive low pass filter (LPF), which is subsequently connected to the drift compensation circuit (Fig. 1(c)) via a unity gain buffer (Fig. 1(d)). The analog output of the buffer is converted to a digital signal by an on-chip 10-bit successive approximation register (SAR) ADC. Each pixel is selected via a bias voltage provided by a 10 bit DAC. The ADC and DAC are standard cells with an SNR of above 50 dB. Each IC of area 16 mm^2 consists of 512 ISFET pixel circuits distributed over the chip in a split-array format with a pitch of 40 µm between two adjacent individual pixel circuits of each array. This arrangement allows for the deposition of on-chip miniaturized reference electrodes with the ISFET. The split-array format of the chip allows for improved compartmentalization which can be utilized for multi-analyte detection and turning off of unused arrays, thus saving power. Furthermore, the array programmability can be utilized for recording small variations in pH while accounting for electrochemical drift via a compensation circuit.

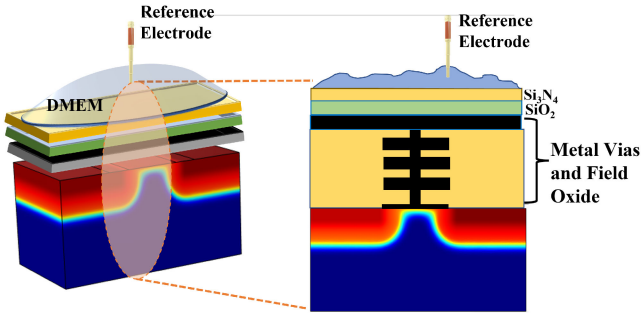

Fig. 2. Schematic of a single CMOS ISFET with nitride sensing membrane placed in DMEM biased with a reference electrode (source-drain contacts and thin-oxide are not shown for simplicity).

B. CMOS ISFET Sensor Design

The target ISFET is fabricated in 4 metal layer 350 nm CMOS technology. The silicon die is not packaged and hence, the passivation layer is available for exposure to the surrounding electrolyte. The top sensing stacked dielectric consists of a silicon nitride layer above the silicon oxide, each of 1 µm thickness as shown in Fig. 2. The total sensing area of the ISFET in contact with the surrounding cell culture media is 576 µm^2. In order to achieve sensor-device level analysis, in-depth multiphysics simulations have been carried out, of which the details are given in Section III. The compatibility between the experimental results and simulations will be demonstrated.

C. Current-Mode ISFET Pixel Design

The presented active pixel topology of which the transistors are shown by M_{ci} (Fig. 1(b)) operates in the current-mode allowing for accelerated signal processing of recorded signals. The choice of a current-mode readout over a voltage- mode read-out is motivated by complexity levels required for maintaining a constant drain current under strain. Furthermore, the proposed 8-Transistor (8T) addressable current-mode pixel circuit reduces sensitivity to the power supply noise and enables rapid signal processing. Existing voltage-mode read-outs using source follower exhibit low power supply rejection ratio. The maximum number of transistors between supply and ground is 3 in the presented pixel circuit. Hence, the supply voltage is reduced to 2 V and therefore, the power consumption of the pixel circuit is reduced. The low input impedance common-gate amplifier acts as both a column-select and a current-buffer. The transistor M_c1 is biased by an external signal V_{bias} via a 10-bit digital-to-analog converted (DAC) and a unity gain amplifier, increasing programmability of the active pixel for calibration purposes. Each pixel, of which the ISFET is operating in the weak inversion region, consumes only 6.28 µW of power with a supply voltage of 2 V. The rest of the circuit blocks are designed for a high SNR (above 50 dB).

The pixel's dimensions are 44.9 µm × 33.5 µm with an ion-sensing electrode of size 24 µm × 24 µm. Each recording pixel operates according to the following mechanism: Variation of the effective surface charge density of ISFET M_c4 due to pH variation will cause a corresponding change in its drain current. The current is mirrored through transistors M_c5 and M_c6 to the branch constituting common-gate transistor M_c7 with diode-connected load M_c8 as shown in Fig. 1(b). Effectively, transistors M_c6 and M_c7 form a cascode stage reducing the current mirroring error. Table I lists the sizes of all transistors in the pixel circuit. The expression for the relative error of the mirrored drain current ($\Delta I_{DS}/I_{DS}$) taking into account random mismatch effects in β (i.e., $\mu C_{ox} W/L$) and threshold voltage is given by Eq. 1

TABLE I
DIMENSIONS OF TRANSISTORS UTILISED IN EACH PIXEL

Transistor	Width (W, µm)	Length (L, µm)
M_c1	1	0.5
M_c2	40	0.9
M_c3	40	0.9
M_c4 (ISFET)	60	0.5
M_c5	1	20
M_c6	1	20
M_c7	1	10
M_c8	2	4

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta \beta}{\beta} - \frac{g_m}{I_{DS}} \Delta V_{th} \tag{1}$$

where g_m and V_{th} denote the average transconductance and threshold voltage of the current-mirror transistors. The noise at the output of the current mirror constituting of M_c5 and M_c6 is the summation of the noise current generated in the channels of ISFET M_c4, and transistors M_c5 and M_c6. Hence, an increased overdrive voltage contributes to noise minimisation, which is required for the detection of low variations in the fluid pH on the chip. In the low-frequency regime, transistors M_c6 and M_c8 are the primary contributors to the input referred noise of the cascode structure given by Eq. 2

$$\overline{V_{n,in}^2} = 4kT \left(\frac{g_{m8}}{g_{m6}^2} + \frac{1}{g_{m6}} \right) + \frac{1}{C_{ox}} \left(\frac{K_p g_{m8}^2}{(WL)_{M8} g_{m6}^2} + \frac{K_n}{(WL)_{M6}} \right) \frac{1}{f} \tag{2}$$

where g_{mi} denotes the transconductance of transistor M_{ci}. The flicker noise coefficients for n-channel and p-channel devices are given by K_n and K_p, respectively. In order to analyse the SNR and THD of the presented circuit, the compact model derived in our previous studies is used [24], [27], [33].

On an average, the extracted variation in the SNR and THD of the pixel circuit output in the compressed state are −0.9 dB and 6.29 dB, respectively. Similarly, variations of 0.24 dB in SNR and −2.23 dB in THD are observed in the tensile state indicating less susceptibility to process variations and strain. The primary parameters contributing to variations in the noise performance of strained circuits are the transconductance of transistors M_c6 and M_c8 as it is evident from Eq. 2. Strain alters mobility and threshold voltage of the transistors as the chip is bent. The SNR and THD of the current-mode readout topology for an input voltage range of 0-5 mV superimposed on V_{ref} is extracted from

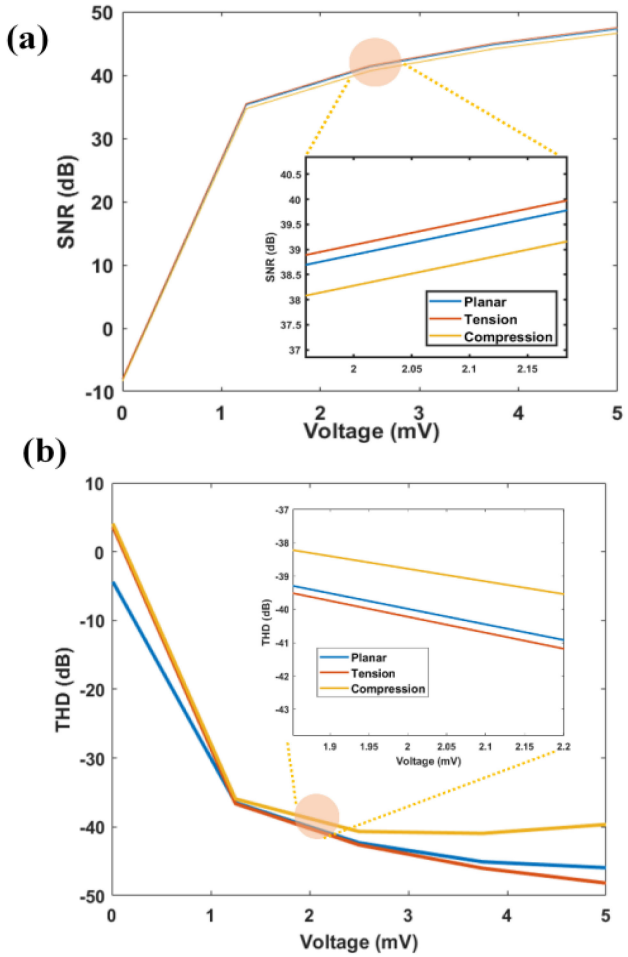

Fig. 3. Simulated (a) SNR and (b) THD of each pixel topology versus input voltage under no stress (planar), and tensile and compressive stress.

simulation. The simulation results are shown in Fig. 3(a) and (b), respectively. The output voltage of the pixel is then transmitted to the drift compensation circuit via a low pass filter and analog buffer, as shown in Fig. 1.

D. Strain and Drift-Induced Compensation Circuit

The combined effects of drift due to ultra-low frequency ionic diffusion across the sensing membrane and dielectric stack as well as strain due to bending of chips placed on non-planar surfaces leads to temporal variations of pixel output even under constant pH and temperature conditions. In order to reduce the drift in the system, correlated double sampling (CDS) circuit is used with two non-overlapping clock phases with the reference voltage controlled by the bias of the bulk solution (Fig. 1(c)) [34]. The output voltages in the sampling phase ϕ_1 and hold phase ϕ_2, are given by equations (3) and (4) respectively under the assumption of $C_1 = C_2$.

$$V_{out}\,(n)\ at\ \phi_1 = V_{in}\ (n) - V_{in}\,(n-1) + V_{ref} \tag{3}$$

$$V_{out}\,(n)\ at\ \phi_2 = \ (V_{in}\,(n-1)) \tag{4}$$

As expressed by Eq. 3, the analog signal at the input of the CDS (V_{in}) is sampled and the difference between the two consecutive samples of V_{in} is available at ϕ_1 to cancel the common-mode drift and strain-induced variations. The CDS circuit is followed by a low-pass filter. To remove the kickback caused during charge rebalancing at the input of the CDS circuit, a two-stage folded-cascode circuit with active load is utilised for the buffer stage [35]. This is incorporated at the input of the drift compensation block. Transistor sizes constituting the folded cascode are given in Table II. The open loop gain and CMRR of the general purpose folded cascode amplifier are 53 dB and 132 dB, respectively while providing 68.1° phase margin. Its open loop output resistance is 80 kΩ and consumes a power of 1.2 mW.

TABLE II
DIMENSIONS OF TRANSISTORS UTILISED IN FOLDED CASCODE AMPLIFIER

Transistor	Width (W, µm)	Length (L, µm)
M1,2	200	1
M3,4	36	1
M5,6	200	1
M7,8	132	1.5
M9,10	2	72
M11	1	25
M12	1	250
M13	1	200

At low frequencies, the input-referred thermal noise density is given by Eq. 5. Further, the input referred offset due to process-induced random mismatch and mechanical strain in the chip is expressed by Eq. 6

$$\frac{\overline{e_n^2}}{\Delta f} = \frac{16kT}{3g_{m1}^2}\ (g_{m1} + g_{m7} + g_{m9}) \tag{5}$$

$$\sigma^2_{offset,\,in} = \sigma^2_{Vth_{M1,2}} + \left(\frac{g_{m7}}{g_{m1}}\right)^2 \sigma^2_{Vth_{M7,8}} + \left(\frac{g_{m9}}{g_{m1}}\right)^2 \sigma^2_{Vth_{M9,10}} \tag{6}$$

where, g_{mi} and σ_{VthMi} denote the transconductance and standard deviation of threshold voltage of transistor M_i. During integration with platforms which undergo dynamic bending (for example in wearable devices), the PMOS differential pair M1-M2, current sink M9-M10 and M7-M8 exhibit variations in their transconductance, which is reflected as a change in the input-referred thermal noise density and offset as seen in Eqs. 5 and 6. Hence, strained circuits provide an effective way in designing topologies of which the electrical properties are controlled by mechanical deformations. The simulated response of the transmission gate to strain exhibits no significant variations in THD as shown in Fig. 4(b) while its SNR is shifted by 0.5 dB in tension and −1.3 dB in compression as seen in Fig. 4(a). It must be noted that while the CDS circuit effectively removes the low-frequency drift depending on its switching frequency, it may additionally filter small variations in pH changes recorded over an extended period of time. However, the ability of the chip to be programmed externally coupled with the CDS circuit can be utilised to perform stable measurements. Furthermore,

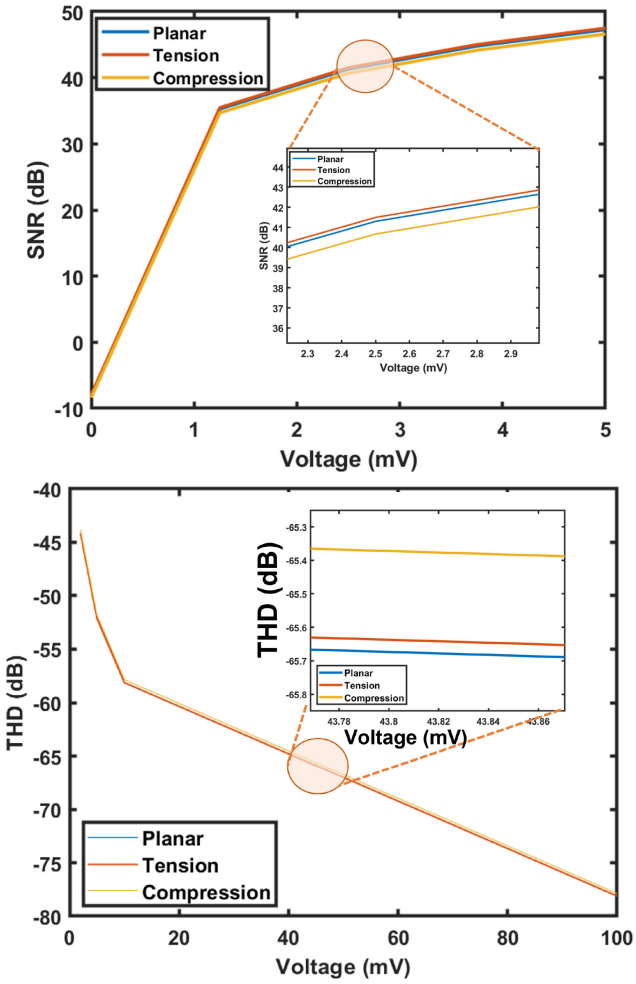

Fig. 4. Simulated (a) SNR and (b) THD of transmission gate versus input voltage under no stress (planar), and tensile and compressive stress.

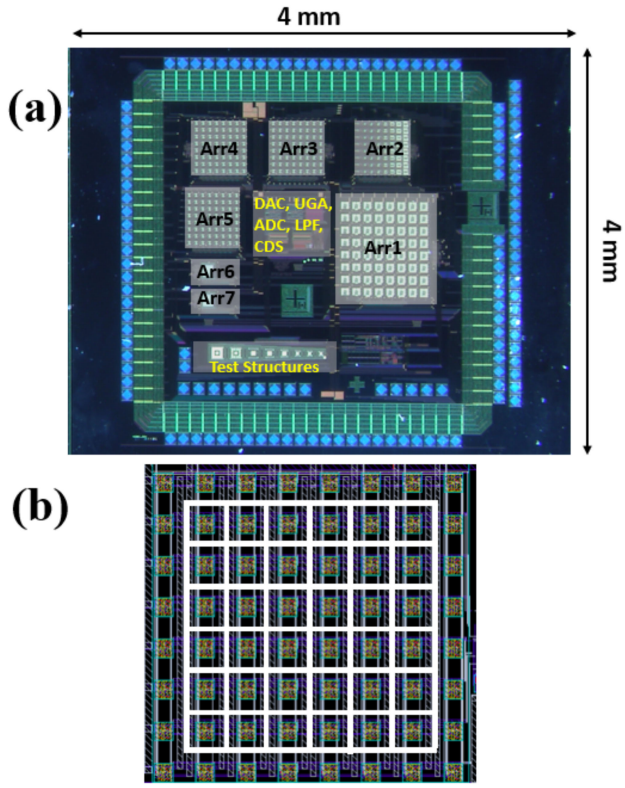

Fig. 5. (a) Chip micrograph of 8 × 8 ISFET pixel arrays along with read-out circuitry, buffers, ADC, DAC and drift compensation architectures (b) Layout of a single array consisting of 8 × 8 ISFET pixel circuits with gap for reference electrode deposition shown in white.

reactions leading to pH variations occur at comparatively higher frequencies of 0.1–1 Hz as compared to drift, which further enhances the effectiveness of the CDS circuit [36].

At the final stage a second-order Gm-C bi-quad is used to filter the output of the circuit which is subsequently digitised at 90 kS/s via a 10 bit SAR ADC. In order to remove kickback at the beginning of acquisition due to charge rebalancing on the converter, a second folded cascode buffer is used. The micrograph of the chip fabricated in Austria Microsystems (AMS) 350 nm CMOS technology is shown in Fig. 5(a). The chip has been designed with a pixel pitch of 40 µm wherein on-chip reference electrodes can be deposited on the CMOS chip as shown in Fig. 5(b).

III. Multiphysics Numerical Simulation of ISFETs

A. Electrochemical Simulations

In order to evaluate the response of the ISFET M_c4 (Fig. 1(b)) to surrounding media, we used *the Electrochemistry Module* of COMSOL Multiphysics v5.6. This study builds upon our previous analytical work on ion sensitive RuO_2 membranes [24]. This implementation has been carried out by considering the ionic composition of DMEM (11995, ThermoFisher Scientific) for robustness and includes the presence of sodium chloride (110.34 mM) and sodium bicarbonate (44.04 mM) molecules which respond to electric fields in the media at room temperature. It may be noted that crowding effects in the system have been neglected and the Boltzmann model is applicable. This assumption is suitable in this study since the electrolyte under consideration is not highly concentrated and the surface of the silicon nitride layer forms a buffering interface with the surrounding media. Silicon nitride consists of two primary binding sites, namely silanol and primary amine. Eq. 7 describes the variable surface charge density on the silicon nitride surface [37].

$$\sigma_{nit} = N_{si}\left(\frac{[H_s^+]^2 - K_+K_-}{[H_s^+]^2 + K_+[H_s^+] + K_+K_-}\right) + N_{ni}\left(\frac{[H_s^+]}{[H_s^+] + K_{N+}}\right) \quad (7)$$

The constants N_{si} and N_{ni} in Eq. 7 denote the surface densities of the silanol and amine sites respectively while K_i denote the dissociation constants of the sites. The activity of the hydrogen ions at the surface of the sensing layer is denoted by $[H_s^+]$ and is a function of the nitride surface potential. The schematic of the 2D model with a dielectric and out-of-plane thickness of 24 μm and 2 μm ($t_1 = t_2 = 1$ μm), respectively is shown in Fig. 6. For better accuracy of the model, very fine boundary sub-nm mesh elements have been used at the interface of the electrolyte and the

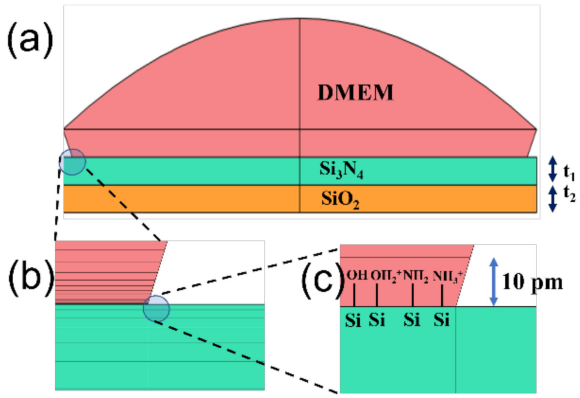

Fig. 6. (a) Schematic of ion-sensitive dielectric stack and DMEM. (b) Boundary layered mesh at interface. (c) First mesh boundary height is 10 pm.

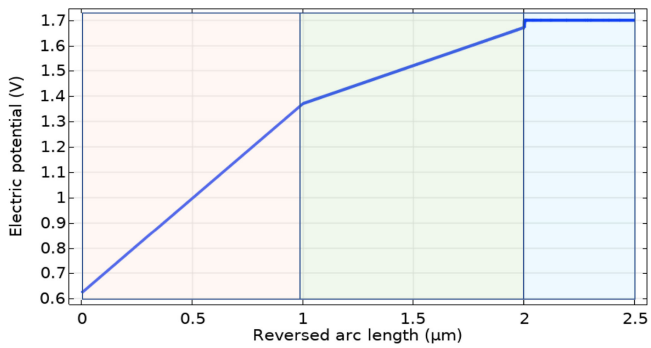

Fig. 7. Potential drop across the ISFET (blue: potential of bulk electrolyte and interface drop, green: potential drop in the nitride layer up to oxide layer, orange: potential drop in the oxide layer up to the floating gate).

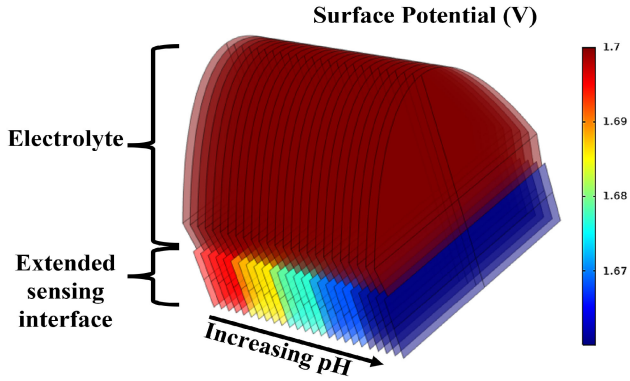

Fig. 8. Surface potential of sensing interface versus pH varying from 5 to 9 (sensing interface is extended for visual clarity).

sensor. The first mesh boundary height into the electrolyte was chosen to be in the same order of magnitude as the ionic radius of hydrogen ion in order to efficiently capture the dynamics of the system. From therein, a geometric progression was utilised on the mesh into the electrolyte solution thus ensuring a high mesh density. This ensures accurate computations at the double layer interface and takes into account complete wetting of the surface, similar to our experimental setup. Biasing of the ISFET has been numerically carried out using the *Electrostatics* physics with a user-defined bulk potential (V_{ref}). The surface charge density, σ_{nit}, is defined across the entire electrolyte-insulator interface boundary. The migration of ions on application of electric fields is modelled using *Transport of Dilute Species* (TDS) physics with bulk ionic concentration defined on the basis of pH and DMEM composition. Multiphysics coupling between the electrostatics and TDS modules ensures the correct derivation of voltage drop across the Stern layer and pH dependent surface potential using the Poisson-Nernst- Planck equation. User-defined differential equations are used to numerically derive the surface potential with an appropriate initial value. The potential computed in the first electrostatics step, ϕ_l, is coupled to the surface potential of the sensing membrane, ϕ_N, via Eq. 8.

$$\phi_N = \phi_l + \frac{D_n}{C_{stern}} \tag{8}$$

The presence of the Stern layer, of which the capacitance is denoted by C_{stern}, entails continuity in the normal component of the electric displacement field, D_n. The latter is computed in the electrostatics physics and fully coupled to the differential equation describing the potential developed on the nitride layer after deviations from electroneutrality. The initial value of the surface potential is taken as the applied bulk potential. Eq. 8 can be further expanded to take into account static as well as dynamic drift in the system via Eq. 9. In our numerical studies we have assumed near-zero drift so as to not deviate from the assumptions of quasi-equilibrium studies i.e., the damping coefficients, a_1 and a_2 are zero.

$$\phi_N = \phi_l + \frac{D_n}{C_{stern}} - a_1\frac{\partial^2\phi_N}{\partial t^2} - a_2\frac{\partial\phi_N}{\partial t} \tag{9}$$

The drop in potential across the interface, the dielectric stack and the floating gate with a reference voltage of 1.7 V and pH equal to 7.5 is shown in Fig. 7. This drop occurs due to the presence of the passivation capacitance, double layer capacitance as well as the transistor-introduced capacitive division due to oxide and depletion capacitances. It is important to take into account this potential drop as it is coupled to the voltage seen by the floating gate of the transistor. Furthermore, the surface potential of the nitride layer is dependent on the pH as shown in Fig. 8, wherein acidic solutions exhibit a higher potential at the interface. The results of the electrochemical study are then coupled to the semiconducting physics as is explained in the following sub-section.

B. Semiconductor Simulations

With the aim of efficient modelling the semiconducting aspects of the ISFET, device model parameters obtained from 350 nm CMOS technology are incorporated into the COMSOL framework, which are also utilised during chip design. Transistor M_c4 (Fig. 1(b)) is separately biased at $V_{DS} = 1$ V with a sweep on V_{ref} from 1.7 V to 2 V and its drain current is recorded experimentally via a source measuring unit. The experimental gate voltage corresponds to the externally probed reference voltage, V_{ref}. To test the applicability of the numerical model, the same biasing conditions are chosen during simulations. The

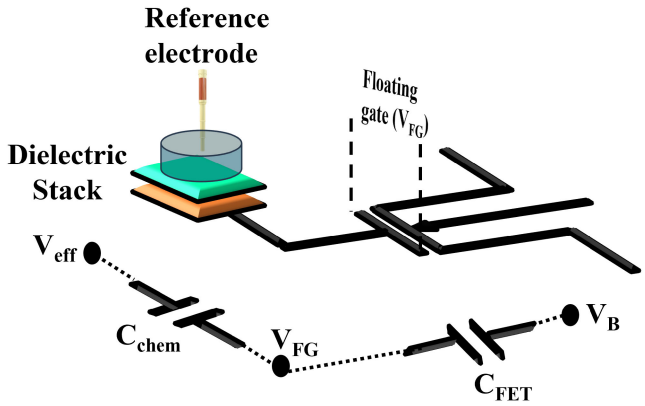

Fig. 9. Capacitive division in ISFET due to dielectric stack and FET capacitance. The body voltage, V_B, is set to zero.

capacitive division occurring at the floating gate of the ISFET is shown in Fig. 9. The floating gate voltage, V_{FG} is given by Eq. 10 at $V_B = 0$. The variable V_{eff} takes into account the applied reference voltage as well as the pH dependent chemical potential V_{chem} [38].

$$V_{FG} = V_{eff} \frac{C_{chem}}{C_{chem} + C_{FET}} \tag{10}$$

The electrochemical capacitance, C_{chem}, is a function of the sensing layer properties and depends on the Stern layer capacitance comprising the inner and outer Helmholtz layer capacitances, the diffuse layer capacitance as well as the drop within the dielectric stack which are computed in the electrochemistry physics. In addition to the capacitance of the sensing aspect of the ISFET, the transistor contributes an additional capacitance, $C_{FET,}$ which can be expressed as a function of the oxide capacitance, C_{ox} and depletion capacitance C_{dep} as seen in Eq. 11.

$$C_{FET} = \frac{C_{ox} C_{dep}}{C_{ox} + C_{dep}} \tag{11}$$

Furthermore, scattering and lateral electric fields in the channel are taken into account via field-dependent mobility variations. The designed channel length of the device is 500 nm across which a drain-source voltage of 1V is applied. Due to the effect of the lateral electric field as well as scattering, four semiconductor material models are taken into account: Arora, Fletcher, Lombardi and Caughey-Thomas mobility models, in the mentioned order [39], [40]. It must be noted that the efficiency of the study relies on the order in which the mobility models are defined. Hence, an effective nested mobility is defined wherein the input mobility of each model is the computed mobility of the previous model. This approach is particularly useful in simulating transistors fabricated on piezoresistive materials due to the inclusion of mobility variations occurring due to external stresses during UTC bending.

A complete simulation linking the electrochemical and semiconducting physics is performed and the drain current is derived as a function of the reference voltage taking into account capacitive division as well as channel response at V_{DS} equal to 1V at pH equal to 7.5. Furthermore, the change in the surface potential of the sensor is derived as a function of pH. In continuum with the electrochemical-semiconducting analysis, this model can be further expanded to efficiently analyse the effects of strain on the ISFET via coupling with the *Solid Mechanics* physics.

This approach is particularly useful in the design of sensors on anisotropic materials such as Si, which exhibit variable mobilities along different crystal directions in the planar as well as strained state. The simulation results of this model are compared with that of the experimental in Section 4b. The device behaviour can then be extracted and coupled in Verilog-A to systematically predict system level performance of ISFETs utilising high-k dielectrics, 2D materials as well as non-planar devices such as gate-all-around ISFETs.

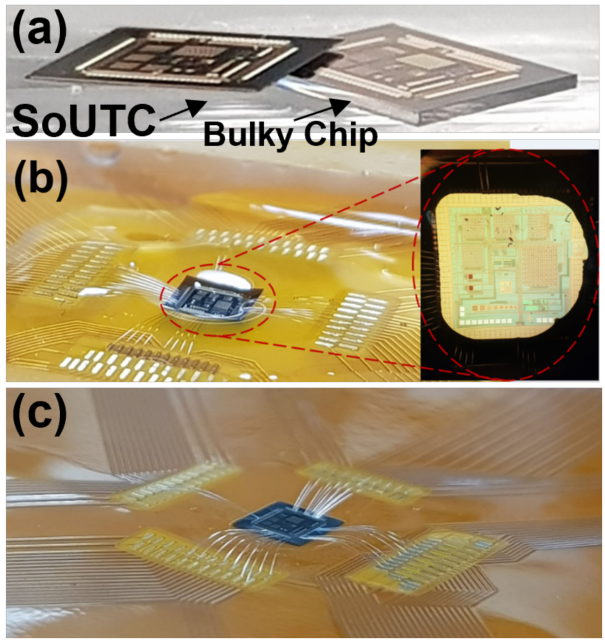

Fig. 10. (a) Ultra-thin and bulky chips. (b) UTC on the flexible PCB followed by epoxy encapsulation. (c) UTC ball bonded on the flexible PCB without epoxy encapsulation.

IV. Fabrication and Experimental Results

A. System-on-Ultra-Thin-Chip (SoUTC)

The fabricated chip with a thickness of ~250 μm is thinned to ~30 μm using in-house processing involving lapping [24], [41]. Lapping, unlike mechanical exfoliation, exhibits low to negligible affects on the leakage current of devices with substrates thinned down to thickness larger than that of the electrical channel and is often used by the optoelectronics industry wherein a high degree of precision is required [41]. Backside chip thinning was carried out using the PM5 Logitech precision lapping and polishing machine. The chips were attached to the sample holding jig by bonding wax of ~1 μm thickness. Slurried aluminium oxide particles of diameter ~3 μm were utilised to physically etch away the chip at the rate of 9 μm/min. Once the desired chip thickness was achieved, the bonding wax was melted and the chips were slid out using a PDMS stamp as shown in Fig. 10(a).

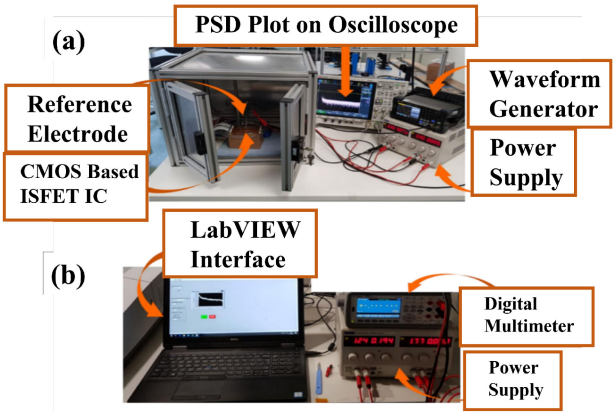

Fig. 11. (a) Electrical setup for PSD measurements. (b) Electrochemical interfacing for extraction of pH and drift.

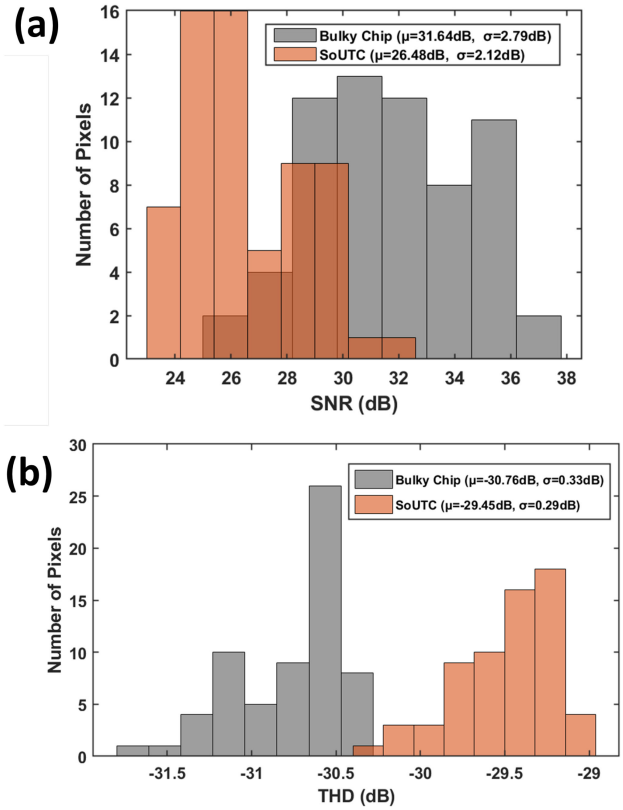

Fig. 12. Array level measurements of (a) SNR and (b) THD of CMOS ISFET chip before and after thinning.

Due to the stacked nature of FETs, which consists of layer made of unequal stiffness materials such poly-Si, dielectrics and metals, the thinning process is likely to induce a non-zero radius of curvature in the chip which causes the chip to become inherently non-planar. The maximum radius of curvature of the IC under no force is 2 μm as measured using profilometry. After thinning, the chip was glued with low stress epoxy (Epo-TEK 301-2) and wire bonded to a polyamide based flexible PCB (FPCB) with the pads encapsulated in room temperate cured epoxy (Epo-TEK 302-3M) as shown in Fig. 10(b). The ball bonding of the UTC without epoxy is shown in Fig. 10(c). As the the UTCs obtained through this post-processiog step can bend and conform to curved surfaces such as the skin, they are likely to lead to improved recording of data related to body fluid pH.

B. Experimental Results

The electrical and electrochemical characterization of bulky ICs and UTCs was carried out in a Faraday cage using DMEM solutions of volume 50 μL having a pH in the range of 5–9 as shown in Fig. 11(a) and (b), respectively. DMEM is a standard solution, of which the chemical content closely resembles biological fluids [42]. The solution consists of amino acids, glucose, vitamins and inorganic salts [42]. This pH range is used as it mimics the body fluid make-up. Additionally, the power spectral density of each pixel was computed via FFT of recorded signals on an oscilloscope (MSO-X, 4154A) with a sampling rate of 5GSa/s. The reference voltage of each pixel was biased using an Ag/AgCl (3M KCl) electrode (MF-2056, Alvatek) connected to an arbitrary waveform generator (T3AFG120 from Teledyne LeCroy) providing a small-signal input voltage of amplitude 10mV$_{\text{p-p}}$ at 1 kHz as shown in Fig. 11(a). The obtained PSD plots are in-turn utilised to compute the SNR and THD of each pixel circuit of which the results are shown in Fig. 12(a) and Fig. 12(b), respectively. The spread in SNR and THD can be attributed to the trapped charges present in the sensing membrane, which induce an offset in each pixel measurement. The reduction in the standard deviation of SNR after chip thinning could entail that the inherent curvature introduced in the IC resulted in bending induced enhancement reducing offset variability, which was also previously observed in our thinned extended gate ISFETs [26]. Furthermore, the THD standard deviation remained unaffected suggesting that variability in signal harmonics was unchanged after thinning.

Pixel-wise data acquisition was carried out via a digital multimeter (Keysight 34461A) and a custom LABVIEW program as shown in Fig. 11(b). Similarly, the drift was recorded over a period of 42 minutes under carefully controlled biasing conditions. The signal chain associated with drift measurement results constitutes the on-chip DAC, addressed pixel circuit, low pass filter, unity gain amplifier and the drift compensation circuit. The pH sensitivity of the "unmodified" CMOS ISFET is $\sim$10 mV/pH with a drift of 0.07 mV/min as shown in Figs. 13 and 14(a), respectively. The latter is reduced to 0.02 mV/min once the drift compensation circuit has been activated as is observed from Fig. 14(b). Furthermore, the same drift compensation circuit can be utilized to remove the offset introduced by trapped charges at the beginning of each measurement [36]. The current-mode read-out circuit is designed to be linear with a gain of unity and hence the magnitude of change in the input and output voltage can be considered approximately equal. It can be seen that the simulated results are in good agreement with experimentally derived values as shown in Figs. 15 and 16. The differences in the drain current between the predicted and derived values can be linked to the presence of buried traps and in-homogeneity of the PECVD silicon nitride layer as well as interface traps between the oxide-nitride layer.

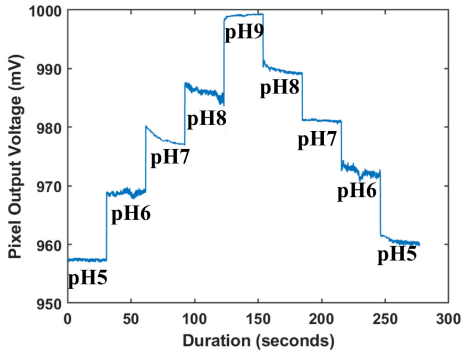

Fig. 13. Average output voltage of each pixel versus pH of surrounding DMEM solution.

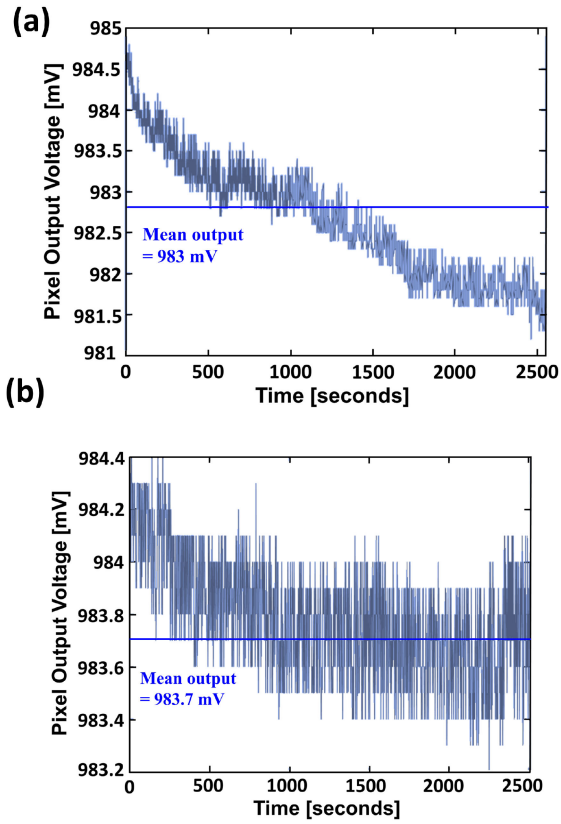

Fig. 14. Drift response of each pixel (a) without CDS active (0.07 mV/min) (b) with CDS active (0.02 mV/min).

Based on the measured noise power spectral density of the bulky and UTC chip shown in Fig. 17(a), the flicker noise spectrum of the UTC is ∼0.5–1 dB above that of the bulky chip. Similarly, thermal noise floor in the UTC was ∼1 dB higher as compared to the bulky chip. Output noise PSD of the final folded cascode unity gain amplifier on both bulky and ultra-thin chip has also been measured, wherein the amplifier load mimics the input impedance of the on-chip SAR ADC, of which the results are shown in Fig. 17(b). It is observed that variation in noise PSD of the signal chain output between the two types of chips follows an acceptable change similar to that of the active pixel circuit further confirming the suitability of ultra-thin CMOS chips for

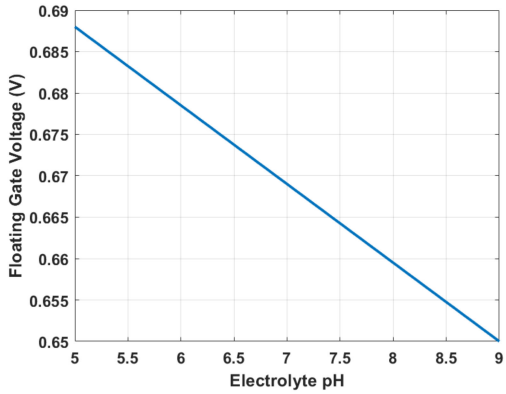

Fig. 15. Simulated floating gate voltage with a sensitivity of ∼9.8 mV/pH (experimental sensitivity is equal to ∼10 mV/pH).

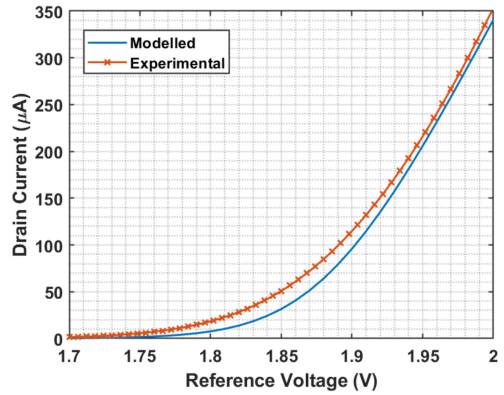

Fig. 16. Experimental and simulated ISFET drain current versus externally applied reference voltage at pH = 7.5.

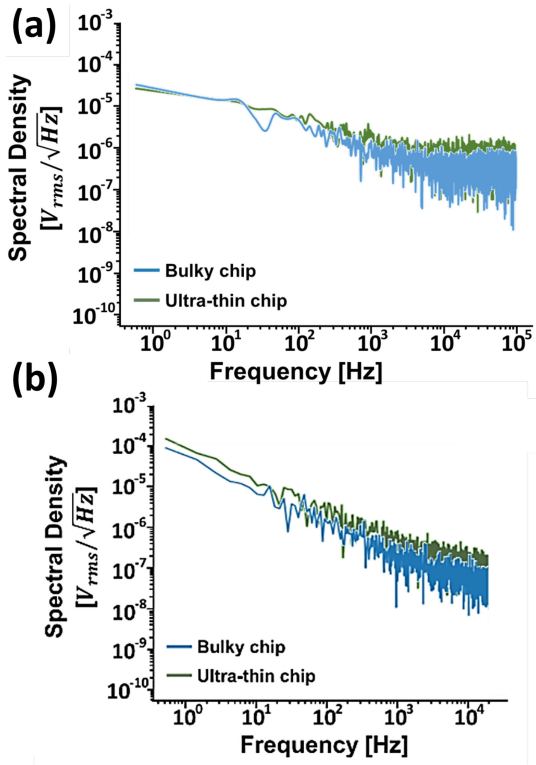

Fig. 17. Noise power spectral density of (a) current-mode pixel circuit and (b) final folded cascode unity gain amplifier on bulk and ultra-thin chip.

TABLE III
COMPARISON OF ISFET SENSING PIXELS

Parameter	This work (tested in DMEM)	[36]	[43]	[44]	[23]
Technology (μm)	0.35	0.35	0.18	0.35	0.35
Thinned CMOS IC	Yes	No	No	No	No
Power Supply (V)	2	3.3	1.8	3.3	3.3
Pixel size (μm^2)	1504.15	2500	1600	1147	50.7
Power per pixel (μW)	6.28	1.98	1190	NA	NA
Drift (mV/min)	0.07 (without CDS)/0.02 (with CDS)	1.5	3.8	6.5	9.2
SNR @ pH = 7 (dB)	31.64 (Bulky)/26.48 (SoUTC)	23.65	NA	34.16	19.9

pH sensing. The SNR and THD of each current-mode pixel has been extracted from the PSD of the output signal using an in-house algorithm developed in Python. In terms of the FoM of the circuit on UTCs, the mean SNR dropped by 5.16 dB and the THD increased by 1.31 dB as compared to bulky or conventional chips. This may have occurred due to non-uniform strain present in the UTC. However, there are no observable changes in the operation of the chip in terms of pH sensitivity and drift. Hence, the acceptable deterioration of the FoM can be neglected as compared to the advantages the UTC provides, particularly in terms of lowered stiffness, conformability, integration with flexible substrates and biological tissues as well as chip stacking. Furthermore, the piezoresistive nature of silicon can be utilized to enhance the response of the device as was indicative in the lowered variability of the FoM in the ultra-thin chips. We have compared the presented pixel circuit with existing state of-the-art CMOS ISFET pixels fabricated on bulky substrates in Table III. In terms of system power information, the power consumption division is as follows. ADC: 250 μW, DAC: 1.1 mW, CDS: 1.3 mW, LPF: 200 μW. The pixel circuit which is the core of the system, is designed for low power consumption and hence is used for a harmonious comparison. It is observed that the response of the proposed pixel circuit is comparable to that of previously reported results, with lowered power per pixel circuit, lowered drift and an ultra-thin substrate which is suitable for development of conformable high density ISFET arrays on a chip.

V. FUTURE PROSPECTS AND CONCLUSION

This paper successfully presents the design and implementation of a fully integrated pH-sensing system-on-ultra-thin chip (SoUTC) for potential use in epidermal electronics or wearable systems. An in-pixel current-mode readout topology has been used to achieve linear pH-to-current conversion and good resilience towards PVT and strain-induced variations. The 8T pixel architecture ensures proper ISFET biasing and high output impedance while the non-ideal effects of drift and strain-induced variations are compensated with a CDS architecture. The sensors

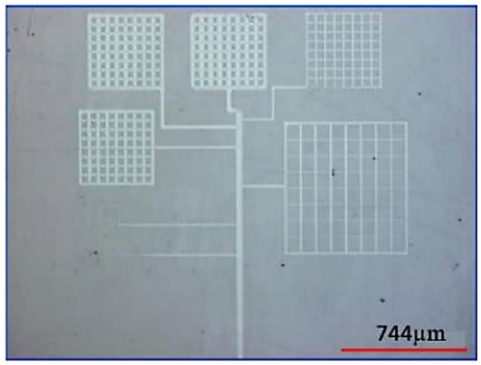

Fig. 18. Super-inkjet printed Ag/AgCl pattern on silicon nitride sensing surface for on-chip biasing of solution under test.

used in the "unmodified" CMOS format exhibit a ∼10mV/pH sensitivity towards H+ ions and a 0.07mV/minute drift in DMEM solutions, which was reduced to 0.02mV/minute with the CDS topology active. The drop in variability of the FoM across the active pixels after chip thinning is indicative of offset reduction due to inherent stresses developed in the piezoresistive silicon substrate.

In order to achieve complete flexibility, we have carried out the initial steps required for the deposition of an on-chip non-polarizable reference electrode via super inkjet printing thus removing the need for an external reference electrode as an extension to our previous study [45]. The reference electrode pattern was printed on silicon nitride membranes utilising electrohydrodynamic printing with Cyclododecene solvent (SIJTechnology, Inc.). A voltage bias of 600 V was applied to the nozzle with the substrate grounded and the printing was carried out at a frequency of 200 Hz. This step is pivotal towards the packaging of the sensor as well as its potential use as an implantable device towards the continuation of this research. An additional advantage provided by printed reference electrodes for CMOS ISFETs is their pixel-like compartmentalization. This leads to localized biasing of the electrolyte thus further reducing the effect of trapped charges [46]. The printed Ag/AgCl pattern on Silicon Nitride is shown in Fig. 18 comprising of the split-array format of the chip with seven 8 × 8 arrays with a minimum line width of 25 μm. In order, to prevent short circuits between the electrolyte and the bonded wires during bending, polymeric chambers will be deposited on the chip via high precision printing of flexible and biocompatible materials. Based on design specifications the effects of strain on the overall SoUTC can be minimized by placing the chip in the neutral plane during packaging.

The presented in-depth numerical analysis of the ISFET taking into account electrolyte composition as well as mobility variations in the transistor provides an efficient method for gauging the response of designed ISFETs prior to fabrication and provides further insight into potential drops occurring as a result of the fabrication process. The electrical and electrochemical performance of the in-pixel topology on UTCs (∼30 μm thick) was compared with the same topology on bulky (∼250 μm) chips and an acceptable degradation of the SNR and THD in the

readout circuit on the ultra-thin die was observed. Additionally, numerical results provide an adequate modelling framework capable of predicting variations in the surface potential of the sensor as well as drain current of the transistor under varying pH conditions. The presented SoUTC paves the way towards the next generation of wearable point-of-care devices.

REFERENCES

[1] J. Choi, R. Ghaffari, L. B. Baker, and J. A. Rogers, "Skin-interfaced systems for sweat collection and analytics," *Sci. Adv.*, vol. 4, no. 2, 2018, Art. no. eaar3921.

[2] L. Manjakkal, W. Dang, N. Yogeswaran, and R. Dahiya, "Textile-based potentiometric electrochemical pH sensor for wearable applications," *Biosensors*, vol. 9, pp. 1–12, Art. no. 14, 2019, doi: 10.3390/bios9010014.

[3] D.-H. Kim *et al.*, "Epidermal electronics," *Science*, vol. 333, no. 6044, pp. 838–843, 2011.

[4] R. Dahiya *et al.*, "Large-area soft e-skin: The challenges beyond sensor designs," *Proc. IEEE*, vol. 107, no. 10, pp. 2016–2033, Oct. 2019.

[5] S. P. Lee *et al.*, "Highly flexible, wearable, and disposable cardiac biosensors for remote and ambulatory monitoring," *NPJ Digit. Med.*, vol. 1, no. 1, pp. 1–8, 2018.

[6] M. Rothmaier, B. Selm, S. Spichtig, D. Haensse, and M. Wolf, "Photonic textiles for pulse oximetry," *Opt. Exp.*, vol. 16, no. 17, pp. 12973–12986, 2008.

[7] K. Meng *et al.*, "Flexible weaving constructed self-powered pressure sensor enabling continuous diagnosis of cardiovascular disease and measurement of cuffless blood pressure," *Adv. Funct. Mater.*, vol. 29, no. 5, 2019, Art. no. 1806388.

[8] Z. Liu *et al.*, "Flexible piezoelectric nanogenerator in wearable self-powered active sensor for respiration and healthcare monitoring," *Semicond. Sci. Technol.*, vol. 32, no. 6, 2017, Art. no. 064004.

[9] Y. Cha, K. Nam, and D. Kim, "Patient posture monitoring system based on flexible sensors," *Sensors*, vol. 17, no. 3, Art. no. 584, 2017.

[10] M. Bhattacharjee, M. Soni, P. Escobedo, and R. Dahiya, "PEDOT: PSS microchannel-based highly sensitive stretchable strain sensor," *Adv. Electron. Mater.*, vol. 6, Art. no. 2000445, 2020.

[11] B. W. An, S. Heo, S. Ji, F. Bien, and J.-U. Park, "Transparent and flexible fingerprint sensor array with multiplexed detection of tactile pressure and skin temperature," *Nat. Commun.*, vol. 9, no. 1, pp. 1–10, 2018.

[12] M. Soni, M. Bhattacharjee, M. Ntagios, and R. Dahiya, "Printed temperature sensor based on PEDOT: PSS-Graphene oxide composite," *IEEE Sensors J.*, vol. 20, no. 14, pp. 7525–7531, Jul. 2020.

[13] C. Grozea, C. D. Voinescu, and S. Fazli, "Bristle-sensors—Low-cost flexible passive dry EEG electrodes for neurofeedback and BCI applications," *J. Neural Eng.*, vol. 8, no. 2, 2011, Art. no. 025008.

[14] M. Bariya, H. Y. Y. Nyein, and A. Javey, "Wearable sweat sensors," *Nat. Electron.*, vol. 1, no. 3, pp. 160–171, 2018.

[15] W. Jia *et al.*, "Electrochemical tattoo biosensors for real-time noninvasive lactate monitoring in human perspiration," *Anal. Chem.*, vol. 85, no. 14, pp. 6553–6560, 2013.

[16] J. Kim *et al.*, "Wearable salivary uric acid mouthguard biosensor with integrated wireless electronics," *Biosens. Bioelectron.*, vol. 74, pp. 1061–1068, 2015.

[17] W. Dang, L. Manjakkal, W. T. Navaraj, L. Lorenzelli, V. Vinciguerra, and R. Dahiya, "Stretchable wireless system for sweat pH monitoring," *Biosens. Bioelectron.*, vol. 107, pp. 192–202, 2018.

[18] W. Gao *et al.*, "Fully integrated wearable sensor arrays for multiplexed in situ perspiration analysis," *Nature*, vol. 529, no. 7587, pp. 509–514, 2016.

[19] J. Kim *et al.*, "Noninvasive alcohol monitoring using a wearable tattoo-based iontophoretic-biosensing system," *ACS Sensors*, vol. 1, no. 8, pp. 1011–1019, 2016.

[20] D. P. Rose *et al.*, "Adhesive RFID sensor patch for monitoring of sweat electrolytes," *IEEE Trans. Biomed. Eng*, vol. 62, no. 6, pp. 1457–1465, Jun. 2015.

[21] J. Bausells, J. Carrabina, A. Errachid, and A. Merlos, "Ion-sensitive field-effect transistors fabricated in a commercial CMOS technology," *Sensors Actuators B: Chem.*, vol. 57, no. 1–3, pp. 56–62, 1999.

[22] B. Merriman, I. T. D. Team, and J. M. Rothberg, "Progress in ion torrent semiconductor chip based sequencing," *Electrophoresis*, vol. 33, no. 23, pp. 3397–3417, 2012.

[23] N. Miscourides, L. Yu, J. Rodriguez-Manzano, and P. Georgiou, "A 12.8 k current-mode velocity-saturation ISFET array for on-chip real-time DNA detection," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 5, pp. 1202–1214, Oct. 2018.

[24] M. Douthwaite, E. Koutsos, D. C. Yates, P. D. Mitcheson, and P. Georgiou, "A thermally powered ISFET array for on-body pH measurement," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 6, pp. 1324–1334, Dec. 2017.

[25] S. Gupta, W. T. Navaraj, L. Lorenzelli, and R. Dahiya, "Ultra-thin chips for high-performance flexible electronics," *NPJ Flexible Electron.*, vol. 2, no. 1, Art. no. 8, 2018, doi: 10.1038/s41528-018-0021-5.

[26] A. Vilouras *et al.*, "Ultra-thin ion-sensitive field-effect transistors chips with bending induced performance enhancement," *ACS Appl. Electron. Mater.*, vol. 2, no. 8, pp. 2601–2610, 2020.

[27] A. S. Dahiya *et al.*, "High-performance printed electronics based on inorganic semiconducting nano to chip scale structures," *Nano Convergence*, vol. 7, no. 1, pp. 1–25, 2020.

[28] H. Heidari, N. Wacker, and R. Dahiya, "Bending induced electrical response variations in ultra-thin flexible chips and device modeling," *Appl. Phys. Rev.*, vol. 4, no. 3, 2017, Art. no. 031101.

[29] A. Vilouras, H. Heidari, S. Gupta, and R. Dahiya, "Modeling of CMOS devices and circuits on flexible ultrathin chips," *IEEE Trans. Electron Dev.*, vol. 64, no. 5, pp. 2038–2046, May 2017.

[30] J. N. Burghartz, W. Appel, C. Harendt, H. Rempp, H. Richter, and M. Zimmermann, "Ultra-thin chip technology and applications, a new paradigm in silicon technology," *Solid-State Electron.*, vol. 54, no. 9, pp. 818–829, 2010.

[31] L. Yu-Min *et al.*, "A novel 3D IC assembly process for ultra-thin chip stacking," in *Proc. Int. Conf. Electron. Packag.*, Apr. 23-25, 2014, pp. 470–474, doi: 10.1109/ICEP.2014.6826723.

[32] A. Vilouras and R. Dahiya, "Ultra-Thin chips with current-mode ISFET array for continuous monitoring of body fluids pH," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 22-28, 2021, pp. 1–5, doi: 10.1109/ISCAS51556.2021.9401616.

[33] A. Vilouras and R. Dahiya, "Compact model for flexible ion-sensitive field-effect transistor," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, Oct. 19-21, 2017, pp. 1–4, doi: 10.1109/BIOCAS.2017.8325217.

[34] B. Premanode, N. Silawan, and C. Toumazou, "Drift reduction in ion-sensitive FETs using correlated double sampling," *Electron. Lett.*, vol. 43, pp. 857–859, 2007, doi: 10.1049/el:20071118.

[35] D. B. Ribner and M. A. Copeland, "Design techniques for cascoded CMOS op amps with improved PSRR and common-mode input range," *IEEE J. Solid-State Circuits*, vol. 19, no. 6, pp. 919–925, Dec. 1984.

[36] Y. Hu, N. Moser, and P. Georgiou, "A 32 $\times$ 32 ISFET chemical sensing array with integrated trapped charge and gain compensation," *IEEE Sensors J .*, vol. 17, no. 16, pp. 5276–5284, Aug. 2017.

[37] J.-P. Cloarec *et al.*, "pH driven addressing of silicon nanowires onto Si3N4/SiO2micro-patterned surfaces," *Nanotechnology*, vol. 27, no. 29, 2016, Art. no. 295602.

[38] Y. Hu and P. Georgiou, "A robust ISFET pH-Measuring front-end for chemical reaction monitoring," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 2, pp. 177–185, Apr. 2014.

[39] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*, 1 ed. Vienna, Austria: Springer, 1984.

[40] "Semiconductor moduleuser's guide," AB Comsol - COMSOL, 2020. Accessed: Jan. 14, 2022. [Online]. Available: https://doc.comsol.com/5.6/doc/com.comsol.help.semicond/SemiconductorModuleUsersGuide.pdf

[41] W. T. Navaraj *et al.*, "Wafer scale transfer of ultrathin silicon chips on flexible substrates for high performance bendable systems," *Adv. Electron. Mater.*, vol. 4, no. 4, 2018, Art. no. 1700277.

[42] "Technical Resources", ThermoFisher Scientific, Accessed: Jan. 14, 2022. [Online]. Available: https://www.thermofisher.com/uk/en/home/technical-resources/media-formulation.171.html

[43] M. Cacho-Soblechero, K. Malpartida-Cardenas, C. Cicatiello, J. Rodriguez-Manzano, and P. Georgiou, "A dual-sensing thermo-chemical ISFET array for DNA-Based diagnostics," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 3, pp. 477–489, Jun. 2020.

[44] N. Moser, J. Rodriguez-Manzano, T. S. Lande, and P. Georgiou, "A scalable ISFET sensing and memory array with sensor auto-calibration for on-chip real-time DNA detection," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 2, pp. 390–401, Apr. 2018.

[45] L. Manjakkal, A. Vilouras, and R. Dahiya, "Screen printed thick film reference electrodes for electrochemical sensing," *IEEE Sensors J.*, vol. 18, no. 19, pp. 7779–7785, Oct. 2018.

[46] N. Miscourides and P. Georgiou, "Calibrating for trapped charge in large-scale ISFET arrays," *IEEE Sensors J.*, vol. 20, no. 10, pp. 5110–5118, May 2020.

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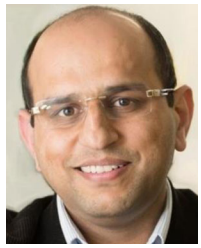

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