Hybrid Power Divider and Combiner for Passive RFID Tag Wireless Energy Harvesting

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ABSTRACT This paper presents three- and five-ports radio frequency (RF) hybrid power divider combiner (HPDC) designs with multiband characteristics operating at 2.4 GHz (ISM, IEEE 802.11b,g); 5.8 GHz (IEEE 802.11n, a and 802.11ac); and 6 GHz (IEEE 802.11ax) wireless standards for energy-efficient 5G-enabled passive Internet of Things (IoT) sensors; energy harvesting (E.H); passive radio frequency identification (RFID) tags; multiple-input multiple-output (MIMO) antenna beamforming; and data communication applications spanning DC to the 6-GHz frequency range. The presented HPDC designs operate at a centre-design frequency of 3 GHz on a Rogers RO4350 substrate. The designed novel HPDC demonstrates a good match between the ports, high isolation between the output ports, and equal power distribution between the output ports. Furthermore, the obtained return and isolation losses are less than -10 dB for the Wi-Fi 6E standards. The reported findings hold an excellent promise for RF energy harvesting and utilisation, adaptive intelligent energy-efficient data communication, and seamless ubiquitous satellite-cellular convergence connectivity applications.

INDEX TERMS 5G communication, energy harvesting, power divider and combiner, passive RFID tags, Wi-Fi, satellite.

I. INTRODUCTION

The Internet of Things (IoT) ecosystem represents the third phase of the internet revolution that advances use cases and applications in smart homes, industrial automation, intelligent energy, connected car, smart city, and wearables. The advancements in wireless systems are an integral part of the intelligent application based on the IoTs technology. IoTs connections are predicted to grow from 7.7 billion in 2019 to 25.4 billion in 2030 [1]. 41.6 billion IoTs devices generating 80 Zettabytes of data are estimated to put mobile operators at a critical juncture by 2025. The fifth generation (5G) radio access network (RAN) ecosystem promises to enable improved bandwidth and open RAN performance metrics for massive IoTs deployments spanning national coverage (low frequency bands e.g., 700 MHz); city coverage (sub-6 GHz band i.e., $3.5 - 7$ GHz), and megacity hotspots (mmWave bands i.e., $24 - 100$ GHz). Within the context

of wireless radio frequency energy harvesting (RF-EH), the 5G network will house massive IoTs [low-cost devices, battery/batteryless operated; small data volumes; and massive numbers (many millions)]; broadband IoTs (high throughput; low latency; and large data volume); and critical IoTs (high reliability; very low latency; and very high availability). With potential disparate IoTs solutions in view, developing low-power RF transceiver subsystems with a RFEH capability promises to provide flexibility, adaptability, and control for satellite-cellular convergence connectivity applications.

Wireless devices require rechargeable energy subsystems to maintain operational stability throughout their lifecycles. The commonly used method to power such devices are battery sources, and they constitute a major design consideration in terms of capacity, form factor, and lifespan. Moreover, the disposal of batteries leads to environmental pollution during its discarding stage. To overcome these challenges, energy harvesting (EH) has emerged as a promising solution that is much greener and more sustainable. EH involves converting other forms of energy (in the environment such as thermal

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energy, solar energy, vibration energy, and propagating RF signals) into green electrical energy [2]–[4]. Though solar energy is the most abundant source in nature, this may fall off due to its intermittent supply. EH is the most convenient alternative that provides controllable, predictable, and constant energy transfer over a distance [5]. The information and a tiny amount of power are delivered to the environment through a wireless RF signal.

The transmitted power could be harvested and converted into cheap green energy to feed various low-power electronic circuits such as wireless sensor networks (WSNs). Although the harvested energy could be small in the order of milliwatt (mW), it can provide enough power to WSNs and other low-power applications. Therefore, EH can reduce the environmental impact of waste batteries and the high maintenance costs of replacing them. In RF-EH, radio signals with a frequency varying from 300 GHz to as small as 3 kHz are used as a medium to carry energy in the form of electromagnetic (EM) radiation [6]. The R'F energy can be harvested from transmitted unlicensed frequency bands such as 868 MHz, 915 MHz, 2.4 GHz and 5.8 GHz [7].

The fifth-generation (5G) wireless radio access technology (RAT) promises 100 times the average consumer data rate and 1000 times more cellular data rate per area with less than 1 ms latency compared with the 4G [8]. Consequently, there is a massive increase in mobile phone subscribers, mobile base stations (BS), and wirelessly connected devices utilising Bluetooth, ZigBee, Wi-Fi, and GPS (global positioning system) with a high demand for data. Besides, the users demand more energy-consuming features including web browsing, emails, massive machine-to-machine (M2M) communication, gaming, video browsing, and IoTs applications with an extended battery life. These expanding large-scale wireless network devices require enormous electrical power for multimode raw and processed data communication operations. Mobile BS; television broadcasting stations; radio BS; wireless LAN transmitters (Wi-Fi Routers); wirelessly connected devices; satellites; and mobile devices are the radio wave sources for RF-WEH. Therefore, a more efficient, healthier, and environmentally friendly solution with zero carbon footprints (CO_2 emission) is needed to extract energy from the atmosphere – which offers nearly infinite energy resources to wireless devices and can eliminate batteries.

The motivation to utilize green energy from the surrounding has propelled global wireless power transfer (WPT) through propagating EM radiation research interests. WPT can be carried out through solid inductive coupling and magnetic resonant coupling with specified near-field regions [9]. The near-field WEH technique involves additional switches, conductors, or inductors which change the inductive power transfer (IPT) characteristics and decrease the efficiency [10]. However, the far-field transition faces unique challenges in improving its conversion efficiency [5]. To overcome these challenges, a novel RF *N*-way multi-antenna, multi-radio standards WEH system has been designed (Fig. 1) thus:
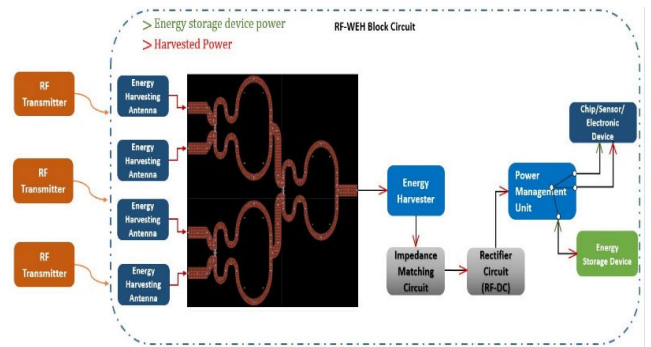

FIGURE 1. A 4-way multi-antenna WEH block circuit diagram.

a) Multiband, multiple RF EH antennas;
b) A 5-port RF hybrid power combiner (HPC) to combine the harvested RF energy has been designed (Fig. 1);
c) An energy harvester consisting of an impedance matching circuitry and a rectifying circuit for RF to DC conversion;
d) A power management unit (PMU) to deliver the DC current to meet the power requirements of the connected electronic device; and
e) An energy storage device (ESD) (i.e., supercapacitors/ultracapacitors) to store the surplus power.

Furthermore, the RF-WEH block circuit (Fig. 1) operates at three different modes, viz:

a) Hybrid power generation, and storage (HPGS) mode;
b) Hybrid power generation, and extraction (HPGE) mode; and
c) Power generation (PG) mode.

The PMU utilizes the power budget information of the RF subsystem to decide on the hybrid power mode (HPGS or HPGE) to deploy. When the received RF signal by EH antennas is strong, the RF-WEH block circuit operates at HPGS mode. The operation of the HPGS mode is as follows:

a) The RF power is harvested from the surrounding environment;
b) The PMU calculates the total amount of power received by the rectifying circuit;
c) The harvested power is delivered to the connected electronic device/load according to the voltage requirements; and
d) The excess energy is stored in the ESD (i.e., supercapacitors/ultracapacitors).

Similarly, in the case of a weak signal strength, the RF-WEH block switches to the HPGE mode. The operation of HPGE mode is as follows:

a) The harvested power will be small and cannot meet the operating voltage of the connected electronic device/load;
b) The HPG chip delivers the harvested power to the electronic device/load; and

c) The HPG chip extracts the remaining power from ESD (i.e., supercapacitors/ultracapacitors) by utilising PMU and delivers it to the connected electronic device.

Furthermore, the RF-WEH will switch to the PG mode when the connected electronic device is in a sleep mode. In this mode, it will harvest power from the environment and store it in the ESD. The PMU utilizes the power budget information of the RF subsystem to decide on the hybrid power mode (HPGS or HPGE) to deploy. Moreover, the programmed operational times of the IoTs subsystems (including signal transmission, reception, data processing and energy storage regimes) will incorporate the active and passive (sleep) modes of the device. A switching IC (i.e., SN74LVC2G157DCTR – a single two-line to one-line data selector multiplexer) will be utilised with the purpose to send signal to PMU in the actual use case deployment. If the connected electronic device/IC will be in a sleep mode, the switching IC will send a signal to the PMU.

In this paper, novel 3- and 5-ports RF-HPDC designs are presented. The HPDC promises multiband characteristics and reduced size at the Wi-Fi 6E frequency bands (2.4 GHz, 5.8 GHz, and 6.0 GHz). The proposed HPDC can be realized within a sensitive channel-aware monolithic microwave integrated circuit (MMIC) low-noise amplifier for adaptive satellite-cellular convergence applications [11], [12]. The novel research findings from the HPDC design hold a great promise for advanced capability-based reconfigurable RF transceiver and regenerative satellite transponder frontends [13]–[19]. Moreover, the HPDC is an excellent RF architecture for a hybrid beamformer development for 5G multiple input multiple output (MIMO) antenna integration. The designed 3- and 5-ports HPDC can be used for wireless communication applications operating at a 2.4 GHz frequency band. 2.4 GHz (IEE 802.11b,g), also known as the ISM band, is the most common unlicensed frequency band. It is mainly utilized for industrial, scientific and medical applications [20]. It is also used in many wireless technologies such as Bluetooth (IEEE 802.1.1), ZigBee (IEEE 802.15.4), and Wi-Fi (IEEE 802.11b and IEEE 802.11g) with 10 mW transmit power [21]. Other applications include RFID tags, WiMAX, cordless phones, car alarms, GPS, smartphones, laptops, remote sensors, tablets, actuators, TV, and microwave ovens (2.45 GHz).

Furthermore, the design of 3- and 5-ports RF-HPDC can be used for wireless communication applications utilising Wi-Fi 4 (IEEE 802.11n) frequency bands. On the other hand, the planned 3- and 5-ports RF-HPDC can be used for Wi-Fi 5 (IEEE 802.11ac) and next-generation wireless applications utilising Wi-Fi 6/6E (IEEE 802.11ax). The Wi-Fi 6/6E standard can provide up to 10 Gbps data rate speed with an extremely low latency and high capacity. It operates at 2.4 GHz, 5.8 GHz and 6 GHz frequency bands utilising multi-user (MU)-MIMO antenna configuration [22], [23].

The main contributions and/or novelties of the presented RF HPDC design include, but are not limited to,
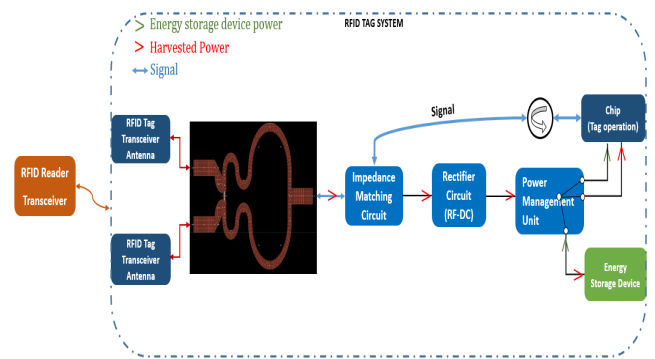

FIGURE 2. A 2-way dual antenna WEH RFID block circuit diagram.

the dynamic fractional bandwidths for RF MIMO frontend applications; reduced RF subsystem frontend form factor; multiband/multiprotocol characteristics; adaptive low-power consumption operation; multiport capabilities for high open radio access network throughput; and simultaneous digitised-analog transceiver frontend functionality.

II. RF WIRELESS ENERGY HARVESTING FOR PASSIVE RFID TAG

RFID is a wireless technology that allows two systems, a RFID reader transceiver and a RFID tag system to communicate with each other (Fig. 2). The RFID reader transceiver and the RFID tag transceiver antennas can both transmit and receive signals. Also, the RFID tag comprises a power circuit [with a matching network and a rectifying (RF-DC) circuit to achieve a stable DC voltage]; and a digital circuit (called passive IC) that communicates with the reader. The reader transmits a RF signal by utilising a RF energy transfer, resonant inductive coupling, or magnetic resonance coupling technique [24]. The most commonly used defined frequency bands for RFID technology are the low-frequency (LF) band (i.e., 125-134 kHz); high-frequency (HF) band (13.56 MHz); ultra-high-frequency (UHF) band (860-960 MHz); and microwave frequency band(2.4 GHz and 5.8 GHz) [25].

Furthermore, the RFID reader first transmits an EM field that contains power and timing information towards the tag antenna. Suppose the passive tag lies within the range of the transmitted signal, the antenna within the tag harvests both power and information from the incoming signal and generates a magnetic field. An alternating RF voltage is generated on the tag antenna and rectified by utilising the rectifying circuit (RF-DC) to energise the digital circuitry in the passive IC for tag operation [26], [27]. The reader gets information from a tag by transmitting a continuous wave (CW) RF signal to the tag [28]. When the passive IC within the tag is energised, it communicates with the reader using backscattered waves. By changing the input impedance of the passive IC connected to the tag antenna, the tag antenna can create two different backscattered waves in the reader's direction [26]. One backscattered wave corresponds to a logic 0, and the other

backscattered wave corresponds to a logic 1 [26]. Next, the tag transmits a digital signal towards the reader by utilising timing information. The reader (transceiver) antenna receives the backscattered wave with the digital information.

Although the RFID technology has been widely applied in many sectors, the progress has slowed down due to the restricted coverage area and efficiency of the system. Passive RFID tags are sensitive towards small scale fading effects, increasing the backscatter radio system [29]. As a result, the power received might not be enough to energise the digital circuit within the chip. Besides, the signal-to-noise ratio (SNR) at the reader end may be low to demodulate the collected waveform [29]. Various antenna (such as a microstrip patch) designs are suggested to increase the coverage area, efficiency, and performance of the RFID tags [30]. Multiple tag antennas have been developed to reduce tag orientation sensitivity and improve energy conversion capacity [31], [32]. To increase the sensitivity of the backscatter communication system to small scale fading effects, utilising multiple readers and tag antennas are recommended [33].

A modified RF-WEH circuit block for the RFID tag system is employed to improve the read range of the passive RFID tag (Fig. 2). The RF-WEH circuit block consists of the following components:

a) Dual tag antennas to harvest RF power transmitted by the RFID reader transceiver;

b) A 3-port power combiner to combine the energy captured by the RFID tag transceiver antennas; and

c) A PMU is linked with an impedance matching network and rectifying circuit.

Furthermore, the RF-WEH block circuit operates at three different modes known as;

a) Data collection mode (DCM);

b) Hybrid power generation and data collection (HPGDC) mode; and

c) Power generation (P.G) mode;

When the RFID tag receives a weak signal, it will operate at DCM mode. By using ESD power, extracted and delivered by PMU, the digital circuitry in the chip energises. Similarly, when the RFID tag receives a strong signal, it will switch to

HPGDC mode. The RFID tag would capture both the information and the power transmitted by the RFID reader transceiver. The chip's digital circuitry will be energised using the harvested power, and no ESD power will be supplied to the chip. When the RFID tag system is not involved in any mode, the RFID tag will switch to PGM mode. In this mode, the RFID tag will harvest the power from the surrounding environment and store it in ESD.

III. HPDC SYSTEM MODELLING

RF power combiners and splitters are passive microwave components used in various RF microwave subsystems for splitting and combining RF microwave power. A essential characteristic of a PDC includes a matched, reciprocal, and lossless network. Since all three requirements of a PDC can-

TABLE 1. Types of power divider and combiner [34].

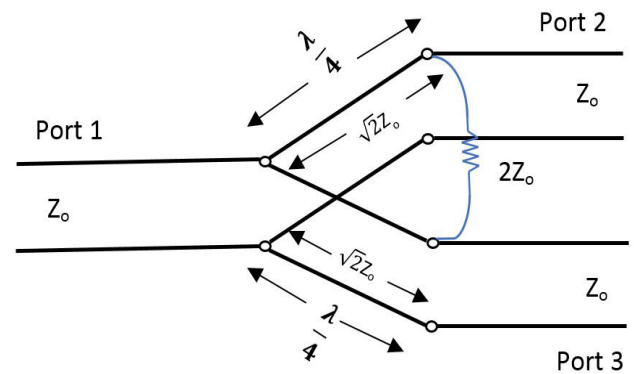| Types	Advantages	Disadvantages
T-Junction	Lossless network; and Reciprocal network;	Not matched at the output ports. No isolation between output ports.
Resistive	Matched network, and Reciprocal network;	Extra losses due to resistive components. Inadequate power management. No isolation between output ports.
Wilkinson PDC	Matched network, and Reciprocal network;	Limited bandwidth.

FIGURE 3. A conventional 3-port WPDC circuit diagram.

not be met simultaneously, one of the characteristics must be compromised to design an efficient PDC. The advantages and disadvantages of a PDC are given in Table 1.

The Wilkinson power divider and combiner (WPDC) is a matched and reciprocal network but not lossless due to an isolation resistor connected between the output ports. The basic model of a WPDC is shown in Fig. 3. If the output ports of a WPD relate to a mismatched load, an output signal reflection will occur. The reflected power from the output port would be coupled and dissipated into an isolation resistor. The only drawback of a WPDC is that it has a limited (fractional) bandwidth.

Many researchers have proposed different design structures to overcome the bandwidth limitations of the WPDC [35]–[41]. In [35]–[38], multiple sections of cascaded transmission lines and multiple sections of transmission lines with open-ended stubs are utilised at the output sections. This technique(s) utilises an increased number of isolation resistors to enhance the bandwidth and increase the circuit cost and size. In [37] and [38], multi-layer substrate designs are used. The drawback of introducing a multi-substrate layer is that the increase in the number of the substrate layer for certain printed circuit boards is inappropriate. Over a wide range, the scattering parameters of the board are not suitable. Similarly, a series/parallel setup of the RLC circuit
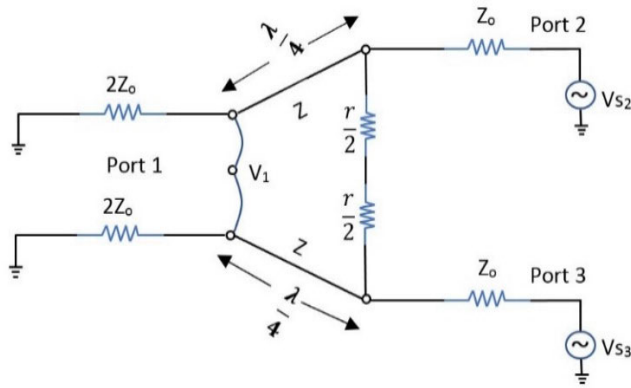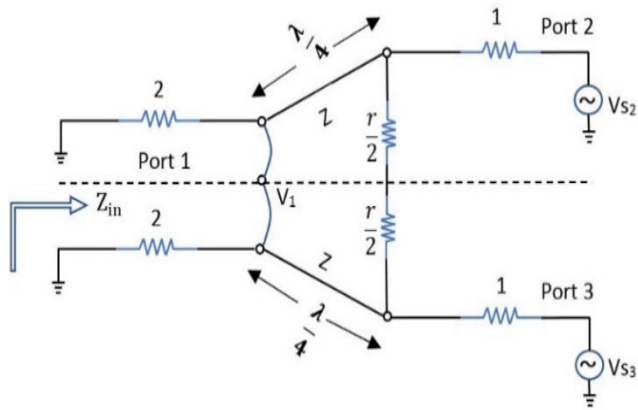
FIGURE 4. Equivalent transmission line circuit.

FIGURE 6. Transmission line circuit diagram when excited with the same magnitude and phase.

FIGURE 5. Equivalent normalized transmission line circuit.
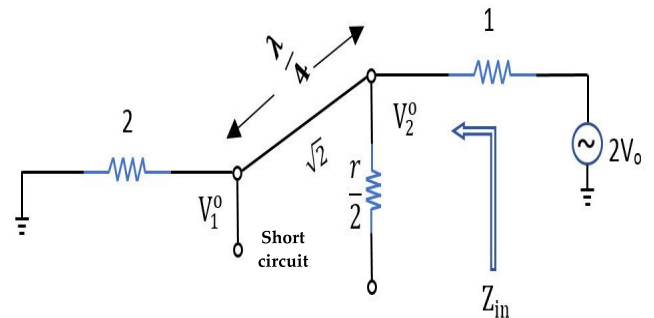
FIGURE 7. Transmission line circuit diagram when excited with the same magnitude and opposite phase.

was introduced at the output ports, which affects the efficiency of the power divider due to losses within the reactive components [41].

A. MATHEMATICAL MODELLING OF POWER DIVIDER AND COMBINER

An equal split WPDC circuit diagram is shown in Fig. 3. The characteristic impedance of the input and the output ports is Z_o. Two sections of the quarter wavelength transmission line (known as impedance transformer) with a wavelength of $\lambda/4$ are linked between the output ports. In this section, some equations will be derived to determine the characteristic impedance of the quarter wavelength section (QWS) and the isolation resistor values. A scattering matrix will be modeled accordingly that can exhibit all the characteristics of an efficient PDC. For a detailed analysis, an equivalent transmission line circuit is needed (Fig. 4). Finally, the characteristic impedance Z_O (Fig. 4) is initialised for analysis, and the equivalent transmission line circuit is shown in Fig. 5.

In sections 4 and 5, some modified designs of 3 and 5-ports HPDC will be discussed. The research findings demonstrate multiband characteristics, reduced size, matched at all ports, and equal power distribution between all ports. The EM-simulated results of the proposed designs will be charac-
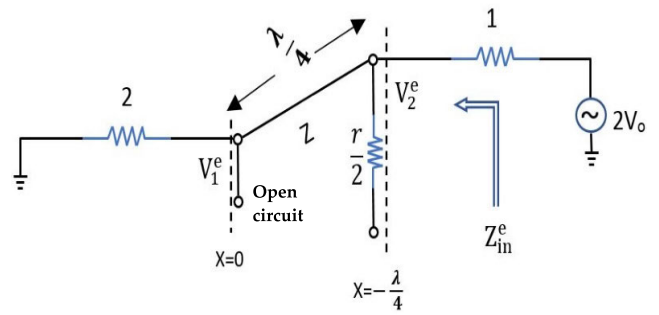
terised by utilising the modeled scattering matrix. For a mathematical modelling purpose, two different scenarios will be considered.

a) The induced voltage on ports 2 and 3 has the same magnitude and phase, i.e., $V_{S2} = V_{S3} = 2V_o$ (Fig. 4).
b) When the induced voltage on ports 2 and 3 have the same magnitude but opposite in phase, i.e., $V_{S2} = -V_{S3} = 2V_o$ (Fig. 4).

After analysing both scenarios altogether, the voltage at port 2 (V_{S2}) is $4V_o$, while the voltage at port 3 (V_{S3}) is 0. This indicates that only port 2 is energised, and the voltage at port 3 is 0. Based on voltage excitation of ports 2 and 3, there will be two different conditions (Figs. 6 and 7). As the upper and the lower parts of the circuit are the same, the circuit is divided into two parts (as indicated by dotted lines) (Fig. 5). Only one part of the circuit will be examined to determine the voltage at each point, and the calculated values for the other part(s) will be the same.

1) WHEN THE INDUCED VOLTAGE HAVE THE SAME MAGNITUDE AND PHASE

When the induced voltage on either port has the same magnitude and phase, the circuit will act as an open circuit at the bisection points (Fig. 6). The current flow will be straight, i.e., towards the load resistor, and no current will flow towards the isolation resistor. The quarter wavelength transmission line characteristic impedance (Z_o) is calculated using the equation

(equation 1). Z_{in} represents the input impedance, Z_L is the load impedance, and Z_o is the characteristic impedance. where $\beta = \frac{2\pi}{\lambda}$ and $l = \frac{\lambda}{4}$.

$$Z_{in} = Z_o \times \frac{Z_L + jZ_o \tan \beta l}{Z_o + jZ_L \tan \beta l} = \frac{Z_o^2}{Z_L} = \frac{Z^2}{2} \quad (1)$$

In the case of a matched network, the value of input impedance Z_{in} should be equal to the value of the resistor connected with the voltage source, which is 1 (Fig. 6). The calculated value of the quarter wavelength transmission line section is $\sqrt{2}$ (equation 2).

$$1 = \frac{Z^2}{2} \rightarrow Z = \sqrt{2} \quad (2)$$

By using the transmission line (equation 3), the voltages at the junction, V_2^e and V_1^e, are calculated.

$$V_x = V^+ \left(e^{-j\beta x} + \Gamma e^{-j\beta x} \right) \quad (3)$$

$$V_2^e = V(x) = V \left(-\frac{\lambda}{4} \right) = jV^+ (1 - \Gamma) \quad (4)$$

$$V_1^e = V(x) = V(0) = V^+ (1 + \Gamma) \quad (5)$$

$$\Gamma = \frac{Z_L - Z_o}{Z_L + Z_o} = \frac{2 - \sqrt{2}}{2 + \sqrt{2}} \quad (6)$$

where Γ is the reflection coefficient at load.

During an open circuit mode of operation, $V_2^e = V_o$. Hence, the voltage induced on the circuit is $2V_o$; half of the voltage will flow through V_2^e junction and the remaining voltage will reach the junction V_1^e. By inserting the value of V_2^e in equation 4, the value of V^+ is calculated (equation 7). Similarly, by inserting the value of Γ and V^+ in equation 5, the voltage at the junction V_1^e is calculated (equation 8).

$$V^+ = \frac{V_o}{j(1 - \Gamma)} \quad (7)$$

$$V_1^e = -jV_o\sqrt{2} \quad (8)$$

2) WHEN THE INDUCED VOLTAGE HAVE THE SAME MAGNITUDE AND OPPOSITE PHASE

In this scenario, there will be no flow of current across the load resistor (Z_L) (Fig. 7). The current will flow from V_2^0 junction towards the $\frac{r}{2}$ resistor to the short-circuit path and the input impedance due to the QWS ($\frac{\lambda}{4}$) is calculated as infinite (equation 9). In this case, $Z_L = 0$ because all the current flows towards the short circuit (Fig. 7). The value of input impedance, V_2^0 and V_1^0 is given in equations 10 and 11.

$$Z_{in} = \frac{Z_o^2}{Z_L} = \frac{(\sqrt{2})^2}{0} = \infty \quad (9)$$

$$V_2^0 = V_o \quad (10)$$

$$V_1^0 = 0 \quad (11)$$

In the case of a matched network, V_2^0 should be equal to the value of the resistor connected with the voltage source (i.e.,

TABLE 2. Design parameters of a 3-Port PDC.

Parameters	S-Parameters	Ideal Value	Performance Analysis
Input Return Loss	S_{11}	<-10 dB	A high absolute value indicates a good match.
Output Return Loss	S_{22} & S_{33}	<-10 dB	$S_{22} = S_{33}$ (All ports are matched)
Isolation Loss	S_{23} & S_{32}	<-20 dB	$S_{23} = S_{32}$ (All ports are Isolated)
Insertion Loss	S_{12} & S_{13}	$=-3$ dB	$S_{12} = S_{13}$ (Power is equally distributed between output ports)

$V_2^0 = 1$). The calculated value of the isolation resistor is 2 (equation 12).

$$V_2^0 = 1 = \frac{r}{2} \rightarrow r = 2 \quad (12)$$

After the detailed analysis of both scenarios, the total input impedance, Z_{in}, is calculated from equation 13 and derived by using a normalized transmission line circuit diagram (Fig. 5).

$$Z_{in} = \frac{1}{2} \times \frac{Z_o^2}{Z_L} \rightarrow Z_{in} = \frac{1}{2} \times \frac{(\sqrt{2})^2}{1} = 1 \quad (13)$$

The scattering matrix for a 3-port network having nine independent variables (also known as S-parameters) is given by:

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \quad (14)$$

As the input impedance, $Z_{in} = 1$ and the normalized value of the output ports 2 and 3 = 1 (Fig. 5), the calculated value of S_{11} (input return loss) is 0 (equation 15) and derived thus:

$$S_{11} = \frac{Z_{in} - Z_O}{Z_{in} + Z_O} = \frac{1 - 1}{1 + 1} = 0 \quad (15)$$

Since the matched condition is used to determine the total input impedance, Z_{in}, in both cases, the values of the S_{22} (output return loss) and the S_{33} (output return loss) will also be zero. Similarly, the calculated S_{12} (isolation loss) and S_{21} (isolation loss) are given by:

$$S_{12} = S_{21} = \frac{V_1^e + V_1^0}{V_2^e + V_2^0} = \frac{-jV_o\sqrt{2} + 0}{Vo + V_o} = \frac{-j}{\sqrt{2}} \quad (16)$$

Due to symmetricity, the value of $S_{13} = S_{31} = S_{12} = S_{21}$. Moreover, the value of the insertion loss, $S_{23} = S_{32}$ (*insertionloss*) = 0. In both scenarios, this holds true because there is no transmission seen due to a short or open circuit at the bisections. After evaluating all the values, the scattering matrix can be written in the form of equation 17

TABLE 3. Design specifications of a 3-port HPDC.

| Symbol	Parameters	Values
Rogers	Substrate used	R04350
Zo	Characteristic Impedance (Input and Output Ports)	50 Ω
H	Height of Substrate	1.50 mm
T	Thickness of Substrate	0.018 mm
ε_r	Dielectric Constant	3.65
TanD	Loss Tangent	0.0031
fo	Centre frequency	3 GHz
Cond	Conductivity (S/m)	4.1e7
r	Modelithics KOA-0603-101-S Resistor (2Zo)	100 Ω
L	Length of input and output transmission line	10 mm
W	Width of input and output transmission line	3.31 mm
$\sqrt{2}\,Z_o$	Characteristic Impedance of QWS (Ω)	70.710
L_2	Length of QWS is one-fourth of HPDC operation	λ/4
$W_{1\&}W_2$	Width of QWS (1 and 2)	1.78 mm
$R_{1\&}R_2$	The radius of QWS (1 and 2)	9.1 mm
$W_{3\&}W_4$	Width of QWS (3 and 4)	1.78 mm
$R_{3\&}R_4$	The radius of QWS (3 and 4)	3 mm
$L \times H$	Size of the proposed design	56×30 mm
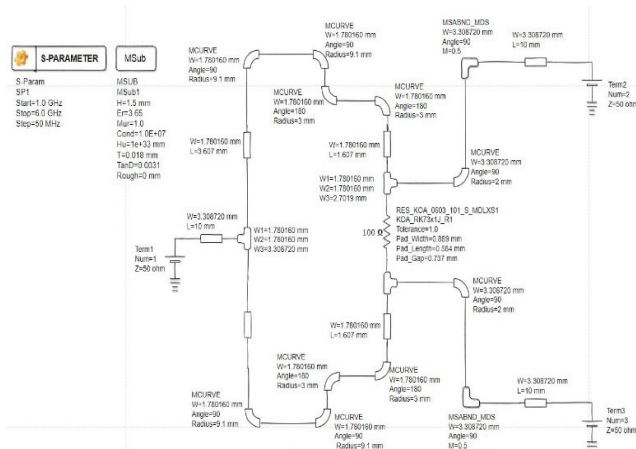
FIGURE 8. A 3-Port HPDC schematic design.

thus:

$$[S] = \begin{bmatrix} 0 & \dfrac{-j}{\sqrt{2}} & \dfrac{-j}{\sqrt{2}} \\ \dfrac{-j}{\sqrt{2}} & 0 & 0 \\ \dfrac{-j}{\sqrt{2}} & 0 & 0 \end{bmatrix} \qquad (17)$$

From equation 17, the diagonal values of the matrices indicate that all ports are matched and reciprocal. The ports are not lossless due to the insertion of an isolation resistor connected between the output ports. As $S_{12} = S_{21} = \frac{-j}{\sqrt{2}}$, the total insertion loss (IL) caused by the isolation resistor is −3.01 dB and derived as:

$$IL = 10\,log_{10}(\frac{-j}{\sqrt{2}})^2 = 10\,log_{10}(\frac{1}{2})$$
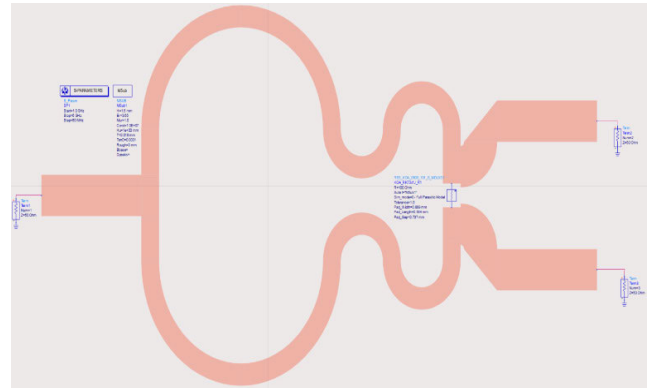$$IL = -3.01\ dB \qquad (18)$$

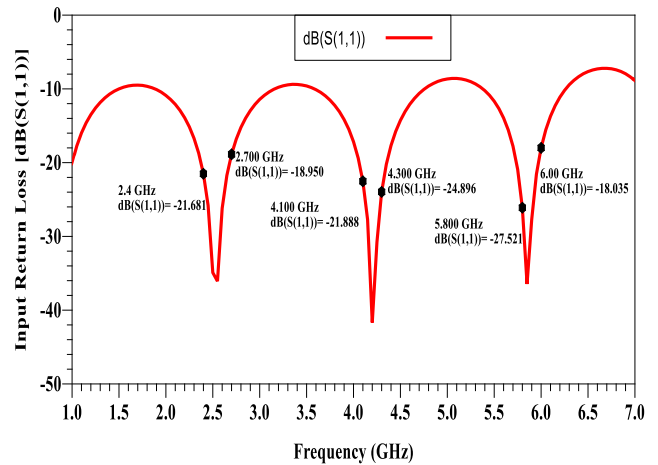**FIGURE 9.** A 3-Port HPDC schematic model.
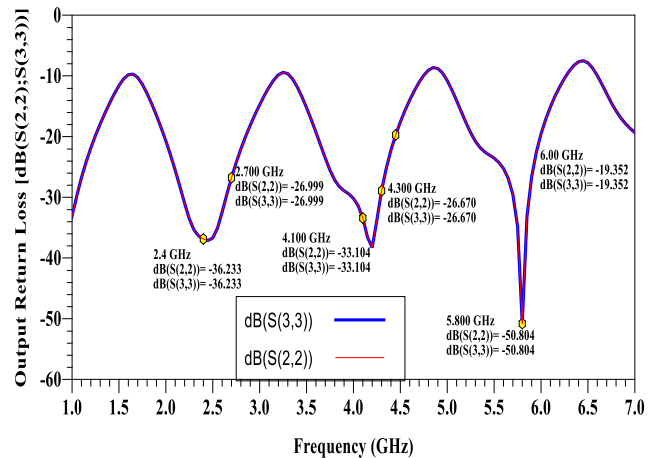

FIGURE 10. Input return loss.

FIGURE 11. Output return loss.

Similarly, the scattering matrix for a 5-port network having 25 independent variables is derived as follows:

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} & S_{15} \\ S_{21} & S_{22} & S_{23} & S_{24} & S_{25} \\ S_{31} & S_{32} & S_{33} & S_{34} & S_{35} \\ S_{41} & S_{42} & S_{43} & S_{44} & S_{45} \\ S_{51} & S_{52} & S_{53} & S_{54} & S_{51} \end{bmatrix} \qquad (19)$$
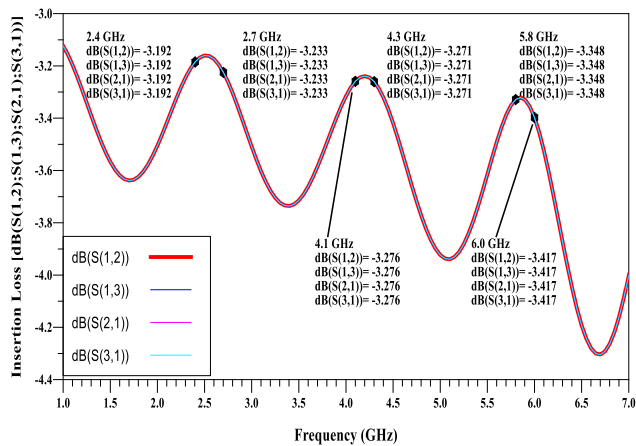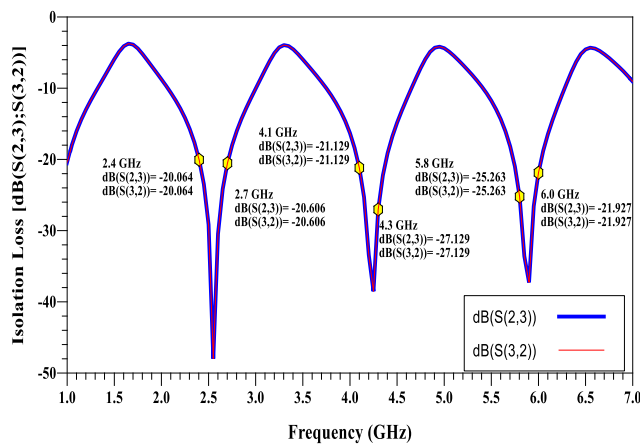
FIGURE 12. Insertion loss.
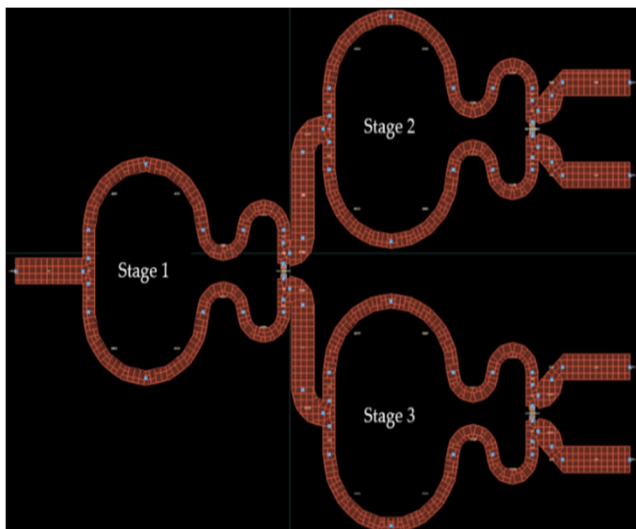

FIGURE 13. Isolation loss.

FIGURE 14. A 5-Port HPDC layout design.

As $S_{12} = S_{21} = \frac{-j}{\sqrt{2}}$; $S_{13} = S_{31} = \frac{-j}{\sqrt{2}}$; $S_{14} = S_{41} = \frac{-j}{\sqrt{2}}$; and $S_{15} = S_{51} = \frac{-j}{\sqrt{2}}$, the total insertion loss caused by three isolation resistors linked between the output ports for a 5-port

TABLE 4. Design specifications of a 5-port HPDC.

Symbol	Parameters	Values
Rogers	Substrate used	R04350
Zo	Characteristic Impedance (Input and Output Ports)	50 Ω
H	Height of Substrate	1.50 mm
T	Thickness of Substrate	0.018 mm
ε_r	Dielectric Constant	3.65
TanD	Loss Tangent	0.0031
fo	Centre frequency	3 GHz
Cond	Conductivity (S/m)	4.1e7
r	Modelithics KOA-0603-101-S Resistor (2Zo)	100 Ω
L	Length of input and output transmission lines (Ports 1 to 5)	10 mm
W	Width of input and output transmission lines (Ports 1 − 5)	3.31 mm
$W_1 - W_4$	Width of QWS 1 - 4 (Stage 1)	1.78 mm
R_1 & R_2	The radius of QWS 1 and 2 (Stage 1)	8.5 mm
R_3 & R_4	The radius of QWS 3 and 4 (Stage 1)	3 mm
L_1 & L_2	Length of transmission lines used to connect two 3-port HPDC	11 mm
$W_5 - W_8$	Width of QWS 5 - 8 (Stage 2)	1.78 mm
R_5 & R_6	The radius of QWS 5 and 6 (Stage 2)	9.2 mm
R_7 & R_8	The radius of QWS 7 and 8 (Stage 2)	2.9 mm
$W_9 - W_{12}$	Width of QWS 9 - 12 (Stage 3)	1.78 mm
R_9 & R_{10}	The radius of QWS 9 and 10 (Stage 3)	9.2 mm
R_{11} & R_{12}	The radius of QWS 11 and 12 (Stage 3)	2.9 mm
$L \times H$	Size of the proposed design	91.7×67.5 mm

network is −6.01 dB and derived thus:

$$IL = 10 \, log_{10}(\frac{-j}{\sqrt{2}})^4 \qquad (20)$$

$$IL = 10 \, log_{10}\left((\frac{-j}{\sqrt{2}})^2 \times (\frac{-j}{\sqrt{2}})^2\right) \qquad (21)$$

$$IL = 10 \, log_{10}(\frac{1}{4}) = -6.01 \text{ dB} \qquad (22)$$

B. HPDC CHARACTERISATION
A PDC is characterised by return loss, isolation loss, and insertion loss under some ideal conditions as illustrated in Table 2.

IV. SYSTEM MODEL DESIGN OF A 3-PORT HYBRID POWER DIVIDER AND COMBINER (HPDC)
A 3-port HPDC is designed with multiple sections of the QWS (known as the impedance transformer) linked between the input and the output ports. To provide high isolation between the output ports, a 100-Ω resistor (Modelithics KOA-0603-101-S) is connected between the two output ports. In the proposed design, two output ports are brought close to each other so that the resistor can be connected directly instead of using bond wires to avoid extra losses. The Rogers R04350 substrate is used in the proposed design because the electrical signal loss for Rogers substrate is minimal. at high frequencies.
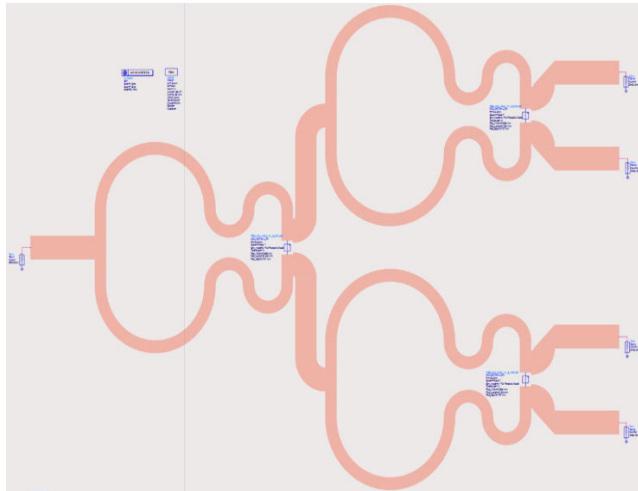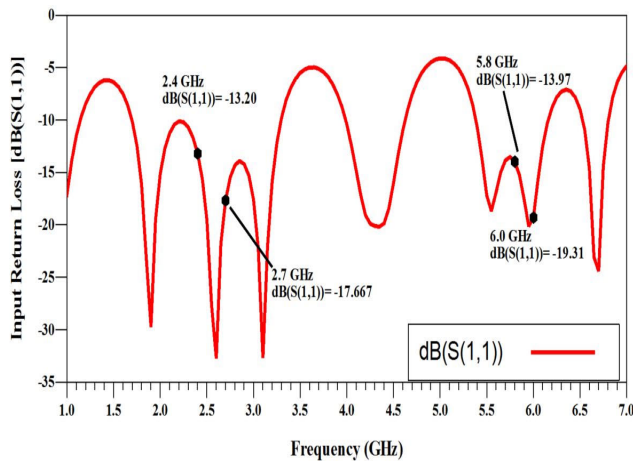
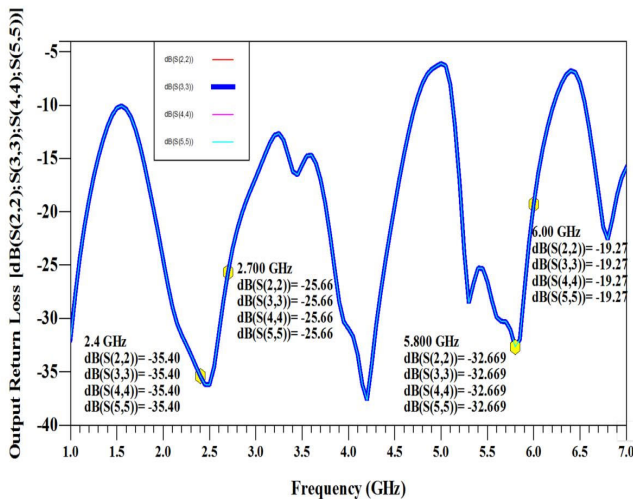**FIGURE 15.** A 5-Port HPDC schematic model.

FIGURE 16. Input return loss.

FIGURE 17. Output return loss.

FIGURE 18. Insertion loss.
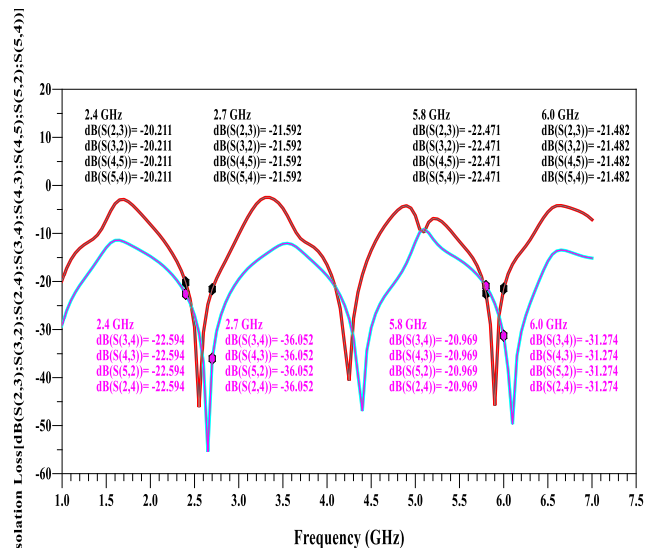
FIGURE 19. Isolation loss.

and the schematic model of the proposed 3-port HPDC is shown in Fig. 8. The length, width, and radius ($S = r \times \theta$) of the transmission lines and the QWS are calculated [by using the line-Calc facility within the Advanced Design System (ADS) software environment] respecting the design parameters (Table 3).

A. RESULTS AND DISCUSSION

The S-parameters obtained from the designed 3- port HPDC in terms of input return loss, output return loss, isolation loss and insertion loss are shown in Figs. 10-13. The input return loss (S_{11}) obtained at 2.4 GHz for the design is -21.68 dB (Fig. 10). The output return loss obtained for all output ports ($S_{22} = S_{33}$) is -36.23 dB (Fig. 11). At 5.8 GHz, the obtained input return loss (S_{11}) is -27.521 dB, and the output return loss obtained for the output ports ($S_{22} = S_{33}$) is -50.80 dB. Similarly, the input return loss (S_{11}) obtained at 6 GHz is -18.04 dB, while the output return loss obtained for outports

Furthermore, the Rogers substrate has a lower dielectric constant with better thermal management and better impedance control at high frequencies. The schematic design
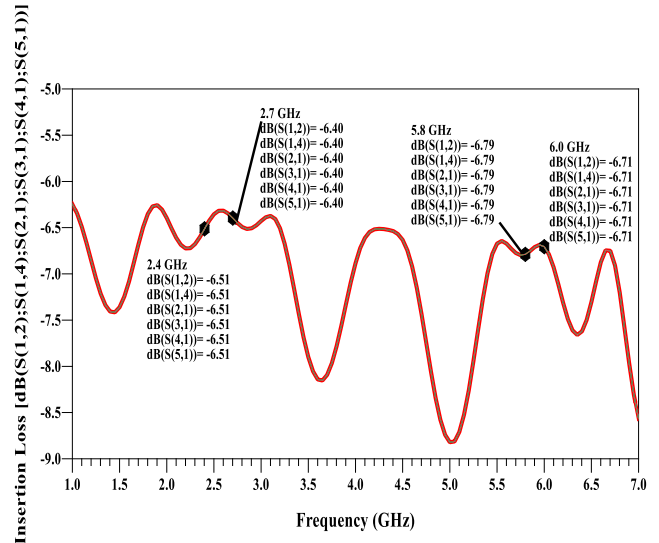
TABLE 5. Performance analysis of a 3-port HPDC.

Parameters	2.4 GHz	5.8 GHz	6 GHz
Input Return Loss (S_{11})	-21.681	-27.521	-18.035
Transmitted Signal (Input Port)	91.75%	95.79%	87.46%
Output Return Loss (S_{22}, S_{33})	-36.233	-50.804	-19.352
Transmitted Signal (Output Port)	98.45%	99.71%	89.23%
Isolation Loss (S_{32}, S_{23})	-20.064	-25.263	-21.927
Insertion Loss (S_{21}, S_{31}, S_{12}, S_{13})	-3.192	-3.348	-3.417

TABLE 6. Performance analysis of a 5-port HPDC.

Parameters	2.4 GHz	5.8 GHz	6 GHz
Input Return Loss (S_{11})	-13.200	-13.970	-19.311
Transmitted Signal (Input Port)	78%	80%	89%
Output Return Loss (S_{22}, S_{33}, S_{44}, S_{55})	-35.40	-32.669	-19.273
Transmitted Signal (Output Port)	98.30%	97.68%	89.12%
Isolation Loss (S_{25}, S_{34}, S_{35}, S_{42}, S_{43}, S_{52}, S_{53}, S_{24})	-22.594	-20.969	-31.273
Isolation Loss (S_{23}, S_{32}, S_{45}, S_{54})	-20.211	-22.471	-21.482
Insertion Loss (S_{12}, S_{13}, S_{14}, S_{15}, S_{21}, S_{31}, S_{41}, S_{51})	-6.513	-6.79	-6.71

ports ($S_{22} = S_{33}$) is -19.35 dB (Fig. 11). Therefore, the significant absolute value of the input return loss and the similar values of the output return loss ($S_{22} = S_{33}$) indicate a good match between all ports.

Furthermore, the isolation loss obtained for all the ports at 2.4 GHz, 5.8 GHz, and 6 GHz is < -20 dB (Fig. 11), indicating that all ports are isolated, and there is no signal leakage between the output ports. In Fig. 12, the insertion loss obtained for all the ports are the same (i.e., $S_{12} = S_{13} = S_{21} = S_{31}$) and indicates an equal power distribution between the output ports. The ideal value of insertion loss for a 3-port network is -3.01 dB, but the obtained value of insertion loss is up to -3.417 dB at the 6 GHz frequency range for the proposed design. The obtained significant insertion loss value compared with the calculated value (equation 18) is due to losses within the connected resistor between the output ports.
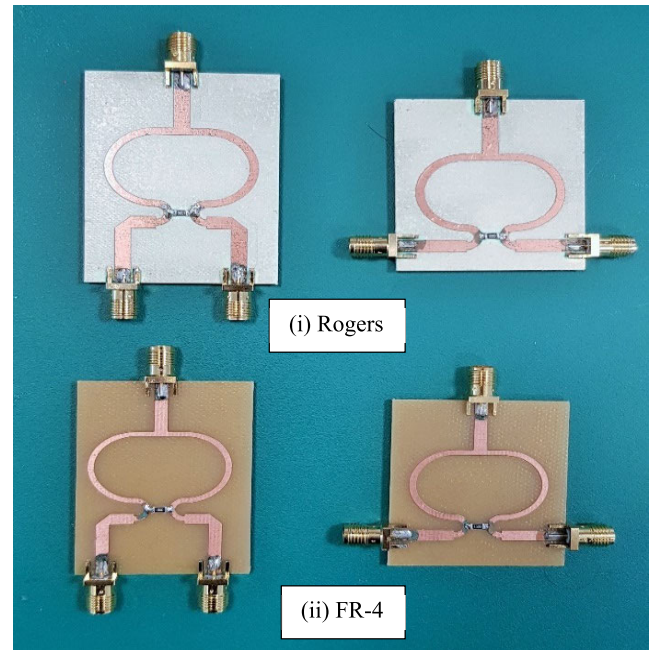
FIGURE 20. Fabricated HPDC using (i) Rogers and (ii) FR-4 substrates.

V. SYSTEM MODEL DESIGN OF A 5-PORT HYBRID POWER DIVIDER AND COMBINER (HPDC)

A 5-port RF HPDC is designed in a three-stage framework (Fig. 14) by interconnecting three 3-port RF HPDCs together. The basic design topology of a 5-port RF HPDC is similar to that of a 3-port HPDC. The non-trivial part whilst designing a 5-port HPDC is interlinking the three 3-port HPDC so that the two interlinked 3-port HPDC (stages 2 and 3) with the output ports of the first 3-port HPDC (stage 1) cannot overlap each other. Moreover, the distance between them must be wide so that the effects of electromagnetic coupling and impedance mismatch can be eliminated. Therefore, an extra transmission line is utilized to interconnect the two 3-port HPDCs to accommodate this design constraint at the two output ports of the first stage (3-port RF HPDC).

In the proposed design, multiple segments of the QWS are linked between the input and the output ports in all three stages of a 5-port HPDC. Besides, three Modelithics KOA-0603-101-S resistors with a value Of 100 Ω are connected to provide high isolation between the output ports. The layout design and schematic model of the designed 5-port HPDC are shown in Fig. 15 and 16. Rogers R04350 substrate is used in the proposed design of 5-port HPDC. The length, width, and radius ($S = r \times \vartheta$) of transmission lines and the QWS are calculated (by using the line-Calc facility within the ADS software environment) respecting the design parameters (Table 4).

A. RESULTS AND DISCUSSION

The S-Parameters obtained for the proposed design of a 5- port HPDC in terms of input return loss, output return loss,

TABLE 7. Comparison of proposed HPDC design with the previous studies.

Source	Frequency		Return loss	Insertion loss	Isolation loss	Size
[42]	2.45 GHz		-25 dB	-3.15 dB, -3.18 dB	-30 dB	42 mm
[38]	Single Layer	2 GHz	-46.8 dB, -48dB	-3.2 dB	-38.3 dB	36 mm
	Double Layer	2 GHz	-42.2 dB, -23.7 dB	-3.3 dB	-25.6 dB	58 mm
	Three Layer	2 GHz	-44.7 dB, -19.8 dB	-3.5 dB	-19.8 dB	81 mm
[43]	1 GHz		-41.977 dB	-2.976 dB	-35.646 dB	41.9 mm
[44]	915 MHz		-58.235 dB, -60.566 dB	-3.046 dB	-55.172 dB	88.391 mm
Proposed Design of 3-port HPDC	2.4 GHz		-21.681 dB -36.233 dB	-3.192 dB	-20.064	56 × 30 mm
	5.8 GHz		-25.612 dB -42.666 dB	-3.348 dB	-25.263	
	6 GHz		-18.035 dB -19.352 dB	-3.417 dB	-21.927	
Proposed Design of 5-Port HPDC	2.4 GHz		-13.200 dB -35.399 dB	-6.513 dB	-22.594 dB, -20.211 dB	91.7×67.5 mm
	5.8 GHz		-13.970 dB -32.673 dB	-6.788 dB	-20.969 dB -22.471 dB	
	6 GHz		-19.311 dB -27.391 dB	-6.706 dB	-31.273 dB -21.482 dB	

isolation loss, and insertion loss is shown in Figs. 16-19. The input return loss (S_{11}) obtained at 2.4 GHz for the proposed design is −13.20 dB (Fig. 16), while the output return loss is obtained for all output ports ($S_{22} = S_{33} = S_{44} = S_{55}$) is −35.40 dB (Fig.17). At 5.8 GHz, the obtained input return loss is −13.97 dB, and the output return loss obtained for output ports ($S_{22} = S_{33} = S_{44} = S_{55}$) is −32.669 dB. Similarly, the input return loss obtained at 6 GHz is −19.31 dB, while the output return loss obtained for outports ports ($S_{22} = S_{33} = S_{44} = S_{55}$) is −19.27 dB (Fig. 17). Thus, the significant absolute value of input return loss and the same values of output return loss ($S_{22} = S_{33} = S_{44} = S_{55}$) indicates a good match between all ports.

Similarly, the isolation loss obtained for all the ports at 2.4 GHz, 5.8 GHz and 6 GHz is less than −20 dB (Fig. 19); this indicates that all ports are isolated, and there is no signal leakage between the output ports. Two different plots of the isolation loss are obtained in the proposed design because of the three-stage networks (Fig. 14). If the signal is inserted from port 2 of the second stage towards ports 4 and 5 of the third stage (Fig. 14), the inserted RF signal will reach its destination port through stage 1. Consequently, two different plots of the isolation loss are obtained. In Fig. 18, the insertion loss obtained for all the ports is the same (i.e., $S_{12} = S_{13} = S_{14} = S_{15} = S_{21} = S_{31} = S_{41} = S_{51}$) and indicates that the power is equally distributed amongst the output ports.

VI. PERFORMANCE ANALYSIS OF 3- AND 5-PORT HPDC

An efficient PDC must be matched at all ports; reciprocal (give the same results in either direction); provide good isolation between the output ports and offer equal distribution of power between the output ports. A scattering matrix is modeled for the 3- and 5-ports PDC network as given in equations (17) and (20). The value of the insertion loss for the 3- and 5- ports HPDC is determined by utilizing the scattering matrix given in equations (17) and (20); the design values are given in equations (18) and (21). The calculated insertion losses for the 3- and 5-ports networks in an ideal situation are −3.01 dB and −6.01 dB respectively. Similarly, the efficiency of the PDC can be calculated (equation 23), in terms of the transmitted RF signal/voltage according to the obtained input and output return losses.

$$\text{Return loss (dB)} = 20 log_{10}[V]$$
$$-10 \text{ dB} = 20 log_{10}[V]$$
$$[V] = 0.316 = 31.6\% \qquad (23)$$

The total loss obtained at −10 dB return loss is 31.6 %, which indicates that 68.4 % signal is transmitted from the input port towards the output port and from the output ports to any connected device. The EM simulated results for the 3- and 5- ports RF-HPDC is evaluated by utilizing the simulation outcomes at 2.4 GHz, 5.8 GHz, and 6 GHz for input and output return losses. The signal transmitted from the input

port towards the output port and from the output port to any connected device is calculated (equation 23) and given in Tables 5 and 6.

Prelim fabricated HPDC designs utilizing FR-4, and Rogers R04350 substrates operating at 1 GHz, 3.15 GHz, 5.2 GHz, and 7.2 GHz have been carried out (Fig. 20). With port 1 excited, the obtained S_{11} is less than -10 dB over the design frequency range. On the other hand, S_{21} and S_{31} are greater than -3.3 dB at the desired operating frequencies except at 1 GHz (-4.8 dB); this is attributed to the load impedance mismatch that can be resolved with the relevant device-under-test measurement setup de-embedding and calibration. Rogers R04350 substrate is used in the proposed design because, at high frequencies, the electrical signal loss for Rogers substrate is minimal compared to FR-4 substrate. The dissipation factor (loss tangent) of FR-4 substrate is 0.02. This makes the use of board impractical above the 2 GHz frequency range due to heavy losses. Furthermore, the dielectric constant of FR-4 substrate is frequency-dependent, and it begins with 4.4 (dissipation factor) at frequencies below 1 GHz and reduces beyond 4 GHz.

The future work involves fabricating the presented Wi-Fi 6E designs and comparing all the practical measurements with the simulation results over the sub-6 GHz 5G-NR spectrum for RF energy harvesting use case and IoTs applications.

VII. CONCLUSION

From the performance metrics and the EM simulation results of the proposed design of a 3-Port HPDC, it can be concluded that at 2.4 GHz (ISM band and IEEE 802.11b,g Wi-Fi standard); 5.8 GHz (IEEE 802.11n Wi-Fi 4 and IEEE 802.11ac Wi-Fi 5 standard); and 6 GHz (IEEE 802.11ax Wi-Fi 6/6E standard), the absolute values of the input and the output return losses obtained indicate a good match between the input and the output ports. Similarly, 91.75 %, 95.79 % and 87.46 % of the RF signal are transmitted from the input towards the output ports at the 2.4 GHz, 5.8 GHz and 6 GHz frequencies respectively. Consequently, 98.45 %, 99.71 % and 89.23 % of the RF signal are transmitted from the output port to any connected device at 2.4 GHz, 5.8 GHz and 6 GHz respectively. Moreover, the results obtained for the isolation loss indicate that $S_{32} = S_{23}$; both output ports are isolated, and there is no leakage of the signal between them. Similarly, for the insertion loss, the calculated value in an ideal situation is -3.01 dB. Still, the obtained value is up to -3.41 dB because of the minimum loss occasioned by the inserted resistor. $S_{21} = S_{31} = S_{12} = S_{13}$ indicates that power is equally distributed amongst all the ports.

Furthermore, based on the EM simulation outcomes and the performance analysis for a 5-port HPDC, it can be inferred that at 5.8 GHz and 6 GHz, 80 % and 89 % of the RF signal are respectively transmitted from the input towards the output ports. As a result, 97.68 % and 89.12 % of the RF signal are transmitted from the output port towards any connected device at 5.8 GHz and 6 GHz respectively. At 2.4 GHz, 78 % of the RF signal is transmitted from the input towards

the output ports, and 98.30 % of the received RF signal is transmitted from the output port to the connected load. The obtained values of the isolation loss are less than -20 dB. It indicates that all output ports are isolated, and there is no current leakage between them. The calculated insertion loss for 5-port networks in an ideal situation is -6.02 dB. In the proposed 5-port HPDC, three resistors with a value of 100 Ω are utilized. Due to the losses within the resistive components, the insertion loss obtained for the proposed design is up to -6.70 dB. The insertion loss obtained for all the ports is the same ($S_{12} = S_{13} = S_{14} = S_{15} = S_{21} = S_{31} = S_{41} = S_{51}$) and indicates that the power is equally distributed. In a 5-port HPDC, two different plots for the isolation loss are obtained because of 3 interlinked 3-port HPDC. If the signal is inserted from port 2 of the second stage toward ports 4 and 5 of the third stage, the inserted RF signal will reach its destination port by going through stage 1. These results are promising for a 5G New Release user equipment and the base station; internet of things applications spanning RF energy harvesting and multiple input multiple output beamforming; and 6G satellite-cellular convergence ecosystem use cases and applications.

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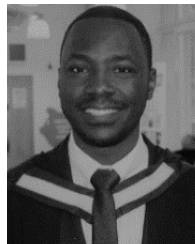
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