December 2021

Clock Trace Structure for Block Sequential Clock Driving

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Abstract:

This publication describes systems and techniques directed at block sequential clock driving to minimize dynamic power consumption associated with driving display panels. In an aspect, clock trace structures within display panels configured to minimize parasitic capacitance associated with display panel circuitry are described herein. In further aspects, techniques enabling resistor-capacitor load matching to minimize a perceived, on-screen luminance delta are also described herein. Through such systems and techniques, display panels can reduce power consumption without degrading user experience.

Keywords:

Display panel, active-matrix organic light-emitting diode (AMOLED), organic light-emitting diode (OLED), clock signal frequency, clock trace structure, block sequential clock driving, display driver integrated circuit, frame rate, refresh rate, pixel array, power consumption

Background:

Many electronic devices (e.g., smartphones) include a display panel (e.g., a screen) having tens of thousands of pixel circuits each with an organic light-emitting diode ("pixel"). These display panels include display panel drivers (e.g., data drivers, gate drivers) connected to the pixel circuits through rows and columns of lines (e.g., electrical traces) to control the brightness, color, and other features of the individual pixels to generate an image. Such display panels may use active-matrix organic light-emitting diode (AMOLED) technology to provide variable refresh

rates, reduced display response times, and lower power consumption in comparison to other display technologies. These advantages make AMOLED displays well-suited for electronic devices and highly-valued by users. To further enhance AMOLED display technology, it is desired to minimize dynamic power consumption in panel-integrated row-line drivers.

Description:

This publication describes systems and techniques directed at block sequential clock driving to minimize dynamic power consumption associated with driving display panels. In an aspect, clock trace structures within display panels configured to minimize parasitic capacitance associated with display panel circuitry are described herein. In further aspects, techniques enabling resistor-capacitor (RC) load matching to minimize a perceived, on-screen luminance delta are also described herein. Figure 1 illustrates an example electronic device in which the described systems and techniques can be implemented.

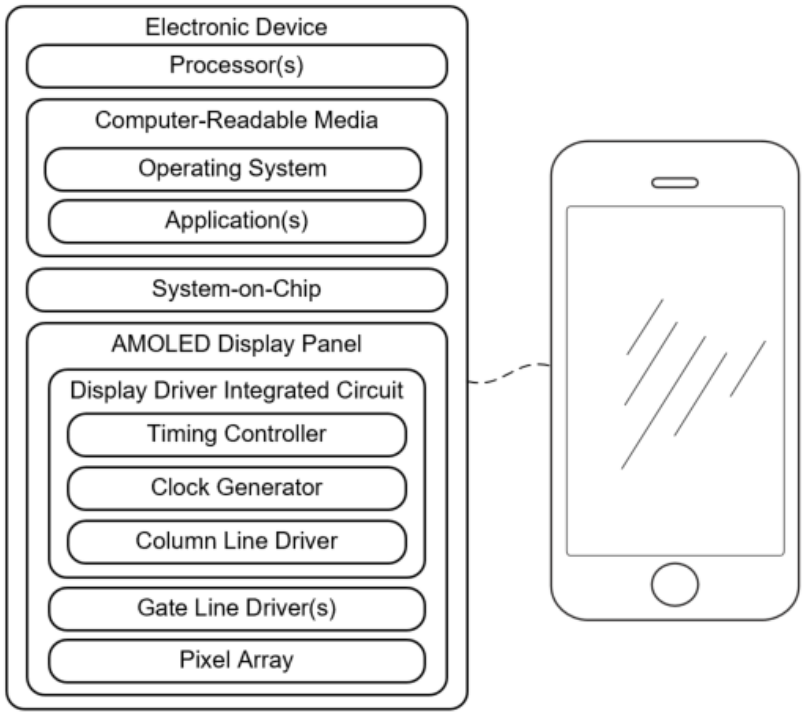

Figure 1

As illustrated in Figure 1, the electronic device is a smartphone. In some implementations, the electronic device can be a variety of other electronic devices. The electronic device may include one or more processors, including a central processing unit (CPU) and a graphics processing unit (GPU). The processor(s) may be configured to execute instructions or commands stored within the computer-readable media to implement an operating system and application(s). For example, the processor(s) may execute instructions of the operating system to implement a display refresh rate of 120 Hertz (Hz).

The electronic device may further include a system-on-chip (SoC) and an active-matrix organic light-emitting diode (AMOLED) display panel. The SoC may be an integrated circuit (e.g., chip) that includes hardware components (e.g., a processor, memory) and software (e.g., custom logic, functions) configured to implement an independent electronic or computing system on a single substrate. In implementations, the SoC is an application specific integrated circuit (ASIC) operably coupled to the AMOLED display panel and implementing display-related operations. For example, under direction of the CPU, the SoC may pass display data to the AMOLED display panel. In implementations, the AMOLED display panel, as illustrated in Figure 1, includes circuitry having a display driver integrated circuit (DDIC), drivers (e.g., a column line driver, gate line driver(s)), and a pixel array of pixel circuits. The DDIC may include a timing controller, a clock generator, and a column line driver.

In configurations, (i) the SoC may be integrated within the AMOLED display panel; (ii) the electronic device may include a DDIC separate from the AMOLED display panel; (iii) the electronic device may include a timing controller and/or clock generator separate from the DDIC and the AMOLED display panel; and/or (iv) the electronic device can include other types of display technology (e.g., a liquid crystal display (LCD) panel). In any of the aforementioned

configurations, as well as any of a variety of alternative combinations unlisted for the sake of conciseness, the systems and techniques described herein can be implemented.

Figure 2 is a schematic illustration of an example AMOLED display panel in which systems and techniques directed at block sequential clock driving to minimize dynamic power consumption associated with driving display panels can be implemented.

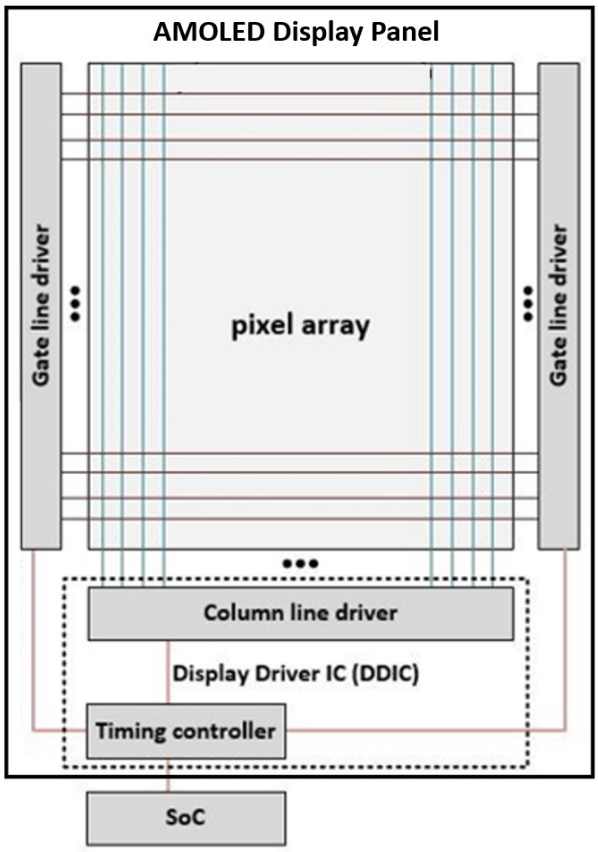

Figure 2

As illustrated in Figure 2, an SoC is operably coupled to the AMOLED display panel via electrical wiring to the timing controller in the DDIC. In implementations, the timing controller provides interfacing functionality between the SoC and the drivers (e.g., column line driver, gate line drivers). In such a configuration, the timing controller can pass signals to the drivers, and the drivers, operably coupled to pixel circuits in the pixel array via driver lines (e.g., electrical traces), can drive the pixel circuits.

As an example, the timing controller may receive commands and display data from the SoC. In response, the timing controller can separate the display data and generate input signals (e.g., image data, control signals) with appropriate voltage, current, timing, and demultiplexing. The input signals may be in the form of square waves, alternating between high and low states, with varying duty cycles. The timing controller may then pass the input signals to a column line driver (e.g., a data-line driver) and gate line drivers. Upon receipt of the input signals, the drivers may pass time-variant and amplitude-variant signals (e.g., voltage signals, current signals) to control the pixel array. For instance, the column line driver may pass data-line signals containing voltage data to the pixel array to control the luminance of an organic light-emitting diode.

The DDIC may further include a clock generator (not illustrated in Figure 2). In an implementation, the clock generator (e.g., internal oscillator, crystal oscillator) is integrated within the DDIC but separate from the timing controller. The clock generator produces a constant clock signal oscillating between a high and a low state ("toggle"). The clock signal may be in a form of a square wave with a 50% duty cycle. The clock signal may be effective to synchronize different parts of the AMOLED display panel circuitry, including the pixel circuits.

In aspects, the gate line drivers may include one or more shift registers. For example, a gate line driver may include a sequential logic circuit having several single bit latches (e.g., D-Type Data Latches) connected together in a serial type daisy-chain arrangement. Each latch may constitute, what is referred to as, a stage. The plurality of stages may be operably coupled to the clock generator and configured to receive clock signals and generate gate signals. As described herein, the gate signals produced by the plurality of stages are referred to as GW signals. In one or more implementations, each stage of the plurality of stages may further generate a carry signal

based on a previous carry signal of a previous stage and a carry clock signal, and generate a scan signal based on the previous carry signal and a scan clock signal.

Figure 3 illustrates the DDIC operably coupled to the pixel array via an example gate line driver.

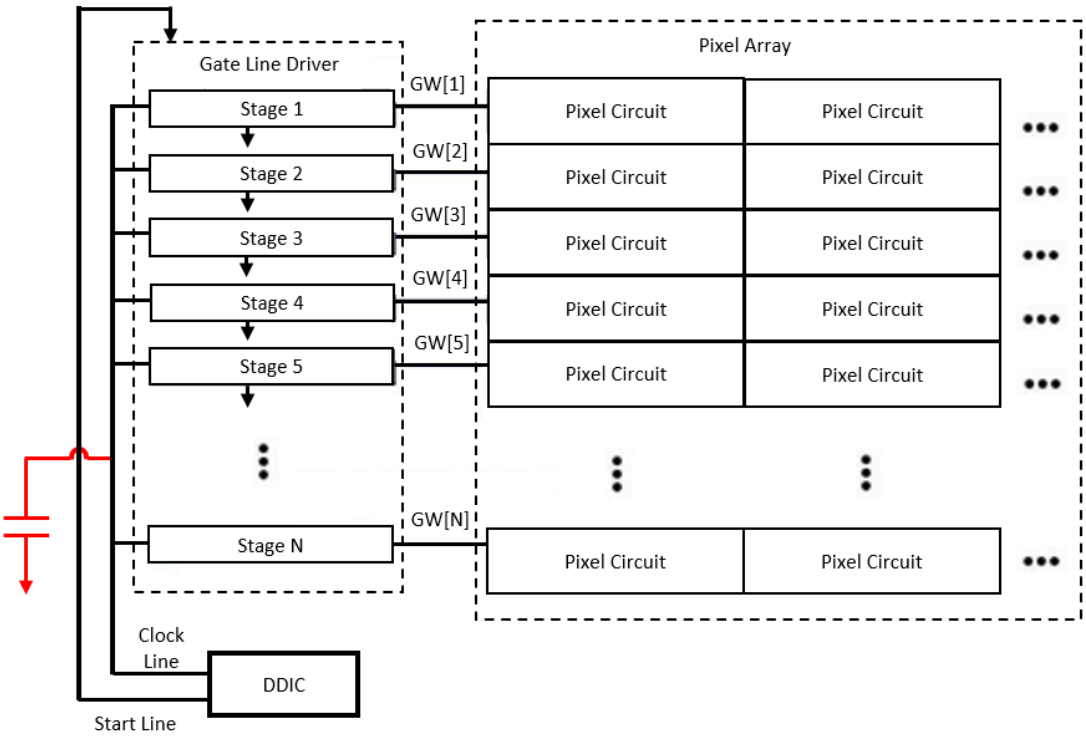

Figure 3

As illustrated in Figure 3, the example gate line driver includes a plurality of stages (e.g., stage 1, stage 2, stage N). The gate line driver may include a stage for each row of pixel circuits in the pixel array (e.g., 3000 rows of pixel circuits) and pass a GW signal (e.g., GW[1], GW[2], GW[N]) to each row of pixel circuits. In the configuration illustrated, the DDIC includes both the clock generator and the timing controller.

A start line and a clock line extend from the DDIC and are operably coupled to the gate line driver. The start line may pass a start signal provided from the timing controller. The clock line (e.g., clock trace) may pass one or more clock signals provided from the clock generator. The clock line may extend from the DDIC to the gate line driver and components therein, as illustrated

in Figure 3. For example, the clock line can pass a set of clock signals (e.g., two clock signals at varying frequencies) via a bundle of electrical wires, multiple traces, modulation, time division multiplexing, and/or the such. The input line may pass the set of clock signals at a predetermined frequency for a defined frame rate.

Figure 4 illustrates an example timing diagram including a start signal and a set of clock signals, as well as resulting GW signals produced by the plurality of stages in the gate line driver.

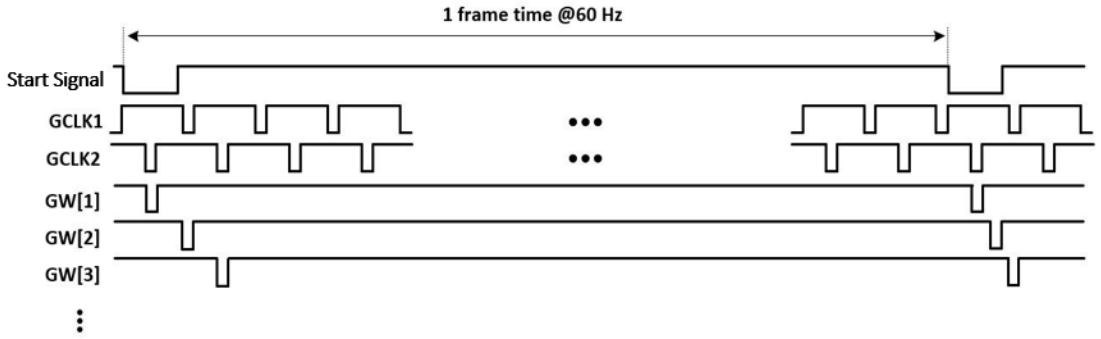

Figure 4

The CPU of the electronic device may implement a frame rate of 60 Hz and direct the SoC to pass commands to the DDIC to generate clock signals supporting and/or corresponding to the 60 Hz frame rate. The DDIC, having the clock generator, may produce two clock signals at varying frequencies (e.g., GCLK1, GCLK2), as illustrated in Figure 4. These clock signals may then be passed as a single set through the clock line. The DDIC, having the timing controller, may concurrently produce a start signal (e.g., pass a low value). The start signal may then be passed through the start line. The start signal and the set of clock signals may cause the plurality of stages to generate GW signals (e.g., GW[1], GW[2], GW[3]) that are passed to rows of pixel circuits in the pixel array in a sequential fashion.

In some instances, the DDIC passing a set of clock signals that toggle multiple times within a single frame time can cause the clock line to charge and discharge, producing parasitic capacitance, as illustrated in Figure 3. This parasitic capacitance is a substantial contributor to

excessive power dissipation in AMOLED display panels, responsible for as much as 20% of a total driving power of a display panel. As a result, a single set of clock signals may be split into multiple sets (e.g., two or more) of clock signals and passed through multiple clock lines. For example, a single set of clock signals may be split into two sets of clock signals using latches and passed through two clock lines operably coupled to the DDIC.

Figure 5 illustrates an example timing diagram including a start signal and two sets of clock signals, as well as resulting GW signals produced by the plurality of stages in the gate line driver.

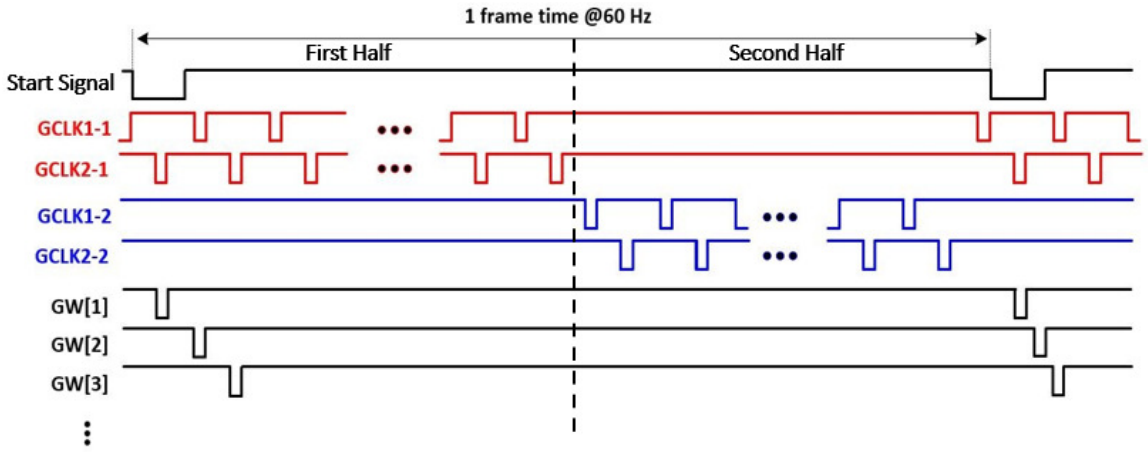

Figure 5

As illustrated in Figure 5, the original set of clock signals (e.g., illustrated in Figure 4) may be split into halves. For example, the original set of clock signals included GCLK1 and GLCK2. This set of clock signals are split into two sets: set one including GCLK1-1 and GCLK2-1; and set two including GCLK1-2 and GCLK2-2. Splitting the set of clock signals into two sets is effective to enable set one to toggle for a first half of a frame time and cause set two to idle for the first half of the frame time, as well as enable set one to idle for a second half of a frame time and cause set two to toggle for the second half of the frame time. Through such a technique, the parasitic capacitance produced in the clock lines are effectively halved. The number of sets of clock signals can be increased to further reduce power consumption.

Figure 6 illustrates an example clock line configuration by which to pass multiple sets of clock signals to the gate line driver.

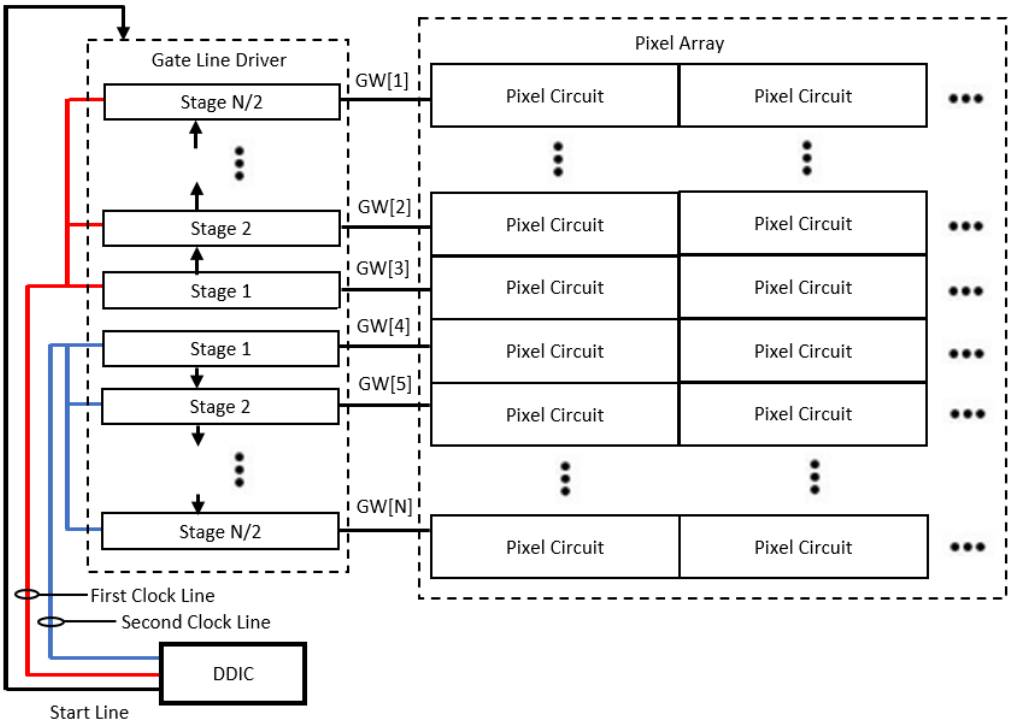

Figure 6

As illustrated in Figure 6, the DDIC includes two clock lines each passing a set of clock signals. Further illustrated, the stages within the gate line driver are partitioned into two portions defined by where the clock lines enter the gate line driver. In order match a RC load (e.g., the impedance) between a first clock line and a second clock line, and thereby reduce a perceived luminance delta (e.g., a difference in brightness) between a row of pixel circuits that receive, for example, GW[3] and a row of pixel circuits that receive, for example, GW[4], the clock lines extending from the DDIC may be structured in such a way that they have nearly identical line (e.g., trace) lengths and enter the gate line driver at stages positioned proximately next to each other. In alternative implementations, the clock lines can enter the gate line driver portioning the gate line driver into unequal portions. In further implementations, the clock lines can be interlaced (e.g., blended), coupling to one or more stages in either portions of the gate line driver.

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