# A 2.45/5.8 GHz high-efficiency dual-band rectifier for low radio frequency input power

**Sara El Mattar, Abdennaceur Baghdad, Abdelhakim Ballouk**
Laboratory of Electronics, Energy, Automatics and Data Processing, Department of Electrical Engineering, Hassan II University, Casablanca, Morocco

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**ABSTRACT**

This article proposes a concurrent rectifier for radio frequency (RF) energy harvesting from the popular ambient RF sources wireless fidelity (WiFi) 2.45 and 5.8 GHz bands. A voltage doubler-based converter circuit with the Schottky SMS7630 diode is used, this chosen diode has shown good results for low power levels. To ameliorate the resulting circuit, we used an interdigital capacitor (IDC) instead of a lumped component; and then we added a filter to reject the 3rd harmonics of each operating frequency. A dual-band impedance transformer with a direct current (DC) block function is used and optimized at low input power points for more harvested DC power. The final circuit was, therefore, more efficient and more reliable. The maximum conversion efficiencies obtained from the resulting circuit are about 60.321% for 2.45 GHz and 47.175% for 5.8 GHz at 2 dBm of input power. Compared to other previous rectifiers presented in the literature, our proposed circuit presents high efficiencies at low power levels and at these operating frequencies.



***Corresponding Author:***

Sara El Mattar
Laboratory of Electronics, Energy, Automatics and Data Processing, Department of Electrical Engineering, Hassan II University
Fst Mohammedia-Casablanca, Morocco
Email: saraelmattar@gmail.com

## 1. INTRODUCTION

The first wireless energy recovery was presented by Nikola Tesla in the 1890s using the electromagnetic wave propagation technique of Heinrich Hertz [1], [2]. Since this discovery, radio frequency (RF) energy harvesting has become an attractive alternative technology, on the one hand, it is considered as green energy [3], and on the other hand, it reduces the dependence of most wireless devices on a power source. Thus, it offers the opportunity to feed the mobile devices remotely, providing the current electricity they need to function, or to reload the batteries included. This technology is applied in many fields of applications such as radio frequency identification (RFID), powering wireless sensors, and powering solar satellites [4]–[6]. The procedure consists in recovering the electromagnetic energy emitted by the immediate sources of the environment and transforming it into continuous power. This can be achieved by a receiving antenna, connected to a system called rectifier capable of converting radio frequency energy (RF) into direct current (DC). In order to meet the progressively challenging energy needs of wireless devices, single band [7]–[9], multiband [10], [11] and broadband [12] rectifiers have been presented. Moreover, the multiband harvest must be even more designed and improved. With the rise in the use of the industrial, scientific, and medical (ISM) band in different systems, certain researchers have designed and presented a number of rectifiers in previous papers for frequencies in this band.

Wang and Negra [13] present a double-band rectifier with 66.8% of maximum efficiency for 2.45 GHz and achieved 51.5% for the second operating frequency at 10 dBm of input power. In a similar manner, in [14], a dual-frequency rectenna for the same operating frequencies was presented with conversion efficiencies greater than 80% at received power levels of 35.6 mW (≈15.5 dBm) and 39.26 mW (≈16 dBm) for the used frequencies respectively. On the 5.8 GHz, a rectenna system with an input power of ≈16.98 dBm was designed in [15] with 82% conversion efficiency. A 2.45 GHz rectifier has been presented in [16] where the RF-DC transformation efficiency achieved is 76% but this maximum efficiency is for an input power of 20 dBm. The principle of wireless energy transmission by radiofrequency waves is based on the fact that a wave propagates in a vacuum while retaining the energy with which it is charged, this energy being attenuated according to the medium crossed by the wave and this attenuation increases with the frequency (in our case more than 2 GHz). In addition, there are norms and standards that define the maximum authorized transmission power levels of access points at these frequencies, which make the power levels received by the antennas in the range of nW/cm² to µW/cm². For all of these reasons 20 dBm [16], 16 dBm [14], [15] and 10 dBm [13] are not normal power levels captured in the air while the feasible power levels of ambient RF energy are lower for these bands generally from -10 to -30 dBm [17].

In this work, a concurrent dual-band rectifier operating efficiently at low levels of incident power is presented for wireless energy recovery using the SMS7630 diode and a reduction of lumped components used. On the one hand, by replacing the rectifying capacitor with an interdigital capacitor (IDC), on the other hand, the use of a matching network with direct current block function, therefore eliminate the DC block capacitor at the input of the voltage doubler. Moreover, the use of harmonic rejection filter which further improves the final design's efficiency.

## 2. RF RECTIFIER DESIGN AND ANALYSIS

Generally, the rectifier structure includes a matching network; that modifies the impedance to achieve a perfect match with the rectifier diode, followed by a conversion circuit that transforms the electromagnetic energy to a continuous signal. An output DC-filter that blocks higher-order harmonics re-radiation and a resistor must be situated in the output to work as a load to measure the continuous output power. Figure 1 depicts the configuration of the used rectifier.

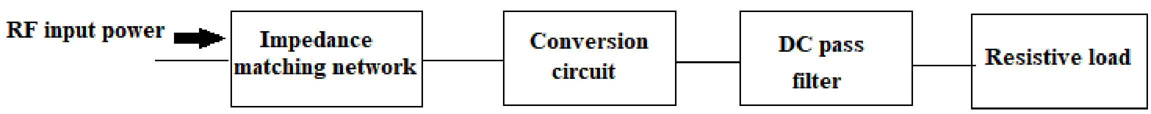



Figure 1. General functional diagram of the rectifier stage

### 2.1. RF to DC conversion circuit design

For this work, and as it is exposed in Figure 2, two diodes are arranged in the sort of a voltage doubler. Because this topology features more efficient energy management capabilities. In addition, the output capacitor (C), the harmonic rejection filter (HRF), and the load resistor (R) efficiently pass the DC output voltage and block higher-order harmonics.

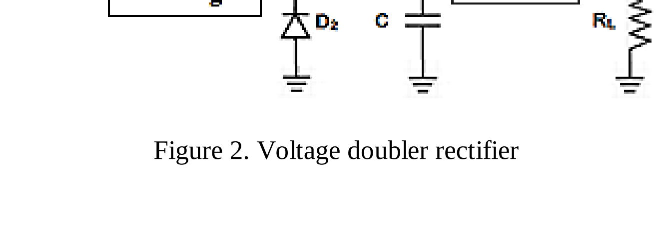



Figure 2. Voltage doubler rectifier

Nowadays, we know that the diode in the rectifier represents the heart of this circuit, which is why the election of the appropriate diode is a fascinating design stage. Schottky diodes are the most used in the rectifier circuit [18]–[22] according to their ability to perform fast switching which allows them to detect very low input signals [23]. The chosen Schottky diode is the SMS7630 from Skyworks as a rectifying element in this study. We chose this diode because of its management capacity of low power levels, this diode provides 2 V of the breakdown voltage 0.14 pF of junction capacitance and 20 Ω as series resistance; this implies that this diode is the best for a lower input power [24], [25]. For the simulations employing the advanced design system (ADS) software, this diode's spice model was used, given by the vendor.

We have opted in the rectifier described in this article to reduce the localized components even if they reduce the size of the resulting circuits; because when operating at relatively high frequencies (this is the case for us), the localized components present significant intrinsic losses. In our design, we use IDC as an alternative solution, it has higher quality factors than the interval capacitor and the metal insulator metal (MIM) capacitor and its use will minimize the cost, increase the reliability and reduce welding procedures [26]. We will exploit ADS software tool to design this capacitor. As a substrate and with a 1575 mm of thickness, the Rogers RT/Duroid 5880 was adopted because of its small dissipation factor (0.0004), and a 2.2 of relative permittivity of all sections of our circuit.

## 2.2. Impedance matching circuits

The components used in rectifiers make them non-linear circuits; since its input impedance varies according to these parameters: the input power, the value of the load and the frequency used. For optimal and maximum transferred power, the rectifier diode impedance must be adapted to the antenna (50 Ω) impedance. For this reason, we use the impedance matching network (MN) part; its purpose to guarantee an appropriate signal transmission between the receiving antenna part and the rectification circuit. Therefore, it will allow us to harvest from ambient RF signals and reach a maximum quantity of converted DC power [27]–[31].

Matching networks which are based on lumped elements have generally been used in most of the work [32], [33]. This presented circuit is based on microstrip lines for matching unit. Using the S-parameters simulation of the rectifier in ADS software, we obtain its input impedance, the input source is a one-tone signal source and the DC block is included. Then MATLAB is used to determine the dual band impedance MN's preliminary design parameters by using the design equations presented in [34].

Afterward, we optimized the result parameters utilizing the ADS tool for optimization to correspond, in the desired frequency bands, the input impedance at the voltage doubler part for a load of 2.7 kΩ and the whole range of low input power. Figure 3 represents the impedance MN and the Table 1 that follows summarizes the design parameters of the system. The matching network used in this work is preferred by the fact that this transformer not only has a double band impedance matching operation but also has an inherent DC block function, which explains the lack of use of a DC block capacitor at the input of the voltage doubler circuit and which further reduces the losses.


Figure 3. Impedance matching network

Table 1. Optimized design dimensions for matching network

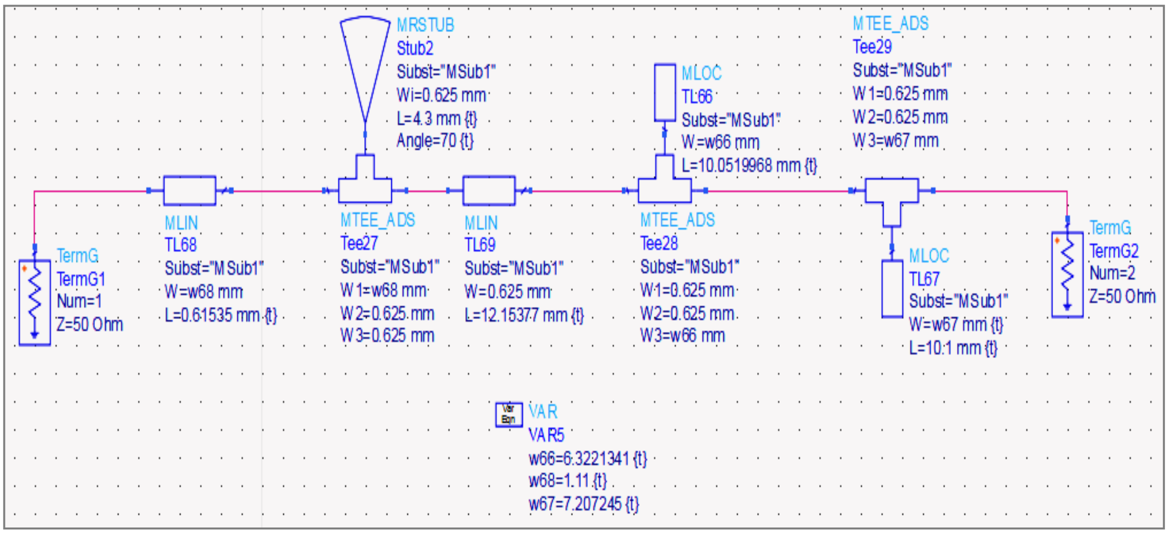
| Parameters | Value(mm) |
|---|---|
| TL1 Length | 21.049 |
| TL1 Width | 0.7556672 |
| CLin1 Length | 13.6773 |
| CLin1 Width | 1.63665 |
| CLin1 spacing between lines | 0.2291085 |

## 2.3. Harmonic rejection filter

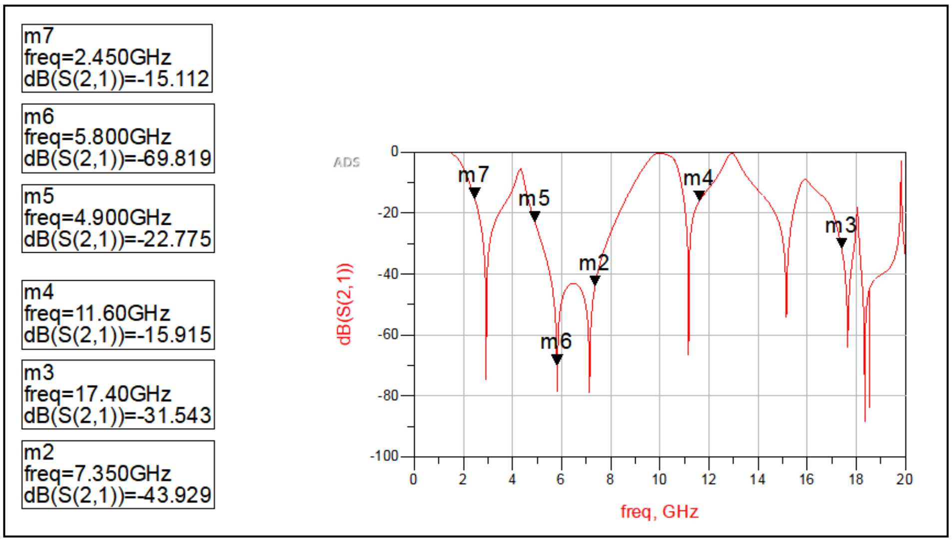
A designed harmonic rejection filter is achieved using a fan-shaped radial stub and two open stubs, the radial stub has an angle of 70° and it is elected by optimization in ADS. There is variation in the size of the three stubs depending on the frequency. They are designed to smooth the fundamental frequency, second-order, and third-order harmonics for each band. The design parameters of HRF and its simulated S parameters are exposed in Table 2, Figures 4(a) and 4(b). We can deduct from the figure that the filter allows the harmonics in the bands 2.45 GHz, 4.9 GHz, 7.35 GHz, 5.8 GHz, 11.6 GHz, and 17.4 GHz to be rejected, which are the three harmonics for the first and second operating frequency respectively. Figure 5 depicts the diagram of the ADS circuit resulting from the proposed rectifier, which consists of an adaptation circuit, a conversion circuit, and the DC filter with harmonic rejection filter.

Table 2. The design parameters of HRF

| Stub name | Values |
|---|---|
| TL68 Width | 1.11 mm |
| Length | 0.61535 mm |
| TL69 Width | 0.625 mm |
| Length | 12.15377 mm |
| TL66 Width | 6.3221341 mm |
| Length | 10.0519968 mm |
| TL67 Width | 7.207245 mm |
| Length | 10.1 mm |
| STUB2 Width | 0.625 mm |
| Length | 4.3 mm |
| Angle | 70° |




(a)




(b)

Figure 4. HRF: (a) ADS design and (b) S21 parameter

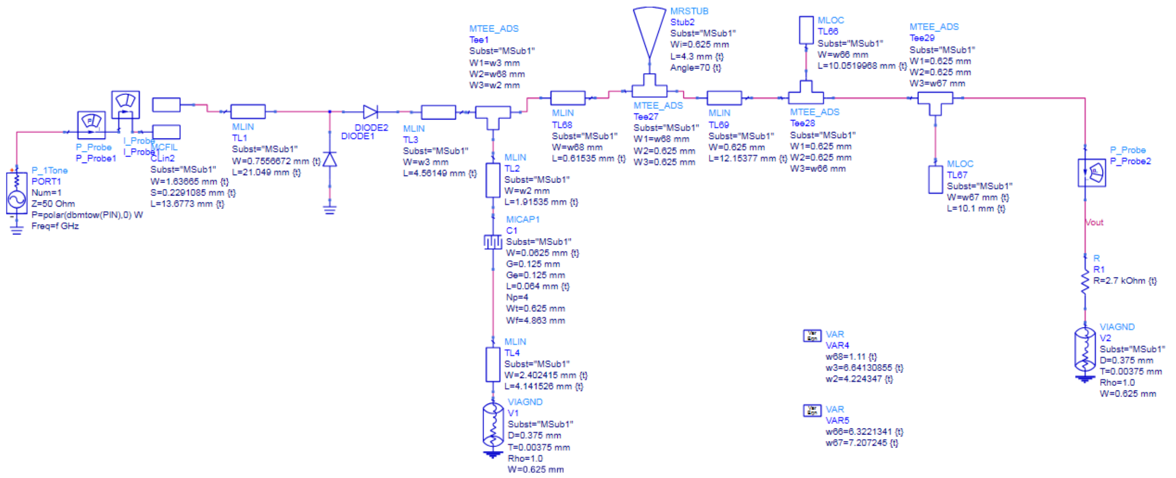


Figure 5. Dual-band rectifier scheme as a result of ADS simulations

## 3. RESULTS AND DISCUSSION

ADS tools (S parameters at large signal and harmonic balance) are used for simulation, optimization, and analyze. Figures 6, Figures 7(a) and 7(b) show the results of these simulations. Table 3 will summarize and compare the proposed rectifier performance with other reported dual-band rectifiers.

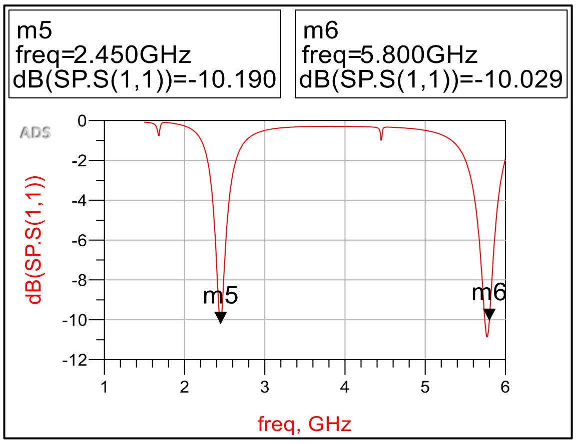



Figure 6. Simulation result of S11 parameter

Table 3. A comparison of dual-band rectifiers

| Ref | Bands [GHz] | Maximum Efficiency (%) at 2.45 GHZ | Maximum Efficiency (%) at 5.8 GHZ | Input power for Maximum Efficiency [dBm] |
|---|---|---|---|---|
| [13] | 2.45/5.8 | 66.8 | 51.5 | 10 |
| [14] | 2.45/5.8 | 84.4 | 82.7 | ≈15.5 for 2.45 GHz<br>≈16 for 5.8 GHz |
| [17] | 2.45/5.85 | 57.1 | 39.2 | 0 for 2.45 GHz<br>1 for 5.8 GHz |
| [35] | 0.915/2.45 | 38 | * | 0 |
| This work | 2.45/5.8 | 60.321 | 47.175 | 2 |

*: Not Applicable

### 3.1. Suggested design results

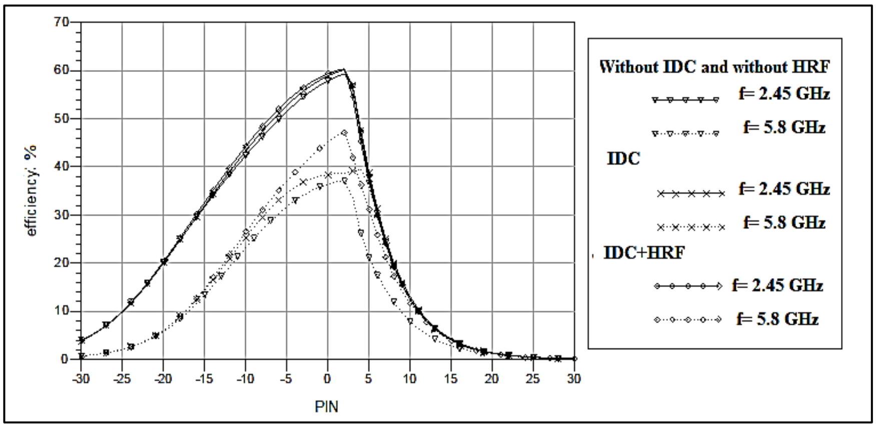
Figure 6 illustrates the variation of the simulated rectifie's S11 parameter with a load of 2.7 kΩ and -10 dBm as input power. The rectifier, as can be shown, is well matched to the desired frequencies, the circuit resonates when the return loss is less than -8 dB: -10.190 dB for the first frequency and -10.029 dB for the second frequency. Efficiency is one of the most significant performance parameters that can be used as a basis for the critical evaluation of the performance of converting RF power to DC power for the rectifier. In general, it is calculated from the expression (1):

$$\text{efficiency} = 100 * (\text{PDC}/\text{PRF}) \quad (1)$$

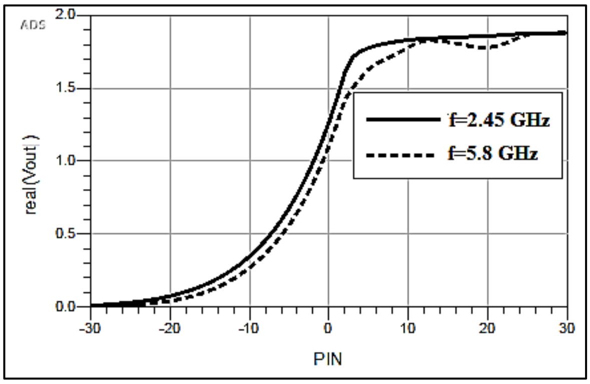
where $P_{DC}$: denotes the converted continuous power, $P_{RF}$: input power of the rectifier.

The result of the simulation of RF to DC conversion efficiency and DC output voltage as a function of the injected power levels is illustrated in Figure 7. It is clearly seen that, depending on power levels, these two parameters vary. In Figure 7(b), the rectifier begins to collect the voltage at low incident powers, and then this voltage mounts with the increase in this power to a maximum value and then they remain constant; these variations are related to the both operating frequencies.

We have shown in the Figure 7(a) the changes made by adding the capacitor IDC and the HRF filter. We aim to compare the effect of each element on the rectifier's efficiency, so we simulated the rectifier with commonly used SMD capacitor first, then we replaced the capacitor with IDC, and next we added the filter HRF. We can clearly deduce that rectifier efficiency has improved and especially for the upper-frequency 5.8 GHz. We went from 37.076% efficiency for the rectifier without IDC and without HRF filter to 47.175% higher efficiency for the same frequency by adding the two circuits (IDC+HRF). In the study interval, the maximum conversion efficiencies achieved are about 60.321% for 2.45 GHz and 47.175% for 5.8 GHz at 2 dBm, and 44.36% for 2.45 GHz and 26.592% for 5.8 GHz at a typical power input of −10 dBm.




(a)




(b)

Figure 7. Results of simulations depending on the given power (a) efficiency and (b) output voltage

### 3.2. Comparison with other works

Table 3 compares the proposed rectifier performance with other reported dual-band rectifiers works. These rectifiers function at various input power levels not necessarily similar to our design. As a result, when compared to other rectifiers for relatively low RF power levels, our rectifier has high efficiency values in the desired frequencies.

## 4. CONCLUSION

We have presented, in this work, a double band rectifier for reduced RF power inputs. The proposed prototype topology consists of the voltage doubler where the SMS7630 diode was chosen as a rectifier element. We opted to reduce the lumped components in the circuit in need to improve reliability and optimize the circuit, which is why an interdigital capacitor and a matching network with dc block function are used. A harmonic rejection filter was also inserted to smooth the fundamental frequency, second-order, and third-order harmonics for each band. We have shown the usefulness of adding each part (IDC and HFR) to the final design and compared the effect it has on the rectifier's efficiency. The addition of these two parts allowed us to further improve the efficiency of our rectifier, especially for the upper frequency, where we went from 37.076% efficiency for the rectifier without IDC and without the HRF filter to 47.175% by adding the two circuits (IDC+HRF). According to the dual-band rectifiers reported in the literature, the proposed rectifier is a concurrent high-efficiency rectifier for reduced RF power input ranges, with a peak of 60.321%, 47.175% achieved for 2.45 GHz and 5.8 GHz respectively.

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## BIOGRAPHIES OF AUTHORS

**Sara El Mattar** born in Mohammedia Morocco on October 14, 1995. In 2016, she obtained her license degree in telecommunications engineering at the Faculty of Science and Technology of Mohammedia - Hassan II University Casablanca, then she had got a Master's degree in Internet of Things and Mobile Systems at national school of applied sciences in Fez. She is currently a Ph.D. student in the Laboratory of Electronics, Energy, Automatics and Data Processing (EEA&TI) Hassan II University, Mohammedia-Casablanca, Morocco. Her works studies are focused on the design and the optimization of the passive RFID tags and especially energy harvesting technology, under the supervision of Pr. A. Baghdad. She can be contacted at email: saraelmattar@gmail.com.

**Abdennaceur Baghdad** is a holder of a doctorate in Electronics in 1992 at the University of Lille-France. He is University Professor (PES) at the University Hassan II Mohammedia Casablanca-Morocco (FSTM) where he teaches the electronics, Hyperfrequencies, antenna and telecommunication. He is a member of the laboratory electronics, energy, automatic and information processing (EEA & TI). His research works concerns the communication and information technology (electronics systems and telecommunication). He can be contacted at email: nasser_baghdad@yahoo.fr.

**Abdelhakim Ballouk** is a University Professor at the Faculty of Science and Technology Mohammedia - Hassan II University of Casablanca. Member of the Laboratory of Electronics, Energy, Automatics & Information Processing. He obtained his Doctorate from the University of Bordeaux France in 1992, in the field of Automatics. The fields of research are Automatic notably robust controls, predictive commands and Telecommunications. He can be contacted at email: balloukhakim@gmail.com.