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Special Power Electronics Converters and Machine Drives with Wide Band-Gap Devices

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Dr. Daniel Lau, Director of Graduate Studies

Special Power Electronics Converters and Machine Drives with Wide Band-Gap Devices

DISSERTATION

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the College of Engineering at the University of Kentucky

By

Yibin Zhang

Lexington, Kentucky

Director: Dr. Dan M. Ionel, Professor and L. Stanley Pigman Chair in Power

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ABSTRACT OF DISSERTATION

SPECIAL POWER ELECTRONICS CONVERTERS AND MACHINE DRIVES WITH WIDE BAND-GAP DEVICES

Power electronic converters play a key role in the power generation, storage, and consumption. The major portion of power losses in the converters is dissipated in the semiconductor switching devices. During recent years, new power semiconductors based on wide band-gap (WBG) devices have been increasingly developed and employed in terms of the promising merits including the lower on-state resistance, lower turn-on/off energy, higher capable switching frequency, higher temperature tolerance than conventional Si devices. However, WBG devices also brought new challenges including lower fault tolerance, higher system cost, gate driver challenges, and high dv/dt and resulting increased bearing current in electric machines.

This work first proposed a hybrid "Si IGBTs + SiC MOSFETs" five-level transistor clamped H-bridge (TCHB) inverter which required significantly fewer number of semiconductor switches and fewer isolated DC sources than the conventional cascaded H-bridge inverter. As a result, system cost was largely reduced considering the high price of WBG devices in the present market. The semiconductor switches operated at carrier frequency were configured as Silicon Carbide (SiC) devices to improve the inverter efficiency, while the switches operated at fundamental output frequency (i.e., grid frequency) were constituted by Silicon (Si) IGBT devices. Different modulation strategies and control methods were developed and compared. In other words, this proposed "SiC+Si" hybrid TCHB inverter provided a solution to ride through a

load short-circuit fault. Another special power electronic, multiport converter, was designed for EV charging station integrated with PV power generation and battery energy storage system. The control scheme for different charging modes was carefully developed to improve stabilization including power gap balancing, peak shaving and valley filling, and voltage sag compensation. As a result, the influence on power grid was reduced due to the matching between daily charging demand and adequate daytime PV generation.

For special machine drives, such as slotless and coreless machines with low inductance, low core losses, typical drive implementations using conventional silicon-based devices are performance limited and also produce large current and torque ripples. In this research, WBG devices were employed to increase inverter switching frequency, reduce current ripple, reduce filter size, and as a result reduce drive system cost. Two inverter drive configurations were proposed and implemented with WBG devices in order to mitigate such issues for 2-phase very low inductance machines. Two inverter topologies, i.e., a dual H-bridge inverter with maximum redundancy and survivability and a 3-leg inverter for reduced cost, were considered. Simulation and experimental results validated the drive configurations in this dissertation.

An integrated AC/AC converter was developed for 2-phase motor drives. Additionally, the proposed integrated AC/AC converter was systematically compared with commonly used topologies including AC/DC/AC converter and matrix converters, in terms of the output voltage/current capability, total harmonics distortion (THD), and system cost. Furthermore, closed-loop speed controllers were developed for the three topologies, and the maximum operation range and output phase currents were investigated. The proposed integrated AC/AC converter with a single-phase input and a 2-phase output reduced the switch count to six and resulting minimized system cost and size for low power applications. In contrast, AC/DC/AC pulse width modulation (PWM) converters contained twelve active power semiconductor switches and a common DC link. Furthermore, a modulation scheme and filters for the proposed converter were developed and modeled in detail.

For the significantly increased bearing current caused by the transition from Si

devices to WBG devices, an advanced modeling and analysis approach was proposed by using coupled field-circuit electromagnetic finite element analysis (FEA) to model bearing voltage and current in electric machines, which took into account the influence of distributed winding conductors and frequency-dependent winding RL parameters. Possible bearing current issues in axial-flux machines, and possibilities of computation time reduction, were also discussed. Two experimental validation approaches were proposed: time-domain analysis approach to accurately capture the time transient, stationary testing approach to measure bearing capacitance without complex control development or loading condition limitations. In addition, two types of motors were employed for experimental validation: an inside out E-type PMSM was used for rotating testing and stationary testing, and a I-type BLDC was used for stationary testing. Possible solutions for the increased CMV and bearing currents caused by the implementation of WGB devices were discussed and developed in simulation validation, including multi-carrier SPWM modulation and H-8 converter topology.

KEYWORDS: Wide band-gap devices, multilevel converter, multiport converter, motor drives, bearing current.

Yibin Zhang

December 18, 2021

SPECIAL POWER ELECTRONICS CONVERTERS AND MACHINE DRIVES WITH WIDE BAND-GAP DEVICES

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December 18, 2021

Date

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current and axial flux machines and provided specialized hardware components.

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Yibin Zhang

November, 2021

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Chapter 1

Introduction

1.1 Wide Band Gap Devices

The energy required by an electron to jump from the highest part of the valence band to the lowest part of the conduction band is the energy band-gap of a semiconductor [1] [2]. For conventional Silicon (Si) devices, the energy band-gap is usually around $1eV$; while the materials known as wide band-gap (WBG) typically are with more than $2eV$ [3]. With the wider band-gap merits, WBG materials has a potential in significantly reducing die size for the equal blocking voltage value. In addition, smaller die size decreases output capacitance C_{oss}, parasitic capacitances and MOSFET gate charge [4] [5]. Furthermore, the reduction of MOSFET capacitances improves the power MOSFETs operating at higher frequencies because of the lower switching losses[6].

1.2 Characteristics and Advantages

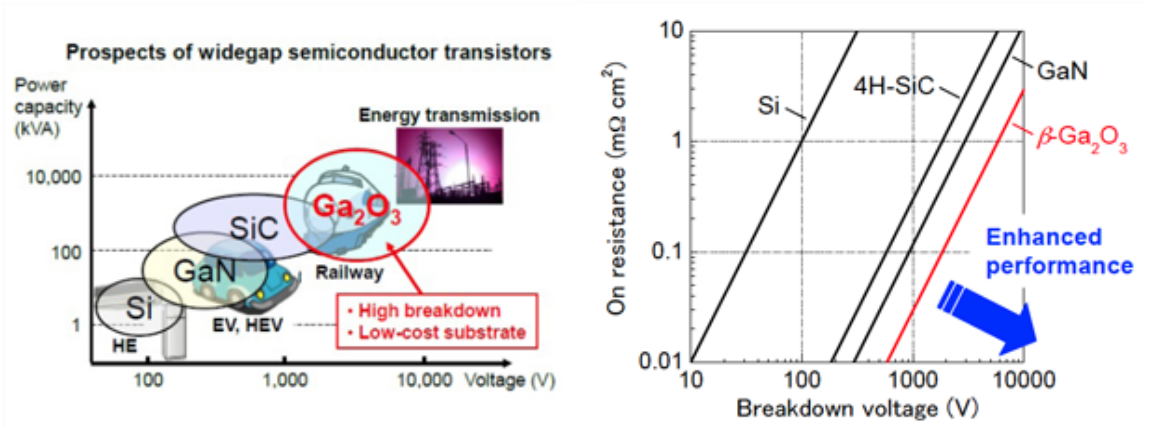
For WBG devices such as SiC and GaN, the advantages can be summarized as following:

- Low on resistance and capacitance
- High operating frequency and reduced switching losses
- Decreased conduction losses due to low on-state resistance
- High power density

For different applications, WBG devices offer different advantages 1.1. In the low power (<500W) and blocking voltage (<600V) area, lateral GaN power HEMTs are offering both high power density and lower power loss over both silicon and SiC devices [7]. In the medium power (1-100kW) and blocking voltage (1-5kV), 1.2kV SiC power MOSFETs are capable of displacing Si IGBTs by increasing the upper limit of switching frequencies and improving the energy efficiency and power density in motor drives and power converters [1]. In the high power (>1MW) and ultra high blocking voltage (>5kV) range, SiC and GaN power devices are making possible topologies which are previously not possible with Si. Above 5kV, the SiC IGBT is preferred over the SiC power MOSFET, due to conductivity modulation in the drift layer [8].

1.3 Comparison Among Commercialized Power Semiconductor Devices: Si, SiC, and GaN

Discarding for diamond due to the prohibitive manufacture cost, WBG power devices including Silicon Carbide (SiC) and Gallium Nitride (GaN) have been penetrating to market [10] as shown in Fig. 1.2a. In general, both SiC and GaN offers similar improvements on the electrical performance of power electronics devices. Due



(a) (b)

Figure 1.1: Comparison of the power semiconductors [9], (a) the application range of transistors, (b) On-resistance versus breakdown voltage of the semiconductors.

to the profiles and manufacturing, SiC and GaN devices offer various advantages for different applications considering the voltage rating, power rating, operating frequency, and temperature conditions (Fig. 1.2b).

SiC-based power MOSFETs as the first wide bandgap semiconductor to reach commercial maturity have higher operating temperature since SiC has high melting point[11]. And high temperature operating has been the main selling point since SiC started to be developed by Purdue [12] and Cree [13]. That helps to decrease the cooling size which improves the overall system power density [4] [14]. Furthermore, SiC power MOSFETs can be fabricated as the vertical channel, the lateral channel, and trench MOSFET. The vertical channel makes the low on-resistance possible [15]. Based on the aforementioned merits of SiC devices, various types of power devices by using SiC semiconductors already achieved significant improvements: power rectifiers including both unipolar Schottky rectifier with fast reverse recovery, high reverse blocking voltage, and reduced power dissipation [16]; bipolar junction rectifier with

significantly reduced reverse recovery charge and and recovery time even under high temperature [17], SiC GTOs with faster switching and tolerance to higher temperature [18], and SiC JFETs. One of the most advanced ICs so far is developed by NASA and the JFET circuits have demonstrated year-long operation at 500 ° [19].

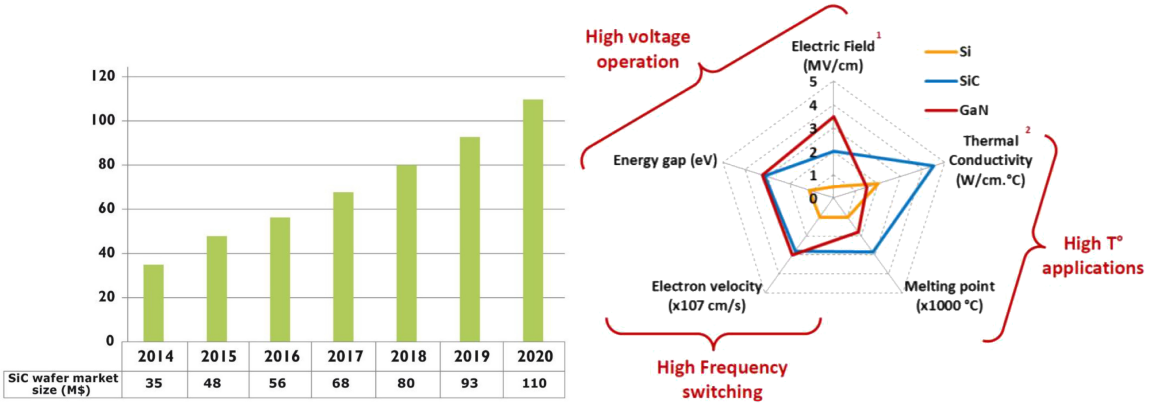
Compared with Si and SiC MOSFETs, the most important features of the GaN power MOSFETs are high current capability and ability to work at even higher switching frequency with lower dead-time [20]. GaN can be designed as vertical and lateral structures [21], and main products and technologies can be summarized as: GaN power diode (Schottky Barrier Diode and PN diodes), [22], GaN high electron mobility transistor (Enhanced GaN HEMT [23], High voltage Cascode GaN HEMT [24]), and GaN MOSFET [25].

A systematic comparison among Si, SiC, and GaN devices are summarized in Table 1.1. Both SiC and GaN devices show advantages over Si devices, and SiC shows larger thermal conductivity ($4.5 W/cm{\cdot}K$), temperature stability (1700 °C), higher voltage rating (1200V) and higher power ratings, compared with GaN devices (>1.5 $W/cm{\cdot}K$, >900°C, and <650V, respectively).

1.4 Research Objectives and Original Contributions

1.4.1 Statement of Problems

- Improvement on electrical performance of power converters and motor drive systems:



(a) (b)

Figure 1.2: The trend and illustration of WBG power devices, (a) SiC market size through 2020 [3], and (b) illustration of the material properties of wide bandgap semiconductors over silicon [1].

Table 1.1: Comparison of characteristic parameters for Si, SiC, and GaN semiconductors.

Characteristic parameters	Unit	Si	SiC	GaN
Energy gap	eV	1.1	3.26	3.49
Electron mobility	cm^2/Vs	1500	700	2000
Intrinsic carrier concentration	cm^{-3}	1.5×10^{10}	8.2×10^{-9}	$1.9\times10^{-1}{}^{0}$
Saturated electron velocity	10^7cm/s	1.0	2.0	2.8
Electric breakdown field	MV/cm	0.4	2	3.3
Thermal conductivity	W/cm·K	1.5	4.5	>1.5
Thermal expansion coefficient	$10^{-}6K^{-1}$	2.6	2.77	5.59
Relative permittivity	ε_r	11.8	10.0	9.0
Lattice mismatch	%	-17	+3.5	–
Wafer size	inches	12	3	1.3
Temperature stability	°C	900	1700	>900
Direct/indirect		I	I	D

WBG devices provide a promising solution to increase power density, and reduce power losses, compared with traditional Si devices [26]. According to WBGs' lower on-resistance along with ultra-small junction capacitance and gate charge in the aforementioned literature review, less conduction loss and switching loss are one of the advantages. With a improved power density, switch number in some special converter topologies such as multi-level converters [27] and multi-port converters [28] which consist of a massive number of power semiconductor switches can be possibly reduced. Associated pulse width modulation (PWM) strategies need to be designed. Furthermore, total harmonics distortion (THD) can also be reduced by employing high switching frequency WBG devices. In another important application - motor drives, high switching frequency up to 200kHz [29] offers motors with a reduced input current ripples. And the size and cost of filters can be further reduced [30].

- System cost:

  The two largest cost contributors in the overall cost breakdown of a typical inverter (Fig. 1.4.1) are the mechanical components (i.e. coldplate, seal, bus bars, etc.), and the power stage (i.e. power semiconductor switches of Si, SiC, or GaN) [31]. Complete device packaging includes baseplate (with cooling fins), direct bonded copper substrate, power semiconductor devices, gate driver for WBG devices, mechanical interface, and signal connections [32] [33]. On the other hand, gate driver circuits need to be re-designed in response to increasing the maximum power module junction temperature limit and dv/dt prevention

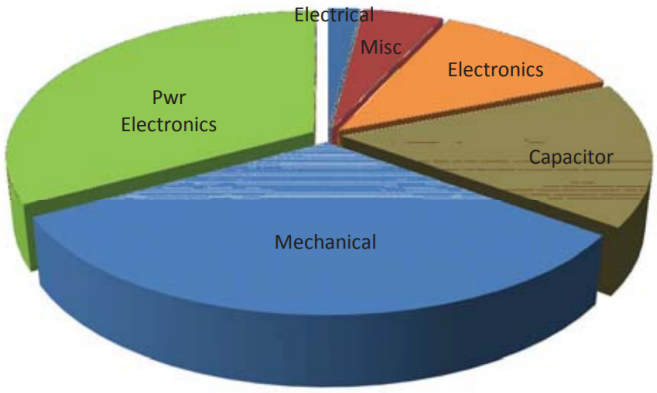


Figure 1.3: Typical cost breakdown for WBG devices based inverters [31].

for WBG devices [34] [35]. A comparison of a phase shifted full bridge converter between Si IGBTs and SiC JFETs [36] shows the contributions on system cost from power semiconductor devices and their related gate drive circuits. If the count of power semiconductor devices can be reduced, the system cost will be significantly reduced.

Pulse width modulation (PWM) technique with high switching frequency is commonly employed in converter control; however, this usually results in a large content of harmonics [37]. Therefore, an output filter is required the first 40th current harmonics can be controlled within the limit [38] in convention Si device based converters, especially in electric vehicles and aerospace related applications where high power density and reduced are the main considerations [39]. With the help pf WBG devices on high switching frequency, harmonics can be massively reduced and it paves the way to possibly reduce the size and cost on filter, and further result in reducing system cost.

- Limited short-circuit capability:

The robustness, and especially the short-circuit capability is critical for power electronics applications [40]. Due to a smaller chip size and higher current density, SiC MOSFETs tend to have a lower short-circuit withstanding time compared to Si devices [41]. Typically the short-circuit withstand time (SCWT) of SiC MOSFETs only has several µs [42], while that of Si IGBTs is usually above 10 µs. Fast response protection circuit or development on extending SCWT are required for SiC MOSFET based converters [43]. De-sat protection scheme are widely used for device protection; nonetheless, drivers with de-sat protection are designed for Si IGBTs and not fast enough for the protection of SiC MOSFETs [44]. In comparison to the standalone SiC, a hybrid switch combining a Si IGBT and SiC MOSFET in parallel has been proposed to provide longer SCWT [45]; however, this solution dramatically increases the count of power semiconductors and resulting increased gate driver burden, converter size, and system cost.

- Balancing system cost and survivability and capability for two-phase machine drives:

  Generally speaking of drive system configurations, filters such as LC [46] and LCL filters [47] have to be implemented to reduce PWM reflected current harmonics. WBG devices which enable the PWM frequency capability of 50 to 100 kHz or even higher, can significantly reduce current ripples keeps the current ripple within acceptable limits for low inductance machine drives [48] and resulting in a cost reduction on filters. Additional benefits brought by WBG devices

to motor drives include enhanced fault tolerance [49], increased efficiency [50], improved power density [51], high-temperature operation [52], reduced system weight including passive component number and reduced heat sink size [53].

To further reduce the system cost of low power motor drive applications such as for residences and small commercial buildings, single-phase or two-phase motors and drives with reduced switch count have shown attractiveness [54] about their the magnetic and electrical isolation between two phases [55], compactness [56], reduced cost [57], and enhanced robustness [58]. Single-phase and two-phase motors work well in constant-speed applications but show difficulties when variable-speed performance is needed [59]. To improve the variable-speed capability of 2-phase machines, it becomes necessary to explore alternative inverter topologies and associated modulation schemes and the optimal use of WBG devices in 2-phase machine drives [60], [61].

- PCB designs due to WBG high dv/dt:

  The high operating frequency of WBG devices causes a very high dv/dt and high di/dt. Additionally, the parasitic factors come into prominence [62]. To overcome mentioned problems the gate trace on PCB should be as short as possible to decrease the parasitic inductance and capacitance and suitable gate resistor should be chosen [62]. With high dv/dt, the threshold voltage of the gate may be exceeded and cause MOSFET to be turn on due to Miller effect. As a result, there is a problem of increasing the risk of dielectric breakdown in motor drive application [63]. An interleaved layout configuration can be used to

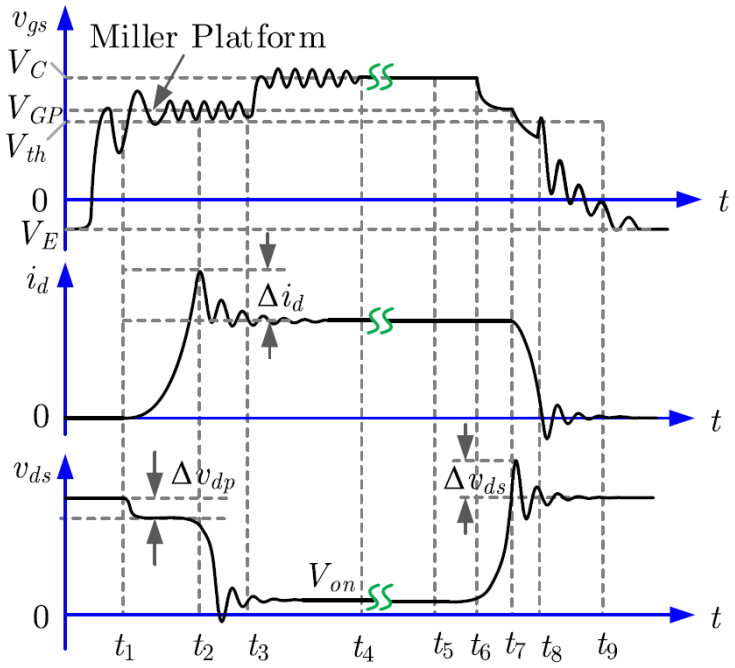


Figure 1.4: Turn-on and turn-off processes of SiC MOSFET. The high dv/dt during WBG switching may induce a significant ringing due to the parasitic inductances and parasitic capacitances [67].

minimize voltage spikes across the DC link [64]. In addition, gating resistance is also important for SiC based MOSFETs and needs to be carefully designed. In researches [63–66], RC snubbers and ferrite beads are demonstrated to dampen the oscillations and switching ringing in different applications.

- Increased bearing current in electric machines by the implementation of WBG devices:

  PWM converters have pulsed voltage outputs featuring high dv/dt (voltage gradient) and high switching frequencies. The sum of the three-phase voltages is not zero and results in the common mode voltage (CMV), whose waveform depends on the DC bus voltage, modulation strategy, and the switching frequency.

The high dv/dt of the CMV at winding terminals introduces displacement currents flowing through not only the bearing lubricant but also winding insulations, which further results in varying flux encirculating the machine shaft. The circular flux around the shaft may introduce bearing currents that flow in both bearings in the drive and non-drive end, depending on the housing structure.

With the implementation of advanced wide band gap (WBG) devices, a much faster turn on/off speed and lower resistance cane be achieved. As a result, WBG devices based machine drives enable higher switching frequencies ranging from a few hundreds of kHz to MHz and higher dv/dt. From a device efficiency point of view, high dv/dt to minimize the turn-on/turn-off times corresponding to the switching losses; however, the high dv/dt poses new challenges for bearing reliability [68]. The increased bearing current caused by WBG devices shortens the lifespan of bearings and causes damages include generalized roughness due to pitting and fluting of the bearing races surfaces and rolling elements[69]. These damages are directly related to current flowing between the bearing components and results in vibration, increased friction with associated heat generation and ultimately can lead to bearing seizure or catastrophic failure [51]. A growing number of bearing current induced premature bearing failures have been reported, calling for more research effort into bearing currents and the associated mitigation techniques [70]. Without appropriate counter-measures for these effects, a machine bearing can be destroyed within a few months of operation. Bearing failures caused by bearing currents account for approximately 9% in the cement industry [71].

1.4.2 Original Contributions

- A hybrid "SiC MOSFETs + Si IGBT" transistor-clamped H bridge (TCHB) five-level converter was proposed. Various modulation schemes including double-reference single-carrier and single-reference double-carrier PWM strategies for the proposed five-level converter were developed. Power losses including conduction loss and switching loss were mathematically evaluated, modeled, and simulated, and efficiency was improved compared with conventional Si based five level TCHB converters. Furthermore, fault tolerance of this proposed converter was validated to be improved.

- A non-isolated multi-port converter based on SiC MOSFETs was proposed for EV charging system, taken power density, system cost, compactness, and power losses into consideration. A systematic comparison based on modeling and simulation was conducted to validate the efficiency improvement by this proposed multi-port converter. Different operating mode including PV charging EVs, PV charging battery energy storage (BES) were discussed and carefully designed, and detailed control scheme was developed and validated in simulation.

- Different converter topologies were developed for low inductance two-phase machines: dual-H bridge to provide full operating range and output capability; three-leg converter to reduce system cost and size. A systematic comparison on topology, modulation, operating range, and power capability was conducted. A field oriented control (FOC) was developed for two phase axial PM machine drive. The control scheme was modeled and validated in both simulation and

experimentation. A re-configurable SiC MOSFET based inverter prototype was built to drive the two-phase AFPM motor.

- An integrated AC/AC converter for two phase motor drive was developed to further reduce the switch count and as a result system cost. Other common used converter topology was also developed for two-phase motor drives including conventional back-to-back converters and matrix converters. A throughout analysis of conventional back-to-back converter, matrix converter, and proposed AC/AC converter was completed to compare the switch number, system cost, filter, control, output capability and operating range. A PCB design was conducted for the two-phase integrated AC/AC converter. SiC MOSFET gate driver circuit, bypass capacitor sizing, driver protection circuit, dv/dt prevention, and turn-off circuit were carefully designed and included in the PCB layout. Simulation and experimental results provided the validation on the effectiveness of both converter and control scheme.

- Two types of combined numerical analysis and test procedures were proposed and validated: a time-domain FEA approach to fully capture the time transient variations, and a special stationary testing to measure bearing voltage and capacitance without complex control development or loading condition limitations. Possible reduction of computation time in this proposed approach was investigated. In addition, two types of motors were employed for experimental validation: an inside out E-type PMSM was used for rotating testing and stationary testing, and a I-type BLDC was used for stationary testing. Possible

solutions for the increased CMV and bearing currents caused by the implementation of WGB devices were discussed and developed in simulation validation, including multi-carrier SPWM modulation and H-8 converter topology.

1.5 Dissertation Outline

In order to address the design of special power electronics converter and motor drives with WBG devices, the following chapters have been included. Chapter 2 proposes a "SiC MOSFET + Si IGBT" hybrid transistor-clamped H-bridge (TCHB) fivl-level converter and different modulation strategies including single-reference double-carrier PWM and double-reference single-carrier PWM. This design consists of only five switches, and features reduced power losses and and enhanced fault tolerance. Chapter 3 presents a systematic study of proposed drive configurations and control scheme with wide bandgap (WBG) devices in order to mitigate current ripples issues and system cost for 2-phase very low inductance machines. A experimental demonstration validates the effectiveness of the design. Chapter 4 proposes an integrated AC/AC converter with a minimized the system cost and size for two-phase machine drives. Converter development, filter design, gate driver, experimental validation, and a systematic comparison between commonly used AC/DC/AC converter and matrix converter are discussed. In Chapter 5 an advanced modeling and analysis approach based on coupled field-circuit electromagnetic finite element analysis (FEA) is proposed for estimating bearing voltage and current in electric machines. The influence of distributed winding conductors and frequency-dependent winding RL parameters are taken into consideration and different types of bearing currents are investigated.

Two BLDC motors are implemented for experimental validation and simulation modeling and analysis, and potential solutions including H-8 topology and multi-carrier SPWM methods are discussed. Conclusions and proposed future works are provided in Chapter 6.

1.6 Publications

The main elements covered in this dissertation have been peer reviewed and published in:

- Yibin Zhang, Jiangbiao He, Sanjeevikumar Padmanaban, and Dan M. Ionel, "Transistor-Clamped Multilevel H-Bridge Inverter in Si and SiC Hybrid Configuration for High-Efficiency Photovoltaic Applications", 2018 IEEE ECCE, Portland, OR, USA, 2018, pp. 2536 – 2542 [72]

- Yibin Zhang, Jiangbiao He, and Dan M. Ionel, "Modeling and Control of a Multiport Converter based EV Charging Station with PV and Battery", 2019 IEEE ITEC, Novi, MI, USA, 2019, pp. 1 - 5 [73]

- Yibin Zhang, Damien L. Lawhorn, Peng Han, Aaron M. Cramer, and Dan M. Ionel, "Electric Drives with Wide Bandgap Devices for Two-Phase Very Low Inductance Machines," 2020 IEEE ECCE, Detroit, MI, USA, 2020, pp. 6125-6129 [57]

- Yibin Zhang, Damien L. Lawhorn, Peng Han, and Dan M. Ionel, "Integrated AC to AC Converters for Single-phase Input to Two-phase Output Motor Drives," 2021 IEEE IEMDC, Hartford, CT, USA, 2021, 5p [74]

- Peng Han, Yibin Zhang, Greg Heins, Dean Patterson, Mark Thiele, and Dan M. Ionel, "On the Modeling of Bearing Voltage and Current in PWM Converter Fed Electric Machines Using Electromagnetic Finite Element Analysis," 2021 IEEE ECCE, Vancouver, Canada, 2021, 5p [75]

Additional conference proceeding papers have been published:

- Yibin Zhang, Oluwaseun M. Akeyo, Jiangbiao He, and Dan M. Ionel, "Control of a Solid State Transformer based Multi-MW Utility-Scale PV-Battery System," 2019 IEEE ECCE, Baltimore, MD, USA, 2019, pp. 6481 - 6486 [76]

- Peng Han, Greg Heins, Yibin Zhang, and Dan M. Ionel, "Integrated Modular Motor Drives Based on Multiphase Axial-flux PM Machines with Fractional-slot Concentrated Windings," 2021 IEEE IEMDC, Hartford, CT, USA, 2021, 6p [77]

Chapter 2

Multi-Level Converters with WBG Devices

2.1 Introduction and Problem Formulation

Multilevel inverters have a number of attractive features, such as the capability of withstanding high voltage, low output harmonic distortion and dv/dt [78]. Therefore, multilevel inverters have been widely applied in various applications such as renewable energy generations [79], [80], energy storage [81], high-voltage direct current power transmission [82], and medium-voltage motor drives [83–85]. However, one drawback with multilevel inverters is the large number of switching devices required in their circuit topologies, which may increase the system cost and failure probability. On the other hand, to improve the efficiency of multilevel inverters especially for PV applications, using WBG devices such as Silicon Carbide (SiC) MOSFETs in multilevel inverters may not be a feasible solution in practice, due to the high cost of WBG devices and the fierce competition of solar inverters in the present market.

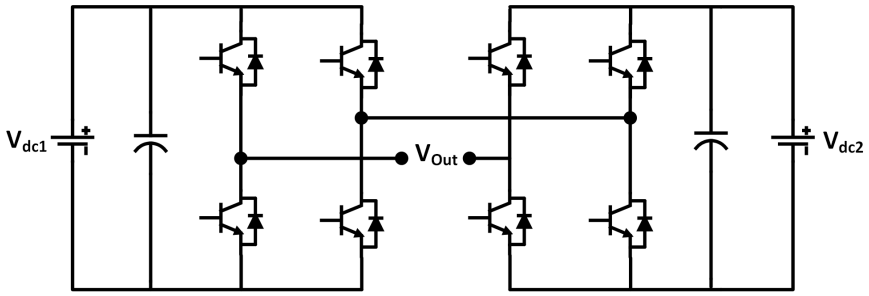


Figure 2.1: Topology of a 5-level cascaded H-bridge inverter. At least 8 power semiconductor devices and two separate DC power supplies are required.

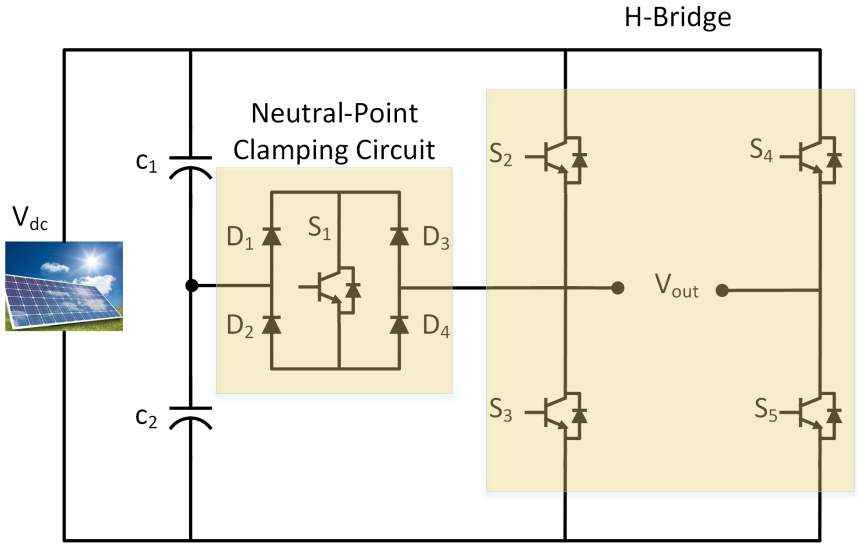


Figure 2.2: Topology of a 5-level transistor clamped H-bridge (TCHB) inverter. This topology largely reduces power semiconductor switch number, diode number, DC capacitor components, and resulting system cost.

2.2 Literature Review

Cascaded-bridge converter (CBC), diode-clamped, and flying capacitor (FC) converters are three well-developed multilevel converters [86]. In the CBC multilevel converter topology, there are multiple units of single-phase full-bridges or H-bridges connected in cascade on their AC side [87]. Each full-bridge or H-bridge unit in the CBC multilevel converters can be control and maintain constant with only one DC capacitor. As a result, CBC multilevel converters are especially suitable for power system applications [88]. However, for medium voltage level motor drives, each full-bridge unit in CBC multilevel converters needs a separate DC power supply for voltage balancing. Similarly, diode clamped multilevel converters require an isolated DC power sources [89], or an additional voltage balancing circuit [90]. A generalized multilevel topology was proposed to investigate the voltage balancing issues and possible solutions [91]. If clamping switches and clamping diodes are eliminated from the generalized multilevel converter topology, a FC multilevel converter is derived and it features natural balancing of the flying capacitor voltages, transformer-less operation, and equally distribution of the switching stress among semiconductor power switches [92].

After the MMC was firstly proposed in [93], it has been considered as an alternative to other multilevel converters, due to its modularity, scalability, and enhanced capability to deal with unbalanced conditions, compared to CHB topologies [94]. Two arms are required for each phase in MMC and each arm needs several submodules (multiple units of half bridges or full bridges) connected in series. Therefore, both

CBC and MMC topologies require a large quantity of active power semiconductor devices, which largely increases the converter size, weight, cost, and complexity of controls [95], [96].

Recently, the transistor clamped H-bridge (TCHB) multilevel inverter has received increasing interests due to the significantly lower number of switching devices and fewer DC sources demanded in the circuit topology [97–101], in comparison to conventional CBC (Fig. 2.1) and MMC multilevel inverters, as shown in Fig. 2.2. It can be seen that the TCHB inverter only consists of two major parts, namely, a neutral-point clamping circuit and an H-bridge. Typically, the neutral point clamping circuit is operated at carrier frequency, while the H-bridge is switched at much lower frequency. Particularly, the second phase leg of the H-bridge (i.e., S_4 and S_5 in Fig. 2.2) is generally modulated at fundamental output frequency (i.e., grid frequency). The circuit topology of a five-level TCHB inverter requires five switches and eight diodes (including anti-parallel diodes of switch), and results in reducing the converter cost and the power loss through transistors.

2.3 Design of TCHB Inverter in "SiC+Si" Hybrid Configuration

A hybrid "SiC MOSFET + Si IGBT" five level TCHB inverter was proposed to reduce system cost (2.3). The auxiliary circuit comprised of a power MOSFET switch. The capacitors used "$C1$" and "$C2$" act as two input capacitors. They split the input voltage given into two equal voltages. The neutral-point clamping

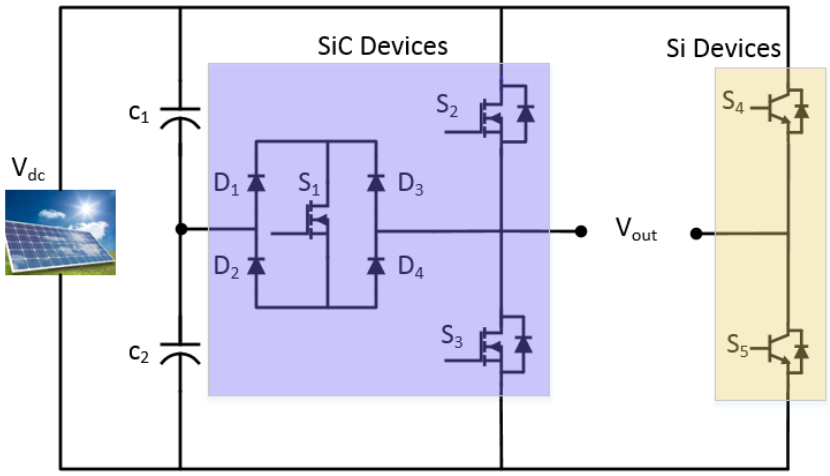


Figure 2.3: The proposed "SiC+Si" hybrid 5-level TCHB inverter. The SiC MOSFET switches S_1 - S_3 will be switching at much higher carrier frequency, and Si IGBT switches S_4 and S_5 are operated at fundamental frequency.

circuit, constituted by four diodes and one switch, generated voltage levels of $V_{in}/2$ and $(-V_{in})/2$. Accordingly, five-level voltage outputs were obtained from the TCHB inverter, namely, V_{in}, $V_{in}/2$, 0, $(-V_{in})/2$, and $-V_{in}$, by providing proper switching patterns to the switches. S_4 and S_5 were operated at fundamental frequency, while the switches S_1 - S_3 switching at much higher carrier frequency.

SiC devices have much lower switching losses than their Si counterparts due to their wide bandgap material characteristics [102, 103]. SiC MOSFETs were employed for the high-frequency switches S_1 - S_3 to further improve the efficiency of the TCHB inverter, and diodes D_1 - D_4 were constituted by SiC Schottky barrier diodes (SBD). The low-frequency switches S_4 and S_5 were still configured by the low-cost Si IGBTs. This research work confirmed the advantages and performance of this proposed hybrid TCHB inverter with simulation and experimental results.

2.3.1 Sizing of the Proposed Hybrid TCHB Inverter

The simulation modeling was based on a single-phase 5-level TCHB inverter used for PV applications, with a rated power of 500W. The nominal DC bus voltage was 120V deriving from four series connected PV panels, with each rated at 30V. An RL load was interconnected between the two phase legs (R_{load} =100Ω, L_{load} =12mH). The rated fundamental frequency was 50Hz, and the carrier frequency was set at 1kHz. Infineon IGBTs IKP08N65H5 [104] (650V/12A, integrated with soft antiparallel diodes) were selected for S_4 - S_5 and their freewheeling diodes in the proposed TCHB inverter. Also, SiC MOSFETs (Rohm SCT3120AL, 650V/15A) were selected for all the switches operated close to the carrier frequency, and SiC Schottky barrier diodes (Rohm SCS212AJHR, 650V/12A) were used for all the four clamping diodes in the TCHB inverter [105]. Based on the device thermal modeling, the comparison of the efficiency and other performance between the all-Si TCHB inverter and the proposed hybrid TCHB inverter were simulated and presented as follows.

2.3.2 Designs of PWM Modulations

Regarding the PWM strategies, the existing PWM method for the TCHB inverter has been developed and is named as single reference double carriers (SRDC) method [97], as shown in Fig. 2.4a. However, as reported in [106] such SRDC method has a higher Total Harmonic Distortion (THD) under certain conditions. Therefore, a double reference single carrier (DRSC) PWM method is adopted, which has better THD performance [106].

The modulation index is defined as follows:

$$m = \frac{V_{ref}}{2V_{Cr}}, \tag{2.1}$$

where V_{ref} and V_{Cr} represent the amplitude of the voltage reference and the amplitude of the carrier signal, respectively.

The switching period Δt can be calculated by:

$$\Delta t = \frac{2\pi f_1}{f_s}, \tag{2.2}$$

where f_1 and f_s represent the fundamental frequency and the switching frequency, respectively. In every switching period, the average voltage can be calculated by:

$$\overline{V} = 2V_s \frac{2\delta - \Delta t}{\delta}, \tag{2.3}$$

where the upper voltage V_s is over the period of δ and the $-V_s$ is for the period $(\Delta t - \delta)$, respectively.

If the reference voltage can be defined as:

$$v_{ref} = V_m sin\theta, \tag{2.4}$$

then, the volt-second area A can be obtained by integrating (2.4), when the period δ is small enough. On this basis, the switching angle can be obtained as:

$$\delta_{sw} = (\Delta t/4) + (\Delta t/4) M sin(t - \delta). \tag{2.5}$$

Such a PWM modulation method still has certain drawbacks especially at light load conditions, including the degradation of the efficiency and the THD. As a result, the DRSC PWM method was employed here, as shown in Fig. 2.4b.

Similar to the development of the SRDC PWM method, reference v_{ref1} and v_{ref2} were derived from a full sinusoidal voltage reference. The voltage reference was defined as:

$$v_{ref} = V_{ref} sin\theta, \tag{2.6}$$

$$v_{ref1} = |1 - v_{ref}|, \tag{2.7}$$

$$v_{ref2} = |2 - v_{ref}|. \tag{2.8}$$

Specifically, two rectified sine-wave reference signals and one triangular carrier signal were utilized in this modulation scheme. When the triangular carrier signal was between the two rectified sine-wave reference signals, the switch S_1 was turned on and turned off otherwise. The switch S_2 was turned on when the carrier signal was higher than the reference-1 signal in first half period or lower than the reference-2 signal in the second half period. The switch S_3 was turned on when the carrier signal was lower than the reference-2 signal in first half period or higher than the reference-1 in the second half period. As shown in Fig. 2.4b, S_4 and S_5 were operated at a fundamental frequency, while the switches S_1 - S_3 switching at a much higher carrier frequency.

2.3.3 Modeling of PV Array and MPPT Controller

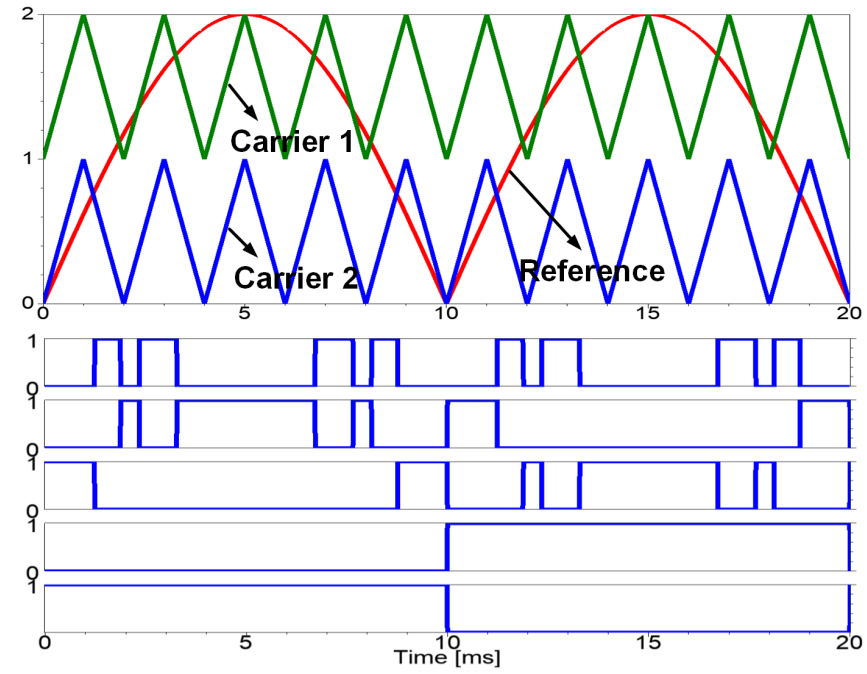
A solar array with the maximum power point tracking (MPPT) strategy was modeled based on SunTech Power STP235-20, which provided 170V/850W at the

maximum power point [107]. Fig. 2.5a showed the typical current-voltage (I-V) and power-voltage (P-V) curves of the modeled PV array at $1000W/m^2$ of irradiation and 25 °C temperature. The MPPT controller tracked the output voltage and power by following the P-V and I-V curves when there was partial shading and the solar irradiance dropped. The controller performance was studied as shown in Fig. 2.5b, where irradiance dropped from 1000 W/m^2 to 400 W/m^2 at 0.4 seconds of the simulation time. With the MPPT controller, the reference DC voltage tracked the PV output voltage, which was then provided to the single stage inverter.

2.4 Performance Evaluation

2.4.1 Efficiency Analysis

First of all, the normal output of the proposed hybrid 5-level single-phase TCHB inverter was simulated at unity modulation index, and the results were shown in Fig. 2.6. Fig. 2.6 depicted the five-level line voltage, output current of the TCHB inverter at RL load. The comparison of the conduction losses and switching losses in each semiconductor device at rated power between the all-Si TCHB inverter and the proposed hybrid TCHB inverter were simulated and shown in Fig. 2.7a-2.7b, respectively. It should be noted that the neutral point clamping circuit that was composed of four SiC diodes and one SiC MOSFET (as shown in Fig. 2.3) was updated with two anti-series-connected SiC MOSFETs in the simulations of the hybrid TCHB inverter, which was to further reduce the device losses and improve the inverter efficiency. Both the conduction and switching losses were reduced in the proposed



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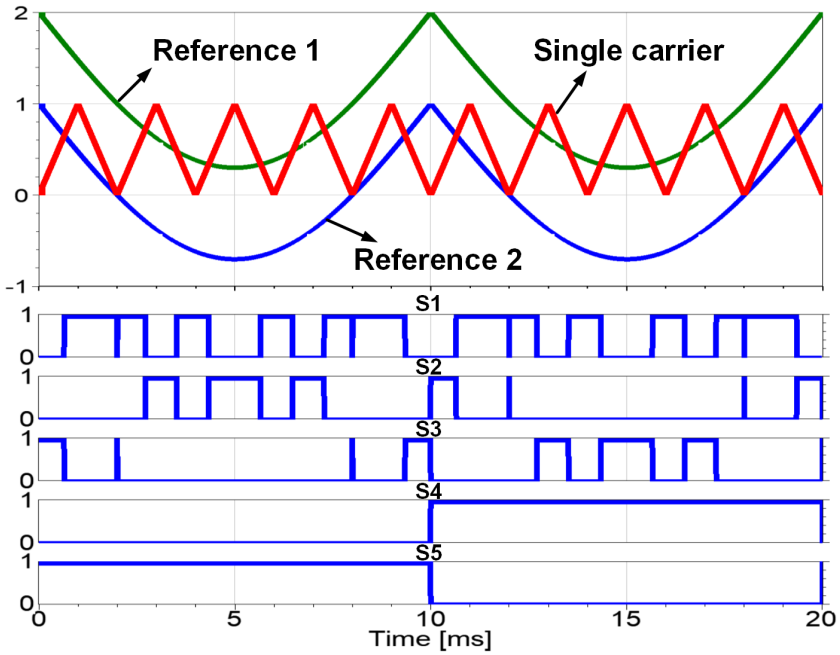
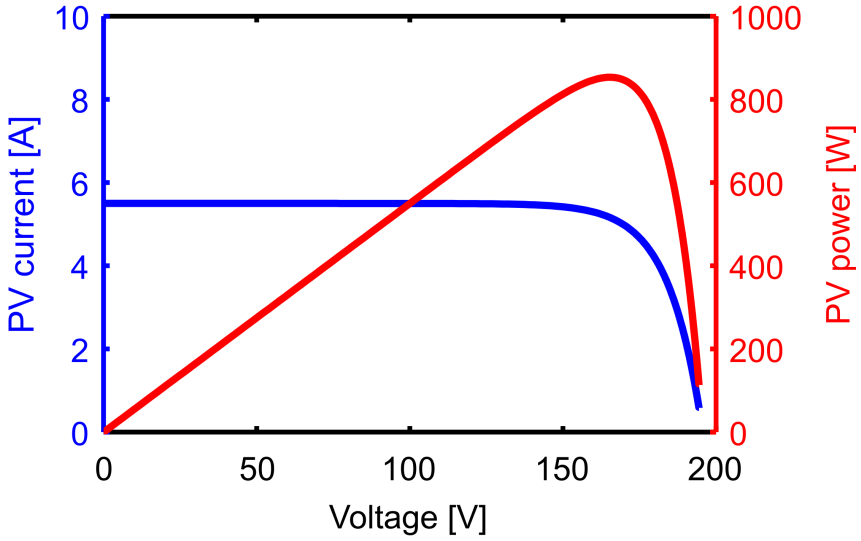


(b)

Figure 2.4: The PWM modulation strategies. (a) Single reference double carrier (SRDC). (b) Double reference single carrier (DRSC)



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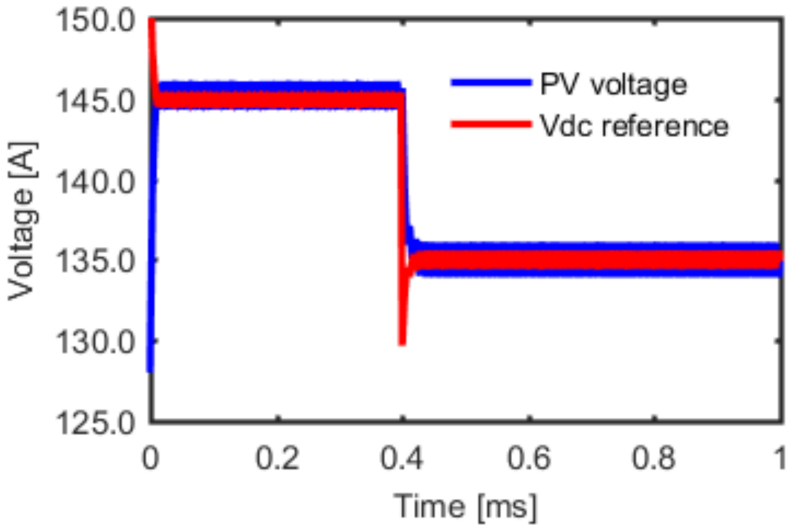


(b)

Figure 2.5: The PV characteristics and the MPPT implementation (a) The I-V and P-V characteristics. (b) The PV voltage and DC reference voltage with various irradiance.

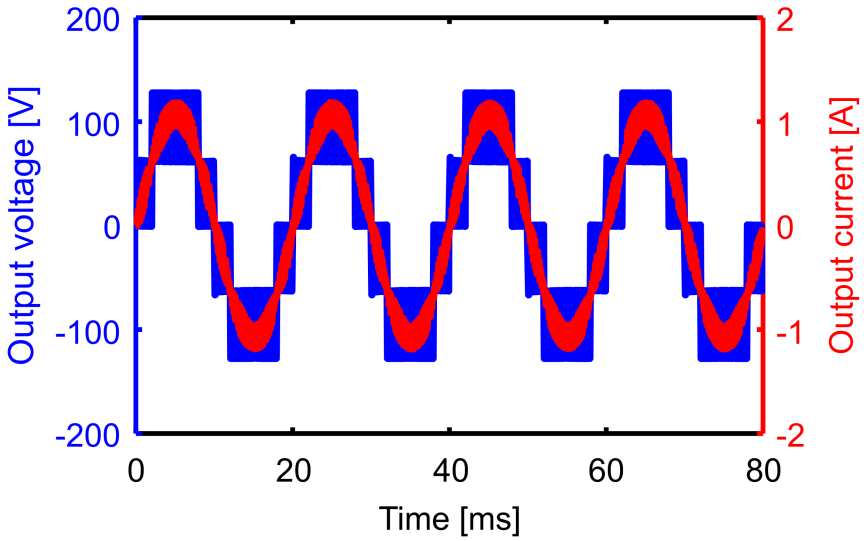


Figure 2.6: The output voltage and current with RL load.

hybrid TCHB inverter. Particularly, the switching loss in the S_1 of the convetional all-Si TCHB inverter was much larger than the one in the proposed hybrid TCHB inverter, mainly due to the high carrier frequency operation of S_1 in the all-Si inverter, which generated significant switching losses. As a result, the efficiency comparison based on the simulated device losses were shown in Fig. 2.7c, which illustrated that the proposed hybrid TCHB inverter with DRSC achieved higher peak efficiency and higher California Energy Commission (CEC) efficiency. At nominal load condition, the proposed TCHB with DRSC had a peak efficiency of 98.97%, which was 0.85% higher than the all-Si TCHB inverter and 0.17% higher than the hybrid TCHB inverter with SRDC at the same condition. As for CEC efficiency, the proposed TCHB with DRSC achieved 97.64%, which is 0.79% higher than the all-Si TCHB and 0.24% higher than than the hybrid TCHB with SRDC. Besides, the output voltage harmonics and the THD were investigated for the proposed TCHB inverter modulated by the DRSC and the SRDC PWM methods, respectively, and the simulated results were

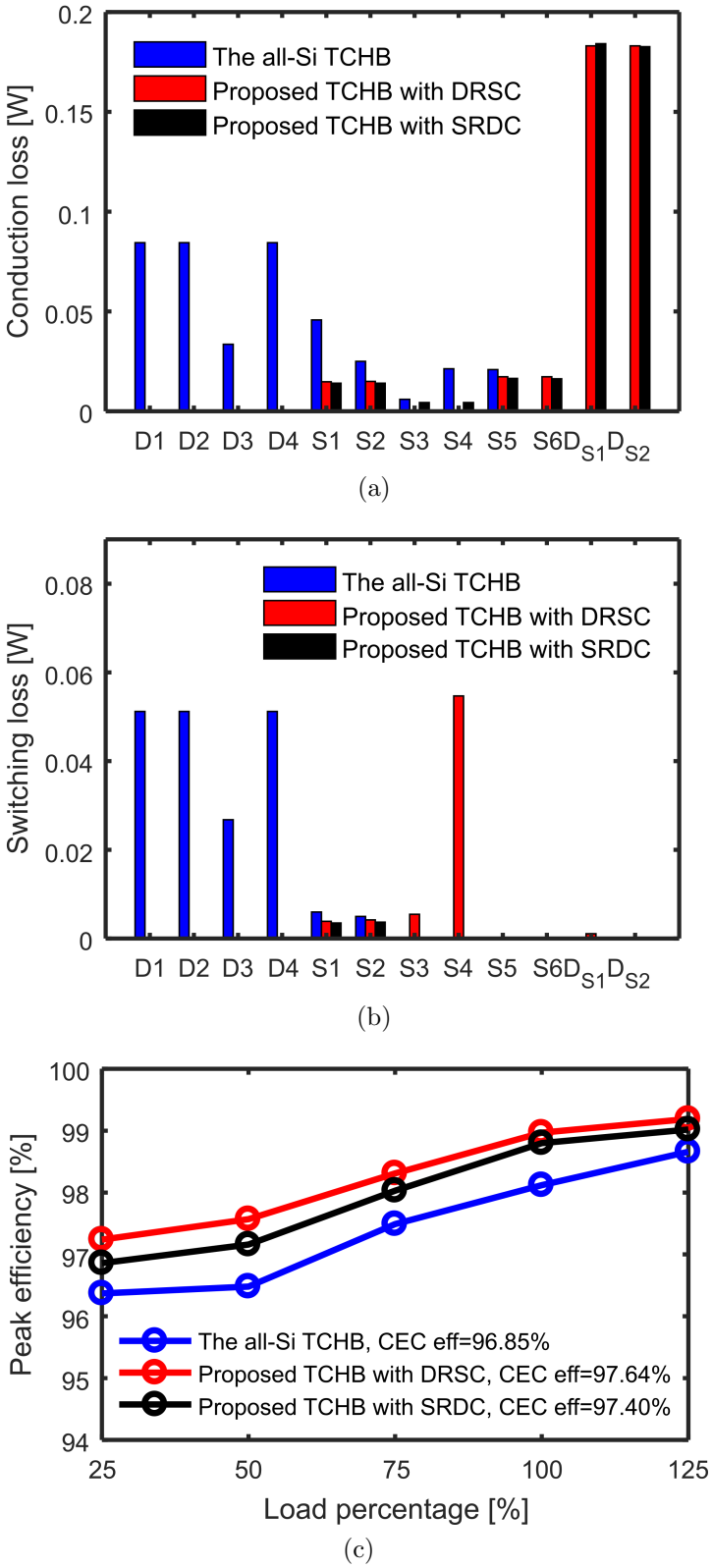


Figure 2.7: Comparison of the power device losses and inverter efficiency between the all-Si TCHB inverter and the hybrid counterpart (a) conduction losses (b) switching losses (c) inverter efficiency at various load levels.

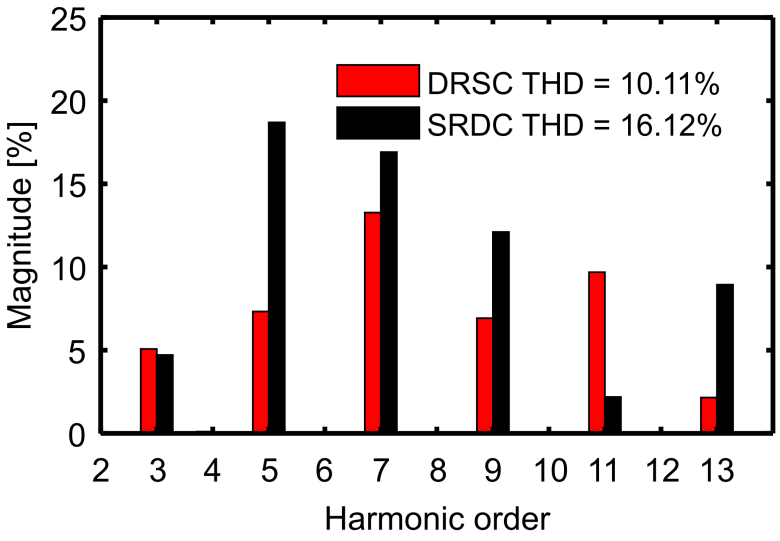


Figure 2.8: The voltage harmonics and THD at unity modulation index.

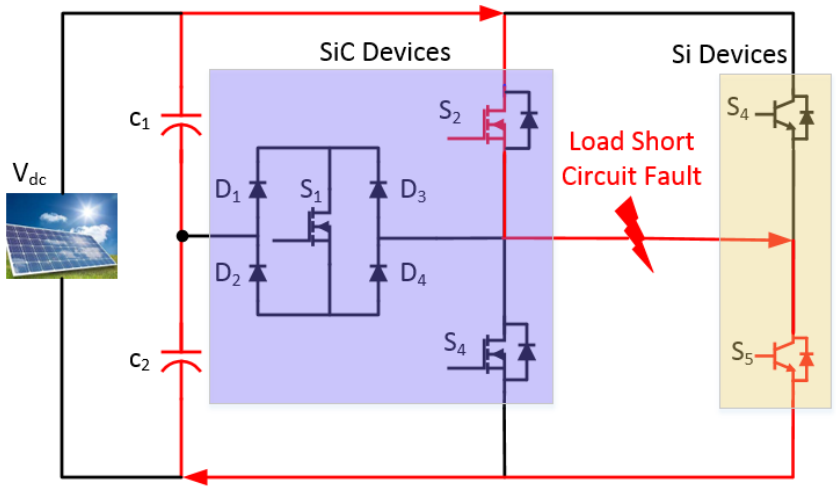


Figure 2.9: Current flow direction during a load short-circuit fault.

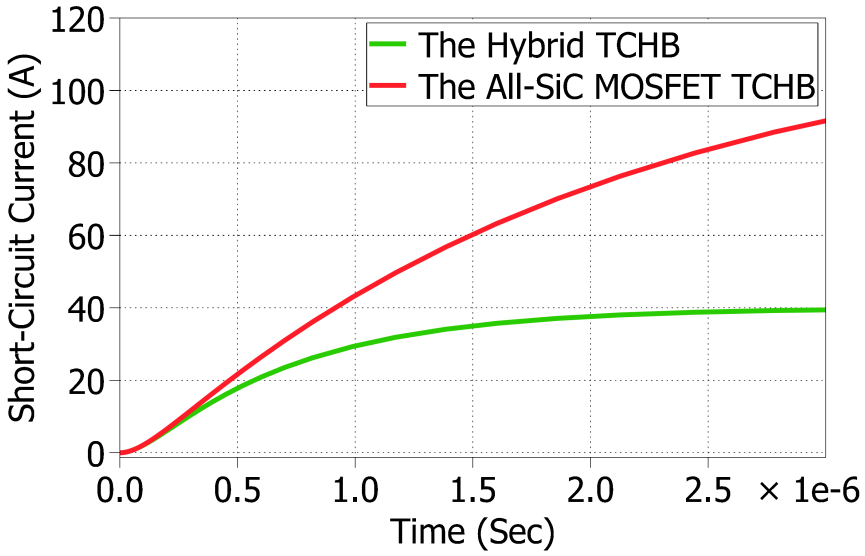


Figure 2.10: Comparison of the short-circuit current between the "SiC+Si" hybrid TCHB inverter and the all-SiC TCHB inverter.

shown in Fig. 2.8. With the conventional SRDC modulation method, the THD value for the TCHB inverter was 16.12%, while the THD value based on the DRSC PWM strategy was reduced to 10.11% under the same operating condition.

2.4.2 Simulation of Load Short-Circuit Behavior

Compared with IGBTs, which can typically withstand 10μs of short-circuit current, SiC MOSFETs have much weaker short-circuit capability, mainly due to the higher saturation current level and smaller physical size of the device die chips. Such issue becomes even worse when the commutation loop inductance of the power inverter is minimized to reduce switching losses, since it facilitates a much higher increase rate of the short-circuit current, leaving very short time for the over current protection circuit to react. However, super-fast short circuit protection requirement, such as 0.5-1μs, is very challenging and may introduce additional problems, such as EMI noise susceptibility and the like.

In this proposed 5-level TCHB inverter, the SiC MOSFETs was capable of withstanding more than 10μs of short-circuit current, without any additional short-circuit current protection scheme in the gate drivers. Such unique benefit resulted from the hybrid configuration of the SiC MOSFETs and Si IGBTs in the proposed inverter. As illustrated in Fig. 2.9, when the fault current flowing through SiC MOSFETs during a load short-circuit fault, the short-circuit current flowing through the SiC MOSFET S_2 was constrained by the faster current saturation in the IGBT S_5. The comparison between an all-SiC-MOSFET TCHB inverter and the proposed "SiC+Si" TCHB inverter under the same load short-circuit fault was simulated and shown in Fig. 2.10. As can be seen, the short-circuit current was constrained at 40 A in the proposed hybrid inverter, much lower than the short-circuit current of the all-SiC-MOSFET counterpart. In other words, the proposed hybrid TCHB inverter was able to ride through such a load short-circuit fault due to the faster saturation characteristics of the Si IGBTs in the inverter.

2.5 Conclusions

A cost-effective approach based on a hybrid utilization of SiC and Si devices was proposed to improve the efficiency of a five-level TCHB inverter. Specifically, the auxiliary neutral-point voltage clamping circuit, which was operated at high carrier frequency was configured with SiC devices, while the H-bridge inverter switched at low fundamental frequency was constituted with Si devices. Simulation and thermal models of the all-Si single-phase five-level TCHB inverter and the proposed "SiC+Si" hybrid counterpart were developed in ANSYS Simplorer. Simulation results showed

that the peak efficiency of the inverter was improved by 0.85% at nominal operating condition, compared to all-Si TCHB inverter under the same operating conditions. The CEC efficiency of the inverter was improved by 0.79% compared to all-Si TCHB inverter at the same conditions. Additionally, both the PWM methods of Single Reference Double Carrier and the Double Reference Single Carrier were investigated for the TCHB inverter, and the comparison showed that the Double Reference Single Carrier method yields higher inverter efficiency. Furthermore, compared to an all-SiC-MOSFET TCHB inverter, the proposed hybrid TCHB inverter was capable of riding through a load short-circuit fault due to the faster saturation characteristics of Si IGBTs constraining the short-circuit current in the inverter. Experimental results were presented to confirm the performance of the five-level TCHB inverter at various operating conditions.

Chapter 3

Multi-Port Converters with WBG Devices

3.1 Introduction and Problem Formulation

With the growing interest in decreasing the fossil fuel utilization and pollution, electric vehicles (EVs) have emerged as an applicable alternative to conventional gas engine vehicles[108]. The development and increasing utilization of EVs requires widely distributed charging stations due to the limited EV battery capacity [109]. However, the large scale of directly grid-connected charging stations, especially fast and super-fast charging stations, stress power grid stability and reliability with peak demand overload, voltage sag, and power gap issues [110]. Some researchers have been integrating photovoltaic (PV) generation with EV charging infrastructure [111]; however, the PV integration is still considered a minor portion of power sources for EV charging stations in researches. As for the higher demand of fast-speed charging during daytime, the rapid development of PV generation optimizes power consumption at peak hours with its adequate daytime generations. With respect to the intermittency of solar energy, a battery energy storage (BES) can be employed to regulate

Table 3.1: Standard and specification for AC and DC charging stations.

Structure	Level	Power [kW]	Voltage [V]	Current [A]
AC	L1	1.9	120	16
AC	L2	19.2	240	80
AC	L3	>20	TBD	TBD
DC	L1	36	200 - 450	80
DC	L2	90	200 - 450	200
DC	L3	240 (not finalized)	200 - 600	400

the DC bus or load voltage, balance power gap, and smooth PV power [112].

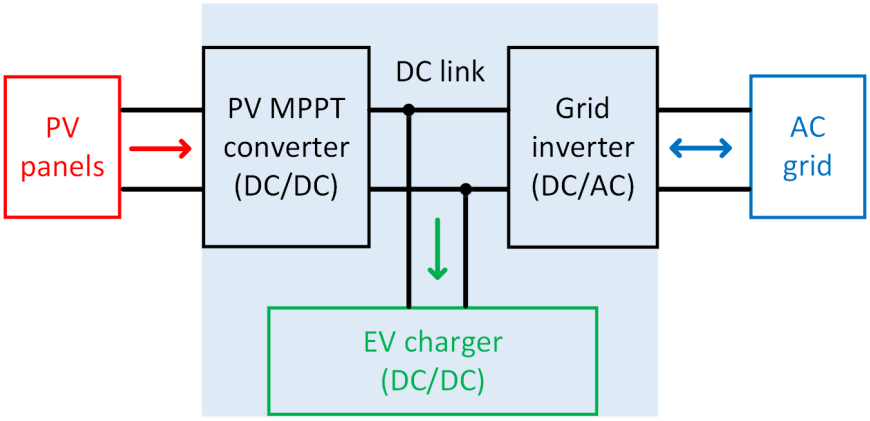
The works and contributions of this chapter include: a DC bus nonisolated structure with SiC switches was leveraged to improve efficiency and power density and minimize the power losses. The PV and BES integration, rather than the power grid, was considered as a predominant power supply for EV charging. In addition, detailed operating modes, control scheme, and the interaction among PV, BES, power grid, and EV charging were developed and investigated, in a scenario of high penetration of PV integration and widely spread EV charging infrastructures. Additionally, detailed power losses and efficiency were compared.

3.2 Literature Review

EV charging architectures can be classified into two topologies: using AC bus or DC bus [113]. The Society of Automotive Engineers (SAE) has defined EV charging methods in North America in the SAE J1772 Standard [114]. AC charging is capable of charging up to 120 V and 240 V for Level 1 and Level 2, respectively, and delivering 1.9 kW and 19.2 kW, respectively. In contrast, DC charging is rated up to 36 kW and 90 kW for Level 1 and Level 2, respectively (Table 3.2). It can be seen AC charging

methods are more suitable for on-board over night charging due to their relatively low power ratings, while DC charging is capable of leading to a fast charging or super fast charging method, which may be developed to off-board EV charging stations [115]. Multiple charging ports and may be utilized for an EV charging station. For example, PV generation and BES can both be regarded as DC current source[116]. This can be achieved by containing several DC-DC converters controlled individually; however, the traditional conversion may be limited by the power density and efficiency, bulky system size, and a high system cost [117].

A number of alternative designs have been reported that combine separate DC-DC converters into one power stage with multiple ports [118–127]. Based on port numbers, multiport converters can be classified in two-port converters [119–122], three-port converters [123–125], multiport (more than three port) converters [126, 127]. According to the existence or absence of a power transformer, multiple port converter architectures can be divided into two categories: isolated [120], [122], [124], [125], [126], [127] and non-isolated [119], [121], [123]. Compared with isolated multiport converters, nonisolated multiport converters that are usually derived from buck or boost converters may feature a more compact design, higher power density, and higher efficiency compared with isolated multiport converters[128][129]. Accordingly, a DC bus nonisolated structure with SiC switches is leveraged, to improve efficiency and minimize the power losses.



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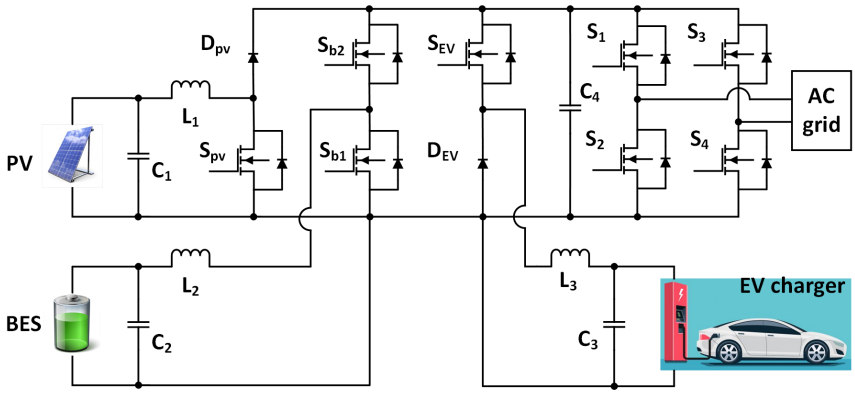


(b)

Figure 3.1: Multiport converter architectures, (a) the conventional architecture of EV charging stations integrated with PV, and (b) the proposed multiport converter based EV charging station architecture integrated with PV and BES.

3.3 Modeling and Operating Principle Design for a Non-isolated Multiport Converter

The increasing number of electrical vehicles (EVs) leads to a pressing need of widely distributed charging stations, and efficiency improvement of each charging converter by using WBG devices may result in a significant energy saving. In this chapter, a non-isolated multiport converter is designed for EV charging station integrated with PV power generation and battery energy storage system.

In the conventional architecture of DC bus charging station with PV integration

(Fig. 3.1a), all the three power sources, including PV and EV charger unidirectional sources, and AC grid bi-directional source, are all connected through three separate converters. The proposed DC bus charging station (Fig. 3.1b), consists of one more bi-directional power source BES sharing the same DC bus. The BES is utilized to maintain the DC link voltage and balance power surplus/insufficiency from the PV (Fig. 3.4). With this configuration, the function and operating modes can be discussed as follows in detail.

3.3.1 Mode 1: PV to EV

In this mode, the switches S_{pv}, S_{b1}, and S_{b2} are turned off while S_{EV} is turned on (Fig. 3.2a). Therefore, PV directly delivers power to the load, as shown in Fig. 3.2a. The differential equations in this stage can be expressed as follows:

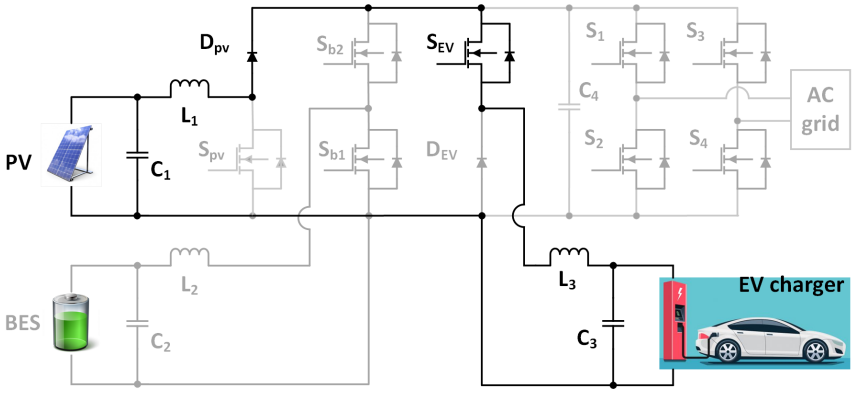
$$i_{PV} = C_1 \frac{dv_{C1}}{dt} + i_{EV}, \tag{3.1}$$

$$C_2 \frac{dv_{C2}}{dt} = \frac{v_{Bat} - v_{C2}}{r_b} - i_{L2}, \tag{3.2}$$

$$i_{EV} = C_3 \frac{dv_{C3}}{dt} + \frac{v_{EV}}{R_{EV}}, \tag{3.3}$$

$$v_{C1} - v_{C3} = L_3 \frac{i_{L3}}{dt}, \tag{3.4}$$

$$L_2 \frac{i_{L2}}{dt} = -v_{C2}, \tag{3.5}$$



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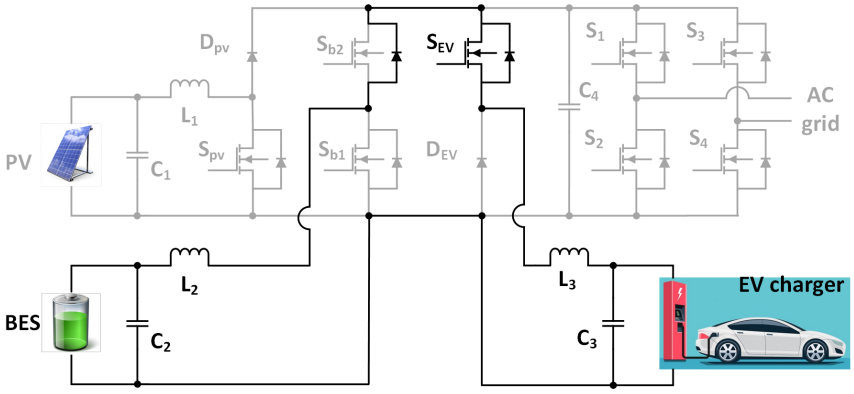

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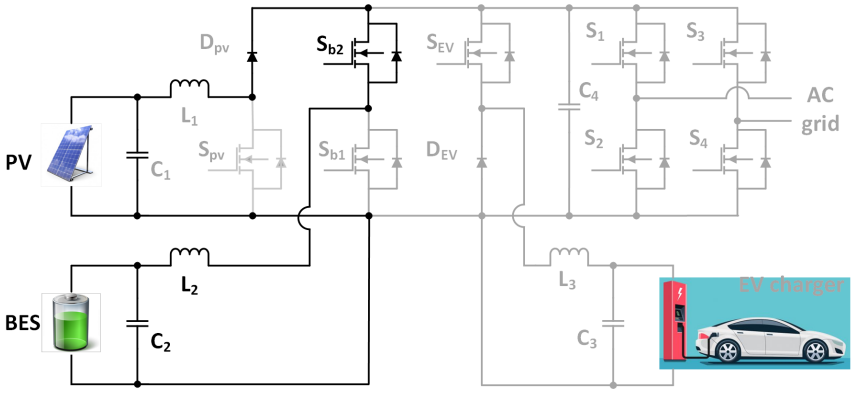


(c)

Figure 3.2: Multiport converter operating modes, (a) PV supplies EV charging when solar energy is sufficient, (b) BES supplies EV charging during PV intermittent, and (c) PV charges BES when solar generation is surplus.

where C_1, C_2, C_3, L_1, L_2, L_3, and r_b represent the capacitance of the PV port capacitor, the capacitance of the BES port capacitor, the capacitance of the EV port capacitor, the inductance of the PV port inductor, the inductance of the BES port inductor, the inductance of the EV load port inductor, and the equivalent resistance between v_{Bat} and C_2, respectively, as shown in Fig. 3.1b; i_{PV}, i_{EV}, i_{L2}, and i_{L3} represent the output current from PV panels, the current of EV load, the current through inductor L_2, and the current through inductor L_3, respectively; v_{C1}, v_{C2}, v_{C3}, v_{Bat}, and v_{EV} represent the voltage across capacitor C_1, the voltage across C_2, the voltage across C_3, output voltage from BES, and the charger voltage, respectively. The duty cycle for the switch S_{pv} can be obtained with:

$$\frac{V_{DC}}{V_{PV}} = \frac{1}{1 - D_{pv}}, \tag{3.6}$$

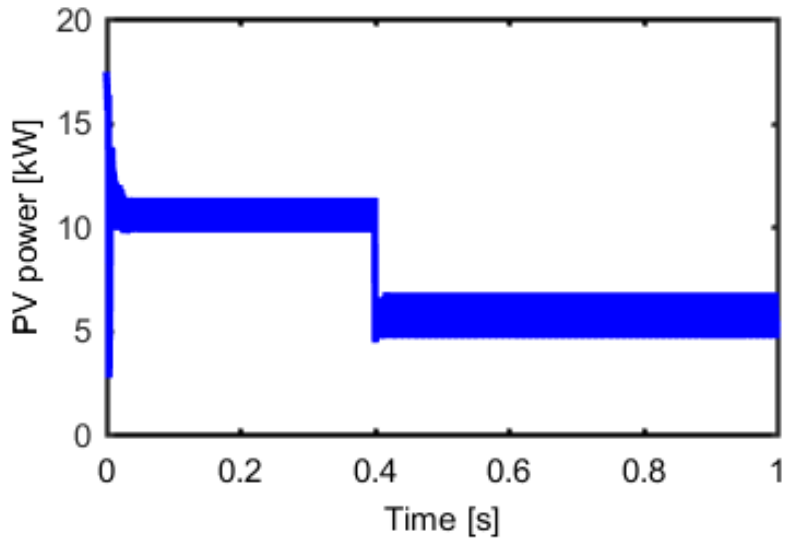
where V_{DC}, V_{PV}, and D_{pv} represent the DC link voltage, voltage of PV array, and duty cycle of switch S_{pv}, respectively.

3.3.2 Mode 2: BES to EV

When S_{pv} and S_{EV} are turned on while S_{b1} and S_{b2} are turned off, BES is discharged to the EV load, as shown in Fig. 3.2b. The differential equations in this mode can be expressed as follows:

$$i_{PV} = C_1 \frac{dv_{C1}}{dt}, \tag{3.7}$$

$$L_2 \frac{i_{L2}}{dt} = v_{DC} - v_{C2}, \tag{3.8}$$



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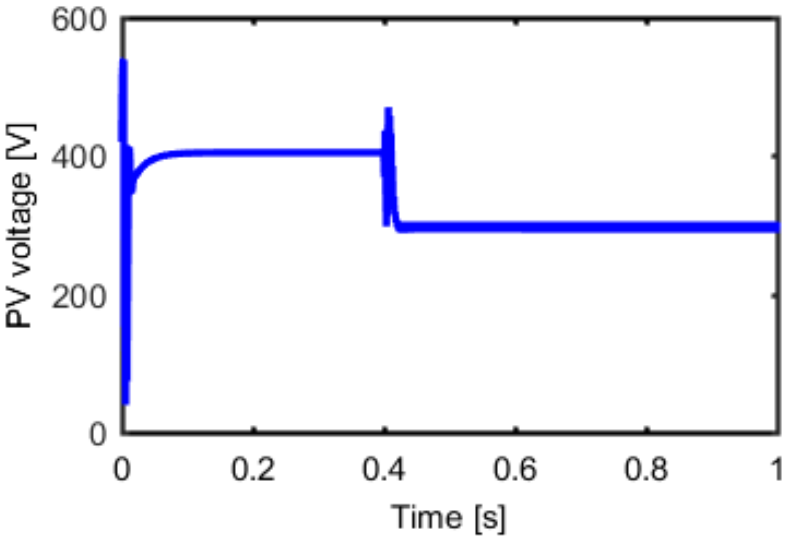


(b)

Figure 3.3: PV outputs when irradiance drops from 1000 to 500 W/m^2, (a) the output power from the PV panels, and (b) the output voltage of the PV panels.

$$v_{DC} - v_{C3} = L_3 \frac{i_{L_3}}{dt}, \tag{3.9}$$

$$C_2 \frac{dv_{C2}}{dt} = \frac{v_{Bat} - v_{C2}}{r_b} - i_{L2}, \tag{3.10}$$

$$i_{EV} = C_3 \frac{dv_{C3}}{dt} + \frac{v_{EV}}{R_{EV}}, \tag{3.11}$$

where v_{DC} refers to DC link voltage, which equals to the voltage across capacitor C_4. The duty cycle for switch S_{b1} can be obtained with:

$$\frac{V_{DC}}{V_{Bat}} = \frac{1}{1 - D_{b1}}, \tag{3.12}$$

where V_{DC}, V_{Bat}, and D_{b1} represent the DC link voltage, voltage of BES, and duty cycle of switch S_{b1}, respectively.

3.3.3 Mode 3: PV to BES

When S_{b2} is turned on while S_{b1}, S_{pv} and S_{EV} are turned off, BES is charged from the PV surplus energy, as shown in Fig. 3.2c. The differential equations in this mode can be expressed as follows:

$$i_{PV} = C_1 \frac{dv_{C1}}{dt} - i_{L2}, \tag{3.13}$$

$$L_2 \frac{i_{L2}}{dt} = v_{C1} + v_{DC} - v_{C2}, \tag{3.14}$$

Table 3.2: The operating modes for EV charging

S_{pv}	S_{b1}	S_{b2}	S_{EV}	Power flow
off	off	off	on	PV to EV
off	off	on	off	PV to BES
on	off	off	on	BES to EV
–	on/off	off/on	on	Grid to EV
off	off	off	off	PV to grid

$$L_3 \frac{i_{L3}}{dt} = v_{DC} - v_{C3}, \tag{3.15}$$

$$C_2 \frac{dv_{C2}}{dt} = \frac{v_{Bat} - v_{C2}}{r_b} - i_{L2}, \tag{3.16}$$

$$i_{EV} = C_3 \frac{dv_{C3}}{dt} + \frac{v_{EV}}{R_{EV}}, \tag{3.17}$$

The duty cycle for the switch S_{b2} can be obtained with:

$$\frac{V_{Bat}}{V_{DC}} = D_{b2}, \tag{3.18}$$

where D_{b2} represents the duty cycle of the switch S_{b2}.

3.3.4 Other Modes: PV to BES, Grid to EV, and PV to Grid

The operating principle of other modes including PV to BES, grid to EV, and PV to grid, are illustrated in Table 3.3.4. Besides, the differential equations can be similarly expressed with the same analysis method in Modes 1 to 3. The detailed simulation analysis will be provided in the following section.

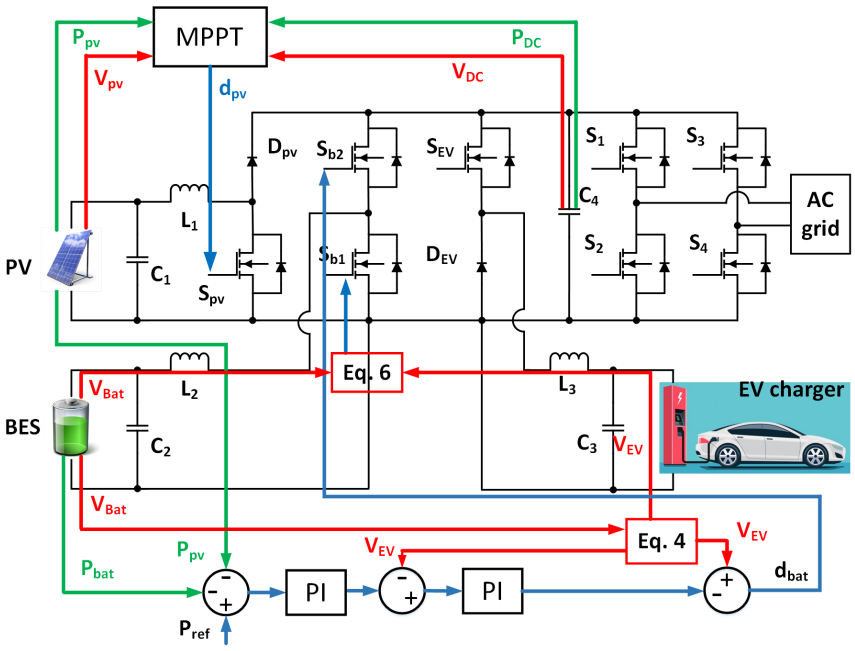
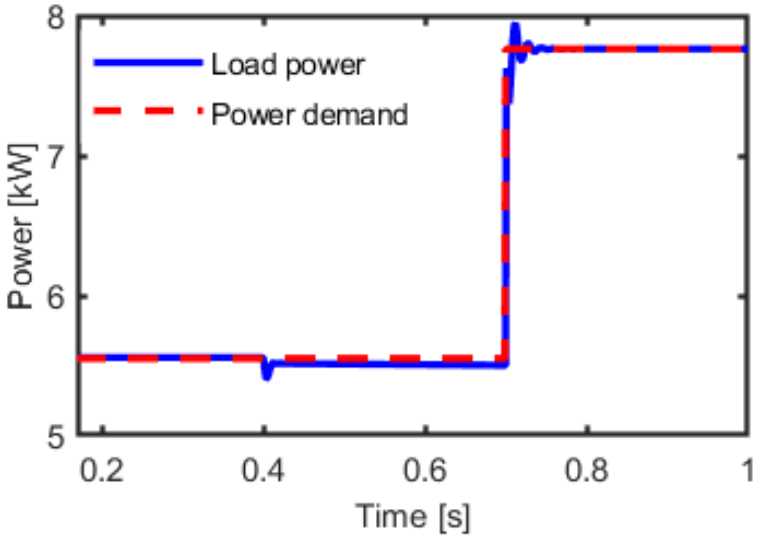


Figure 3.4: The block diagram for the BES controller and the PV controller with MPPT.

3.4 Simulation Results

To evaluate the proposed charging station functions and control schemes, a simulation model following the structure in Fig. 3.1b was established in ANSYS Simplorer. The PV array was modeled with Suntech STP235-20-Wd[107], with 14 strings in series and 5 strings in parallel. For the open circuit, the modeled PV array was able to supply $16kW$ $500V$ to feed the EV charger and a MPPT controller was developed to extract the maximum power from PV panels while maintains a constant DC voltage.

For the BES controller, the objective was to regulate the power gap and support the load voltage (Fig. 3.4). When the solar was sufficient, EV charging was supplied from PV panels. If the PV generation was surplus, BES would be charged and consumed locally. If PV was insufficient such as partial shading and other intermittent conditions, BES would start to discharge and fill in the power gap between PV and



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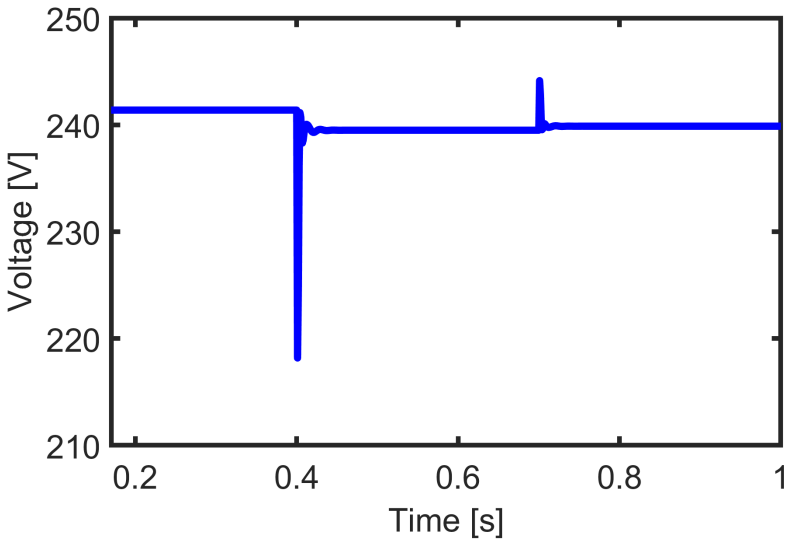


(b)

Figure 3.5: The simulation results of EV charging, (a) the demand and consumed power of EV charging, (b) the terminal voltage of the EV charger.

EV charging.

A case of this control scheme was simulated with ANSYS Simplorer. At 400ms of the simulation time, the irradiance dropped from $1000k/W^2$ to $500k/W^2$, and the output power of the PV panels dropped from $11kW$ to $5.7kW$ at $425V$ (Fig. 3.3), with the MPPT strategy implemented. At 700ms of the simulation time, EV charging demand suddenly went up from $5.7kW$ to $7.7kW$.

In this scenario, between the simulation time of 0 to 400ms, the EV charging demand was low while the PV generation was sufficient. Therefore, both PV-to-EV and PV-to-BES modes were triggered, and the surplus PV generation charged the BES. Between the simulation time of 400ms to 700ms, the PV panels could provide $5.7kW$, which met the EV charging amount. As a result, the system was operated in PV-to-EV mode and no BES charging/discharging was required. After the charging demand increased at 700ms, the PV panels were not able to supply all the required $7.7kW$ charging power under the condition of $500k/W^2$ irradiance. Therefore, the BES started to discharge and supply EV charging with $2kW$ and provided voltage support as shown in Fig. 3.6.

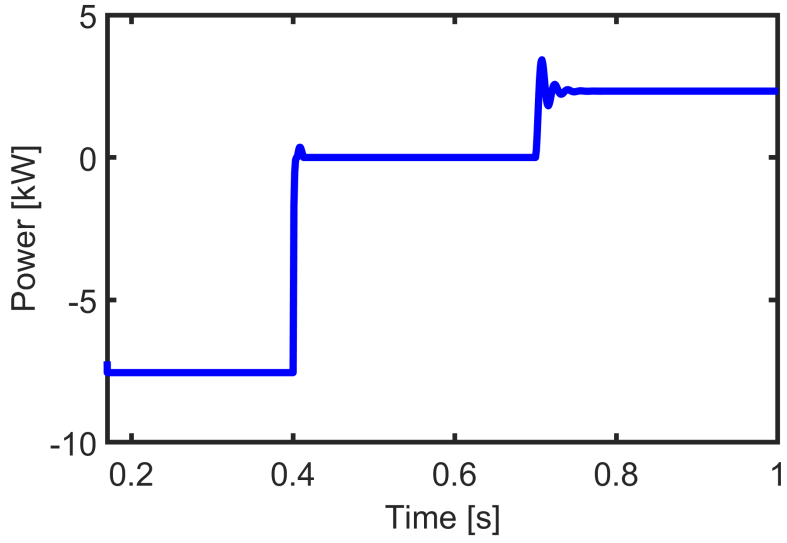
Additionally, to improve the efficiency and power density of the multiport converter, SiC MOSFETs (CREE 900V/36A C3M0065090D [130]) were utilized. The comparison of the conduction losses and switching losses in each semiconductor device for different operating modes at different load percentage was simulated, as shown in Fig. 3.7. Both the conduction (Fig. 3.7a) and switching losses (Fig. 3.7b) were reduced in the proposed SiC based EV charging stations. Particularly, the switching loss of the conventional Si converters was much larger than the one in the proposed

SiC counterparts. As a result, the efficiency comparison based on the simulated device losses were shown in Fig. 3.8. At nominal load condition, the proposed EV charging station had an efficiency of 98.41% for PV-to-EV mode, which was 5.67% higher than the conventional Si (Infineon 900V/36A IPW90R120C3 Si MOSFET [131]) based converter at the same condition. For PV-to-BES mode at nominal rating, the proposed EV charging station had an efficiency of 98.37%, which was 4.46% higher than the conventional Si based converter under the same condition. Under the condition of the nominal rating of the BES-to-EV mode, the efficiency of the proposed charging station was 6.00% higher than the Si counterpart.

3.5 Conclusions

A multiport converter based EV charging station with PV and BES was proposed. A BES controller was developed to regulate the voltage sag, and balance the power gap between PV generation and EV charging demand. With the proposed control design, BES starts to discharge when PV was insufficient for local EV charging, and started to charge when PV generation was surplus or power grid was at "valley" demand, such as during nighttime. As a result, the combination of EV charging, PV generation, and BES enhanced the stability and reliability of the power grid. Different operating modes and their benefits were investigated and then, simulation and thermal models of the multiport converter based EV charging stations and the proposed SiC counterpart were developed in ANSYS Simplorer. Simulation results showed that the efficiency was improved by 5.67%, 4.46%, and 6.00%, respectively, for PV-to-EV mode, PV-to-BES, and BES-to-EV mode at nominal operating condition,

compared to Si based EV charging stations under the same operating conditions.



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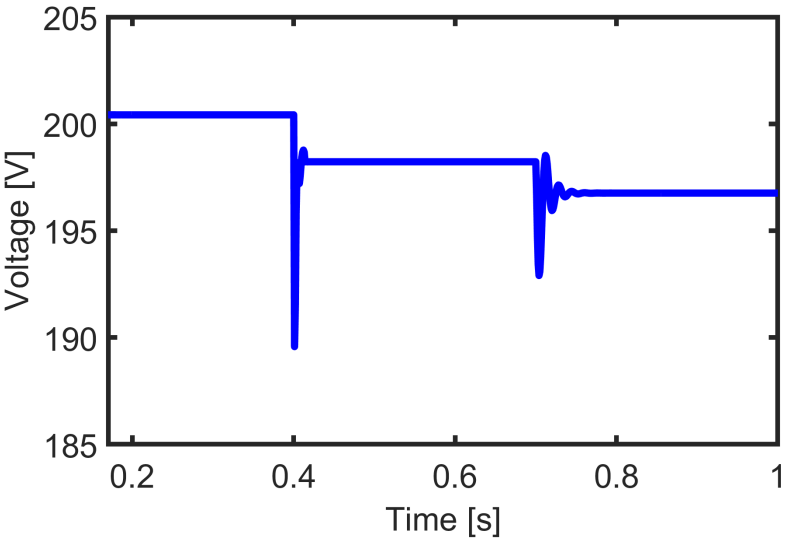

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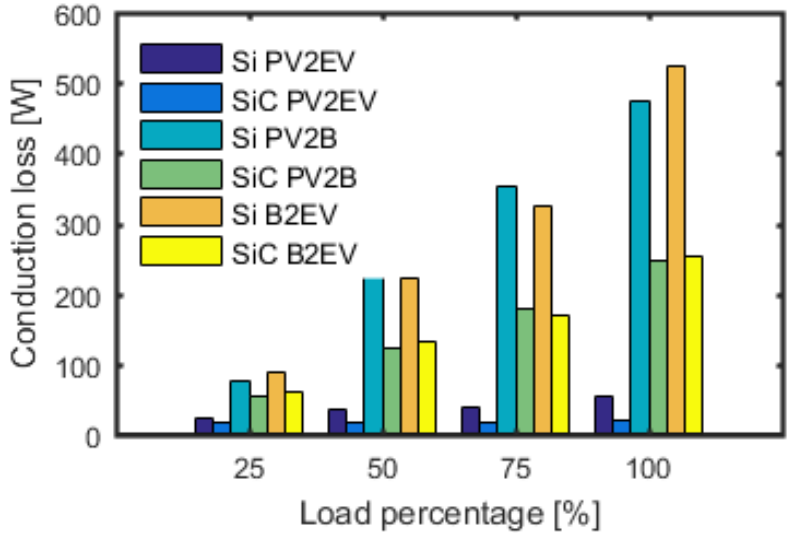
Figure 3.6: The simulation results of the BES, (a) the output power from BES, (b) the terminal voltage of the BES.



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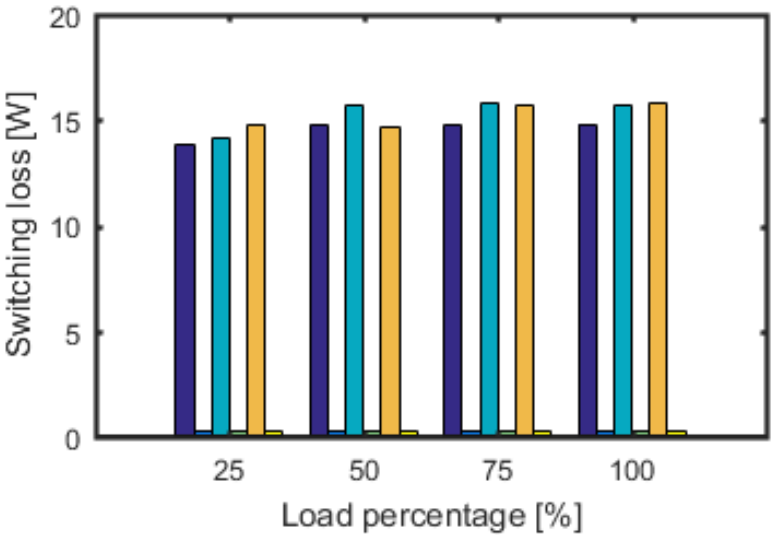


(b)

Figure 3.7: Comparison of the power device losses between the Si converters and SiC counterpart, at various load percentage and different operating modes (PV to EV, PV to BES, and BES to EV), (a) conduction losses, (b) switching losses with the same labels and orders as in (a).

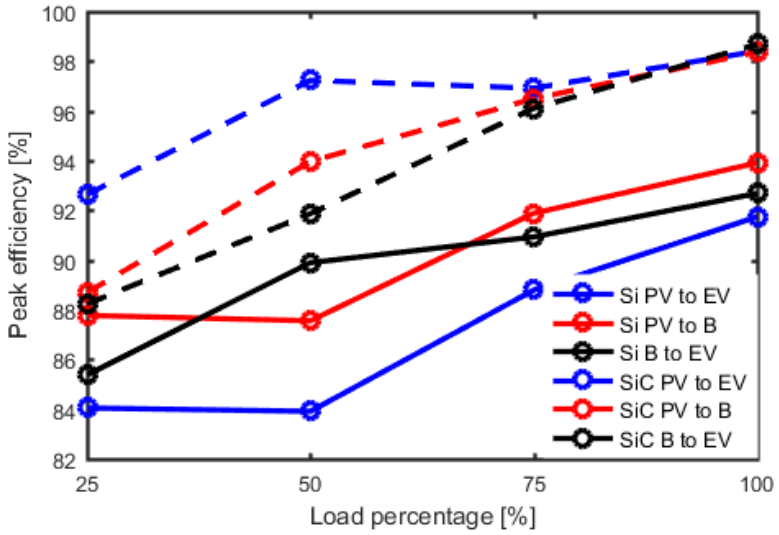


Figure 3.8: Comparison of the peak efficiency between the Si converters and SiC counterpart, at various load percentage and different operating modes (PV to EV, PV to BES, and BES to EV).

Chapter 4

Inverters and Controls for Low-Inductance Motor Drives

4.1 Introduction and Problem Formulation

Slotless and coreless machines with low inductance and low core losses are attractive for high speed and high power density applications [132], [133]. However, with pulse width modulation (PWM) inverters, low inductance machines may exhibit high current harmonics. Though the DC bus utilization is improved at high speed, PWM voltage produces considerable harmonics in machine currents, degrading the efficiency and reliability of drive systems [134].

With the increase in fundamental frequency, typical drive implementations using conventional silicon-based devices are performance limited and also produce large current and torque ripples for low inductance machines. Therefore, filters, such as LC and LCL filters have to be implemented to reduce PWM reflected current harmonics [46]. LC filters do not contain any resistive components, so the voltage/current waveform distortion appears especially in LC resonant areas, and leads to circulating currents between the inverter and the filter [47]. Active damping compensation and

LCL filters have been proposed to address the aforementioned issues. However, the cost, weight, and volume added by the filters still need to be reduced.

Wide band-gap (WBG) semiconductor devices, such as SiC MOSFETs, enable the PWM frequency capability of 50 to 100 kHz or even higher, which keeps the current ripple within acceptable limits for low inductance machine drives [48]. WBG semiconductors outperform silicon counterparts in terms of on-resistance. Employing one H-bridge for each phase is the most common drive topology, which offers the highest per-phase DC bus utilization but at the same time the highest number of devices and cost [135]. Additionally, the increase of the switching speed in power devices increases the power density of power electronic converters as it reduces the weight and volume of passive components [51].

To further improve the compactness, reduce cost, and enhance the robustness, single-phase and 2-phase machines have been drawing increased attention [58]. Single-phase and 2-phase motors work well in constant-speed applications but show difficulties when variable-speed performance is needed [59]. To improve the variable-speed capability of 2-phase machines, it becomes necessary to explore alternative inverter topologies, associated modulation schemes and the optimal use of WBG devices in 2-phase machine drives [60], [61].

In this chapter, two drive configurations for 2-phase low inductance machines were studied in terms of the operating capability, survivability, and cost (Fig. 4.1). For the proposed dual H-bridge drive topology, each phase was electrically isolated and driven by one H-bridge and a separate DC supply. In the case of failure in one

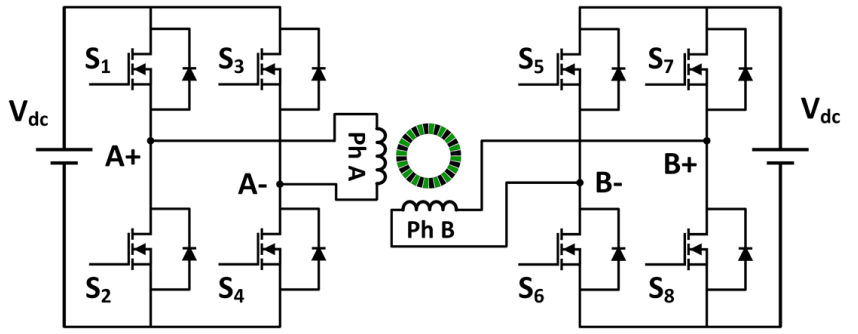
phase, the other phase was still capable of supplying the motor. However, the dual-topology consisted of a large number of switching devices, two capacitors with high capacitances, and multiple supplies, which might increase the system cost. A 3-leg topology was proposed and studied as a cost-effective solution. A noticeable limitation of 3-leg inverters in driving 2-phase motors was that the root mean square (RMS) value of the common leg current was higher than those of the other two legs, which necessitated the utilization of switches with higher current ratings at least in one leg. The low inductance machine under study was a SMC axial-flux permanent-magnet (AFPM) machine and another benefit of the 2-phase motor was the electrically and magnetically isolation between two phases.

4.2 Converter Topology and Modulation Development

4.2.1 Modulation for Dual H-bridge Inverter

The first topology, referred to as the dual H-bridge inverter, consists of two independent H-bridges and two separate DC sources, as illustrated in Fig. 4.1a. Each phase winding of the 2-phase machine is supplied by a single H-bridge, which provides full electrical isolation between two phases. The two phase windings are also elaborate on the connection between 90 degree of separation and magnetic isolation. This drive configuration is expected to have the maximum reliability considering the inherent electrical and magnetic isolation between two phases.

To drive the 2-phase machine with the dual H-bridge inverter topology, suitable



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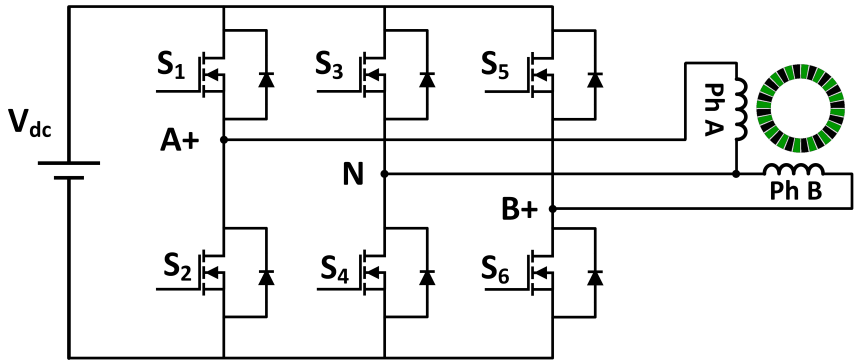


(b)

Figure 4.1: Proposed inverter topologies for 2-phase very low inductance machines considered in the study: (a) a dual H-bridge inverter supplied by two separate DC sources, which offers full isolation between two phases and maximum output capability, (b) a three-leg inverter with one leg shared by two phases, which has a cost advantage of 1/4 fewer switches and one DC supply.

modulation schemes have to be derived. To produce the rotating magnetic field required for torque production, the fundamental components of the inverter output voltages are required to have the same amplitude and a phase shift of 90 electrical degrees. Assuming the amplitude of the inverter output voltage are V, the fundamental components of the two phase voltages for the dual H-bridge inverter are:

$$\begin{cases} v_{PhA} &= v_{A^+O} - v_{A^-O} \\ &= mV_{dc}\cos(\omega t - \varphi), \\ v_{PhB} &= v_{B^+O} - v_{B^-O} \\ &= mV_{dc}\cos(\omega t - \varphi - \pi/2), \end{cases} \tag{4.1}$$

where v_{PhA} and v_{PhB} are the terminal voltages of phase A and phase B windings, respectively. O is the middle point of the DC bus. v_{A^+O} and v_{B^+O} represent the voltage of A^+ and B^+ to O, respectively. m and V_{dc} are the modulation index and DC voltage amplitude, respectively. The angular frequency of the 2-phase machine ω is obtained from $\omega = 2\pi f$, and φ is the initial phase of the reference wave. Equation (4.1) indicates the carrier-based sinusoidal PWM (SPWM) scheme can be used for the dual H-bridge inverter.

4.2.2 Modulation for 3-Leg Inverter

The second topology is a 3-leg inverter (Fig. 4.1b). Each phase winding of the machine is supplied by one H-bridge and one leg is shared by two phases. This change reduces the number of required WBG devices by 1/4 and is more attractive in terms of the system cost. Compared with the dual H-bridge, the 3-leg topology is more susceptible to failures of power supply, in which case both phase windings are out of power and fault-tolerant operation becomes impossible.

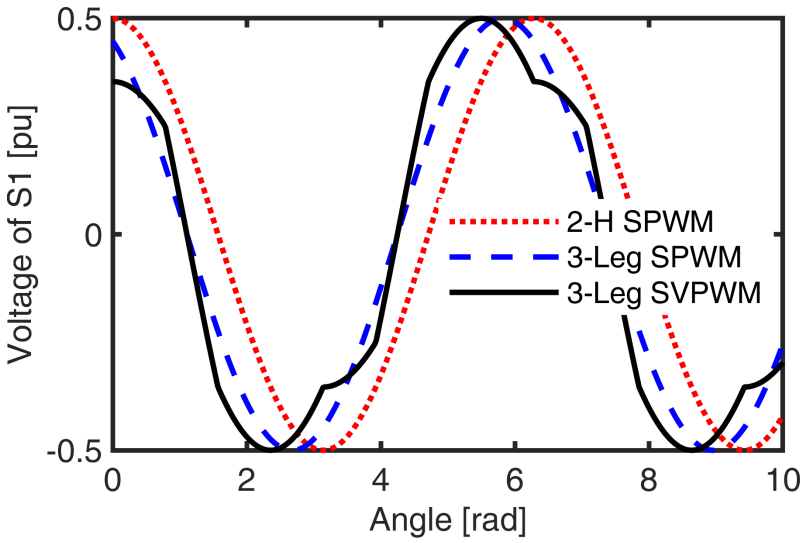


Figure 4.2: Reference signals of the two inverter topologies with various modulation schemes (full modulation).

The fundamental components of the two phase voltages for the 3-leg inverter are similar to those expressed by Equation (4.1) except that "A^-" and "B^-" are replaced by N:

$$\begin{cases} V_{PhA} &= V_{A+O} - V_{NO} \\ &= mV_{dc}\cos(\omega t - \varphi), \\ V_{PhB} &= V_{B+O} - V_{NO} \\ &= mV_{dc}\cos(\omega t - \varphi - \pi/2). \end{cases} \tag{4.2}$$

The solution that can achieve the maximum reference amplitude is:

$$\begin{cases} V_{A+O} &= m\left(\frac{V_{dc}}{2}\right)\left[\frac{2}{3}\cos(\omega t) - \frac{1}{3}\sin(\omega t)\right], \\ V_{NO} &= m\left(\frac{V_{dc}}{2}\right)\left[-\frac{1}{3}\cos(\omega t) - \frac{1}{3}\sin(\omega t)\right], \\ V_{B+O} &= m\left(\frac{V_{dc}}{2}\right)\left[-\frac{1}{3}\cos(\omega t) + \frac{2}{3}\sin(\omega t)\right]. \end{cases} \tag{4.3}$$

Equation (4.3) indicates both the carrier-based SPWM and space vector PWM (SVPWM) can be used for the 3-leg inverter. In the case of SVPWM, the phase voltage is not symmetrical due to the unbalance in V_{A+O}, V_N and V_{B+O}, as shown in Fig. 4.2.

4.2.3 Converter Modeling and Filter Sizing for Machine Drive

To meet the voltage, power, and switching frequency requirements, a DC input voltage of 60 Vdc to the drive converter is required, and a phase current of 4.4 Arms at 3000 rpm. A CREE SiC evaluation board KIT8020CRD8FF1217P-1 has been selected for the switching devices in the inverter (Fig. 4.3). The CREE evaluation board takes up to 10 Arms continuous input current and up to 20 kW. The switching frequency is capable of operating up to 300kHz, which leaves enough margin for system transient and operating requirements.

Moreover, filter sizing is developed and determined. According to the machine designs and simulation results, the input voltage ripple and transient voltage ripple are chosen as 2% and 3% of the input voltage, respectively. The current and voltage have relationships with the filter capacitors and inductors, as described in Equations (4.4) and (4.5). The required input capacitance is no smaller than 680 μH; output inductance and output capacitance should be 400 μF and 300 μF, respectively:

$$i_C = C\frac{dv}{dt}, \tag{4.4}$$

$$v_L = L\frac{di}{dt}. \tag{4.5}$$

Figure 4.3: The prototype inverter developed as part of this PhD research based on the Wolfspeed SiC evaluation board KIT8020CRD8FF1217P-1.

4.3 Modeling of Two-phase AFPM Machine and Motor Drive Controls

An equivalent circuit model for the 2-phase AFPM machine was first modeled in MATLAB/Simulink (Fig. 4.4a), based on equations (4.3 - 4.8):

$$T_{em} = N\phi i_q = \frac{p}{2}\lambda_{fd} i_q, \tag{4.6}$$

$$J\frac{d\omega_m}{dt} = T_{em} - T_L, \tag{4.7}$$

$$\lambda_s = v_s - \lambda_s \omega_m - R_s i_s. \tag{4.8}$$

In addition, dq to ab and ab to dq transformations were modeled (Fig. 4.4c and

Table 4.1: Parameters for the 2-phase motor and drives prototype implemented for the experimental study.

Parameters	Value	Per unit
Number of poles, p	10	-
Slots, s	12	-
Inertia of rotor, J	0.0421 kg.m^2	-
Phase inductance, L_s	4.95 mH	0.09
Phase resistance, r_s	0.735 Ω	0.04
Rated torque, T	1.12 Nm	1
Rated speed, ω_n	3,450 rpm	1
Open-circuit back EMF	9.47 Vrms/krpm	1
Rated current, I_n	4.4 Arms	1
Rated power, P_{rated}	0.5 hp	1
DC bus voltage, V_{dc}	60 V	-
Switching frequency, f_w	10 kHz	-

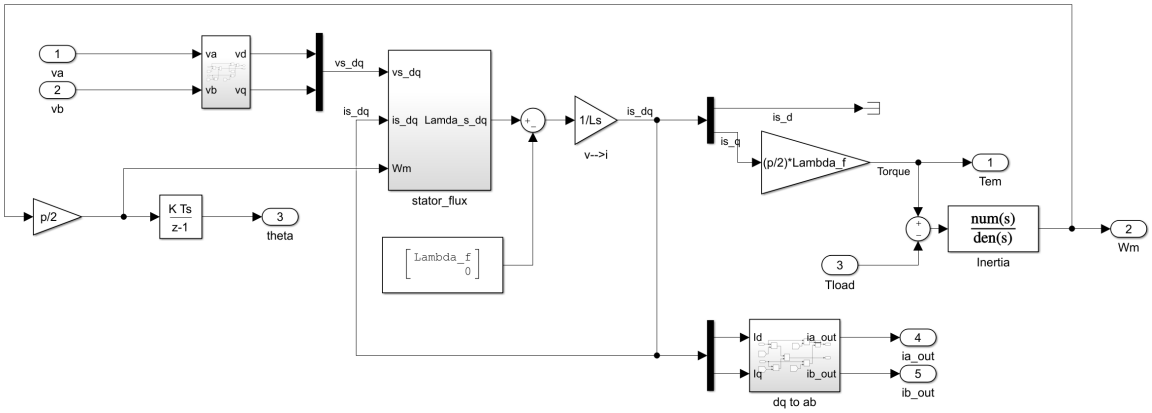
4.4d, respectively), based on the calculation equations (4.10) and (4.9):

$$\begin{cases} v_a = v_d \times \sin\theta + v_q \times \cos\theta, \\ v_b = -v_d \times \cos\theta + v_q \times \sin\theta. \end{cases} \tag{4.9}$$

$$\begin{cases} v_d = v_a \times \cos\theta + v_b \times \sin\theta, \\ v_q = -v_a \times \sin\theta + v_b \times \cos\theta, \end{cases} \tag{4.10}$$

The 2-phase AFPM SMC machine was designed and manufactured by Regal Beloit Corporation with 12 slots, 10 poles, 4.95 mH phase inductance, 0.735 Ω phase resistance, and rated at 1.12 Nm, 4.4 Arms, 0.5 hp, and 60Vdc. Ratings and parameters of the 2-phase SMC motor were listed as in Table 4.1.

Based on the mathematical modeling of the machine and drive system, converter ratings and current loop PI controller were developed in simulation as well. Firstly,



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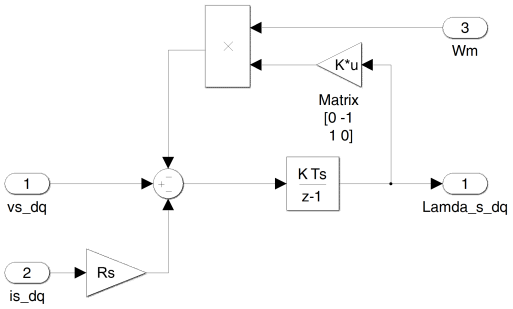

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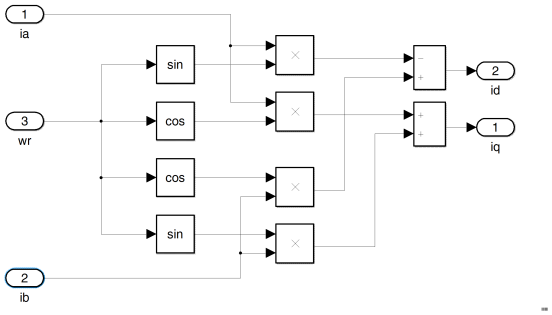

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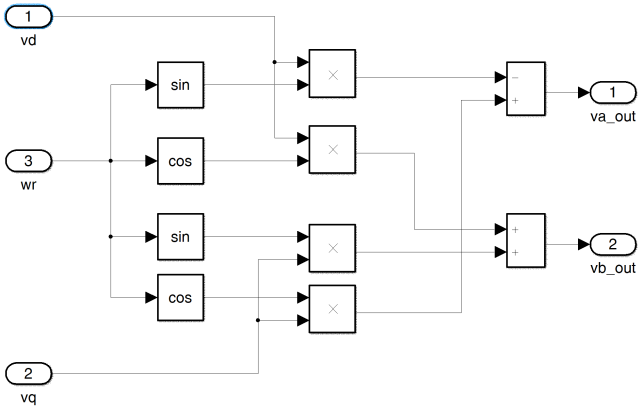
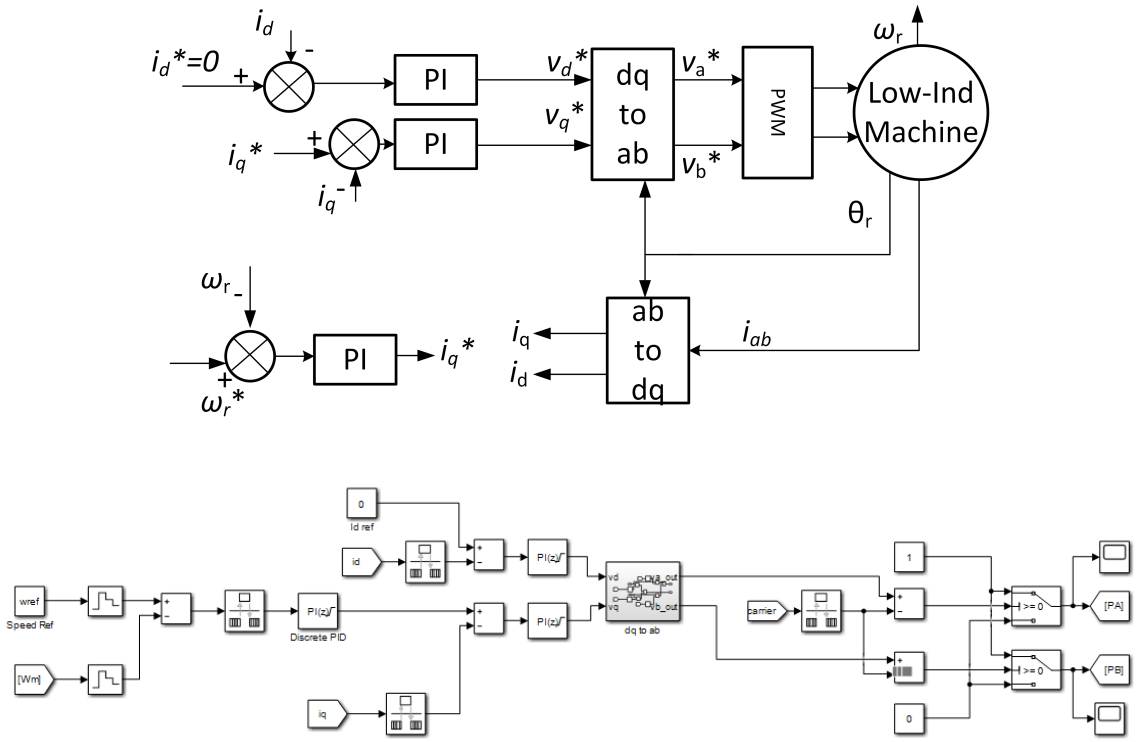


(d)

Figure 4.4: Models of the 2-phase AFPM machine. (a) the 2-phase AFPM SMC motor with transformation blocks, (b) equivalent circuit of stator flux, (c) ab to dq transformation, and (d) dq to ab transformation.



(b)

Figure 4.5: Modeling of drive systems, (a) FOC control diagram for the 2-phase low inductance machine drive systems, (b) current loop controller modeling for the drive system.

a closed-loop controller (field oriented control as in Fig. 4.5a) and a H-bridge drive circuit were developed and modeled as in Fig. 4.5b. In this scenario, the measured currents i_d and i_q from the machine were compared with the reference currents. After PI controllers, a reference wave was generated for the PWM modulation. A 90 degree phase shift was considered between phase A and phase B references. The switching frequency of 5kHz was selected for the H-bridge switches. ADC sampling frequency was set as (200kHz), sampling frequency for current loop was 20 kHz, and speed loop 2 kHz. The same sampling settings were employed by using rate transition blocks and PI controller sampling time in the simulation modeling (Fig. 4.5b).

4.4 Transfer Function and Closed Loop Parameter Design

To obtain PI control parameters, the transfer function with closed-loop controller of the 2-phase AFPM machine was calculated (Fig. 4.4). PI controllers were taken into consideration in the closed-loop block diagram as a negative feedback on basis of machine transfer function as in equations (4.3 - 4.8). As a result, current loop and speed loop transfer functions in the frequency-domain were obtained as in equations (4.11) and (4.12), respectively:

$$G_I(s) = \frac{(K_{pc} + \frac{K_{ic}}{s})(\frac{1}{R+Ls})}{1 + (K_{pc} + \frac{K_{is}}{s})(\frac{1}{R+Ls})} = \frac{K_{pc} + K_{ic}}{Ls^2 + (R + K_{pc})s + K_{ic}}, \tag{4.11}$$

$$G_\omega(s) = \frac{(K_{ps} + \frac{K_{is}}{s})K_t\frac{1}{Js+B}}{(K_{ps+\frac{K_{is}}{s}})K_t(\frac{1}{J_{eq}s+B}) + 1} = \frac{(K_{ps}K_t)s + K_{is}K_t}{J_{eq}s^2 + (B + K_{ps}K_t)s + K_{is}K_t}. \tag{4.12}$$

For the current loop, the crossover frequency was designed as 10% of switching frequency, and phase margin was designed to provide 60 degrees or in *radian* $\phi = \pi/3$. In this way, integral time constant τ_i and proportional gain K_{pi} for current loop were calculated as in equations (4.13 to 4.15).

$$\omega_{cross} = \frac{2 \times \pi \times f_{sw}}{10}, \tag{4.13}$$

$$\tau_i = \frac{ang(R_s + j\omega_{cross}L_s) + \phi + \pi/2}{\omega_{cross}}, \tag{4.14}$$

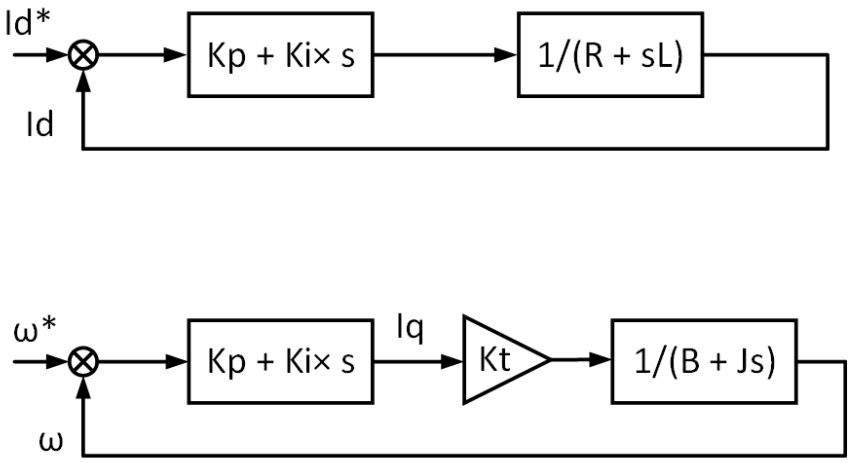


Figure 4.6: Block diagram of the two phase AFPM machine transfer function mathematical model. Speed loop and current loop PI controllers are taken into consideration.

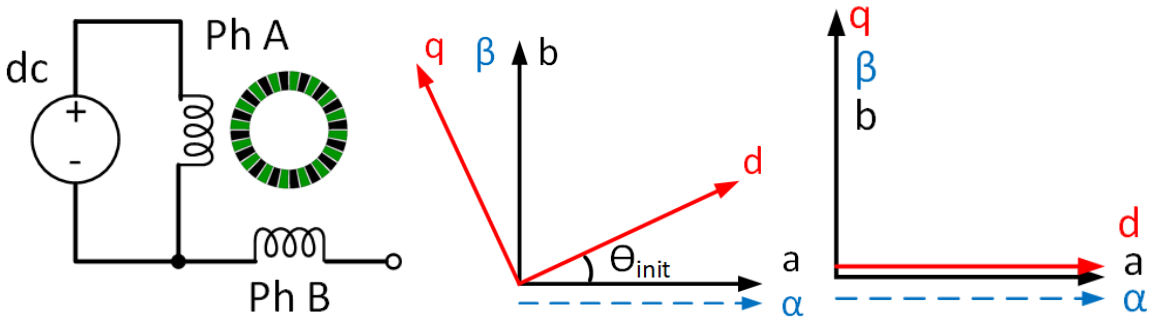
$$K_{pi} = \frac{1}{|\frac{V_{dc}(j\tau_i\omega_{cross}+1)}{(R_s+j\omega_{cross}L_s)(j\tau_i\omega_{cross})}|}. \tag{4.15}$$

For the speed loop, the crossover frequency was set at 10% of current loop, and similarly phase margin was designed as 60 degrees ($\phi = \pi/3$, in radian). And integral time constant τ_s and proportional gain K_{ps} for current loop were calculated as in equations below:

$$\omega_{cross} = \frac{2 \times \pi \times f_{sw}}{100}, \tag{4.16}$$

$$\tau_s = \frac{ang(j\omega_c J_{eq} + B) + \phi - \pi/2}{\omega_c}, \tag{4.17}$$

$$K_{ps} = \frac{1}{|\frac{p/2\lambda_f(j\tau_s\omega_c+1)}{(j\omega_c J_{eq}+B)(j\tau_s\omega_c)}|}. \tag{4.18}$$



(a) (b) (c)

Figure 4.7: Rotor initial position alignment for 2-phase AFPM motor drive with an incremental encoder. (a) The hardware connection and alignment with d-axis diagram, (b) phase diagram before alignment, and (c) phase diagram after alignment.

4.4.1 Initial Rotor Angle Alignment

An incremental encoder was employed in this prototype, whose output speed and position information were a continuous stream of ubiquitous pulses. Therefore, initial rotor position alignment was implemented in the control. A constant DC link voltage was applied on phase A of the 2-phase AFPM machine with a very small current; while phase B is kept open as is depicted in Fig. 4.7a. If the rotor was not aligned with A-axis as in Fig. 4.7b at the moment DC voltage applied, a constant current would flow in phase A and place the stator current vector in the α-axis. Therefore, the rotor was forced to move into alignment as shown in Fig. 4.7c. Thus in this manner, A-axis, α-axis and d-axis were aligned physically.

Besides the physical alignment, the initial angle reading in control program needed to be compensated. After the compensation, both the control program and hardware were aligned between d-axis and a-axis.

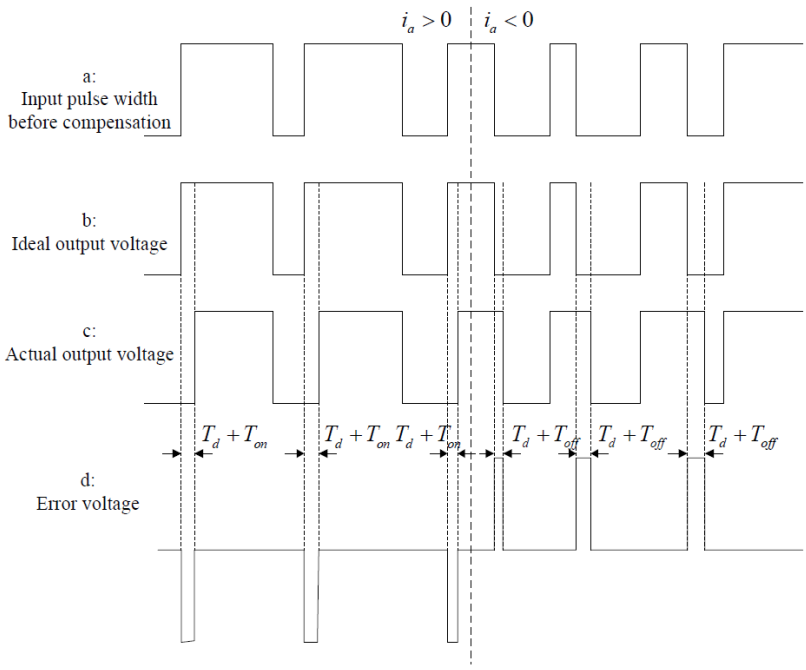


Figure 4.8: Dead-time investigation for PWM fed inverters. The effect of dead-time on the output of the inverter is illustrated in each switching cycle [136].

4.4.2 Dead-time Compensation

In order to avoid short circuit between positive and negative terminals of the power supply, both switches in an inverter leg should never conduct simultaneously. One of the most common methods to avoid such short circuit is to add a small time delay (T_d in Fig. 4.4.2) to the gate signal of the turning-on device. This delay is called dead-time and introduces a load dependent magnitude and phase error in the output voltage [137].

Besides dead-time, the turn-on delay time T_{on} and turn-off delay time T_{off} in MOSFET or IGBT devices, occurs in every PWM cycle and brings a continuous error in inverse proportion to the output. If dead time is not compensated, a serious waveform distortion, fundamental voltage drop, and instabilities, as well as additional losses may be caused [138] [139].

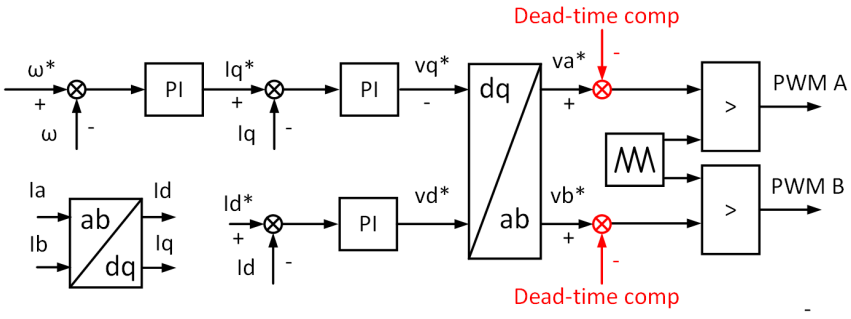


Figure 4.9: Dead-time compensation development in control algorithm. The dead-time caused in each switching cycle is compensated on the d- and q-axis reference voltage in the closed-loop controller.

In every PWM cycle, the PWM voltage error ΔU caused by the total delay time error t_{err} can be calculated as:

$$t_{err} = T_d + T_{on} + T_{off}, \quad \Delta U = \frac{t_{err}}{T_s} U_{dc} sign(i_x), \tag{4.19}$$

where i_x indicates the current of phase x (x can be A or B in this drive system).

The calculated dead-time was compensated at d- and q-axis voltage references (Fig. 4.4.2). The complete control program was developed in dSPACE (Fig. 4.4.2) and featured encoder position and speed calculation and reading, ADC and calibration, FOC closed-loop, PWM generation, initial angle alignment, dead-time compensation, and switchable modes among initialization mode, open loop, and closed-loop.

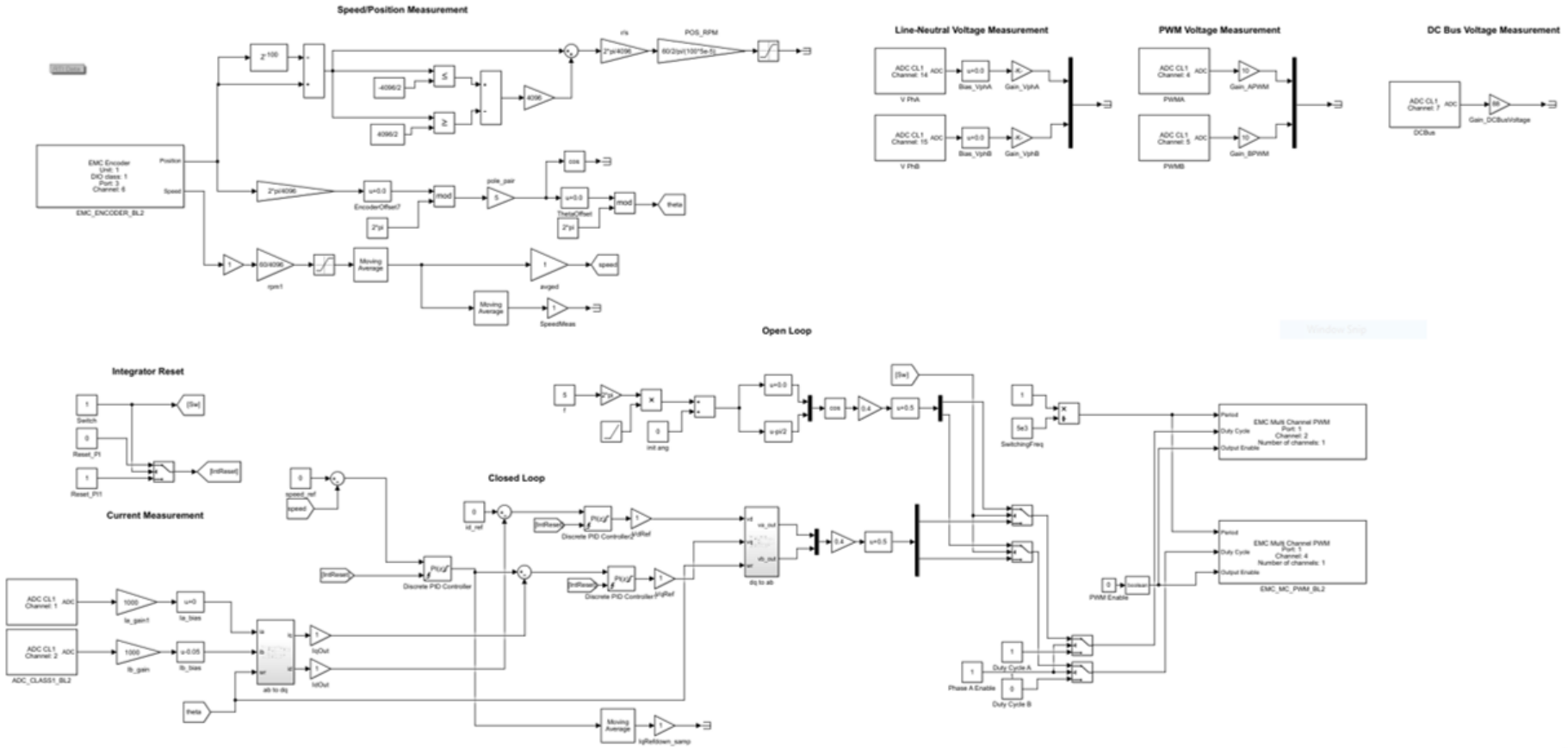


Figure 4.10: The control program developed in dSPACE as part of this PhD research, including encoder position and speed calculation and reading, ADC and calibration, FOC closed-loop, PWM generation, initial angle alignment, dead-time compensation, and switchable modes among initialization mode, open-loop, and closed-loop.

4.5 The Analysis of Operating Range

A physical phase variable model of the 2-phase AFPM machine was developed, whose PM flux linkage and phase inductance were extracted from 3-dimensional finite element analysis (FEA). It has been shown that for machine designs with low inductance, the selection of switching frequency plays an important role in improving the system performance [140].

The operating range is first analyzed for the two proposed configurations (Fig. 4.11). Any point within the intersection of the voltage and current limitation circles is operational for the motor. The voltage limit is centered at $(-\lambda_{pm}/L_d,\ 0)$ with the radius of $V/\omega L_d$. It can be observed that for the low inductance machines, the voltage limit circle has a much larger radius, and the center of the circle is shifted far from the center. Therefore, the operating range becomes narrow for low inductance machine drives.

The simulated phase voltage ranges for the two inverters with various modulation schemes are presented in Fig. 4.12. If the voltage of the dual H-bridge inverter with SPWM is considered as 1.0 pu, the phase voltage of SPWM and SVPWM in 3-leg topology are 0.67 pu and 0.71 pu, respectively.

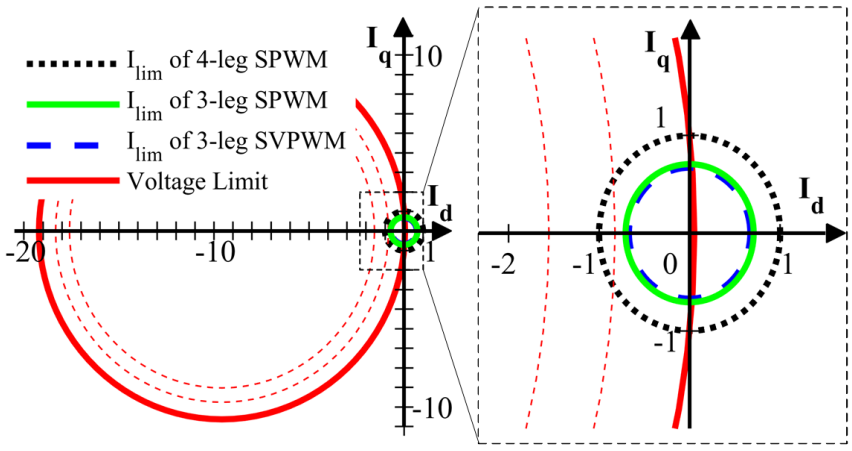


Figure 4.11: The operating ranges of the proposed two drive systems with different modulation schemes (in p.u.).

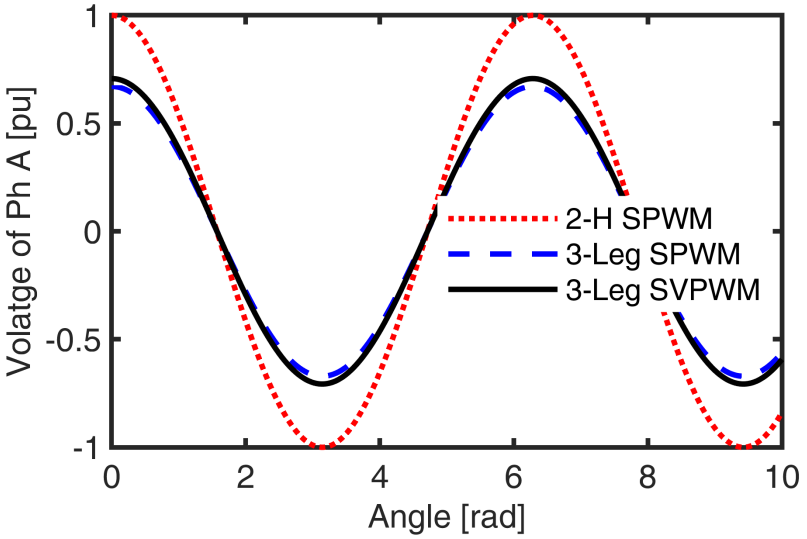


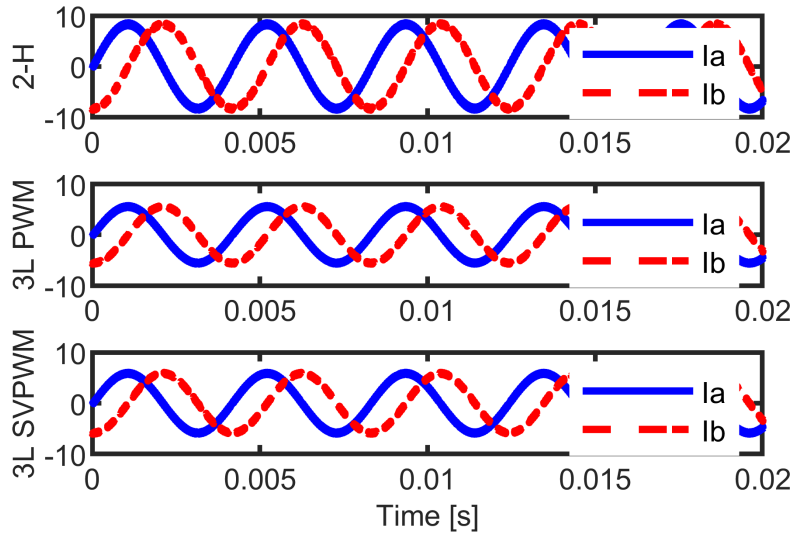
Figure 4.12: Phase A voltage. Compared with 1.0 pu voltage rating of the dual H-bridge topology with SPWM, the 3-leg topology with SPWM and SVPWM can at most produce 0.67 pu and 0.71 pu voltage, respectively, under the same condition.

4.6 Simulation and Experimental Validation

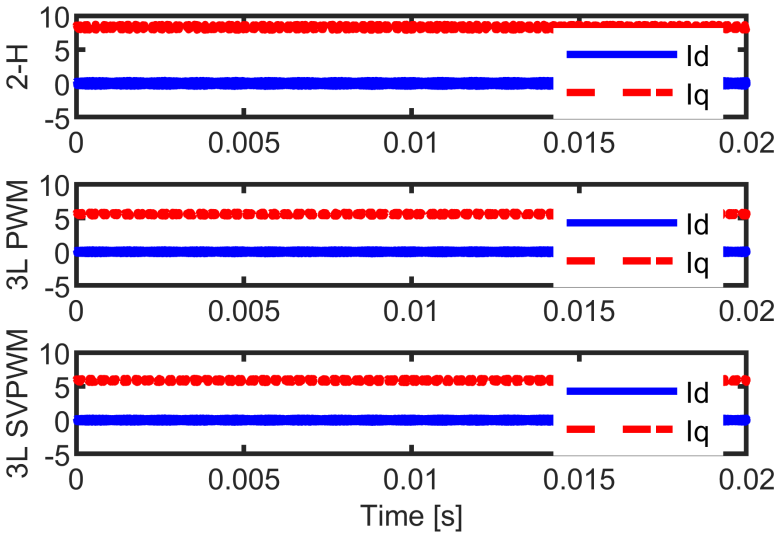
4.6.1 Simulation Validation on Different Modulation and Motor Drive Controls

The 2-phase motor was operated at 266.67Hz fundamental frequency with full load. The simulated phase currents were investigated to compare the current capability of different topologies with various modulation methods (Fig. 4.13). The phase currents I_a and I_b for the 3-leg drive systems with PWM and SVPWM were 71% and 67% of dual H-bridge system capacity under the same condition (in Fig. 4.13a). The dq currents I_d and I_q for the dual H-bridge drive system were 0 and 8.30A, respectively. With the same DC bus voltage, the I_q of the 3-leg drive system was reduced to 5.56A with SPWM and 5.87A with SVPWM, respectively, as shown in Fig. 4.13b. To have the same current/torque capability, it was necessary to increase the V_{dc} for the 3-leg drive system.

To apply the 2-phase very low inductance machine for variable speed applications, the closed-loop speed control based on $i_d = 0$ control strategy was implemented, as illustrated by the schematic diagram in Fig. 4.5a. Responses of motor speed and phase currents to a step change in the reference speed were presented in Fig. 4.15. At 0.1s, the speed reference was increased from 1,000 rpm to 1,500 rpm, and speed was tracking the speed reference, and frequency of phase currents i_a and i_b was increased accordingly.

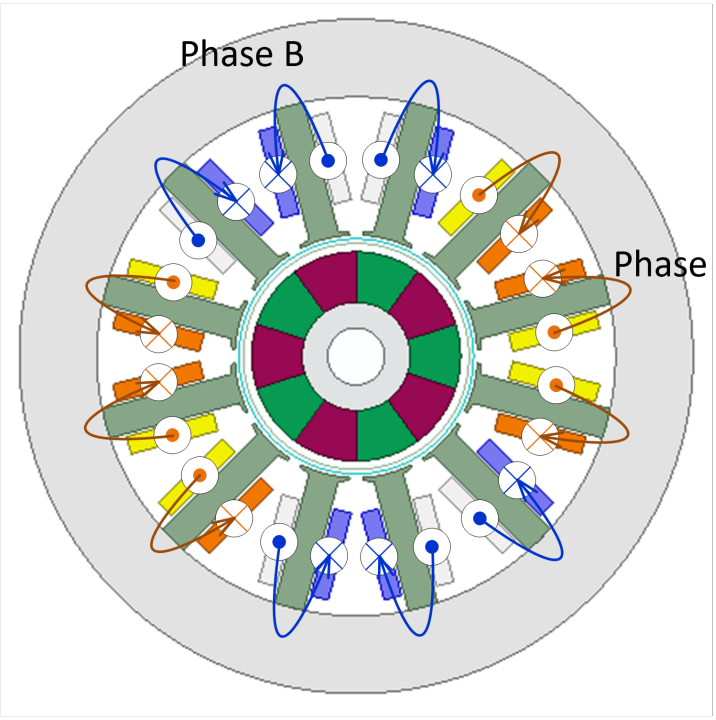


(a)

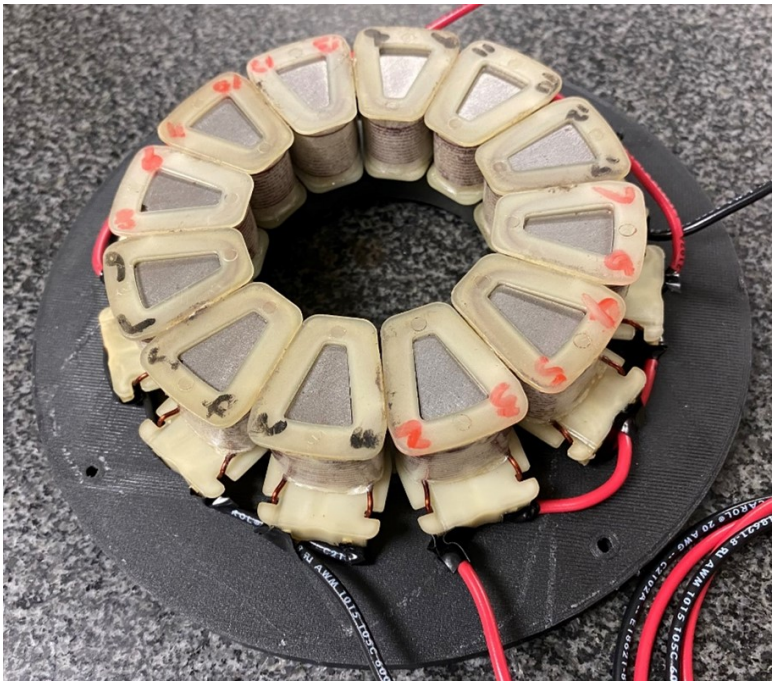


(b)

Figure 4.13: Simulated performance of the two drive configurations with various modulation schemes, (a) *ab* phase currents, (b) *dq* currents. To have the same current/torque capability for the 3-leg drive system, a higher V_{dc} is necessary, and hence higher voltage ratings for the WBG devices, are required.



(a)



(b)

Figure 4.14: The 2-phase APFM motor winding diagram, (a) configuration diagram, and (b) configured APFM SMC machine.

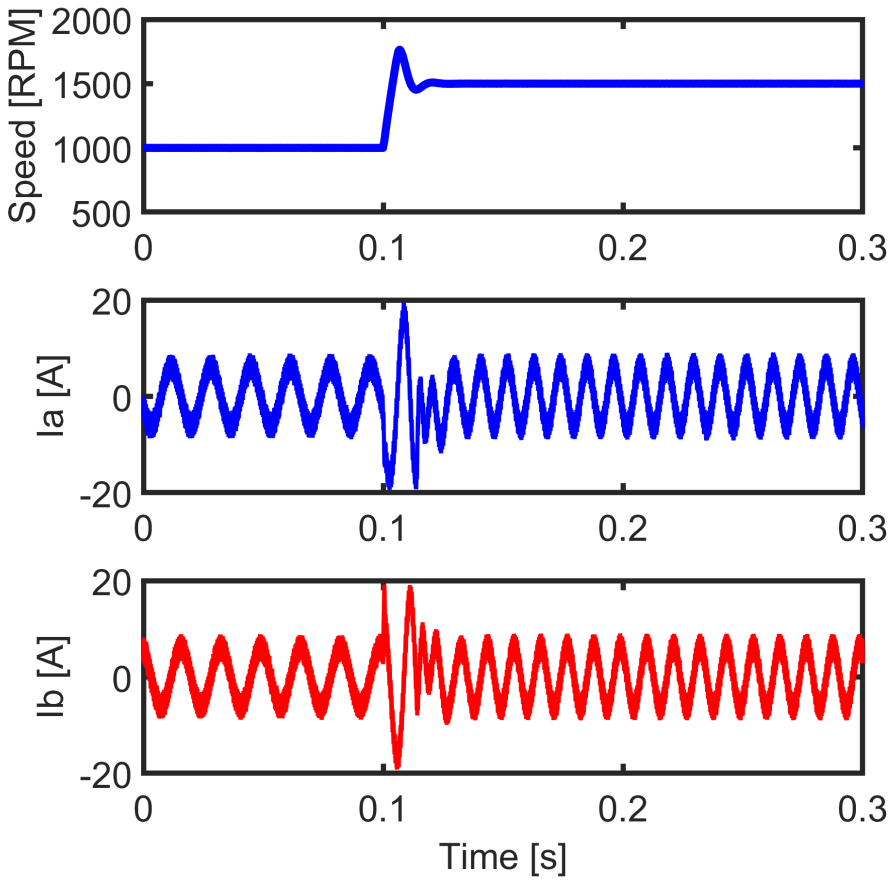


Figure 4.15: Simulated results: transient state of speed and phase currents when speed is increased from 1,000 rpm to 1,500 rpm at 0.1s of simulation time.

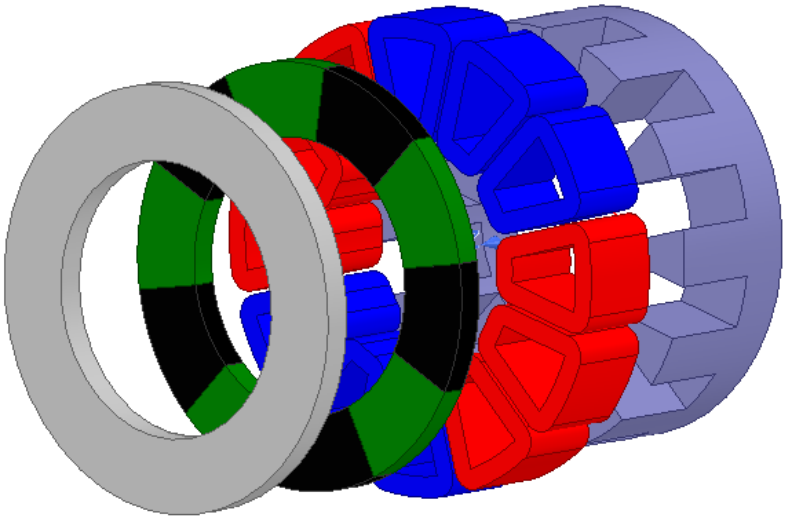


Figure 4.16: The exploded view of the 2-phase SMC AFPM motor developed by Regal Beloit Corporation.

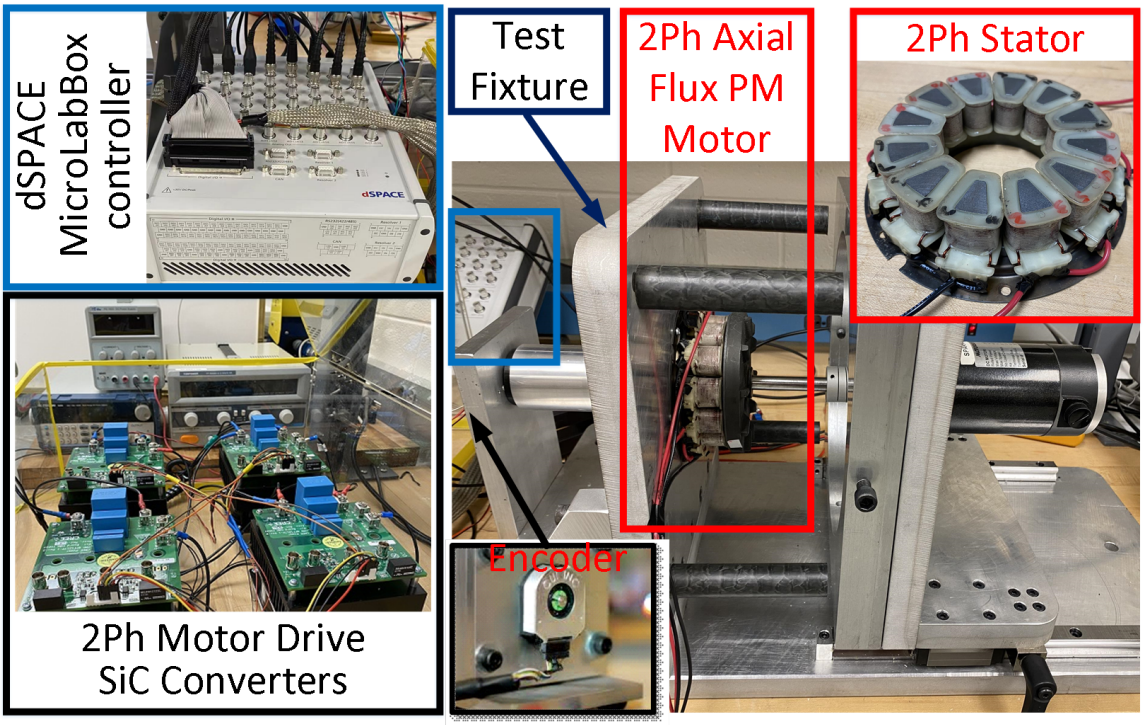


Figure 4.17: The prototype for the 2-phase AFPM SMC motor drives developed as part of this PhD research at UK. The control is programmed through dSPACE control board, dual H-bridge inverter is developed with SiC MOSFETs, and a DC generator is coupled to SMC motor on test fixture and loaded with a programmable DC load.

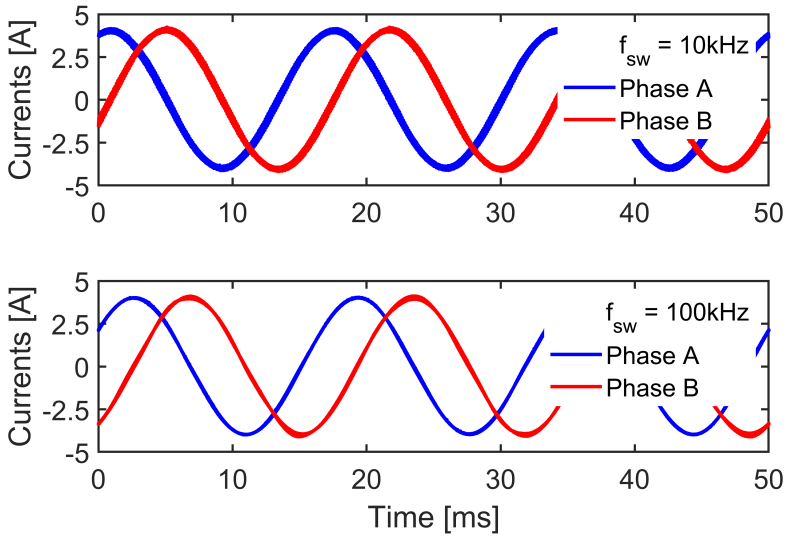


Figure 4.18: Experimental results for the proposed two inverter topologies with suitable modulation schemes developed for dual H-bridge inverters with SPWM.

4.6.2 Experimental Validation for Current Ripple Improvement by Employing High Switching Frequency WBG Devices

An experimental test setup has been built as part of the PhD research to validate the theoretical analysis and evaluate the performance of the studied drive systems. The motor to be tested is a 2-phase AFPM SMC machine with configuration in Fig. 4.14, and exploded view shown in Fig. 4.16. The two phases of stator have two independent phase windings with 90 electrical degrees of angular displacement between each other. The developed test fixture is shown in Fig. 4.17, which can be used to adjust the airgap length during the test.

The drive systems using WBG devices and the dSPACE control board were designed and built as shown in Fig. 4.17. Two isolated DC supplies with separate DC capacitors fed the two phase windings independently. The dSPACE control board

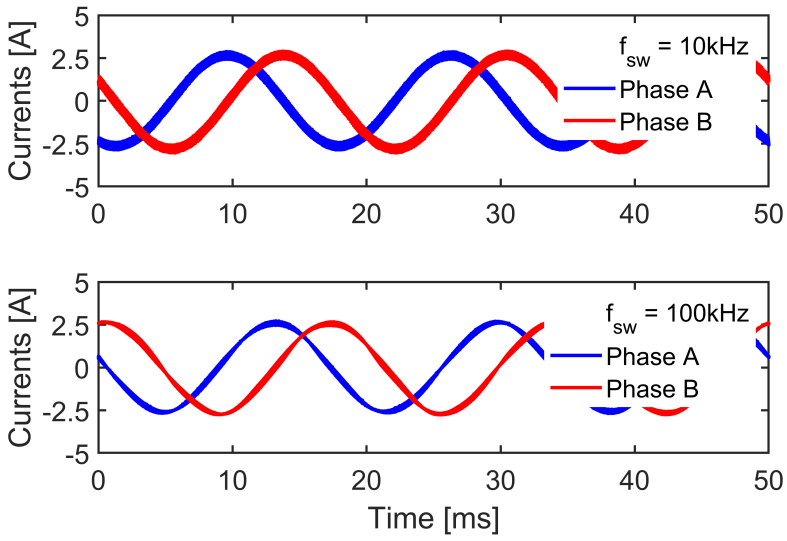


Figure 4.19: Experimental results for the proposed two inverter topologies with suitable modulation schemes for the three-leg inverter with SPWM.

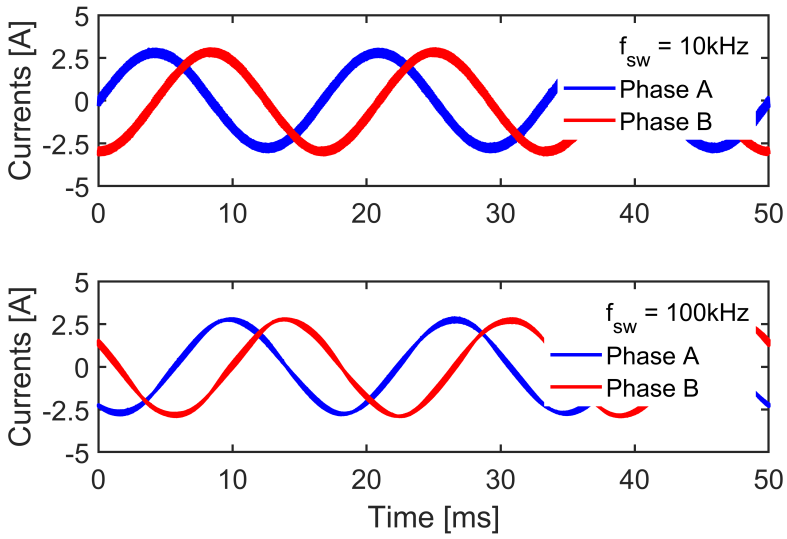


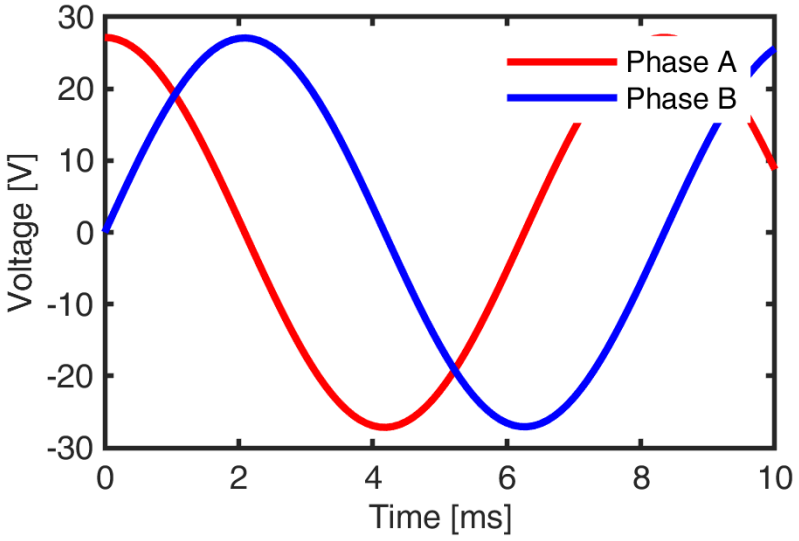
Figure 4.20: Experimental results for the proposed two inverter topologies with suitable modulation schemes for the three-leg inverter with SVPWM. By using WBG devices, the switching frequency can be significantly increased, which helps reduce the current ripple and thus torque ripple.

generated gating signals to drive the inverters. Based on the proposed modulation schemes, gating signals for the two phases were generated 90 electrical degrees apart from each other, matching the machine drive requirements. The Wolfspeed SiC MOSFET power semiconductors C2M0280120D (rated at 1200V/10A and operated at switching frequency 10kHz and 100kHz) were employed for the prototype drive system.

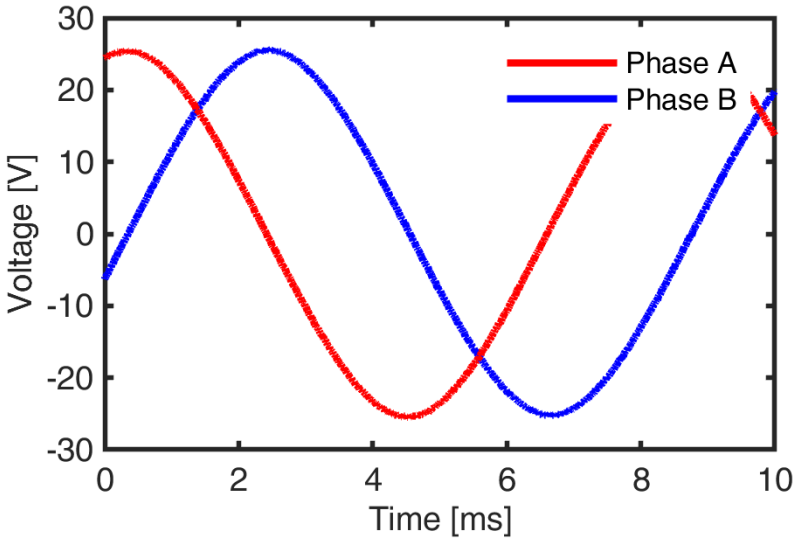
The experimental results were presented in Fig. 4.13. The current ripple reduces significantly in each set of results with the increase of switching frequency enabled by SiC devices (from 10kHz to 100kHz). With the same DC bus voltage and modulation index, the dual H-bridge drive system can produce the maximum phase currents (2.64A), while the 3-leg drive systems can only produce 1.87A with SVPWM and 1.77A with SPWM, respectively. To have the same operating range, it is necessary to increase the DC bus voltage for the 3-leg topology.

4.6.3 Experimental Validation with Two-phase AFPM SMC Motor and FOC Closed-Loop Control

A back EMF testing and simulation was first conducted (Fig. 4.21). The back EMF simulation was set as running at 1435 rpm with an air gap of 1.5 mm in Ansys Maxwell (Fig. 4.21a) according to the back EMF measurement speed setting (Fig. 4.21b). The measured back EMF (51.87 Vpk-pk) was very close to the machine design in simulation (54.29 Vpk-pk). Other parameters including flux constant and phase inductance and phase resistance were measured and validated in experimentation and used for control parameter development.



(a)



(b)

Figure 4.21: Back EMF of the 2-phase AFPM SMC motor, (a) simulation results, (b) measured results at 1435 rpm and air gap 1.5mm.

After the aforementioned validations, a FOC closed-loop motor drive control was developed by using a dyno system (2-phase AFPM SMC motor coupled with a DC generator, and connected with a programmable DC load, which had various modes including constant resistance load, constant current load, constant power load, and constant voltage load). The measured electrical angle and phase A current were plotted together for angle alignment validation (Fig. 4.6.3). The measured speed (Fig. 4.6.3) was maintained at the speed reference, which was 3000 rpm in this testing case. Moving average digital filters were implemented in the control program to filter measured speed and measured current waveforms. For speed measurement, an average speed was calculated based on every 50 speed samples, and 20 samples for filtering current measurements. The speed ripples were kept to lower than 5%. The d-axis current reference was given 0 and q-axis reference current was calculated from speed loop (black solid color line in Fig. 4.6.3). Measured phase currents I_a and I_b (Fig. 4.6.3) were balanced with 90 degrees apart between the two phases. The d-axis and q-axis currents were satisfactorily constant and tracking the current references with encoder position reading and programmed dq to ab transformation.

Other operation conditions were experimentally validated using the testing setup. A power analyzer was employed to measure the input power into the inverter, the input power to the motor (can be calculated as in Eq. 4.20), the line-line voltages of the machine, current, and the output power from DC generator are recorded in Table 4.2. For the testing case at rated speed 3000 rpm, motor power in was 297.1 W and DC generator power out was 187.0 W. The efficiency of the dyno system (AFPM motor coupling with DC generator) was 64%, within the typically accepted efficiency

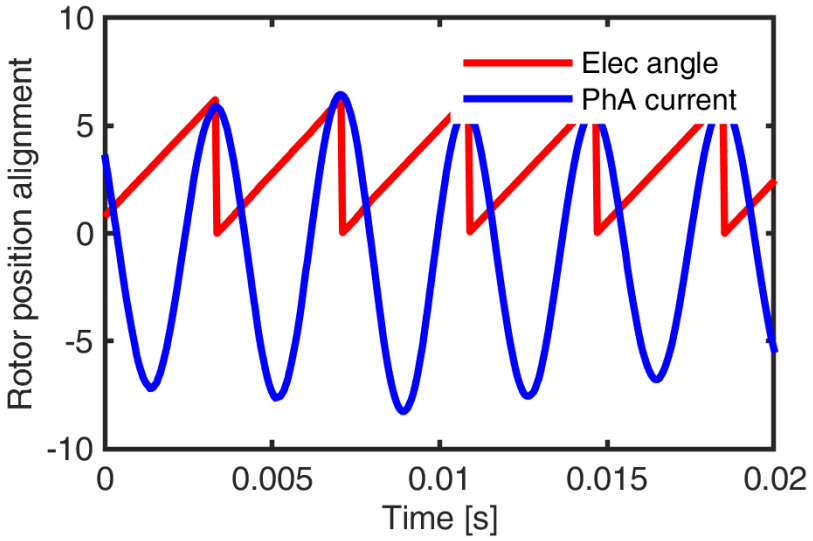


Figure 4.22: Experimental validation on rotor position alignment. Phase A current and measured electrical angle are plotted in the same figure for alignment comparison.

Table 4.2: Experimental operating conditions of the 2-phase SMC AFPM machine.

Speed [rpm]	Inverter Power In [W]	Motor Power In [W]	Inverter Eff [%]	Current [A]	Phase Voltage [V]	DC Generator Power Out [W]
1500	126.4	103.8	82.1	4.6	15.6	72.0
2000	184.9	165.6	89.5	5.0	23.4	111.0
2500	220.0	198.4	90.2	5.2	26.5	127.0
3000	327.9	297.1	90.6	6.1	31.7	187.0

range for low power motors.

$$P_{2ph} = 2 \times V_{ph} \times I_{ph} \times \cos\theta \tag{4.20}$$

where P_{2ph} is active power for 2-phase motors, V_{ph} phase voltage, I_{ph} the phase current, and θ the power factor angle which is 0 degree in this experimentation.

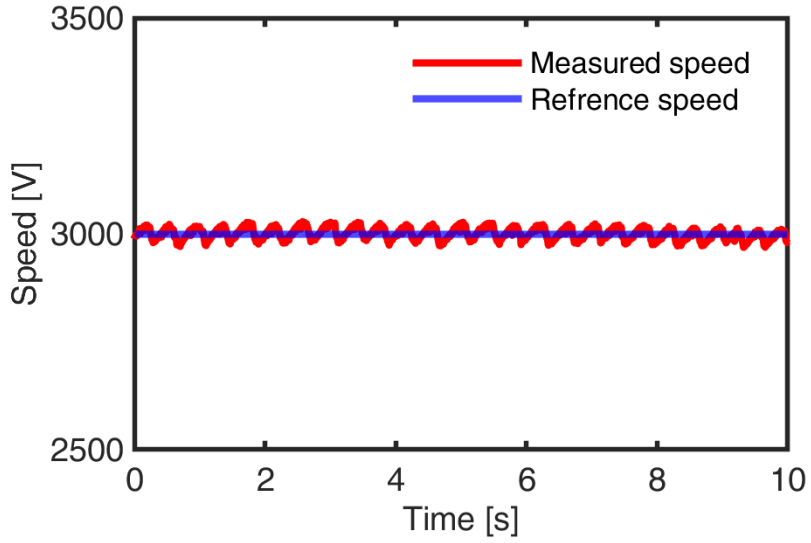


Figure 4.23: Experimental speed result and reference speed of dual H bridge inverter topology with SPWM.

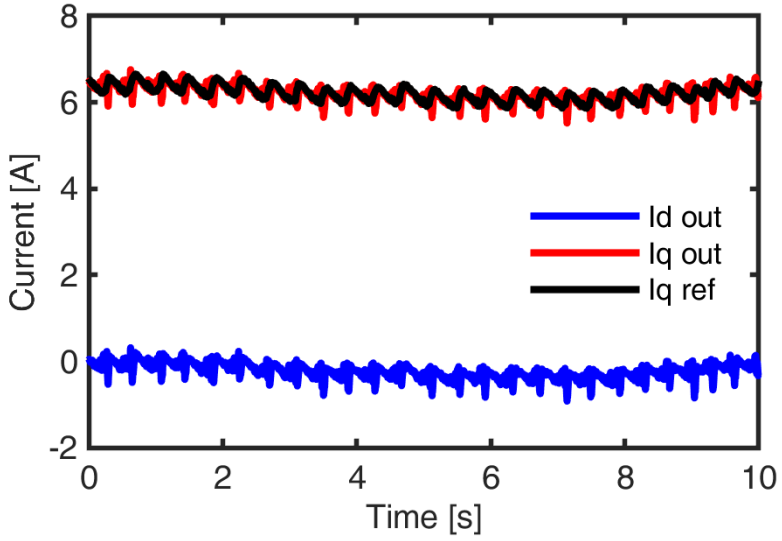


Figure 4.24: Experimental and reference d-q axis currents of dual H bridge inverter topology with SPWM.

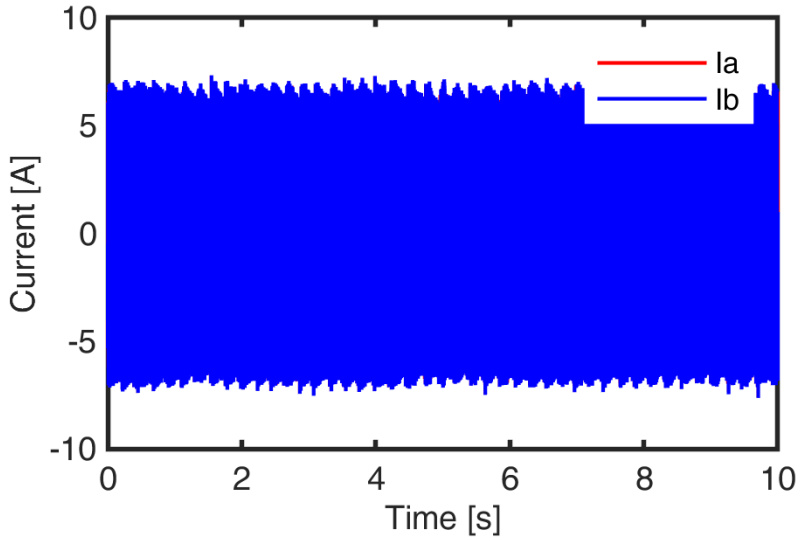


Figure 4.25: Experimental phase current result of dual H bridge inverter topology with SPWM.

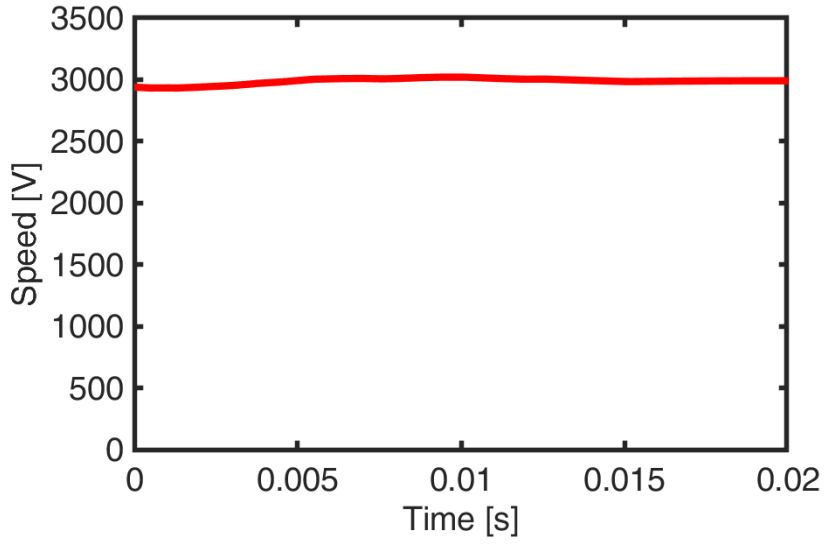


Figure 4.26: Zoomed-in experimental speed result and reference speed of dual H bridge inverter topology with SPWM.

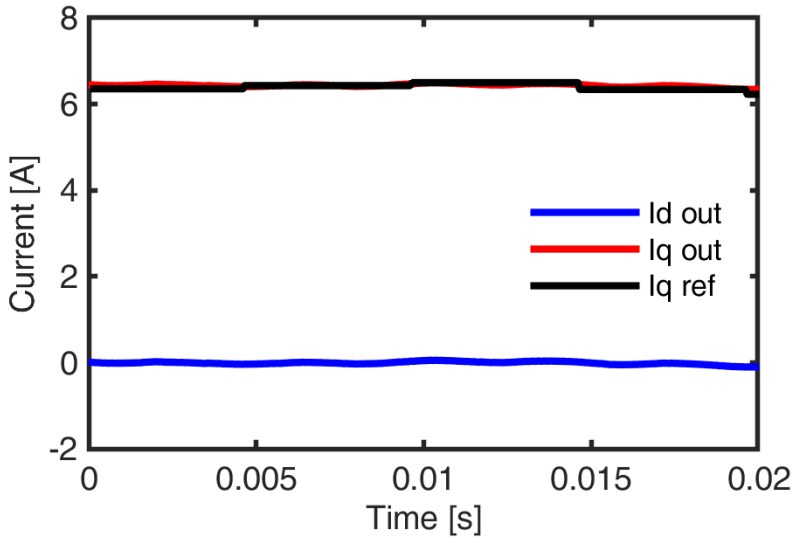


Figure 4.27: Zoomed-in experimental and reference d-q axis currents of dual H bridge inverter topology with SPWM.

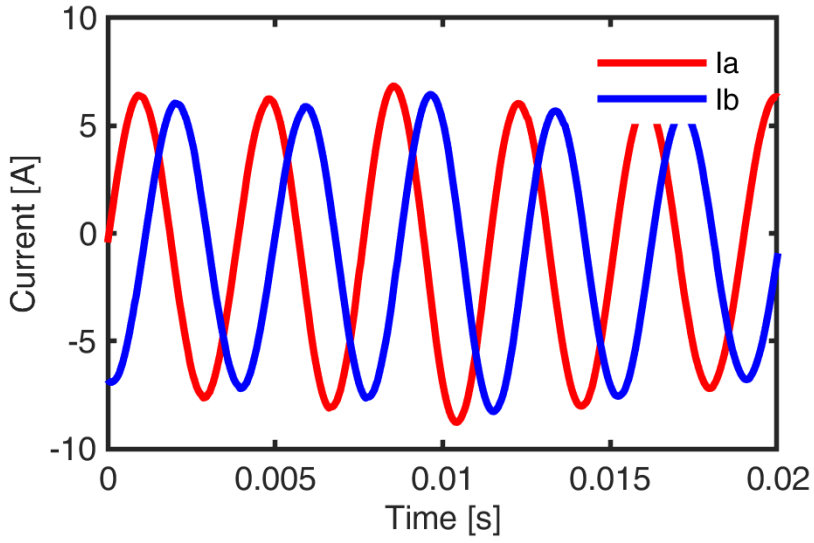


Figure 4.28: Zoomed-in experimental phase current result of dual H bridge inverter topology with SPWM.

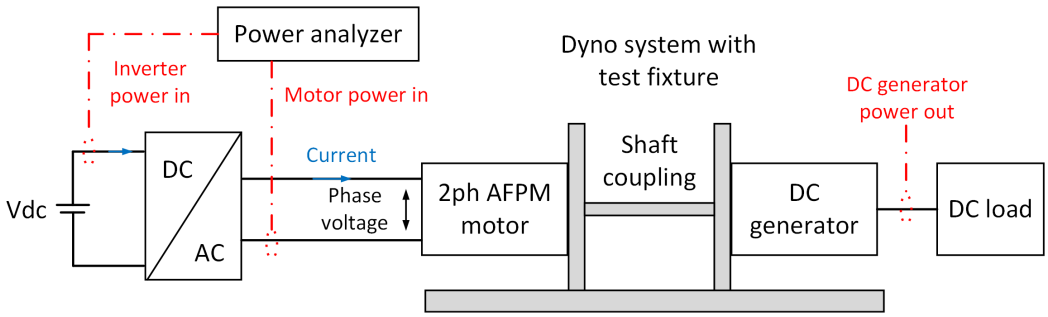


Figure 4.29: Schematic diagram of the 2-phase AFPM dyno drive system. Inverter power in, motor power in, DC generator power out, phase voltage, and current were measured for efficiency evaluation.

4.7 Conclusion

This chapter described the performance evaluation of a dual H-bridge and a 3-leg inverter based drive system for 2-phase AFPM machines featuring low inductance. It was shown that the dual H-bridge inverter supplied by two separate DC sources provided complete electrical isolation between phases. If one supply failed, a single phase might still be supplied and thus the dual H-bridge has maximum survivability.

In terms of output capability, the 3-leg drive system was capable of producing at most 71% the voltage generated by the dual H-bridge inverter for the same DC bus voltage. In the case of a supply failure, the whole system of the 3-leg inverter failed. In the 3-leg topology there was only one DC source and one of the three legs was shared by two phases. Therefore, this configuration offered a more cost effective solution by reducing power semiconductor switch count from 8 to 6, and reducing DC supply count from 2 to 1, compared with the dual H-bridge configuration at the same DC bus rating.

It was also experimentally shown that the current ripple was effectively reduced by implementing the two drives with WBG devices and operating the inverters at

high switching frequencies. The 100kHz switching frequency enabled by SiC devices, compared to the 10kHz achievable by traditional silicon devices, largely reduced the current ripple and total harmonic distortion.

Back EMF was measured and compared with machine design results from simulation. The phase inductance and phase resistance were measured and confirmed to match the designs of the 2-phase AFPM SMC motor. Field oriented control was developed for the 2-phase AFPM SMC motor drives. Initial angle alignment and dead-time compensation were developed to provide synchronization between rotor rotation and control algorithm. Experimental results of closed-loop drives validated the effectiveness of the control design: speed was constant and tracking the speed reference; speed ripple was controlled within 5%; phase currents I_a and I_b were balanced and 90 degrees apart; d-q axis currents were constant and tracking current references.

Chapter 5

Integrated AC to AC Converters for Single-Phase Input to Two-Phase Output

5.1 Introduction and Problem Formulation

The single-phase grid has been widely used in power distribution systems for residences and small commercial buildings, where single-phase to two-phase and single-phase to three-phase power conversions are required to drive low-power motors [54] [56]. In particular, two-phase machines have shown attractiveness due to the magnetic and electrical isolation between two phases, and low cost on developing the drive systems [55] [57].

To achieve the single-phase to two-phase power conversion, one of the most commonly utilized topologies is the AC/DC/AC pulse width modulation (PWM) converter, which requires ten or twelve active power semiconductor switches and a common DC link [141]. However, especially for low power applications, a component minimized topology offering the same functionality can reduce switch counts and therefore the system cost. [142]

On the other hand, researchers have been working on reducing DC capacitance for a minimized system cost. The matrix converter, which does not require either any dc-link circuit or large energy storage elements has been studied and developed [143]. The key element in a matrix converter is the fully controlled four-quadrant bidirectional switch module, which allows high frequency operation but contains two power semiconductor devices for each module [144]. Additionally, filters must be used at the input of matrix converters.

A systematic study on the comparison among the conventional back-to-back converters, matrix converters, and component-minimized AC/AC converters is in great need considering some aspects of the subject matter has been discussed but scattered in the existing literature. In this chapter, three topologies, the modulation scheme, and filter designs for the two commonly utilized topologies and the proposed integrated AC/AC converter were presented. Closed-loop speed controllers and an experiment prototype were developed. As a result, a systematic comparison on system cost and output performance was studied and validated.

5.2 Conventional Single-phase Input to Two-phase Output Converters: AC/DC/AC Converter and Matrix Converter

As one of the commonly utilized topologies, the AC/DC/AC PWM converter usually contains a full-wave rectifier, a DC link, and two H-bridges to drive the two phases of the load (Fig. 5.1). The input filter and DC capacitors smooth the input

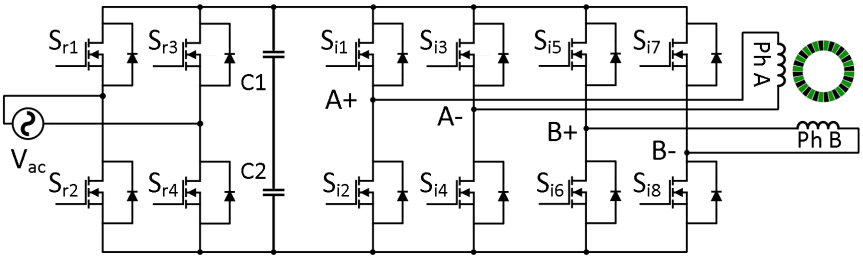


Figure 5.1: A conventional back-to-back converter for single-phase full-wave input and two-phase output.

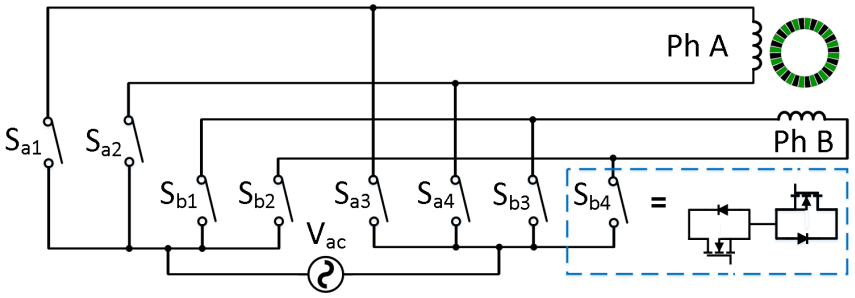


Figure 5.2: Matrix converter for single-phase input two-phase output.

current and DC voltage, respectively. The rectifier can be operated in active or passive mode, and the PWM modulation for the inverter can be expressed as follows:

$$\begin{cases} V_{PhA} &= V_{A^+} - V_{A^-} = mV_{dc}\cos\left(\omega t - \varphi\right), \\ V_{PhB} &= V_{B^+} - V_{B^-} = mV_{dc}\sin\left(\omega t - \varphi\right), \end{cases} \tag{5.1}$$

where V_{PhA} and V_{PhB} are the terminal voltages of phase A and phase B of the load, respectively. V_{A^+}, V_{A^-}, V_{B^+}, and V_{B^-} represent the voltage at the points A^+, A^-, B^+,

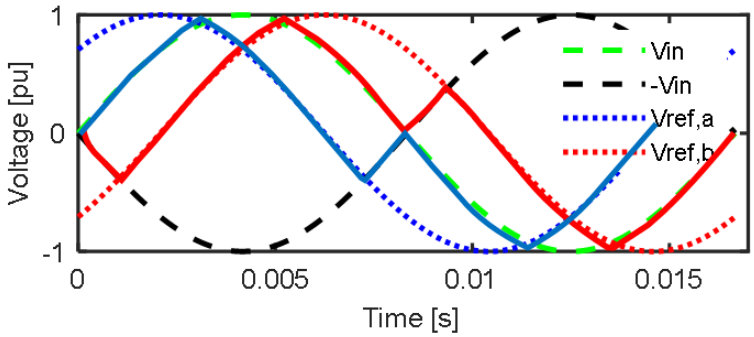


Figure 5.3: Modulation scheme developed for single-phase to two-phase matrix converter.

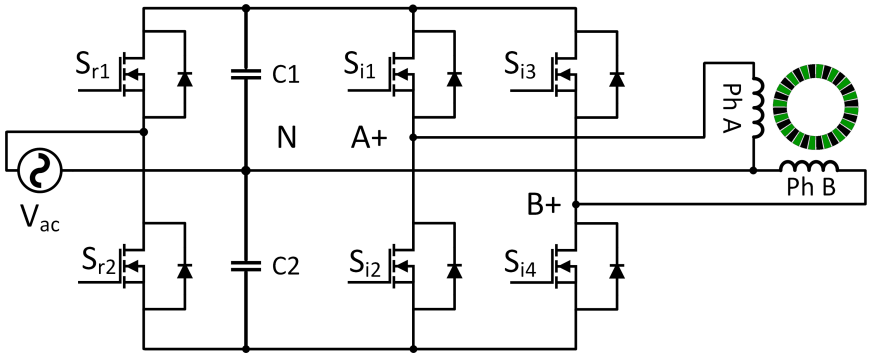


Figure 5.4: The proposed integrated AC/AC converter for single-phase input to two-phase output.

and B^-, respectively. m and V_{dc} are the modulation index and DC voltage amplitude, respectively. The angular frequency of the two-phase machine ω is obtained from $\omega = 2\pi f$, and φ is the initial phase of the reference wave.

The single-phase to two-phase matrix converter (Fig. 5.2) includes 8 active bidirectional switching modules, input filter, and load side filter. To be specific, each switching module usually has 2 active semiconductor switching devices. The key benefit of matrix converter is the elimination of DC link capacitor; however, the input filter and load side filter are required in matrix converters. Besides, since there is no natural freewheeling path, commutation has to be actively controlled at all times. The control scheme (Fig. 5.3) and operating scheme (Table 5.1) for matrix converters thus are more complicated than AC/DC/AC converters, which is presented as follows:

$$\begin{cases} V_{ac} & = V_g \cos(\omega t) = V_{refA} + V_{refB}, \\ V_{refA} & = \left(\frac{V_g}{\sqrt{2}}\right) \cos\left(\omega t + \frac{\pi}{4}\right), \\ V_{refB} & = \left(\frac{V_g}{\sqrt{2}}\right) \sin\left(\omega t + \frac{\pi}{4}\right), \end{cases} \tag{5.2}$$

where V_{ac} is the input voltage and V_g is the amplitude of input voltage. V_{refA} and V_{refB} represent the reference voltage for Phase A and Phase B, respectively.

Table 5.1: The operating scheme for single-phase to two-phase matrix converter.

Mode	I	II	III	IV
$V_{refA} \times V_{ac}$	+	+	-	-
$\|V_{refA}\|$ - $\|V_{ac}\|$	+	-	-	+
$\|S_{a1}\|$	On	PWM	Off	Off
$\|S_{a2}\|$	Off	Off	PWM	On
S_{a3}	Inverse of S_{a1}			
S_{a4}	Inverse of S_{a2}			

5.3 Modeling and Development of Integrated 1Ph to 2Ph AC/AC Converter

5.3.1 Load Impedance Compensation and Modulation Scheme for the Proposed Integrated AC to AC Converters

In this topology, the neutral point of DC link is accessed by both rectifier and inverter, and the DC capacitor provides conduction path for both rectifier and inverter (Fig. 5.4). As a result, inverter switching is interfering with the rectifier control, and the load side impedance has an influence on voltage/current amplitude balance. To develop a control scheme for the proposed converter, a load impedance compensation angle is necessary and appropriate filter designs are required.

Consider input voltage and current can be formulated as:

$$\begin{cases} v_g(t) &= V_g \cos\left(\omega_g t - \theta_g\right), \\ i_g(t) &= I_g \cos\left(\omega t\right), \end{cases} \tag{5.3}$$

where $v_g(t)$ and $i_g(t)$ indicate input voltage and current, respectively. V_g and I_g are the amplitudes and θ_g represents the phase angle between grid voltage and current.

For the load side, the load voltage and current can be expressed as:

$$\begin{cases} v_l(t) &= V_l \cos\left(\omega_l t - \sigma\right), \\ i_l(t) &= I_l \cos\left(\omega t - \sigma + \theta_l\right), \end{cases} \tag{5.4}$$

where $v_l(t)$ and $i_l(t)$ indicate load side voltage with amplitude V_l and load side current with amplitude of I_l. θ_l represents the phase difference between load voltage and load current, and σ is the compensation angle used for control development. Then the power $p_c(t)$ flows into DC capacitor can be written as:

$$\begin{aligned} p_c(t) = \frac{V_g I_g}{2}\cos\theta_g - \frac{V_l I_l}{2}\cos\theta_l - \frac{V_l I_l}{2}\cos\left(\theta_l - \frac{\pi}{2}\right) \\ + \frac{V_g I_g}{2}\cos\left(2\omega_g t - \theta_g\right) - \frac{V_l I_l}{2}\cos\left(2\omega_l t - 2\sigma + \theta_l\right) \\ - \frac{V_l I_l}{2}\cos\left(2\omega_l t - \frac{\pi}{2} - 2\sigma + \theta_l\right). \end{aligned} \tag{5.5}$$

To have a balanced DC capacitor power flow, which is supposed to be controlled to zero, the modulation scheme with load impedance compensation angle σ can be obtained as:

$$\begin{cases} V_A &= V_s \cos(\omega t + \sigma) = V_s \cos(\omega t + \frac{\theta_g + \theta_l}{2}), \\ V_B &= V_s \sin(\omega t + \sigma) = V_s \sin(\omega t + \frac{\theta_g + \theta_l}{2}). \end{cases} \tag{5.6}$$

5.3.2 Filter Designs for the Proposed Integrated AC to AC Converters

The real power flowing from single-phase AC source into DC link can be expressed as:

$$P_i = \frac{V_{ac} V_{dc}}{X_i}\sin\theta, \tag{5.7}$$

where X_i and θ represent the reactance of input L filter and angle difference between input V_{ac} and DC link V_{dc}, respectively. The input power factor, pf, can be expressed

as:

$$pf = \cos\phi = \frac{V_{dc}\sin\theta}{\sqrt{V_{ac}^2 + V_{dc}^2 - 2V_{ac}V_{dc}\cos\theta}}. \tag{5.8}$$

A constant k can be defined as:

$$k = \frac{V_{dc}/2}{\sqrt{2}V_{ac}}, \tag{5.9}$$

and the value of reactance X_i maintains the input power factor as:

$$X_i = \frac{V_{ac}^2\sqrt{k^2-1}}{P_i}. \tag{5.10}$$

In this design, the system was operated at unity power factor in which $V_{dc} = \sqrt{2}V_{ac}/2$. As a result, the input L filter and DC capacitance C were designed, respectively, as follows:

$$L = \frac{X_i}{\omega}, \qquad \Delta V_{C,ripple} = \frac{I_{C,ripple}}{\omega C}. \tag{5.11}$$

5.4 Gate Driver and PCB Design

5.4.1 Gate Driver Component Selection

Based on the ratings of the 2-phase AFPM motor (Table 4.1), the proposed AC/AC converter needs to be capable of 4.4 Arms with transient overshoots. CREE SiC MOSFET (C2M0280120D) rated at 10 Arms was selected to leave enough margin. For the gating voltages, it was recommended to employ around +20V and -5V for turning on and turning off the selected MOSFETs, respectively. Accordingly, Zener diodes (24V and 5.1 V) for gating voltage requirements and the DC/DC converter G1212S (to provide ±12 Vcc) were selected. The gating resistance was originally

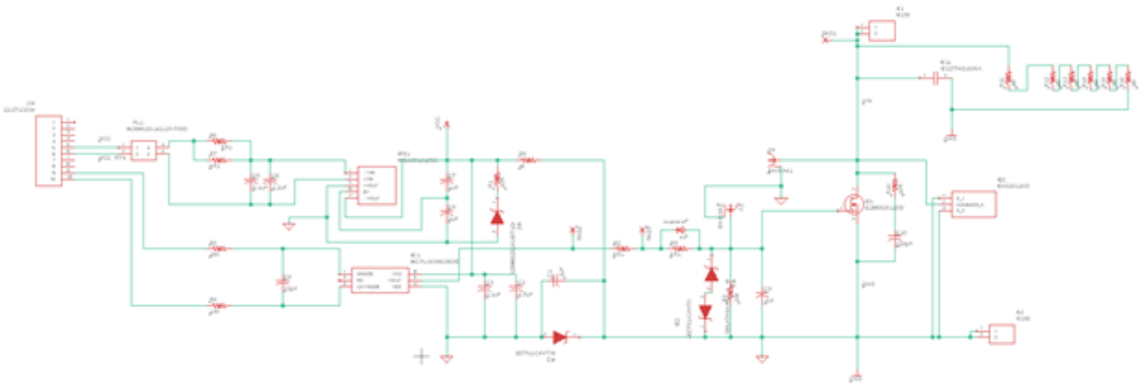


Figure 5.5: Gate driver circuit for one leg of the proposed integrated 2-phase AC/AC converter developed as part of this PhD research. The schematic for the other two legs are designed with the same layouts.

selected as 5Ω to avoid high dv/dt and resulting circuit faults. Further optimization on reducing gating resistance value would be the subject of future work to reduce power losses.

The schematic of the gate drive circuitry (Fig. 5.5) was designed with symmetric trace distance, which should introduce balance impendence on the gate drive. For PCB layout design (5.6), the gate drive should be placed as close as possible to the SiC MOSFETs. De-coupling film capacitors were placed close to the SiC devices, and it could reduce high frequency switching loop and bypass noise within the switching loop. The circuit protections including bypass capacitor, driver protection, dv/dt protection, turn-off circuit, and gate malfuction protection were carefully designed to build the prototype of the proposed integrated 2-phase AC/AC converter (Fig. 5.7).

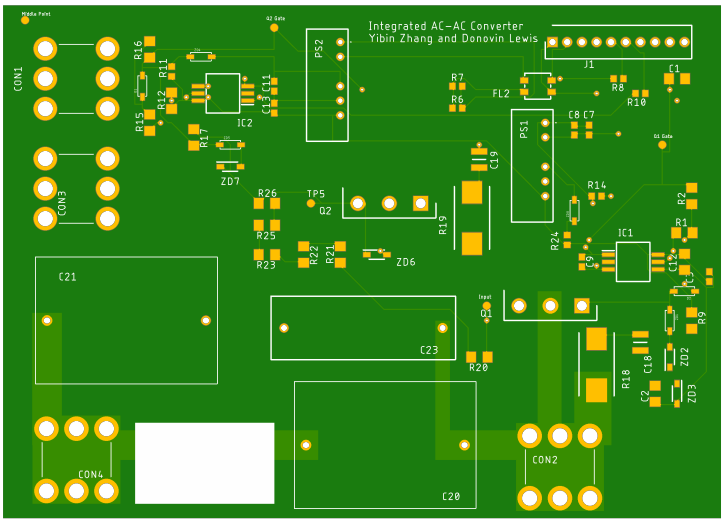


Figure 5.6: PCB layout of one leg of the 2-phase AC/AC converter developed as part of this PhD research. Gate driver circuit and power paths are included on the 2-layer PCB board.

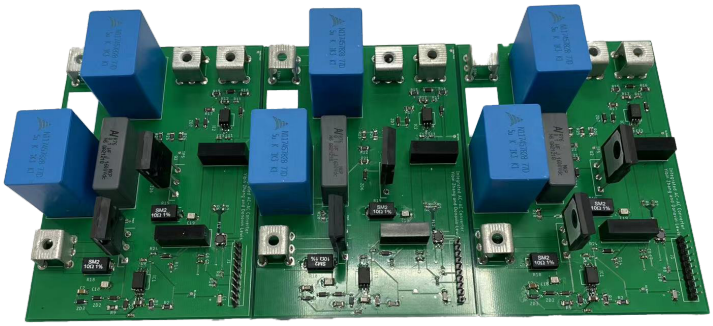


Figure 5.7: The prototype of the proposed integrated 2-phase AC/AC converter as part of this PhD research, which consists of 6 SiC MOSFET devices.

5.4.2 Bypass Capacitor Sizing

The MOSFET gate driver's bypass capacitor was calculated first. The bypass capacitor provided the gate drive current when the MOSFET was at turning-on. Two components were mainly considered: quiescent current and gate current.

With different input states, the quiescent current could change by ten times, which usually would cause a duty cycle dependent ripple across the bypass capacitor. This consideration was presented as:

$$\Delta V_Q = \frac{I_{Q,HI} \times D_{max}}{C_{DRV} \times f_{DRV}}. \tag{5.12}$$

Although in piratical operations, the actual current amplitude was not always certain as in the above equation, the voltage ripple could be estimated by using gate charge instead. As a result, the bypass capacitance and voltage ripple were calculated as:

$$\Delta V_{QG} = \frac{Q_G}{C_{DRV}}. \tag{5.13}$$

By solving the equations for C_{DRV}, the bypass capacitor value was found as:

$$\Delta C_{DRV} = \frac{I_{Q,HI} \times \frac{D_{max}}{f_{DRV}}}{\Delta V}, \tag{5.14}$$

where Q_G is the total gate charge, $I_{Q,HI}$ is the quiescent current of the driver at high input, D_{max} the maximum duty cycle of the driver at high state, and f_{DRV} the driver operating frequency.

In addition, the bypass capacitor was placed as close as possible to the IC (across bias and ground pins).

5.4.3 Driver Protection Design

Another important circuit feature was to protect the MOSFETs against reverse currents. Typically MOSFETs were capable of handling currents in one direction without any concerns, but were more difficult to sink currents with the opposite current direction. During MOSFET turning-on and turning-off, unavoidable oscillations between the power source and the input-side capacitor could happen and required the driver circuit to deal with current flowing in both direction. To offer this reverse flowing path, a low forward voltage drop Schottky diode was selected and placed as close as possible to both output pin and bypass capacitor to protect the outputs

5.4.4 Protection Design for dv/dt

Another key challenge for SiC MOSFET gate driver was dv/dt protection. With a much reduced on-resistance and capacitance, and higher achievable switching frequency, dv/dt for SiC MOSFETs could be extremely high and causing serious issues with capative or inductive loads. Especially at the start of powering up the system, a dv/dt protection such as a protection resistor between the gate and source could reliably prevent the dv/dt damage. The pull down resistor value was calculated based on the worst dv/dt case as follows:

$$R_{GS} < \frac{V_{TH}}{C_{GD}} \times \left(\frac{dt}{dv}\right)_{turn-on}. \tag{5.15}$$

The biggest challenge for this dv/dt protection design was to find the highest dv/dt that could occur and provide sufficient protection for that specific moment.

Another common situation required dv/dt protection was in regular operation

when turn-off dv/dt was forced across the drain-to-source terminals. Most resonant and soft switching converters could force a dv/dt across the main switch right after its turn-off instance, driven by the resonant components of the power stage [145]. It was necessary that the low output impedance of the gate drive circuit was to provide protection because V_{TH} was usually lower dv/dt. The design was conducted based on the following procedure. The maximum dv/dt was first determined. Second, by using the internal gate resistance $R_{G,I}$ and the gate-to-drain capacitance C_{GD} from the datasheetthe, the natural dv/dt limit was estimated for the selected Wolfspeed SiC MOSFETs as follows:

$$\frac{dv}{dt_{limit}} = \frac{V_{TH} - 0.007 \times (T_J - 25)}{R_{G,I} \times C_{GD}}, \tag{5.16}$$

where V_{TH} was the gate threshold at 25 $^{\circ}C$, and –0.007 the temperature coefficient of V_{TH}.

The resonant circuit maximum dv/dt should be lower than the natural dv/dt limit, or a negative gate bias voltage would be required. To this consideration, the maximum gate drive impedance was checked as following:

$$R_{max} = \frac{V_{TH} - 0.007 \times (T_J - 25)}{C_{GD}} \times \left(\frac{dt}{dv}\right)_{max}, \tag{5.17}$$

where $R_{max} = R_{LO+R_{GATE}+R_{G,I}}$

5.4.5 Turn-off Circuit Development

MOSFETs could be turned on without any concerns, and the turn-on speed could be adjusted by implementing a snubber resistor R_{GATE}. However, to turn off the SiC

MOSFETs, the fast turn off time (turn-off delay time plus falling time) might not give enough time to turn off the semiconductor. In this PCB design, turn-off diodes (D1 and D2 in Fig. 5.5 and Fig. 5.6) were added in the position of anti-parallel with the snubber resistor. The turn-off diodes D1 and D2 worked only when:

$$I_G > \frac{V_{D,FWD}}{R_{GATE}}. \tag{5.18}$$

Typically the turn-off diodes helped aggressively in the beginning of turning-off but helped very little when voltage was close to zero. As a result, this circuit only provided a significant reduction in turn-off delay time only incremental improvement on switching times and dv/dt immunity.

Turn-off speed enhancement circuits could be further developed by shunting out R_{GATE} at turn-off as follows:

$$\frac{dv}{dt} = \frac{V_{TH} - 0.007 \times (T_J - 25)}{\left(R_{G,J} + \frac{R_{GATE}+R_{LO}}{\beta}\right) \times C_{GD}}. \tag{5.19}$$

5.4.6 Gate Malfunction Prevention

When SiC MOSFET devices are turned on and off at a high switching frequency, the high dv/dt introduced by SiC MOSFETs may cause a significant voltage drop or increase considering the capacitance elements or the equivalent capacitance effect based on tray distance. If the induced voltage is high enough, the MOSFET device can be turned on by fault. To prevent this gate malfunction, a capacitor (C1 and C17 in Fig. 5.5) is added to maintain the gating voltage at off stage.

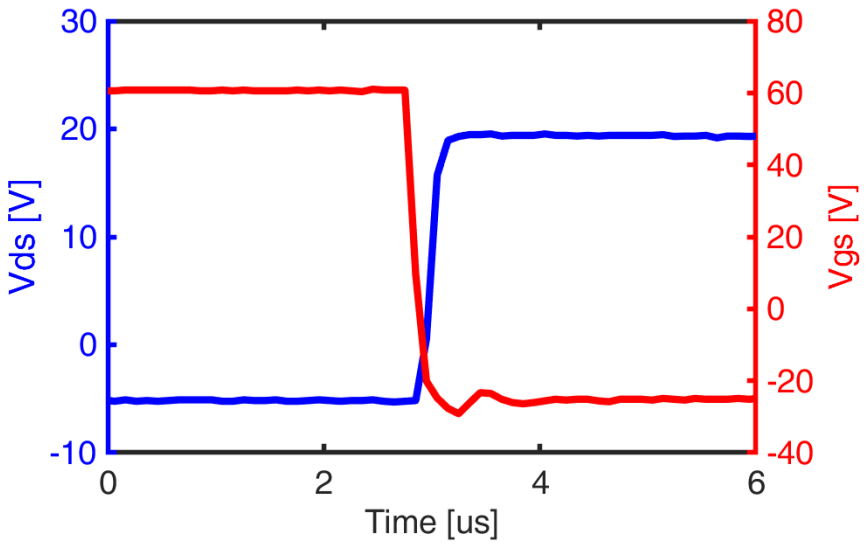


Figure 5.8: Double pulse testing results validate SiC MOSFET switching parameters are matching datasheet and the design.

5.4.7 Double Pulse Test to Evaluate Dynamic Behaviors of SiC MOSFETs

The first experimental validation of the PCB design was a double pulse testing for checking MOSFET switching parameters including turn-on delay time, rise time, turn-off delay time, and fall time. For example, to test the lower MOSFET on each leg of the converter prototype, an inductor was connected between mid point and +Vdc terminal. The upper MOSFET device was kept off, and gating signal to lower MOSFET was given a PWM signal. As a result, Vds and Vgs were measured (Fig. 5.4.7) at rising and falling edges. The measured turn-on time and turn-off time were 100 μS and 200 ns, respectively.

5.5 Simulation and Experimentation Validation

Simulation and experimentation were carried out to validate the feasibility and effectiveness of the proposed integrated AC/AC converter, AC/DC/AC converters, and matrix converters. With the residential electricity (single-phase AC 120Vrms, 60Hz in the United States), the conventional AC/DC/AC PWM converter was capable of providing 10A output current (Fig. 5.5), while the matrix converter with direct modulation method providing 3.1A under the same condition (Fig. 5.5). For the proposed integrated AC/AC converter, the output current under the same condition was up to 6.7A (Fig. 5.5).

By using Fast Fourier transform (FFT) tools to analyze the current results, the THD for the conventional AC/DC/AC converter, matrix converter, and the proposed integrated AC/AC converter showed 1.7%, 22.1%, and 3.7%, respectively (as shown in Fig. 5.12). A systematic comparison among these three topologies was listed in Table 5.2.

In addition, a speed closed-loop controller (Fig. 5.13) was developed and simulated to drive a two-phase axial flux PM machine using residential electricity as input AC source. Responses of motor speed and currents to a step change in the reference speed were presented in Fig. 5.5. With a conventional back-to-back converter, the rated speed of 3000rpm was reached (Fig. 5.5). In contrast, the proposed AC/AC converter and a matrix converter with direct modulation were able to be operated up to 2000rpm and 1830rpm (Fig. 5.5 and 5.5), respectively. The results of estimated electromagnetic torque and output phase currents were also presented and compared.

Furthermore, the prototype of the proposed AC/AC converter wass built for the designed two-phase axial flux PM motor drives using residential electricity (single-phase AC 120Vrms, 60Hz) as part of this PhD research. The PCB performance would be further enhanced by the fine tuning of component parameters such as the snubber resistance value. In this study, a RL load (resistor and inductor in series) was used to mimic AFPM motor phase resistance and inductance. The dSPACE control board generated gating signals to drive the converter. Based on the proposed modulation schemes, gating signals for the two phases were generated 90 electrical degrees apart from each other, matching the machine drive requirements. CREE SiC MOSFET power semiconductors C2M0280120D (rated at 1200V/10A and operated at switching frequency 5kHz and 50kHz) were employed for the prototype drive system. An experimental validation (Fig. 5.17) showed that with residential electricity, the ripple percentage of DC link voltage (Fig. 5.17a) was maintained within 5% by using developed DC link voltage filter) on rectification stage. The output two-phase currents on inversion stage (Fig. 5.17b) featured a acceptable ripple percentage with RL load ($R_s = 0.5\Omega$, $L_s = 1.9$mH) at 5 kHz. With the help of SiC MOSFETs, a higher switching frequency 50 kHZ was achieved and offers a reduced phase current ripple percentage.

5.6 Conclusion

This chapter proposed an integrated AC/AC converter for single-phase input and two-phase output motor drives, which reduced the switching device count to 6 and

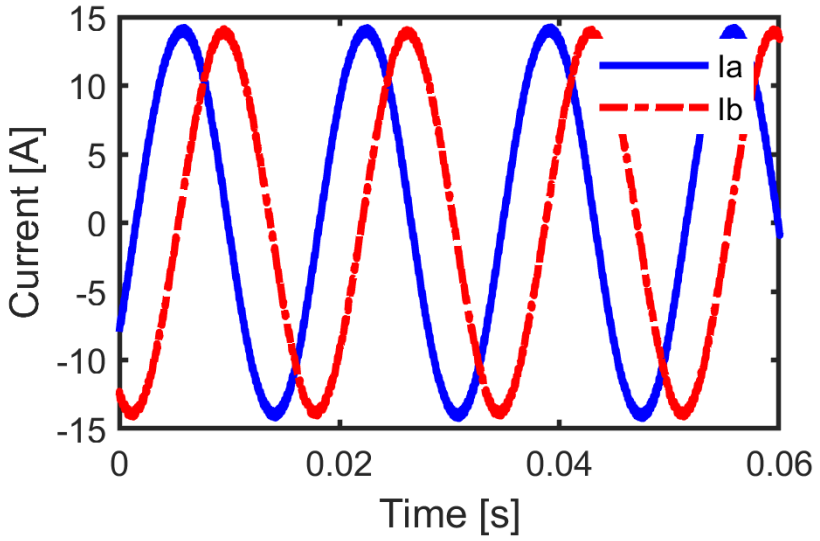


Figure 5.9: The output phase currents of a conventional single-phase to two-phase back-to-back converter.

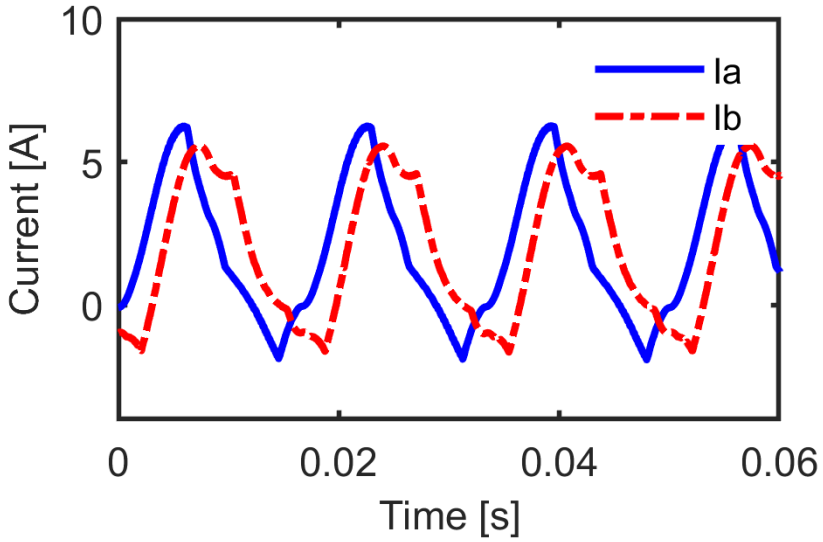


Figure 5.10: The output phase currents of a single-phase to two-phase matrix converter.

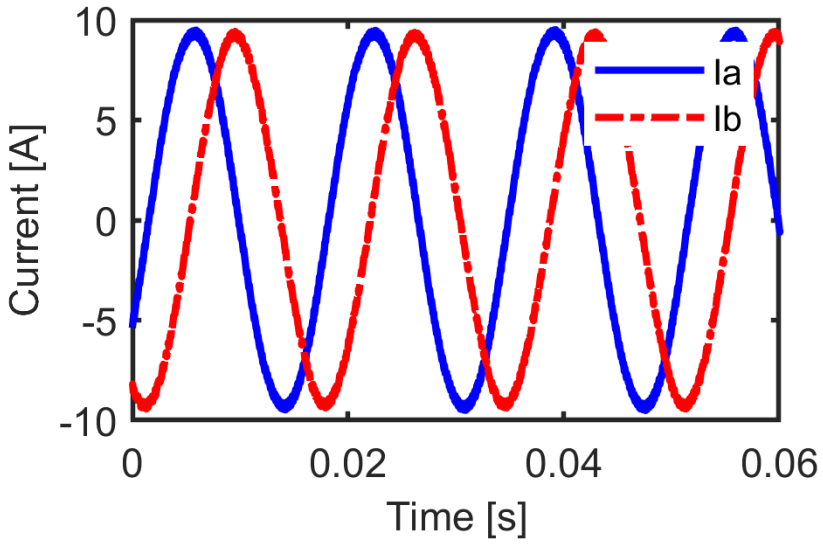


Figure 5.11: The output phase currents of the proposed integrated AC/AC converter.

Table 5.2: The comparison among the three topologies with the same input AC source (V_{ac} = 120Vrms) and the same loading ($R_{ph} = 1\Omega$, L_{ph} = 5mH).

Converter	Input filter	DC cap	Switch count	$V_{ph,rms}(\%)$	$I_{ph,rms}(A)$	$P_{out}(W)$	THD (%)
Conventional	Small	Small	12	100	10	271	1.7
Matrix	Small	No	8 bidirectional	61.2	3.1	21	22.1
Integrated AC/AC	Large	Large	6	66.7	6.7	167	3.7

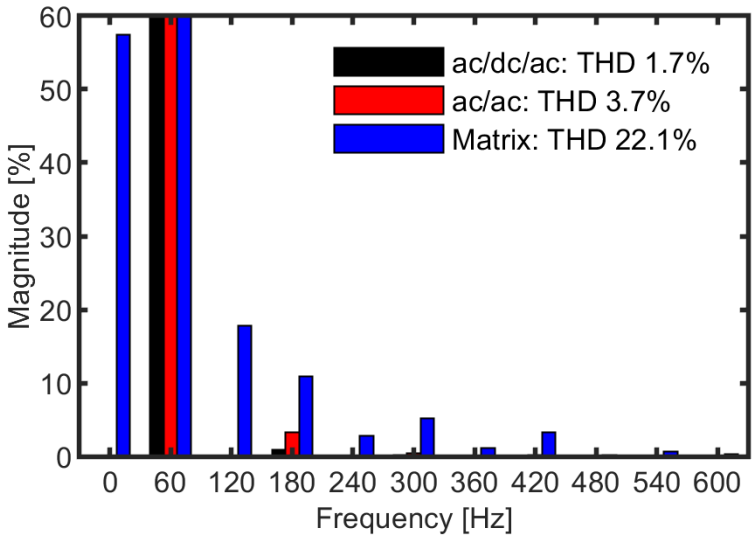


Figure 5.12: The current harmonic spectra in % of the magnitude at 60Hz fundamental frequency for the three types of converters.

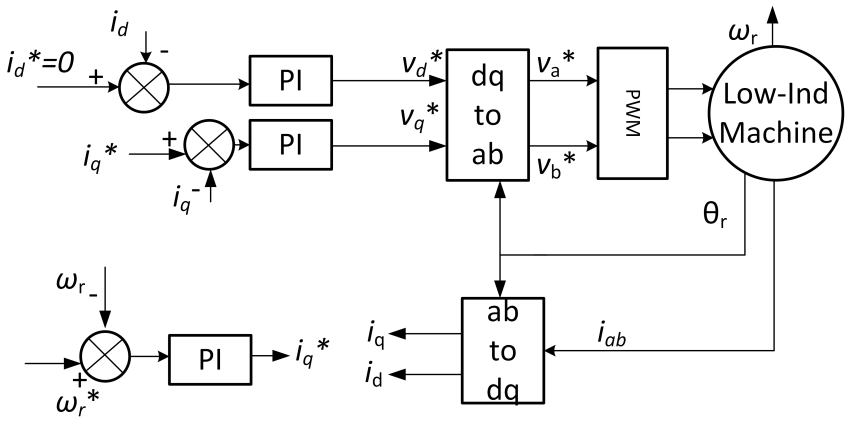


Figure 5.13: Closed-loop speed control strategy for a two-phase axial flux PM machine drive system.

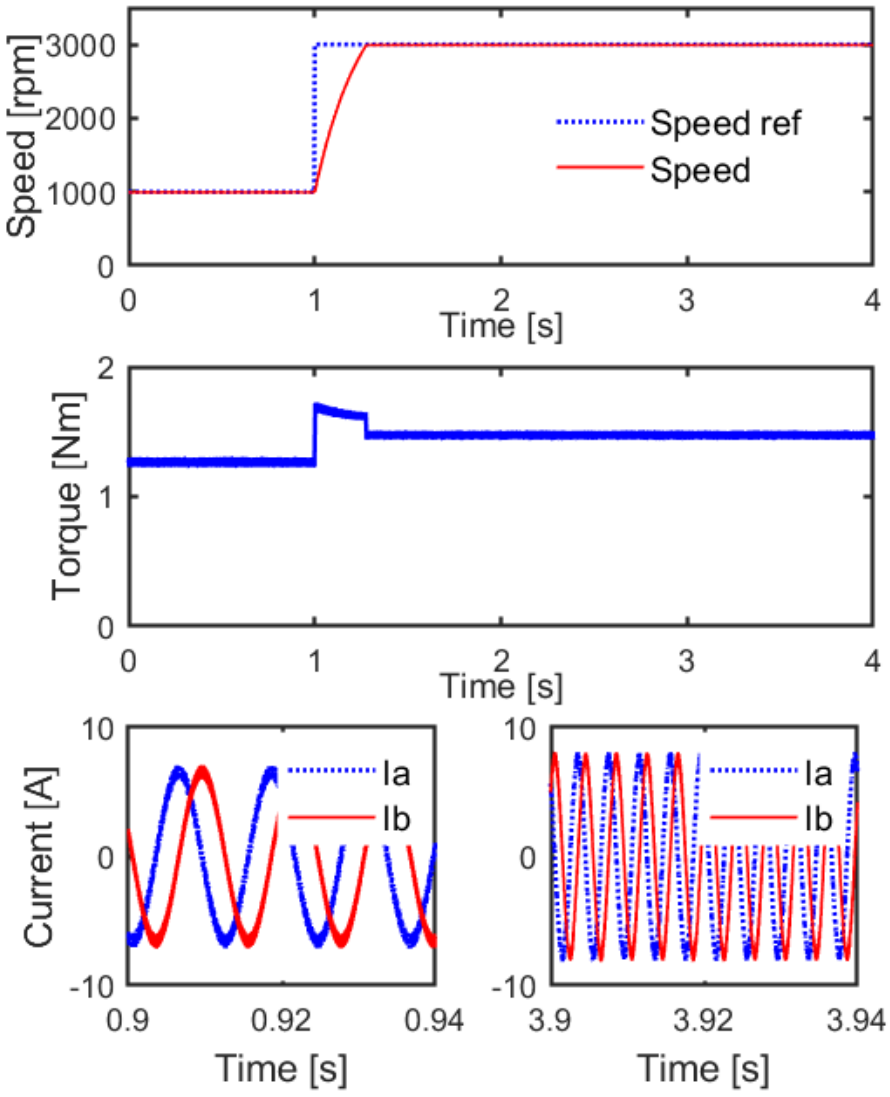


Figure 5.14: Simulation results, including the motor speed, estimated electromagnetic torque, and phase currents of closed-loop speed control for a two-phase axial flux PM motor drives in response to the reference speed step change from 1000rpm to maximum operating speed: a conventional single-phase to two-phase back-to-back converter.

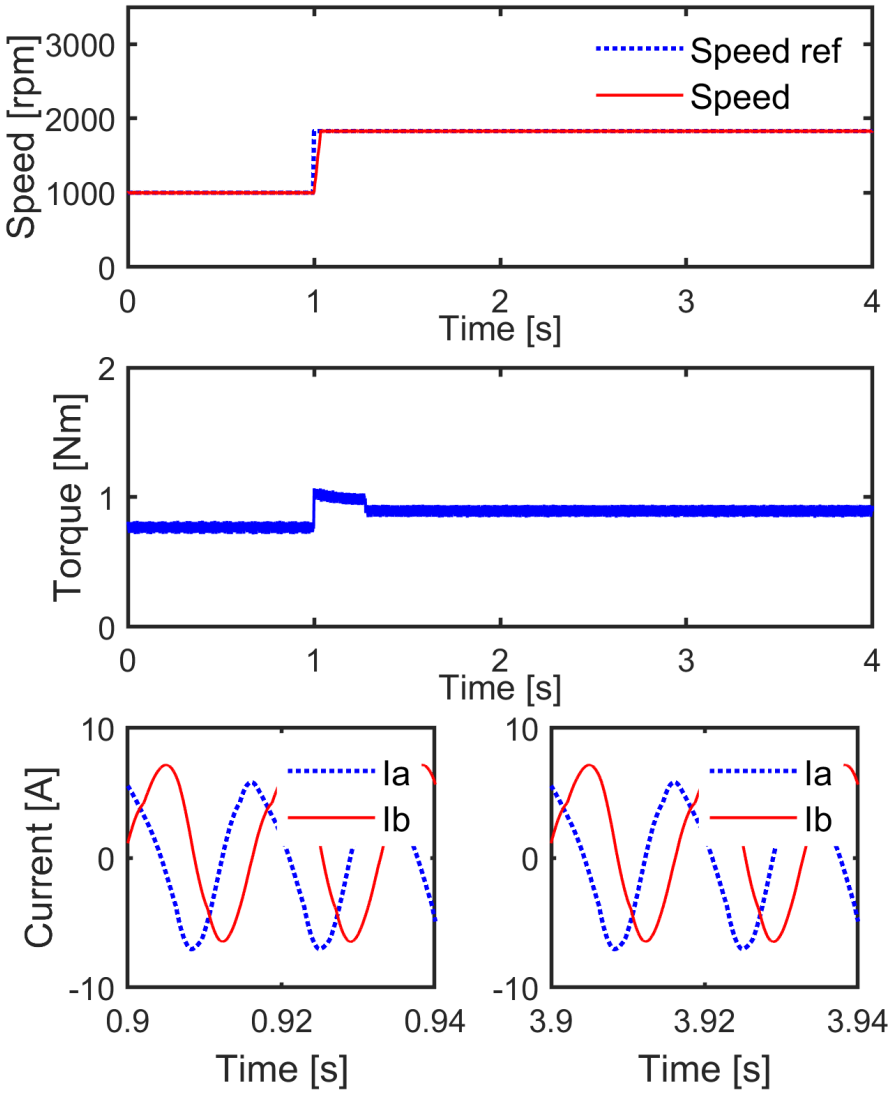


Figure 5.15: Simulation results, including the motor speed, estimated electromagnetic torque, and phase currents of closed-loop speed control for a two-phase axial flux PM motor drives in response to the reference speed step change from 1000rpm to maximum operating speed: a single-phase to two-phase matrix converter.

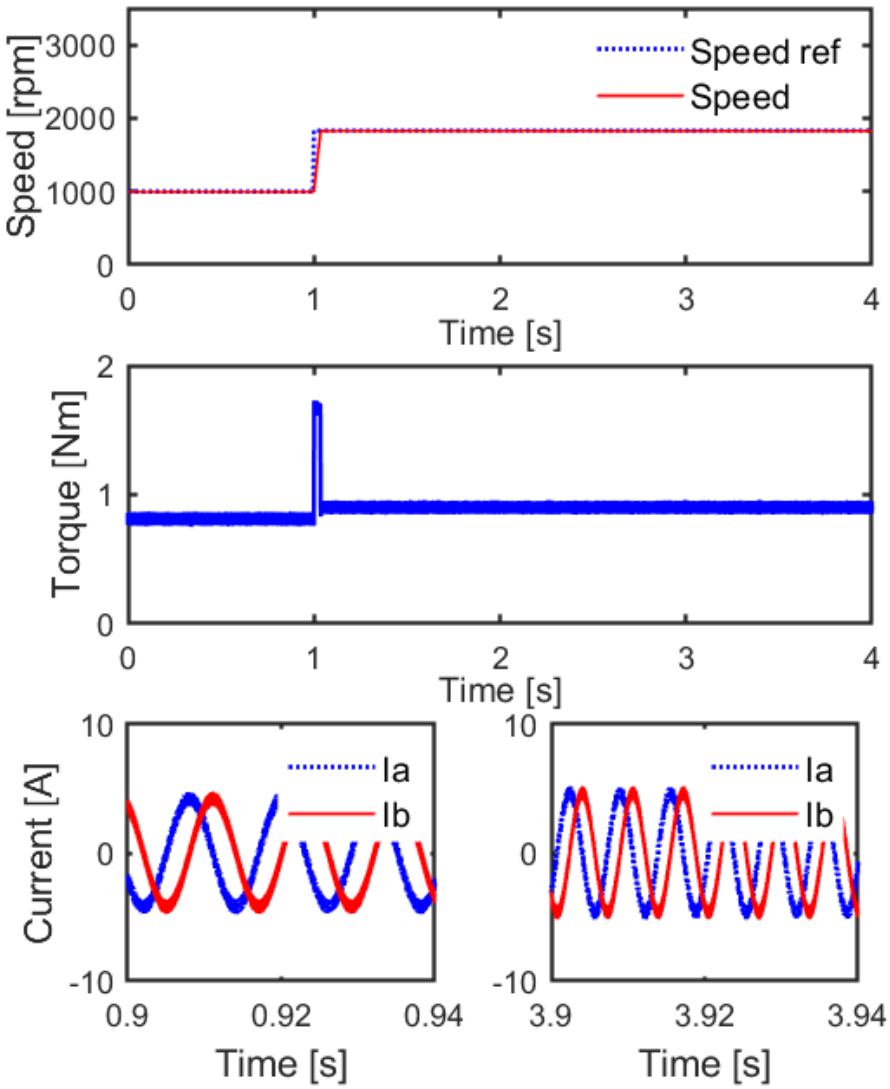
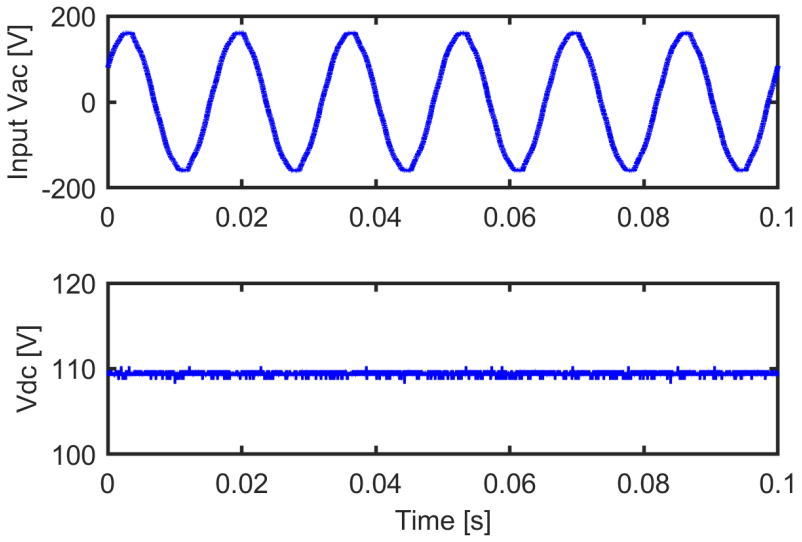


Figure 5.16: Simulation results, including the motor speed, estimated electromagnetic torque, and phase currents of closed-loop speed control for a two-phase axial flux PM motor drives in response to the reference speed step change from 1000rpm to maximum operating speed: the proposed integrated AC/AC converter.



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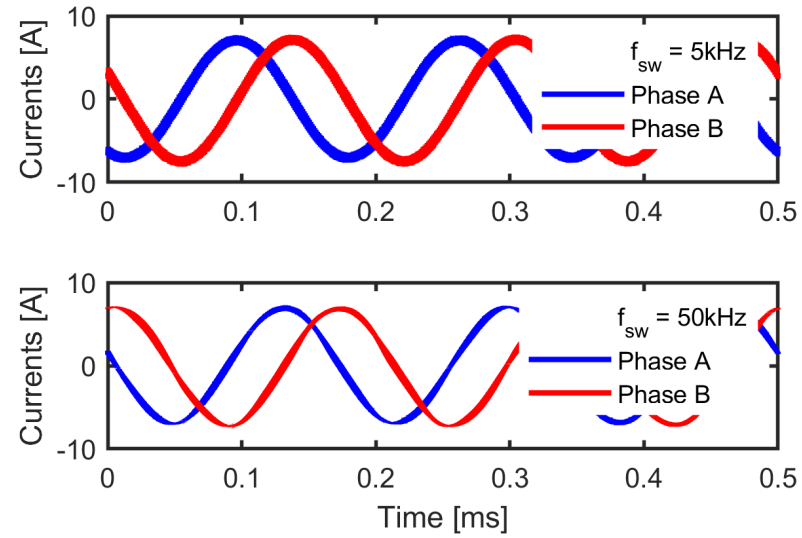


(b)

Figure 5.17: Experimental results of the proposed AC/AC converter, (a) input AC voltage and DC link voltage with developed voltage filter, and (b) output phase currents.

maintain the same functionality and output performance. Furthermore, a systematic comparative study of three converter topologies for single-phase to two-phase low-power motor drives, including topologies and associated modulation schemes, system cost, filter size, output voltage capability, speed operation range, and output distortion, was presented. The conventional AC/DC/AC topology was capable of providing the full output voltage capability with a low distortion (THD 1.7%); however, it required 12 active semiconductor switching devices and DC capacitors, which therefore dramatically increased the system cost. The matrix converter did not have any DC link; however, it still required a large number of switching devices (8 bidirectional modules) and offered a reduced output voltage range (61.2%) with a very high THD of 22.1% under the same condition. In the proposed topology, the switch count was largely reduced to 6 and the output distortion also remained low (THD 3.7%). The modulation scheme and filter design were also included. In addition, a prototype for a two-phase axial flux permanent magnet motor drive was built and the experimental results validated the effectiveness of the proposed AC/AC converter and converter control schemes.

Chapter 6

Bearing Voltage and Current in PWM Converter-fed PM Synchronous Machines

6.1 Introduction and Problem Formulation

PWM converters have pulsed voltage outputs featuring high dv/dt (voltage gradient) and high switching frequencies. The sum of the three-phase voltages is not zero and results in common mode voltage (CMV) with a waveform depends on the DC bus voltage, modulation strategy, and the switching frequency.

The high dv/dt of the CMV introduces displacement currents flowing through not only the bearing lubricant, but also winding insulation, which further results in varying flux encircling the machine shaft. The circular flux around the shaft may ultimately introduce currents that flow in bearings, both in the drive and non-drive end, depending on the housing structure. Bearing currents occur when the bearing voltage is high enough to overcome the breakdown voltage of the lubricant. In the case of ceramic bearings, the situation is different; Once the bearing currents occur, they will flow through and damage the surface of bearing raceways, leading to premature

bearing failures.

Without appropriate counter-measures for these effects, a machine bearing meybe prematurely or permanently destroyed. Approximately 9% of bearing failures in the cement industry are caused by bearing currents [71]. A growing number of bearing current induced premature bearing failures have been reported, calling for more research effort into bearing currents over the last decade and the associated mitigation techniques [70]. More recently, advanced wide band gap (WBG) devices such as SiC and GaN devices achieve faster turn on/off speed and lower on-state resistance. As a result, machine drives which incorporate WBG technology are often operated with higher switching frequencies ranging from a few hundreds of kHz to MHz and therefore exhibit higher dv/dt which poses new challenges for bearing reliability [68]. Unless otherwise stated, "bearing currents" in this research refers to PWM converter induced high-frequency currents flowing through the bearings.

High-frequency bearing currents mainly include: the non-circulating type caused by the shaft-to-frame voltage [146], the circulating type introduced by the shaft end-to-end voltage [147], and the leakage current to the ground [148]. The bearing voltage becomes a commonly-used indicator of bearing failures since all of these bearing current types depend on whether the voltage across the bearing is larger than the break-down value of the lubricant, which may vary from case to case [146], [70]. The flowing paths will be discussed in more detail later in this chapter.

The main contributions of this chapter include: proposed a coupled field-circuit finite element analysis (FEA) modeling approach for bearing voltage and current study in electric machines to take into account the influence of distributed winding

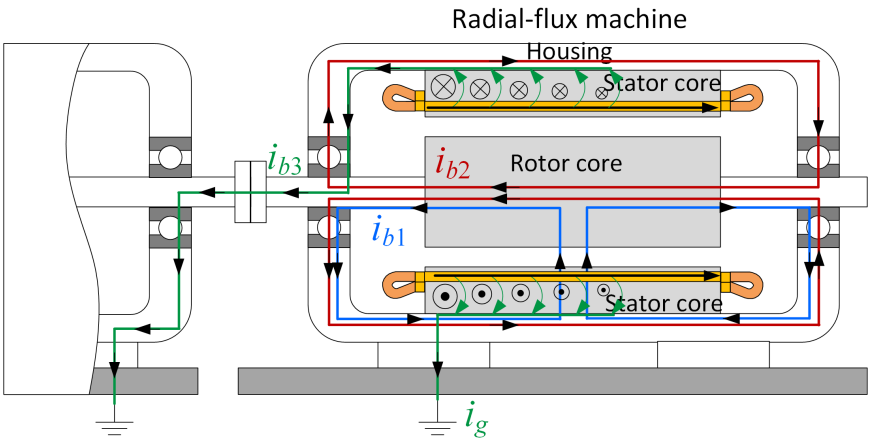
conductors and frequency dependency of winding resistance and inductance; proposed a parametric screening approach to estimate bearing capacitance; a stationary measurement approach was proposed to measure bearing capacitance, which did not require to develop a motor drive closed-loop control or loading conditions; the proposed approaches were validated based on two production motors: inside out E-type motor for static measurements and dynamic analysis, another I-type motor for static measurement; explained and modeled three known bearing current types based on the distributed-element circuit representation of electric machines and developed models in a unified way; investigated the bearing voltage sensitivity of capacitances between machine components; explored methods for computation time reduction and possible solutions to reduce bearing currents induced by WBG devices.

6.2 Main Types of Bearing Currents in Electric Machines

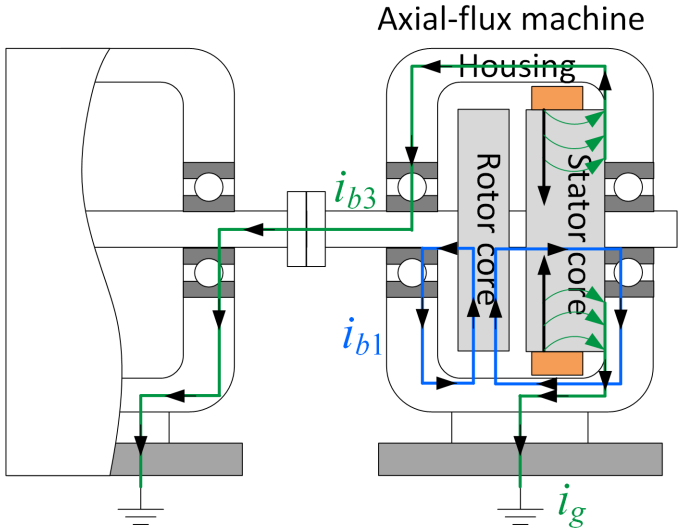
With inact bearing lubricant film, the bearing voltage v_b produced by the capacitive coupling is a function of the CMV at the winding terminals v_{com}, whose waveform mainly depends on the modulation scheme as shown in [149] - [150]. In steady state, the bearing voltage can be written concisely as:

$$v_b \text{ (steady)} = \frac{C_{wr}}{C_{wr} + C_{sr} + (C_{b,DE} + C_{b,NDE})} v_{com}, \tag{6.1}$$

where C_{wr} is the total capacitance between windings and rotor core, C_{sr} the total capacitance between stator and rotor cores, $C_{b,DE}$ and $C_{b,NDE}$ bearing capacitances



(a)



(b)

Figure 6.1: Possible flowing paths of bearing currents in: (a) radial-flux PM machines, (b) axial-flux PM machines. i_{b1} represents non-circulating bearing current, i_{b2} refers circulating bearing current, and i_{b3} is leakage current to the ground. There is no conductive path for the circulating bearing currents in E-type motor due to the cup-shaped outer PM rotor. The non-circulating type and ground leakage current still exist.

at the drive end and non-driven end, respectively (Fig. 6.1). It should be noted that, the rising and falling of CMV also introduce some transients in bearing voltages, which has not been fully considered in previous studies.

According to equation (6.1), the steady-state bearing voltage mirrors the waveform of the CMV. With the proposed modeling approach, it has been found that even in steady state, the bearing voltage to CMV ratio is related to the winding capacitances and frequency dependent, as shown in Fig. 6.2. Observations in [151] also confirm this frequency dependency. When the instantaneous bearing voltage is large enough to break down the lubricant film, the bearing current flow through the breakdown point and its amplitude will be determined by the overall voltage and impedance along the flowing path denoted by blue lines in Fig. 6.1.

The high dv/dt at the winding terminals causes additional displacement currents mainly flowing into the stator core through the winding insulation due to the winding-to-stator-core capacitance C_{ws}. The frequencies of these currents range from a few kHz to several MHz. These currents excite a circular magnetic flux around the machine shaft similar to that introduced by magnetic asymmetries, which further induces a shaft end-to-end voltage v_{sh}, which can be calculated by:

$$v_{sh}(t) = -\frac{d\psi_{cir}}{dt} = -\frac{d}{dt}\int_0^{2\pi}\int_0^{Ro} B_t(r,\theta,t) L_{stk} dr d\theta, \tag{6.2}$$

where ψ_{cir} is the circular flux around the shaft, R_o the radius of the selected region for calculation, $B_t(r,\theta,t)$ the tangential component of the flux density as a function of radius r, angle θ and time t, and lastly, L_{stk} the stack length.

If v_{sh} is large enough to break down the lubricant films of the drive-end bearing

and non-drive-end bearing, a circulating type bearing current will flow along the loop "housing - non-drive end - shaft - drive end" [147], as denoted by red lines in Fig. 6.1. Therefore, the bearing currents in the drive-end and non-drive-end bearings are of the opposite directions, whose amplitude depends on the shaft end-to-end voltage induced by the circulating flux and the overall impedance of flowing path.

If the rotor of the machine under study or the load machine is grounded and has a significantly lower impedance path than the grounding of its housing, as denoted by green lines in Fig. 6.1, the capacitive currents produced by the high dv/dt at the winding terminals may flow partly as the rotor-to-ground leakage current through the bearings. A typical example for the rotor-to-ground leakage current via the driven machine has been presented in [148]. This type of bearing current is caused by the impedance difference between possible flowing paths so it is inherently modeled once all the components, such as grounding and supplying cables, driven machines, couplers, etc, are included.

In radial-flux machines, all of the three types of bearing current may occur, and their flowing paths have been illustrated in Fig. 6.1a. For axial-flux machines, the non-circulating bearing current and ground leakage current exist. There is still no clear evidence on whether there is the circulating bearing current in axial-flux machines, which needs more careful examination. Therefore, only the flowing paths of the non-circulating current and ground leakage current are plotted in the axial-flux machine shown in Fig. 6.1b.

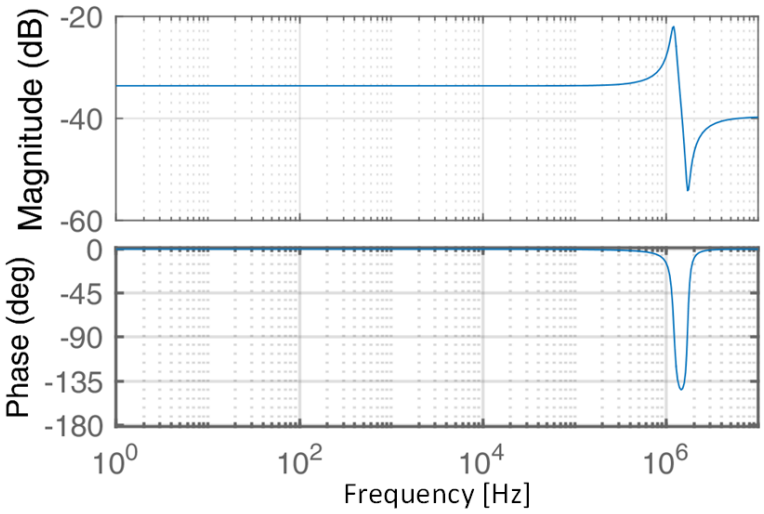


Figure 6.2: Frequency dependency of bearing voltage to CMV ratio showing the importance of predicting bearing current transients at varied frequencies (non-circulating type).

6.3 FEA based Modeling, Time-domain Analysis, and Experimental Measurements on Rotating Machines

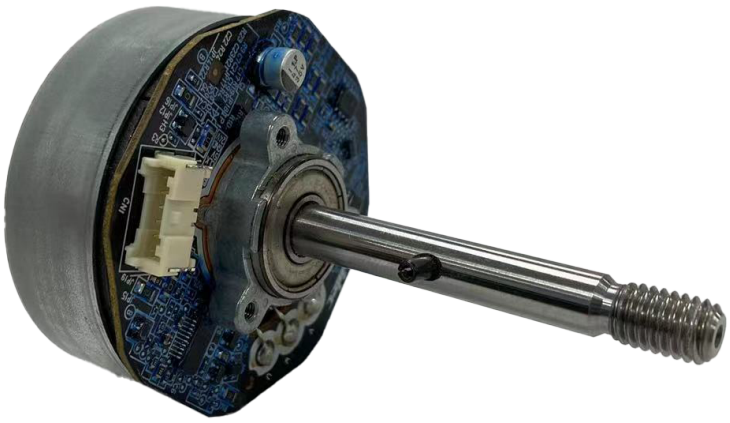
6.3.1 Electromagnetic FEA

Accurate techniques are needed for the modeling of bearing voltage and current in electric machines such as the detailed distribution of winding conductors (turns), frequency dependency of winding RL parameters, and variation of bearing capacitance. Previous studies by other authors mainly focus on the steady state value of bearing voltages in radial-flux machines, i.e., the bearing voltage to CMV ratio, and model the bearing voltages using equivalent circuits for frequency-domain analysis. The frequency-dependent winding RL parameters extracted from eddy-current solvers cannot fully capture the time transient variations and therefore this approach

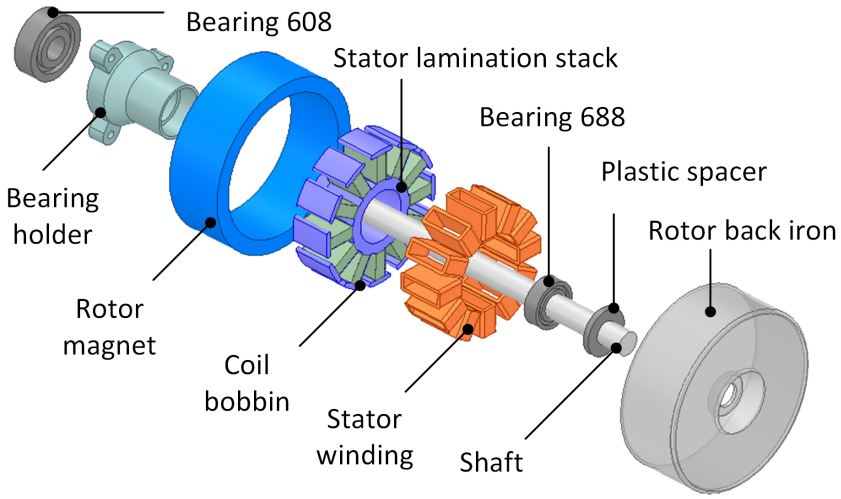
encounters difficulties in accurate time-domain analysis.

An inside out E-type motor [152], which was a 12-slot and 10-pole permanent magnet synchronous machine (PMSM) as shown in Fig. 6.3, was used and modeled in Ansys Maxwell for validating the proposed time-domain analysis approach. Specifically, the E-type motor as illustrated in Fig. 6.3b had a cup-shaped external rotor structure and the bearing currents caused by the CMV and machine-related capacitors are the dominating component, as shown by the measured waveforms in Fig. 6.4. The voltage across the bearing lubricant film in steel ball bearings, i.e., the bearing voltage v_b, can be the result by the electrostatic charge accumulation, the CMV through capacitive coupling, and the circular flux created by displacement currents through the winding insulation or magnetic asymmetry via inductive coupling. Bearing currents occur when the bearing voltage is high enough to overcome the breakdown voltage of the lubricant. In the case of ceramic bearings, the situation is different; once the bearing currents occur, they will flow through and damage the surface of bearing raceways, leading to premature bearing failures.

A coupled field-circuit electromagnetic FEA and experimental measurement based approach for the modeling of bearing voltage and current has been presented by a group of authors from our SPARK Lab at UK [153] - [154]. A 3D electrostatic FEA of the E-type motor was developed in Ansys Maxwell (Fig. 6.5). The 3D mesh for the electrostatic model was described as in Fig. 6.5b. There were in total 29.14 million tetrahedral elements and it took 35 hours to solve the problem on a high-performance PC with an 8-core Intel Xeon processor and 128GB RAM. By defining different excitation nodes and using an electrostatic solver, capacitances in the E-type



(a)



(b)

Figure 6.3: The E-type PMSM motor for FEA modeling and time-domain analysis as part of the PhD research. (a) the E-type production motor, and (b) exploded view of a E-type PMSM, which has a cup-shaped outer PM rotor.

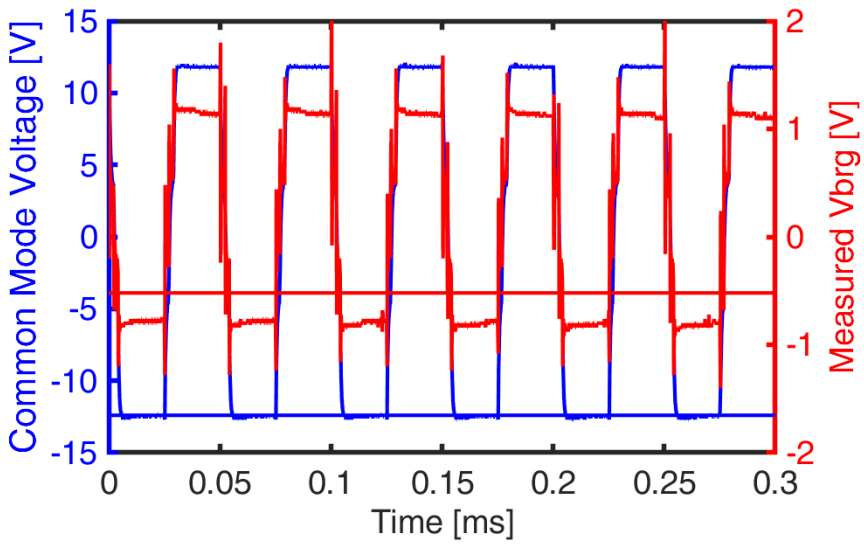
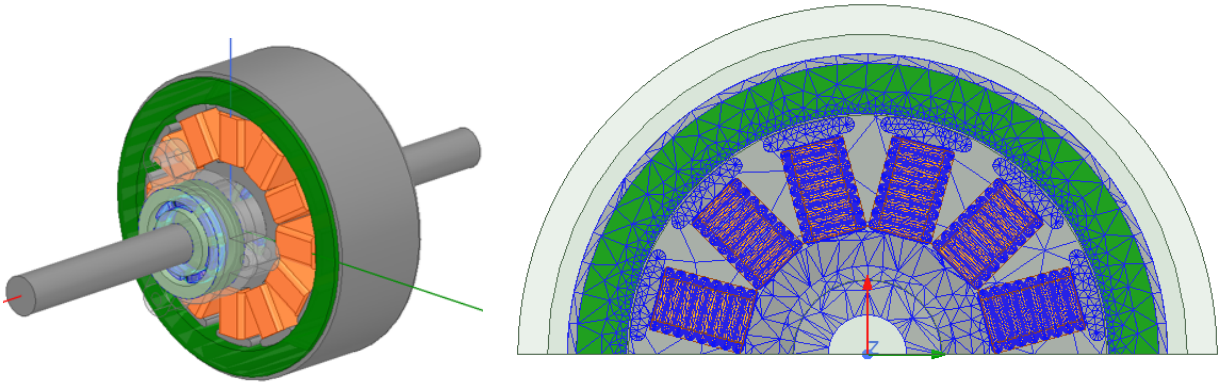


Figure 6.4: Measured bearing voltage and common mode voltage (CMV) for the E-type PMSM shown in Fig. 6.3b at 1,500 rpm using ceramic ball bearings. Bearing voltage peak spikes, as seen here, may induce large currents, further contributing to premature failure of the bearing.

motor were calculated and therefore incorporated into a detailed external circuit (Fig. 6.6). Individual turns were modeled by a Π- or Γ-shaped circuit element. As a result, the distribution effect of conductors was taken into consideration and bearing voltage transients could be captured.

Through a detailed comparison study, the research conducted as part of this PhD research has demonstrated that when the coupled external circuit is distributed enough, i.e., with a sufficiently large number of turns, the predicted bearing voltages are the same no matter whether the Π- or Γ-shaped circuit element is used. A typical example of the external circuit for bearing voltage and current study following this approach is visualized in Fig. 6.7. For clarity and faster calculations, only capacitors with a coupling coefficient no smaller than 0.05 are included, which corresponds to the triangular regions in Fig. 6.7. For automated analysis, the external circuit may



(a) (b)

Figure 6.5: FEA model of the E-type motor with detailed winding modeling. (a) 3D FEA model, and (b) mesh plot on Z-axis orient with more than 29 million tetrahedral elements.

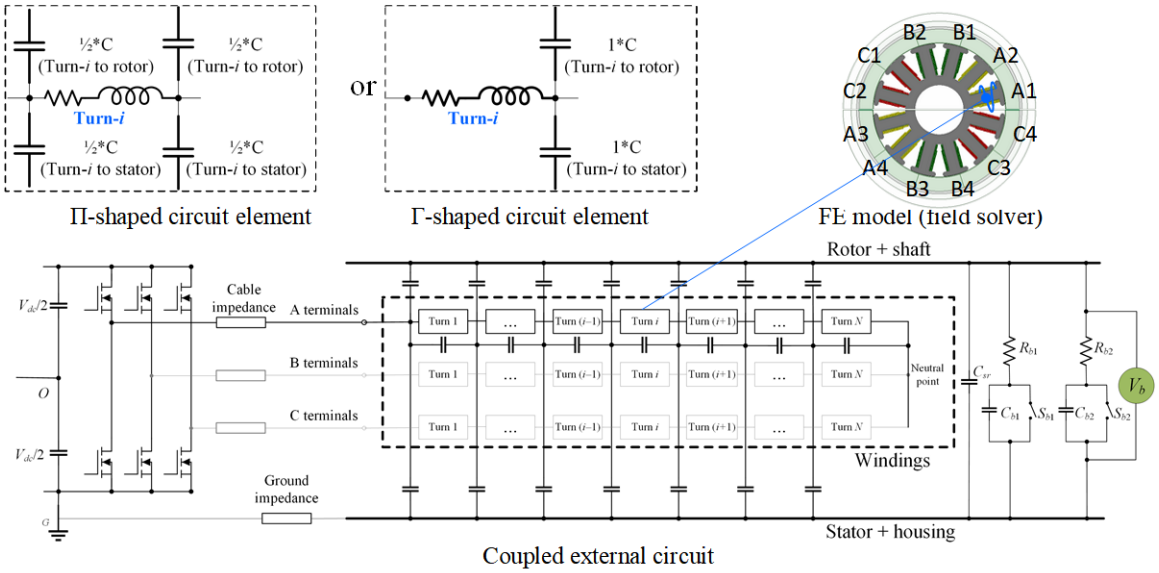


Figure 6.6: Illustrated for the proposed modeling approach for bearing voltage and current based on coupled field-circuit electromagnetic FEA and experimental measurements. The details of winding wires are included in the FEA model. The connection of winding turns and the capacitors are included in the coupled external circuit. The bearing capacitances are measured from experiments using the approach presented in [153]. The FEA model and coupled external circuit are solved together step by step to obtain the waveforms of bearing voltages, bearing currents, and voltage distribution in the winding turns.

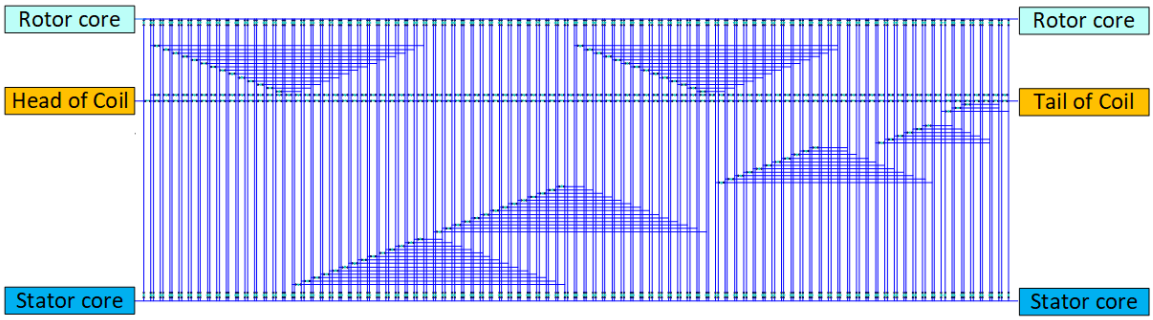


Figure 6.7: Example of the coupled external circuit segment for one coil with 92 turns. Capacitors with low coupling coefficients are not shown in the circuit for simplicity.

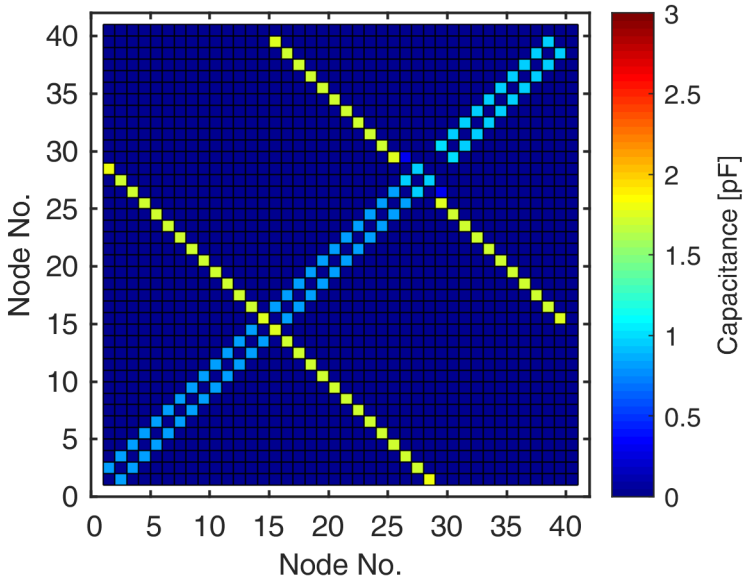


Figure 6.8: Capacitance matrix for one coil of Phase B winding from 2D FEA

be edited using scripts to describe the connection between electrical nodes.

6.3.2 Parametric Screening Approach for Bearing Capacitance Estimation

In real applications, bearing current cannot be measured because the bearing current flowing path is not accessible for current probes or sensors. Additionally, bearing capacitance varies at different speed and loading condition. A repeatable measurement of bearing current/capacitance of a rotating machine requires a drive system and operation at exactly the same speed and loading condition. In this following, an parametric screening approach combining FEA analysis and experimentation is proposed to accurately estimate bearing capacitance.

Based on the advanced FEA approach described in the previous section, a detailed model of the motor under study was identified in Ansys Maxwell. The equivalent capacitances between any two nodes were obtained, by defining different nodes of motor components and excitation voltages (Table 6.1). Moreover, a direct measurement by using LCR meter was conducted to validate the capacitance results obtained from FEA analysis. The capacitors C_{w-s} between winding and stator, C_{s-r} between stator and rotor, and C_{w-r} between winding and rotor were measured between one phase coil terminal and stator core, between stator core and shaft (rotor and shaft were conducted), and between winding and shaft, respectively. According to the calculated capacitance matrix, an equivalent circuit of the motor was built (Fig. 6.9) to represent the voltage distribution inside the motor. In this equivalent circuit, the capacitance values of bearings were unknown and was calculated by using the following

Table 6.1: Extracted capacitance matrix based on 3D FEA.

Capacitance	FEA [pF]	LCR measurement [pF]	Percentage difference [%]
Winding - stator	316.3	299.9	5.2
Stator - rotor	64.9	71.5	9.2
Winding - rotor	4.5	3.8	18.4

proposed parametric screening approach.

By experimentally applying the CMV at the machine input terminals, the voltage between motor shaft and grounding v_{sh-gnd} was measured. Both CMV voltage data and v_{sh-gnd} data was then imported to the circuit study. A parametric study was programmed to identify the bearing capacitance value at which the simulated bearing voltage matched the experimentally measured waveform v_{sh-gnd}. The mean values for both the high-state and low-state of v_{sh-gnd} were calculated. The minimum error percentage between simulated and tested V_{sh-gnd} by sweeping bearing capacitance values was calculated and plotted:

$$min \sum |\frac{V_t(h) - V_s(h)}{V_t(h)}| \times 100\% + |\frac{V_t(l) - V_s(l)}{V_t(l)}| \times 100\%, \tag{6.3}$$

where $V_t(h)$ is the mean value of tested high-state bearing voltage, $V_s(h)$ the mean value of simulated high-state bearing voltage, $V_t(l)$ the mean value of tested low-state bearing voltage, and $V_s(l)$ the mean value of simulated low-state bearing voltage.

6.3.3 Testing and Validation

A rotating test was conducted for the E-type PMSM. The E-type motor was operated at 1500 rpm by employing a closed loop motor drive control. The CMV measured at input terminals and bearing voltage measured between the shaft and

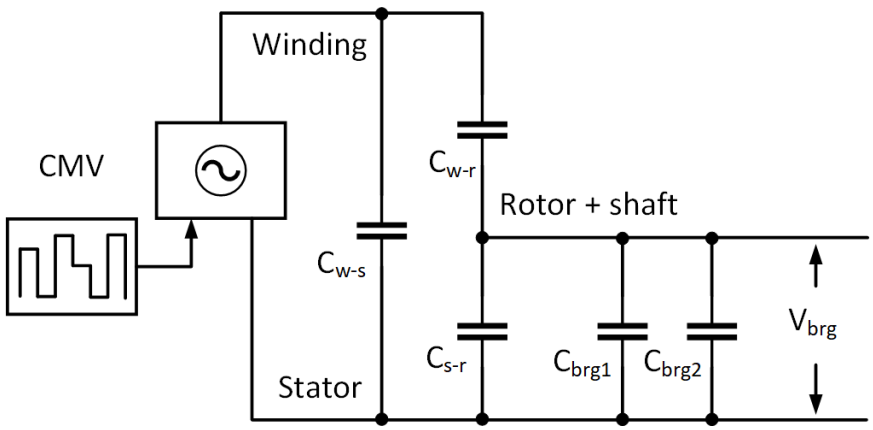


Figure 6.9: High frequency equivalent circuit for a motor used for analyzing bearing voltage.

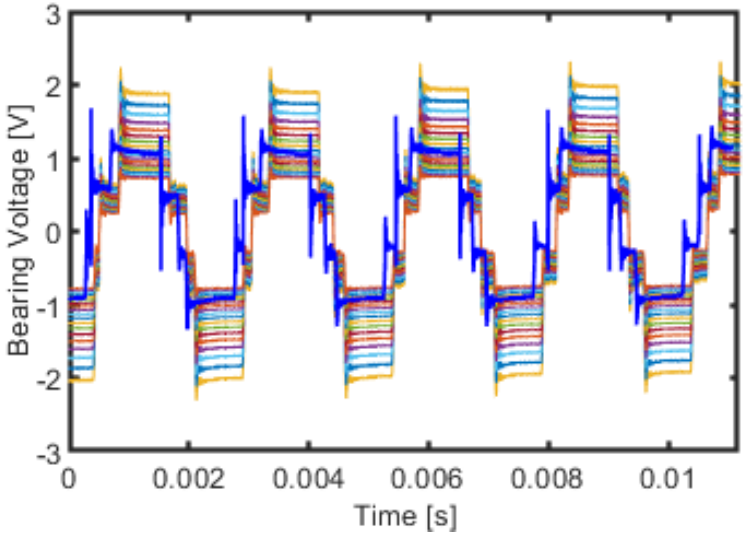


Figure 6.10: Parametric screening of bearing capacitances swept from 5 pF to 140 pF. Bearing voltage profile corresponds to the bearing capacitance. The larger bearing capacitance leads to lower bearing voltage.

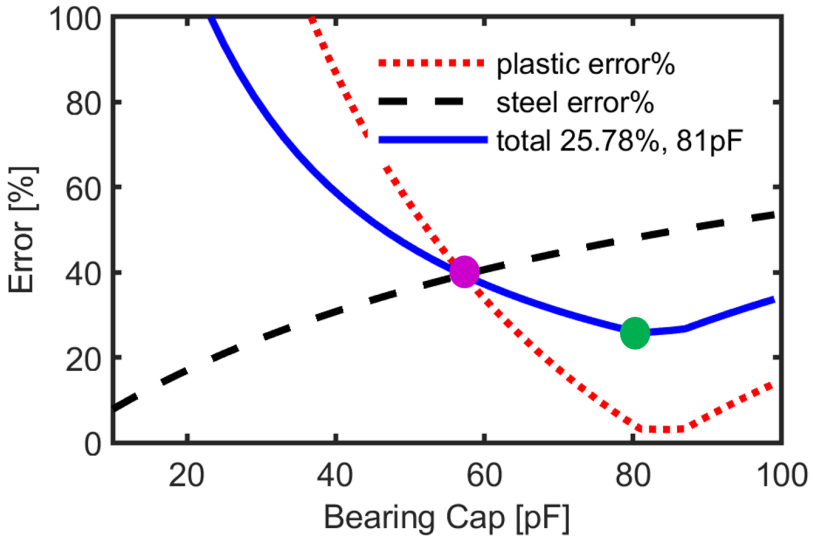


Figure 6.11: The total error percentage trend through the screening range of bearing capacitance values. The green point indicates the minimal total error percentage of ceramic bearing and steel bearing. The pink point represents the same error percentage in ceramic bearing and steel bearing screenings.

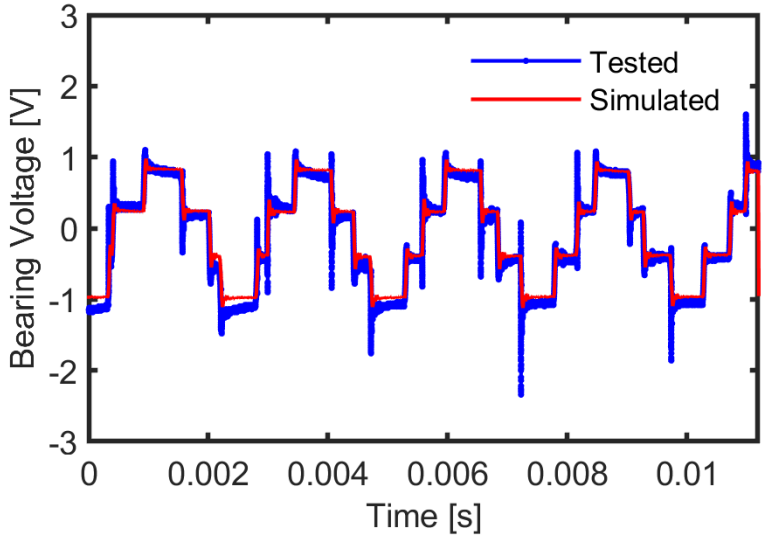


Figure 6.12: The experimental bearing voltage and simulated bearing voltage illustrate the satisfactory fitting results based on the estimated bearing capacitance 81 pF in the proposed parametric screening approach.

ground showed -332 Vpk and -1.06 Vpk, respectively (Fig. 6.4). By using the high frequency equivalent circuit of the E-type PMSM extracted from the proposed FEA approach, the proposed parametric screening approach was validated and used to estimate the bearing capacitance (Fig. 6.10). A bearing capacitance sweep between 5 and 140 pF (sweeping step 1pF) yielded the simulated bearing voltage from 2V to 0.6V accordingly. Furthermore, the total error percentage as described in equation (6.3) was calculated (Fig. 6.11).

The capacitance at the lowest total error percentage was selected as the closest capacitance value for ball bearing. For this study, the extracted bearing capacitance was 81 pF, based on the total error percentage through the screening capacitance range (Fig. 6.10). The simulated bearing voltage (Fig. 6.12) showed a satisfactory result in fitting the experimental results based on the estimated bearing capacitance.

To quantify the circular flux around the shaft and the introduced shaft end-to-end voltage using electromagnetic FEA, the rotor center of the E-type PMSM was adjusted to provided a 1 degree eccentricity. The flux contour under loaded condition with rotor eccentricity shows some asymmetry. By using equation (6.2), the shaft end-to-end voltage v_{sh} can be obtained, as shown in Fig. 6.13. Specifically $V_{sh} = 0$ indicates the shaft end-to-end voltage without rotor eccentricity.

Similar to the magnetic asymmetry introduced by rotor eccentricity, the displacement currents through the winding insulation led to a non-zero net current in the machine cross section and consequently created similar circular flux ψ_{cir} and shaft end-to-end voltage. By incorporating this voltage into the model illustrated in Fig. 6.6, the circulating bearing current was also taken into account.

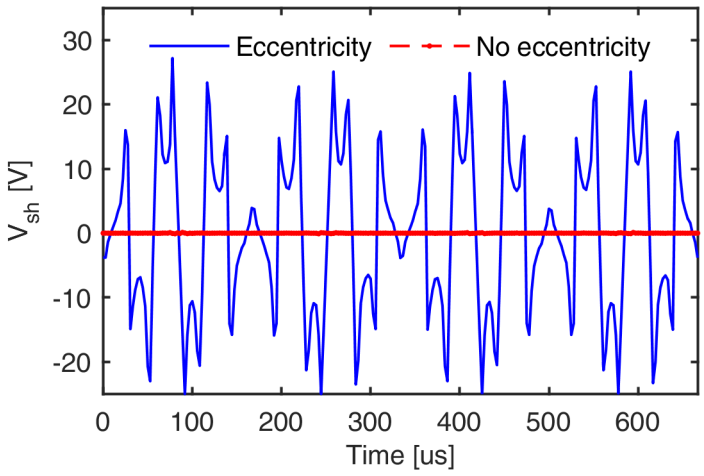


Figure 6.13: Shaft voltage waveforms v_{sh} in a 12s10p PMSM with 1mm static rotor eccentricity and without rotor eccentricity. The amplitude depends on the eccentricity and rotor speed (circulating type).

6.3.4 Sensitivity Study

By comparing the capacitance results (Table 6.1) of electric motors, every capacitance between two nodes has a very different range. The capacitance between winding and stator C_{w-s} ranges around 1 uF, while the capacitance between stator and shaft ranges at pF level. It is important to know which capacitor dominates the bearing voltage or contributes the most to the voltage distribution.

A schematic sensitivity study was proposed to investigate the contributions of each capacitor on bearing voltage. The base value for each capacitor value was the extracted capacitance value in the FEA approach as shown in the capacitance matrix (Table. 6.1). When investigating the sensitivity of one capacitor, all other capacitance values were kept at their base values, and the studied capacitor value was swept from 50% to 150% of its base capacitance value. In this way, the sensitivity results

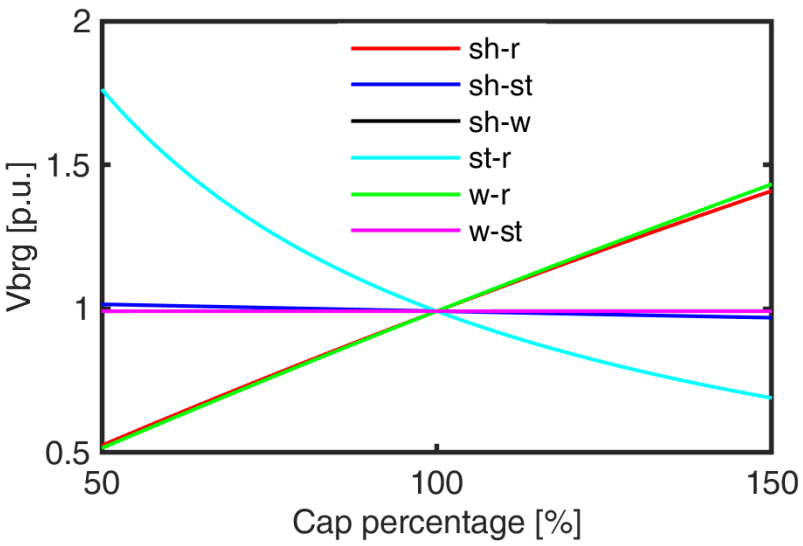


Figure 6.14: The relationship between bearing voltage and equivalent capacitance between pairs of nodes. sh indicates the node of shaft, r the rotor, st the stator, and w the winding, respectively.

of each capacitor were obtained in Fig. 6.14. Although C_{w-s} showed a large capacitance value, it was not the dominant capacitance for bearing voltage. The capacitors between winding and rotor C_{w-r}, shaft and rotor C_{sh-r}, and between stator and rotor C_{st-r} were the most sensitive components among the capacitors in this research for bearing voltage.

6.3.5 Discussion on Reduction of Computation Time

The proposed method has a high fidelity in terms of the bearing voltage and current calculations, but at the same time, requires large computational efforts since it involves the detailed modeling of winding turns and predicts the voltage and current in very fine time steps (ns level) and long time intervals (μs level) to capture the fast transients. Therefore, the potential reduction of model complexity and computation time is also necessary.

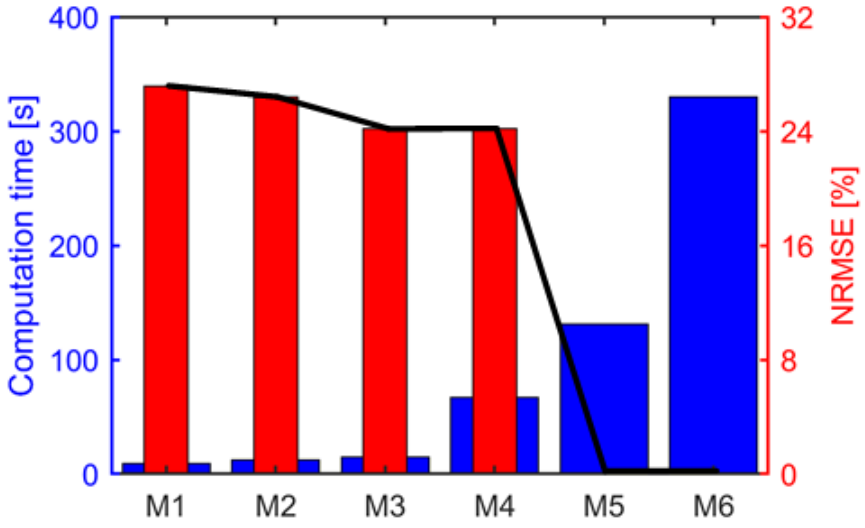


Figure 6.15: Computation time and NRMSE for models. M1 – 92 turns per FE coil; M2, M3, M4 and M5 – 46, 23, 4, and 2 turns per FE coil, respectively; M6 – 1 turn per FE coil.

Different models were built and compared: Model 1 (M1 in Fig. 6.15) represented 92 real turns by 1 coupled turn per coil in Maxwell, M2 46 turns, M3 23 turns, M4 4 turns, M5 2 turns, and M6 1 turn per coil, respectively. The computation time for each model was recorded: M1 9s, M2 12s, M3 15s, M4 67s, M5 131s, and M6 330s.

One effective approach to reducing the computation time was to reduce the number of turns in the coupled external circuit because the time-stepping scheme used in this research required multiple FEA calculations to extract the resistance and inductance matrices for each time step. A comparison of 6 models in terms of computation time and normalized root mean square error (NRMSE) was plotted in Fig. 6.15, showing the feasibility of this approach. NRMSE was defined as:

$$NRMSE = \frac{RMSE}{\bar{O}}, \tag{6.4}$$

where $\bar{O}$ is the average value from the baseline model. RMSE is the root mean square

error, and it can be calculated by:

$$RMSE = \sqrt{\frac{\sum_{i=1}^{n}(X_{b,i} - X_{m,i})^2}{n}}, \tag{6.5}$$

where $X_{b,i}$ and $X_{m,i}$ are values from the baseline model and studied model, respectively. n is the number of temporal data points. In the example shown in Fig. 6.15, M6 is the baseline model and all the other models are compared with it.

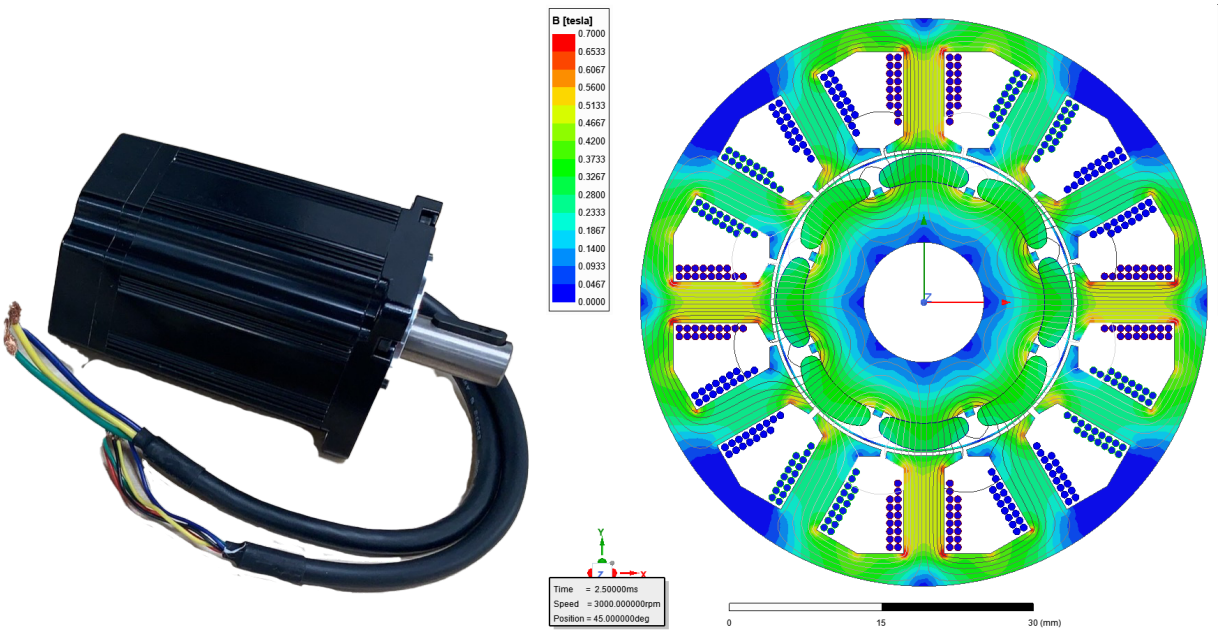
With two real turns represented by 1 in the coupled circuit, the computation time was reduced from 330s to 131s without losing the accuracy. Other approaches, including optimizing the time-stepping scheme, optimizing the number of real turns per circuit coil, simplifying the external circuit by neglecting the insignificant capacitors, using adaptive time step size, etc., can be further contributions for future studies.

6.4 Modeling, Analysis and Experimentation for Special Stationary Testing

6.4.1 Electromagnetic FEA of I-type BLDC Motor

A E-type PMSM (Fig. 6.3a) and a I-type BLDC motor [155] (Fig. 6.16a) were employed for validation and measurements of a stationary testing. The I-type motor for this part of research was a 3-phase 8-pole 12-slot BLDC, and developed in Ansys Maxwell. The 2D FEA model was built by using the measured parameters and validated conductor layout. There are 16 turns in 2 conductor layers, and simulated flux density distribution was depicted as in Fig. 6.16b.

In this proposed stationary testing, the ceramic bearings were replaced with 3D printed spacers. The 3D print material in this research was Polylactic Acid [156], with



(a) (b)

Figure 6.16: The I-type BLDC motor for FEA modeling and stationary testing. (a) I-type BLDC motor, and (b) 2D FEA model and flux density distribution result of the I-type motor with measured dimensions and detailed winding models.

which the replaced spacers could be considered as the ideal insulation between the motor shaft and ground. One of the benefits of this proposed stationary testing was that drive control system was not required and operating conditions such as speed and loading were not a limitation for bearing capacitance measurement. Detailed parameter measurement procedure and stationary testing setup will be discussed in the followings.

6.4.2 Parameter Measurement for the I-type and E-type Motors in the Stationary Testing

One of two identical I-type motors was disassembled (Fig. 6.19) for detailed dimension measurements and material analysis. The disassembled motor offered access

Table 6.2: Extracted capacitance comparison between E-type and I-type motors.

Capacitance	E-type FEA [pF]	I-type FEA [pF]
Winding - stator	316.3	7906.4
Stator - rotor	64.9	229.2
Winding - rotor	4.5	0.012

to validate the component dimension, number of turns, coil conductor diameter, and materials. The other motor was set up for experimental static measurement of bearing voltage.

Firstly, the front end cap was carefully removed to access the stator, rotor, shaft with key, and front end bearing (Fig. 6.19a). Secondly, rotor was removed from housing and stator and after that, the length of shaft, front end bearing dimensions (Fig. 6.19b), and stator dimensions (Fig. 6.19c) were accessible for the dimension measurement. The back end bearing (Fig. 6.19d) was disassembled from rotor after the hall sensor magnet ring removed. Furthermore, the back end cap was removed (Fig. 6.19e) to make windings, lamination, and teeth available for measuring as well as the hall sensor plate (Fig. 6.19f).

By far, windings became reachable from both back end and front side of the I-type BLDC motor, which allowed to un-wind coils and count number of turns. Fig. 6.19h showed one of the coils was un-winded for counting number of turns and measuring conductor dimension. Moreover, the shape of lamination (Fig. 6.19i) could be confirmed with insulation layer taken off. For an accurate measurement on the tooth dimensions, one piece of the laminations was removed. Detailed measurements on each component of the BLDC motor were illustrated (Fig. 6.21) and listed in Table 6.3. Phase resistance and phase inductance were measured by using a LCR

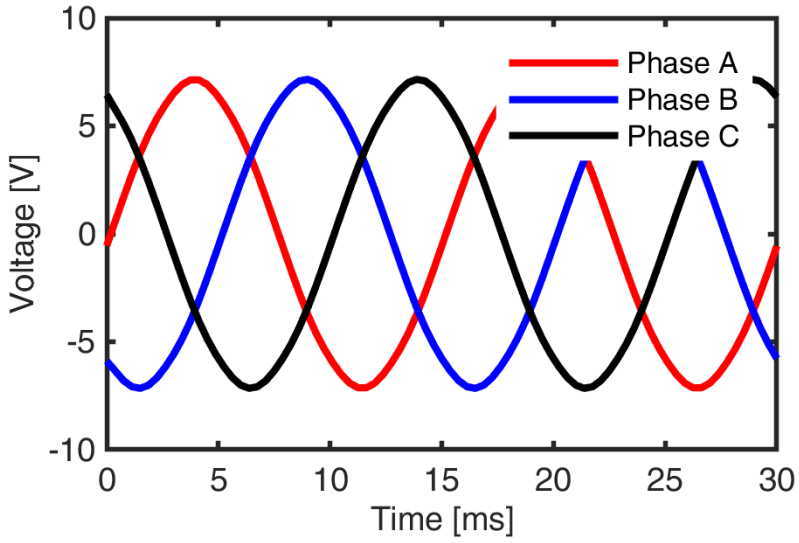


Figure 6.17: The simulated back EMF of the I-type motor modeled in Ansys Maxwell.

meter and the open circuit back EMF waveform was captured with a high-resolution Yokogawa oscilloscope.

The open circuit back EMF was also validated with a testing case operated at 1000 rpm (Fig. 6.18), and the developed 2D FEA model was used to validate back EMF under the same operating condition. The experimentally measured back EMF was 6.9 Vpk and simulated back EMF was 7.1 Vpk at 1000 RPM (Fig. 6.17), which showed a acceptable matching between FEA model and experimental measurement.

A E-type PMSM (Fig. 6.23a) motor was implemented and validated for the special stationary testing. First the integrated power electronics drives PCB was removed (Fig. 6.23b). Moreover, shaft was able to be removed, internal stator and winding profile (Fig. 6.23c) and external rotor (Fig. 6.23d) were accessible for measurement and setup. The original bearings (bearing types 608 and 688) were replaced with 3D printed spacers (same dimension, PLA+ material) as shown in Fig. 6.23e. Lastly,

Table 6.3: Parameters of the BLDC motors for the estimation and measurements of bearing current and bearing capacitance.

Number of phases	3
Number of poles p	8
Rated voltage	220Vac
Rated torque T	0.64 Nm
Peak torque T_{pk}	1.92 Nm
Rated speed ω_n	3,000 rpm
Rated current I_n	1.5 A
Peak current I_{pk}	4.5 A
Rated power P_{rated}	200 W
Phase inductance L_s	373.13 uH
Phase resistance r_s	0.27 Ω
Inertia of rotor J	0.21 kg.m^2
Torque constant	0.42 Nm/A
Voltage constant	38V/kRPM
Weight	0.6 Kg
Insulation class	Class B
Dielectric strength	1500VDC for 1 minute
Insulation resistance	100 $M\Omega$ Min., 1500VDC
Rotor outer diameter	30mm
Stator inner diameter	31.2mm
Stator outer diameter	57mm
Length of stack	42mm

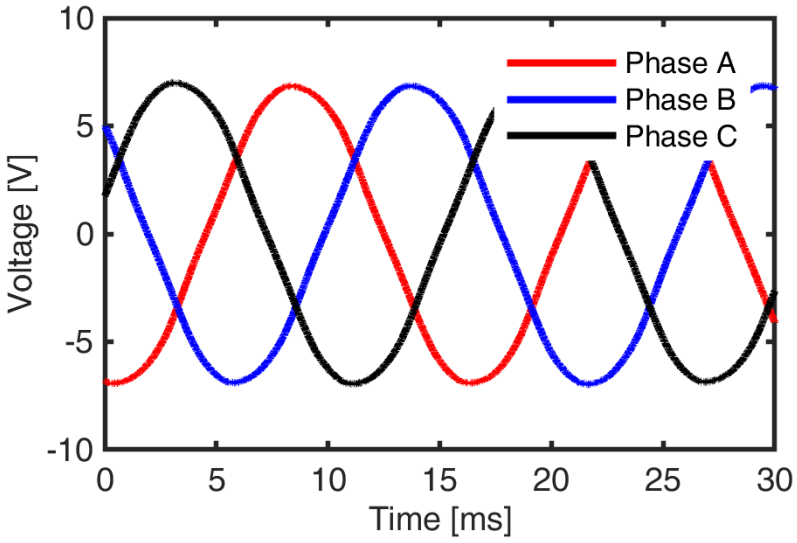


Figure 6.18: The measured back EMF result of the studied I-type motor.

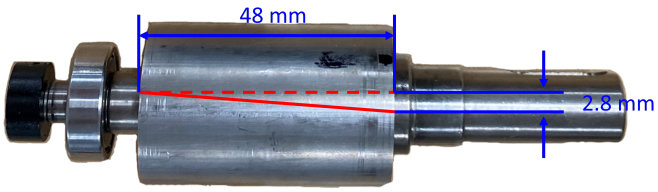
the E-type motor was re-assembled together with the 3D printed spacers (Fig. 6.23f) and set for stationary testing.

6.4.3 Testing and Validation

The bearing capacitance of a motor with ball bearings and the resulting bearing voltage vary at different speed and loading conditions. In other words, a direct bearing capacitance measurement requires a closed-loop motor drive control and measurements under the exactly same operating condition.

A static bearing voltage measurement approach was proposed in this work. Motor bearings were replaced with 3D printed plastic spacers (Fig. 6.22b), which could be considered as an ideal insulation between motor shaft and ground (extremely large resistance). By connecting capacitors in parallel between shaft and ground, the static bearing voltage measurement would be approaching to the simulated bearing voltage in the detailed FEA model. As a result, the bearing capacitance could be estimated

Figure 6.19: I-type BLDC motor de-assembly. (a) BLDC with front end cap removed, (b) stator and rotor, (c) windings, (d) rotor with bearings, (e) back end cap, (f) hall sensor plate, (g) back end bearing, (h) one coil un-winded, and (i) one lamination removed.



(a)

(b)

(c)

Figure 6.20: Rotor skew and material analysis, (a) rotor magnet skew angle measurement, (b) sleeve disassembled from rotor and shaft, and (c) side view of rotor magnet alignment.

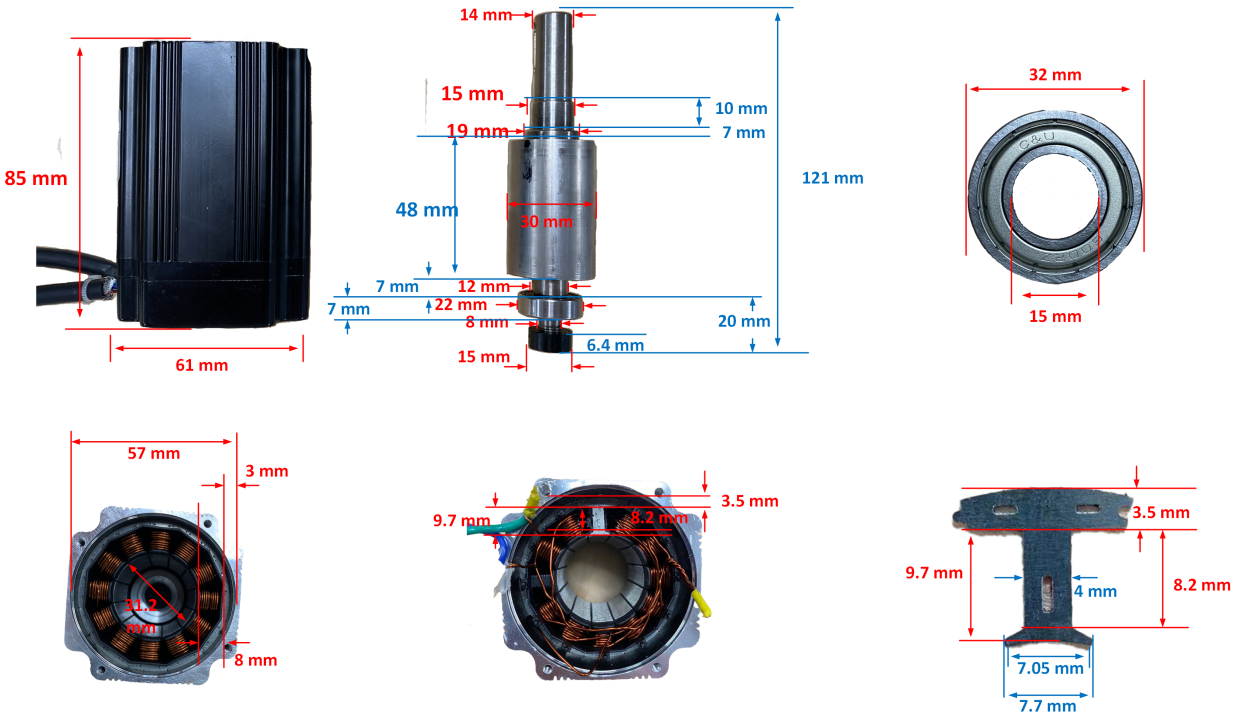
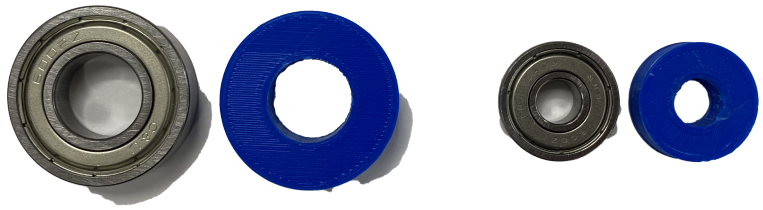
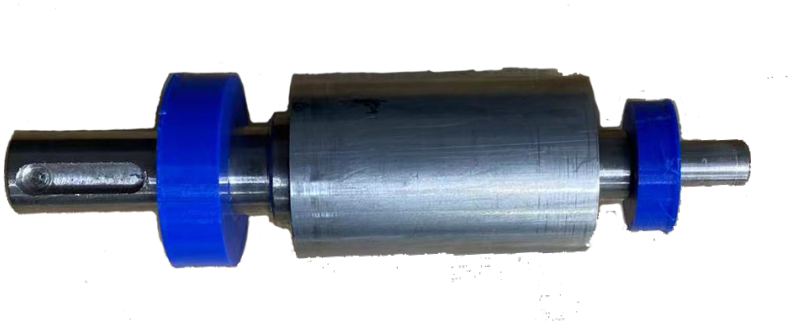


Figure 6.21: Dimension measurements on each component of the BLDC motor.

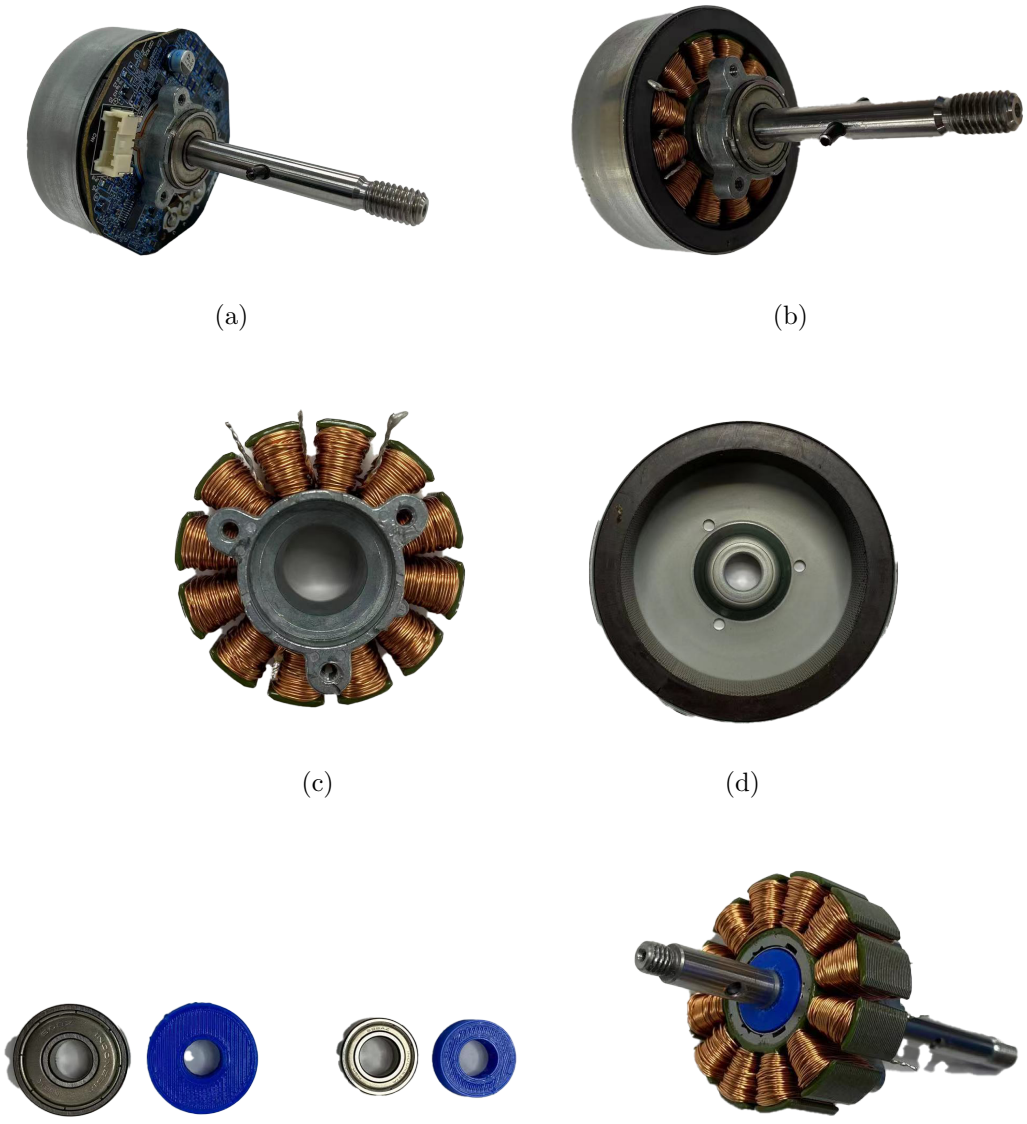


(a)



(b)

Figure 6.22: Rotor setup for the special stationary testing, (a) 3D printed spacers with the same dimensions to replace bearings, and (b) the 3D printed spacers installed on the rotor.



(a) (b)

(c) (d)

(e) (f)

Figure 6.23: E-type PMSM motor disassembly and setup for the special stationary testing. (a) E-type motor with integrated power electronic drives, (b) E-type motor with PCB drive removed, (c) stator winding profile, (d) external rotor profile, (e) bearings and 3D printed spacers (PLA+ material), and (f) E-type motor re-assembled with PLA+ spacers and set up for stationary testing.

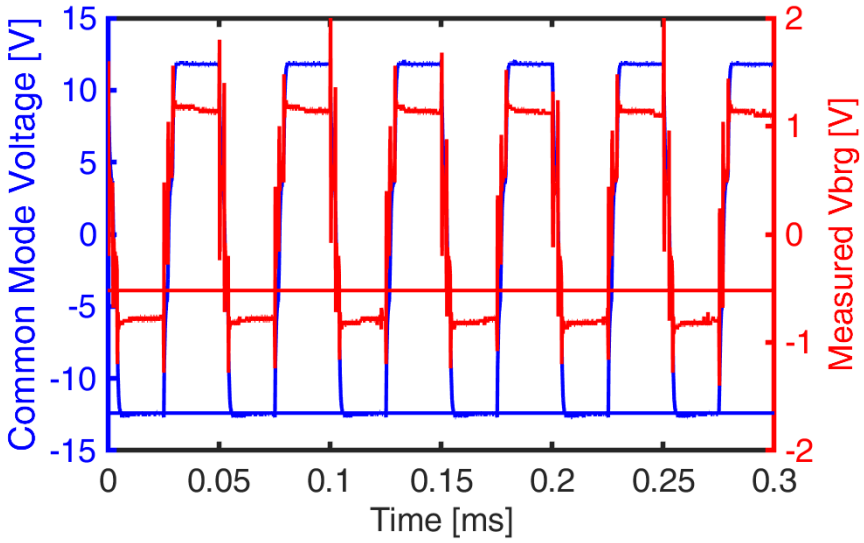
without setting up a drive control system or a rotating testing under a specific loading condition.

One of the two I-type BLDC motors was set for the stationary testing. The experimental result for the stationary bearing voltage measurement was presented in Fig. 6.25. A square waveform with 150kHz frequency and 12 Vpk, which was comparable to WBG high switching frequency range, was generated and applied on the I-type motor terminals. The induced bearing voltage between shaft and ground was 0.7 Vpk with the same frequency (150kHz).

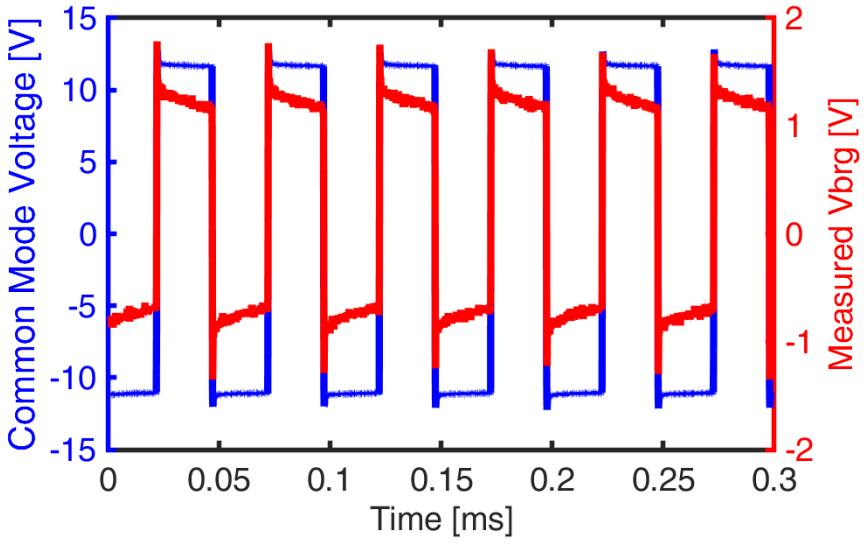
The E-type PMSM motor was also implemented to validate the proposed stationary testing (Fig. 6.24) and compared with bearing voltage measurement result from the rotating testing (Fig. 6.24a). A CMV waveform with 20 kHz switching frequency 12.5 Vpk was generated and applied on the E-type motor terminals. The induced bearing voltage between shaft and ground was measured, plotted, and analyzed as in Fig. 6.24b, in which measured bearing voltage is comparable between rotating testing and the proposed stationary testing with the same CMV.

6.5 Possible Solutions to Reduce Bearing Currents in WBG Drives

For the bearing current failure, improved bearing insulation [157], electromagnetic shielding slot wedge [158], well designed filters [159] [160], improved PWM modulations [161], and power electronics converter topology [162] offer potential solutions. In this section, a multi-carrier SPWM modulation and H-8 topology are studied.



(a)



(b)

Figure 6.24: The bearing voltage measurement forE-type motor. (a) Rotating testing measurement with a closed loop motor drive controller, and (b) stationary testing measurement without controller or loading shows a satisfactorily comparable V_{brg} result.

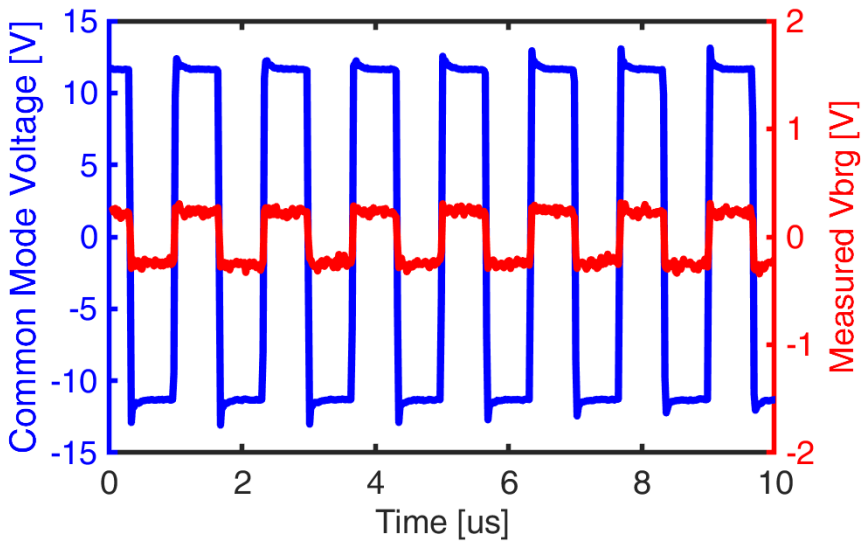


Figure 6.25: The bearing voltage measurement for the stationary I-type motor. PWM frequency is at 150kHz which is comparable to WBG high switching frequency range.

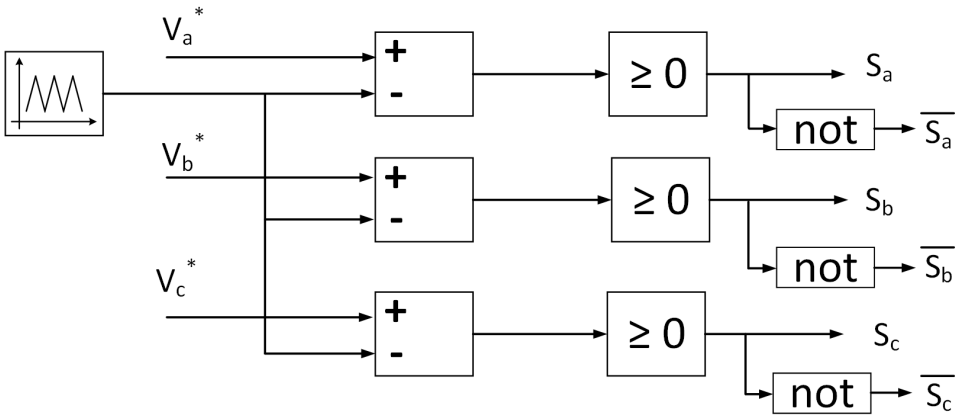
6.5.1 Multi-carrier SPWM Modulation Development

The CMV is determined by the summation of the phase voltages divided by the number of phases of the variable speed drive (VSD). Therefore, considering a three-phase two-level VSD, the CMV is determined as:

$$CMV = \frac{V_{aO} + V_{bO} + V_{cO}}{3}, \tag{6.6}$$

where V_{xO} is the phase voltage of phase x (x = a, b, c).

In conventional SPWM modulation, CMV(t) is highly dependent on the values of the displacement angles of the carriers ϕ_b and ϕ_c. To reduce CMV, four possible values of [ϕ_b, ϕ_c] can be defined as [0°, 0°], [0°, 180°], [180°, 0°], [180°, 180°]. The optimal displacement angle can be determined by mitigating the content of the first harmonic order content of the CMV at every sampling time. As a result, CMV can



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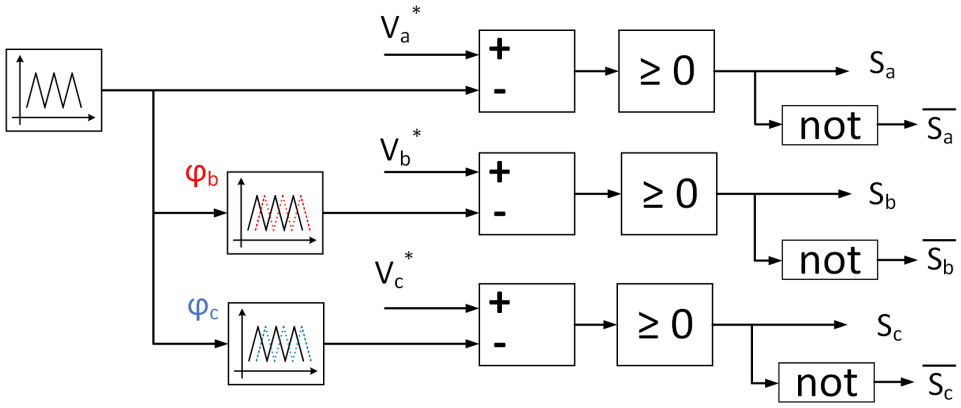

(b)

Figure 6.26: CMV mitigation technique using adaptive multi-carrier PWM: (a) conventional PWM modulation, (b) adaptive multi-carrier PWM technique.

be reduced by applying the adaptively shifted SPWM.

6.5.2 H-8 Converter Topology

Another possible solution to reduce CMV therefore bearing current is to add another two switches in the conventional 3-leg 6-switch topology (Fig. 6.27). To reduce the CMV or leakage current between source and ground, it is necessary to separate the power source (Fig. 6.28) during zero voltage stages. Based on the conventional operating scheme, such as SVPWM (Table 6.4, a SVPWM modulation

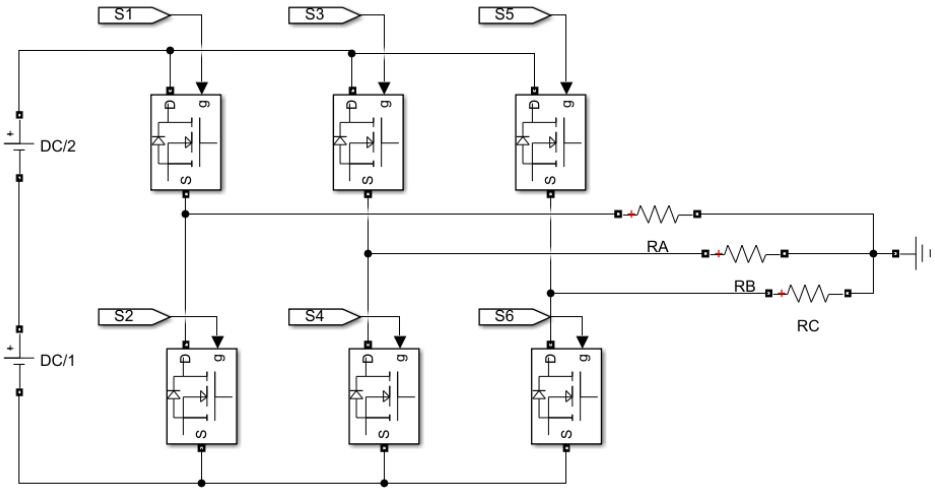

Figure 6.27: Conventional three phase H-6 converter topology.

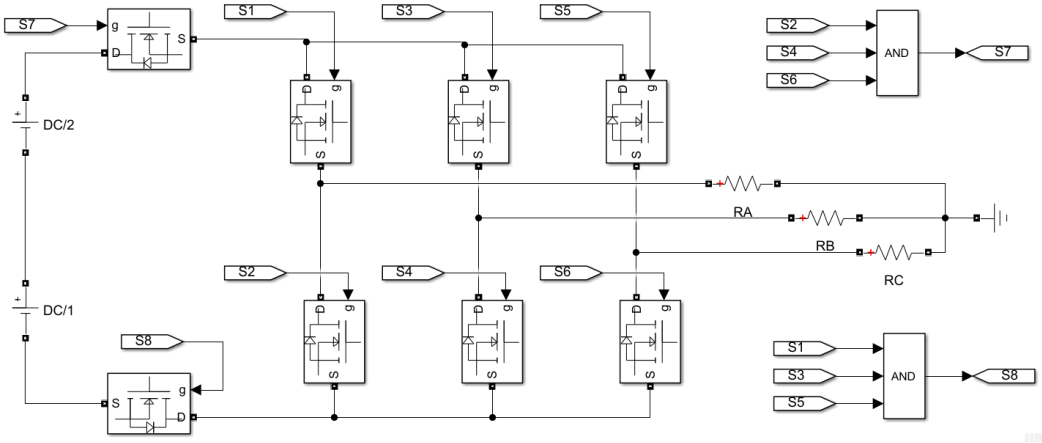

Figure 6.28: Conventional three phase H-8 converter topology.

designed for H-8 topology is developed (Table 6.5) in which the stages V7 and V8 are targeted at reducing CMV.

By implementing the potential solution, one simulation case shows the CMV comparison between conventional inverter and H-8 inverter with developed SVPWM (Fig. 6.29): the proposed solution reduced CMV from 200Vpk to 100Vpk.

Table 6.4: SVPWM operating scheme and switching and switching patterns for H-6 converter.

	S1	S2	S3	S4	S5	S6	V_{cm}
V1	On	On	Off	Off	Off	On	$2V_{dc}/6$
V2	On	On	On	Off	Off	Off	$4V_{dc}/6$
V3	Off	On	On	On	Off	Off	$2V_{dc}/6$
V4	Off	Off	On	On	On	Off	$4V_{dc}/6$
V5	Off	Off	Off	On	On	On	$2V_{dc}/6$
V6	On	Off	Off	Off	On	On	$4V_{dc}/6$
V7	On	Off	On	Off	On	Off	V_{dc}
V8	Off	On	Off	On	Off	On	0

Table 6.5: SVPWM operating scheme and switching and switching patterns for H-8 converter.

	S1	S2	S3	S4	S5	S6	V_{cm}
V1	On	On	Off	Off	Off	On	$2V_{dc}/6$
V2	On	On	On	Off	Off	Off	$4V_{dc}/6$
V3	Off	On	On	On	Off	Off	$2V_{dc}/6$
V4	Off	Off	On	On	On	Off	$4V_{dc}/6$
V5	Off	Off	Off	On	On	On	$2V_{dc}/6$
V6	On	Off	Off	Off	On	On	$4V_{dc}/6$
V7	On	Off	On	Off	Off	On	$3V_{dc}/6$
V8	Off	On	Off	On	On	Off	$3V_{dc}/6$

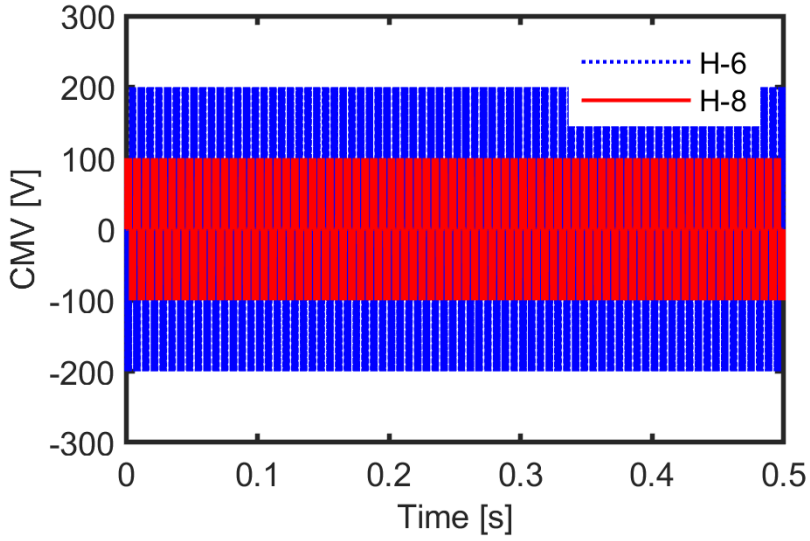

Figure 6.29: Common mode voltage improvements on WBG devices based drive systems. (a) CMV comparison between H-6 and H-8 topologies, and (b) zoomed-in CMV comparison between H-6 and H-8 topologies.

6.6 Conclusion

This chapter proposed to use electromagnetic FEA to model bearing voltage and current in electric machines to better consider the effect of distributed winding turns and frequency dependence of winding RL parameters. By examining the distributed-element equivalent circuit representation of electric machines, more specifically, the PMSM, all the three known bearing current types in machines driven by PWM converters were derived once the distributed capacitors were considered. The reduction of computation time was possible by grouping multiple real winding turns into one FE coil without reducing the accuracy. Additionally, two experimental validation approaches were proposed: time-domain analysis approach to accurately capture the time transient, stationary testing approach to measure bearing capacitance without complex control development or loading condition limitations. In addition, two types

of motors were employed for experimental validation: an inside out E-type PMSM was used for rotating testing and stationary testing, and a I-type BLDC was used for stationary testing. For the stationary testing, two identical motors of each type were used: one was disassembled for dimension measurement and parameter validation, and furthermore for modeling in Ansys Maxwell; the other motor was used for bearing voltage and bearing capacitance measurement experimentally. Possible solutions for the increased CMV and bearing currents caused by the implementation of WGB devices were discussed and developed in simulation validation, including multi-carrier SPWM modulation and H-8 converter topology.

Chapter 7

Conclusions

7.1 Summary and Conclusions

A cost-effective approach based on a hybrid utilization of SiC and Si devices was proposed to improve the efficiency of a five-level TCHB inverter in Chapter 2. Simulation results showed that the both peak efficiency CEC efficiency of the inverter was improved compared to all-Si TCHB inverter at the same conditions. Additionally, different modulations were developed including Single Reference Double Carrier and the Double Reference Single Carrier. Furthermore, compared to all-SiC-MOSFET TCHB inverter, the proposed hybrid TCHB inverter was able to ride through a load short-circuit fault due to the faster saturation characteristics of Si IGBTs constraining the short-circuit current in the inverter. Experimental results were presented to confirm the performance of the five-level TCHB inverter at various operating conditions.

Moreover, a non-isolated multi-port converter based EV charging station with PV and BES was proposed in Chapter 2. A BES controller was developed to regulate the voltage sag, and balance the power gap between PV generation and EV charging

demand, resulting in enhancing PV penetration and the stability and reliability of the power grid. Different operating modes and their benefits were developed and validated in simulation. The system efficiency was improved by 5.67%, 4.46%, and 6.00%, respectively, for PV-to-EV mode, PV-to-BES, and BES-to-EV mode at nominal operating condition, compared to Si based EV charging stations under the same operating conditions.

In Chapter 3, two inverter topologies for two-phase motor drives were investigated: a dual H-bridge supplied by two separate DC sources provides complete electrical isolation between phases and full survivability; and a 3-leg inverter offers a cost efficient solution for low power rating two-phase motor drives. The output capability was systematically compared and also experimentally validated. Current ripple was effectively reduced by implementing the two drives with WBG devices and operating the inverters at high switching frequencies. The 100kHz switching frequency enabled by SiC devices, compared to the 10kHz achievable by traditional silicon devices, largely reduced the current ripple and total harmonic distortion. Field oriented control was developed for the two-phase AFPM SMC motor drives. Comprehensive features were included in the closed-loop program such as initial angle alignment and dead-time compensation for the synchronization between rotor rotation and control algorithm. Experimental results of closed-loop drives validated the effectiveness of the control design: speed was constant and tracking speed reference; speed ripple was controlled within 5%; phase currents I_a and I_b were balanced and 90 degrees apart; d-axis and q-axis currents were constant and tracking current references.

In Chapter 4, an integrated AC/AC converter for single-phase input and two-phase

output motor drives was proposed, which reduced the switching device count to 6 and maintain the same functionality and output performance. Furthermore, a systematic comparative study of three converter topologies for single-phase to two-phase low-power motor drives, including topologies and associated modulation schemes, system cost, filter size, output voltage capability, speed operation range, and output distortion, was presented. The conventional AC/DC/AC topology was capable of producing the full output voltage capability with a low distortion (THD 1.7%); however, this topology required 12 active semiconductor switching devices and DC capacitors which therefore increased the system cost. The matrix converter did not have any DC link; however, it still required a large number of switching devices (8 bidirectional modules) and offered a reduced output voltage range (61.2%) with a very high THD of 22.1% under the same condition. In the proposed topology, the switch count was largely reduced to 6 and the output distortion also remained low (THD 3.7%). The modulation scheme and filter were carefully designed. In addition, a prototype for the integrated AC/AC converter was built and the experimental results validated the designs of PCB, converter topology, modulation, and filter.

Chapter 5 proposed to use electromagnetic FEA to model bearing voltage and current in electric machines to better consider the effect of distributed winding turns and frequency dependence of winding RL parameters. By examining the distributed-element equivalent circuit representation of electric machines, more specifically, the PMSM, all the three known bearing current types in machines driven by PWM converters were derived once the distributed capacitors were considered. The reduction of computation time was possible by grouping multiple real winding turns into one

FE coil without reducing the accuracy. Additionally, two experimental validation approaches were proposed: time-domain analysis approach to accurately capture the time transient, stationary testing approach to measure bearing capacitance without complex control development or loading condition limitations. In addition, two types of motors were employed for experimental validation: an inside out E-type PMSM was used for rotating testing and stationary testing, and a I-type BLDC was used for stationary testing. For the stationary testing, two identical motors of each type were used: one was disassembled for dimension measurement and parameter validation, and furthermore for modeling in Ansys Maxwell; the other motor was used for bearing voltage and bearing capacitance measurement experimentally. Possible solutions for the increased CMV and bearing currents caused by the implementation of WGB devices were discussed and developed in simulation validation, including multi-carrier SPWM modulation and H-8 converter topology.

7.2 Original Contributions

The main original contributions of this dissertation may be best summarized as follows:

1. A hybrid "SiC MOSFETs + Si IGBT" transistor-clamped H bridge (TCHB) five-level converter was proposed. Various modulation schemes including double-reference single-carrier and single-reference double-carrier PWM strategies for the proposed five-level converter were developed. Power losses including conduction loss and switching loss are mathematically evaluated, modeled, and simulated, and efficiency was improved compared with conventional Si based five level TCHB converters.

Furthermore, fault tolerance of this proposed converter was validated to be improved. (Chapter 2)

2. A non-isolated multi-port converter based on SiC MOSFETs was proposed for EV charging system, taken power density, system cost, compactness, and power losses into consideration. A systematic comparison based on modeling and simulation was conducted to validate the efficiency improvement by this proposed multi-port converter. Different operating mode including PV charging EVs, PV charging battery energy storage (BES) were discussed and designed, and detailed control scheme was developed and validated in simulation. (Chapter 3)

3. Two converter topologies were developed for low inductance two-phase machines: dual-H bridge to provide full operating range and output capability, and three-leg converter to reduce system cost and size, respectively. A systematic comparison on topology, modulation, operating range, and power capability was conducted. A field oriented control (FOC) was developed for two phase axial PM machine drive. The control scheme was modeled and validated in both simulation and experimentation. A re-configurable SiC MOSFET based inverter prototype was prototyped and tested to drive the two-phase AFPM motor. (Chapter 4)

4. An integrated AC/AC converter for two phase motor drive was developed to further reduce the switch count and as a result system cost. Other common used converter topology was also developed for two-phase motor drives including conventional back-to-back converters and matrix converters. A throughout analysis of conventional back-to-back converter, matrix converter, and proposed AC/AC converter was

completed to compare the switch number, system cost, filter, control, output capability and operating range. A PCB design was conducted for the two-phase integrated AC/AC converter. SiC MOSFET gate driver circuit, bypass capacitor sizing, driver protection circuit, dv/dt prevention, and turn-off circuit was carefully designed and included in the PCB design. Simulation and experimental results provided the validation on the effectiveness of both converter and control scheme. (Chapter 5)

5. Two types of combined numerical analysis and test procedures were proposed and validated: a time-domain FEA approach to fully capture the time transient variations, and a special stationary testing to measure bearing voltage and capacitance without complex control development or loading condition limitations. Possible reduction of computation time in this proposed approach was investigated. In addition, two types of motors were employed for experimental validation: an inside out E-type PMSM was used for rotating testing and stationary testing, and a I-type BLDC was used for stationary testing. Possible solutions for the increased CMV and bearing currents caused by the implementation of WGB devices were discussed and developed in simulation validation, including multi-carrier SPWM modulation and H-8 converter topology. Possible solutions for the increased CMV and bearing currents caused by the implementation of WGB devices were discussed and developed in simulation validation, including multi-carrier SPWM modulation and H-8 converter topology. (Chapter 6)

7.3 Recommendations for Future Work

Based on the study of this dissertation and earlier research conducted by others, possible further research may include the following:

1. Further studies on 2-phase AFPM SMC motor drives control and testing may be conducted. Measured results have been focused on steady state performance evaluation, and experimentation already in progress will analyze the transient state of motor drives. Furthermore, expansion will include 3-leg topology motor drives, related control development, and experimental measurements.

2. Further development on the proposed integrated AC/AC converter may be performed including thermal analysis, heat sink sizing, and cooling system development. With the updated thermal development included, the dynamic characteristic evaluation of the integrated AC/AC converter and continuous testing with RL load may be conducted and reported on.

3. For bearing current research, a third analysis and testing approach, which may work for any type of bearings, will be conducted. A systematic FE analysis will be conducted on the influence of demagnetized rotor magnets on bearing voltage and other performance first. If with the demagnetized rotor, capacitance or bearing voltage are comparable, then the rotor magnets will be experimentally demagnetized and CMV applied on motor terminals while motor rotating for measuring bearing voltage. A motor drive system for the I-type BLDC motor may be developed and prototyped. The measured CMV and bearing voltage results of the I-type BLDC motor may be obtained and analyzed for bearing capacitance estimation. In addition,

the possible solutions to reduce CMV may be further developed and implemented in the I-type and E-type motor drives. As a result, the effectiveness of the possible solutions may be validated for the I-type and E-type motors in both simulation and experimentation.

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