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Reliability Improvement of Voltage Regulator Modules by a Virtual Series Voltage Source

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Abstract—**Output voltage deviation is a key performance index of voltage regulator modules (VRMs) with consecutive load transients. Usually, a large-capacity filter capacitor bank is used in VRMs to reduce the voltage deviation and stabilize the output voltage during transients. However, capacitors are one of the most vulnerable links in power electronic converters. For reliability reasons, it is essential to reduce the capacitance requirement while guaranteeing the transient performances of VRMs. Focusing on this, many efforts have been made to optimize the design of VRMs, where the transient auxiliary circuit-based scheme is a popular one. Unfortunately, there exists a large number of additional components in the existing auxiliary circuits. Considering this issue, this paper presents a virtual series voltage source (VSVS) based auxiliary circuit scheme, which has minimum component counts. By using a controlled coupled inductor as the VSVS, the proposed scheme enables VRMs to have a relatively small transient voltage overshoot and without needing large bulk capacitance. Moreover, considering different control schemes with the same designing aim, the number and the electro-thermal stress of critical components (e.g., capacitors) of VRMs are different, it is difficult to compare directly their advantages and disadvantages. Regarding this issue, this paper investigates the converter-level reliability of VRMs with different control schemes. Taking a 12−3.3-V VRM as a case study, the reliability benchmarking results illustrate that the proposed scheme can significantly improve the reliability of VRMs.**

***Index Terms*—Voltage regulator module (VRM), auxiliary circuit, reliability benchmarking, transient performance.**

I. Introduction

VOLTAGE regulator modules (VRMs) are being widely used to power modern electronic devices with continuously load transient events, such as central processing units (CPUs), digital signal processors (DSPs), microprocessors, and network-application integrated circuits [1], [2]. In order to store energy and stabilize the output voltage during load transients, a large-capacity filter capacitor bank is commonly used at the output side of VRMs [3]. Unfortunately, capacitors are one of the most vulnerable links in power electronic converters [4]−[6]. For reliability reasons, it is essential to reduce the capacitance requirement while guaranteeing the steady-state and transient performances of VRMs.

TABLE I
ADDITIONAL COMPONENTS IN UNLOADING AUXILIARY CIRCUITS

Types	Auxiliary circuits	Addition components
I	gyrator circuit [2]	S×5, L×1, C×2
	output-side buck-boost circuit [9]	S×2, L×1, C×1
II	small auxiliary phase [10]	S×2, L×1
	buck-boost circuit [7],[11]	S×1, L×1, D×1
	resonant circuit [12]	S×2, L×2, C×1
III	parallel-inductor circuit [13]	S×4, L×1, R×1
	parallel-coupled-inductor circuit [14]	S×3, D×1, R×1
	series-coupled-inductor circuit [15]	S×2
Proposed	virtual series voltage source	S×1

Note: S-switch, L-inductor, D-diode, C-capacitor, R-resistor.

Voltage deviation including the voltage overshoot and undershoot is a key performance index of VRMs, where voltage overshoot has been widely concerned in popular low-duty-cycle conversion applications (e.g., 12 V_{dc}→3.3 V_{dc}) [7]. From the perspective of control strategy, a traditional linear control, such as proportional-integral (PI) control, could achieve the system's steady-state performance well. However, a large-capacity filter capacitor bank is required to reduce the voltage overshoot due to its inferior transient performance [7]. Although the advanced nonlinear control, e.g., time-optimal control (TOC), could push the transient performance of a converter near to its physical limit, undesired large voltage overshoots during unloading transients still dominate the capacitance requirement [8].

On the basis of the TOC scheme, some auxiliary circuits consisting of auxiliary switches, auxiliary inductors, etc., have been presented to further reduce the capacitance requirement while suppressing the transient voltage overshoot of VRMs [2], [9]−[15]. In terms of connection style, they can be divided into three types, i.e., the shunt-output style (Type I), bridge-connection style (Type II), and inductance-switching style (Type III), as summarized in Table I. These schemes could efficiently reduce the transient voltage overshoot of VRMs, thereby reducing the capacitance requirement. However, the number of additional auxiliary components is relatively high. Considering this issue, this paper proposes a virtual series voltage source (VSVS) based auxiliary circuit scheme, which has minimum component counts, as shown in Table I.

On the other hand, although the proposed VSVS scheme can reduce the capacitance requirement, it may bring new reliability risks due to the use of an additional power switch. It is essential to conduct the reliability performance benchmarking of the proposed VSVS scheme (using additional power switches and a small volume of capacitance) with traditional schemes (using a large volume of capacitance). Recently, many efforts have been

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made to investigate the reliability of power electronic converters, and the mission profile-based method is the state-of-the-art one [16]. Considering actual mission profiles of converters, the lifetime of capacitors in adjustable speed drives, wind power converters, and metro traction drives are investigated in [17]–[19], respectively. Similarly, the reliability of power semiconductor switches in some converters has been evaluated by using the same mission profile-based methods [20]–[22]. Furthermore, based on the reliability analysis of discrete components or modules, the converter- or system-level reliability can be investigated using a reliability block diagram [23]–[25].

The above-mentioned reliability analysis methods provide a reference for lifetime evaluation and reliability-oriented design of power converters. However, it is not suitable to apply these methods in VRMs with frequent loading transients (the loading step frequency is usually larger than 1 kHz [26]). Because of the sampling frequency of mission profiles in traditional schemes is usually smaller than 1 Hz (the sampling rate is 1 hour in [17]), which easily results in missing important transient information. Although Zhao *et al*. investigated the reliability of capacitors in VRMs [27], in which transient stresses have been considered. However, there is a lack of research efforts focusing on the converter-level reliability evaluation of VRMs with frequent loading transients.

To overcome the above-mentioned limitations, this paper proposes a VSVS based auxiliary circuit scheme and conducts the reliability performance benchmarking with traditional TOC and PI schemes. The main contributions are given as follows.

1) A VSVS based auxiliary circuit scheme is proposed to improve the reliability while guaranteeing the performance of VRMs. Comparing with the existing auxiliary circuit-based schemes, the proposed scheme has minimum component counts.
2) Investigate the converter-level reliability of the proposed VSVS scheme and conduct its performance benchmarking with traditional PI and TOC schemes. Here, the effect of transient stress on capacitors is considered, in order to improve the evaluation accuracy.

The rest of this paper is organized as follows. Section II presents the VSVS scheme and a case study for reliability benchmarking is introduced. Section III describes the electro-thermal model, lifetime and cumulative damage models. Section IV presents the matchmaking results. Finally, the conclusion is drawn in Section V.

II. Proposed VSVS Scheme and the Description of a Case Study

A. Proposed VSVS Scheme

1) Circuit Topology

Fig. 1(a) shows the topology of the proposed VSVS scheme. A coupled inductor L_1 is used as the output inductor, and another coupled inductor L_2 is connected with the input source v_i by an auxiliary MOSFET S_{aux}. The coupling coefficient σ is calculated as $\sigma = M/\sqrt{L_1 L_2}$, where M represent the mutual inductance. During steady state and loading transients, the auxiliary switch S_{aux} is disabled, then the converter works with a large inductance L_1, and a classical TOC control method is used [11]. The

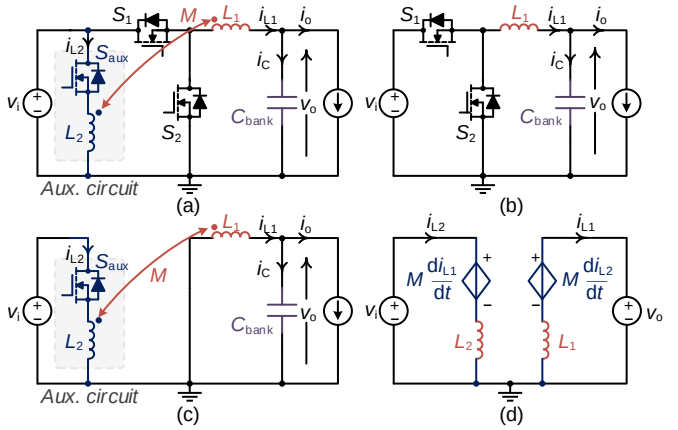


Fig. 1. Topology of the proposed VSVS scheme. (a) Proposed circuit topology. (b) Equivalent circuit during steady-state and loading transient. (c) Equivalent circuit during unloading transient. (d) Equivalent circuit of controlled source during unloading transient.

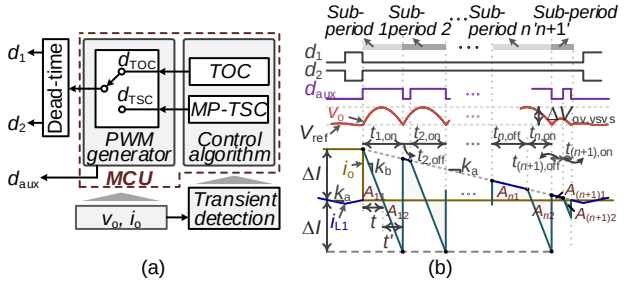


Fig. 2. Block diagram and unloading transient waveforms of the proposed scheme. (a) Block diagram. (b) Unloading transient waveforms.

equivalent circuit is shown in Fig. 1(b).

During unloading transients, S_1 turns OFF and S_2 turns ON. The auxiliary circuit is enabled, as shown in Fig. 1(c). When S_{aux} turns ON, the coupled inductor works as a virtual series voltage source. The equivalent circuit of the converter is shown in Fig. 1(d). Based on Kirchhoff's circuit law, the slew rate of inductor current i_{L1} is

$$k_b = \left|di_{L1}/dt\right| = \left(v_o + Mv_i/L_2\right)\Big/\left(L_1 - M^2/L_2\right) \quad (1)$$

where v_o is the output voltage. Assuming the slew rate of the inductor current is k_a when S_{aux} is disabled (i.e., classical TOC scheme), we have

$$k_a = v_o/L_1 . \quad (2)$$

From (1) and (2), it is easily found that $k_b >> k_a$, which means that the inductor current decreases much faster when S_{aux} turns ON.

2) Control Strategy

Fig. 2(a) shows the block diagram of the proposed VSVS scheme, where d_1, d_2, d_{aux} represent the driving signals of S_1, S_2, and S_{aux}. The control algorithms including the TOC strategy and a multi-period frame transient switching control (MP-TSC) strategy are implemented in a microcontroller unit (MCU). The TOC strategy is used for steady state and loading transients [11], the MP-TSC strategy is designed for unloading transients [15]. Notice that the transient detection circuit is implemented by an *RC* differential circuit and a comparator, as discussed in [15].

The transient event of the MP-TSC scheme for a negative load step (the step amplitude is ΔI) is shown in Fig. 2(b), where v_o, i_{L1}, i_o are the output voltage, inductor current, and load current, respectively. Using the capacitor-charge balance principle, the

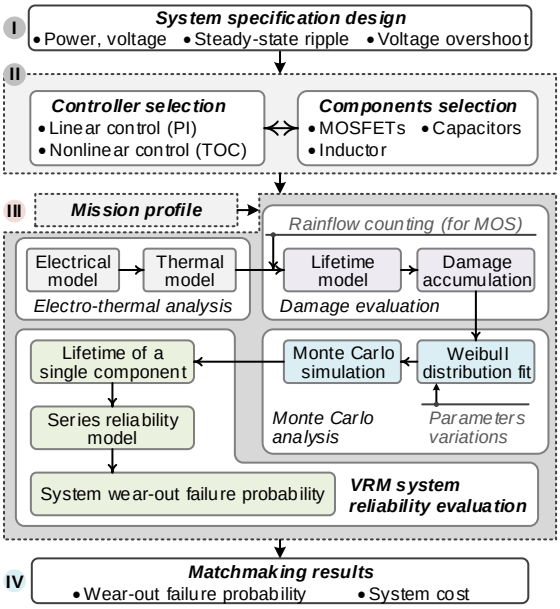


Fig. 3. Reliability benchmarking procedure.

unloading transient event is divided into n+1 sub-periods. In each sub-period, the charge area equals the discharge area, i.e.,

$$\begin{cases} A_{11} = A_{12} = A_{n1} = A_{n2} \\ A_{(n+1)1} = A_{(n+1)2} \end{cases}, n \geq 2 \tag{3}$$

where A_{11}– $A_{(n+1)1}$, A_{12}– $A_{(n+1)2}$ represent the charge area and discharge area in each sub-period, respectively. The MP-TSC strategy enables the former n sub-periods to have the same output voltage overshoot $\Delta V_{ov,vsvs}$, and the last one to have a smaller overshoot [15]. The system voltage overshoot is defined as $\Delta V_{ov,vsvs}$.

Taking Sub-period 1 as an example, it is easily found that i_{L1} decreases rapidly and much faster than that for the classical TOC scheme due to $k_b >> k_a$, which results in the system having a smaller voltage overshoot $\Delta V_{ov,vsvs}$. In order to satisfy the capacitor charge balance (CCB) principle, the time period t should equal t', i.e., $t = t' = \Delta I/k_b$. Furthermore, $\Delta V_{ov,vsvs}$ can be calculated using A_{11} and C_{bank}, i.e.,

$$\Delta V_{ov,vsvs} = A_{11}/C_{bank} = \Delta I \cdot t/(2C_{bank}) = \Delta I^2/(2k_b C_{bank}) \tag{4}$$

where C_{bank} represents the output capacitance [14].

Referring to Fig. 2(b), the turn-ON duration of Sub-period 1 is calculated as $t_{1,on} = 2t = 2\Delta I/k_b$. Furthermore, using the CCB principle, the turn-ON duration $t_{n,on}$ and turn-OFF duration $t_{n,off}$ of n-th sub-period are derived as

$$\begin{cases} t_{n,on} = 2\Delta I/k_b - x'_n \\ t_{n,off} = x_n + x'_n \end{cases}, n \geq 2 \tag{5}$$

where x_n and x'_n represent the intermediate, which are detailed discussed in [15]. Similarly, the turn-ON duration $t_{(n+1),on}$ and the turn-OFF duration $t_{(n+1),off}$ of (n+1)-th sub-period can be derived in the same way.

Notice that a hybrid capacitor bank consisting of polymer aluminum electrolytic capacitors (Al-Caps) and multi-layer ceramic capacitors (MLC-Caps) is usually used at the output side of VRMs, in order to reduce the total equivalent series resistance (ESR) and equivalent series inductance (ESL).

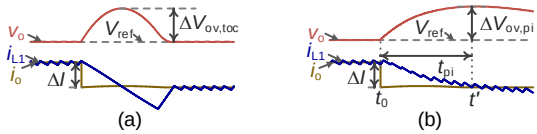


Fig. 4. Unloading transient waveforms of the TOC and PI schemes (a) TOC scheme. (b) PI scheme.

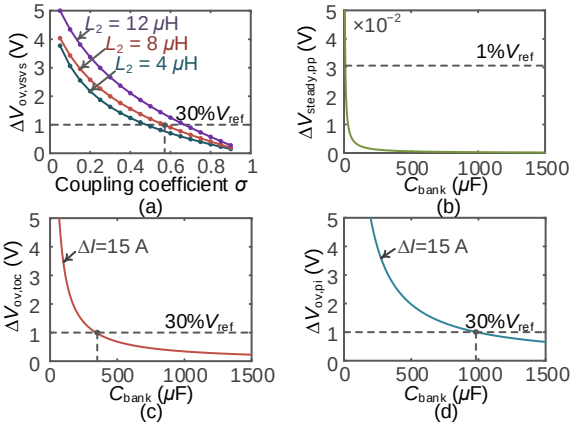


Fig. 5. The relationship between voltage overshoot, steady-state ripple, and circuit parameters. (a) $\Delta V_{ov,vsvs}$ versus σ in the VSVS scheme. (b) $\Delta V_{steady,pp}$ versus C_{bank} in the VSVS, TOC and PI schemes. (c) $\Delta V_{ov,toc}$ versus C_{bank} in the TOC scheme. (d) $\Delta V_{ov,pi}$ versus C_{bank} in the PI scheme.

Therefore, the ESR and ESL are not considered in (4).

B. Case Study for the Reliability Benchmarking

In order to evaluate the reliability of the proposed VSVS scheme, a classical VRM with a linear control scheme (i.e., PI scheme) and a nonlinear control scheme (i.e., TOC scheme) are chosen as benchmarks. Fig. 3 shows the reliability benchmarking procedure, where Steps I and II are introduced in this part. Steps III and IV are given in the next section.

1) *Classical VRMs with TOC and PI Schemes*

Fig. 4(a) and Fig. 4(b) show the transient waveforms of VRMs with the classical TOC and PI schemes. Here a traditional synchronous buck converter without auxiliary circuits is considered, the inductance is the same as that in Fig. 1, i.e., L_1.

According to the derivation in [8], the voltage overshoot $\Delta V_{ov,toc}$ of a TOC-controlled VRM is calculated as

$$\Delta V_{ov,toc} = \Delta I^2/(2k_a C_{bank}) \tag{6}$$

where, k_a is the slew rate of the inductor current, as derived in (2). Because the duty cycle d of the PI scheme usually cannot reach 0 or 1 during transients, its transient period is relatively long, as shown in Fig. 4(b). Assuming an unloading transient occurs at t_0, and the inductor current reaches the new load current at t'. To simplify the analysis process, the transient period is defined as $t_{pi} = t' - t_0$. Assuming the mean value of d is d_{mean} during t_{pi}, it is approximated as

$$t_{pi} = \Delta I L_1/\left[v_o(1-d_{mean}) - (v_i - v_o)d_{mean}\right] \tag{7}$$

Then, the voltage overshoot $\Delta V_{ov,pi}$ is approximated as

$$\Delta V_{ov,pi} = \Delta I t_{pi}/(2C_{bank}) \tag{8}$$

The peak-to-peak value $\Delta V_{steady,pp}$ of capacitor voltage ripple (i.e., the output voltage ripple) is calculated as

$$\Delta V_{steady,pp} = (v_i - v_o)v_o/(8v_i L_1 f_s^2 C_{bank}) \tag{9}$$

where f_s is the switching frequency.

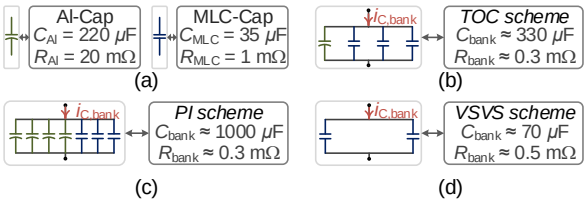


Fig. 6. Capacitor configuration for different schemes. (a) Parameters of a single Al-Cap and a single MLC-Cap. (b) Capacitor bank of the TOC scheme. (c) Capacitor bank of the PI scheme. (d) Capacitor bank of the VSVS scheme.

TABLE II
SPECIFICATIONS AND PARAMETERS OF CAPACITORS

Parameter	Polymer Al-Cap [28]: WCAP-PSLP875105144008	MLC-Cap [29]: GRM31CR60J107MEA8
Dimension	43.6×5.8 mm	5.1×0.6 mm
Capacity	220 μF/6.3 V	100μF/6.3 V, 35μF/3.3 V
ESR	20 mΩ @ 100 kHz, 20 °C	1 mΩ @ 100 kHz, 25 °C
Lifetime	2000 h @ +105 °C, 6.3 V	1000 h @ +85 °C, 12.6 V
R_{ha} [27]	133.1 °C/W	22.9 °C/W
τ_{ha} [27]	83.9 s	0.14 s

2) *Circuit Parameters Design*

A 12−3.3-V VRM is chosen as a case study, the main circuit parameters are v_i = 12 V, v_o = 3.3 V, f = 100 kHz, steady-state inductance L_1 = 10 μH. Assuming a 70-μF capacitor bank is selected in the proposed VSVS scheme. Using (5), Fig. 5(a) shows the relationship between $\Delta V_{ov,vsvs}$ and σ. Here, three different coupled inductances are chosen as exam0825ples, i.e., L_2 equals to 4 μH, 8 μH, and 12 μH, respectively. For a 15 A unloading transient, our design aims are $\Delta V_{steady,pp} \leq 1\% V_{ref}$ and $\Delta V_{ov,vsvs} \leq 30\% V_{ref}$. According to the calculation results in Fig. 5(a), L_2, M can be designed as 4 μH and 3 μH, respectively. Moreover, the steady-state ripple also meets the design aim in this case, as shown in Fig. 5(b).

For comparison, a TOC scheme and a PI scheme with the same steady-state and transient performance indexes are designed. Using (6) and (8), Figs. 5(c) and 5(d) show the relationship between capacitance and the voltage overshoot ΔV_{ov} for TOC -and PI-controlled VRMs. Here, the mean duty cycle of PI-controlled VRM during unloading transients is assumed as 0.2. According to the calculated results in Fig. 5, C_{bank} for the TOC and PI schemes can be designed as 330 μF and 1000 μF, respectively. The design results illustrate that the proposed VSVS scheme can enable the converter to have the same voltage overshoot when using a small capacitance, which can reduce the capacitance requirement.

3) *Simulation and Experimental Verifications*

In order to verify the effectiveness of the proposed VSVS scheme, a converter is carried out in the power electronics simulator (PSIM) simulation environment. With the same design aim, Fig. 6 shows the capacitor configurations of the proposed VSVS scheme, TOC scheme, and PI scheme. Here, two types of different capacitors are considered. The detailed capacitor parameters are listed in Table II. Notice that polymer Al-Caps are used in priority to reduce the number of employed capacitors. In Fig. (6), C_{Al}, R_{Al} represent the capacitance and ESR of a single Al-Cap. C_{MLC}, R_{MLC} denote the capacitance and ESR of a single MLC-Cap. R_{bank} is the total ESR of a capacitor bank. $i_{C,bank}$ represents the current of capacitor banks. In the simulation, the parasitic parameters of inductors and MOSFETs are also

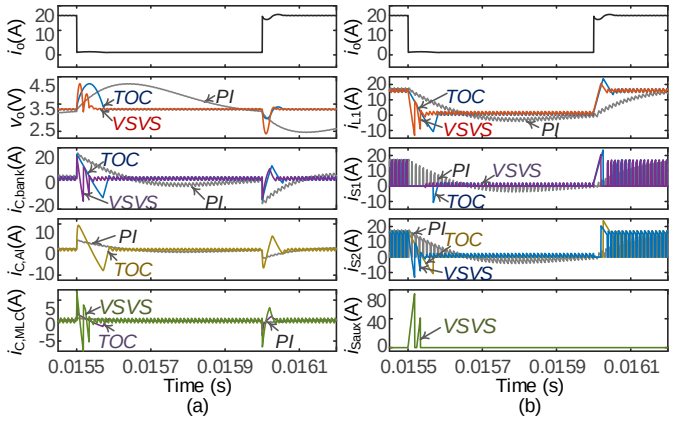


Fig. 7. Simulated response for VRMs with a 15-A repetitive load transient. (a) Output voltage and capacitor current. (b) Current of MOSFETs and L_1.

considered. Referring to the datasheet of AUIRF1324 [30], the on-state resistance R_{ds} of MOSFETs is 1.5 mΩ. The parasitic resistance of L_1 (i.e., steady-state inductance) and L_2 are about 13.2 mΩ and 5.3 mΩ, respectively.

Fig. 7 shows VRMs' transient response to a repetitive load transient of 15 A, where $i_{C,bank}$, $i_{C,Al}$ and $i_{C,MLC}$ represent the current of capacitor banks, a single Al-Cap and a single MLC-Cap, respectively. i_{L1}, i_{S1}, i_{S2}, i_{Saux} denote the current of L_1, S_1, S_2, and S_{aux}, respectively. Referring to (5) and the detailed design guideline of MP-TSC strategy in [15], the number of switching times of S_{aux} in the VSVS scheme is 2 during unloading transient. The turn-ON duration of Sub-period 1 is 18 μs, the turn-OFF and turn-ON duration of Sub-period 2 are 5.6 μs and 10 μs, respectively. In the PI-controlled VRM, the proportion and integral coefficients are 0.3 and 0.008, respectively. Moreover, the control timing of TOC-controlled VRM are derived from [7].

Referring to Fig. 7, it can be seen that the voltage deviation of these three schemes are less than 30% of the reference voltage, which satisfies the expected designing aim. Compared with the TOC and PI schemes, the proposed VSVS scheme has the shortest settling time during unloading transient. Moreover, Fig. 7 illustrates that the electrical stress of capacitors and MOSFETs in different schemes are different. According to the simulation results, Fig. 8(a) shows the root mean square (rms) current of key components during one time of unloading transient [15]. It can be seen that the rms current of S_2 in the VSVS scheme is smaller than that in the TOC and PI schemes. And, the rms current of S_1 equals to 0 due to it is turned OFF during unloading transient. However, the electrical stress of S_{aux} and MLC-Caps in the proposed scheme is relatively large.

Furthermore, Fig. 8(b) shows the energy loss of key components during one time of unloading transient [15]. It is found that the total energy loss of VSVS-based VRM is larger than that of the TOC-based VRM. Its energy loss is dominated by the loss of auxiliary circuits, i.e., S_{aux} and L_2. Moreover, the most influential factor to the energy loss during unloading transient is the conduction loss of inductors. If the loss of inductors is not considered, the total energy loss of MOSFETs and capacitors in the proposed VSVS scheme is similar to that in the TOC scheme, and it is far smaller than that in the PI scheme.

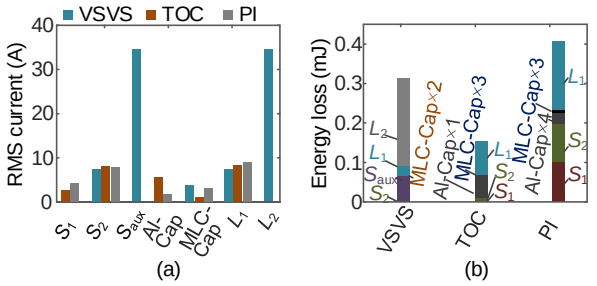


Fig. 8. Simulated rms current and energy loss of key components during one time of unloading transient. (a) RMS current of single components. (b) Energy loss.

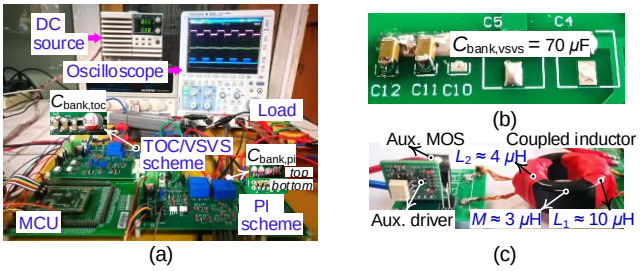


Fig. 9. Built experimental platform. (a) Experimental platform. (b) Photo of the used capacitor bank in the VSVS scheme. (b) Photo of the proposed auxiliary circuit in the VSVS scheme

In order to further evaluate the proposed scheme, VRMs with the VSVS scheme as well as the traditional TOC and PI schemes are carried out in experiments, as shown in Fig. 9(a). Here, a microcontroller unit (MCU) TMS320F28377D is used to implement the digital control. The parameters of circuits and controllers are the same as those in simulation. The photos of the capacitor bank and auxiliary circuits of the proposed VSVS scheme are shown in Fig. 9(b) and Fig. 9(c), respectively. Using the MP-TSC strategy, the experimental result of the VSVS scheme is shown in Fig. 10(a). It can be seen that the voltage overshoot satisfies the expected designing aim, i.e., $\Delta V_{ov,vsvs}$ <30%V_{ref}. For comparison, Fig. 10(b) and Fig. 10(c) show the experimental waveforms of the conventional TOC and PI schemes. The experimental results illustrate that the proposed scheme can significantly reduce the capacitance requirement when compared with the TOC and PI schemes, in order to achieve the same voltage overshoot.

Fig. 10(d) shows the measured efficiency curves of the VSVS, TOC, and PI schemes, where the load transient repeating frequency f_{tr} is varied from 0.25 kHz to 1.5 kHz with a 50% load duty ratio. The results demonstrate that the efficiency of the proposed scheme is larger than that for the PI scheme, however, it is smaller than that for the TOC scheme. Usually, the efficiency of VRMs decreases as f_{tr} increases. And, the efficiency of the VSVS scheme is closer to that of the TOC scheme when the load transient frequency is lower. However, it is lower when f_{tr} is higher, which is similar to that in the existing auxiliary circuit-based schemes [9], [12].

The simulation and experimental results illustrate that the number and electrical stress of critical components (i.e., capacitors and MOSFETs) in different schemes are different. In order to conduct the reliability performance benchmarking of the proposed VSVS scheme with traditional schemes, a mission-profile-based reliability evaluation method is

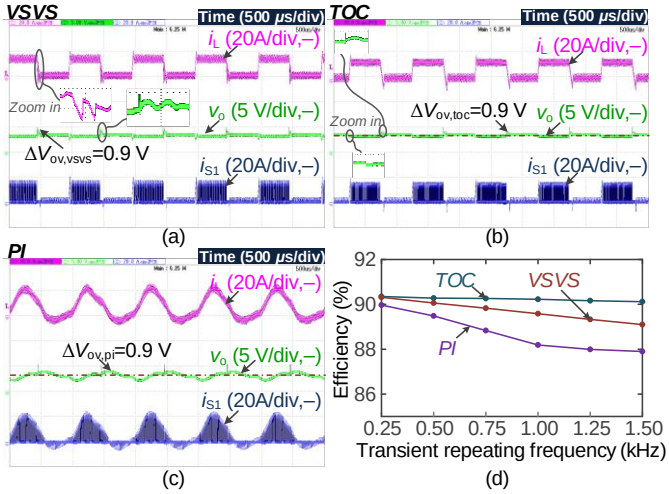


Fig. 10. Experimental results. (a) Experimental waveforms of the proposed VSVS scheme. (b) Experimental waveforms of the TOC scheme. (c) Experimental waveforms of the PI scheme. (d) Efficiency measurement results under repetitive load transients.

introduced, as discussed in the following sections.

III. Electro-Thermal Modeling and Accumulated Damage Analysis

MOSFETs and capacitors are the weakest links in power electronic converters. Generally, the wear-out failure of MOSFETs is mainly caused by the junction temperature fluctuation ΔT_j, and the failure of capacitors is dominated by the rise of hot-spot temperature [16]. In this section, the electro-thermal modeling of MOSFETs and capacitors is introduced. Then, the accumulated damage is analyzed based on the mission profile of a VRM used in a data center.

A. Electro-Thermal Modeling of Critical Components

Taking the TOC-controlled VRM as an example, Fig. 11(a) shows the typical electro-thermal waveforms of a converter with consecutive load transients, which is a simplified simulation result of VRMs carried out in PSIM 2021a. Here, i_o, $P_{loss,S2}$, $T_{j,S2}$, $P_{loss,Al}$, and $T_{h,Al}$ represent the load current, power loss of S_2, junction temperature of S_2, power loss of Al-Caps, and host-spot temperature of Al-Caps, respectively.

Fig. 11(a) shows that there exist power loss steps on S_2 during transients, however, the junction temperature fluctuation of S_2 is mainly caused by load change [17]. Therefore, the effect of transient on the lifetime damage of S_2 can be ignored. Similarly, the transient stress of S_1 does not need to be considered. Notice that S_{aux} in the proposed topology is only enabled during transients, the power loss during transient should be calculated.

Different from that for junction temperature fluctuation, the rise of hot-spot temperature is mainly caused by the average power loss. Referring to Fig. 11(a), it can be seen that the power loss of Al-Caps during transients is significantly larger than that for steady state. Therefore, the power loss of capacitors is dominated by transient stress, which should be considered in the reliability evaluation.

1) *Electrical Stress of MOSFETs and Capacitors*

The power loss of MOSFETs is comprised of conduction loss and switching loss. The conduction loss $P_{con,S}$ is calculated as

$$P_{con,S} = I_{S,rms}^2 R_{ds} \tag{10}$$

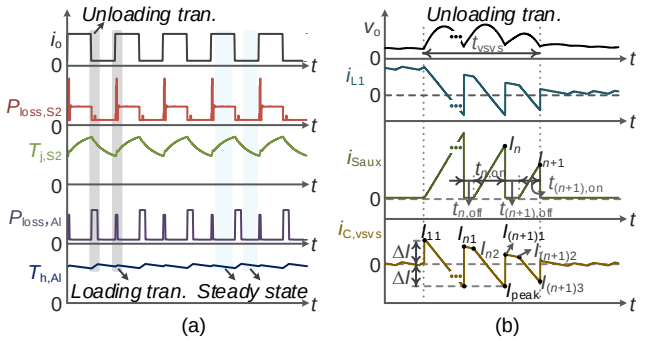


Fig. 11. Electro-thermal waveforms. (a) Electro-thermal waveforms of a TOC-controlled VRM. (b) Electrical response waveform of the proposed VSVS scheme.

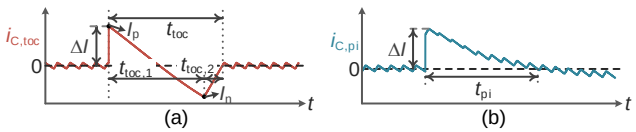


Fig. 12. Capacitor current of the TOC and PI schemes. (a) TOC scheme. (b) PI scheme.

where $I_{S,rms}$ represent the rms currents of MOSFETs. During steady state, the rms current $I_{S1,rms}$, $I_{S2,rms}$ of S_1 and S_2 for these three schemes are the same, i.e.,

$$I_{S1,rms}=\sqrt{di_o^2},\ I_{S2,rms}=\sqrt{(1-d)i_o^2}. \tag{11}$$

In the proposed VSVS scheme, the auxiliary switch S_{aux} is enabled during unloading transients. Referring to Fig. 11(b), the rms current $I_{Saux,rms}$ of i_{Saux} is calculated as

$$I_{Saux,rms}=\sqrt{\sum_{n+1}\left(1/3\left(I_{n+1}^2 t_{(n+1),on}\right)/t_{vsvs}\right)} \tag{12}$$

where I_{n+1} represents the peak current, and t_{vsvs} is the transient period of the VSVS scheme.

In (10), R_{ds} is the on-state resistance of MOSFETs, which is dependent on the junction temperature T_j, i.e.,

$$R_{ds}\left(T_j\right)=R_{ds,25°C,max}\left(1+\alpha/100\right)^{T_j-25}. \tag{13}$$

Here, $R_{ds,25℃,max}$ denotes the maximum value of R_{ds} at 25 ℃, α is the temperature coefficient, which can be obtained from the datasheet [31].

The switching loss $P_{sw,S}$ is calculated as

$$P_{sw,S}=\left(E_{on}+E_{off}\right)f_s \tag{13}$$

where E_{on} and E_{off} are the turn-on and turn-off energy loss of MOSFETs, which are detailed derived in [31].

Referring to Fig. 11(b), the rms value $I_{C,rms,vsvs}$ of transient capacitor current $i_{C,vsvs}$ in the proposed scheme is calculated as

$$I_{C,rms,vsvs}=\sqrt{I_{inter,(n+1)}+\sum_n I_{inter,n}} \tag{15}$$

where, the intermediary variables $I_{inter,n}$ and $I_{inter,(n+1)}$ are

$$\begin{cases} I_{inter,n}=1/3\left(I_{n1}^2+I_{n2}^2+I_{n1}I_{n2}\right)t_{n,off}/t_{vsvs} \\ \qquad +1/3\left(I_{n2}^2+I_{peak}^2+I_{n2}I_{peak}\right)t_{n,on}/t_{vsvs} \\ I_{inter,(n+1)}=1/3\left(I_{(n+1)1}^2+I_{(n+1)2}^2+I_{(n+1)1}I_{(n+1)2}\right)t_{(n+1),off}/t_{vsvs} \\ \qquad +1/3\left(I_{(n+1)2}^2+I_{(n+1)3}^2+I_{(n+1)2}I_{(n+1)3}\right)t_{(n+1),on}/t_{vsvs} \end{cases}. \tag{16}$$

In (16), I_{peak} is the peak current, I_{11}–$I_{(n+1)3}$ are the current values at each switching instant, which are detailed derived in [14].

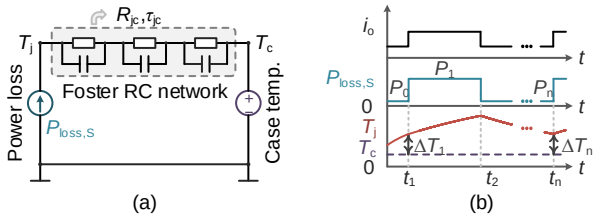


Fig. 13. Electro-thermal models of MOSFETs. (a) Thermal model of MOSFETs. (b) Electro-thermal waveforms of MOSFETs.

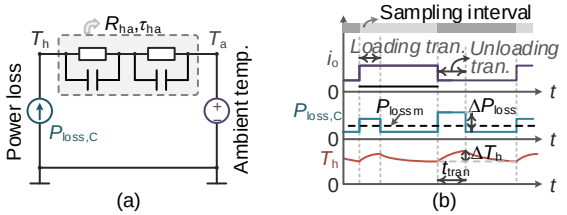


Fig. 14. Electro-thermal models of capacitors. (a) Thermal model of capacitors. (b) Electro-thermal waveforms of capacitors.

For comparison, Figs. 12(a) and 12(b) show the capacitor current in TOC and PI schemes. Referring to Fig. 12(a), the rms current $I_{C,rms,toc}$ is calculated as

$$I_{C,rms,toc}=\sqrt{1/3\left(I_p^2+I_n^2+I_pI_n\right)t_{toc,1}/t_{toc}+1/3I_n^2t_{toc,2}/t_{toc}} \tag{17}$$

where the current peak values I_p, I_n, and the transient durations t_{toc}, $t_{toc,1}$ and $t_{toc,2}$ are detailed derived in [8]. Referring to Fig. 12(b), the rms current $I_{C,rms,pi}$ is approximately calculated as

$$I_{C,rms,pi}=\sqrt{\Delta I^2/3} \tag{18}$$

During steady state, the rms current $I_{C,rms,s}$ of capacitor bank in these three schemes are the same, i.e.,

$$I_{C,rms,s}=v_o\left(1-d\right)/\left(2\sqrt{3}f_sL_1\right) \tag{19}$$

where f_s represents switching frequency.

Considering the current distribution of individual capacitor in capacitor banks, the rms current of the k-th capacitor is [27]

$$I_{C,rms,k}=I_{C,rms}\times\frac{1}{Z_k}\Big/\sum_{i=1}^{n}\frac{1}{Z_n} \tag{20}$$

where $I_{C,rms}$ represents the rms current of capacitor bank during steady state or transient, Z_k is the impedance of the k-th capacitor in the bank, and n is the number of capacitors. Using (19), the power loss of capacitors is calculated as

$$P_{C,rms,k}=I_{C,rms,k}^2\mathrm{ESR}_k. \tag{21}$$

2) *Thermal Stress of MOSFETs*

Fig. 13(a) shows the typical thermal model of MOSFETs, where T_j and T_c represent the junction temperature and case temperature, respectively [23]. Usually, a high-order Foster network can be implied as a first-order network by means of curve fitting [25]. Here, the total equivalent thermal resistance and thermal time constant from the junction (T_j) to case (T_c) are defined as R_{jc} and τ_{jc}, respectively.

Ignoring the power loss during transients, Fig. 13(b) shows the detailed electro-thermal response waveforms of MOSFETs, where $P_{loss,S}$ represents the power loss. According to the thermal model in Fig. 13(a), the junction temperature fluctuation ΔT_n can be calculated by interaction as

$$\Delta T_n=\Delta T_{n-1}e^{-(t_n-t_{n-1})/\tau_{jc}}+P_nR_{jc}\left(1-e^{-(t_n-t_{n-1})/\tau_{jc}}\right) \tag{22}$$

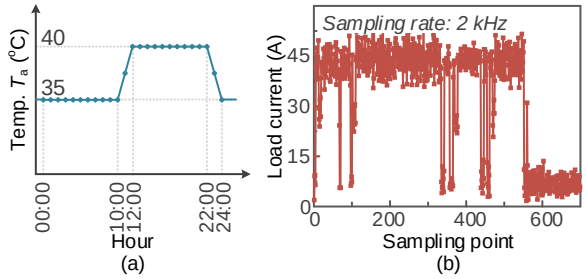


Fig. 15. Mission profile of a VRM in a data center. (a) Daily ambient temperature. (b) Loading profile of a VRM in a specified period.

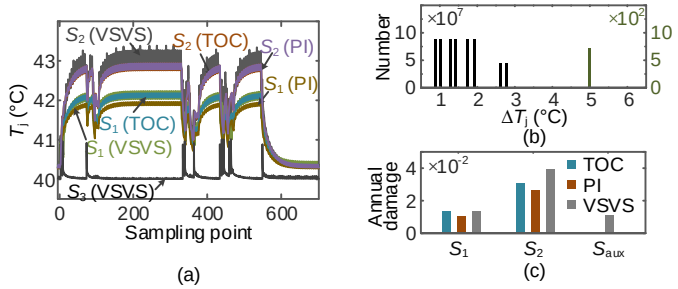


Fig. 16. Temperature profile, junction temperature fluctuation, and annual damage of MOSFETs. (a) Temperature profile in the specified period. (b) Statistical junction temperature fluctuation of S_2 in the TOC scheme. (c) Annual damage.

where ΔT_{n-1} is the previous temperature, P_n represent the power loss [25].

3) *Thermal Stress of Capacitors*

Fig. 14(a) shows the typical thermal model of capacitors, where T_h and T_a represent the hotspot temperature and ambient temperature, respectively [27]. R_{ha} and τ_{ha} are the total equivalent thermal resistance and thermal time constant from T_h to T_a, respectively. Fig. 14(b) shows the electro-thermal response waveforms of capacitors during two sampling intervals. It is easily found that the power loss during transients is larger than that for steady state.

Taking the unloading transient interval as a case study, the hotspot temperature fluctuation caused by step loss ΔP_{loss} is calculated as

$$\Delta T_h = \Delta P_{loss} R_{ha} \left(1 - e^{-t_{tran}/\tau_{ha}}\right) \tag{23}$$

where t_{tran} is the transient duration. Referring to Fig. 14(b), T_h during one sampling interval is approximately calculated as

$$T_h = T_a + P_{lossm} R_{ha} + 0.5\Delta T_h \tag{24}$$

where P_{lossm} is the mean loss of one sampling interval. The analysis in [27] demonstrates that T_h and P_{lossm} can be calculated using the mean value of one or multiple loading sampling intervals, the results are the same. Usually, τ_{ha} is larger than the transient duration, i.e., $\tau_{ha} >> t_{tran}$, then the hotspot temperature fluctuation ΔT_h can be ignored. T_h can be approximated as $T_h = T_a + P_{lossm} R_{ha}$.

B. Accumulated Damage Analysis

1) *Description of the Mission Profile*

Taking a VRM used in data centers as a case study, Fig. 15(a) shows the daily ambient temperature, where the sample rate is one hour [32]. The loading profile of a node component in data centers is shown in Fig. 15(b), where the sampling rate is 2 kHz [26], [27].

2) *Static Annual Damage of MOSFETs*

As shown in Fig. 15(a), the temperature of a data center is usually constant. Assuming the case temperature (i.e., ambient temperature T_a) of a VRM is 40 ℃, Fig. 16(a) shows the simulated temperature profile during the specified period, where the circuit parameters are same as that in Fig. 7. The simulation environment is PSIM 2021a. The type of MOSFETs is AUIRF1324, its R_{jc} and τ_{jc} are 1.031 ℃/W and 0.00107s, respectively [30]. Referring to the simulation results, it is found that the junction temperature of S_2 is larger than that of S_1 due to its relatively large electrical stress.

According to the simulation results in Fig. 16(a), the short-term junction temperature fluctuation of MOSFETs (caused by loading power fluctuation) can be counted with the help of a Rainflow counting algorithm [16]. Referring to the typical temperature profile shown in Fig. 16(a), it is found that the ambient temperature is changed 2 times in one day (the change amplitude is 5 ℃). For simplification, ΔT_j caused by ambient temperature fluctuation is defined as 5 ℃ (2 times every day). Assuming the temperature profile and loading profile are repeated every 24 h and 0.35 s, respectively, the long-time-scale temperature fluctuation (caused by ambient temperature fluctuation) and the short-time-scale temperature fluctuation (caused by loading power fluctuation) can be counted. Taking S_2 in the TOC scheme as an example, Fig. 16(b) shows the statistical results of ΔT_j for 1-year operation. Similarly, ΔT_j of MOSFETs in other schemes can be obtained using the same method. Although damage consumption caused by small-amplitude ΔT_j is relatively small, it has a non-negligible effect on component aging [33] [34]. In this case study, the temperature fluctuation larger than 0.5 ℃ is considered.

Furthermore, Fig. 16(c) shows the annual damage of MOSFETs, which are obtained based on the Coffin-Manson reliability model and Miner's rule [23], [24], i.e.,

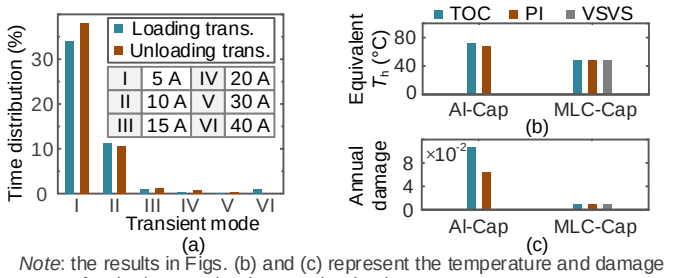
$$N_k = a \times \left(\Delta T_{j,k}\right)^{-b}, D_{MOS} = \sum_k n_k / N_k \tag{25}$$

where, N_k, $\Delta T_{j,k}$, and D_{MOS} represent the cycle-to-failure, thermal stress and accumulated damage, respectively. n_k is the number of cycles with the thermal stress $\Delta T_{j,k}$. a and b represent the scaling factor and exponential factor, which can be identified by fitting the experimental data of accelerated stress tests. According to the fitting results in [35], a and b are 5×10^{11} and 5.3, respectively.

Referring to Fig. 16(c), it is found that the damage consumption of S_2 is largest than S_1, due to its electro-thermal stress is relatively large in low-voltage high-current applications, i.e., low duty-cycle converters. The damage consumption of MOSFETs in the proposed scheme is slightly larger than that for TOC and PI schemes, the converter-level reliability needs to be further considered in order to evaluate the proposed scheme.

3) *Static Annual Damage of Capacitors*

In the foregoing analysis, the hotspot temperature is calculated using the sampling interval as a unit. For simplification, the loading profile is divided into six typical modes based on the step amplitudes of load current, i.e., Mode



Note: the results in Figs. (b) and (c) represent the temperature and damage of a single capacitor in capacitor banks.

Fig. 17. Transient-mode distribution, equivalent hotspot temperature and annual damage of capacitors. (a) Transient-mode distribution. (b) Equivalent hotspot temperature. (c) Annual damage.

I−Mode VI. The step amplitudes are 5 A, 10 A, 15 A, 20 A, 30 A, and 40 A, respectively. Assuming the loading profile is repeated every 0.35 s, the time distribution of different modes is shown in Fig. 17(a). Moreover, the long-term temperature profile is considered in the reliability evaluation processes. Referring to Fig. 17(a), the ambient temperature can be divided into three typical levels, i.e., 35 ℃, 37.5 ℃, and 40 ℃. Assuming the temperature profile is repeated every 1 day, durations are account for 42%, 8%, and 50%, respectively.

Considering the above-mentioned distributions of ambient temperature and transient modes as well as the effect of damage level on ESR and capacitance of capacitors [36], [37], the damage of capacitors can be estimated using the following lifetime model and damage model [22], [23], i.e.,

$$L_x = L_0 \times m^{\frac{T_0 - T_h}{n_1}} \times \left(V_x / V_0\right)^{-n_2},\ D_{CAP} = \sum l_x / L_x \tag{26}$$

where l_x, L_x, V_x represent the operation time, calculated lifetime, capacitor voltage under the case that the thermal stress is T_h. L_0, V_0, T_0 are the rated lifetime, rated voltage under the reference condition. Generally, the typical values of coefficients m, n_1, and n_2 are provided by capacitor manufactures based on accelerated aging tests. As reported in [38], m, n_1, and n_2 for polymer Al-Caps are 10, 20, and 0, respectively. For MLC-Caps, m, n_1, and n_2 are 2, 8, and 3, respectively [39].

Figs. 17(b) and 17(c) show the equivalent hotspot temperatures and annual damage of capacitors. It can be seen that the thermal stress of Al-Caps is larger than that for MLC-Caps, and the equivalent hotspot temperature of MLC-Caps in different schemes are similar due to its relatively small ESR and R_{th}. The results in Fig. 17(c) illustrate the damage consumption of MLC-Caps in the proposed scheme is similar to that for TOC and PI schemes due to the degradation of MLC-Caps is dominated by the voltage stress. Although the TOC scheme has superior transient performance when compared with the PI scheme, the damage consumption of Al-Caps is larger than that for PI schemes.

IV. Reliability Benchmarking

A. Monte Carlo Simulation

Generally, the lifetime model shown in (26) describes the wear-out failure of capacitors at the 1% lifetime percentile (i.e., B_1 lifetime). However, the lifetime model given in (25) is used to describe the wear-out failure of power switches at the 10% lifetime percentile (i.e., B_{10} lifetime) [16]. In order to estimate the lifetime of MOSFETs and capacitors at the same probability

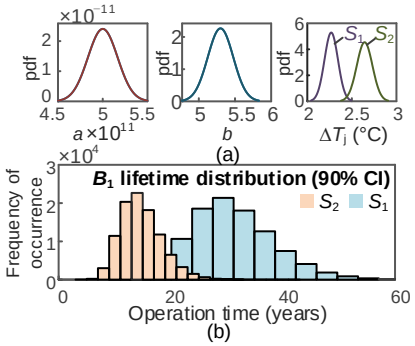


Fig. 18. Monte Carlo simulation for MOSFETs in the TOC scheme. (a) PDFs of the parameters. (b) B_1 lifetime distribution with 90% CI.

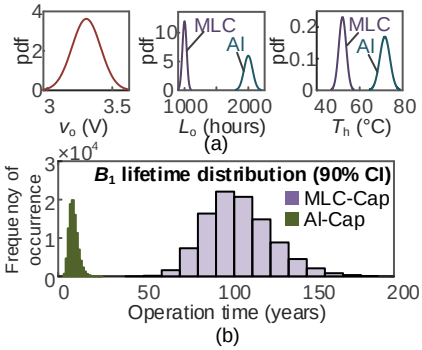


Fig. 19. Monte Carlo simulation for capacitors in the TOC scheme. (a) PDFs of the parameters. (b) B_1 lifetime distribution with 90% CI.

of failure level, the Weibull distribution is considered [40], i.e.,

$$f(t) = (\beta/\eta)\cdot(t/\eta)^{\beta-1} e^{-(t/\eta)^{\beta}},\ F(t) = 1 - e^{-(t/\eta)^{\beta}} \tag{27}$$

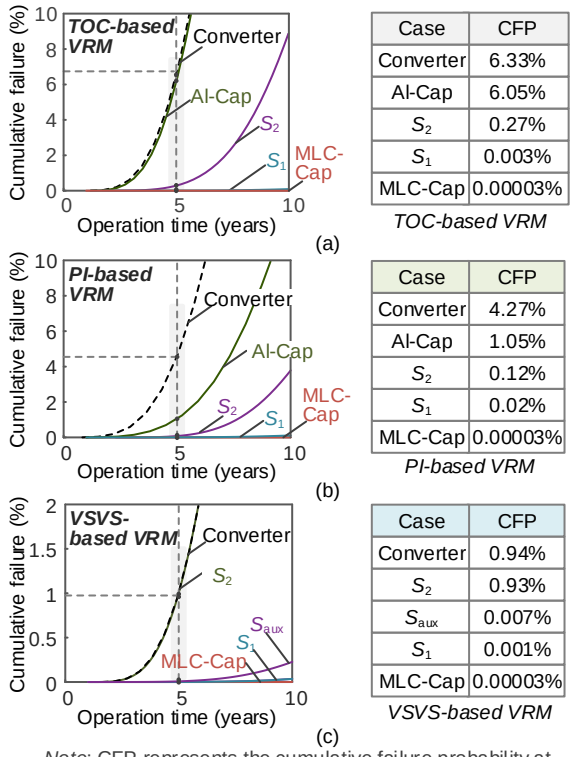
where $f(t)$ and $F(t)$ are the probability density function (pdf) and cumulative distribution function (CDF), β and η represent the shape and scale parameters, respectively. Assuming the shape parameter is β = 3, η can be calculated using the estimated B_{10} lifetime (i.e., the reciprocal of annual damage in Fig. (16) and (27). Then, the obtained CDF is used to estimate the B_1 lifetime.

Considering the uncertainty of lifetime model coefficients, component parameters, and mission profiles, a statistical approach is introduced to the evaluation process, i.e., Monte Carlo simulation [23], [24]. Referring to Fig. 18(a), assuming all the parameters (e.g., a, b, ΔT_j) have a 10% variation, 100000 samples are chosen to analyze the lifetime distribution of MOSFETs in the TOC scheme. The results of the Monte Carlo analysis are shown in Fig. 18(b), which illustrates that the B_1 lifetime (i.e., 1% probability of failure) of S_2 is between about 5 and 30 years, with a 90% confidence interval (CI). Due to a lower electro-thermal stress of S_1, its failure ranging between approximately 15 and 60 years.

Similarly, the lifetime distribution of capacitors can be calculated, as shown in Fig. 19. It can be seen that the Al-Cap seems to be more prone to failure when compared with the MLC-Cap. Furthermore, the lifetime distribution of MOSFETs and capacitors in the PI scheme and the proposed scheme can be obtained using the same method.

B. Converter-Level Reliability Benchmarking

The CDF curves of MOSFETs and capacitors in TOC, PI, and VSVS schemes are shown in the left parts of Fig. 20. Based on the reliability block diagram (RBD) method [23], the



Case	CFP
Converter	6.33%
Al-Cap	6.05%
S_2	0.27%
S_1	0.003%
MLC-Cap	0.00003%

TOC-based VRM

Case	CFP
Converter	4.27%
Al-Cap	1.05%
S_2	0.12%
S_1	0.02%
MLC-Cap	0.00003%

PI-based VRM

Case	CFP
Converter	0.94%
S_2	0.93%
S_{aux}	0.007%
S_1	0.001%
MLC-Cap	0.00003%

VSVS-based VRM

Note: CFP represents the cumulative failure probability at the end of 5 years of operation

Fig. 20. Cumulative wear-out failure probability curves and failure probability at the end of 5 years of operation. (a) Classical TOC scheme. (b) Classical PI scheme. (c) Proposed VSVS scheme.

converter-level reliability curves are obtained to analyze the failure probability (FP) of VRMs, which are also shown in Fig. 20. Assuming the target service lifetime of VRMs is 5 years [41], the right parts of Fig. 20 give the probability that the components and systems fail before the target service life. Notice that the CFP in the right part of Fig. 20 represents the failure probability of a single component. The component count should be considered in the converter-level reliability evaluation.

It can be seen that given 5 years of operation, the cumulative wear-out failure probability for the TOC, PI, and VSVS schemes are approximately 6.33%, 4.27%, and 0.94%, respectively, which illustrates that the proposed scheme can significantly improve the converter-level reliability under the same design aim. Comparing with the TOC and PI schemes, the failure probability at the end of 5 years of operation has decreased by 85% and 78%, respectively. The results also illustrate that Al-Cap is the weakest link in the classical TOC and PI schemes, however, MOSFET (i.e., S_2) is the weakest one in the proposed scheme.

Furthermore, Table III lists the cumulative failure probability (CFP), component counts, and total costs of these three schemes, where the types of capacitors are shown in Table II. The types of MOSFETs, synchronous driver, and auxiliary driver are AUIRF 1324, IRF21844, and MCP1401, respectively. Notice that the total costs of different schemes are calculated based on the price (for 1 quantity) provided by Digi-Key Electronics [42]. It is found that the cost of the proposed VSVS scheme is slightly higher than that for the TOC and PI schemes with the same design aim (i.e., the transient voltage overshoot and stead-state ripple amplitude). However, its reliability is significantly larger than TOC and PI schemes, which illustrates that the proposed scheme has a relatively high economy and reliability.

TABLE III
COMPARISON RESULTS OF DIFFERENT VRM SCHEMES

Schemes	TOC	PI	VSVS
CFP at the end of 5 years of operation	6.33%	4.27%	0.94%
Main components	MOSFET ×2, Al-Cap ×1, MLC-Cap ×3, syn. driver ×1	MOSFET ×2, Al-Cap ×4, MLC-Cap ×3, syn. driver ×1	MOSFET ×3, MLC-Cap ×2, syn. driver ×1, aux. driver ×1
Total cost [42]	9.84 $	11.52 $	12.44 $

Note: CFP-cumulative failure probability

V. CONCLUSION

This paper presents a virtual series voltage source (VSVS) based auxiliary circuit scheme, in order to reduce the capacitance requirement while guaranteeing the performance of VRMs. Then, its reliability performance benchmarking with classical TOC and PI schemes is conducted. The main conclusions are given as follows.

1) In order to achieve the same transient performance index (mainly refers to the small transient voltage overshoot) for VRMs with different control schemes, the system configuration and reliability are different. Although the capacitance requirement and cost of the state-of-the-art TOC scheme are less than that of the classical PI scheme, it has inferior reliability due to its electro-thermal stress is relatively large.
2) By using the proposed VSVS scheme, the converter-level reliability can be significantly improved. Comparing with the existing auxiliary circuit-based schemes, the component counts of the proposed scheme are minimum. However, the cost is slightly higher when compared with the classical TOC and PI schemes.
3) For VRMs with different system configurations, control strategies, and auxiliary circuits, the converter-level reliability can be evaluated using the same method. Moreover, the idea of the proposed auxiliary circuit could be applied in multi-phase non-coupled-inductor and coupled-inductor VRMs. However, the circuit topology and control strategy need to be further investigated in future work.

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