A robust passivity based model predictive control for buck converter suppling constant power load

Zhou, Jiyao; Zhang, Qianye; Hassan, Mustafa Alrayah; Zhang, Zehua; Hou, Mingxuan; Wu, Shang; Li, Yongjian; Li, Erping; Guerrero, Josep M.

Published in:
Energy Reports

DOI (link to publication from Publisher):
10.1016/j.egyr.2021.09.193

Publication date:
2021

Document Version
Publisher's PDF, also known as Version of record

Available online at www.sciencedirect.com
ScienceDirect
Energy Reports 7 (2021) 792–813
www.elsevier.com/locate/egyr

2021 International Conference on Energy Engineering and Power Systems (EEPS2021), August 20–22, 2021, Hangzhou, China

A robust passivity based model predictive control for buck converter suppling constant power load

Jiyao Zhou[a,b,*], Qianye Zhang[c], Mustafa Alrayah Hassan[d,e], Zehua Zhang[a,b], Mingxuan Hou[f], Shang Wu[g], Yongjian Li[a,b], Erping Li[h,i], Josep M. Guerrero[j]

[a] *State Key Laboratory of Reliability and Intelligence of Electrical Equipment, School of Electrical Engineering, Hebei University of Technology, Tianjin 300130, China*
[b] *Key Laboratory of Electromagnetic Field and Electrical Apparatus Reliability of Hebei Province, Hebei University of Technology, Tianjin 300130, China*
[c] *State Grid Integrated Energy Service Group CO., LTD, Beijing, 100010, China*
[d] *Department of Electrical Engineering, National Kaohsiung University of Science and Technology, Kaohsiung 807618, Taiwan*
[e] *Department of Electrical Engineering, University of Blue Nile, Damazeen 26613, Sudan*
[f] *Korqin District Power Supply Branch, East Inner Mongolia Electric Power Co., Ltd., States Grid, Tongliao 028000, China*
[g] *State Grid Jibei Electric Power Co., Ltd., States Grid, Beijing 102488, China*
[h] *Key Laboratory of Advanced Micro–Nano Electronic Devices & Smart Systems and Applications, College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China*
[i] *Zhejiang University–University of Illinois at Urbana-Champaign Institute, Zhejiang University, Haining 314400, China*
[j] *Center for Research on Microgrids (CROM), AAU Energy, Aalborg University, 9220 Aalborg East, Denmark*

Received 5 September 2021; accepted 29 September 2021

Abstract

In this paper, the instability problem caused by the constant power load in Buck converter is addressed. In order to solve this instability problem, a composite controller is proposed. Due to the double loop structure of this controller, the passivity based control (PBC) is adopted in the voltage loop to track the reference voltage and make the system stable, while a simplified continuous control set model predictive control (CCS-MPC) is selected as the current controller to track the current reference. Moreover, in order to improve the robustness of the controller and avoid the static error in output, a high order disturbance observer (HODO) is designed out to compensate the negative effects caused by the disturbance and uncertainty. Then, a mixed potential theory based large signal stability analysis is conducted to investigate the large signal stability of the studied system. In order to verify the proposed method, MATLAB simulation, OPAL-RT based hardware in loop and rapid control prototype experiments are conducted.

Peer-review under responsibility of the scientific committee of the International Conference on Energy Engineering and Power Systems, EEPS, 2021.

Keywords: Constant power load; Buck converter; DC microgrid; Model predictive control; Passivity based control

* Corresponding author.
E-mail address: 201611401002@stu.hebut.edu.cn (J. Zhou).

https://doi.org/10.1016/j.egyr.2021.09.193

Peer-review under responsibility of the scientific committee of the International Conference on Energy Engineering and Power Systems, EEPS, 2021.

1. Introduction

As an important part of future intelligent power distribution system, microgrid technology represents the future development trend of distributed energy supply system [1]. Recently, the number of PVs, batteries, supercapacitors, LED lighting, laptop, cellphone, EVs and other DC devices are increasing day by day, when these DC appliances are connected to AC microgrid, a large amount of interface power converters are needed, leading to an increment in the system cost and energy consumption. Moreover, compared with AC microgrid, DC microgrid are more easily to control since the absence of reactive power, phase and frequency. Therefore, the research and development of DC microgrid system has been largely prompted by the scholar from worldwide [2–6]. Fig. 1 depicts the normal structure of the DC microgrid, source plants such as PVs, ESS and the DC loads connect to the bus through interface power converters, the introduction of interface converter can largely improve the efficiency and controllability, however, some converter connected loads always operate in tight regulate mode. In this mode, they usually consume a fix amount of power regardless of the variation of the bus voltage, thus, they are redeemed as constant power load (CPL). The application of CPL will introduce the negative incremental impedance characteristics into the system, which will deteriorate the damping of system and cause the limit cycle dynamic [7–10]. This unwanted phenomenon will lead to the increment of the stress of the switches, which will lead to the temperature rising, reducing of the lifetime or even completely damage it. Moreover, from the perspective of system level, it also causes potential instability problem.

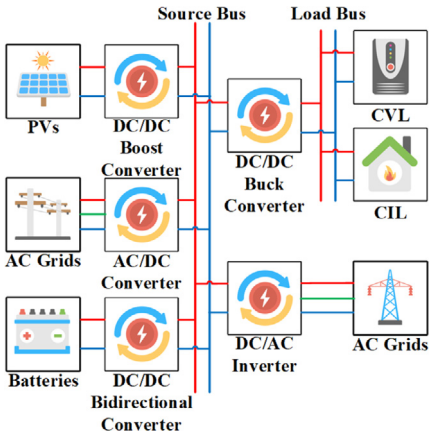

Fig. 1. A typical structure of DC microgrid system

In order to mitigates the instability problems caused by CPL, a large number of researches have been conducted. In [7–9], passive damping approach was adopted to increase the damping of the system, therefore, necessary inductors, capacitors, resistors or LC filters are designed and applied in the circuit. Although the passive damping approach can eliminate the energy oscillation caused by the CPL, the weight, cost and power loss of the system are also increased with the addition of the passive elements. In order to ensure the stability without additional power loss, active damping approaches are proposed, with the modification of the control loops, the impedance of load and source can be reshaped to improve the damping of the system [11,12]. However, these above methods are based on the linear small signal model, which can only ensure the stability around the operating points. In order to overcome this disadvantage, some nonlinear algorithm based stable controller are proposed [13–15]. A boundary controller is proposed in [13] to overcome the destabilizing effect caused by the CPL in the DC–DC Buck power converter. However, because this controller is designed based on the hysteresis band, the issues such as variable switching frequency and degraded ripple effect are introduced by its application. A fixed switching frequency sliding mode controller is designed in [14] to stabilize the CPLs over a wide operating range. However, this algorithm needs the measurement of DC capacitor voltage, which leads to a large equivalent series resistance and degraded ripple filtering effect. Moreover, the proposed method requires a very high switching frequency to operate which may cause the chattering problem. In [15], a synergetic control method is proposed to mitigate the CPL caused instability problem in parallel buck converters. However, detailed analysis for CPLs is lack in this paper. Disturbance observer techniques provide an effective way to estimate the disturbance, uncertainty and model

mismatch in the system. Therefore, better robustness and dynamic performance can be provided if control method can be combined with disturbance observer [16]. In [17], by the introduction of nonlinear disturbance observer, the proposed adaptive backstepping control can ensure the global stability of the boost converter system even when the CPL has a large variation. Another adaptive backstepping algorithm is presented in [18] for stabilizing boost converter suppling CPL with a third degree cubature Kalman filter for the estimation of the uncertainty. In [19], an adaptive passivity based control is combine with nonlinear disturbance observer to mitigates the instability problem in the buck converter suppling CPL. With the addition of the NDO, the control robustness is largely improved.

Model predictive control (MPC) is one of the most popular controllers among the industrial application, recently, with the development of the microprocessors, more and more MPC are used in power electronics by researchers [20]. In this algorithm, the predictive output state at next step is predicted through the predictive model equation, then the cost function will pick out the optimized control action which can track the reference best. Therefore, the performance of the model predictive control depends on the predictive model which will be easily impacted by the disturbance, uncertainty and model mismatch. For the buck converter feeding CPL in this paper, the disturbance, uncertainty and model mismatch can be represented by the variation of inductance, capacitance, equivalent series resistance of inductor, equivalent series resistance of capacitor, resistance and the CPL. In order to compensate the negative impact caused by them, some researches are conducted. An adaptive continuous control set model predictive control is proposed in [21] to track the voltage reference regardless of the variation of the resistance. In the proposed method, a Luenberger observer is designed to estimate the value of the resistor load, suppling with the real-time information, the proposed CCS-MPC can fulfill the reference tracking without static error. In [22], a finite control set model predictive control (FCS-MPC) is combined with proportional–integral (PI) controller and Luenberger observer to mitigate the output offset in boost converter caused by the model mismatch of the ESR of inductor. Although these literatures have demonstrated the feasibility of the disturbance observer based MPC algorithm against the uncertainty and model mismatch, the instability problem caused by CPL is not involved by them. Recently, several literatures focusing on the stable control of the converters suppling with CPL have been published. An explicit model predictive control (eMPC) is proposed in [23] to ensure the stability of the boost converter feeding CPL. However, rather than disturbance observer, this paper use sensor to obtain the load current, which will cause the increment of the cost and deterioration on the reliability. Similar, a decentralized model predictive control (DMPC) is proposed to ensure the power sharing and stability of the dc bus voltage in a multi boost converters system suppling CPL [24]. Similarly, in order to operates, this algorithm also needs to obtain the power of CPL by the addition of sensor. In [25], an extended Kalman Filter based adaptive model predictive control is proposed to ensure the stability of an onboard DC microgrid with CPLs, however, this controller stabilize the system from the secondary control level of the DC microgrids. An high order sliding mode observer(HOSMO) is adopted for the estimation of the disturbances in boost converter suppling CPL, and a model predictive control is work in parallel with the observer to track the reference. Due to the fast convergence rate of the HOSMO, this composite controller has a good performance, however, just as stated by the author, the tuning of this observer relies on time and experience hardly [26–28].

In this paper, an observer based robust CCS-MPC method is proposed to mitigates the instability problem caused by the CPL fed by the buck converter. During the construction of the feedback controller part, double loop control structure is adopted, in the outer loop, the passivity based control is applied, while a CCS-MPC method is designed and applied in the inner loop. For the feedforward estimation part, a high order disturbance observer is adopted. Combined together, the proposed method can ensure the rapid and accurate reference tracking even under disturbance and uncertainty. This paper is organized as follows: the system model and problem description are presented in Section 2. The foundation of the proposed control algorithm is shown in Section 3. Section 4 investigates the large signal stability of the proposed system. Section 5 verifies the proposed controller by MATLAB simulations and OPAL-RT based hardware in loop (HIL) experiments, moreover, the comparisons towards the previous nonlinear controllers are also shown in this section. Meanwhile, in Section 6, an OPAL-RT based rapid control prototype (RCP) experimental platform is built to further verify the proposed adaptive control algorithm.

2. Modeling and problem description

The typical architecture of DC microgrid is shown in Fig. 1, which is often applied in data center, telecom power supply and electrical transportation as EVs, electric ships or airplanes. As can be seen, the distributed generation, grid and energy storage system delivery their power to the source bus through source power converters, while the

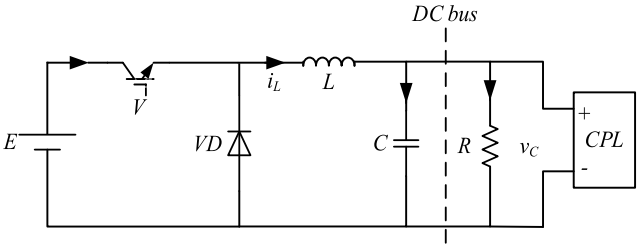

Fig. 2. Simplified cascade model of DC microgrid shown above.

loads bus are supplied by source bus through a buck converter since the difference of the voltage level between the source bus and load bus. As an important part of the power system, the load has high diversity, usually they can be divided into two kinds of load: constant impedance load (CIL) which is mainly represented by the heater; constant power load such as the motor and electronics device. The loads and its power supply in Fig. 1 can be simplified as the cascaded system shown in Fig. 2 which consists of buck converter and composite loads.

The dynamic model of the simplified system can be described as Eq. (1).

$$\begin{cases} L\dfrac{di_L}{dt} = E\mu - v_C \\ C\dfrac{dv_C}{dt} = i_L - \dfrac{v_C}{R} - \dfrac{P_{CPL}}{v_C} \end{cases} \tag{1}$$

where i_L and v_C represents the inductor current and capacitor voltage; E represents the input voltage of the source; R, L and C represents the resistive load, inductance and capacitance respectively; μ represents the duty ratio; i_{CPL} represents the power consumed by CPL. Eq. (1) is based on the condition when the whole system works in their rated condition. However, with the ignorance of uncertainty and disturbance, static error in the output will be generated, or even cause the instability problem of the whole system. When take these uncertainty and disturbance into consideration, Eq. (1) can be rewritten as

$$\begin{cases} L\dfrac{di_L}{dt} = E\mu - v_C + d_1 \\ C\dfrac{dv_C}{dt} = i_L - \dfrac{v_C}{R} - \dfrac{P_{CPL}}{v_C} + d_2 \end{cases} \tag{2}$$

where, d_1 represents the lumped disturbance caused by the variation of the input voltage and inductance.

$$d_1 = \frac{E}{L}\mu - \frac{E_0}{L_0}\mu + \frac{v_C}{L_0} - \frac{v_C}{L} \tag{3}$$

Similarly, d_2 reflects the lumped disturbance create by the variation of the CPL, CIL and capacitance.

$$d_2 = \frac{i_L}{C} - \frac{i_L}{C_0} + \frac{v_C}{C_0 R_0} - \frac{v_C}{CR} + \frac{P_{CPL0}}{C_0 v_C} - \frac{P_{CPL}}{C v_C} \tag{4}$$

where, R_0, L_0, C_0, E_0 and P_{CPL0} represent the rated value of the resistance, inductance, capacitance, input voltage and power of the CPL. Defining

$$\boldsymbol{x} = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} i_L \\ v_C \end{bmatrix}, \quad \boldsymbol{A} = \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}, \quad \boldsymbol{B} = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix},$$
$$\boldsymbol{R} = \begin{bmatrix} 0 & 0 \\ 0 & \dfrac{1}{R} + \dfrac{P_{CPL}}{x_2^2} \end{bmatrix}, \quad \boldsymbol{U} = \begin{bmatrix} E \\ 0 \end{bmatrix}, \quad \text{and} \quad \boldsymbol{d} = \begin{bmatrix} d_1 \\ d_2 \end{bmatrix}$$

Therefore, Eq. (1) and Eq. (3) can be rewritten as Eq. (5) and Eq. (6), respectively

$$\boldsymbol{A}\dot{\boldsymbol{x}} + (\boldsymbol{B} + \boldsymbol{R})\boldsymbol{x} = \mu \boldsymbol{U} \tag{5}$$

$$\boldsymbol{A_0\dot{x} + (B + R_0)x = \mu U_0 + d} \tag{6}$$

In the matrix shown above, A_0, R_0 and U_0 represent the rated value of A, R and U, respectively. The destination of the algorithm is to achieve global asymptotically equilibrium point under the existence of the disturbances or uncertainty, which is as follows

$$\lim_{t\to\infty} [x - x_d] = 0 \tag{7}$$

For Eq. (7), the $x_d = \begin{bmatrix} i_{Ld} & v_{Cd} \end{bmatrix}$ is the reference value of x, and for the initial value of x_0, $i_{L0} > 0$, $v_{C0} > \varepsilon$, where ε is a positive value.

3. The construction of the proposed controller

In this part, the design process of the proposed controller will be represented. This procedure contains three parts: the design of voltage loop controller, the design of current loop controller and the design of high order disturbance observer. For the voltage loop controller, it tracks the reference voltage and creates the reference current which will be used in the current loop controller. The current loop controller tracks the current reference and generate the PWM which will be used to drive the IGBT of the buck converter. Meanwhile, the HODO works in parallel with the double loop controller to compensates the output static error or mitigates the instability problem caused by the uncertainty or disturbance.

3.1. Design of the voltage loop controller

Fig. 3 shows the output of the system shown in Fig. 2 during different situations, as can be seen, when the resistance of the constant impedance load is larger than the equivalent resistance of the constant power load, the latter dominates the load impedance, thus, the output of the system oscillates. However, at the time of 0.05 s, the resistance of the CIL decrease by adding a parallel resistor, the CIL dominates the composite loads, the whole system become stable. Although, the introduction can stabilize the proposed system, it dissipates an extra amount of energy which leads to a decrease in the efficiency. Hence, in the voltage loop design period, the Passivity Based Control (PBC) theory is applied which can inject the damp without increase the energy loss and hardware cost. The PBC theory can be explained by Fig. 4, by the addition of virtual resistor R_V, the constant impedance load can be modified to dominate the whole composite load. Thus, the energy which leads to the limit cycle can be dissipated,

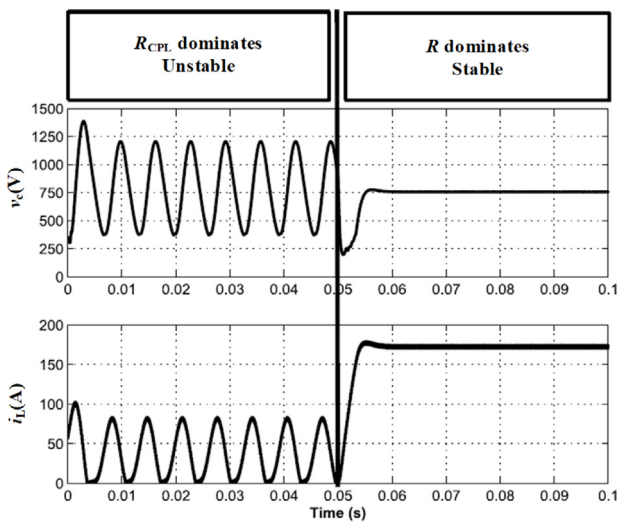

Fig. 3. Dynamic behavior of the buck system during different kind of load dominates.

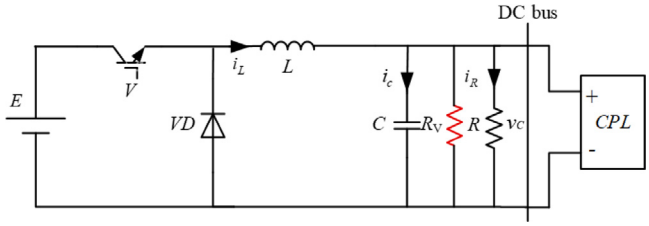

Fig. 4. Schematic diagram of passive control for proposed system.

and the output oscillation can be mitigated at the same time. Let the $x = \tilde{x} + x_d$, where $\tilde{x}$ is the error from output value set value x_d, Eq. (5) can be modified as below

$$\boldsymbol{A}\dot{\tilde{\boldsymbol{x}}} + \boldsymbol{B}\dot{\boldsymbol{x}} + \boldsymbol{R}\tilde{\boldsymbol{x}} + \boldsymbol{R_d}\tilde{x} = \mu\boldsymbol{U} - \boldsymbol{A}x_d + \boldsymbol{B}x_d + \boldsymbol{R}x_d + \boldsymbol{R_d}x_d \tag{8}$$

where R_{d} is the virtual matrix introduced into the system which can be represents as

$$R_d = \begin{bmatrix} 0 & 0 \\ 0 & R_V \end{bmatrix}$$

Due to the introduction of the virtual resistance, the transit energy of the system can be dissipated which is also consistent with the Lyapunov sense, the system will be become completely passive (stable). Therefore, the left part of Eq. (8) reaches a global asymptotically stable equilibrium point $\tilde{x} = 0$ [9,29]. Then, the stable control design can be obtained as

$$\mu\boldsymbol{U} - \boldsymbol{A}x_d + \boldsymbol{B}x_d + \boldsymbol{R}x_d + \boldsymbol{R_d}x_d = 0 \tag{9}$$

Since the buck converter belongs to the non-nominal phase system, the direct output voltage regulation approach can be easily deal by set $x_{2ref} = x_{20}$. Therefore, the PBC based voltage loop controller can be derived from Eq. (9) as

$$i_{ref} = \frac{V_{Cref}}{R} + \frac{P}{V_{Cref}} + \frac{1}{R_V}\left(V_{Cref} - v_C\right) \tag{10}$$

Although, Eq. (10) can operate well during the system in the nominal condition, static error or instability will be produced during the existence of uncertainty or disturbance. In order to make the system track its reference without offset, the voltage loop controller shown above should be modified by compensating the amount of the lumped disturbance or uncertainty, thus, Eqs. (9) and (10) can be rewritten as

$$\mu\boldsymbol{U} + \boldsymbol{d} - \boldsymbol{A}x_d + \boldsymbol{B}x_d + \boldsymbol{R}x_d + \boldsymbol{R_d}x_d = 0 \tag{11}$$

$$i_{ref} = \frac{V_{Cref}}{R} + \frac{P}{V_{Cref}} + \frac{1}{R_V}\left(V_{Cref} - v_C\right) - d_2 \tag{12}$$

3.2. Design of the current loop controller

Since the model predictive control has the advantages as rapid dynamic performance, simply to handle, accurate reference tracking ability [20], a continuous set model predictive controller is adopted as the inner loop control method. Different from other model predictive controller, its predictive horizon is set at only one, which can lead to a decrease of the computation burden [21]. Assuming the current change in one switching period is linearly as shown in Fig. 5, the rise or drop of the current is directly related to the state of the switch state. In Fig. 5, the t_n(n=1, 2, 3) is the time of the first turn on period, first turn off period and the second turn on period of the switch, i_{sn}(n=1, 2, 3) represents the current value at the instant of t_n(n=1, 2, 3), i_{s0} or $i_L(k)$ is the current at the end of last switching period.

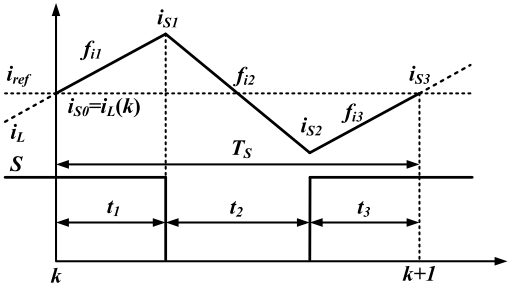

Fig. 5. Current waveform in one switching period.

Combined with Eq. (1), the slope of the current during different switching operation can be obtain by set the duty ratio as 1 or 0, thus the slope for the current in one switching period can be shown as

$$\begin{cases} f_{i1} = f_{i3} = \dfrac{E - v_C}{L} \\ f_{i2} = -\dfrac{v_C}{L} \end{cases} \tag{13}$$

According to the above equation, the current at each point can be calculated out. However, in order to simplify the equation and further reduce the computation burden, the t_1 and t_3 are forced to be equal. Then, the simplified equation to calculate the inductor current at $t_n(n = 1,2,3)$ is shown below

$$\begin{cases} i_{S1} = i_{S0} + f_{i1}t_1 \\ i_{S2} = i_{S0} + f_{i1}t_1 + f_{i2}t_2 \\ i_{S3} = i_{S0} + 2f_{i1}t_1 + f_{i2}t_2 \end{cases} \tag{14}$$

The tracking mode for the predictive current control method can mainly represented by the peak tracking mode, valley tracking mode and the average tracking mode [30,31]. In order to make sure the current algorithm has a good dynamic performance without static error, an improved average tracking mode will be applied by which all the current poles in one switching period can be taken into consideration by the cost function of MPC shown below.

$$J(k) = (i_{ref} - i_{S1})^2 + (i_{ref} - i_{S2})^2 + (i_{ref} - i_{S3})^2 \tag{15}$$

Combined equation (15) with Eqs. (13) and (14), the cost function can be rewritten as the equation represent by the slope and switching time as shown below

$$J(k) = (i_{ref} - i_{S0} - f_{i1}t_1)^2 + (i_{ref} - i_{S0} - f_{i1}t_1 - f_{i2}t_2)^2 + (i_{ref} - i_{S0} - f_{i1}t_1 - f_{i2}t_2 - f_{i3}t_3)^2 \tag{16}$$

Since t_1 is equal with t_3 forcibly, and t_2 can be expressed as $t_2 = T_S\text{-}2t_1$, the cost function can be redeemed as a quadratic equation whose minimum value can be easily calculated through its derivative. Thus, the value of t_1 which according to the minimum value of the cost function can be obtained by the equation shown below

$$\begin{cases} t_1 = t_3 = \dfrac{4(i_{ref} - i_{S0}) - 3T_S f_{i2}}{6(f_{i1} - f_{i2})} \\ t_2 = T_S - 2t_1 \end{cases} \tag{17}$$

With the acknowledge of the values of t_n(n=1,2,3), the duty ratio can be also been calculated as

$$\mu = \frac{2t_1}{T_S} \tag{18}$$

It is worthy to mention that in order to make the proposed algorithm operates, the PWM modulation needs to be the trailing triangle mode. The aforementioned process is based on the system works without any uncertainty or disturbance, however, ignorance of the them will lead the inaccuracy of the slope equation. To make the system

can track its reference accurately without offset, the slope equation (13) should be modified as shown below which can compensate the lumped disturbance.

$$\begin{cases} f_{i1} = f_{i3} = \dfrac{E - v_C - d_1}{L} \\ f_{i2} = -\dfrac{v_C + d_1}{L} \end{cases} \tag{19}$$

3.3. Design of the high order disturbance observer

The disturbances mentioned above are time-varying signals which cannot be measured easily without the increment of the cost of the system. In this situation, disturbance observer technology is a good choice to estimate the disturbances, especially for the high order disturbance observer which have a better performance on estimation of the time-varying disturbance when comparing with basic nonlinear disturbance observer [16,32]. Reformulate equation (2) as

$$\underbrace{\begin{pmatrix} \dot{i}_L \\ \dot{v}_C \end{pmatrix}}_{\dot{x}} = \underbrace{\begin{pmatrix} \dfrac{E\mu - v_C}{L} \\ i_L - \dfrac{v_C}{R} - \dfrac{P_{CPL}}{v_C} \end{pmatrix}}_{f(x,\mu,t)} + \underbrace{\begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}}_{F} \underbrace{\begin{pmatrix} d_1 \\ d_2 \end{pmatrix}}_{d(t)} \tag{20}$$

Thus, Eq. (20) can satisfy the normal form of the normal nonlinear system (Eq. (21)) on which the HODO will be developed

$$\dot{x} = f(x, \mu, t) + Fd(t) \tag{21}$$

where $x \in R^n$, $u \in R^m$, $d \in R^r$ are the state, the control input, and the disturbance vectors, respectively. $f(x, \mu; t)$ and the matrix F with rank(F)=r is known, and the state variables x are measurable and its initial value can be obtained. A reduced order system of Eq. (21) can be expressed as

$$F^+\dot{x} = F^+ f(x, \mu, t) + Fd(t) \tag{22}$$

where the matrix F^+ is the Moore–Penrose pseudo-inverse of the matrix F. In this paper, since the matrix F is the Identity matrix, F^+=F. Therefore, the reduced order system of Eq. (20) can be represented by itself. Accordingly, the high order disturbance observer can be expressed as

$$\begin{cases} \dot{z} = F^+ f(x, \mu, t) + \Gamma_0(F^+ x - z) \\ \hat{d} = \Gamma_0(F^+ x - z) \end{cases} \tag{23}$$

In the above equation, the $\hat{d}$ is the disturbance estimation vector, $\Gamma_0 = diag\{\gamma_{01}, \ldots, \gamma_{0r}\}$, $\gamma_{0i} > 0$ denotes the observer gains needs to be design. Thus, the high order disturbance observer for the proposed system can be expressed as

$$\begin{cases} \dot{z}_1 = \dfrac{1}{L}(\mu E - v_C) + \Gamma_1(i_L - z_1) \\ \hat{d}_1 = \Gamma_1(i_L - z_1) \end{cases} \tag{24}$$

$$\begin{cases} \dot{z}_2 = \dfrac{1}{C}(i_L - \dfrac{v_C}{R} - \dfrac{P_{CPL}}{v_C}) + \Gamma_2(v_C - z_2) \\ \hat{d}_2 = \Gamma_2(v_C - z_2) \end{cases} \tag{25}$$

Defining the disturbance estimation error as

$$e_d = \hat{d} - d \tag{26}$$

Combining Eqs. (26), (22) and (23), the dynamics of disturbance estimation error can be derived as

$$\dot{e}_d = -\Gamma_0 e_d \tag{27}$$

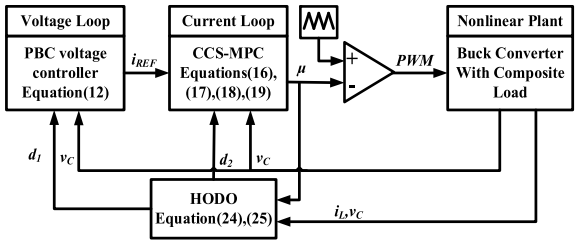

Fig. 6. Schematic diagram of the proposed controller.

Therefore, if the observer gain Γ_0 is chosen as a Hurwitz matrix, the error of the estimation will finally converge to zero. Therefore, the robust controller proposed in this paper can be represented as Fig. 6 shown below. As can be seen, with the information of output state and disturbance, the PBC based controller in the voltage loop tracks the reference voltage and generate the inductor current reference which will be applied by CCS-MPC in the inner loop. Then the circuit performs with the received PWM signal and generate the related output. With the acquirement of the output state and duty ratio, HODO can estimate the disturbance. At last, the output the disturbance information will be sent into the double loop controller to calculated the PWM signal for the next cycle.

4. The large signal stability of the proposed method

The large signal stability of the proposed system will be investigated in this part through mixed potential theory. The mixed potential theory was first proposed in 1960s [33,34], before it is used in the large signal stability analysis towards the power electronics, it was applied to investigate the stability of the nonlinear circuits [35]. The unified form of the mixed potential function can be expressed as follows

$$P(i, v) = -A(i) + B(v) + (i, \gamma v - \alpha) \tag{28}$$

where $A(i)$ is the current potential function, $B(v)$ is the voltage potential function, γ is a circuit structure-related constant matrix, and α is a constant vector. There are three related stability theorems for the mixed potential function based large signal stability analysis. Since the current potential function is linear in the first stability theorem, and the voltage potential function is linear in the second theorem, neither of them are suitable for the studied system. Therefore, the large signal stability analysis can only adopt the third theorem shown below

If $\mu_1 + \mu_2 \geq \delta(\delta > 0)$, for all i, v and

$$P^*(i, v) = (\frac{\mu_1 - \mu_2}{2})P(i, v) + \frac{1}{2}(P_i, L^{-1}P_i) + \frac{1}{2}(P_v, C^{-1}P_v) \to \infty \tag{29}$$

As $|i| + |v| \to \infty$, all solutions of the studied system will approach the equilibrium solutions as $t \to \infty$ [33,34]. In Eq. (29), μ_1 is the minimum eigenvalue of $L^{-1/2}A_{ii}(i)L^{-1/2}$ and μ_2 is the minimum eigenvalue of $C^{-1/2}B_{vv}(v)C^{-1/2}$, and $P_i = \partial P(i, v)/\partial i$, $P_v = \partial P(i, v)/\partial v$, $A_{ii}(i) = \partial^2 A(i)/\partial i^2$, $B_{vv}(v) = \partial^2 B(v)/\partial v^2$.

For proposed controller and the system shown in Fig. 2, the value of the inductor current is directly related to the error between capacitor voltage and its reference, moreover, the current drown into the CPL also has direct relationship with the its input voltage. Thus, the source part and the CPL are regarded as controlled current source, thus, the equivalent circuit of the proposed system can be shown as Fig. 7. Based on this equivalent circuit and the construction process aforementioned, the mixed potential function for the proposed system can be expressed as

$$P(i, v) = \int_0^{i_L} v_C di_L - \int_0^{i_R} v_C di_R - \int_0^{i_{CPL}} \frac{P_{CPL}}{i_{CPL}} di_{CPL} - v_C(i_L - i_R - i_{CPL}) \tag{30}$$

where, the i_R and i_{CPL} denote the current drown to the CIL and CPL, respectively. By applying the partial integral method, the above equation can be simplified as

$$P(i, v) = -\int_0^{v_C} i_L dv_C + \int_0^{v_C} i_R dv_C + \int_0^{v_C} \frac{P_{CPL}}{v_C} dv_C \tag{31}$$

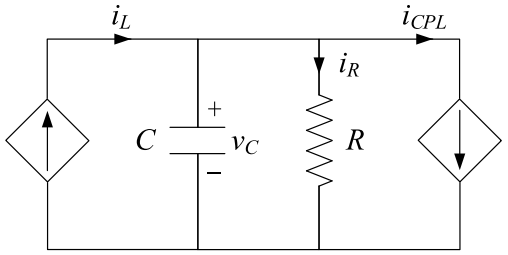

Fig. 7. The Equivalent circuit of the cascade Buck converter with composite loads.

Then, Eq. (31) can be rewritten to a unified form as

$$\begin{cases} A(i) = 0 \\ B(v) = -\int_0^{v_C} i_L dv_C + \int_0^{v_C} i_R dv_C + \int_0^{v_C} \dfrac{P_{CPL}}{v_C} dv_C \\ (i, \gamma v - \alpha) = 0 \end{cases} \tag{32}$$

According to the third theorem of the mixed potential theory

$$\begin{cases} A_{ii} = 0 \\ B_{vv} = -\dfrac{\partial i_L}{\partial v_C} + \dfrac{1}{R} - \dfrac{P_{CPL}}{v_C^2} \end{cases} \tag{33}$$

Assuming the current control can track the reference current rapidly and precisely, Eq. (33) can me modified by combined voltage loop controller.

$$\begin{cases} A_{ii} = 0 \\ B_{vv} = \dfrac{1}{R_V} + \dfrac{1}{R} - \dfrac{P_{CPL}}{v_C^2} \end{cases} \tag{34}$$

Finally, when $|i| + |v| \to \infty$, the $P^*(i, v) \to \infty$, and the large signal stability theorem for proposed system can be expressed as

$$\frac{1}{C}\left(\frac{1}{R_V} + \frac{1}{R} - \frac{P_{CPL}}{v_C^2}\right) > 0 \tag{35}$$

Therefore, it can be observed from the above equation that by the large signal stability can be guaranteed if the virtual resistance R_V is tuned properly. According to Eq. (35), the large signal stability boundary scan of the proposed system can be represented as Figs. 8 and 9.

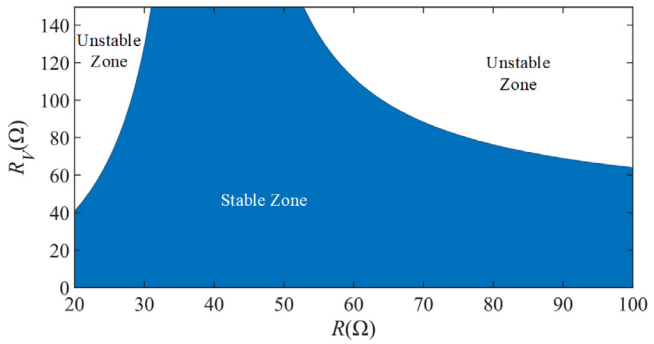

Fig. 8. Large signal stability boundary graph of the proposed system during the variation of CIL. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

Both the above two figures are derived from the mixed potential theory based large signal stability theorem shown in Eq. (35), the difference between them is that, in Fig. 8, the impedance of the CIL is independent variable

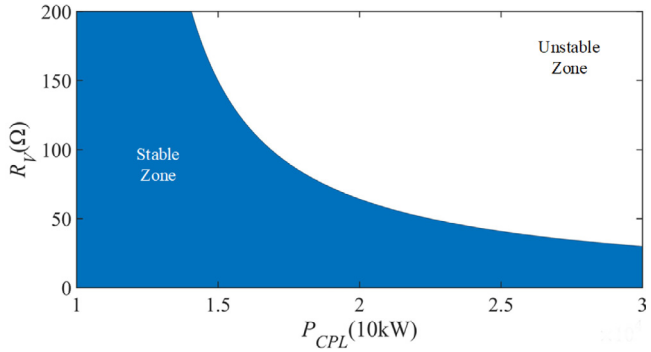

Fig. 9. Large signal stability boundary graph of the proposed system during the variation of CPL. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

while in Fig. 9 the independent variable change to the power of the CPL. During the construction process of Fig. 8 and Fig. 9, except for the virtual resistance and independent variable, all the other parameters are set at their rated value. As can be seen from the above two figures, each of them are divided into stable zone which is marked in blue and unstable zone which is marked in white. During the change of the independent variable, if the point (R, R_{V}) or (P_{CPL}, R_{V}) locates in the blue area, the proposed system is regraded as large signal stable system according to the mixed potential theory, or large signal instability if they do not. Since the virtual resistance is set at 0.2 Ω and the variations of the CIL and CPL are [33.3, 50] Ω and [14.4, 21.7] kW, respectively, according to Eq. (35), Figs. 8 and 9, the large signal stability of the proposed system is ensured by the proposed controller.

5. Simulation results and discussions

In order to represent the robustness of the proposed algorithm towards the disturbance and uncertainty, the related MATLAB simulations are conducted. During these simulations performing, the virtual resistance R_V is set as 0.2, since a higher value will create static error in the output voltage, while a less value make the dynamic performance faster but with large output ripple. The observer gains Γ_1 and Γ_2 are set at 1000 and 5000, respectively, since the larger gain will not only make the error converge fast but also introduce the ripple into the estimated value. For the other parameter relating to the proposed system, their values are shown in Table 1.

Table 1. System parameters.

Variable	Description	Value
V_{ref}	Output voltage reference	750 V
f_s	Switching frequency	20 kHz
E	Nominal input voltage	1500 V
R	Nominal resistive load	50 Ω
L	Inductance	4 mH
C	Capacitance	1 mF
P_{CPL}	Nominal power of CPL	14.4 kW

5.1. Input voltage variations

The dynamic performance of the proposed method during the variation of the input voltage is shown in Fig. 10. The change of the input voltage is shown in the third subfigure of it, as can be seen, the input voltage decreases to 1000 V from 1500 V and recover to its nominal value in a few seconds, after that it increases to 2000 V and back to 1500 V in the end. During these variations, the output voltage is regulated at its reference value tightly, the largest transit deviation is about 0.3 V which is eliminated quickly, and no obvious change can be observed in the inductor current.

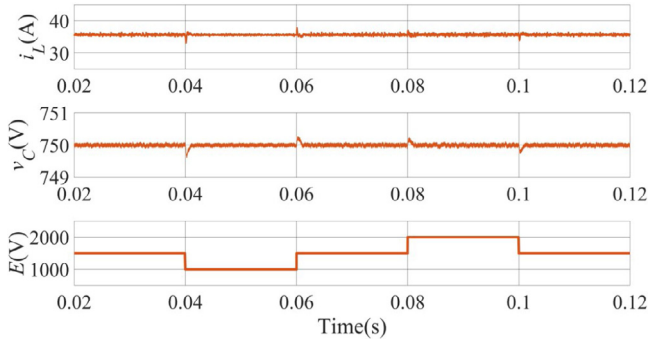

Fig. 10. The output waveforms of the proposed system during the variation of input voltage.

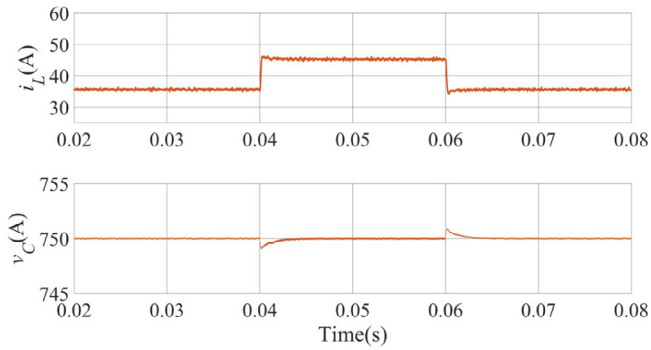

Fig. 11. The output waveforms of the proposed system during the variation of CPL.

5.2. CPL variations

In this part, the robustness of the proposed system under the variation of the CPL will be verified. As presented in Fig. 11, the power of the CPL P_{CPL} increases from 14.4 kW to 21.7 kW in the instant of 0.04 s and back to its rated value of 14.4 kW at 0.06 s. As can be observed in Fig. 11, the output voltage can track its reference value accurately and rapidly, the largest deviation during the change of CPL is about 0.8 V and it is eliminated in 2 ms, while the inductor current operates according to variation of P_{CPL}.

5.3. CIL variations

In this section, the performance of the proposed algorithm against the CIL change will be presented. Fig. 12 depicts its dynamic performance during the change of the CIL from 50 Ω to 33.3 Ω at 0.04 s and back to its rated value at 0.06 s. As can be seen, during the drop of the CIL from 50 Ω to 33.3 Ω, the output voltage only has a slight variation about 0.6 V from its rated value. Similarly, when the resistance of CIL recover to 50 Ω, except for the tiny overshoot of around 0.5 V no change can be observed. For the inductor current, it changes with the power consumed by the CIL.

5.4. Comparison simulation towards nominal CCS-MPC

In order to further verify the robustness of the proposed controller, comparison simulations are performed between the proposed method (in red) and the nominal CCS-MPC controller (in blue) which is same as the proposed controller but without the HODO parts. The comparison simulation towards nominal method during the change of input voltage is shown in Fig. 13. In this simulation, the change of the input voltage is same with that shown in Fig. 10, it can be observed that static errors are generated by the nominal controller, however, the proposed

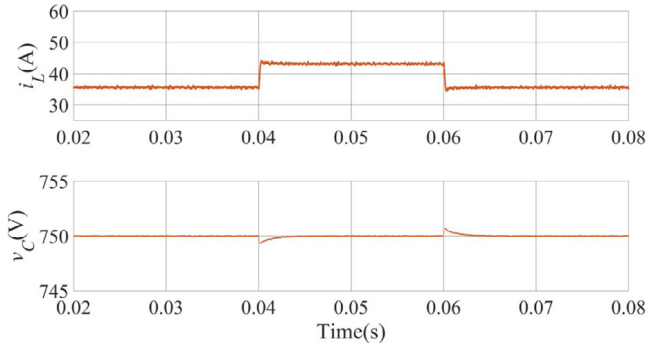

Fig. 12. The output waveforms of the proposed system during the variation of CIL.

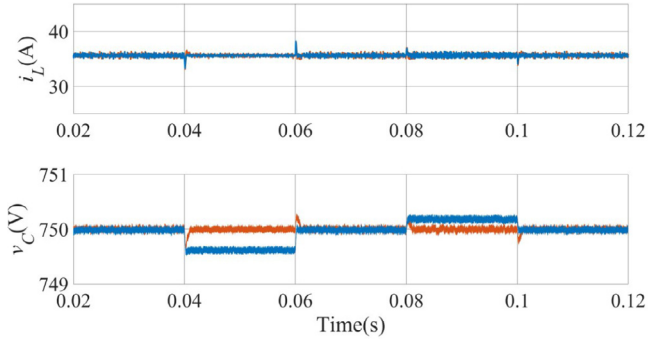

Fig. 13. The comparison simulation towards the nominal CCS-MPC during the variation of input voltage. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

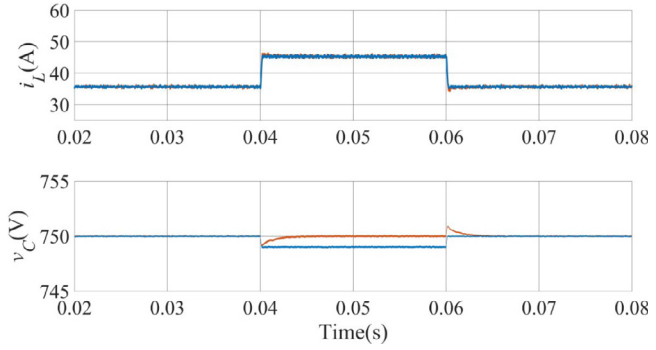

Fig. 14. The comparison simulation during the variation of CPL between the proposed method and nominal CCS-MPC. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

method can maintain the robust operation during the variation of the input voltage and no obvious static error can be observed.

Fig. 14 represents the comparison simulation towards the nominal CCS-MPC controller during the CPL changes which is similar with that shown in Fig. 11. As can be seen, with the increment of P_{CPL} the nominal CCS-MPC (in blue) failed to track the reference and a negative static error is created, while the proposed controller (in red) can track the reference and no offset can be found.

The compared simulation results between the proposed algorithm (in red) and nominal method (in blue) during the variation of constant impedance are shown in Fig. 15. As a further verification of Fig. 12, the change of the impedance is same with that in Fig. 12. It can be observed, during decrease of the impedance the output voltage of

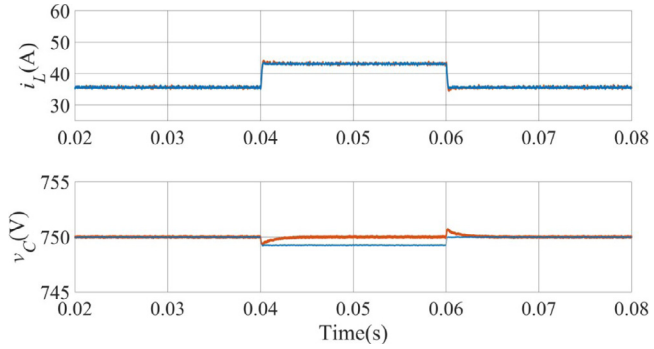

Fig. 15. The comparison simulation during the variation of CIL between the proposed method and nominal CCS-MPC.

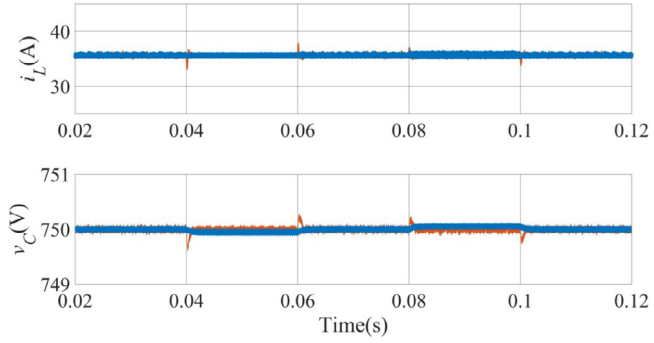

Fig. 16. The comparison simulation during the variation of input voltage between the proposed algorithm and PBC+NDO. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

the nominal controller drops about 1 V, and this offset exists until the impedance recover to its rated value. While the proposed method can fulfill the accurate tracking during the disturbance happens.

Thus, it can be proved that the proposed controller is robust enough to operates under the variation of the input voltage, constant impedance load and constant power load. In the following parts, further comparison simulation will be conducted to show the dynamic performance of the proposed controller. In that part, the nonlinear disturbance observer based PBC (PBC+NDO) controller presented in [19] will be taken as a contrast.

5.5. Comparison simulation towards PBC+NDO

The comparison simulation between the proposed algorithm (in red) and the PBC+NDO (in blue) is conducted under the same condition represented in Fig. 10. As can be observed in Fig. 16, during the rise and drop of the input voltage, slight static errors can be observed in the output voltage of the PBC+NDO when the input voltage is not at its rated value, while the proposed method can track the reference accurately.

Fig. 17 shows the comparison simulation between the proposed algorithm (in red) and PBC+NDO (in blue) during the step changes of CPL. It can be seen, during the step-up change of the CPL from 14.4 kW to 21.7 kW, the output voltage of PBC+NDO has a deviation around 4 V while that of proposed algorithm is only around 1 V and its settling time is only a half of that of PBC+NDO. The results for these two controllers under the step-down of the CPL are similar, the proposed method shows advantage in both the overshoot and settling time.

The simulated dynamic performance of those two controllers under the change of the resistance is shown in Fig. 18. During the step-down of the CIL from 50 Ω to 33.3 Ω, a deviation about 3 V is generated by PBC+NDO which takes around 3 ms of it to mitigates, and similar results can be observed during the step-up change of the CIL from 33 Ω to 50 Ω. However, the proposed method only takes around one third of that time to eliminated the 1 V deviation for the both changes. Therefore, it can be known that the proposed controller is not only robust against the disturbance but also have a good dynamic performance when compared with recent control algorithm.

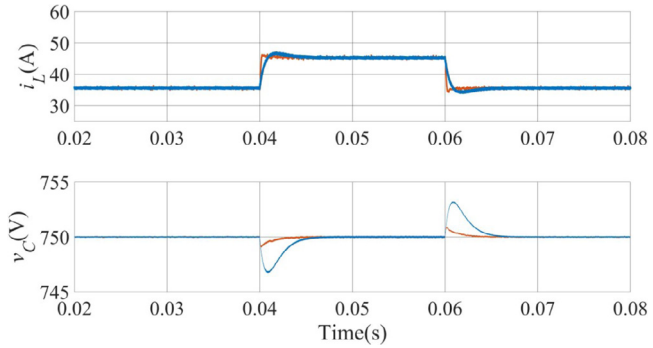

Fig. 17. The comparison simulation during the variation of CPL between proposed algorithm and PBC+NDO. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

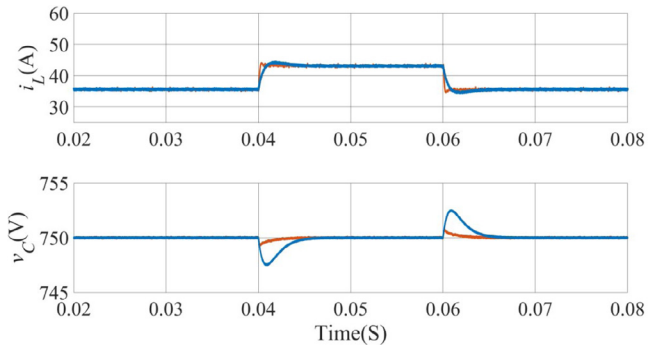

Fig. 18. The comparison simulation during the variation of CIL between proposed algorithm and PBC+NDO.

However, above results are all based on MATLAB simulation which is not a real-time simulation, in order to get the simulation results which is closer to the hardware experiment, real time simulation will be conducted in the following parts.

In order to further verify robustness and dynamic performance, an OPAL-RT based hardware in loop (HIL) experimental platform is constructed, and its detailed constructure is shown in Fig. 19. In this laboratory platform, the DSP TMS320F28335 embedded with proposed controller is act as the controller, while the OPAL-RT with

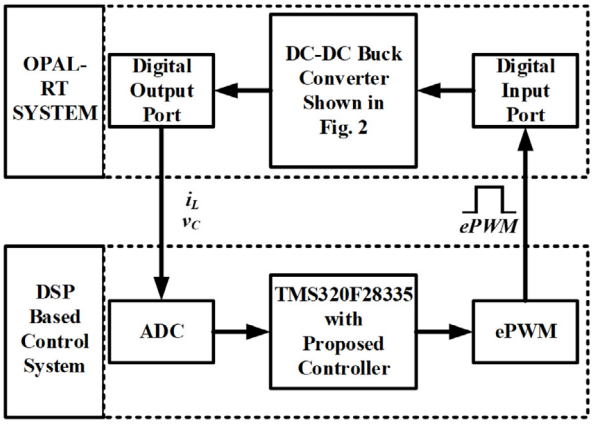

Fig. 19. Schematic diagram of the OPAL-RT based HIL experimental platform.

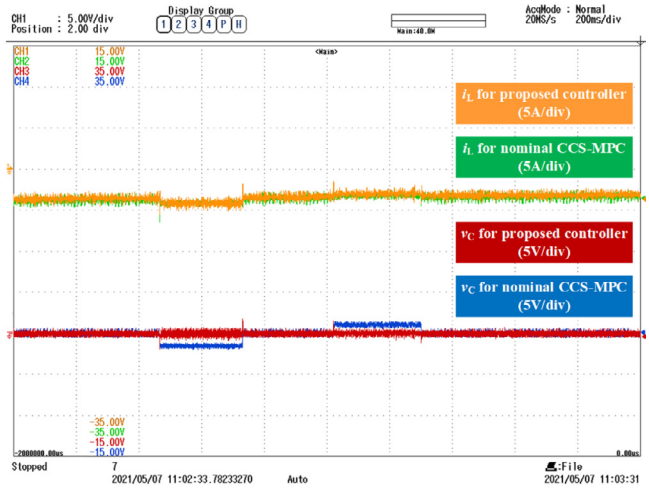

Fig. 20. The HIL comparison experiment between proposed controller and nominal CCS-MPC during the input voltage change.

proposed circuit inside operates as the control plant. The detailed control process is depicted as follow: the AC port of DSP obtains the output states from the OPAL-RT, after calculated by DSP controller, the related PWM signal is generated and send to the digital input port of the OPAL-RT. Then, the output states are calculated with the given PWM signal on the circuit planted in the OPAL-RT and are exported through the analogy signal output port of the OPAL-RT. It is worthy to mention that due to the output range of the OPAL-RT is limited from -16 V to $+16$ V, in order to fits this limit, the output voltage is subtracted by 750 V and the inductor current is subtracted by 50 A. Moreover, the minimum stepping time of OPAL-RT is 50 μS, so the step size is modified to 10^{-5} s from 10^{-6} s and the switching frequency for the IGBT in the buck converter is reduced from 20 kHz to 10 kHz. For other parameters, they are just same with that shown in Table 1 without any change.

In order to verify the results obtained from the simulation related to Fig. 13, the similar HIL experiment is conducted and its result is shown in Fig. 20. During this experiment, the change of the input voltage is similar with that in Fig. 13. As can be seen, the similar conclusion can be drawn that the proposed controller can operates accurately during the input voltage variation, however, an obvious static error can be observed in the output voltage of the nominal CCS-MPC controller. Fig. 21 shows the contrast HIL experiment between the proposed method and

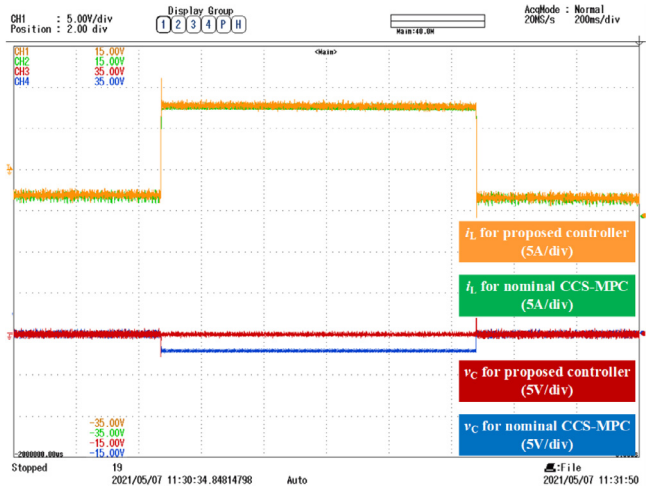

Fig. 21. The HIL comparison experiment between proposed controller and nominal CCS-MPC during the CPL change.

Fig. 22. The HIL comparison experiment between proposed controller and nominal CCS-MPC during the CIL change.

the nominal CCS-MPC during the variation of CPL. In this experiment, the change of the CPL is similar with that in Fig. 14. As can be seen, with the increment of the CPL, the output voltage of the nominal controller decreases from the reference around 3 V, while the proposed controller can fulfill the accurate and rapid tracking of the reference voltage. Fig. 22 shows the comparative HIL experiment between the proposed method and nominal controller during the variation of impedance which is similar with the simulation depicts in Fig. 15. As can be seen, with decrease of the impedance, a static error can be observed in the output voltage of the nominal CCS-MPC method, however, the proposed method can keep the static error free operation. Thus, the conclusion can be drawn that with the addition of HODO, the disturbances can be compensated to enhance the robustness of the controller.

In the following part, the comparative HIL experiments are conducted between the proposed method and PBC+NDO during the variation of the input voltage, CIL and CPL. In order to verify the results shown in 16, the corresponding HIL experiment is conducted and its results is shown in Fig. 23. As can be seen, the proposed method can track the reference voltage tightly. However, tiny errors can be found in the output of the PBC+NDO during the variation of the input voltage away from its rated value. Its static errors during the input voltage of 1000 V and 2000 V are 0.4 V and 0.3 V, respectively, these static errors exist until the input voltage return to its rated value.

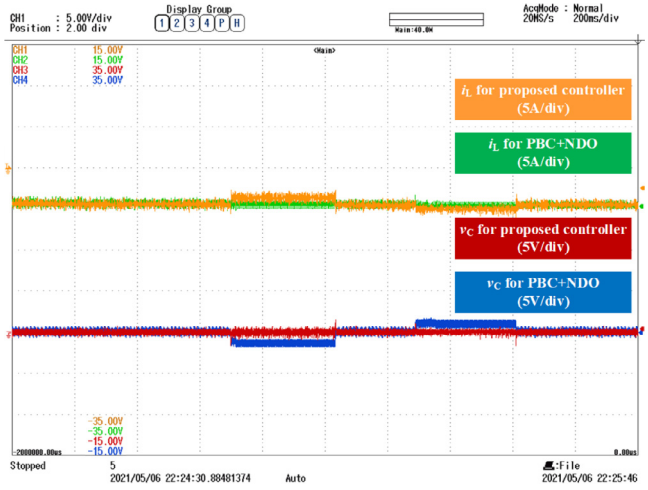

Fig. 23. The HIL comparison experiment between proposed controller and PBC+NDO during the input voltage change.

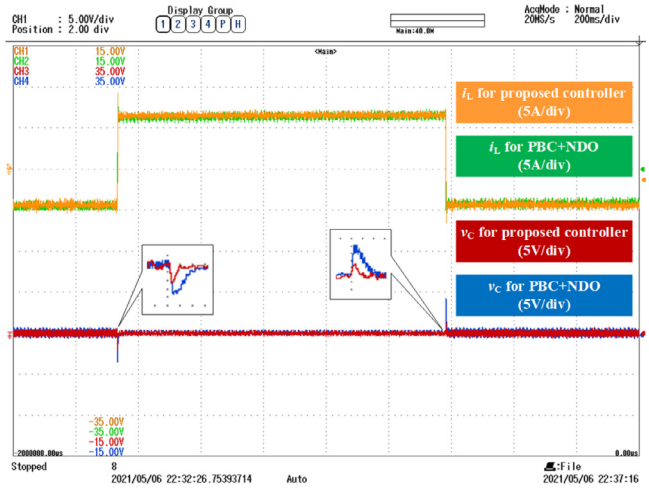

Fig. 24. The HIL comparison experiment between proposed controller and PBC+NDO during the CPL change.

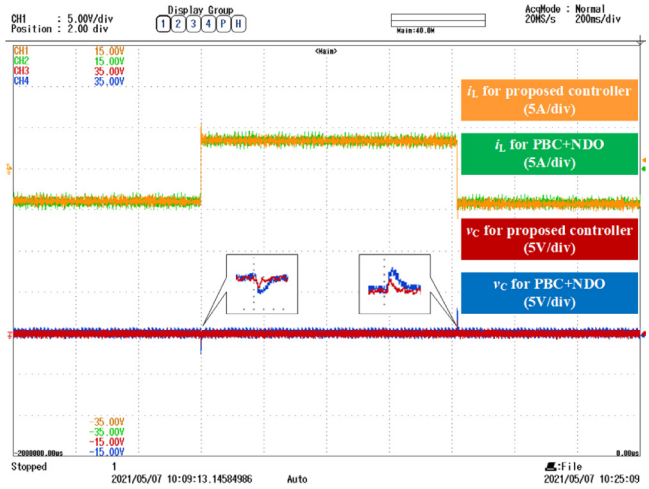

Fig. 25. The HIL comparison experiment between proposed controller and PBC+NDO during the CIL change.

Fig. 24 depicts the comparative HIL experiment which is conducted between the proposed method and PBC+NDO during the CPL variation. In this experiment, overshoots can be observed in the output voltage of both controllers during the step variations of the CPL. During the step-up variation of the CPL from 14.4 kW to 21.7 kW, the overshoots of the proposed method and PBC+NDO are 2.3 V and 4 V respectively, and those for the step-down variation are 2.5 V and 4.2 V respectively. Meanwhile, the settling time for the PBC+NDO are 5 ms for the step-up variation and 4 ms for step-down variation, while those for proposed algorithm are both around 2 ms.

The results of the comparison during the variation of the CIL is represented in Fig. 25. As can be observed, with the resistance of the CIL drop from 50 Ω to 33.3 Ω, the PBC+NDO needs 4 ms to mitigates the overshoot of 2.5 V while the proposed method needs 2 ms to mitigates the overshoot of 1.5 V. Similarly, when the resistance recovers back to 50 Ω, it takes the PBC+NDO 5 ms to eliminates the overshoot of 3 V, while for the proposed method it only cost 2 ms to back to the reference voltage from 1.6 V. Through the HIL experiments shown above, it can be found that the proposed algorithm is not only robust enough but also has a good dynamic performance. When compared towards PBC+NDO, its amplitude is half of that of the contrast controller, and its settling speed is also two times faster.

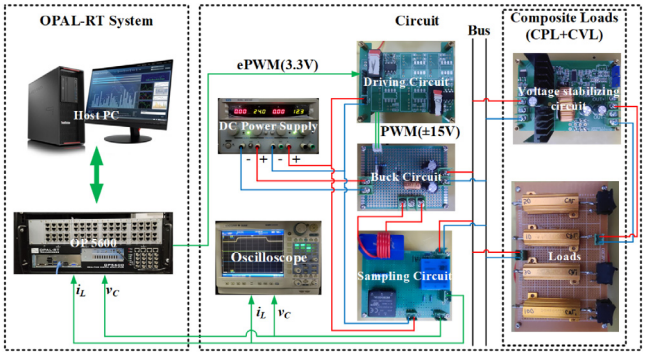

Fig. 26. The OPAL-RT based RCP experimental platform.

6. Rapid control prototype hardware experiments

In order to verify the proposed algorithm with hardware experiment, an OPAL-RT based rapid control prototype (RCP) hardware experimental platform is designed and constructed. As depicts in Fig. 26, the mentioned hardware experimental platform consists of Buck converter, drive circuit, sampling circuit, composite load, and OPAL-RT 5600 system (including a host PC). In this platform, the OPAL-RT generates and sends the PWM signal to Buck circuit through driving circuit which can increase the voltage level of the PWM signal from 3.3 V to 15 V so that the IGBT can be driven by the improved signal. Meanwhile, the output signals are sent to OPAL-RT systems through sampling circuit, then these signals will be used in the calculation by proposed method and the next PWM signal will be send to the driving circuit.

Based on this RCP hardware experiment platform, the verification of proposed method is conducted during the variation of input voltage, CIL and CPL. Fig. 27 shows the experimental result of the proposed method during the change of the input voltage which rise from 24 V to 28 V and then back to its rated value at 24 V again. As can be seen, the output voltage of the proposed controller has been fixed at its rated value of 18 V, indicating it is robust enough under the variation of the input voltage. The verification of the proposed method during the variation of CPL is shown in Fig. 28. In this experiment, the CPL decrease from 13.3 W to 10 W and recover back to its rated value at 13.3 W again. In this procedure, the output voltage is fixed at 18 V and no obvious static error can be observed. Fig. 29 shows the experimental result of the proposed controller during the variation of CIL. In this experiment, the resistance of the CIL first rise from 33.3 Ω to 50 Ω and then recover to 33.3 Ω again. As can be

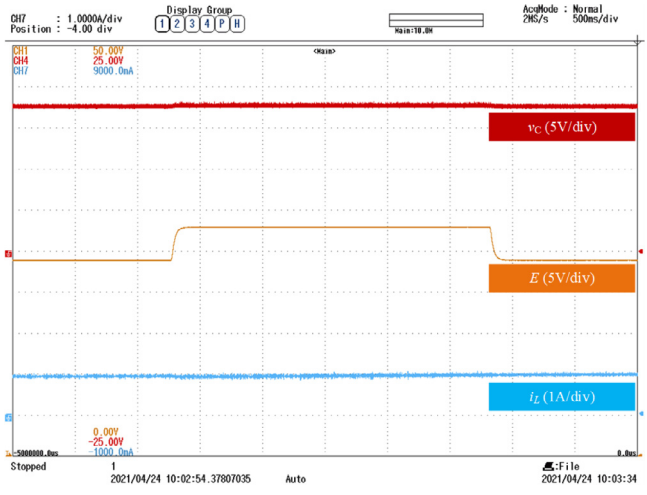

Fig. 27. The RCP experimental result of proposed controller during the input voltage change.

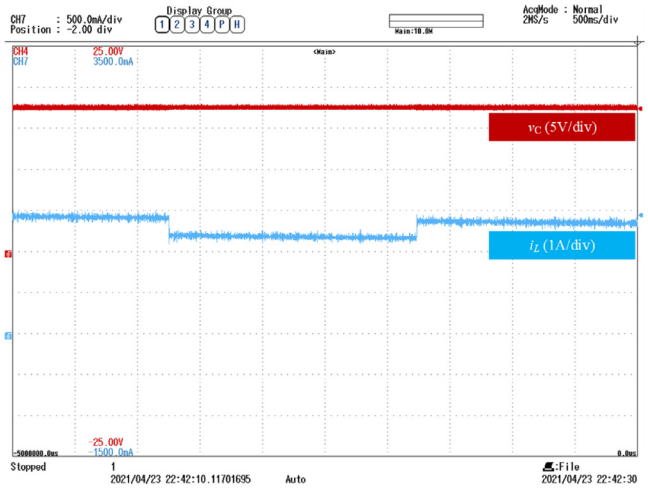

Fig. 28. The RCP experimental result of proposed controller during the CPL change.

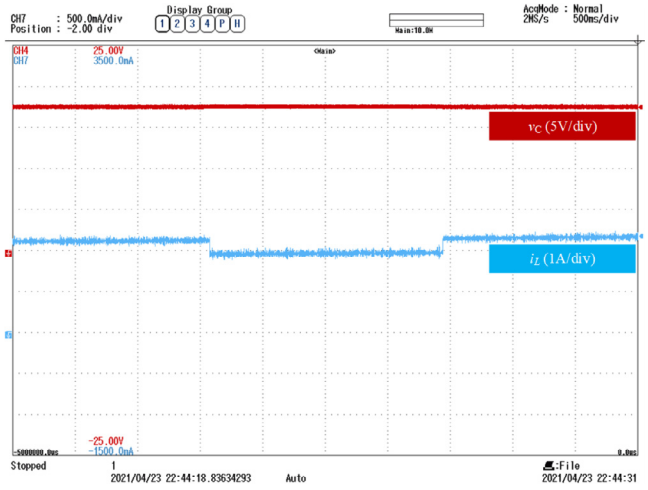

Fig. 29. The RCP experimental result of proposed controller during the CIL change.

seen from Fig. 29, the proposed method maintains the robust operation of the system, no static error is found in its output voltage, and the inductor varies according to the power consumed by the load. Thus, it can be proved that the proposed control algorithm is robust enough to grantee the stable and static error free operation of the system under the disturbance and uncertainty.

7. Conclusion

In this paper, the instability problem caused by the CPL and other disturbances or uncertainty in the buck converter system have been addressed. Based on the PBC and MPC technology, a composite controller is proposed and utilized to mitigates the instability problems mention above. Moreover, a HODO is design and set in parallel with that controller to compensate the static error caused by the disturbance and uncertainty. According to the mixed potential based large signal stability analysis, the proposed method can guarantee the large signal stability of the proposed system. In order to verify the performance of the proposed controller, MATLAB simulations, HIL experiments and RCP experiments are conducted for the proposed method, while comparative simulations and HIL experiments are conducted towards other nonlinear controller to investigates the dynamic performance

of the proposed controller. According to their results, the proposed algorithm has a good robustness and dynamic performance towards the disturbance and uncertainty.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

References

[1] Xinfa Yang, Jian Su, Zhipeng Lu, Haitao Liu, Rui Li. Overview on micro-grid technology. Proc CSEE 2014;34(1):57–70.

[2] Xialin Li, Li Guo, Chengshan Wnag, Yunwei Li. Key technologies of DC microgrids: An overview. Proc CSEE 2016;36(1):2–17.

[3] Katiraei Farid, Iravani Reza, Hatziargyriou Nikos, Dimeas Aris. Microgrids management. IEEE Power Energy Mag 2008;6(3):54–65.

[4] Guerrero Josep M, Tan Don FD. Guest editorial special issue on structured dc microgrids. IEEE J Emerg Sel Top Power Electron 2017;5(3):925–7.

[5] Dragičević Tomislav, Lu Xiaonan, Vasquez Juan C, Guerrero Josep M. DC microgrids—Part I: A review of control strategies and stabilization techniques. IEEE Trans Power Electron 2016;31(7):4876–91.

[6] Dragičević Tomislav, Lu Xiaonan, Vasquez Juan C, Guerrero Josep M. DC microgrids—Part II: A review of power architectures, applications, and standardization issues. IEEE Trans Power Electron 2015;31(5):3528–49.

[7] Singh Suresh, Gautam Aditya R, Fulwani Deepak. Constant power loads and their effects in DC distributed power systems: A review. Renew Sustain Energy Rev 2017;72:407–21.

[8] Emadi Ali, Khaligh Alireza, Rivetta Claudio H, Williamson Geoffrey A. Constant power loads and negative impedance instability in automotive systems: definition, modeling, stability, and control of power electronic converters and motor drives. IEEE Trans Veh Tecnol 2006;55(4):1112–25.

[9] Kwasinski Alexis, Onwuchekwa Chimaobi N. Dynamic behavior and stabilization of DC microgrids with instantaneous constant-power loads. IEEE Trans Power Electron 2011;26(3):822–34.

[10] Riccobon Antonino, Santi Enrico. Comprehensive review of stability criteria for DC power distribution systems. IEEE Trans Ind Appl 2014;50(5):3525–35.

[11] Lu Xiaonan, Sun Kai, Guerrero Josep M, Vasquez Juan C, Huang Lipei, Wang Jianhui. Stability enhancement based on virtual impedance for DC microgrids with constant power loads. IEEE Trans Smart Grid 2015;6(6):2770–83.

[12] Du Weijing, Zhang Junming, Zhang Yang, Qian Zhaoming. Stability criterion for cascaded system with constant power load. IEEE Trans Power Electron 2012;28(4):1843–51.

[13] Onwuchekwa Chimaobi N, Kwasinski Alexis. Analysis of boundary control for buck converters with instantaneous constant-power loads. IEEE Trans Power Electron 2010;25(8):2018–32.

[14] Zhao Yue, Qiao Wei, Ha Daihyun. A sliding-mode duty-ratio controller for DC/DC buck converters with constant power loads. IEEE Trans Ind Appl 2013;50(2):1448–58.

[15] Kondratiev Igor, Santi Enrico, Dougal Roger A, Veselov Gennady. Synergetic control for DC-DC buck converters with constant power load. In: IEEE 35th annual power electronics specialists conference. 2004.

[16] Li Shihua, Yang Jun, Chen Wenhua, Chen Xisong. Disturbance observer-based control: methods and applications. Boca Raton. Florida: CRC Press; 2014.

[17] Xu Qianwen, Zhang Chuanlin, Wen Changyun, Wang Peng. A novel composite nonlinear controller for stabilization of constant power load in DC microgrid. IEEE Trans Smart Grid 2019;10(1):3053.

[18] Kardan Mohammad A, Asemani Mohammad H, Khayatian Alireza, Vafamand Navid, Khooban Mohammad H, Dragičević Tomislav, Blaajerg Frede. Improved stabilization of nonlinear dc microgrids: Cubature Kalman filter approach. IEEE Trans Ind Appl 2018;54(5):5104–12.

[19] Hassan Mustafa A, Li Erping, Li Xue, Li Tianhang, Duan Chenyang, Chi Song. Adaptive passivity-based control of DC–DC buck power converter with constant power load in dc microgrid systems. IEEE J Emerg Sel Top Power Electron 2019;7(3):2029–40.

[20] Vazquez Sergio, Rodriguez Jose, Rivera Marco, Franquelo Leopoldo G, Norambuena Margarita. Model predictive control for power converters and drives: Advances and trends. IEEE Trans Ind Electron 2017;64(2):935–7.

[21] Cheng Long, Acuna Pablo, Aguilera Ricardo P, Jiang Jiuchun, Wei Shaoyuan, Fletcher John E, Lu Dylan DC. Model predictive control for DC–DC boost converters with reduced-prediction horizon and constant switching frequency. IEEE Trans Power Electron 2018;33(10):9064–75.

[22] Po Li, Ruiyu Li, Tianying Shao, Jingrui Zhang, Zheng Fang. Composite adaptive model predictive control for DC–DC boost converters. IET Power Electron 2018;11(10):1706–17.

[23] Andrés Oswaldo, Flores Antonio, Martinez Omar FR, Mayo-Maldonado Jonathan. Nonlinear model predictive stabilization of DC–DC boost converters with constant power loads. IEEE J Emerg Sel Top Power Electron 2020;9(1):822–30.

[24] Karami Zeinab, Shafiee Qobad, Khayat Yousef, Yaribeygi Meysam, Dragičević Tomislav, Bevrani Hassan. Decentralized model predictive control of DC microgrids with constant power load. IEEE J Emerg Sel Top Power Electron 2021;9(1):451–60.

[25] Yousefizadeh Shirin, Bendtsen Jan D, Vafamand Navid, Khooban Mohammad H, Dragičević Tomislav, Blaabjerg Frede. EKF-based predictive stabilization of shipboard DC microgrids with uncertain time-varying load. IEEE J Emerg Sel Top Power Electron 2019;7(2):901–9.

[26] Xu Qianwen, Yan Yunda, Zhang Chuanlin, Dragicevic Tomislav, Blaabjerg Frede. An offset-free composite model predictive control strategy for DC/DC buck converter feeding constant power loads. IEEE Trans Power Electron 2020;35(5):5331–42.
[27] Levant Arie. Higher-order sliding modes, differentiation and output-feedback control. Internat J Control 2003;76(9–10):924–41.
[28] Shtessel Yuri, Edwards Christopher, Fridman Leonid, Levant Arie. Sliding mode control and observation. New York: Springer; 2014.
[29] Ortega Romeo, Loría Antonio, Nicklasson Per J, Ramirez Hebertt S. Passivitybased control of Euler–Lagrange systems: Mechanical, electrical and electromechanical applications. Communications and control engineering, London: Springer; 1998.
[30] Chen Jingquan, Prodic Aleksandar, Erickson Robert W, Maksimovic Dragan. Predictive digital current programmed control. IEEE Trans Power Electron 2003;18(1):411–9.
[31] Qiu Ying, Liu Helen, Chen Xiyou. Digital average current-mode control of PWM DC–DC converters without current sensors. IEEE Trans Ind Electron 2010;57(5):1670–7.
[32] Kim Kyung-Soo, Rew Keun-Ho, Kim Soohyun. Disturbance observer for estimating higher order disturbances in time series expansion. IEEE Trans Automat Control 2010;55(8):1905–11.
[33] Brayton Robert K, Moser Jürgen K. A theory of nonlinear networks. I. Quart Appl Math 1964;22(1):1–33.
[34] Brayton Robert K, Moser Jürgen K. A theory of nonlinear networks. II. Quart Appl Math 1964;22(2):81–104.
[35] Jiang Jianbo, Liu Fei, Pan Shangzhi, Zha Xiaoming, Liu Wenjun, Chen Chao, Hao Lidong. A conservatism-free large signal stability analysis method for DC microgrid based on mixed potential theory. IEEE Trans Power Electron 2019;34(11):11342–51.