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Published in:
Journal of Modern Power Systems and Clean Energy

DOI (link to publication from Publisher):
10.35833/MPCE.2020.000876

Publication date:
2021

Document Version
Publisher's PDF, also known as Version of record

Analysis and Control of Modular Multi-terminal DC Power Flow Controller with Fault Current Limiting Function

Qianming Xu, Xinyu Huang, Xu Chu, Mingshen Li, Zhikang Shuai, Chunming Tu, and Josep M. Guerrero

***Abstract*—In order to overcome the problems of power flow control and fault current limiting in multi-terminal high voltage direct current (MTDC) grids, this paper proposes a modular multi-terminal DC power flow controller (MM-DCPFC) with fault current limiting function. The topology structure, operation principle, and equivalent circuit of MM-DCPFC are introduced, and such a structure has the advantages of modularity and scalability. The power balance mechanism is studied and a hierarchical power balance control strategy is proposed. The results show that MM-DCPFC can achieve internal power exchange, which avoids the use of external power supply. The fault characteristics of MM-DCPFC are analyzed, fault current limiting and self-protection methods are proposed, and the factors affecting the current limiting capability are studied. The simulation models are established in PLECS, and the simulation results verify the effectiveness of MM-DCPFC in power flow control, fault current limiting, and scalability. In addition, a prototype is developed to validate the function and control method of MM-DCPFC.**

***Index Terms*—Fault current limiting, multi-terminal high voltage direct current (MTDC) grid, power balance, DC power flow controller.**

I. Introduction

IT is beneficial for solving the problem of energy shortage by developing renewable energy vigorously [1], [2]. Multi-terminal high voltage direct current (MTDC) grid, which is highly reliable and stable relative to conventional AC grid, is one of the most effective technologies to solve the issues of grid integration, transmission, and absorption of renewable energy [3], [4]. However, there are still problems in MTDC system such as power flow regulation and fault current limitation, which need to be further studied.

In complex MTDC grids such as the meshed DC grid, insufficient degrees of freedom of power flow control will lead to line overloading and increased load loss [5]. The utilization of DC power flow controllers (DCPFCs) can address this problem and improve the power flow control capacity of MTDC grids [6], [7]. The principle of DCPFCs can be divided into two categories: changing the resistance or voltage of the line [8], [9], where the variable voltage type DCPFC can be divided into three categories: DC transformers, series adjustable voltage source, and interline DC power flow controller (IDCPFC). IDCPFC, as a new configuration, can be used to distribute power flow between two or more lines. Since the power exchange is completed internally without external power supply, IDCPFC has great advantages over the other two DCPFCs.

A dual H-bridge IDCPFC is proposed in [10], which has the advantages of simple structure, low cost, and easy control, but it will introduce large ripples to the line current. The IDCPFC in [11] connects a capacitor in series on each of the two lines, and realizes power exchange through an inductor or a DC/DC converter, which improves the line current ripple problem. The topology in [11] is further improved in [12], which can be applied to the condition of current reversal. The output voltage levels of IDCPFCs proposed in [10]-[12] are limited because they are all single-module structures. The multi-module IDCPFC proposed in [13] and [14] is composed of three-phase converters and an AC transformer, which is large in size and high in cost. The cascaded form of dual H-bridge topology is proposed in [15], in which high-voltage switches are added to realize the isolation of the capacitor voltage. In [16], a ring type IDCPFC is proposed, which has better redundancy and flexibility.

Another major challenge hindering the development of MTDC grids is fault protection [17]. As a series equipment, the damage of IDCPFC under fault conditions will lead to current flow interruption and even endanger the whole DC system [18], [19]. However, IDCPFCs in [10]-[16] only focus on the steady-state operation principle, and cannot deal with DC faults. Therefore, it is necessary to study the fault operation characteristic and protection mechanism of DCPFC. In addition, due to the rapid rise of fault current and the limited response time of DC circuit breakers (DCCBs), it is

Manuscript received: December 17, 2020; accepted: June 10, 2021. Date of CrossCheck: June 10, 2021. Date of online publication: September 2, 2021.

This work was supported in part by National Key R&D Program of China (No. 2018YFB0904600) and National Natural Science Foundation of China (No. 51807053).

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DOI: 10.35833/MPCE.2020.000876

difficult to interrupt the fault current. Hence, fault current limitation is one of the key points of DC fault research. The basic principle of DCPFC is to change the line impedance or voltage, which is similar to the principle of current limiter. If this impedance or voltage characteristic can be used under fault conditions, DCPFC can limit the fault current, which is beneficial to reduce the interruption current of DCCBs, so as to reduce the cost.

This paper proposes a modular multi-terminal DC power flow controller (MM-DCPFC), which can realize the free regulation of the current between multiple lines and perform a current limiting function when a short-circuit fault occurs in the DC system. The main contributions are as follows. ① The modular structure offers strong scalability. MM-DCPFC can increase the power flow regulation range by expanding the number of sub-modules (SMs) and realize the power flow control between multiple lines by expanding the number of arms without installing multiple DCPFCs, which is more economical. ② Since MM-DCPFC achieves its power balance through a hierarchical control strategy, it does not need external power supply, nor does it need transformers, inductors, and other magnetic components to complete power exchange. Therefore, it is of small size, low cost, and high efficiency. ③ The fault current limiting is realized by the original topology without increasing the complexity of DCPFC structure, which can reduce the interruption current of the DCCB. After limiting the fault current, the bypass protection strategy is used to prevent capacitor overvoltage.

The rest of this paper is organized as follows. In Section II, the operation principle is analyzed. In Section III, the hierarchical power balance mechanism is studied, including the overall power balance and internal power balance. Then, the control strategy of power flow distribution and fault current limiting is presented in Section IV. Subsequently, the above analysis is verified by the simulation data and experimental results in Section V. In Section VI, MM-DCFPC is compared with several typical DCPFCs. Finally, conclusion is made in Section VII to summarize the findings and results.

II. Operation Principle

A. Topology of MM-DCPFC

The MM-DCPFC with m terminals is shown in Fig. 1(a), including m arms (A1, A2, …, Am) with the same structure. It can be installed at one of the terminals (p_1, p_2, or p_3) in the DC grid to redistribute the terminal current I_1 among $m-1$ branches ($I_{l,1}, I_{l,2}, \ldots, I_{l,m-1}$) to make them meet expectations. The topology of the arm is shown in Fig. 1(b). Ignoring the small arm resistance, each arm is composed of N cascaded SMs and the arm inductance L_e. The SM contains a full-bridge module and two thyristors as shown in Fig. 1(c). Since each full-bridge can output U_C, $-U_C$, and 0 voltage levels, the peak value of the voltage output by N cascaded SMs is $\pm NU_C$. Each arm can be equivalent to a controllable voltage source, and its output voltage u_x (x = A1, A2, …, Am) can be controlled by adjusting the coefficient n_x:

$$u_x = n_x N U_C \quad -1 \le n_x \le 1 \tag{1}$$

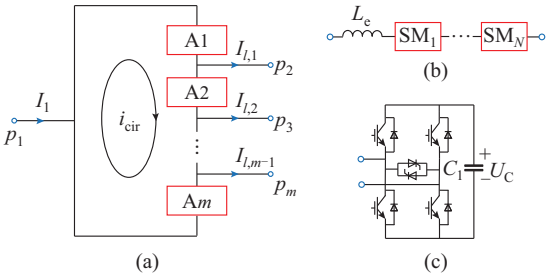

Fig. 1. Topology of MM-DCPFC. (a) Structure of m-terminal MM-DCPFC. (b) Structure of arm. (c) Structure of SM.

In order to meet the needs of power flow control under normal conditions and current limitation under fault conditions, MM-DCPCF has two operation modes: power flow control mode and fault current limiting mode. The thyristors in SMs will only be triggered in fault current limiting mode.

B. Power Flow Control Mode

In order to facilitate the analysis, a simple three-terminal MM-DCPFC is taken as an example to illustrate its operation principle. In the three-terminal DC grid shown in Fig. 2(a), to regulate the current I_{12} and I_{13}, MM-DCPFC is installed at terminal 1, where U_1, U_2, and U_3 are the terminal voltages; I_1, I_2, and I_3 are the terminal currents; I_{12}, I_{13}, and I_{23} are the line currents; and u_{A1}, u_{A2}, u_{A3} and i_{A1}, i_{A2}, i_{A3} are the arm voltages and arm currents of A1, A2, and A3, respectively. The equivalent circuit of MM-DCPFC in power flow control mode is shown in Fig. 2(b), where the line impedance $Z_y = R_y + \mathrm{j}L_y$ (y = 12, 13, 23) is mainly determined by the length of the lines.

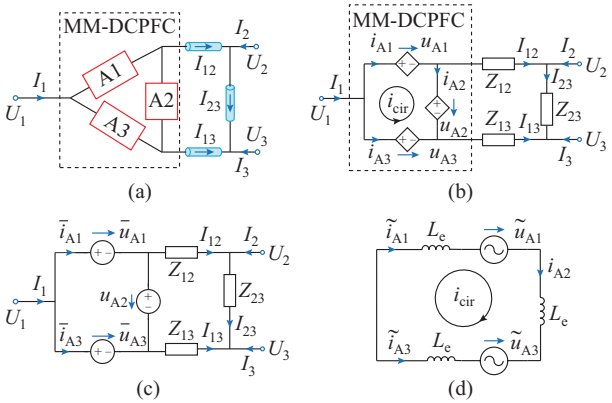

Fig. 2. Three-terminal MM-DCPFC. (a) Three-terminal DC grid with MM-DCPFC. (b) Equivalent model of MM-DCPFC in power flow control mode. (c) DC loop equivalent circuit. (d) AC loop equivalent circuit.

In order to ensure the normal operation of MM-DCPFC in power flow control mode, the following two functional requirements need to be met: ① insert positive and negative DC voltages into the two transmission lines to regulate the power flow; ② complete power exchange internally to ensure its own power balance. Therefore, the output voltages of A1 and A3 contain both DC and AC components, where the DC voltage component is used to realize the first function, and the AC voltage component is used to achieve the power exchange between the two arms and realize the sec-

ond function. In addition, the arm A2, which is not connected in series to any line, only outputs DC voltage and flows through AC circulating current. The equivalent circuit model can be obtained by decoupling AC and DC components in MM-DCPFC, as shown in Fig. 2(c) and (d), where $\bar{u}_{A1}$ and $\bar{u}_{A3}$ are the DC voltages of A1 and A3, respectively; $\bar{i}_{A1}$ and $\bar{i}_{A3}$ are the DC currents of A1 and A3, respectively; $\tilde{u}_{A1}$ and $\tilde{u}_{A3}$ are the AC voltages of A1 and A3, respectively; and $\tilde{i}_{A1}$ and $\tilde{i}_{A3}$ are the AC currents of A1 and A3, respectively.

According to the Kirchhoff's voltage law and Fig. 2(c), we can obtain (2), which proves that the distribution of I_1 between the two branches can be changed by adjusting the DC components of u_{A1} and u_{A3}.

$$\begin{cases} I_{12} = \dfrac{U_1 - U_2 - \bar{u}_{A1}}{R_{12}} \\ I_{13} = \dfrac{U_1 - U_3 - \bar{u}_{A3}}{R_{13}} \\ I_{23} = \dfrac{U_2 - U_3}{R_{23}} \end{cases} \tag{2}$$

According to the Kirchhoff's current law and Fig. 2(c), we can obtain (3). It can be observed from (3) that if the terminal current I_1 is fixed, only one of I_{12} and I_{13} is fully controllable. Therefore, one degree of freedom is required to adjust the current of the two branches, and there is an extra degree of freedom among the adjustable quantities $\bar{u}_{A1}$ and $\bar{u}_{A2}$ in (2) that can be used to meet the external power balance.

$$\begin{cases} I_1 = I_{12} + I_{13} \\ I_{12} = \bar{i}_{A1} \\ I_{13} = \bar{i}_{A3} \end{cases} \tag{3}$$

According to Fig. 2(d), we can obtain (4), where $X = j\omega L_e$. It can be observed from (4) that the internal circulating AC current i_{cir} can be controlled by adjusting the AC voltage components of A1 and A3.

$$\begin{cases} \tilde{i}_{A1} = i_{cir} \\ \tilde{i}_{A2} = i_{cir} \\ \tilde{i}_{A3} = -i_{cir} \\ 3Xi_{cir} = \tilde{u}_{A1} - \tilde{u}_{A3} \end{cases} \tag{4}$$

C. Fault Current Limiting Mode

A single-pole grounding fault is assumed to occur on line 12 near terminal 2. The transient characteristics, current limiting mechanism, and self-protection scheme of MM-DCPFC are analyzed. As shown in Fig. 3(a), there are two paths to inject short-circuit current to the fault point: l_{12}, and l_{13}-l_{23}. Since arms A1 and A3 are respectively connected in series in two branches, the fault current of l_{12} is limited by A1, while the fault current of the other path is suppressed by A3. The action sequence of A1 is as follows, and A3 is the same.

1) Fault current limiting stage: after MM-DCPFC receives the fault command, all insulated gate bipolar transistors (IGBTs) will be blocked immediately to make each SM in an uncontrolled rectification state. The capacitor at the DC side is charged by the fault current through freewheeling diodes, and the reverse voltage is inserted in the l_{12} to limit the fault current as shown in Fig. 3(b). Note that in Fig. 3, the dashed red line indicates the current flow path.

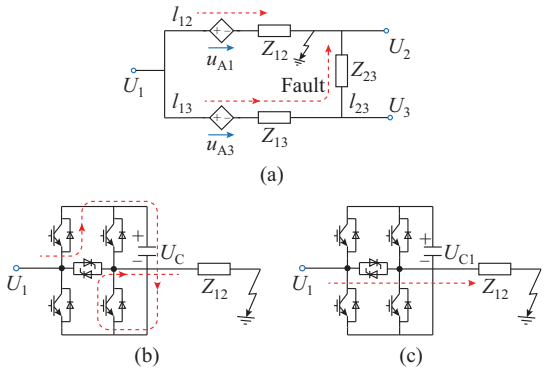

Fig. 3. Fault current limiting mode. (a) Flow path of fault current. (b) Fault current limiting stage. (c) Bypass protection stage.

2) Bypass protection stage: in order to ensure the safety of the capacitor, once the capacitor voltage reaches the upper limit, the thyristors in parallel at the output end of the SM will be forced to conduct for commutation, so as to realize the self-protection function as shown in Fig. 3(c).

Since the current limiting function fails after the capacitor is bypassed, it is the effective current limiting time of MM-DCPFC from the fault detection to the bypass protection. The transient model of this stage is established, as shown in Fig. 4, where R_f and L_f are the total equivalent resistance and inductance of the fault circuit, respectively.

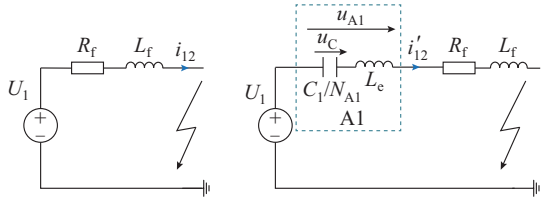

Fig. 4. Equivalent model of fault current limiting stage. (a) Equivalent model without fault current limiting. (b) Equivalent model with fault current limiting.

Figure 4(a) shows the equivalent circuit without current limiting, which satisfies:

$$-U_1 + R_f i_{12} + L_f \frac{\mathrm{d}i_{12}}{\mathrm{d}t} = 0 \tag{5}$$

If the steady-state line current is I_0, the fault current is calculated as:

$$i_{12} = \frac{U_1}{R_f}\left(1 - \mathrm{e}^{-\frac{R_f t}{L_f}}\right) + I_0 \mathrm{e}^{-\frac{R_f t}{L_f}} \tag{6}$$

The equivalent circuit with current limiting is shown in Fig. 4(b).

$$-U_1 + u_{A1} + R_f i_{12} + L_f \frac{\mathrm{d}i_{12}}{\mathrm{d}t} = 0 \tag{7}$$

$$u_{A1} = u_C + L_e \frac{C_1}{N_{A1}} \frac{\mathrm{d}^2 u_C}{\mathrm{d}t} \tag{8}$$

where C_1 is the capacitance of the SM, and since the capacitors of the N_{A1} SMs are connected in series, the capacitance becomes C_1/N_{A1}; and u_C is the capacitor voltage.

If a short-circuit fault occurs at t_0 and the initial capacitor voltage is U_0, u_C at t_1 can be expressed as:

$$u_C = \begin{cases} U_0 + \dfrac{N_{A1}}{C_1}\displaystyle\int_{t_0}^{t_1} i'_{12}(t)\mathrm{d}t & u_C \le U_{lim} \\ U_{lim} & u_C > U_{lim} \end{cases} \tag{9}$$

where U_{lim} is the upper limit of capacitor voltage.

The fault current i'_{12} is calculated from (7):

$$i'_{12} = \frac{U_1 - u_{A1}}{R_f}\left(1 - \mathrm{e}^{-\frac{R_f t}{L_f}}\right) + I_0 \mathrm{e}^{-\frac{R_f t}{L_f}} \tag{10}$$

It can be observed from (6) and (10) that MM-DCPFC can reduce the line voltage from U_1 to $U_1 - u_{Al}$ by inserting a reverse voltage, and the current limiting capacity can be obtained by:

$$\frac{I_L - I'_L}{I_L} = \frac{\dfrac{u_{A1}(\Delta t)}{R_f}\left(1 - \mathrm{e}^{-\frac{R_f \Delta t}{L_f}}\right)}{\dfrac{U_1}{R_f}\left(1 - \mathrm{e}^{-\frac{R_f \Delta t}{L_f}}\right) + I_0 \mathrm{e}^{-\frac{R_f \Delta t}{L_f}}} \tag{11}$$

where Δt is the time delay from fault occurrence to interruption; I_L and I'_L are the fault currents at Δt in the DC system without and with current-limiting capability, respectively; and $u_{Al}(\Delta t)$ is the arm voltage of A1 at Δt.

Due to the small arm inductance in (8), it can be considered that all the current limiting capabilities are provided by the capacitor voltage. Moreover, compared with the fault current component, the steady-state component I_0 is very small and can be ignored. Therefore, when u_{A1} and u_C are regarded as equal and I_0 is not considered, the current limiting capacity in (10) can be approximately expressed as:

$$\frac{I_L - I'_L}{I_L} = \frac{u_C(\Delta t)}{U_1} \tag{12}$$

where $u_C(\Delta t)$ is the capacitor voltage at Δt.

Two factors affecting the current limiting capacity can be concluded: the capacitance value affects the rise rate of fault current, and the upper limit of capacitor voltage affects the current limiting time. The smaller the capacitance is, the faster the capacitor voltage rises in finite time, and the larger $u_C(\Delta t)$ is. The larger the capacitor voltage limit is, the longer the effective current limiting time is. Therefore, the current limiting capacity of MM-DCPFC can be improved by appropriately reducing the capacitance and increasing the capacitor voltage limit. In addition, the most effective method is to increase the number of SMs in the arm, but the cost will increase. It is necessary to consider the cost and current limiting ability comprehensively and choose a better scheme in the actual application.

When U_{lim} of the capacitor is determined, the maximum possible current limiting capacity is also determined, as shown in (13). The premise of reaching this maximum is that the capacitor voltage of SMs just reaches U_{lim} at Δt. The capacitance value meeting this requirement can be calculated as follows. According to (6) - (8), the analytical expression $u_C(t)$ of u_C relative to t can be obtained. When the interruption time Δt of DCCB is known, $u_C(\Delta t) = U_{lim}$ can be solved to obtain the capacitance value with the maximum current limiting capacity.

$$\left(\frac{I_L - I'_L}{I_L}\right)_{max} = \frac{NU_{lim}}{U_1} \tag{13}$$

When a single-pole grounding fault occurs, there is a case that does not cause a large fault current, i.e., the DC system is grounded through a large impedance, which can effectively limit the fault current. At this time, the fault current limiting stage can be skipped, and the MM-DCPFC is directly bypassed. In addition to line-to-ground faults, a line-to-line fault is a rare event, but the impact is catastrophic and also needs to be considered. When the DC system is in bipolar mode, both the positive and negative poles need to be installed with MM-DCPFC, and can be used to limit the fault current. Therefore, although the line-to-line fault is more serious, the current limiting capacity of MM-DCPFC is also greater.

III. Hierarchical Power Balance Mechanism

The power of A1 and A3 is shown in (14). The external and internal power balance is achieved by the following two power exchange mechanisms: ① the overall net power balance is realized by exchanging DC power between arms (A1 and A3) and the DC system; ② the internal power balance is realized by transferring average AC power between A1 and A3.

$$\begin{cases} P_{A1} = \bar{P}_{A1} + \tilde{P}_{A1} \\ P_{A3} = \bar{P}_{A3} + \tilde{P}_{A3} \end{cases} \tag{14}$$

where $\bar{P}_{A1}$ and $\bar{P}_{A3}$ are the DC power of A1 and A3, respectively; and $\tilde{P}_{A1}$ and $\tilde{P}_{A3}$ are the average AC power of A1 and A3, respectively.

A. External Power Balance

MM-DCPFC has no power loss under ideal conditions, i.e., the DC power exchanged between A1 and DC system is balanced with that exchanged between A3 and DC system:

$$\bar{P}_{A1} + \bar{P}_{A3} = 0 \tag{15}$$

According to (15), we can obtain:

$$\bar{u}_{A1} I_{12} = -\bar{u}_{A3} I_{13} \tag{16}$$

Although MM-DCPFC has no loss under ideal conditions, in actual operation, when affected by power devices and equipment losses, MM-DCPFC needs to properly absorb the power from the outside to achieve its overall power balance:

$$\bar{P}_{A1} + \bar{P}_{A3} = P_{loss} \tag{17}$$

Since DC currents are regulated quantities, the overall power balance can only be realized by adjusting the DC voltage of arms. When Δu_{dc} is added to $\bar{u}_{A1}$ and $\bar{u}_{A2}$ to compensate the internal loss, the compensated power loss is obtained as:

$$P_{\text{loss}} = \Delta u_{\text{dc}} (I_{12} + I_{13}) = \Delta u_{\text{dc}} I_1 \tag{18}$$

For three-terminal MM-DCPFC, $\bar{u}_{\text{A1}}$ and $\bar{u}_{\text{A2}}$ provide two degrees of freedom in order to satisfy (2) and (16), i.e., power flow control and external power balance. It can be inferred that for *m*-terminal MM-DCPFC, the DC voltage component of arms should provide $m-1$ degrees of freedom to realize power flow control and overall power balance, and the extra arm such as A2 in three-terminal MM-DCPFC exists as a balancing arm, and its main functions are providing a pathway for circulating AC current i_{cir}. The DC voltage of A2 can also be used to compensate the DC voltage difference between A1 and A3 to eliminate the circulating DC current inside the MM-DCPFC. Therefore, u_{A2} needs to satisfy:

$$\bar{u}_{\text{A1}} + u_{\text{A2}} - \bar{u}_{\text{A3}} = 0 \tag{19}$$

It can be observed from the above analysis that A2 neither needs to output AC voltage nor limits the fault current. Therefore, the number of SMs of A2 can be reduced, and even can be replaced by a non-polar capacitor.

B. Internal Power Balance

In order to ensure the internal power balance of MM-DCPFC, the power of the A1 and A3 needs to meet: ① the DC power of one arm is balanced with its own average AC power; ② the average AC power of one arm is balanced with that of the other, that is:

$$\begin{cases} \bar{P}_{\text{A1}} = -\tilde{P}_{\text{A1}} \\ \bar{P}_{\text{A3}} = -\tilde{P}_{\text{A3}} \\ \tilde{P}_{\text{A1}} = -\tilde{P}_{\text{A3}} \end{cases} \tag{20}$$

The two arms transfer the power in the form of average AC power, so it is necessary to modulate the AC voltage and circulating AC current to meet the needs of internal power balance. The AC voltage components of A1 and A3 can be decomposed into u_x and u_y:

$$\begin{cases} \tilde{u}_{\text{A1}} = u_x + u_y \\ \tilde{u}_{\text{A3}} = u_x - u_y \end{cases} \tag{21}$$

where u_x is used to generate average AC power and has the same phase as i_{cir}; and u_y is 90° ahead of the phase of i_{cir} to compensate reactive power and generate AC circulating current.

Equation (22) can be derived from (16) and (20).

$$\begin{cases} \dfrac{1}{2} \hat{u}_x \hat{i}_{\text{cir}} = \bar{u}_{\text{A1}} \bar{i}_{\text{A1}} \\ \bar{u}_{\text{A1}} \bar{i}_{\text{A1}} = -\bar{u}_{\text{A3}} \bar{i}_{\text{A3}} \end{cases} \tag{22}$$

where $\hat{u}_x$ and $\hat{i}_{\text{cir}}$ are the amplitudes of u_x and i_{cir}, respectively.

One degree of freedom is needed to satisfy (22) and realize internal power balance, and an extra degree of freedom among the two adjustable variables $\hat{u}_x$ and $\hat{i}_{\text{cir}}$ can be used for optimization. Since A1 and A3 will inevitably insert AC voltage in the lines and cause current ripple, $\hat{u}_x$ can be reduced as much as possible, which needs to increase $\hat{i}_{\text{cir}}$, and then increase a part of loss to reduce the ripple. In addition to the optimization inside the device, series inductors can also be used to reduce the current ripple.

Equation (20) is based on the ideal condition that A2 has no loss. Under actual conditions, in order to maintain the power balance of A2, an AC voltage Δu_{ac} is subtracted and added to the voltage of A1 and A3, respectively, and the compensated loss of A2 is as follows:

$$P_{\text{loss}}^{\text{A2}} = \Delta \hat{u}_{\text{ac}} \hat{i}_{\text{cir}} \tag{23}$$

where $\Delta \hat{u}_{\text{ac}}$ is the amplitude of Δu_{ac}.

Based on the above analysis, the arm voltages u_{A1}, u_{A2}, u_{A3} and arm currents i_{A1}, i_{A2}, i_{A3} can be expressed as:

$$\begin{cases} u_{\text{A1}} = \bar{u}_{\text{A1}} + \tilde{u}_{\text{A1}} = U_1 - U_2 - I_{12} R_{12} + \Delta u_{\text{dc}} + u_x + u_y - \Delta u_{\text{ac}} \\ u_{\text{A2}} = \bar{u}_{\text{A3}} - \bar{u}_{\text{A1}} \\ u_{\text{A3}} = \bar{u}_{\text{A3}} + \tilde{u}_{\text{A3}} = U_1 - U_3 - I_{13} R_{13} + \Delta u_{\text{dc}} + u_x - u_y + \Delta u_{\text{ac}} \end{cases} \tag{24}$$

$$\begin{cases} i_{\text{A1}} = \bar{i}_{\text{A1}} + \tilde{i}_{\text{A1}} = I_{12} + i_{\text{cir}} \\ i_{\text{A2}} = i_{\text{cir}} \\ i_{\text{A3}} = \bar{i}_{\text{A3}} + \tilde{i}_{\text{A3}} = I_{13} - i_{\text{cir}} \end{cases} \tag{25}$$

The electrical stress is also a major concern in actual design, which will affect the cost and volume of hardware. Therefore, the voltage and current stresses for key power electronic devices are listed in Table I, where I_{peak} is the peak value of fault current.

TABLE I
VOLTAGE AND CURRENT STRESSES OF KEY POWER ELECTRONIC DEVICES

Device	Current stress	Voltage stress
IGBT of A1 and A3	$\sqrt{I_1^2 + \hat{i}_{\text{cir}}^2/2}$	U_{lim}
IGBT of A2	$\hat{i}_{\text{cir}}/\sqrt{2}$	U_{lim}
Diode	I_{peak}	$U_{\text{lim}}/2$
Thyristor	I_{peak}	U_{lim}

IV. CONTROL STRATEGY OF POWER FLOW DISTRIBUTION AND FAULT CURRENT LIMITING

The control system of MM-DCPFC is divided into power flow control mode and fault current limiting mode. In the power flow control mode, there are mainly current distribution control and power balance control, as shown in Fig. 5(a), where I_{12}^{ref} and $i_{\text{cir}}^{\text{ref}}$ are the reference values of line current I_{12} and circulating AC current i_{cir}, respectively; $U_{\text{C}}^{\text{A1}}(i)$, $U_{\text{C}}^{\text{A2}}(j)$, and $U_{\text{C}}^{\text{A3}}(k)$ are the SM capacitor voltages of A1, A2, and A3, respectively; $U_{\text{C,ref}}^{\text{A1}}$, $U_{\text{C,ref}}^{\text{A2}}$, and $U_{\text{C,ref}}^{\text{A3}}$ are the capacitor voltage reference values of A1, A2, and A3, respectively; $\Delta u_{\text{C}}^{\text{A1}}(i)$, $\Delta u_{\text{C}}^{\text{A2}}(j)$, and $\Delta u_{\text{C}}^{\text{A3}}(k)$ are the modulation commands of internal capacitor voltage sharing of A1, A2, and A3, respectively; and $u_{\text{A1}}(i)$, $u_{\text{A2}}(j)$, and $u_{\text{A3}}(k)$ are voltage modulation commands of SMs of A1, A2, and A3, which are converted into switching signals by carrier-phase-shifted pulse width modulation (PWM) method [20].

A. Current Distribution Control

The current distribution control includes open-loop feedforward control and closed-loop feedback control, as shown in Fig. 5(b). According to (2), the DC component of arm voltage mainly depends on the current distribution and the length of the lines. Given the reference values of I_{12} and the terminal current I_1, the initial DC voltage values of A1 and

A3 can be calculated according to (2). In order to improve the accuracy and dynamic performances, a closed-loop feedback control is added, and the output command of PI controller is combined with the above initial value to output DC voltage command.

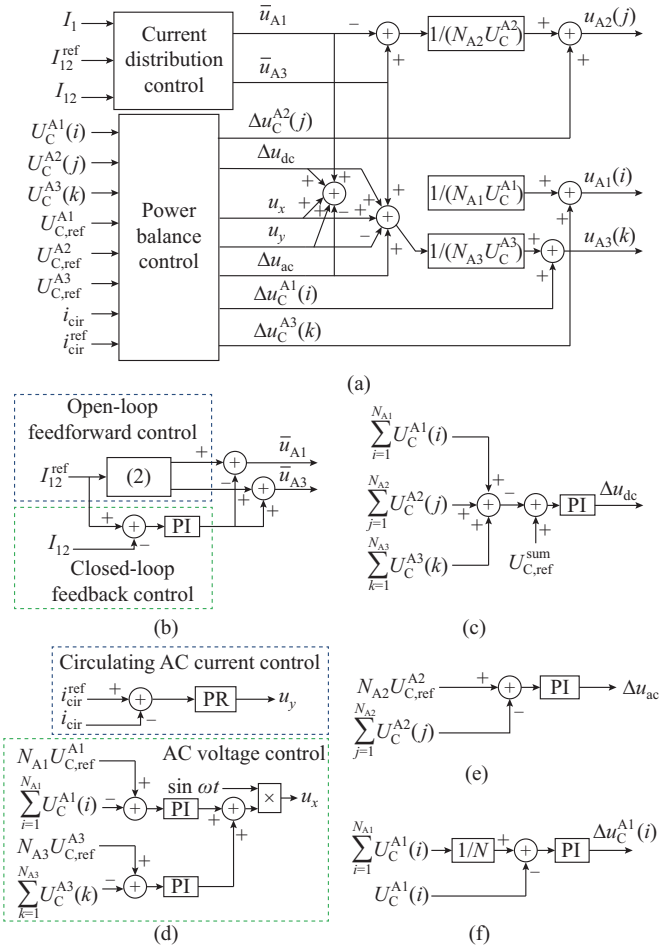

Fig. 5. Control block diagram of MM-DCPFC. (a) Overall control. (b) Current distribution control. (c) Power balance control. (d) A1 and A3 power balance control. (e) A2 power balance control. (f) SM power balance control.

B. Power Balance Control

The power balance of MM-DCPFC is controlled at three levels: overall power balance, arm power balance, and SM power balance.

Figure 5(c) shows the power balance control, where $U_{\mathrm{C,ref}}^{\mathrm{sum}}$ is the reference value of the sum of all capacitor voltages, and $U_{\mathrm{C,ref}}^{\mathrm{sum}} = U_{\mathrm{C,ref}}^{\mathrm{A1}} + U_{\mathrm{C,ref}}^{\mathrm{A2}} + U_{\mathrm{C,ref}}^{\mathrm{A3}}$. According to Section III-A, Δu_{dc} is added to the DC voltage of A1 and A3 to compensate for losses and thus ensure overall power balance.

The control block diagram of arm power balance is shown in Fig. 5(d), where PR stands for proportional-resonant. i_{cir} is modulated by adding and subtracting AC voltage u_y respectively at the voltage of A1 and A3. Given the reference value of i_{cir}, PR controller is used to generate the command u_y to make i_{cir} track the reference value. According to (22), AC voltages of the arms need to be modulated to meet the power balance requirements. PI controller is used to output the command of AC voltage amplitude of the arm, and then the sinusoidal command u_x is obtained. Furthermore, according to Section III-B, Δu_{ac} is subtracted and added to the AC voltage of A1 and A3 respectively to realize the power balance of A2, as shown in Fig. 5(e).

The above control strategy ensures the power balance of the whole MM-DCPFC and the arms. In addition, the capacitor voltage sharing control is needed to ensure the power balance of each SM. Figure 5(f) shows that the control block diagrams of A1, A2, and A3 are the same. The control strategy is as follows. The average value of all capacitor voltages in one arm is calculated. Each capacitor voltage is made to track this average value. The commands $\Delta u_{\mathrm{C}}^{\mathrm{A1}}(i)$ $(i = 1, 2, \ldots, N_{\mathrm{A1}})$ output by the PI controller cause a small change in the modulation wave of each SM to ensure the balance of the capacitor voltage.

C. Fault Current Limiting Control

Whether MM-DCPFC can limit the current in the entire fault process can be divided into the following two situations.

1) If the capacitor voltage reaches the upper limit U_{lim} before the fault is cleared, MM-DCPFC will first limit the fault current, and then it will be bypassed when $U_{\mathrm{C}} = U_{\mathrm{lim}}$, and the current limiting function will also fail. Since the DC-CB has not been activated at this time, the current will continue to rise at a large rate until the fault is cleared. The curve of short-circuit current is shown in Fig. 6(a).

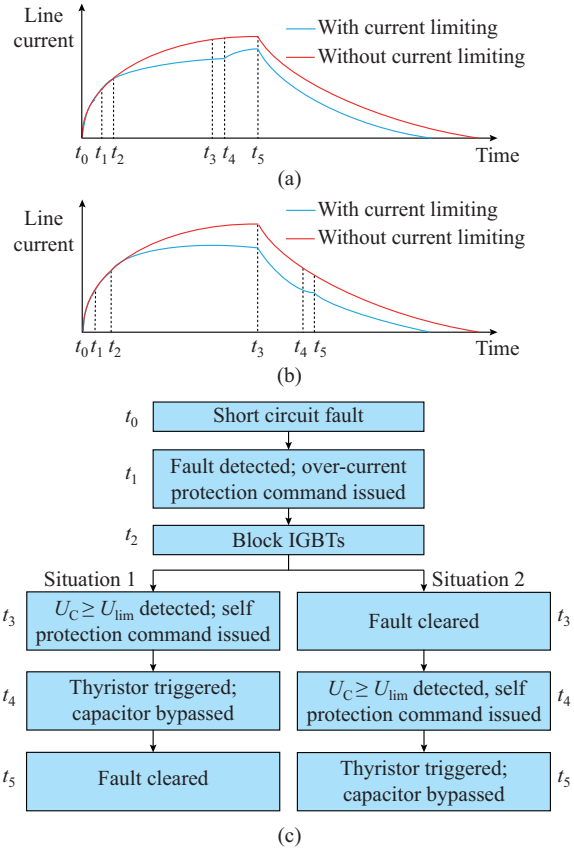

Fig. 6. Fault current limiting mode control. (a) Current curve of situation 1. (b) Current curve of situation 2. (c) Action sequence of MM-DCPFC in fault current limiting mode.

2) If the capacitor voltage does not reach U_{lim} before the fault is cleared, the current limiting function can be exerted during the entire short-circuit fault process, as shown in Fig. 6(b).

The action sequence of MM-DCPFC in fault current limiting mode can be obtained based on the above two situations, as shown in Fig. 6(c). Since the second situation is generally expected, under a certain operation condition, MM-DCPFC can limit the fault current during the entire fault process by selecting the capacitance and the upper limit of the capacitor voltage reasonably.

V. Simulation and Experimental Verification

The simulation model of three-terminal DC system with MM-DCPFC in Fig. 2(a) is built in PLECS, where terminal 1 operates in constant voltage control mode and U_1 = 200 kV, while terminal 2 and terminal 3 operate in constant power control mode and P_2 = −81 MW, P_3 = −157 MW. The main parameters of the transmission lines are shown in Table II [11], [21], and the parameters of three-terminal MM-DCPFC are shown in Table III.

TABLE II
Parameters of Transmission Lines

DC line	Distance (km)	Resistance (Ω)	Inductance (H)	Capacitance (μF)
Line 12	400	4	0.16	480
Line 13	300	3	0.12	360
Line 23	300	3	0.12	360

TABLE III
Parameters of Three-terminal MM-DCPFC

Parameter	Value
C_1	3 mF
N_{A1}	10
N_{A2}	1
N_{A3}	10
L_e	1 mH
i_{cir}^{ref}	200 A

A. Start-up and Power Flow Control

The power flow control mode of MM-DCPFC consists of two basic stages: start-up stage and normal operating stage. The control objective of the start-up stage is to charge capacitors to the rated operating voltage. Thus, only the power balance mechanism is put into operation in this stage, while the current distribution mechanism does not work, and the control method is the same as that in Section IV-B. MM-DCPFC is started at t = 0.2 s. As can be observed from Fig. 7(a), MM-DCPFC absorbs energy from the DC system during the rise of capacitor voltage, causing slight fluctuation of line current, and it will no longer affect line current when the capacitor voltage is stable.

The power flow control starts at 1 s, and the given value of I_{12} is 0.6 kA. Before starting the power flow control, the line current is I_1 = 1.20 kA, I_{12} = 0.49 kA, I_{13} = 0.71 kA. After starting the power flow control, the line current is regulated according to the given value and stabilized again. At this time, I_{12} = 0.6 kA, I_{13} = 0.6 kA, as shown in Fig. 7(a). It can be observed from Fig. 7(b) that the capacitor voltage of SMs of A1 and A3 can be stabilized at 400 V, and that of A2 can be stabilized at 900 V.

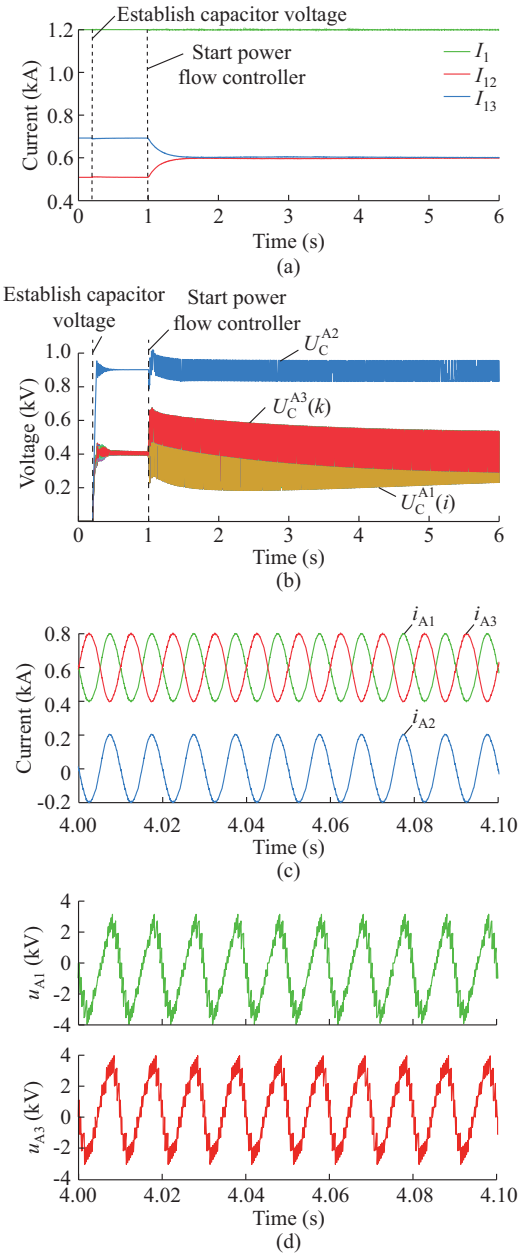

Fig. 7. Simulation waveforms of start-up and power flow control. (a) Line currents. (b) Capacitor voltages of SMs. (c) Arm currents. (d) Arm voltages.

B. Fault Current Limiting

At t = 3 s, a short-circuit fault shown in Fig. 3(a) occurs. In the absence of any current limiting measures, the line current rises rapidly, far exceeding the rated current, and continues to rise to 3.96 kA before the fault is cleared. In the system with fault current limiting capacity, the fault is detected at 0.2 ms after occurrence and cleared at 3.5 ms. At this time, I_{12} = 3.43 kA, which is reduced by 13.31% compared

with no current limiting, as shown in Fig. 8(a). It can be observed from Fig. 8(b) that the capacitor voltage in SMs rises to the set protection value (5 kV) at 5 ms after the fault occurs, and then it is bypassed. After that, in order to protect the power electronic modules, it is necessary to discharge the capacitor to a safe voltage level. Therefore, a large resistor controlled by a switch can be connected in parallel with the capacitor to consume its energy.

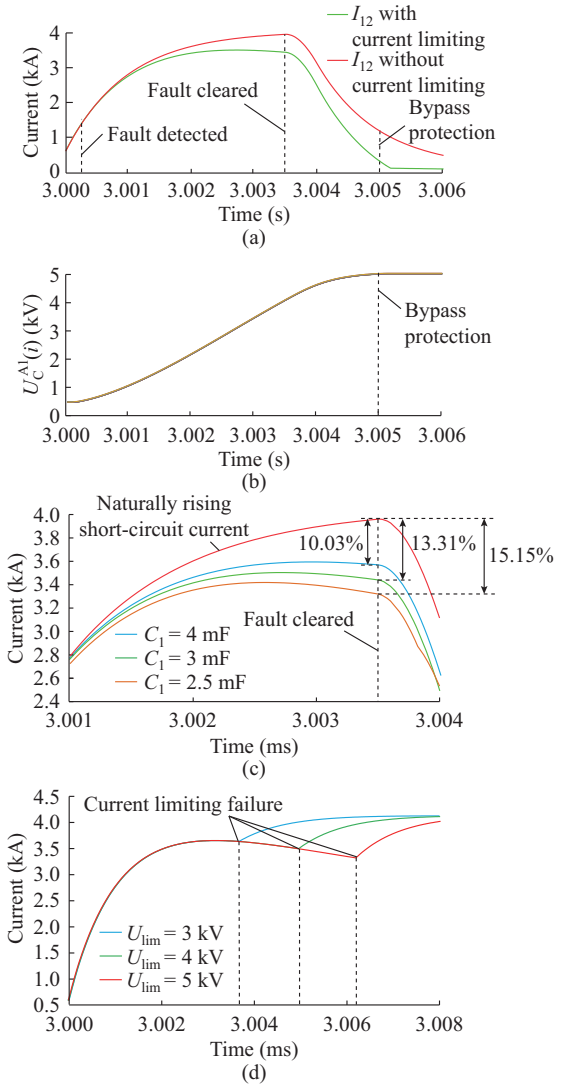

Fig. 8. Simulation waveforms of fault current limiting mode. (a) Line currents. (b) Capacitor voltages of SMs. (c) Comparison of current limiting capability with different capacitance values. (d) Comparison of effective current limiting time with different voltage limits.

In order to further study the current limiting characteristics, simulations are carried out for different capacitance values and different upper limits of capacitor voltage. When U_{lim} is set to be 5 kV, the current limiting capability corresponding to different capacitances is shown in Fig. 8(c). When the capacitance is set to be 5 mF, the effective current limit time corresponding to different U_{lim} is shown in Fig. 8 (d). The simulation results are consistent with the theoretical analysis of Section II-C.

C. Four-terminal MM-DCPFC

In order to verify the scalability of MM-DCPFC, four-terminal power flow controller is simulated. The four-terminal MM-DCPFC is composed of four arms, i.e., $m=4$ in Fig. 1, which can adjust the distribution of terminal currents in the three branches l_1, l_2, and l_3. The parameters of three branches connected to terminal 1 are shown in Table IV, and the SM capacitance and arm inductance of MM-DCPFC are the same as those in Table III. There is one SM in A2, while there are 10 SMs in A1, A3, and A4, and the simulation results are shown in the Fig. 9. The MM-DCPFC is started at $t=0.2$ s, and capacitor voltages are established. At this time, $I_{12}=0.34$ kA, $I_{12}=0.43$ kA, $I_{13}=0.43$ kA. The power flow control starts at 1 s, and the currents of lines are stable as $I_{12}=0.5$ kA, $I_{12}=0.35$ kA, $I_{13}=0.35$ kA, which is equal to the expected value as shown in Fig. 9(a). The capacitor voltages of A1, A3, and A4 can be stabilized at 500 V, while that of A2 can be stabilized at 1200 V, as shown in Fig. 9(b).

TABLE IV
LINE PARAMETERS OF FOUR-TERMINAL MM-DCPFC

DC line	Distance (km)	Resistance (Ω)	Inductance (H)	Capacitance (μF)
Line12	500	5	0.20	600
Line13	400	4	0.16	480
Line14	400	4	0.16	480

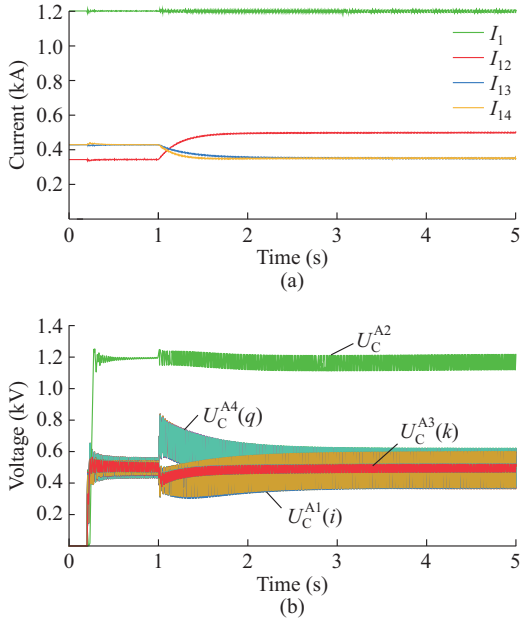

Fig. 9. Simulation waveforms of four-terminal MM-DCPFC. (a) Line currents. (b) Capacitor voltages of SMs.

D. Experimental Validation

In order to verify the function and control method of MM-DCPFC, a small-scale experimental system shown in Fig. 10 is built in the laboratory, and the parameters of DC system are: $U_1=300$ V, $P_2=-1$ kW and $P_3=-1$ kW, $R_{12}=3.6$ Ω, $R_{13}=5.4$ Ω. In the MM-DCPFC prototype, there is one SM in A1 and A3, and A2 is replaced by capacitance as described in

Section III-A, and the amplitude of AC circulating current is set to be 3 A.

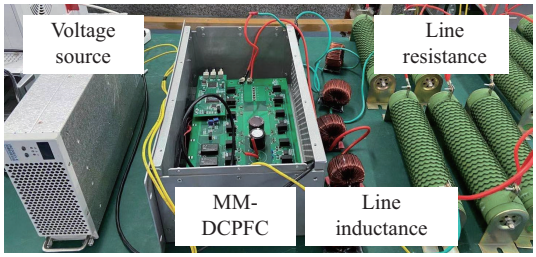

Fig. 10. Picture of experimental system.

The reference values of I_{12} and the capacitor voltage are 3 A and 30 V, respectively. In the initial state, MM-DCPFC is bypassed and the line currents are naturally distributed. Since the capacitor voltage is small, the capacitor voltage establishment and power flow regulation are carried out simultaneously after MM-DCPFC is put into operation. When the system reaches to be stable, the line current and the capacitor voltage are equal to their reference values as shown in Fig. 11(a) and Fig. 11(b). The current waveforms of A1 and A3 are shown in Fig. 11(c), where the DC components are equal to the line currents of 3 A and 4 A, respectively, and the amplitude of the AC component is 3 A. The output voltages of A1 and A3 are three-level waveforms as shown in Fig. 11(d).

The experimental results under fault conditions are shown in Fig. 12, where $C_1 = 500$ μF, and $U_{\text{lim}} = 150$ V. Due to the low-voltage level of the system, with the increase of the capacitor voltage, the fault current not only increases slowly, but also begins to decrease. At 3.5 ms after the fault occurs, I_{12} is 15.6 A in the system without fault current limiting function and 8.4 A in the system with fault current limiting function, and the current limiting capacity is 46.15%. At 5.04 ms after the fault, the capacitor voltage reaches 150 V and is bypassed. At this time, I_{12} drops to 5.6 A. Since there is no DC-CB, it will continue to rise as shown in Fig. 12(b). In practical applications, the fault current can be interrupted by DC-CB within 3-5 ms [22].

VI. Comparison with Other Typical IDCPFCs

Firstly, as a power flow control device, MM-DCPFC is compared with IDCPFCs, which are also of modular cascaded structures.

The modular IDCPFCs proposed in [13] and [14] are composed of modular multi-level converters (MMCs) and an AC transformer. In contrast, MM-DCPFC applies a power exchange mechanism based on the circulating AC current without the need for the transformer, which is beneficial to reduce the volume and cost of DCPFC. In addition, although both of them are cascaded schemes, the number of power electronic devices of the three-phase converter used in [13] and [14] is three times that of this paper at the same voltage level of DC side. Even if MM-DCPFC adds an additional A3, the number of SMs of this arm is small.

The cascaded form of dual-H-bridge IDCPFC is proposed in [15].

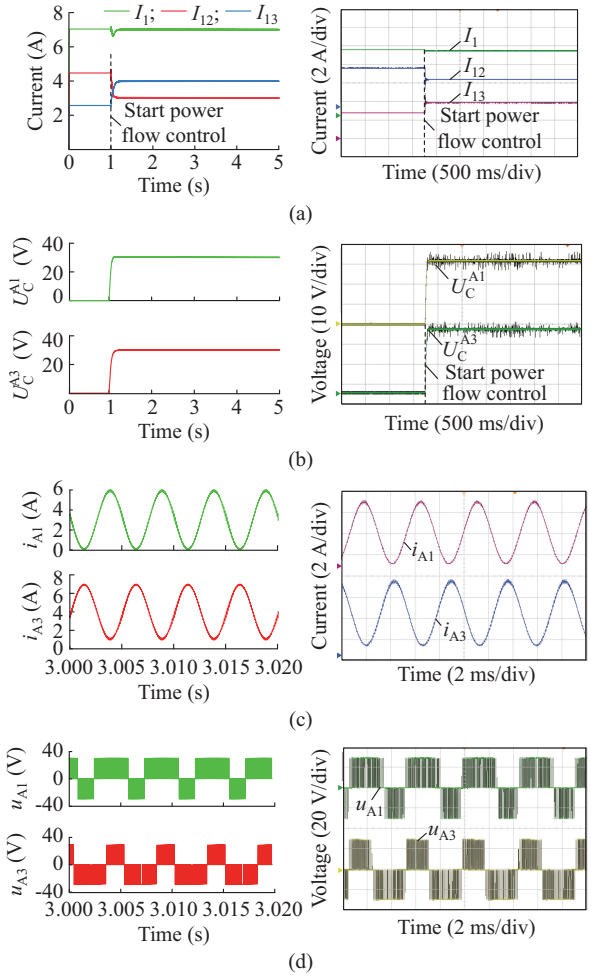

Fig. 11. Simulation (left) and experimental (right) results of power flow control mode. (a) DC line current. (b) Capacitor voltage. (c) Arm current. (d) Arm voltage.

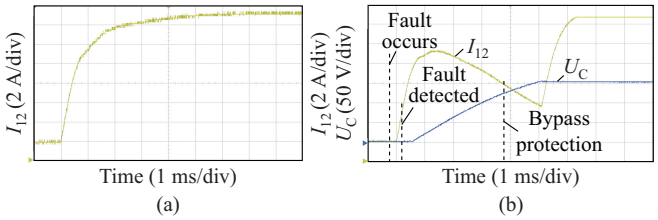

Fig. 12. Experimental results of fault current limiting mode. (a) I_{12} without current limiting. (b) Capacitor voltage and I_{12} with current limiting.

Bidirectional switches are added in [15] to realize the isolation of the capacitor voltage, thereby ensuring that the currents of two lines are independent of each other. At the same voltage level, i.e., the number of SMs is N, the number of power electronic devices in [15] is $16N$, of which $8N$ are used as isolation switches. For MM-DCPFC, if the number of SMs in A1 and A2 is N, and the number of SMs in A3 is n, the number of power electronic devices used for power flow control is $8N+4n$ (bypass thyristors do not participate in power flow regulation). Taking the simulation parameters as an example, where $N=10$, $n=1$, the scheme in [15] needs 160 IGBTs, while MM-DCPFC needs 84 IGBTs. Moreover, the voltage stress of the isolation switches in [15]

increases with the number of SMs. Therefore, MM-DCPFC can not only save more than 45% of power electronic devices, but also has advantages in the voltage stress of the devices.

The power balance of IDCPFCs in [15] and [16] can be achieved by their own power exchange mechanism instead of transformers. When realizing multi-line power flow regulation, the mechanism needs to install multiple IDCPFCs with the same structure. In contrast, MM-DCPFC provides a scheme of expanding the number of arms for multi-line regulation, which makes the advantages of MM-DCPFC continue to expand in the DC grid with complex structure.

In addition to the basic power flow control function, the current limiting function of MM-DCPFC indirectly reduces the cost of DCCBs. Without consideration of other current limiting devices, we compare the cost of circuit breaker when installing ordinary DCPFC (scheme 1) and MM-DCPC (scheme 2). Assuming that the DCCB is ABB's hybrid DC breaker [23], and the IGBT model is 5SNA1200G450300, with rated voltage of 4500 V and rated current of 1200 A. Under the simulation parameters in Section V, the DCCB needs to withstand the over-current and over-voltage when a fault occurs. There is no current limiting measure in scheme 1, so the DCCB needs to withstand the peak fault current of 3.96 kA and the system-level voltage of 200 kV, in which the voltage needs to retain 1.5 times of margin. Therefore, scheme 1 needs 67 IGBTs in series and 4 IGBTs in parallel. In order to ensure bidirectional controllability, a total of 536 IGBTs are needed. In scheme 2, the fault current can be limited by MM-DCPFC, so the DCCB needs to withstand the peak fault current of 3.43 kA and the system-level voltage of 200 kV. Considering the voltage margin and current bidirectionality, scheme 2 needs 402 IGBTs, of which 67 are connected in series and 3 are connected in parallel. Although MM-DCPFC adds 40 thyristors to protect itself, the overall number of power electronic devices is still reduced. In addition to cost saving, the reduction in the number of power electronic devices is accompanied by a reduction in gate drivers and monitoring and communication systems, thus reducing the overall power loss.

In summary, the comparison of several typical modular IDCPFCs is presented in Table V.

TABLE V
COMPARISON OF SEVERAL TYPICAL MODULAR IDCPFC

Scheme	Economy	Loss	Power flow regulation ability	Port scalability
IDCPFC in [13], [14]	1	1	5	4
IDCPFC in [15]	1	2	5	-
IDCPFC in [16]	3	3	5	-
MM-DCPFC	5	4	5	5

Note: 1 represents very bad; 2 represents poor; 3 represents moderate; 4 represents good; 5 represents very good; and "-" means that this function is not available.

VII. CONCLUSION

The MM-DCPFC proposed in this paper adopts a modular structure and has strong scalability. The power flow regulation between multiple lines can be realized by expanding the number of arms, and it can be applied to high-voltage scenarios by expanding the number of SMs. A hierarchical control method is proposed to achieve its own power balance. The simulation and experimental results verify the power flow control and power balance functions. In fault current limiting mode, MM-DCPFC can limit the rise of fault current before protecting itself. The simulation and experimental results show that MM-DCPFC can reduce the peak value of the fault current, and the current-limiting capability can be further improved by reducing the capacitance and increasing the withstand voltage value of the capacitor.

REFERENCES

[1] L. Cheng, M. Liu, Y. Sun *et al*., "A multi-state model for wind farms considering operational outage probability," *Journal of Modern Power Systems and Clean Energy*, vol. 1, no. 2, pp. 177-185, Sept. 2013.
[2] P. Song, Z. Xu, H. Dong *et al*., "Security-constrained line loss minimization in distribution systems with high penetration of renewable energy using UPFC," *Journal of Modern Power Systems and Clean Energy*, vol. 5, no. 6, pp. 876-886, Nov. 2017.
[3] P. Rodriguez and K. Rouzbehi, "Multi-terminal DC grids: challenges and prospects," *Journal of Modern Power Systems and Clean Energy*, vol. 5, no. 4, pp. 515-523, Jul. 2017.
[4] E. Veilleux and B. Ooi, "Multiterminal HVDC with thyristor power-flow controller," *IEEE Transactions on Power Delivery*, vol. 27, no. 3, pp. 1205-1212, Jul. 2012.
[5] J. Dai, Y. Tang, Y. Liu *et al*., "Optimal configuration of distributed power flow controller to enhance system loadability via mixed integer linear programming," *Journal of Modern Power Systems and Clean Energy,* vol. 7, no. 6, pp. 1484-1494, Nov. 2019.
[6] X. Zhong, M. Zhu, Y. Chi *et al*., "Composite DC power flow controller," *IEEE Transactions on Electron Devices*, vol. 35, no. 4, pp. 3530-3542, Apr. 2020.
[7] S. Balasubramanian, C. E. Ugalde-Loo, J. Liang *et al*., "Experimental validation of dual H-Bridge current flow controllers for meshed HVDC grids," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 381-392, Feb. 2018.
[8] J. Sau-Bassols, E. Prieto-Araujo, and O. Gomis-Bellmunt, "Modelling and control of an interline current flow controller for meshed HVDC grids," *IEEE Transactions on Power Delivery*, vol. 32, no. 1, pp. 11-22, Feb. 2017.
[9] H. Y. Diab, M. I. Marei, and S. B. Tennakoon, "Operation and control of an insulated gate bipolar transistor-based current controlling device for power flow applications in multi-terminal high-voltage direct current grids," *IET Power Electronics*, vol. 9, no. 2, pp. 305-315, Jan. 2016.
[10] C. D. Barker and R. S. Whitehouse, "A current flow controller for use in HVDC grids," in *Proceedings of 10th IET International Conference on AC and DC Power Transmission (ACDC 2012)*, Birmingham, UK, May 2012, pp. 1-5.
[11] W. Chen, L. Yao, G. Ning *et al*., "A novel interline DC power-flow controller (IDCPFC) for meshed HVDC grids," *IEEE Transactions on Power Delivery*, vol. 31, no. 4, pp. 1719-1727, Aug. 2016.
[12] Z. Fan, G. Ning, and W. Chen, "Power flow controllers in DC systems," in *Proceedings of 43rd Annual Conference of the IEEE Industrial Electronics Society*, Beijing, China, Oct. 2017, pp. 1447-1452.
[13] M. Ranjram and P. W. Lehn, "A three-port power flow controller for HVDC grids," in *Proceedings of International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, Seoul, Korea, Jul. 2015, pp. 1815-1822.
[14] M. Ranjram and P. W. Lehn, "A multiport power-flow controller for DC transmission grids," *IEEE Transactions on Power Delivery*, vol. 31, no. 1, pp. 389-396, Feb. 2016.
[15] V. Hofmann and M. Bakran, "An HVDC current flow controller for multi-terminal grids," in *Proceedings of International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM)*, Nuremberg, Germany, Jun. 2018, pp. 1-9.
[16] V. Hofmann, A. Schön, and M. Bakran, "A modular and scalable HVDC current flow controller," in *Proceedings of 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-*

Europe), Geneva, Switzerland, Oct. 2015, pp. 1-9.
[17] B. Li, J. He, J. Tian *et al.*, "DC fault analysis for modular multilevel converter-based system," *Journal of Modern Power Systems and Clean Energy*, vol. 5, no. 2, pp. 275-282, Mar. 2017.
[18] S. Balasubramanian, C. E. Ugalde-Loo, and J. Liang, "Series current flow controllers for DC grids," *IEEE Access*, vol. 7, pp. 14779-14790, Jan. 2019.
[19] S. Balasubramanian, C. E. Ugalde-Loo, J. Liang *et al.*, "Pole balancing and thermal management in multi-terminal HVDC girds using single H-bridge based current flow controllers," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 6, pp. 4623-4634, Jun. 2019.
[20] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1737-1746, Jul. 2009.
[21] W. Wu, X. Wu, Y. Zhao *et al*., "An improved multiport DC power flow controller for VSC-MTDC grids," *IEEE Access*, vol. 8, pp. 7573-7586, Jan. 2020.
[22] J. Hafner and B. Jacobson, "Proactive hybrid HVDC breakers – a key innovation for reliable HVDC grids," in *Proceedings of CIGRE Bologna Symposium*, Bologna, Italy, Sept. 2011, pp. 1-6.
[23] M. Heidemann, G. Nikolic, A. Schnettler *et al*., "Circuit-breakers for medium-voltage DC grids," in *Proceedings of 2016 IEEE PES Transmission & Distribution Conference and Exposition-Latin America*, Morelia, Mexico, Sept. 2016, pp. 1-6.

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