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A novel continuous control set model predictive control to guarantee stability and robustness for buck power converter in DC microgrids

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Abstract

In this paper, an adaptive continuous control set model predictive control (CCS-MPC) is proposed to eliminate the instability problem caused by the constant power load (CPL) in DC–DC buck converter applied in DC microgrids. Based on the dynamic model of energy storage elements (inductor and capacitor) in circuit, a parallel feedforward algorithm (PFA) is designed to estimate the variation of the load and input voltage. By supplying the information of the variation to the CCS-MPC controller, the large signal stability and fast recovery performance can be ensured under the existence of disturbances. To verify the control robustness of the adaptive CCS-MPC controller, the MATLAB simulations, hardware-in-loop (HIL) experiments and rapid-control-prototype (RCP) experimental results are conducted. Moreover, the comparative simulations and HIL experiments towards other nonlinear controller are conducted to investigate its dynamic performance.

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1. Introduction

Recently, DC microgrids emerge as an essential network that can support the future development of smart grids. DC microgrid is an efficient and natural connection platform that can largely integrate renewable DC power sources, energy storage systems (ESS), and loads [1–4]. In DC microgrids, loads connects to the bus directly or through the interface converters. For the former one, such as purely resistive load, since the constant voltage around reference is required for its nominal operation, it is also called as constant voltage loads (CVLs). For the latter one, by connecting the load bus through power converter, the high conversion efficiency and controllability of the loads can be guaranteed. However, such loads often operate in tight regulated mode which makes them behave as the constant power loads (CPLs). Because the CPL consumes a fixed amount of power, therefore, negative incremental impedance characteristics are introduced. This phenomenon introduces the limit-cycle dynamic (i.e., stable oscillated dynamic) [5–8] which will not only leads to the damage of the system components (capacitor & switches) but also deteriorate the stability of the overall system. To solve the instability problem caused by the CPL, several passive and active control approaches have been proposed by scholars in previous literatures. In the passive damping approaches reported in [7–9], researchers improve the system damping by add capacitors, resistors or passive LC filters into the circuit system. Although the improved circuit have a stable output performance, the new added parts cause serious increments in viewpoint of weight, cost and the power loss. On the other hand, to guarantee the system stability, active damping approaches are proposed to modify the control loops and reshape the impedance of load and source converters [10,11]. In these solutions, the small signal model based linear controller are applied, leading to the instability when the system behavior is away from its nominal operation point [6]. To overcome this defect, some control approaches which are based on the nonlinear control techniques are proposed [12–14]. A boundary controller is proposed in [12] to overcome the destabilizing effect of the DC–DC buck power converter supplying CPLs. However, since this controller is belong to hysteresis band based controller, new problems like variable switching frequency and degraded ripple effect are introduced. A fixed switch frequency based sliding mode control strategy is proposed in [13]. This strategy can stabilize the CPLs at wide load variation only when the real time value of the capacitor current is obtained. However, during its measurement, a equivalent resistance which is series to capacitor and degraded ripple filtering effect are introduced. Moreover, chattering problem may be introduced, since the proposed method requires a very high switching frequency to operate. A synergetic controller based approach is reported in [14] to deal with the instability problem caused by CPL supplied by a parallel DC–DC buck converters system. The results showed better and faster control response when compared with linear control method. However, no detailed analysis of CPL can be found in this paper. In [15], an nonlinear disturbance observer based passivity-based control is proposed to solve the instability problem caused by the CPL. Although, this control strategy provides robust control dynamic. However, it is highly influenced by the tuning of the control parameters such as damping gains (R_{1d} , R_{2d}) and observer gains (λ_1 , λ_2).

One of the most popular nonlinear control strategies used recently in power electronic converters is the model predictive control (MPC). As a promising nonlinear control method, MPC is effective, easy to master, easy to contain multiple constrain and various objectives [16]. Among various kinds of MPC, finite control set model predictive control (FCS-MPC) and continue control set model predictive control (CCS-MPC) are the most popular [17]. According to the definition, MPC can only achieve good performance when the prediction model is accurate sufficiently. However, the accurate model of the system is usually affected by external disturbance, system uncertainties and system mismatches during its operation. To avoid the static error caused by the inductance's equivalent series resistance (ESR), FCS-MPC is combined with the proportional–integral (PI) controller and the Luenberger observer [18]. In this combination, the FCS-MPC strategy acts as the inner current-loop while the PI is used as outer voltage-loop, and Luenberger observer is used to compensate model mismatch caused by the ESR of inductor. By combined with the observer, the steady-state output error is eliminated by this composite controller. In [19], in order to remove the static error caused by the variation of resistance and the model mismatch of inductance, the CCS-MPC controller is combined with Luenberger observer. In this paper, the CCS-MPC is used in inner-loop of a double-loop controller, whereas, the observer is used to supply the disturbance information. Combined together, the static error of output voltage is mitigated. The strategies described in [18] and [19], provided acceptable performance, they can ensure the stability under the model mismatch or resistance load variation. However, the instability caused by CPL has not been considered in these works. Recently, several literatures about eliminating the disturbance of CPL by MPC are published. An explicit model predictive control (eMPC) is proposed in [20] to maintain the stability of boost converters supplying CPL. By solving a multiparametric nonlinear problem over

a simplex partition of state space, the optimal control law can be obtained even with the disturbance of CPL. However, similar with the fixed switching frequency sliding mode controller mentioned above, this approach needs the real time information of the output current to operates. A decentralized model predictive control (DMPC) is proposed in [21]. Although this method can not only guarantee the stability of the multi-boost converters system, but also ensures power sharing to different subsystems, the operation of this approach needs the real time value of the power consumed by the CPL [21]. An extended Kalman Filter based MPC is proposed in [22] to guarantee the stability of the DC microgrid on board. However, it mitigates the instability problem from the view point of the secondary control. In [23], the MPC is combined with higher order sliding mode observer (HOSMO) to eliminate the instability caused by system disturbance such as the load (CVL and CPL) and input voltage variations. In order to maintain a good dynamic performance, the observer needs to be well tuned which is rely on experience and plenty of time [24,25].

In this paper, based on the buck converter supplying parallel load (R+CPL), a novel adaptive CCS-MPC is constructed to eliminate the voltage output static error generated by the system disturbances such as the variations of source bus voltage and load (CVL and CPL). A double loop controller consists of CCS-MPC and another capacitor dynamic based voltage control method is proposed to track the reference in nominal condition. Although this double-loop controller has a good performance, it is not robust enough during disturbances. Therefore, in order to improve the robustness of the mentioned controller, a parallel feedforward algorithm is presented to compensate the disturbance. Combined together, the static error of the output voltage can be eliminated even during the disturbances appear.

This paper is organized as follows: Section 2 presents the equations modeling of the system and problem description. Section 3 introduces the closed-loop control design process of the mentioned CCS-MPC and also the parallel feedforward algorithm. The MATLAB simulation and HIL experimental results are shown in Sections 4 and 5, respectively. While the rapid control prototype experimental results are represented in Section 6. The conclusion is written in Section 7.

2. System modeling and problem description

As a new efficient power system, DC microgrids are widely applied in data center, telecom power supply systems, electrical transportation (such as EVs, ships and airplanes) [16]. The typical structure of DC microgrid has cascaded distributed power architectures as shown in Fig. 1.

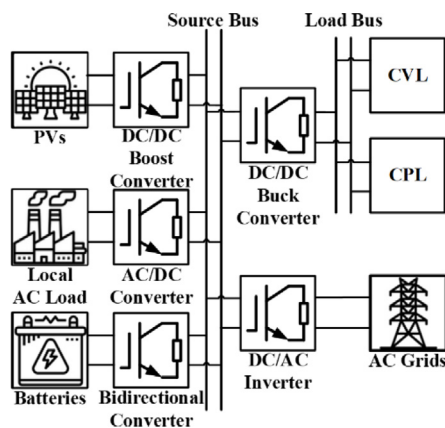


Fig. 1. A generic scheme of DC microgrid systems.

As can be seen from the above figure, the renewable resources (represented as PV), energy storage system (ESS) or AC grid (if not works in island mode) transmit its energy to DC microgrid through the interface converters. However, to reduce the power loss during the transmission, the source bus voltage level is too high to be used by the loads directly. In order to provide energy at the load voltage level, DC/DC converter are applied to reduce the voltage to the meets the requirement of the load bus. As an important part of the DC microgrid, the load includes resistive load, load connected to DC/AC inverter and load connected to DC/DC converter. Since the last

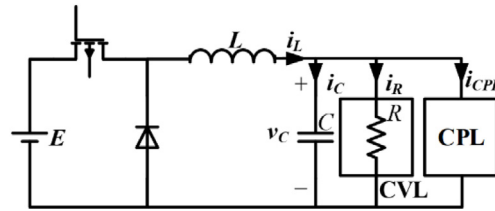


Fig. 2. DC–DC buck converter supplying composite loads.

two loads often work in tightly regulated mode, they can be redeemed as CPLs. The system represented in Fig. 1 can be simplified as a cascaded system consisting of DC/DC buck converter connecting with CVL and CPL, and the simplified system is shown in Fig. 2.

The dynamic model of system in Fig. 2 can be described as

$$\begin{cases} L \frac{di_L}{dt} = E\mu - v_C \\ C \frac{dv_C}{dt} = i_L - \frac{v_C}{R} - \frac{P_{CPL}}{v_C} \end{cases} \quad (1)$$

In (1), i_L represents the inductor current, v_C represents capacitor voltage, E represents the input voltage; R , L and C represents the resistive load, inductance and capacitance respectively; μ represents the duty ratio; i_{CPL} represents the power consumed by CPL.

According to Eq. (1), the input voltage, resistive load, inductance, capacitance, power consumed by CPL, the ESR of inductor can affect the stable output of buck converter. However, according to the data shown in [18], we can know that, the influence of inductance and capacitance on the output can be ignored when compared with that of the ESR of inductor. Moreover, it is difficult for inductance and capacitance values to change dramatically under normal conditions. And when compared with the variation of CPL, resistive load and input voltage, the influence caused by ESR of inductor can be neglected [15]. Therefore, the main focus of this paper is to mitigate the instability caused by the variation of the input voltage, resistance of CVL, and power of CPL. Generally, during the operation of the controller, except for the inductance current and capacitance voltage, the other values in the control equations are redeemed as constant. However, in order to globally track the reference voltage of buck circuit during disturbances, the fluctuation of input voltage, load resistance and CPL must be taken into consideration and the specific methods will be introduced later.

3. Proposed method

In this section, the design process of a robust and adaptive CCS-MPC will be presented. The aim of the proposed control algorithm is fulfilling the stable tracking of the reference voltage free from the influence of disturbances. The control algorithm proposed in this paper can be divided into two parts, a double loop controller and a feedforward state estimation algorithm. The double loop controller consists of a capacitor dynamic based outer voltage loop and an CCS-MPC based inner current loop. The double loop control ensures the tracking of the reference voltage and current under nominal condition, while the state feedforward algorithm provides real-time disturbance information. Combined together, the proposed algorithm can achieve accurate tracking under disturbance state.

3.1. Voltage loop controller

As depicted in Fig. 2, the voltage of DC load side is directly related to the effect of capacitor C. According to the dynamic characteristic equation of capacitance:

$$C \frac{dv_C}{dt} = i_C \quad (2)$$

The change of the v_C is related to the current flowing through it. According to forward Euler method, the (2) can be rewritten as

$$i_C(k+1) = C \frac{dv_C}{dt} = C \frac{v_C(k+1) - v_C(k)}{T_s} \quad (3)$$

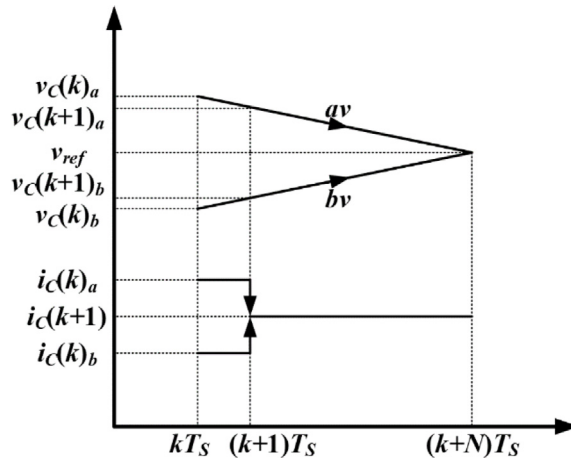


Fig. 3. Next instant reference design.

where the T_S is the switching period of the converter. During the period v_C pursuing the v_{ref} , we assume the change of v_C in a very short period is linear, just as illustrated in Fig. 3. Since the value of i_C which is related to the error between v_C and v_{ref} cannot be randomly large, this paper introduces a parameter N to acted as the reference prediction horizon [26,27].

As depicted in Fig. 3, $v_C(k)_a$ (or $v_C(k)_b$) represents the voltage at moment k which is higher (or lower) than the reference voltage v_{ref} . During its approach to the v_{ref} , the output voltage follows the av (or bv) route. Meanwhile, the current step down (or step up) to $i_C(k + 1)$ from $i_C(k)_a$ (or $i_C(k)_b$). As defined above, the reference prediction horizon N stands for the number of switching cycles for the voltage reach its final reference from its present value. Therefore, Eq. (3) can be modified as

$$i_C(k + 1) = C \frac{v_{ref} - v_C(k)}{NT_S} \tag{4}$$

Besides, based on the first Kirchoff’s law (KCL), the value of the current flowing through the inductance i_L is equal to the sum of capacitance current i_C , resistor current i_R and CPL current i_{CPL} . Therefore, the inductance current i_L at the instant of $k + 1$ can be calculated out through Eq. (5) as shown below.

$$i_L(k + 1) = C \frac{v_{ref} - v_C(k)}{NT_S} + \frac{v_{ref}}{R} + \frac{P_{CPL}}{v_{ref}} \tag{5}$$

Then, the current of the inductor at the $k + 1$ moment can be brought into the current loop as the reference current.

3.2. Current loop controller

In inner loop, an CCS-MPC with one step horizon is adopted, its demand for computing ability is not as high as that of multiple steps horizon MPC [19]. Fig. 4 shows the variation of the inductor current in a switching cycle. According to Eq. (1), the current slopes in a switching period are

$$\begin{cases} f_{i1} = f_{i3} = \frac{E - v_C}{L} \\ f_{i2} = -\frac{v_C}{L} \end{cases} \tag{6}$$

Assuming inductor current at the end of previous switching period is i_{s0} , then the inductor current at the instant of $k + 1$ can be calculated by

$$i_L(k + 1) = i_{s3} = i_{s0} + f_{i1}t_1 + f_{i2}t_2 + f_{i3}t_3 \tag{7}$$

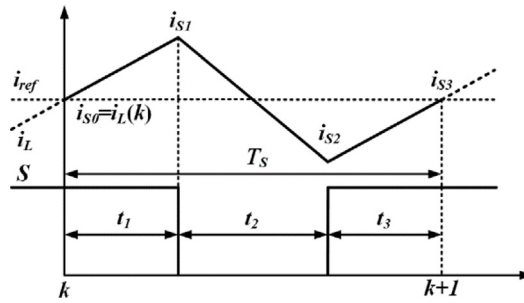


Fig. 4. Inductor current variation in one switching cycle.

In the above formula, t_1 represents first turn-on period, t_2 represents the second turn-off period and t_3 represents second turn-on period. For reducing burden of computation, the value of t_3 are assigned equally with t_1 . Therefore, the relationship among i_{sn} , t_n and f_{in} ($n = 1,2,3$) can be summarized as follow.

$$\begin{cases} i_{S1} = i_{S0} + f_{i1}t_1 \\ i_{S2} = i_{S0} + f_{i1}t_1 + f_{i2}t_2 \\ i_{S3} = i_{S0} + 2f_{i1}t_1 + f_{i2}t_2 \end{cases} \quad (8)$$

In order to achieve accurate current tracking, the current value at t_n ($n = 1,2,3$) in a switching period is taken into consideration by put them into cost function shown below.

$$J(k) = (i_{ref} - i_{S1})^2 + (i_{ref} - i_{S2})^2 + (i_{ref} - i_{S3})^2 \quad (9)$$

In the above equation, i_{S1} , i_{S2} and i_{S3} are the inductance current values at the instant $k + t_1$, $k + t_2$ and $k + t_3$, respectively. By substitute i_{sn} ($n = 1,2,3$) into the cost function, the cost function can be modified as

$$J(k) = (i_{ref} - i_{S0} - f_{i1}t_1)^2 + (i_{ref} - i_{S0} - f_{i1}t_1 - f_{i2}t_2)^2 + (i_{ref} - i_{S0} - f_{i1}t_1 - f_{i2}t_2 - f_{i3}t_3)^2 \quad (10)$$

The value of t_1 which makes the cost function got its minimum value can be gotten by deriving Eq. (10), and that optimal value is shown as

$$\begin{cases} t_1 = t_3 = \frac{4(i_{ref} - i_{S0}) - 3T_S f_{i2}}{6(f_{i1} - f_{i2})} \\ t_2 = T_S - 2t_1 \end{cases} \quad (11)$$

Therefore, the duty ratio of PWM can be determined by acquiring the action time of each switch state in a switching cycle. Moreover, in order to ensure the switch operates as planned, the PWM modulation in this paper is in an isosceles triangle modulation mode.

3.3. Parallel feedforward algorithm

As mentioned above, the reference current i_{ref} used in the inner loop can be obtained by (5). However, the time-varying parameters such as the resistive load and the power of the CPL which contained in (5) usually changes frequently. Moreover, these parameters are often set at their nominal value in the controller. As shown in the equation below, if their variations are ignored, off-set shown in the end of below equation will be introduced.

$$\begin{aligned} i_L(k+1) &= C \frac{v_{ref} - v_C(k)}{NT_S} + \frac{v_{ref}}{R + \Delta R} + \frac{P_{CPL} + \Delta P_{CPL}}{v_{ref}} = C \frac{v_{ref} - v_C(k)}{NT_S} + \frac{v_{ref}}{R} + \frac{P_{CPL}}{v_{ref}} \\ &\quad - \frac{v_{ref} \Delta R}{(R + \Delta R)R} + \frac{\Delta P_{CPL}}{v_{ref}} \end{aligned} \quad (12)$$

In the above equation, the ΔR stands for the change of the CVL resistance, and the ΔP_{CPL} stands for the change of the CPL power. Similarly, the change of input voltage can affect the slope of current as shown below

$$\begin{cases} f_{i1} = f_{i3} = \frac{E + \Delta E - v_C}{L} \\ f_{i2} = -\frac{v_C}{L} \end{cases} \quad (13)$$

where ΔE is the change of the input voltage.

To overcome this defect, the information of time-varying parameters need to be obtained. Based on the first Kirchhoff’s law (KCL), the inductive current i_L is equal to the sum of capacitance i_C , resistance i_R and constant power load currents i_{CPL} . Meanwhile, the inductance current i_L can be obtained by the current sensor, and the capacitor current i_C can be obtained by the change of capacitor voltage. Therefore, the value of current flowing through the load can be calculated by the following equation

$$i_R + i_{CPL} = i_L - i_C = i_L - C \frac{v_C(k) - v_C(k - 1)}{T_S} \quad (14)$$

Therefore, the equation calculating the current reference value at the next step should be modified as

$$i_{ref}(k + 1) = C \frac{v_{ref} - v_C(k)}{NT_S} + i_L(k) - C \frac{v_C(k) - v_C(k - 1)}{T_S} \quad (15)$$

The variation of input voltage E can also be obtained by the dynamic characteristics of the inductor. Therefore, the input voltage value can be calculated as

$$E = \frac{v_C + L\dot{i}_L}{\mu} = \frac{v_C}{\mu} + L \frac{i_L(k) - i_L(k - 1)}{\mu T_S} \quad (16)$$

By substituting (16) into (6), we can get the current slope equations considering input voltage variation are

$$\begin{cases} f_{i1} = f_{i3} = \frac{v_C}{L\mu} + \frac{i_L(k) - i_L(k - 1)}{L\mu T_S} - \frac{v_C}{L} \\ f_{i2} = -\frac{v_C}{L} \end{cases} \quad (17)$$

To sum up, the reference current can be calculated by Eq. (15), and the duty ratio can be obtained by solve the equations of (9), (10), (11) and (17), then the diagram of proposed method can be described as Fig. 5.

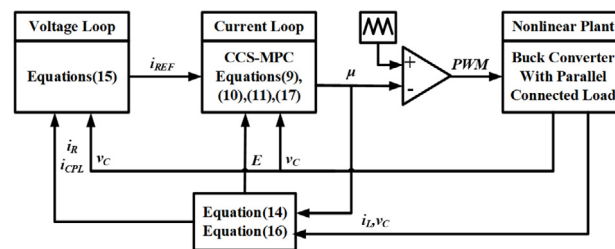


Fig. 5. The diagram of the proposed control method.

As depicted in Fig. 5, the current consumed by the load and the input voltage are calculated and send to the dual loop controller. After that, the double loop control algorithm is applied to fulfill the stable tracking of voltage and current under disturbance without static error.

4. Simulations and discussions

In this section, the effectiveness of proposed control method against disturbance have been verified using MATLAB simulation. During the simulation and latter HIL experiment, N is set as 2. Meanwhile, the i_L , v_C and μ used in (14) and (16) are their average value. The system parameters applied in the simulation are shown in Table 1.

Table 1. System parameters.

Variables	Description	Value
V_{ref}	Output voltage reference	750 V
f_s	Switching frequency	20 kHz
E	Nominal input voltage	1500 V
R	Nominal resistive load	50 Ω
L	Inductance	4 mH
C	Capacitance	1 mF
P_{CPL}	Nominal power of CPL	14.4 kW

4.1. Input voltage disturbance

In this section the robustness of the proposed control strategy during the input voltage variations will be investigated. As shown in Fig. 6, initially, the input voltage is set at 1500 V; then the input voltage decreased to 1000 V at 0.04 s and it recovered to 1500 V at 0.06 s. At 0.08 s, the input voltage increased to 2000 V and recovered to 1500 V at 0.1 s. As can be observed, the proposed controller provides a robust control dynamic performance.

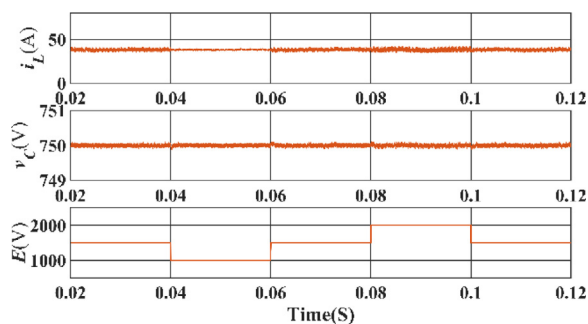


Fig. 6. Voltage and current waveforms with input voltage variation.

4.2. CPL disturbance

This section presents the effectiveness of the proposed controller during the change of the CPL. Fig. 7 represents the output performance of the system during the CPL variations. The power of the CPL varied from 14.4 kW to 21.7 kW at 0.04 s and returned to 14.4 kW at 0.06 s. It can be noticed that, with the increase of CPL, a robust transient performance is achieved (0.5 V) with short settling time (0.9 ms). Similarly, with the decrease of CPL, the recovery time is short (1.34 ms) and the transient voltage performance is robust (0.6 V). In both CPL changes, the proposed control scheme CCS-MPC showed accurate control tracking with fast recovery performance.

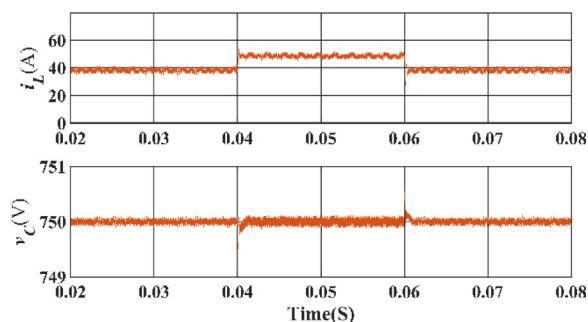


Fig. 7. Voltage and current waveforms with CPL power variation.

4.3. CVL disturbance

This part presents the performance of the adaptive control scheme against the change of the resistive load. Fig. 8 depicts the dynamic performance of the mentioned controller during resistive load changes. Initially, the resistive load is fixed at 50 Ω and then decreased to 33.33 Ω at 0.04 s, and recovered to 50 Ω at 0.06 s. During the decrease of resistance load, the voltage drops slightly to 749.7 and returns to 750 in 1.1 ms. During the increase of the resistive load from 33.33 Ω to 50 Ω, the output voltage rises from 750 to 750.4 and returns to the reference voltage (750 V) in 0.9 ms. This slight deviation with fast recovery performance proved that, the proposed control algorithm ensures large signal stability during resistive load changes.

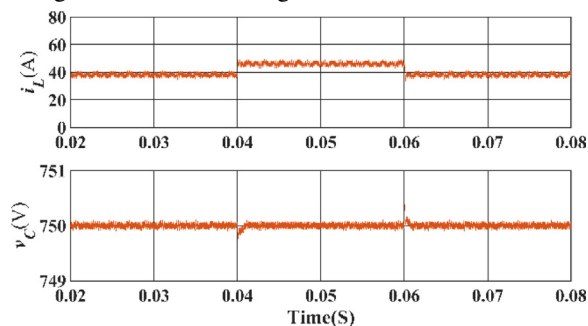


Fig. 8. Voltage and current waveforms with resistance variation.

4.4. Comparison simulation between the adaptive CCS-MPC and previous literature

In this part, two comparisons have been undertaken. First comparison is made between the adaptive control strategy before and after adding the parallel feedforward estimation algorithm (nominal CCS-MPC). The second comparison is conducted between the adaptive controller and the passivity-based control with nonlinear disturbance observer (PBC+NDO) strategy reported in [15]. Fig. 9 presents the dynamic performance of nominal CCS-MPC and the proposed controller during the change of the input voltage. We can notice that, the nominal CCS-MPC failed to track the reference voltage precisely, while the proposed method depicts robust control dynamic. Fig. 10 depicts the comparison between the nominal and the proposed adaptive CCS-MPC strategy under the change of CPL. We can notice that, in Fig. 10, steady-state error can be observed in the output voltage of the nominal CCS-MPC, and it exists until the CPL recover to its nominal value. Whereas, the proposed control strategy keeps the voltage properly regulated at the reference value as 750 V. Fig. 11 shows the performance of proposed algorithm and nominal CCS-MPC under the changes of the resistance. As can be observed, the adaptive strategy maintain the voltage at 750 V accurately. However, the contrast set failed in the tracking of the reference voltage and steady-state error is generated.

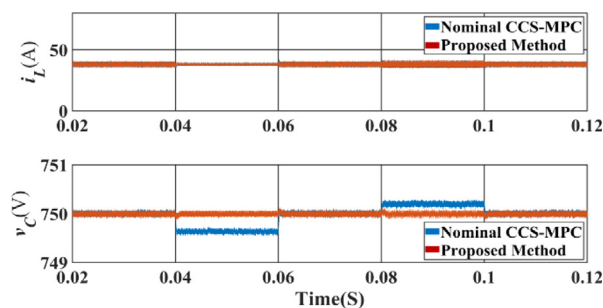


Fig. 9. Voltage and current waveforms with input voltage variation compared with nominal CCS-MPC.

Secondly, we compare the dynamic performance of the adaptive control strategy with the PBC+NDO strategy shown in [15]. We make this comparison because both control strategies are nonlinear control systems, and both of

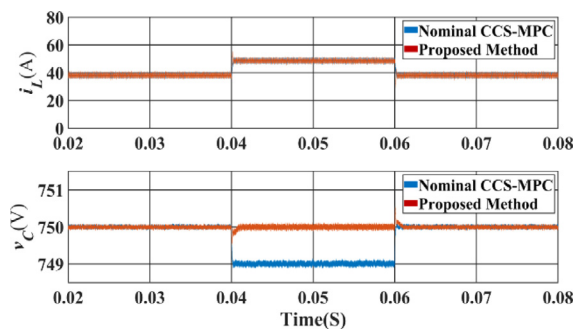


Fig. 10. Voltage and current waveforms with CPL variation compared with nominal CCS-MPC.

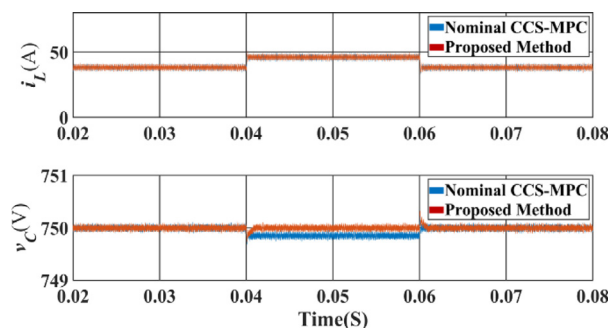


Fig. 11. Voltage and current waveforms with resistance variation compared with nominal CCS-MPC.

them consist of the observing technique to avoid the static error. Therefore, the comparison is made between them during CPL and resistive load changes. The dynamic performance of the output voltages and inductor currents during the CPL changes are presented in Fig. 12. It is obviously that, the adaptive CCS-MPC strategy is better than the PBC+NDO in terms of less overshoot dynamics and faster settling time performance. Fig. 13 depicts the dynamic performances of PBC+NDO and proposed control method under the resistive load changes. The resistive load decreased from 50 Ω to 33.3 Ω at 0.04 s, and recovered to 50 Ω at 0.06 s. It can be notice that, the proposed adaptive CCS-MPC has less overshoot and faster response when compared with PBC+NDO.

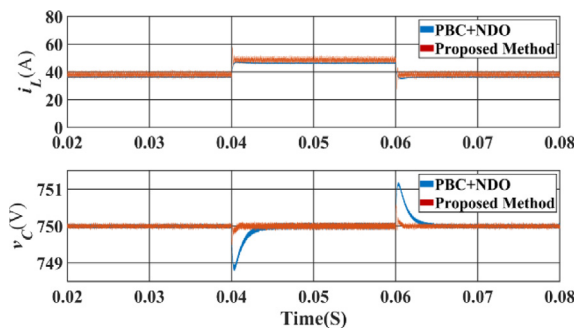


Fig. 12. Voltage and current waveforms with CPL power variation compared with PBC+NDO.

5. Hardware-in-loop experimental results

This part presents a hardware-in-loop (HIL) experimental platform which is used to further verify the MATALAB simulation results obtained above. This setup allows to connect the MATLAB Simulink model with the digital signal

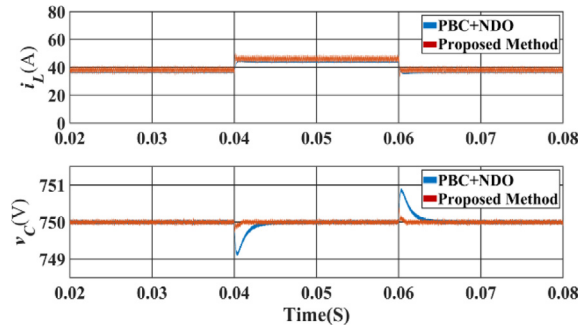


Fig. 13. Voltage and current waveforms with resistance variation compared with PBC+NDO.

processor (DSP) through the OPAL-RT real-time simulator. Fig. 14 represents the structure of the HIL experimental setup.

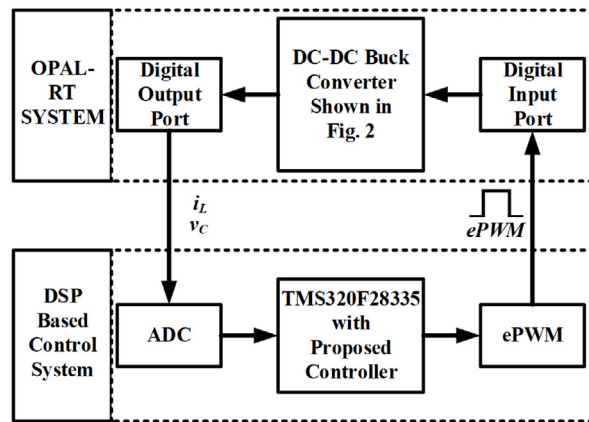


Fig. 14. Block diagram represents the HIL experiment.

In this platform, the controller mentioned above is performed in the DSP TMS320F28335, while the Simulink model operates in the OPAL-RT in real-time. The system output signal such as i_L and v_C are send from the analog port of the OPAL-RT to the ADC module of DSP. After calculated by the adaptive CCS-MPC, the PWM signal is send to the digital input port of the OPAL-RT to maintain the operation of the system in next cycle. In the experiments, in order to meets the output limits of OPAL-RT, the i_L and v_C of the system are minused 740 and 50, respectively. Meanwhile, due to the computing power of the OPAL-RT, the switching frequency is decreased to 10 kHz and the step size is set at 10^{-5} s.

Fig. 15 depicts the HIL dynamic performance of the proposed adaptive CCS-MPC controller and the nominal CCS-MPC controller to further verify the results obtained in Fig. 9. We can observe that, the nominal CCS-MPC (CH3, blue) failed to track the reference voltage during input voltage variations and a steady-state error in output voltage is created. The proposed algorithm (CH4, red) shows the robust dynamic performance against input voltage variation and the maximum variation of the output is only around 0.8 V which recover to reference in 4 ms. In order to further verify the simulation result shown in Fig. 10 the HIL comparison towards nominal CCS-MPC during the variation of CPL is conducted, and the result is depicted in Fig. 16. As it depicts, when the power of CPL increases from 14.4 kW to 21.7 kW, the output voltage of proposed control strategy (CH4, red) drops to 749 V and after around 2 ms it back to the reference voltage again. When the power of CPL decreases back to 14.4 kW, the output voltage of proposed control strategy rises to 751 V and it back to 750 V in 2 ms. However, for the nominal CCS-MPC (CH3, blue), the target of tracking the reference voltage accurately cannot be fulfilled, and a static error of 5.2 V can be observed during the period in which the CPL consumes 21.7 kW from buck converter

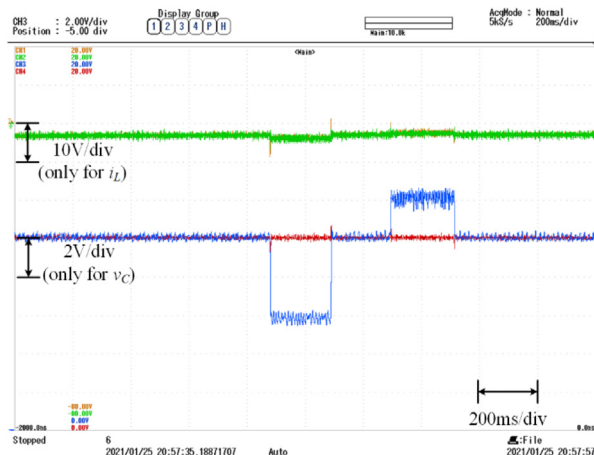


Fig. 15. Voltage and current waveforms with input voltage variation compared with Nominal CCS-MPC in HIL. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

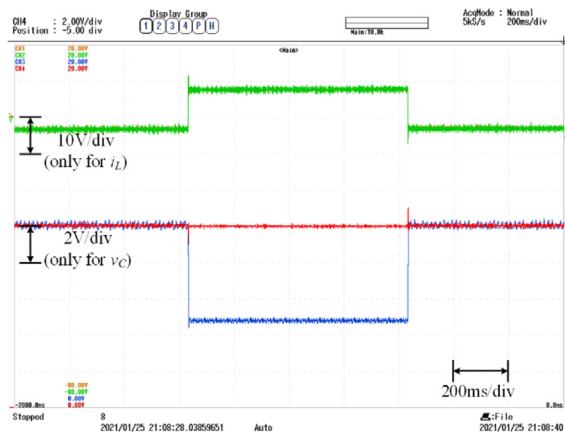


Fig. 16. Voltage and current waveforms with CPL variation compared with Nominal CCS-MPC in HIL.

Fig. 17 shows the HIL contrastive experimental results towards nominal CCS-MPC during the variation of resistance. As can be seen, the voltage of the proposed algorithm (CH4, red) drops 0.6 V and it back to 750 V in 2 ms when the resistance load decrease to 33.3 Ω from 50 Ω. When the resistance recovers to 50 Ω, the voltage of the proposed algorithm rises 0.6 V and after 2 ms it back to reference voltage. However, for the nominal CCS-MPC (CH3, blue), a static error of 3.8 V can be observed when the resistance is 33.3 Ω. Fig. 18 demonstrates the HIL verification for the result obtained in Fig. 12. The variation of CPL is performed for both PBC+NDO and proposed adaptive CCS-MPC strategy to compare the dynamic performance of them under disturbance of time-varying CPL load. We can notice that, when the CPL increase from 14.4 kW to 21.7 kW the voltage of PBC+NDO (CH3, blue) drops to 749.2 and it recovers in 4 ms while the voltage of the proposed method (CH4, red) back to reference voltage from 749.6 in less than 3 ms. Similarly, we can observe that, very fast recovery response and little overshoot are obtained when the power back to 14.4 kW.

Fig. 19 represents the dynamic performance of the proposed control method and PBC+NDO during the resistance variation. As the resistance decreases to 33.3 Ω, the voltage of proposed controller (CH4, red) drops to 749.4 V and after 2 ms it back to reference value while that of PBC+NDO (CH3, blue) drops to 749.1 V and after 4 ms it back to reference value. When the resistive load increases back to 50 Ω, the voltage of proposed control method rises to 750.5 V and after 2 ms it back to 750 while that of PBC+NDO rises to 750.9 V and it spends 3 ms to recover. With aid of Simulink and HIL results, it can be concluded that, the proposed controller provides superior dynamic performance with fast recovery response and short settling time.

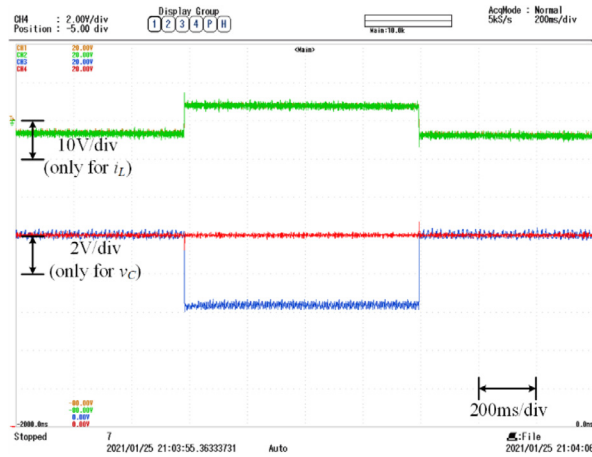


Fig. 17. Voltage and current waveforms with resistance variation compared with Nominal CCS-MPC in HIL. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

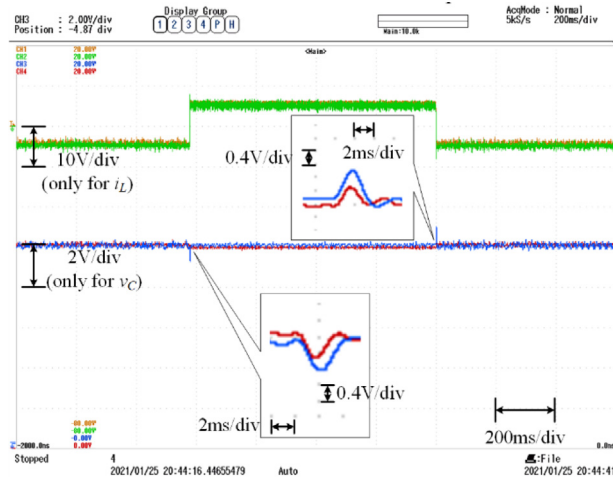


Fig. 18. Voltage and current waveforms with CPL variation compared with PBC+NDO in HIL.

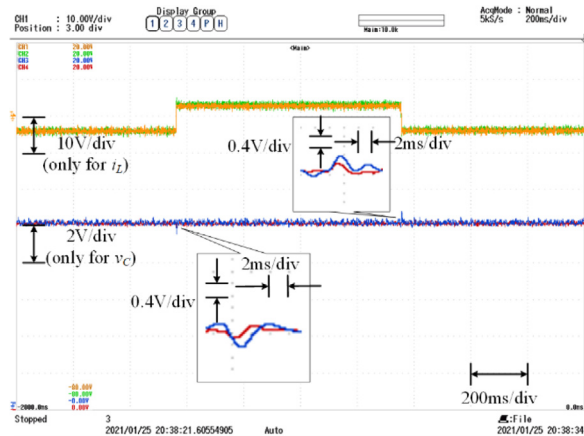


Fig. 19. Voltage and current waveforms with resistance variation compared with PBC+NDO in HIL. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

6. Rapid control prototype experimental results

In order to further verify effectiveness the controller on hardware experimental platform, a rapid control prototype (RCP) experimental set is build and applied. The structure of the RCP experiment platform is shown in Fig. 20, this platform is consisting of Buck converter, drive circuit, sampling circuit, composite load, and OPAL-RT 5600 system (including a host PC). In this platform, the OPAL-RT send the PWM signal (3.3 V) to Buck circuit through driving circuit which can improve the signal so that the IGBT can be driven by it (± 15 V). Meanwhile, the output signals are sent to OPAL-RT systems through sampling circuit, then these signals will be used in the calculation of the proposed method and the next PWM signal will be send to the driving circuit.

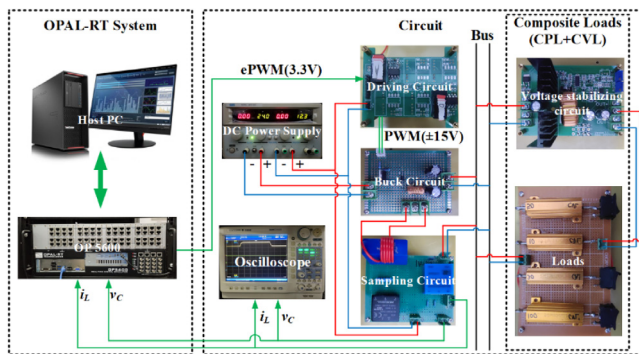


Fig. 20. The structure of the rapid control prototype experiment platform.

The experimental performance of the proposed algorithm during the variation of input voltage, CVL and CPL will be shown below. Fig. 21 depicts the waveforms of capacitor voltage (CH2, green) and inductor current (CH7, blue) during the change of the input voltage (CH1, yellow). In this experiment, the input voltage increases to 34 V from 24 V and after about 1 s, it recover to its reference value again. During this process, the power of CPL stays at 10 W and the resistance of CVL fixes at 50 Ω . As can be seen, the capacitor voltage tracks its reference voltage well at 18 V, indicating the proposed algorithm provide a robust behavior during the input voltage variation.

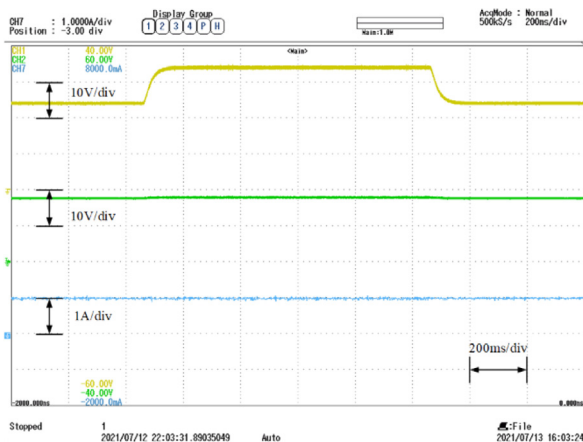


Fig. 21. Voltage and current waveforms with input voltage variation in RCP experiment . (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

Fig. 22 shows dynamic performance of the capacitor voltage and inductor current during the variation of the power of CPL. In this experiment, the power of CPL changes from 10 W to 13.4 W and recover to 10 W around 1S, meanwhile, the input voltage stays at 24 V and the resistance of the CVL fixes at 50 V. It can be observed from Fig. 22 that during the change of the CPL, the capacitor voltage is fixed at 18 V, and inductor current varies with the change of the CPL which is coincidence with Fig. 18.

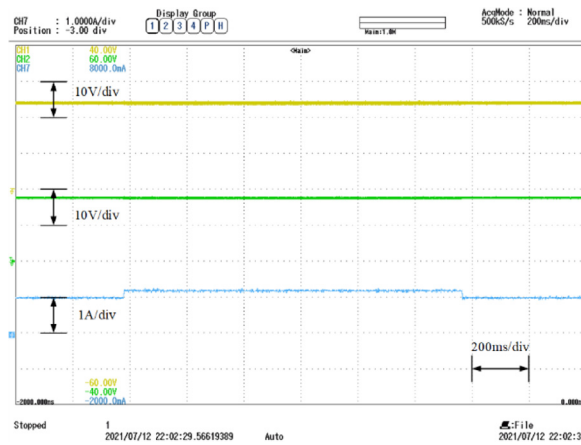


Fig. 22. Voltage and current waveforms during CPL variation in RCP experiment.

Fig. 23 represents the dynamic performance of the system during the variation of CVL. In this process, the input voltage and power of CPL do not change, the only variations are the resistance of CVL, which drops from 50Ω to 33.34Ω and recover to 50Ω in around 0.5S. As can be seen, the proposed algorithm ensures robust and accurate control performance during the change of the CVL.

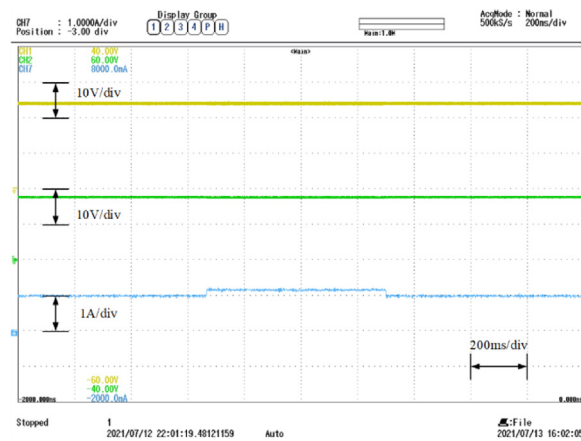


Fig. 23. Voltage and current waveforms with CVL variation in RCP experiment.

7. Conclusion

The instability problem caused by the DC–DC buck power converter feeding the CVL and CPL in DC microgrid systems has been addressed. An adaptive CCS-MPC control strategy is proposed and used to stabilize the system and to eliminate the steady-state error caused by the system disturbance such as input voltage and load variations. To verify the control performance, fair comparisons have been undertaken among the normal CCS-MPC, PBC+NDO and proposed adaptive CCS-MPC through Matlab/Simulink simulation and HIL real-time simulator. Moreover, the proposed method is also verified on the RCP experimental platform. According to the results above, the proposed control strategy can have a fairly good performance in terms of recovery, settling time, and overshoot during a variation in load and input voltage. The information obtained would allow engineers more confidence in making power converter designs concerning DC microgrid system stable and robust operation

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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