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ORIGINAL RESEARCH PAPER

An enhanced single gate driven voltage-balanced SiC MOSFET stack topology suitable for high-voltage low-power applications

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Abstract

In the fabrication of some high-voltage low-power applications, low cost is much concerned, and thus using silicon carbide (SiC) MOSFET stack consisting of series connected low-voltage devices is preferred rather than using an expensive single high-voltage device. Therefore, a cost-efficient single gate driven voltage-balanced SiC MOSFET stack topology is proposed in this paper, where only some passive components are equipped with the stack. With a concept of single gate driver, the gate driver design of an SiC MOSFET stack is simplified. With an automatic balancing circuit which operates well with the sequential lagging single gate driver, good voltage balancing of SiC MOSFETs in the stack is realized without causing much extra loss and no additional active control is required. The working principle is illustrated in detail and the parameter selection together with design consideration is presented. Next, this topology is compared with RCD snubber method and active delay adjusting method to better illustrate its advantages. Finally, in a typical high-voltage low-power application, auxiliary power supply, the simulation and experimental results further verify the effectiveness of the proposed topology.

1 | INTRODUCTION

Nowadays, power electronics converters rated from several kilovolts to tens of kilovolts have widely emerged in plenty of industrial applications for meeting higher power demand [1]. In such a tendency, the research on high-voltage high-power applications is very popular, where the multilevel converters are generally adopted as the main topologies, including modular multilevel converter (MMC) and cascaded H-bridge topology (CHB). Apart from that, the research on high-voltage low-power applications has also drawn extensive attention, for example, the design of auxiliary power supplies (APSs) for above MMC, CHB etc.

In those high-voltage low-power applications, low cost is a factor of great concern since they usually just paly supporting roles for high-voltage high-power applications. Take APS of MMC shown in Figure 1 as an example [2], APS is an essential part in each sub-module (SM) to power the gate drivers (GD) etc. for inside high-voltage high-power switching devices (S_1, S_2) such as 10 kV silicon-carbide (SiC) based metal-oxide-semiconductor field-effect transistors (MOSFETs). To ease the burden of high-voltage insulation design and facilitating the expansion of SMs, such APS extracting the power from the capacitor of each SM is more common. In this way, the input voltage of APS is high, and the power that APS needs to provide is low, which makes APS a high-voltage low-power dc/dc converter. Using high-voltage devices to design such an APS is an inappropriate choice due to the high cost. Instead, low-voltage devices are much preferred and easier to obtain, where some devices are especially built for the APS application, such as 1.7 kV/5 A SiC MOSFET [3]. Therefore, although the reliability is reduced, using the SiC MOSFET stack, that is, the series connection of SiC MOSFETs, is a good solution in order to meet the high-voltage requirement.

In the conventional way, as shown in the lower right part of Figure 1, each SiC MOSFET in the stack requires an independent driving voltage pulse [4]. Since the gate loops and power loops of devices are not identical caused by the difference of device parasitic parameters and driving pulses, a natural voltage unbalancing exists [5]. Therefore, static voltage balancing resistors and dynamic voltage balancing circuit are necessary [6, 7]. In the meantime, this way gives sufficient

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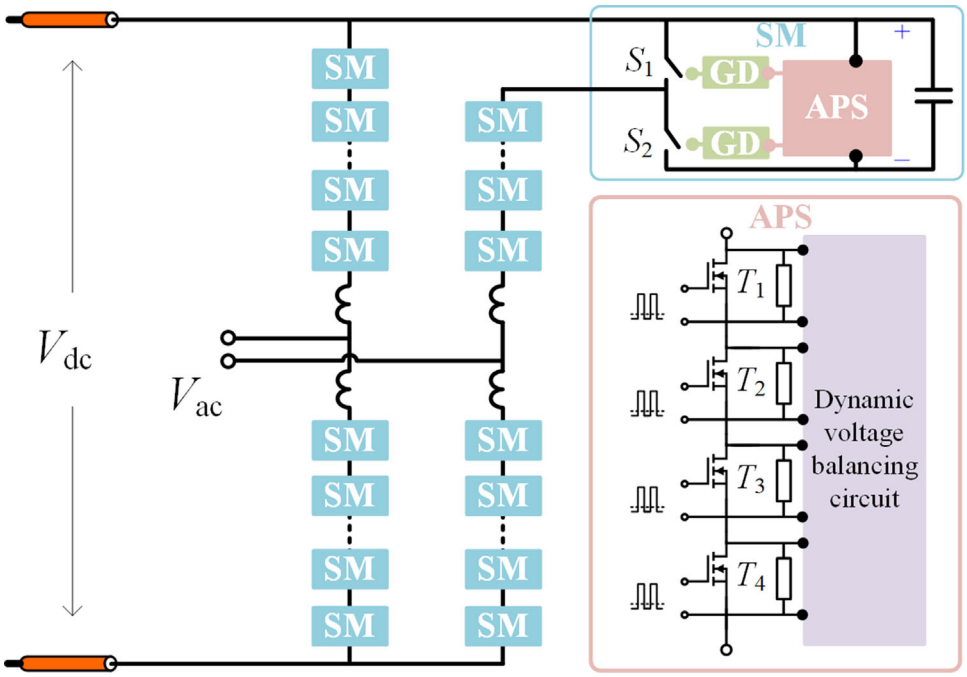

FIGURE 1 The structure of APSs for MMC

flexibility for the adjustments of the driving pulse characteristics including voltage shapes and driving delays, which provides the basic for active voltage balancing methods. For example, active delays adjusting methods [8, 9], active gate voltage synchronization methods [10], active gate voltage and current compensation methods [11–13]. Indeed, aforementioned methods could achieve the goal of voltage balancing, however, at the expense of increasing complexity including more complicated gate loop and power loop design, followed by the greatly increased cost as well, which is contrary to the original intention of low cost if they are employed in high-voltage low-power applications.

Comparatively, using single gate driver is much more cost-efficient, where only one standard gate driver is required to drive the bottom device in the stack and some simple passive components are adopted to drive the upper ones. However, such a way will cause intrinsic switching delays of series-connected devices and induce severe voltage unbalancing [14–17]. Also, some voltage balancing methods have been proposed in the converter design. In [18, 19], well-known resistor-capacitor-diode (RCD) snubbers are adopted for voltage balancing, where the high-loss problem exists as in the conventional way if a fairly balanced voltage sharing is expected. Besides, the gate loop of each device is equipped with an additional power supply, which still increases the cost. In [20], just two small capacitors are in parallel with two serial devices respectively for voltage balancing, but the performance is highly sensitive to the parameters. Once the parameters are chosen in a specific situation, as the power loop voltage varies, they need to be tuned accordingly, otherwise unacceptable voltage unbalancing would occur again.

Therefore, how to enhance the voltage adaptability of single gate driver while not causing much loss remains to be solved. Although the authors in [21] have reach the goal by using the controller together with two compensation loops to adjust the driving speed, it is still a quite complicated design and only for two series-connected SiC MOSFETs. While in [22], a novel snubber structure can balance the voltages with the help of automatic balancing loops, which possesses a good voltage adaptability. However, it adopts conventional gate loop design, and due to its working principle, a complex start-up circuit is also necessary. Therefore, in this paper, an enhanced single gate driven voltage-balanced SiC MOSFET stack topology is proposed by combining the advantages in [21] and [22], which becomes a much more simplified solution. The proposed topology consists of a specifically designed single gate driver that we define as a sequentially lagging single gate driver, and a modified RCD snubber that we define as an automatic voltage balancing RCD^2 circuit. Based on above, its features and advantages are summarized as followed:

1. A good voltage balancing of multiple series connected SiC MOSFETs is achieved, and it is well suitable for the power loop voltage variation, which makes it flexible for converter design.
2. With the automatic voltage balancing RCD^2 circuit rather than the well-known RCD snubbers, the voltage balancing is realized without causing much extra loss.
3. With the concept of single gate driver, only some passive components are equipped with the SiC MOSFET stack, no additional active control is required and the cost is low.

In Section 2, the working principle of proposed single gate driven voltage-balanced SiC MOSFET stack is introduced. In

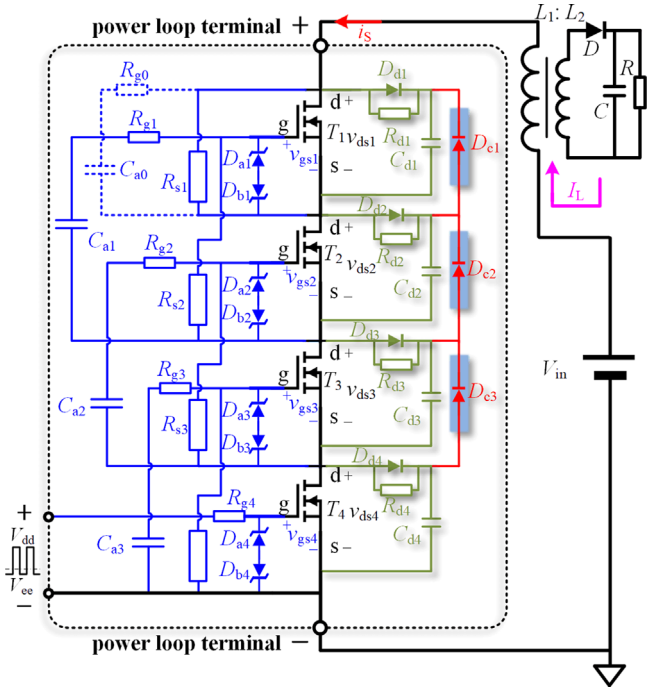

FIGURE 2 The enhanced single gate driven voltage-balanced SiC MOSFET stack topology

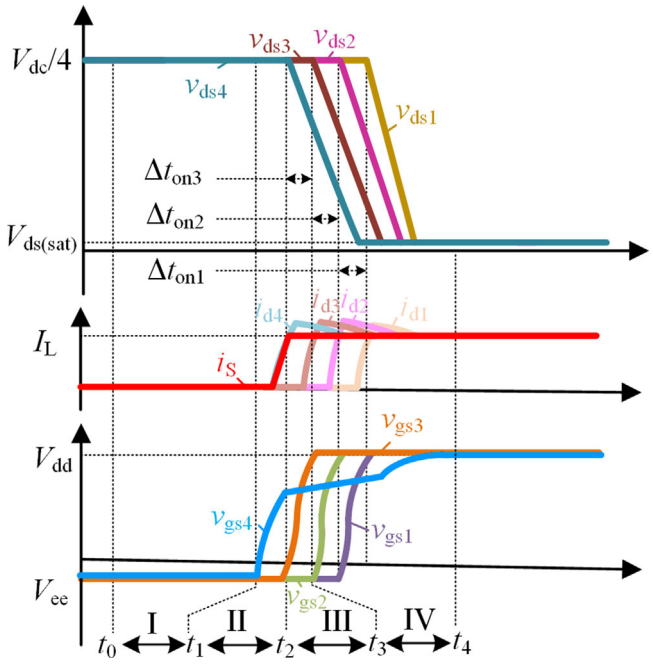

FIGURE 3 Turn-on process of SiC MOSFET stack

Section 3, the parameter selection and design consideration are analysed. In Section 4, the comparison of proposed topology versus RCD method and active delay adjusting method is given to better illustrate its advantages. In Section 4, the proposed topology is used in a typical high-voltage low-power application, auxiliary power supply, and the simulation and experimental results are given. Finally, the conclusion is given in Section 5.

2 | WORKING PRINCIPLE OF PROPOSED SINGLE GATE DRIVEN VOLTAGE-BALANCED SIC MOSFET STACK TOPOLOGY

The SiC MOSFET stack analysed in this paper consists of four series connected SiC MOSFETs T_i (i = 1–4), which is decided by using 1.7 kV/5 A ones to meet 5 kV input voltage requirement of the high-voltage low-power application and considering the margin. Based on it, an enhanced single gate driven voltage-balanced SiC MOSFET stack topology is proposed for the purpose of cost-efficiency, and the typical inductive load is assumed here to conduct the analysis of its working principle. Take its application in a flyback converter as an example, as shown in Figure 2. Apart from the input voltage V_{in}, transformer (L_1:L_2), diode D, capacitor C and load R, the blue part shows the structure of sequential lagging single gate driver, where only the bottom SiC MOSFET requires a standard gate driver, and the upper ones are driven by added coupling capacitors C_{ai} (i = 1–3) between the gate terminal of T_i and the source terminal of its adjacent one. R_{si} (i = 1–4) is the static voltage balancing resistor. R_{gi} (i = 1–4) is the gate resistor. Zener diodes D_{ai} and D_{bi} (i = 1–4) are used for gate protection. The other coloured part shows the automatic voltage balancing RCD[2] circuit for the voltage balancing of drain-source voltage v_{dsi} (i = 1–4) of T_i. Different from the well-known RCD snubber, R_{di} is chosen to be large for loss saving in the combination of resistors R_{di}, capacitors C_{di}, diodes D_{di} (i = 1–4). In order to obtain better voltage balancing performance, diodes D_{ci} (i = 1–3) between snubber capacitors in [22] are applied directly, which benefits from the sequential lagging single gate driver design and provides low impedance loops for automatic balancing of C_{di} (it will be explained later). The turn-on and turn-off processes of SiC MOSFET stack are respectively analysed in following part A and part B, and in order to facilitate the analysis, C_{dsi} in parallel with T_i through D_{di} could be considered as a constant voltage source since it is a large value, which will be further illustrated in part C.

2.1 | Turn-on process of proposed topology

The turn-on process of SiC MOSFET stack could be divided into four stages, named from stage I to stage IV, which is shown in Figure 3.

Stage I [t_0–t_1]: During this stage, the turn-on signal has not been received by the gate driver, and the gate-source voltage v_{gs4} of T_4 is equal to the negative driving voltage V_{ee}. Thus, such a current loop exists as shown in Figure 4a. By properly setting the Zener voltage of D_{bi} and the values of R_{si} [23], v_{gsi} (i = 1–3) of T_i is equal to V_{ee} as well and the drain-source voltages v_{dsi} of T_i are statically balanced. Therefore, the SiC MOSFET stack is in reliable off state.

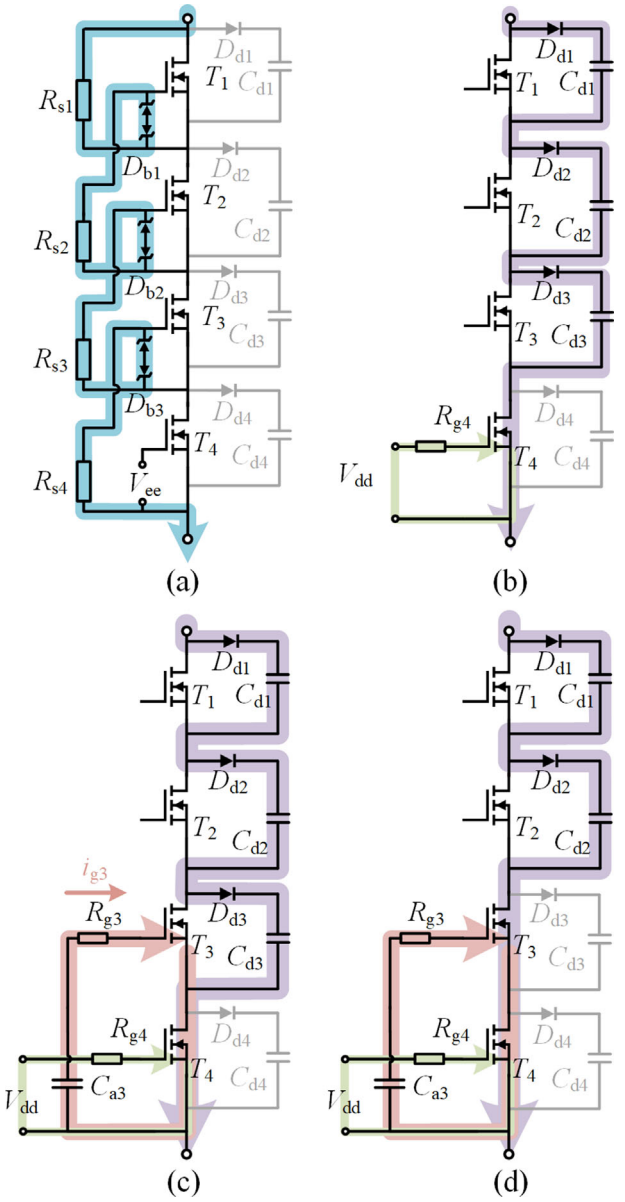

FIGURE 4 Key instant states at (a) t_0, (b) t_1, (c) t_2, (d) t_3

Stage II [t_1–t_2]: at t_1, the driving voltage is changed to V_{dd} since the turn-on signal is received, and v_{gs4} starts to rise from V_{ee}. Once T_4 enters its saturation region, the load current I_L will commutate to the stack from D and i_S flowing through the stack will rise from zero. If no clamping circuit exists, a voltage unbalancing will occur since T_i (i = 1–3) is still in its cutoff region. Instead, here in our design, i_S will flow through C_{di} (i = 1–3) as shown in Figure 4b.

Stage III [t_2–t_3]: After i_S reach I_L at t_2, D starts to withstand the reverse voltage, and v_{ds4} starts to drop, which induces another current loop on the gate side of T_3, as shown in Figure 4c. Therefore, a spike occurs in the drain current i_{d4} of T_4 compared with i_S.

In order to estimate dv_{ds4}/dt, an analysis during this transient is based on the equivalent model of SiC MOSFET, as shown in Figure 5, and such a relation exists:

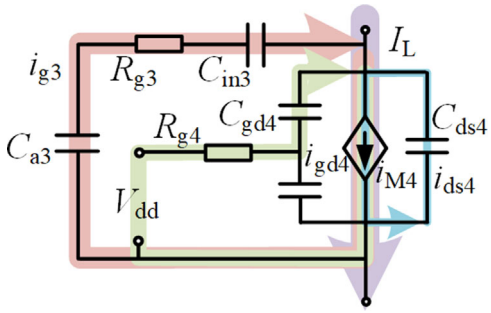

FIGURE 5 Current flowing during switching transient of T_4

$$i_{M4}=i_{ds4}+i_{gd4}+i_{g3}+I_L. \tag{1}$$

where i_{ds4} and i_{gd4} are respectively the currents through drain-source capacitance C_{gd4} and Miller capacitance C_{ds4}, i_{g3} is the gate current flowing through R_{g3}, C_{in3} is the gate capacitance of T_3 and i_{M4} is the channel current of T_4.

By introducing transconductance parameter G_M and threshold voltage V_{th}, the relations are as followed:

$$\begin{cases} i_{M4} = G_M(v_{gs4} - V_{th}), v_{gs4} > V_{th} \\ i_{g3} \approx \dfrac{-dv_{ds4}/dt}{(1/C_{a3} + 1/C_{in3})} \\ i_{gd4}/C_{gd4} \approx i_{ds4}/C_{ds4} = -dv_{ds4}/dt \end{cases}. \tag{2}$$

Combining Equations (1) and (2), dv_{ds4}/dt can be solved as:

$$\frac{dv_{ds4}}{dt} \approx -\frac{G_M(v_{gs4} - V_{th}) - I_L}{C_{gd4} + C_{ds4} + 1/(1/C_{a3} + 1/C_{in3})}. \tag{3}$$

From Equation (2), it is seen that i_{g3} is highly relevant to dv_{ds4}/dt and contributes to the rising of v_{gs3}. By setting the Zener voltage of D_{ai}, v_{gs3} will be clamped at V_{dd} finally. Once T_3 enters the saturation region as well, the current through C_{d3} will commutate to T_3 and cause the rising of drain current i_{d3} of T_3.

Stage IV [t_3–t_4]: At t_3, i_{d3} reached I_L and the SiC MOSFET stack is switched to the state shown in Figure 4d, followed by the dropping of v_{ds3}, which lags Δt_{on3} behind v_{ds4}. With the same manner, the gate loop and power loop of T_i (i = 1–3) are similar with T_4. After Δt_{on2}, v_{ds2} drops as well, followed by v_{ds1} after Δt_{on1}, and $dv_{ds\,i}/dt$ (i = 1–3) could be solved as:

$$\begin{cases} \dfrac{dv_{dsi}}{dt} \approx -\dfrac{G_M(v_{gsi} - V_{th}) - I_L}{C_{gdi} + C_{dsi} + 1/(1/C_{a(i-1)} + 1/C_{in(i-1)})}, \quad i= 2, 3 \\ \dfrac{dv_{ds1}}{dt} \approx -\dfrac{G_M(v_{gs1} - V_{th}) - I_L}{C_{gd1} + C_{ds1}} \end{cases}. \tag{4}$$

In Equation (4), dv_{ds1}/dt of T_1 is higher since one charging branch of its equivalent model is missing (the

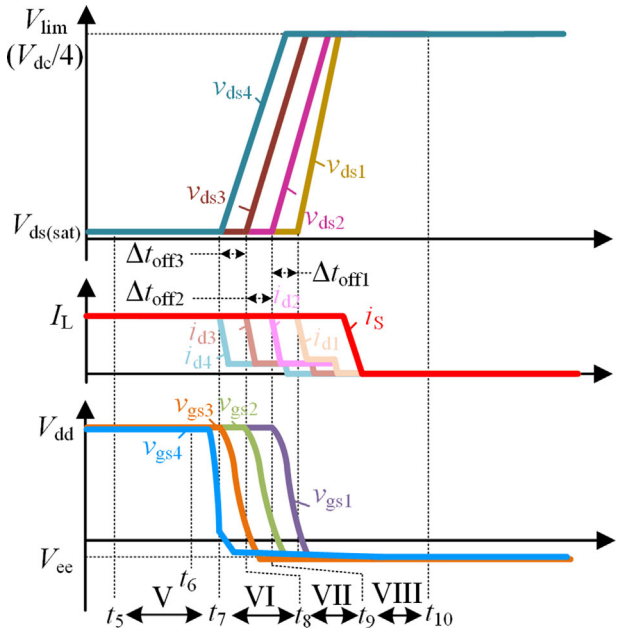

FIGURE 6 Turn-off process of SiC MOSFET stack

resistance-capacitance $R_{g0}C_{a0}$ branch is not included in this section). Comparatively, the falling slopes of v_{ds2}, v_{ds3} and v_{ds4} are similar.

At t_4, I_L has completely flowed through T_i (i = 1–4) and v_{gs4} has reached V_{dd}, which means the ending of turn-on process of SiC MOSFET stack.

2.2 | Turn-off process of proposed topology

The turn-off process of SiC MOSFET stack could be divided into four stages as well, named from stage V to stage VIII, which is shown in Figure 6.

Stage V [t_5–t_7]: At t_5, the SiC MOSFET stack is in on state, which is shown in Figure 7a, and i_S is equal to I_L. Then the gate driver received the turn-off signal at t_6, and the driving voltage is changed from V_{dd} to V_{ee}. Therefore, v_{gs4} starts to decrease.

Stage VI [t_7–t_8]: With the decreasing of v_{gs4}, T_4 enters the saturation region from linear region at t_7, and v_{ds4} starts to rise, which induces the gate side discharging of T_3, as shown in Figure 7b. By setting the Zener voltage of D_{bi}, v_{gs3} will be clamped at V_{ee} finally. In the meantime, the equivalent model during this transient is the same as that in Figure 5, therefore, Equation (3) is still valid here, and dv_{ds4}/dt can be estimated as well.

Stage VII [t_8–t_9]: At t_8, T_3 enters the saturation region as well, and the rising of v_{ds3} lags Δt_{off3} behind v_{ds4}. Similarly, the rising slope of v_{ds3} could be estimated according to Equation (4), and it will induce a current loop on the gate side of T_2. Once v_{ds4} reaches the limiting value V_{lim}, that is, $V_{dc}/4$, i_S will flow through C_{d4} instead of T_4, as shown in Figure 7c. Since C_{d4} could be considered as a voltage source, v_{ds4} will not continue to rise, and thus, the voltage unbalancing is avoided.

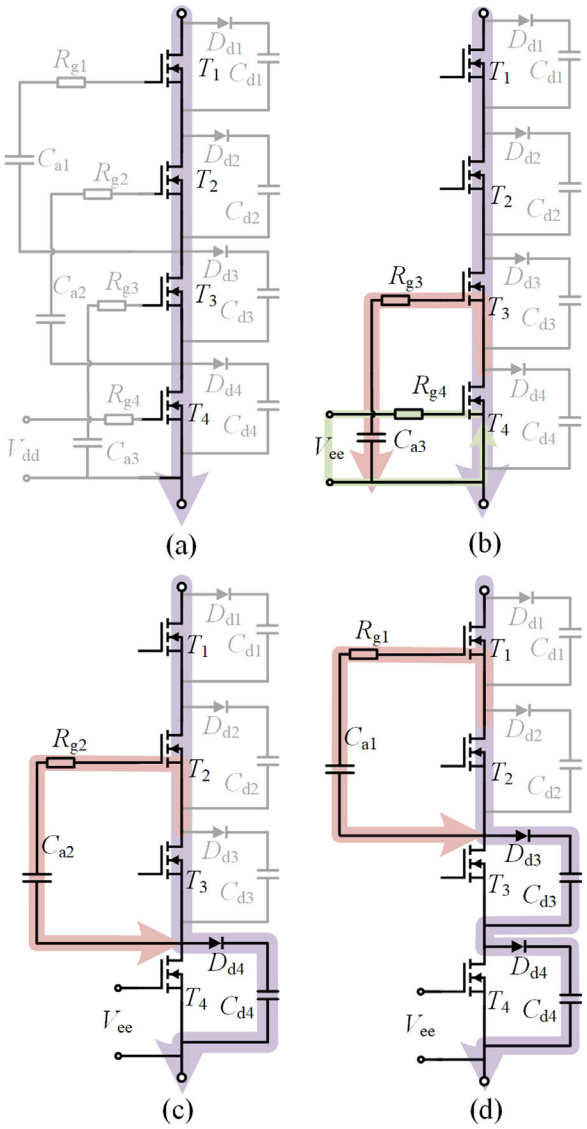

FIGURE 7 Key instant states at (a) t_5, (b) t_7, (c) t_8, (d) t_9

Stage VIII [t_9–t_{10}]: At t_9, v_{ds2} starts to rise which lags Δt_{off2} behind v_{ds3}, and the SiC MOSFET stack is changed to the state shown in Figure 7d. The voltage unbalancing of v_{ds3} is also avoided since it is limited to V_{lim}. After Δt_{off1}, v_{ds1} will start to rise as well, and the rising slopes of v_{ds1} and v_{ds2} could be estimated by Equation (4). Similarly, dv_{ds1}/dt is higher since one discharging branch is missing. Both of them will be limited to V_{lim} as well. Consequently, the voltage balancing of SiC MOSFET stack is well achieved. Finally, the turn-off process of the stack is finished at t_{10}.

2.3 | The basic for voltage balancing

Through the above analysis, the voltages v_{dsi} (i = 1–4) of the SiC MOSFET stack are well balanced during both the turn-on and turn-off processes. As mentioned, it is based on

C_{di} (i = 1–4) considered as a constant voltage source, and in this part, the explanation will be given.

Since the stack is applied in high-voltage low-power applications, I_L is very small, and the magnitude of dv_{dsi}/dt during turn-on process is much larger than that of dv_{dsi}/dt during turn-off process according to Equations (3) and (4). Consequently, Δt_{offi} (i = 1–3) is much larger than Δt_{oni}, which could be concluded by following relationships:

$$\begin{cases} \Delta t_{oni} \approx \dfrac{C_{ini}(V_{dd}-V_{ee})}{i_{g_i}} \approx \dfrac{C_{ini}(V_{ee}-V_{dd})(1/C_{ai}+1/C_{ini})}{dv_{ds(i+1)}/dt} \\ \Delta t_{offi} \approx \dfrac{C_{ini}(V_{ee}-V_{dd})}{i_{g_i}} \approx \dfrac{C_{ini}(V_{dd}-V_{ee})(1/C_{ai}+1/C_{ini})}{dv_{ds(i+1)}/dt} \end{cases}, i = 1 \sim 3 \tag{5}$$

As the stack is continuously switched on and off in the application, the energy in C_{di} will be gradually accumulated. As illustrated in part A and B, the energy ΔE_i accumulated by C_{di} during one switching cycle is highly relevant to Δt_{offi} and Δt_{offi}, and could be expressed as:

$$\begin{cases} \Delta E_1 = V_{lim} I_{L(on)} (\Delta t_{on1} + \Delta t_{on2} + \Delta t_{on3}) \\ \Delta E_2 = V_{lim} I_{L(on)} (\Delta t_{on1} + \Delta t_{on2}) + V_{lim} I_{L(off)} \Delta t_{off3} \\ \Delta E_3 = V_{lim} I_{L(on)} \Delta t_{on1} + V_{lim} I_{L(off)} (\Delta t_{off2} + \Delta t_{off3}) \\ \Delta E_4 = V_{lim} I_{L(off)} (\Delta t_{off1} + \Delta t_{off2} + \Delta t_{off3}) \end{cases}. \tag{6}$$

where $I_{L(on)}$ and $I_{L(off)}$ are distinguished load currents. Rather than both equal to I_L, they are different in actual applications for energy consuming and $I_{L(off)} > I_{L(on)}$. From (6), since Δt_{offi} is much larger than Δt_{oni} as well, it is concluded that $\Delta E_4 > \Delta E_3 > \Delta E_2 > \Delta E_1$, which provides the working basic of automatic balancing RCD circuit.

As shown in Figure 2, D_{ci} (i = 1–3) and R_{di} (i = 1–4) are further added together with C_{di} and D_{di} to construct such an automatic balancing RCD[2] circuit. Therefore, during turn-on process of the SiC MOSFET stack, additional current loops are formed, as shown in Figure 8a. Since C_{d4} accumulates the most energy, once the voltage v_{cd4} across C_{d4} is larger than v_{cd3} across C_{ds3}, D_{c3} will be conducted during the on state of T_4, and thus, v_{cd4} and v_{cd3} are equal again. With the same manner, v_{cdi} (i = 1–4) across C_{di} will be all equal, which makes it easy to select R_{di}, whose function is to consume ΔE_i. In this way, v_{cdi} across C_{di} could be maintained at V_{lim} since accumulated ΔE_i is released during every switching cycle. Therefore, C_{di} could be considered as a constant voltage source, and the stack works as expected.

It is noticed that, in the well-known RCD snubbers, the resistors would be chosen very small to slow down the switching transients of SiC MOSFETs in order to well balance the voltages. This way would cause a lot of extra losses and that is why passive methods are not preferred compared with active control method. Instead, in this proposed topology, R_{di} is only required to consume ΔE_i which is small according to (6), and thus, R_{di} is chosen very large, which will be illustrated in following Section 3.

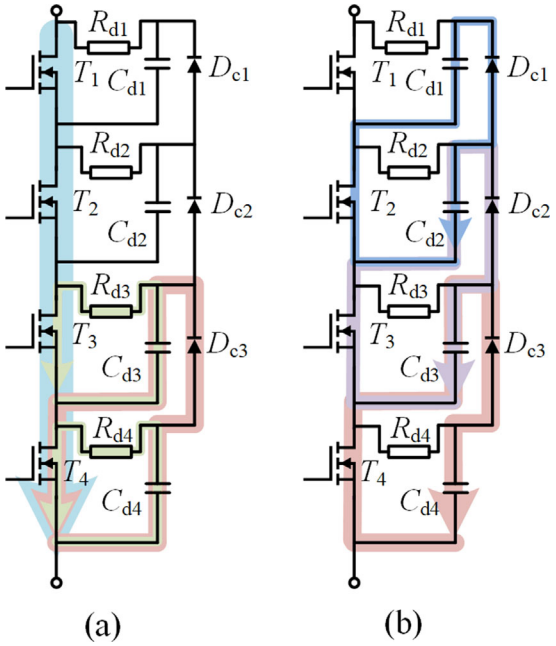

FIGURE 8 (a) Automatic balancing process of SiC MOSFET stack (b) non-ideal current loops during turn-off process of SiC MOSFET stack

3 | PARAMETER SELECTION AND DESIGN CONSIDERATION

3.1 | Capacitors and resistors selection

In actual applications, C_{di} could not be chosen as large as possible since it will cause a large volume as well, and thus, a design criterion should be given. Therefore, when v_{ds4} reaches V_{lim}, rather than clamping v_{ds4}, C_{d4} with a large value will greatly slow its rising. By adding a C_{d4} branch to the model in Figure 5, dv_{ds4}/dt could be expressed as:

$$\frac{dv_{ds4}}{dt} \approx \frac{I_{L(off)}}{C_{d4}+C_{gd4}+C_{ds4}+1/(1/C_{a3}+1/C_{in3})} \approx \frac{I_{L(off)}}{C_{d4}}. \tag{7}$$

And then, after a duration of $t_{sum} = \Delta t_{off3} + \Delta t_{off2} + \Delta t_{off1}$, the further increment of v_{ds4} is expected to be a small value ΔV, which causes the voltage unbalancing and should be defined here in our design. It could be described as followed:

$$\Delta V = \frac{dv_{ds4}}{dt} t_{sum} \approx \frac{I_{L(off)} t_{sum}}{C_{d4}}. \tag{8}$$

In (8), when ΔV is given and $I_{L(off)} t_{sum}$ is estimated, C_{d4} together with the same C_{di} (i = 1–3) could be selected.

As for the selection of R_{di} (i = 1–4), in Figure 8, the equivalent discharging model of $R_{di}C_{di}$ during on state is a natural response of the RC circuit, which could be further simplified since the voltage drop of v_{Cdi} (i = 1–4) is relatively very small. With the principle of that v_{Cdi} is equal and back to be V_{lim} after

one switching cycle, such a relation exists as followed:

$$\frac{C_{di}[(\Delta V + V_{lim})^2 - V_{lim}{}^2]}{8} \approx \frac{T_{on} V_{lim}{}^2}{R_{di}}, i = 1 \sim 4. \quad (9)$$

where T_{on} is the on time of one switching cycle.

In (9), when V_{lim} is given and other parameters are confirmed, R_{di} (i = 1–4) could be selected as well.

3.2 | Influence of non-ideal factors

The above analysis is based on ideal situations, which provides the guidance. Actually, the components are non-ideal in real applications, which must be considered. During the selection of R_{di}, some components such as non-ideal diodes do lead to other paths of energy consumption. Consequently, R_{di} could be chosen even larger. Apart from that, two major influences are summarized:

1. Since D_{ci} (i = 1–3) needs reverse recovery during the turn-off process of SiC MOSFET stack, the rising of v_{dsi} (i = 2–4) will induce reverse current loops, as shown in Figure 8b. Therefore, another discharging loop should be added to the model in Figure 5 during turn-off transient of T_i (i = 2–4), and Equations (3) and (4) should be amended. In this way, v_{dsi}/dt (i = 1–3) will be smaller while v_{ds1}/dt remains unchanged, which may cause v_{ds1} rises to V_{lim} earlier than v_{ds2}, that is, Δt_{off1} is a negative value.
2. Since the parasitic capacitances of transformer and D exist in real applications, the high dv/dt during turn-on process of the SiC MOSFET stack will induce an extra current to flow through the stack, which may cause $I_{L(on)} > I_{L(off)}$.

According to (6), both of above two influences could lead to the inconsistency of the conclusion $\Delta E_4 > \Delta E_3 > \Delta E_2 > \Delta E_1$, and the voltage balancing of proposed topology would be influenced. Therefore, an additional $R_{g0}C_{a0}$ branch is in parallel with T_1, as shown in the dash line in Figure 2. Such a way makes v_{ds4}/dt smaller, so that $\Delta E_4 > \Delta E_3 > \Delta E_2 > \Delta E_1$ is assured and good voltage balancing performance is realized.

4 | COMPARISON OF PROPOSED TOPOLOGY WITH RCD METHOD AND ACTIVE DELAY ADJUSTING METHOD

In order to better illustrate the advantages of proposed single gate driven voltage balanced SiC MOSFET stack, taking the flyback converter in Figure 2 as the common main topology and the parameters listed in Table 1 (explained in Section 5), its experimental comparison versus RCD snubber method and active delay adjusting method is given in this section.

As mentioned, in the conventional way T_i (i = 1–4) in the stack requires an independent driving pulse, which means four groups of isolated power supply and driving chip with optic fibre isolation are needed [4]. Although the gate loops are designed to be identical, voltage unbalancing still occurs. In order to balance the voltages, the well-known RCD snubber can be equipped with T_i, as shown in Figure 9a. From the experimental results in Figure 10a, it is found that, with R_{di} = 550 Ω and C_{di} = 100 nF (i = 1–4), the voltage unbalancing of the stack is achieved within 3.5% under V_{in} = 1.6 kV (the voltage unbalancing degree is defined as the maximum difference of v_{dsi} and v_{dsj} (i,j = 1–4) divided by $V_{in}/4$). However, such an acceptable voltage balancing performance is obtained at the cost of high loss, which will be analysed later. And that is why the pure RCD method is not suggested for the stack.

TABLE 1 Parameters of components

Name	Parameter
T_i (i = 1–4)	C2M1000170J (1.7 kV/5 A)
D_{ai} (i = 1–4)	PTZ18B (18 V)
D_{bi} (i = 1–4)	TDZ6_2B (6.2 V)
D_{ci} (i = 1–3), D_{di} (i = 1–4)	C5D05170H (1.7 kV/5 A)
R_{si} (i = 1–4)	500 kΩ
R_{gi} (i = 1–4)	20 Ω
C_{ai} (i = 1–3)	47 pF
C_{di} (i = 1–4)	50 nF

Therefore, active voltage balancing methods are preferred. Such a conventional gate driver configuration gives sufficient flexibility for the adjustments of gate loops, which provides the basic of active methods. Here the typical active delay adjusting method which realizes voltage balancing by adjusting driving delays Δt_{di} (i = 1–4) is analysed. Besides, T_i is equipped with a low-loss snubber (R_{di} = 50 kΩ, and C_{di} = 100 nF, i = 1–4) to absorb the leakage energy of the transformer, as shown in Figure 9b. From the results in Figure 10b, the voltage unbalancing of the stack under V_{in} = 1.6 kV is achieved within 2%. However, complex sampling circuits such as ADCs are necessary to provide feedbacks, then the controller properly adjust Δt_{di} for voltage balancing [7, 8]. Obviously, such a complex gate loop and power loop design would greatly increase the total cost.

Comparatively, in the proposed method, with the concept of single gate driver, the gate driver design becomes much easier, and just one group is needed (which will be further substituted by a single chip in the next section), as shown in Figure 9c. With automatic voltage balancing RCD^2 circuit to cooperate with the sequential lagging single gate driver, the voltage unbalancing of the stack under V_{in} = 1.6 kV is achieved within 0.1%, which is even smaller than the active one, as shown in Figure 10c. Here for the current measuring purpose, a long wire is placed at the drain electrode of T_i. which causes the additional loss and influences the automatic balancing. Therefore, a 18 Ω resistor is in series with D_{ci}, which is not included in the next section.

Next, the switching loss of T_i and key energy-consuming component R_{di} with above three methods are compared, as shown in Figure 11. With the RCD snubber method, as shown in Figure 11a, R_{di} loss is severe since C is discharging though R_{di}

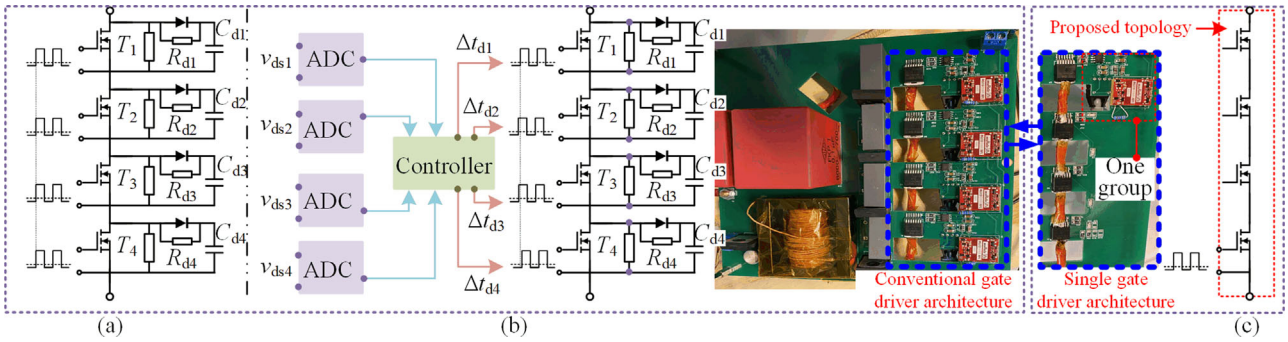

FIGURE 9 Schematic and prototype with (a) RCD snubber method (b) active delay adjusting method 5c) proposed method

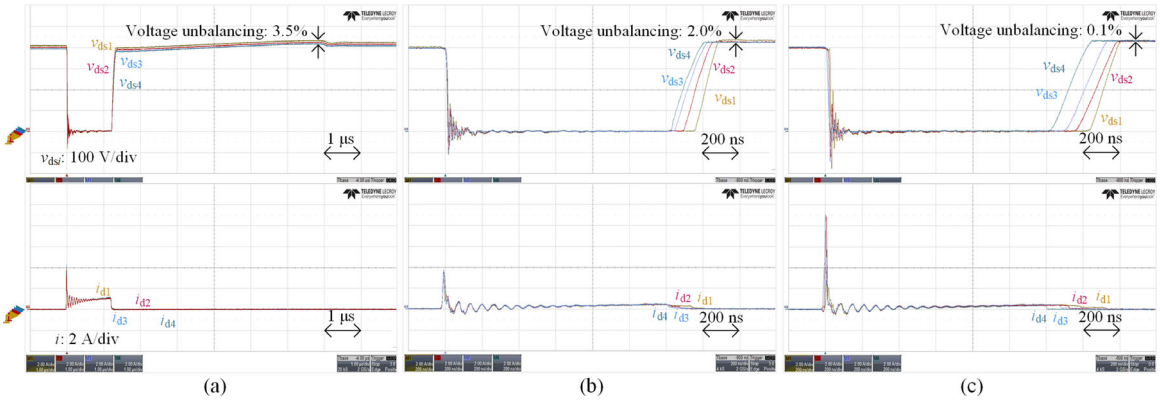

FIGURE 10 Voltage sharing and currents of SiC MOSFET stack with (a) RCD snubber method (b) active delay adjusting method (c) proposed method

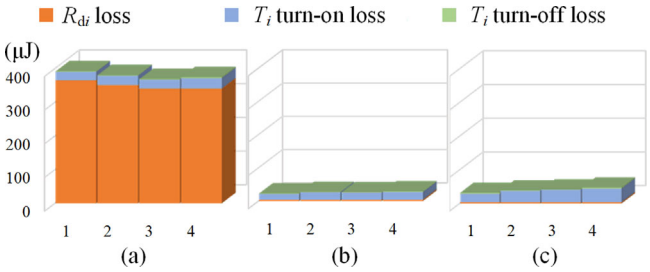

FIGURE 11 Switching loss distribution with (a) RCD snubber method (b) active delay adjusting method (c) proposed method

during the whole on time, as a higher current following through T_i can be observed in Figure 10a. With the active delay adjusting method, the total loss is reduced by 93.07% compared with RCD snubber method, as shown in Figure 11b. Besides, four groups of T_i turn-on loss, turn-off loss and R_{di} loss are almost the same. With the proposed method, the total loss is reduced by 89.45% compared with RCD snubber method, as shown in Figure 11c. And it is found that turn-on losses of T_2, T_3 and T_4 are similar while that of T_1 is smaller. It is because the automatic balancing process causes the extra turn-on loss of T_i ($i = 2$–4), as a lager current overshoot can be observed in Figure 10c. Despite of more loss of proposed topology compared with active delay adjusting method, the extra loss is not much, and it is acceptable in high-voltage low-power applications. Comparatively, the advantages of the proposed topology are, both the gate loop and power loop designs are greatly simplified, therefore, the cost is low.

5 | SIMULATION AND EXPERIMENTAL RESULTS IN AN APS APPLICATION USING PROPOSED TOPOLOGY

After above, the performance of proposed single gate driven SiC MOSFET stack is further verified in a typical high-voltage low-power application, APS, where a flyback converter is also the main topology, as shown in Figure 12. In such a low-power APS, discontinuous current mode (DCM) is a preferred choice since zero current switching (ZCS) is realized during MOSFETs turn-on and diode turn-off processes. Therefore, in our design, LT3798 is chosen as the offline controller [24]. Since the output side of LT3798 is +10 V/0 V, in order to make it suitable for SiC MOSFET, a pulse boost circuit is applied as shown in the grey part, and the driving voltage V_{dd}/V_{ee} of T_4 is +20 V/0 V. Besides, the parts of controller powering, DCM detecting, voltage sensing and current sensing shown in other colours are designed for its normal operation.

The LTspice simulation models of key components in this APS are acquired, including T_i, D_{ai}, D_{bi}, D_{ci}, D_{di}, LT3798 and its peripheral devices, which makes the simulation results close

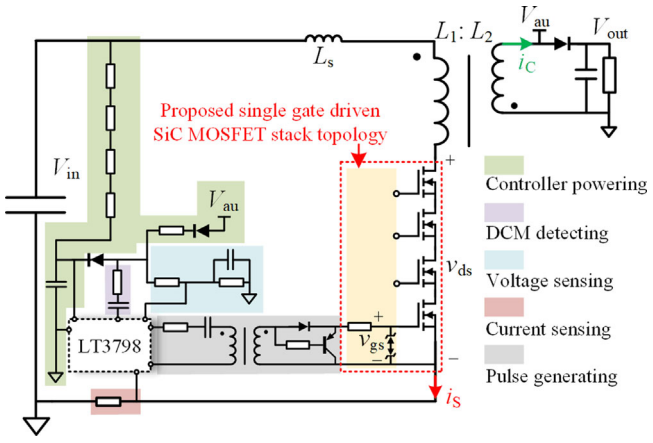

FIGURE 12 APS diagram using proposed SiC MOSFET topology

to the experimental ones, and thus, some simulation results could be reliable. With the aid of simulation and theoretical analysis, the parameters of key components are chosen and listed in Table 1. Based on above, the testing platform is built and the photograph of APS is shown in Figure 13.

5.1 | Performance of SiC MOSFET stack

In the simulations, under the condition of $V_{in} = 2$ kV and the expected output voltage $V_{out} = 24$ V, the voltage waveforms of SiC MOSFET stack during one switching cycle is given in Figure 14. When the secondary current i_C decreases to zero during a switching cycle, D is not conducted and the voltage across the secondary winding starts to oscillate from the parasitic capacitance and the magnetizing inductance of the transformer. Therefore, several cycles of big ringing drain-source voltage v_{ds} of the stack occur. For the purpose of minimizing energy loss, LT3798 waits the ringing v_{ds} to reach its minimum value with the help of DCM detector and then turns back on the stack. It is seen that v_{dsi} ($i = 1$–4) suddenly drops from the valley of waveform to zero, and rises to the limiting value 557 V after a while. During this process, as analysed, the voltage balancing of four SiC MOSFETs is good. However, turn-off and DCM cause oscillation of v_{dsi}, which induces spikes of v_{gsi} ($i = 1$–3). Also, the greater the stray inductance of power loop is, the greater the oscillation and spike will be. Therefore, D_{bi} is required to generate a negative voltage to avoid false turn-on.

When output power P_o is 12 W, the overall performance of APS and SiC MOSFET stack is shown in Figure 15. It is seen that V_{out} fluctuates in a small range around 24 V and the peak value of i_S is 500 mA during every switching cycle. Due to the adjusting process of controller, the turn-on timing of every switching cycle may vary a bit, and one of the cycles is enlarged and displayed in the bottom. It is observed that during turn-on process v_{ds4} drops firstly, followed by v_{ds3} after 10 ns, v_{ds3} followed by v_{ds2} after 9 ns and v_{ds2} followed by v_{ds1} after 5 ns. Similarly, during turn-off process, the rising delay of v_{ds3} compared to v_{ds4} is 147 ns, 106 ns delay of v_{ds2} compared to v_{ds3} and 87 ns delay of v_{ds1} compared to v_{ds2}. Thanks to the automatic balancing RCD[2] circuit, the voltage balancing caused by those delays is eliminated and extra loss is low since R_{di} is 50 kΩ. Consequently, it is concluded that the voltage balancing of SiC MOSFET stack is well achieved.

In the experiments, the parameter setting is the same as that in the simulations. Under $V_{in} = 2$ kV, expected $V_{out} = 24$ V and $P_o = 12$ W, the performance of APS is shown in Figure 16. It is seen that V_{out} is 24 V, the peak value of i_S is 500 mA, and v_{ds} suddenly drops from the valley point, which is consistent with the simulations. The oscillation of i_L is caused by the leakage inductance L_s and the parasitic capacitances of transformer and D, which could be alleviated by adding RC snubber for D.

In order to ensure the accuracy of voltage measurement, four passive high-voltage probes are adopted to measure v_{dsi} ($i = 1$–4), and the results are shown in Figure 17. v_{dsi} could not be shown directly since the probes share one common ground, and the waveforms from the bottom to the top are v_{ds4}, $v_{ds3}+v_{ds4}$, $v_{ds2}+v_{ds3}+v_{ds4}$, $v_{ds1}+v_{ds2}+v_{ds3}+v_{ds4}$. It is observed that, during the steady state of APS, the voltage balancing of the SiC MOSFET stack is the same in every cycle. Besides, it is found that the steady voltages are well balanced by deriving v_{dsi} ($i = 1$–4) using the data in Figure 17. However, it is worth noticing that, due to the difference between the probes and the influence of the ground wires of four passive high-voltage probes, the voltage transient of v_{dsi} ($i = 1$–4) is not accurate if v_{dsi} is directly obtained by mathematical calculations using the original data in Figure 17.

Therefore, the enlarged view of v_{ds4}, $v_{ds3}+v_{ds4}$, $v_{ds2}+v_{ds3}+v_{ds4}$, $v_{ds1}+v_{ds2}+v_{ds3}+v_{ds4}$ is obtained by using the same probe in four experiments shown in the bottom of Figure 17. Based on it, the voltage balancing performance of SiC MOSFET stack is shown in Figure 18. It is observed that, during turn-on process, v_{ds4} drops firstly, followed by v_{ds3} after 7 ns, v_{ds3} followed by v_{ds2} after 5.5 ns and v_{ds2} followed by v_{ds1} after another 4 ns. During turn-off process, v_{ds4} rises firstly, followed by v_{ds3} after 120 ns, v_{ds3} followed by v_{ds2} after 80 ns, v_{ds2} followed by v_{ds1} after 80 ns, and the voltages are limited at 560 V. Compared to simulations, despite the delays are slightly different which is caused by device parameters spread in experiments, the voltage transients are similar and good voltage balancing performance is consistent.

5.2 | Voltage sharing during input and output transients

Additionally, the voltage sharing of SiC MOSFET stack during some transient states of APS is shown in order to better demonstrate the advantages of the proposed single gate driven SiC MOSFET stack topology.

Figure 19 gives the voltage sharing of SiC MOSFET stack during input voltage transient. It is seen that V_{in} is gradually decreased from 2 kV to 1.6 kV, and then increased back to 2 kV. During this process, the voltages of SiC MOSFETs in the stack are always well balanced. Besides, Figure 20 gives the voltage sharing of SiC MOSFET stack during output load transient. P_o is 12 W from the beginning state, and voltage balancing is well

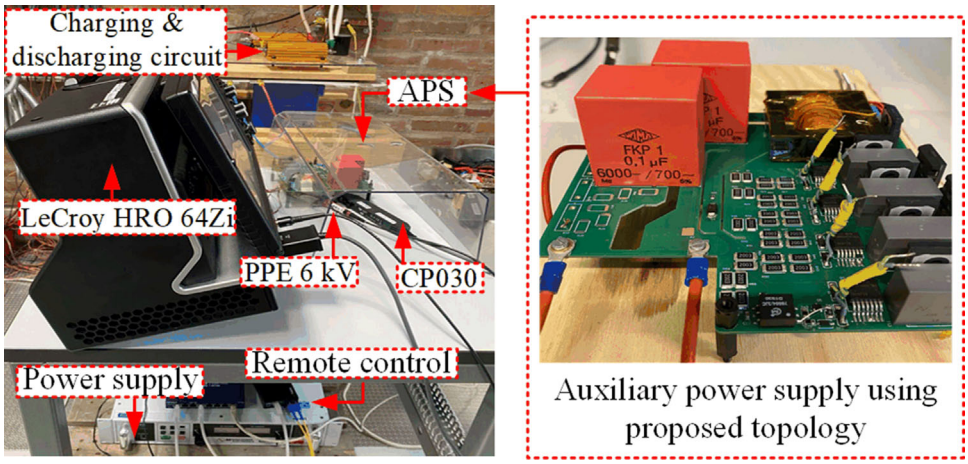

FIGURE 13 Photograph of APS using proposed single gate driver

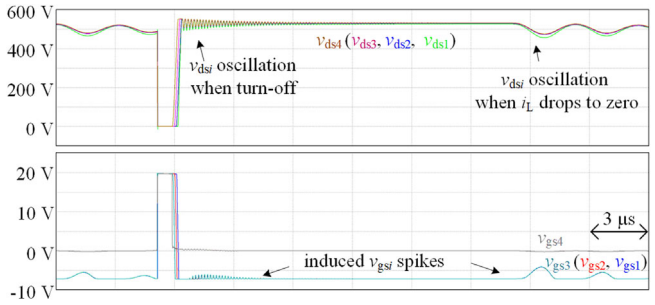

FIGURE 14 One cycle performance of SiC MOSFET stack in simulations

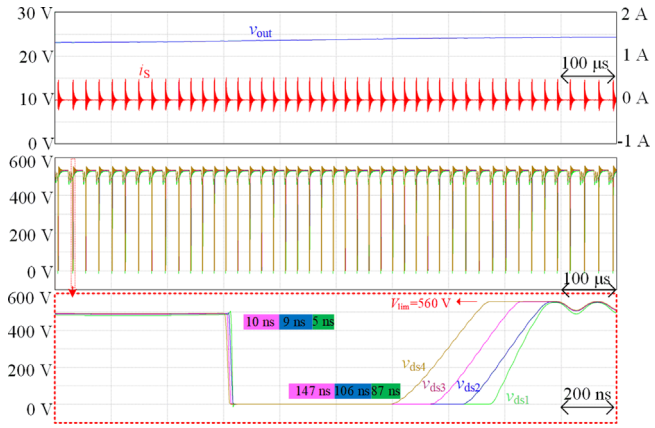

FIGURE 15 Overall performance of APS and the stack in simulations

achieved. After a while, P_o is suddenly decreased to 6 W, and the switching frequency becomes lower due to the adjustment of LT3798 for lower output power. As observed, the voltages are still well balanced. Then, P_o is suddenly increased to 12 W again, and the frequency is back to higher and good voltage balancing is seen. Therefore, both the circumstances verify the good voltage balancing performance of proposed single gate driven SiC MOSFET stack.

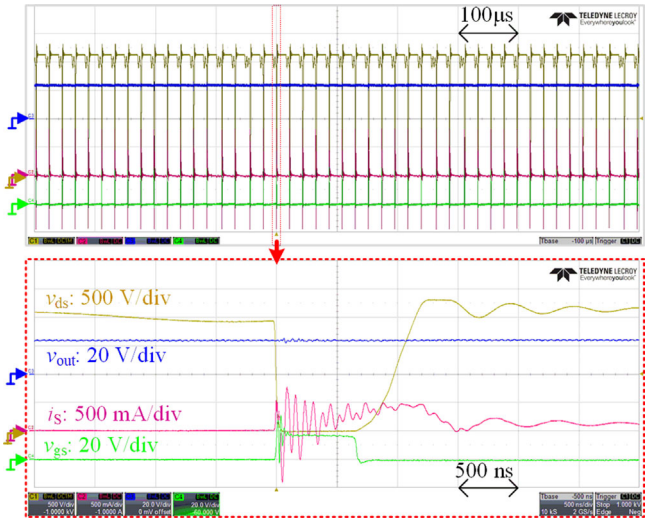

FIGURE 16 Overall performance of APS in experiments

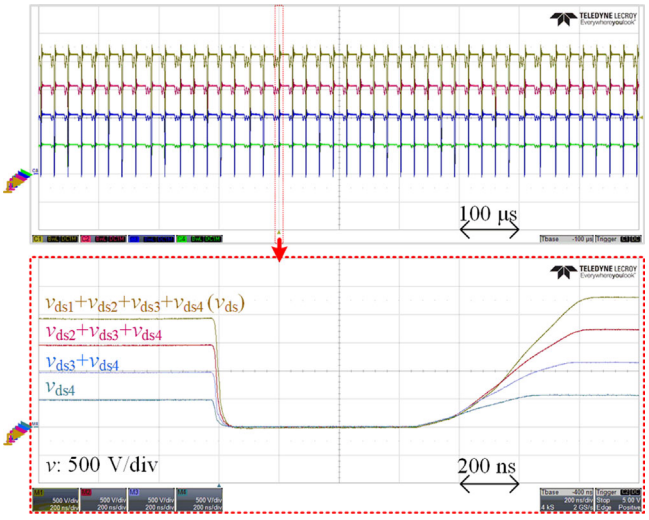

FIGURE 17 Overall performance of SiC MOSFET stack in experiments

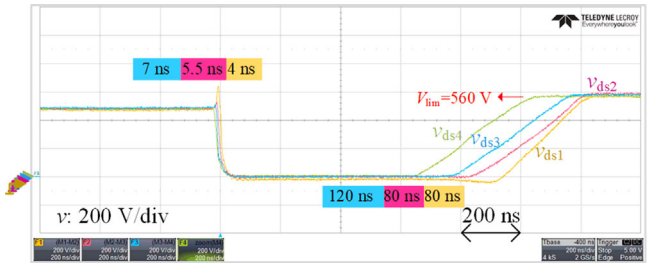

FIGURE 18 Detailed voltage balancing of SiC MOSFETs in experiments

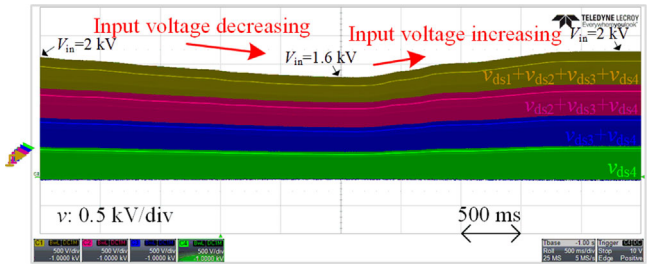

FIGURE 19 Voltage sharing during input voltage transient

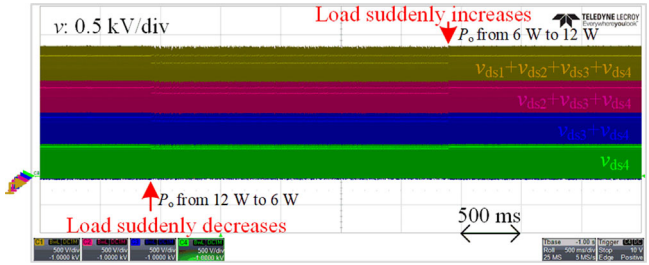

FIGURE 20 Voltage sharing during output load transient

5.3 | Voltage balancing robustness to voltage variation

In order to verify the voltage balancing robustness to voltage variation of SiC MOSFET stack, under expected V_{out} = 24 V and P_o = 12 W, V_{in} is gradually increased from 2 kV to 5 kV without changing any circuit parameter. It is found that, a slight voltage unbalancing could be gradually observed as V_{in} increasing, which will be illustrated in the case of maximum V_{in} (5 kV) following.

Figure 21 gives the overall performance of SiC MOSFET stack when V_{in} = 5 kV. It is seen that, because of the closed-loop control of LT3798, the frequency becomes changing, and the on time becomes less from the enlarged view of one switching cycle shown in the bottom. In every switching cycle, the voltage sharing of SiC MOSFET stack is the same, however, a slightly voltage unbalancing of T_1 occurs.

In order to facilitate the observation, with mathematical calculation using the data in Figure 21, the voltage sharing of v_{dsi} (i = 1–4) in the SiC MOSFET stack is shown in Figure 22. It is found that the voltage balancing of v_{ds2}, v_{ds3} and v_{ds4} is good, but v_{ds1} is slightly higher than others. It is consistent with the

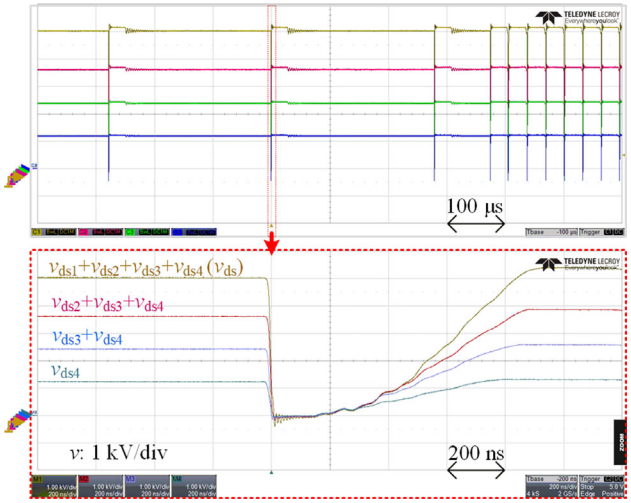

FIGURE 21 Overall performance of SiC MOSFET stack under V_{in} = 5 kV

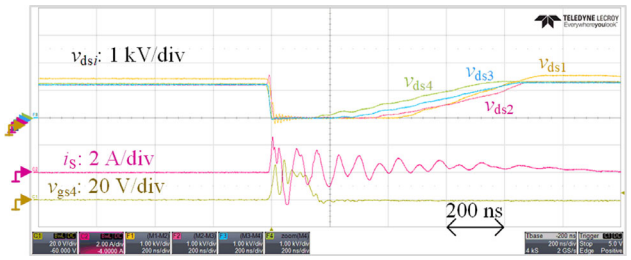

FIGURE 22 Voltage sharing of SiC MOSFETs when C_{a0} = 47 pF

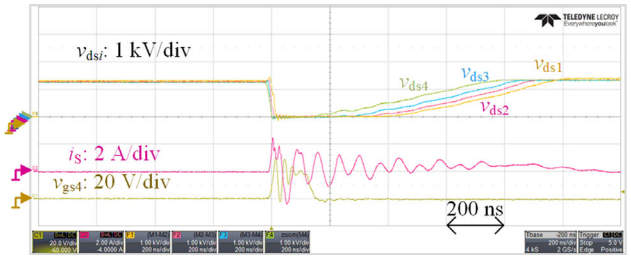

FIGURE 23 Voltage sharing of SiC MOSFETs when C_{a0} = 94 pF

theoretical analysis in Section 3: (1) As the voltage increasing, the reverse recovery of D_{ci} (i = 1–3) becomes more obvious, which makes the rising slope of v_{dsi} (i = 2–4) slower than that of v_{ds1}. (2) The parasitic capacitances of a real transformer and the reverse recovery of diode cause a current flowing into the SiC MOSFET stack during turn-on transient. As the voltage increasing, higher dv/dt during turn-on transient induces higher current, which can be observed in Figures 16 and 22 where the current spike of i_S during turn-on when V_{in} = 5 kV is much higher than that when V_{in} = 2 kV. In addition, the high-voltage probes for measurement still bring some extra parallel capacitances, which influences the voltage balancing as well.

In order to eliminate the slight voltage unbalancing, C_{a0} could be higher, and Figure 23 shows the voltage sharing of

v_{dsi} (i = 1–4) when C_{a0} is increased to 94 pF. Compared with Figure 22 when C_{a0} = 47 pF, it is seen that the rising slope of v_{ds1} becomes smaller and good voltage balancing is obtained. It should be noticed that, it is compatible with lower voltage levels, which means once C_{a0} is chosen by simulation under a maximum voltage level, C_{a0} does not need to be adjusted again. In the meantime, the *dv/dt* during turn-off process is decreased, which becomes a considerable limitation if the frequency needs to be increased.

6 | CONCLUSION

In this paper, a single gate driven voltage-balanced SiC MOSFET stack topology is proposed and illustrated, which is suitable for high-voltage low-power applications. And then, the parameters selection and design consideration are analysed. Compared with the well-known RCD method, the active delay adjusting method and the proposed topology can reduce the loss by 93.07% and 89.45%, respectively. Through the simulations and experiments of an APS application using proposed topology, the good voltage balancing performance of four series connected 1.7 kV/5 A SiC MOSFETs is verified from 2 to 5 kV. Simple structure, no active control and low cost are the greatest advantages of proposed topology. However, limited by the operation principle, it is not suitable for high-voltage high-power applications, and thus the corresponding improvement will be focused on in future work.

CONFLICT OF INTEREST

No

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