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DEMONSTRATION OF 10 KV SILICON CARBIDE POWER SEMICONDUCTOR TECHNOLOGY IN MEDIUM VOLTAGE POWER CONVERSION

BY
DIPEN NARENDRA DALAL

DISSERTATION SUBMITTED 2021

AALBORG UNIVERSITY
DENMARK

Demonstration of 10 kV Silicon Carbide Power Semiconductor Technology in Medium Voltage Power Conversion

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To my parents...

Abstract

In present-day electricity networks, power electronics is widely employed or one can say “omnipresent” as an enabling technology for the conversion and control of electric power at generation, transmission, distribution and consumer end. At the consumer end, industrial sector constitutes the single largest share in the global electric energy consumption. A significant portion of electric energy in the industrial sector is consumed by medium voltage motor drive systems, that often utilize high power (375 kW – 10,000 kW), medium voltage (1 kV – 10 kV) power electronic converters. At the distribution end, high power medium voltage converters are used for grid support functionalities. At generation end, penetration of renewable energy sources such as photovoltaics and wind with their increasing power generation capabilities, demand for medium voltage power electronics which can offer potential benefits in terms of system level efficiency gains and reduced levelized cost of energy production.

Power semiconductor devices constitute the key building block of modern power electronic converters. Commercial high power medium voltage converters utilize Silicon (Si) based power semiconductor devices, which has evolved as a mature technology and dominated power electronics industry for the past years. With Si based power semiconductor devices reaching their theoretical limits of performance, newly emerging Silicon Carbide (SiC) based wide band gap (WBG) devices are foreseen as a likely alternative to Si based devices. The SiC based power semiconductor devices, with their smaller size, high blocking voltage capability, faster switching speed and high temperature withstand capability offer significant benefits to power electronic converters in terms of simplification of power converter topology with increased efficiency and power density.

This PhD thesis demonstrates 10 kV SiC power semiconductor devices in medium voltage power conversion applications. The high rate of change of voltage ($\mathrm{d}v/\mathrm{d}t$) in case of SiC Metal Oxide Field Effect Transistor (MOSFET) due to the medium voltage levels and fast switching transient requires careful consideration of electrical parasitics. Especially parasitic capacitive couplings to limit the displacement currents during the switching transients that can adversely impact electromagnetic interference and compatibility as well as switching performance for the power electronic converter. In particular, parasitic

capacitive couplings within the power modules, as well as external interfacing circuits such as gate drivers and passive components. The PhD thesis begins with introducing state of the art and 10 kV half-bridge SiC MOSFET power modules utilised in this research work. Thereafter, a gate driver with high voltage isolation and a very low coupling capacitance (< 3 pF) is presented. The main contribution of the PhD thesis lays in investigating the power module parasitic capacitance induced displacement current path and its impact on the switching energy dissipation. By solving scientific challenges and implementing mitigation techniques, to lessen the impact of high $\mathrm{d}v/\mathrm{d}t$ induced displacement currents on the half-bridge power module and circuits interfacing power modules, a 50 kVA, 4.16 kV rated medium voltage power stack demonstrator is designed, built and experimentally validated close to its intended operating condition. For designed medium voltage power stack, efficiency higher than 99% is inferred from the converter measurements in a DC fed three phase back-to-back regenerative test setup. The PhD thesis concludes by summarizing the research and the contemplated future work.

Dansk resumé

Effektelektronik er brugt i vid udstrækning i det moderne elektriske system. Man kan endda sige det er en allestedsnærværende teknologi der muliggør omdannelse og kontrol af elektrisk energi ved produktion, transmission, distribution og slutbrug. Ved slutbrug står den industrielle sektor for den største del af det globale elektriske energiforbrug. En betydelig del af elektrisk energi brugt i den industrielle sektor er brugt i mellemspændings motordrev systemer, på høj effekt (375 kW – 10,000 kW), mellemspændings (1 kV – 10 kV) effektelektronik konvertere. På distributionssiden bruger man højeffekts effektelektronik mellemspændings konvertere til elektrisk net støttefunktioner. På produktionssiden er der efterspørgsel på mellemspændings effektelektronik på grund af forøgelsen af vedvarende energi så som solceller og vind turbiner da det har potentielle fordele ved øget effektivitet på system-niveau og kan reducere "levelized cost of energy" for disse energi-kilder. Halvleder komponenter til effektelektronik udgør en central byggesten af moderne effektelektronik konverterer. I dag er kommercielle højeffekts mellemspændings konverterer baseret på silicium (Si) halvleder komponenter som har udviklet sig til en moden teknologi og har domineret effektelektronik industrien i mange år. Da halvleder komponenter baseret på silicium har nået deres teoretiske grænse for ydeevne spås det at de relativt nyligt fremkomne siliciumkarbid (SiC) baseret, "wide band gap" (WBG), komponenter vil være et fremtidigt alternativ til Si-baseret komponenter. SiC-baserede komponenter giver signifikante fordele til effektelektronik konvertere da de kan simplificere konverter topologi og samtidigt øge effektiviteten og effekttætheden. Dette kan de på grund af deres mindre størrelse, højere spændingsblokeringsevne, hurtigere skiftehastighed og evne til at modstå høje temperaturer. Dette PhD speciale vil demonstrere brugen af 10 kV SiC effektelektronik komponenter i mellemspændings effektelektronik. Den hurtige spændingsændring ($\mathrm{d}v/\mathrm{d}t$) som kommer fra kombinationen af mellemspænding og hurtig skiftehastighed i en SiC "Metal Oxide Field Effect Transistor" (MOSFET) kræver nøje betragtning af elektriske parasitter. Især parasitisk kapacitans koblinger kan negativt påvirke elektrisk interferens og kompatibilitet men også influere skifte-transienterne i en effektelektronik konverter. Særligt parasitisk kapacitans koblinger fra effekt-moduler er vigtige, såvel som eksterne

kredsløb så som “gate-drivers" og passive komponenter. Dette PhD speciale begynder med en introduktion af “State of the art” og 10 kV SiC MOSFET effekt-moduler som er brugt i dette speciale. Derefter vil der blive præsenteret en “gate-driver" med høj spændingsisoleringsevne og meget lav koblings-kapacitans ($<$ 3 pF). Hovedbidraget af dette PhD speciale ligger i en undersøgelse af de strømme som opstår fra effekt-modulers parasitiske kapacitanser og deres påvirkning af energien brugt på at tænde og slukke halvleder-komponenterne i effekt-modulerne. Ved at løse diverse videnskabelige udfordringer og implementere mitigeringsstrategier for at minimere høje $\mathrm{d}v/\mathrm{d}t$ inducerede strømme på effekt-modulerne og deres kredsløb er det lykkedes at designe og bygge et 50 kVA, 4.16 kV mellemspændings effekt-modul demonstrator som er eksperimentelt valideret tæt på dets tiltænkte driftstilstand. Fra konverter målinger kan det udledes at den designede mellemspændings effekt har en effektivitet på mere end 99% i en jævnstrømsinjiceret 3-fase “back-to-back" regenerativ test opstilling. Dette PhD speciale vil ende med en opsummering af forskningen udført og kommer med overvejelser om fremtidigt arbejde.

Contents

Abstract **v**

Dansk resumé **vii**

Preface **xiii**

I Extended summary 1

1 Introduction **3**
- 1.1 Background and motivation . . . 3
- 1.2 State of the art . . . 6
- 1.3 Thesis hypotheses and objectives . . . 9
  - 1.3.1 Thesis hypotheses . . . 9
  - 1.3.2 Thesis objectives . . . 10
- 1.4 Thesis outline and contributions . . . 10
- 1.5 List of publications . . . 11

2 SiC MOSFET power modules **15**
- 2.1 Introduction . . . 15
- 2.2 10 kV half-bridge SiC MOSFET power modules . . . 15
- 2.3 Static characterisation of 10 kV SiC MOSFET and JBS diode . 17
- 2.4 Summary . . . 19

3 Galvanically isolated low-isolation capacitance gate driver **21**
- 3.1 Introduction . . . 21
- 3.2 DC-DC isolated power supply . . . 26
  - 3.2.1 Transformer design . . . 27
- 3.3 Gate driving stage . . . 30
- 3.4 Experimental validation . . . 31
- 3.5 Summary . . . 33

4 Dynamic switching characterisation of SiC MOSFET power modules 35
4.1 Introduction 35
4.2 Impact of power module parasitic capacitances on the SiC MOSFET switching transients 36
4.2.1 Device under test 36
4.2.2 Impedance network between the power module and heatsink 38
4.2.3 Experimental test bench 39
4.2.4 Analysis of SiC MOSFET turn-on and turn-off switching transients 41
4.2.5 Discussion on an indirect measurement method utilized to obtain the power module parasitic capacitance related displacement current 44
4.2.6 Analysis of power module parasitic capacitance impact on the turn-on and turn-off switching energy dissipation 47
4.3 Assessment on the impact of SiC JBS diode on SiC MOSFET switching transient 54
4.3.1 Device under test 54
4.3.2 Analysis of turn-on and turn-off switching energy dissipation for power module with and without SiC JBS diode 54
4.4 Impact of power module design change in terms of reduced module capacitance and elimination of SiC JBS diode 62
4.5 Summary 64

5 10 kV SiC MOSFET enabled medium voltage power stack 65
5.1 Introduction 65
5.2 Topology and system specification 66
5.3 MV power stack assembly 67
5.3.1 DC-link and busbar design 67
5.3.2 Thermal management 70
5.4 Experimental setup and results 75
5.5 Summary 78

6 Conclusion: Summary and future work 81
6.1 Summary and main contributions 81
6.2 Future work 83
References 86

II Appended papers 99

A Gate driver with high common mode rejection and self turn-on mitigation for a 10 kV SiC MOSFET enabled MV converter 101
A.1 Introduction . . . 103
A.1.1 Transformer design . . . 106
A.1.2 Design consideration for primary switch snubber and secondary snubber . . . 107
A.2 Design of a gate driving stage with active Miller clamp functionality 107
A.3 Device under test . . . 109
A.3.1 Continuous switching operation . . . 111
A.3.2 MOSFET first quadrant operation: turn on/off switching transition . . . 112
A.4 Conclusion . . . 115
References . . . 115

B Impact of Power Module Parasitic Capacitances on Medium Voltage SiC MOSFETs Switching Transients 119
B.1 Introduction . . . 121
B.2 Device under test - 10 kV half bridge SiC MOSFET power module 123
B.2.1 Equivalent impedance network between power module and the heatsink . . . 126
B.3 Experimental test bench . . . 127
B.4 Understanding Impact of power module parasitic capacitance on MOSFET turn-on and turn-off switching transients based on experimental results . . . 129
B.4.1 Analysis for the turn-on switching transient . . . 129
B.4.2 Analysis for the turn-off switching transient . . . 131
B.5 Indirect methodology utilized to obtain module parasitic capacitance related displacement currents . . . 132
B.6 Analysis of impact of module parasitic capacitance impact on turn-on switching energy dissipation . . . 137
B.7 Analysis of module parasitic capacitance impact on turn-off switching energy dissipation . . . 144
B.8 Conclusion . . . 146
References . . . 147

C Switching Performance Assessment of 10 kV Half-Bridge SiC MOSFET Power Modules With and Without Anti-Parallel SiC JBS Diode 151
C.1 Introduction . . . 153
C.2 Device under test - 10 kV half-bridge SiC MOSFET power module 156
C.3 Experimental test setup . . . 158

C.4 Impact of the anti-parallel SiC JBS diode on the SiC MOSFET switching transient 158
C.4.1 Analysis of the turn-on switching transient 159
C.4.2 Analysis of the turn-off switching transient 162
C.5 Comparison of the switching energy dissipation for the module with and without anti-parallel SiC JBS diode 164
C.5.1 Analysis of the turn-on switching energy dissipation . . 164
C.5.2 Analysis of the turn-off switching energy dissipation . . 171
C.6 Conclusion 173

D Demonstration of a 10 kV SiC MOSFET based Medium Voltage Power Stack 175
D.1 Introduction 177
D.2 Medium voltage power stack 178
D.2.1 Half bridge 10 kV SiC MOSFET power module 178
D.2.2 Isolated power supply and gate driver 179
D.2.3 DC-link and busbar design 180
D.2.4 Thermal management 182
D.2.5 Power stack assembly 183
D.3 Experimental results 184
D.3.1 On-sate and switching characteristics of the half bridge 10 kV SiC MOSFET power module 184
D.3.2 Experimental setup and test results 186
D.4 Conclusion 188
References 189

E Multi-chip Medium Voltage SiC MOSFET Power Module with Focus on Low Parasitic Capacitance. 193
E.1 Introduction 195
E.2 Medium Voltage Design Considerations 196
E.3 Design of 10 kV, 80 A SiC MOSFET Power Module 197
E.4 Parasitics and Simulation 200
E.5 Double Pulse Setup 201
E.6 Experimental Results and discussion 201
E.7 Conclusion 206
References 207

Preface

As I am writing this dissertation towards the fulfillment of Doctor of Philosophy degree, I would like to express my sincere appreciation to the individuals who have made important contributions in my professional and personal development to grow as an independent researcher and a better human being.

I would like to express my utmost appreciation to Prof. Stig Munk-Nielsen for giving me the opportunity to work within the field of medium voltage Wide Band Gap power semiconductor devices and their applications. His enthusiasm for research, optimism and expertise within the field of power electronics has been a source of inspiration for me. I would like to thank him for his constant availability and many technical as well as professional guidance during my PhD, more importantly for introducing me to this exciting field of research during my Master's studies at Aalborg University, which culminated my interest in continuing further research.

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Furthermore, I would like to acknowledge Department of Energy Technology, Innovation Fund Denmark, KK Wind Solutions, Siemens Gamesa Renewable Energy and Vestas Wind Systems that co-funded MV-BASIC (Medium Voltage Converters Based on SiC) / MVolt (Medium voltage Power Electronics for Wind Systems) research projects, through which this PhD project has been supported.

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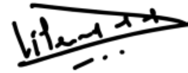
Aalborg, September 2021
Dipen Narendra Dalal



Part I

Extended summary

Chapter 1

Introduction

1.1 Background and motivation

The electric energy consumption of the world reached 22,847 TWh in 2019, out of which 41.9 % of the total consumed electric energy accounts for the industrial sector [1]. To meet the growing demand electric energy production has accelerated over the past few years. The global push towards green energy transition to tackle the climate change and economies of scale has lead to a rapid deployment of renewable energy sources, in particular wind and solar, increasing their share to almost 7.8 % in the 26,936 TWh global electric energy production in 2019 [1]. Global electric energy consumption and electricity generation by different sources over the years 2010 – 2018 is presented in Fig. 1.1. Along with the decarbonization of electric energy sources, significant improvements in energy efficiency by means of implementation of the available technology is necessary [2]. In present-day electricity network, power electronics is utilized at power generation, transmission, distribution and consumer end as the enabling technology for the conversion and control of power. At the consumer end, electric motor drive systems hold the single largest share, accounting for 43 % - 50 % of the global electric energy consumption [4]. Of these, high power (375 kW – 10,000 kW) medium voltage (MV) (1 kV – 10 kV) drive systems constitute the smallest portion of total electric drive systems in terms of number of installations. However, medium voltage drive systems are of great interest from the energy efficiency point of view due to their enormous energy consumption [4]. In 2019, European Union (EU) Commission laid down regulation 2019/178 for energy efficiency eco-design requirements for motors and variable speed drive systems with rated power of 0.12 kW – 1000 kW and voltages up to 1 kV with an aim to reduce 10 TWh of energy savings in EU that corresponds to 2030 goal of 3 Mt equivalent of annual CO_2 emission reduction [5]. The Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology is

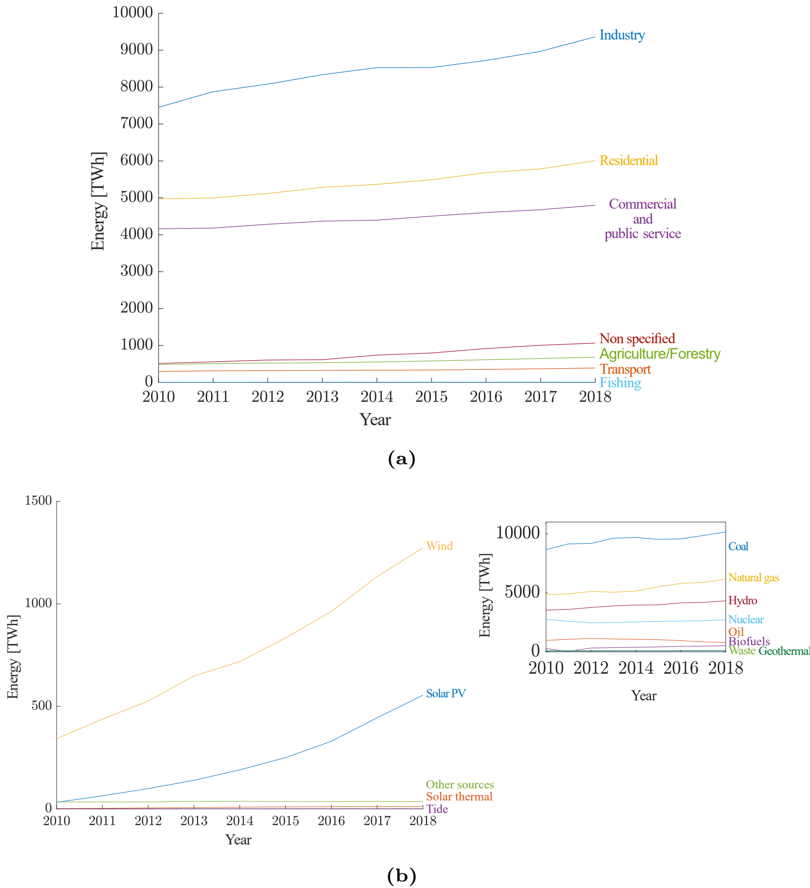


Fig. 1.1: (a) Electricity consumption by sector and (b) electric energy production by sources during the years 2010 – 2018. Source: [1], [3]

classified as the best available technology for the energy efficiency improvements by means of reducing the semiconductor losses in the variable speed drive systems compared to an existing solution [5]. Electric motors and variable speed drive systems with voltages above 1 kV are relevant but have been excluded for the time being as no classification exists for the energy efficiency of motors for this voltage class [5].

At the generation end, high power MV power electronic converters are finding its application in the wind industry, as the increasing turbine power levels in range of tens of megawatts exemplify requirements for the MV generators. Since adapting MV solutions at increased power levels can provide benefits in terms of reduced ohmic losses and levelized cost of energy (LCoE) [6]. Recently announced offshore wind turbine Haliade - X from General Electric Renewable

Energy utilizes 12 MW - 13 MW, 3.3 kV synchronous generator with PCS 6000 MV power electronic converter from ABB [7]–[9].

Another application of the high power MV converter is found for grid support functionalities. An emerging application and widely discussed alternative to the low frequency transformer, the solid state transformer (SST) utilizes the power electronics converter with medium frequency transformer for direct interfacing of the MV and low voltage (LV) grid [10]. Solid state transformers have been proposed for variety of applications such as traction, data center power supplies, MV high power electric vehicle (EV) battery chargers and interconnection of renewable energy sources to the distribution grid [11].

In 2011 SiC MOSFETs in 1.2 kV – 1.7 kV voltage class were first introduced commercially, since then there has been significant improvements in SiC MOSFET technology in terms of lower on-state resistance, increase in wafer diameters and improved reliability [12]–[14]. In recent years, SiC MOSFETs in 3.3 kV, 6.5 kV and 10 kV voltage class have been demonstrated by Wolfspeed and are available as an engineering sample [15], [16]. SiC MOSFETs in 3.3 kV – 15 kV voltage class have gained significant interest from industry and academia for a broad range of applications including active filters for MV distribution grids [17], motor drives [18], [19], shore-to-ship power supply [20], renewable energy [21] and SST based applications i.e, MV connected distribution systems [22]–[24], data center power supply [25], grid support [26], EV fast charger [27], railway traction drives [28] and high-voltage direct current transmission [29].

Considering the high power MV converters rated for 4.16 kV - 7.2 kV line-line voltages, MV SiC MOSFETs in 10 kV voltage class are of particular interest as an alternative to Silicon (Si) power semiconductor based solution, since higher blocking voltage capability, relatively low on-state resistance, smaller device capacitance and higher thermal conductivity of SiC MOSFET offer numerous benefits [30], [31], such as: simplification of the power converter topology and control complexity by eliminating the need of series connection of semiconductor devices and multi-level converter topologies. Thereby reduced component count, lower switching losses, increased power density and efficiency [16]. At present, the cost of MV SiC MOSFETs is significantly higher than their Si counterparts, however SiC MOSFET due to its technological benefits is seen as the enabling technology for EV drive trains [32]. Lately, the EV market is experiencing a rapid growth as a result of the global push for environment friendly policies in terms of CO_2 emission standards [33]. With higher penetration of the SiC MOSFETs in EV drive trains as well as charging infrastructure and success in fabrication of the relatively large diameter (150 mm – 200 mm) SiC wafer is expected to bring down the cost of these devices [32], [34]. As a possible alternative to the Si based power semiconductor technology, SiC semiconductor devices exhibit potential to push the limits of attainable power density, efficiency and thermal performance.

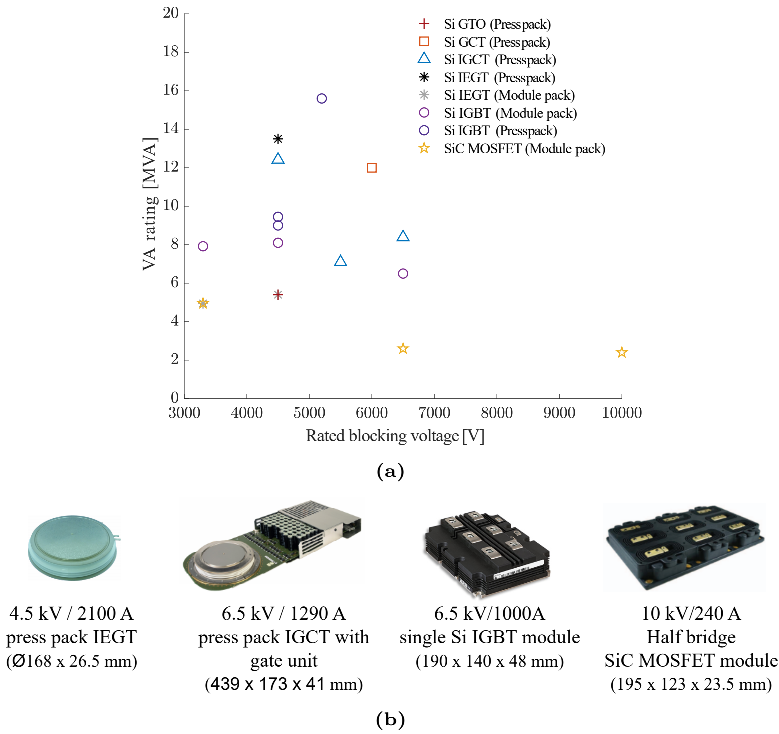
With superior performance characteristics of MV SiC power semiconductor

technology comes new challenges in terms of utilizing these power semiconductor devices in practical applications. The medium voltage levels and the fast switching characteristics of MV SiC devices introduce new design challenges with regards to their application in power electronic converter as it imposes different design considerations in terms of electrical parasitics for the power module, interfacing auxiliary circuits and passive components when compared to their Si counterparts. The PhD thesis aims to unfold these key electrical parasitics and their impact on utilizing MV SiC MOSFETs in 10 kV voltage class for its intended use in MV high power conversion applications.

1.2 State of the art

Generally, power electronic converters rated at high power utilize MV in comparison to the LV as it offers benefits in terms of lower ohmic i^2R losses for similarly rated power level. Currently, the peak blocking voltage capability of the commercially available modern power semiconductor devices is limited up to 6.5 kV. The choice of power semiconductor devices in this voltage class is primarily dominated by Si based bipolar devices such as: insulated-gate bipolar transistor (IGBT) [35]–[38], injection enhanced gate transistor (IEGT) [39], integrated-gate commutated thyristor (IGCT) [40], symmetric gate-controlled thyristor (SGCT) [41] and gate turn-off thyristor (GTO) [41]–[43] for the power converters utilizing voltage source converter (VSC) topology and thyristors or phase controlled thyristor (PCT) for current source converter (CSC) topology. Commercially available MV Si and recently announced noncommercial SiC based wire bonded or press pack power modules from major manufacturers in 3.3 kV or higher voltage class are presented in Fig. 1.2a, based on their maximum Volt Ampere (VA) ratings in their respective voltage class [28], [35]–[40], [44], [45].

The high power MV power electronic converters can be broadly classified into current source and voltage source topologies as presented in Fig. 1.3. The VSCs have become dominant in the high power MV applications up to few tens of MW, due to their versatility, continuous development of power semiconductor technology and ease of integration. Commercial high power MV converters cover wide power range from a few hundreds of kilowatts to tens of megawatts with rated line-line output voltage between 1.2 kV to 13.8 kV with most common voltage ratings being: 2.4 kV, 3.3 kV, 4 kV, 4.16 kV, 6 kV, 6.6 kV, 10 kV, 11 kV or 13.8 kV [46], [47]. To attain improved power quality with lower filtering requirements at medium voltages, multi-level converter topologies or series connection of power semiconductor devices is adopted due to practical limitation of the prevailing power semiconductor devices in terms of their peak blocking voltage capability and maximum operating switching frequency [46]. These topologies are three level neutral point clamped (3L-NPC)



(a)

(b)

Fig. 1.2: (a) Overview of medium voltage Si and SiC power modules (b) Image of the modern Si and SiC based press pack or power module packages. Source: [28], [35]–[45]

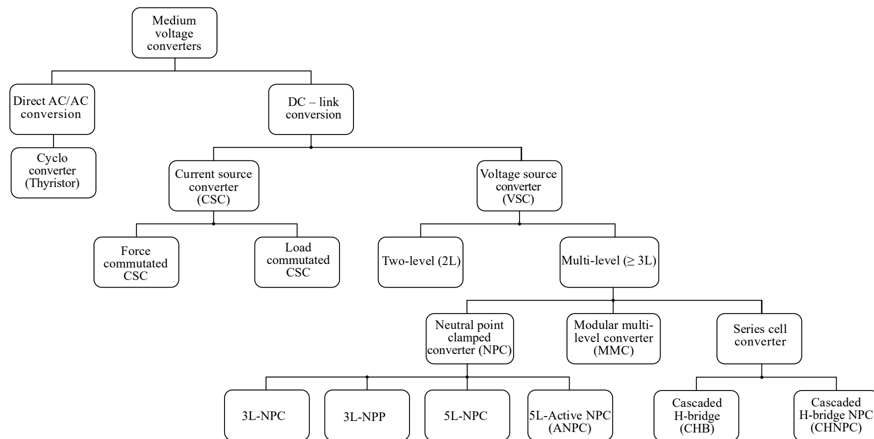


Fig. 1.3: Overview and classification of high power MV converter topologies.

[48]–[51], five level H-bridge neutral point clamped (5L-NPC) [52], cascaded H-bridge (CHB) [53] and modular multi-level converter (MMC) [54], [55]. In spite of offering numerous advantages, multi-level converter topologies suffer from several drawbacks due to their higher component counts, converter design and control complexity. A brief overview and comparative evaluation of the most commonly used topologies in commercial high power MV converters is presented in Table 1.1.

Table 1.1: Performance characteristics comparison of the most commonly implemented power converter topologies in commercial high power MV converters [47].

Performance characteristics	3L-NPC	5L-NPC	CHB	MMC
Power quality				
Output current total harmonic distortion (THD)	+	++	+++	+++
Output voltage THD	+	++	+++	+++
Max. output voltage step	+	++	+++	+++
Output voltage dv/dt	+	++	+++	+++
Filter requirements	+	++	+++	+++
Controllability				
Ease of control implementation	++	+	+	+
Control or design challenges	DC-link voltage balancing	DC-link voltage balancing	Voltage and current sharing within cascaded H bridge	Submodule capacitor voltage balancing
Converter topology				
Semiconductor component count	++	+	+	+
Power loss distribution	+	++	+++	+++
Modularity & redundancy	+	+	+++	+++
Input transformer design complexity	+++	+	+	+++

From the literature survey it has been identified that no commercial MV converters (rated for line-line voltage $\geq$ 3.3 kV) exist that utilize the two-level VSC topology. Lately, the MV SiC power semiconductor devices are getting attention in high power MV application since there is very little or no room for converter performance improvements with prevalent Si based technology as they seem to have attained their theoretical performance limits [30], [31].

1.3 Thesis hypotheses and objectives

This section presents the thesis hypotheses and objectives for the research work.

1.3.1 Thesis hypotheses

Increased voltage level and very high rate of change of voltage ($\mathrm{d}v/\mathrm{d}t$) during switching transients that can approach the values as high as 250 kV/µs for SiC MOSFETs, are order of magnitudes higher than their Si counter parts [22], [56]. Medium voltage levels combined with high $\mathrm{d}v/\mathrm{d}t$ switching transients of SiC MOSFET introduce new challenges in terms of their practical application in power electronic converters. This leads to the formulation of the following hypotheses:

- The high $\mathrm{d}v/\mathrm{d}t$ switching transient of MV SiC MOSFETs combined with their relatively lower current ratings, impose new design considerations in terms of reduced parasitic capacitance for the SiC MOSFET power modules and circuits or components interfacing the power modules such as gate drivers and filter inductors. Due to fast switching transient, the parasitic capacitances that experience high $\mathrm{d}v/\mathrm{d}t$ can introduce displacement currents during switching transients. The magnitude of this displacement current can be significantly higher, which may result in worsening the electromagnetic interference and compatibility (EMI/EMC) performance, increased power loss and difficulties in achieving reliable operation for a power electronic converter.

- Due to medium voltage levels and high $\mathrm{d}v/\mathrm{d}t$ switching transient, the impact of power module parasitic capacitance on SiC MOSFET switching transient and switching energy dissipation can be significant, which may not be neglected in the case of MV SiC MOSFET power modules.

- With implementing key design considerations in terms of low coupling capacitance for power modules and interfacing circuits, MV SiC MOSFET enabled power electronic converter based on simple two-level voltage source converter topology can be demonstrated.

1.3.2 Thesis objectives

Based on the hypotheses presented in the previous section, the main objectives of the PhD thesis are formulated as follows:

- To design and experimentally validate the low coupling capacitance and MV isolated gate driver, with a high common mode noise immunity for 10 kV half-bridge SiC MOSFET power module.
- To analyse the impact of power module parasitic capacitance on SiC MOSFET switching transient and switching energy dissipation.
- To design a kVA rated MV power stack, utilizing 10 kV half-bridge SiC MOSFET power modules and demonstrate experimental validation of power stack close to its rated operating point, with feasible efficiency estimation based on measured power loss data.

1.4 Thesis outline and contributions

This PhD dissertation is presented in the form of article based thesis and consists of six chapters. The chapters are based on journal and conference publications [A]–[E], as listed in Section 1.5.

Chapter 1
Introduction
This chapter introduces background and motivation for the PhD thesis and presents state of the art.

Chapter 2
SiC MOSFET power modules
The chapter introduces custom-packaged 10 kV half-bridge SiC MOSFET power modules utilized in this research project. Furthermore, it presents key static characterisation data for 10 kV SiC MOSFET and 10 kV SiC Junction Barrier Schottky (JBS) diode.

Chapter 3
Galvanically isolated low-isolation capacitance gate driver
This chapter presents 10 kV SiC MOSFET gate driver design with MV isolation and very low coupling capacitance ($<$ 3 pF) for a high common-mode (CM) noise immunity. The experimental validation of the designed gate driver in terms of DC voltage withstand capability, overall gate driving functionality and CM current measurements when subjected to high $\mathrm{d}v/\mathrm{d}t$ switching transient is presented. The design and experimental validation of the gate driver is published in article [A].

Chapter 4
Dynamic switching characterisation of SiC MOSFET power modules
This chapter presents an in-depth analysis regarding the impact of power module

parasitic capacitance on SiC MOSFET switching transient and switching energy dissipation by utilizing two custom-made 10 kV SiC MOSFET half-bridge power modules, that differ in terms of their direct bonded copper (DBC) layouts. The contribution of module parasitic capacitance in terms of added switching energy dissipation is analysed with proposed switching energy dissection method. This work is published in article [B]. In another case study, the assessment of 10 kV half-bridge power modules with and without anti-parallel SiC JBS diode in terms of their switching performance is carried out, using switching energy dissection method proposed in article [B]. The work is summarised in article [C]. Furthermore, the dynamic switching characterisation for a reduced parasitic capacitance 10 kV multi-chip power module is presented, which is based on article [E].

Chapter 5
10 kV SiC MOSFET enabled medium voltage power stack
This chapter presents the design of a 50 kVA, 4.16 kV rated MV power stack utilizing 10 kV half-bridge SiC MOSFET power modules in a simple two-level voltage source converter topology. Experimental validation of the designed power stack is performed in a DC-fed three phase back-to-back regenerative test setup and key electrical measurements for the converter close to its rated operating point are demonstrated. This work is published in article [D].

Chapter 6
Conclusion: Summary and future work
The PhD thesis is concluded in this chapter with a summary highlighting main research contributions and propounded future work.

1.5 List of publications

The PhD Thesis is based on the following publications which have been published or submitted in international conferences or scientific journals in the field of power electronics.

[A] **D. N. Dalal**, N. Christensen, A. B. Jørgensen, S. D. Sønderskov, S. Bęczkowski, C. Uhrenfeldt, S. Munk-Nielsen,"Gate driver with high common mode rejection and self turn-on mitigation for a 10 kV SiC MOSFET enabled MV converter," 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), 2017, pp. P.1-P.10

[B] **D. N. Dalal**, N. Christensen, A. B. Jørgensen, J. K. Jørgensen, S. Bęczkowski, S. Munk-Nielsen, C. Uhrenfeldt, "Impact of Power Module Parasitic Capacitances on Medium-Voltage SiC MOSFETs Switching Transients," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 298-310, March 2020

[C] **D. N. Dalal**, J. K. Jørgensen, H. Zhao, M. M Bech, S. Bęczkowski, C. Uhrenfeldt and S. Munk-Nielsen, “Switching Performance Assessment of 10 kV Half-Bridge SiC MOSFET Power Modules With and Without Anti-Parallel SiC JBS Diode,” submitted to IEEE Open Journal of Power Electronics, 2021. [Submitted]

[D] **D. N. Dalal**, H. Zhao, J. K. Jørgensen, N. Christensen, A. B. Jørgensen, A. B. Jørgensen, S. Bęczkowski, C. Uhrenfeldt, S. Munk-Nielsen, “Demonstration of a 10 kV SiC MOSFET based Medium Voltage Power Stack,”2020 IEEE Applied Power Electronics Conference and Exposition (APEC), 2020, pp. 2751-2757

[E] J. K. Jørgensen, **D. N. Dalal**, S. Bęczkowski, S. Munk-Nielsen and C. Uhrenfeldt, “Multi-chip Medium Voltage SiC MOSFET Power Module with Focus on Low Parasitic Capacitance,” CIPS 2020; 11th International Conference on Integrated Power Electronics Systems, 2020, pp. 1-6.

The co-authored conference and journal publications pertinent to the medium voltage SiC MOSFETs and its applications are listed below:

- H. Zhao, **D. Dalal**, J. K. Jørgensen, M. M. Bech, X. Wang, S. Munk-Nielsen, “Behavioral Modeling and Analysis of Ground Current in Medium-Voltage Inductors,” in IEEE Transactions on Power Electronics, vol. 36, no. 2, pp. 1236-1241, Feb. 2021
- H. Zhao, **D. N. Dalal**, J. K. Jørgensen, A. B. Jørgensen, X. Wang, B. Rannestad, S. Munk-Nielsen, “Identification of the Terminal-to-Core Couplings in Filter Inductors by Using Double-Pulse-Test Setup,” 2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL), 2020, pp. 1-6
- J. K. Jørgensen, N. Christensen, **D. N. Dalal**, A. B Jørgensen, H. Zhao, S. Munk-Nielsen, C. Uhrenfeldt, “Loss Prediction of Medium Voltage Power Modules: Trade-offs between Accuracy and Complexity,” 2019 IEEE Energy Conversion Congress and Exposition (ECCE), 2019, pp. 4102-4108
- H. Zhao, **D. N. Dalal**, X. Wang, J. K. Jørgensen, C. Uhrenfeldt, S. Beczkowski, S. Munk-Nielsen, “Modeling and Design of a 1.2 pF Common-Mode Capacitance Transformer for Powering MV SiC MOSFETs Gate Drivers,” IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, 2019, pp. 5147-5153
- A. B. Jørgensen, N. Christensen, **D. N. Dalal**, “Reduction of parasitic capacitance in 10 kV SiC MOSFET power modules using 3D FEM,” 2017 19th European Conference on Power Electronics and Applications (EPE’17 ECCE Europe), 2017, pp. P.1-P.8

- N. Christensen, A. B. Jørgensen, **D. Dalal**, S. D. Sønderskov, S. Bęczkowski, C. Uhrenfeldt, S. Munk-Nielsen, "Common mode current mitigation for medium voltage half bridge SiC modules," 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), 2017, pp. P.1-P.8

Chapter 2

SiC MOSFET power modules

2.1 Introduction

It was only recently that the first manufacturer of 10 kV SiC devices Wolfspeed Inc., announced the 10 kV/240 A SiC MOSFET power modules [45]. However until then, the 10 kV SiC semiconductor devices were only available in the form of bare dies as an engineering samples from the manufacturer.

To utilize these semiconductor devices in a MV power electronic converter, packaging of these devices in the form of power module is a necessary requirement. The 10 kV SiC MOSFET power modules utilized in this research work are custom packaged at the Packaging Laboratory, Aalborg University [57], [58]. To provide an overview, the 10 kV SiC MOSFET power modules together with key static characteristics for a 10 kV SiC MOSFET and JBS diode dies are presented in this chapter.

2.2 10 kV half-bridge SiC MOSFET power modules

The custom packaged single-chip 10 kV half-bridge SiC MOSFET power module is shown in Fig. 2.1 with markers labeling the terminals. The power module is populated with 8.1 mm x 8.1 mm third generation 10 kV 350 mΩ SiC MOSFETs and an anti-parallel SiC JBS diode dies (from Wolfspeed [16], [59]) per switch position. The 10 kV SiC MOSFETs and diode dies are rated for the continuous drain current of 20 A as per their preliminary datasheet. The dies are soldered on a 0.63 mm Aluminium Nitride (AlN) direct bonded copper (DBC) substrate with a 3 mm thick 104 mm x 59 mm Aluminium Silicon-Carbide (AlSiC)

baseplate [57]. There is an access to the die surface through a pipette, which allows insertion of fiber optic temperature sensors for monitoring purpose. This single-chip 10 kV power module is utilized in a MV three phase power stack demonstrator, which is presented in Chapter 5.

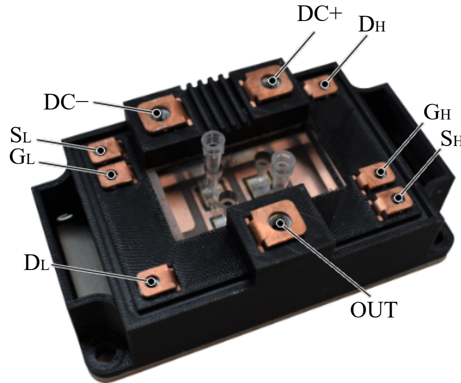


Fig. 2.1: Picture of a 10 kV single-chip half-bridge SiC MOSFET power module. (Letters D, G, H indicate drain, gate and source respectively. Subscripts H and L stands for the high side and low side devices, respectively.) [D]

The custom packaged multi-chip half-bridge power module is shown in Fig. 2.2. The multi-chip power modules is populated with four third generation 10 kV 350 mΩ dies per switch position. The dies are soldered on two separate 1 mm AlN DBC substrates with 3 mm thick 104 mm x 59 mm AlSiC baseplate [58]. The module has a power loop inductance of 21.1 nH and a maximum gate loop inductance of 31 nH [58].

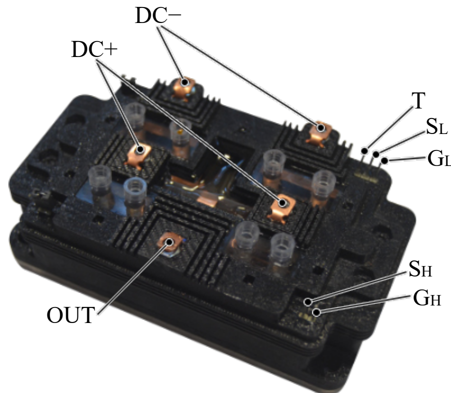


Fig. 2.2: Picture of a multi-chip 10 kV half-bridge SiC MOSFET power module. (Letters G, H, T indicate drain, gate and thermistor, respectively. Subscripts H and L stands for the high side and low side devices respectively.)

2.3 Static characterisation of 10 kV SiC MOSFET and JBS diode

The first quadrant I–V characteristics at gate bias of 20 V as well as third quadrant characteristics at gate bias of 20 V and −5 V for a SiC MOSFET bare dies together with the forward characteristics for a 10 kV SiC JBS diode at 25°C and 125°C temperatures are presented in Fig. 2.3. The I–V characteristics are obtained from the static measurements utilizing Tektronix B371A curve tracer [60].

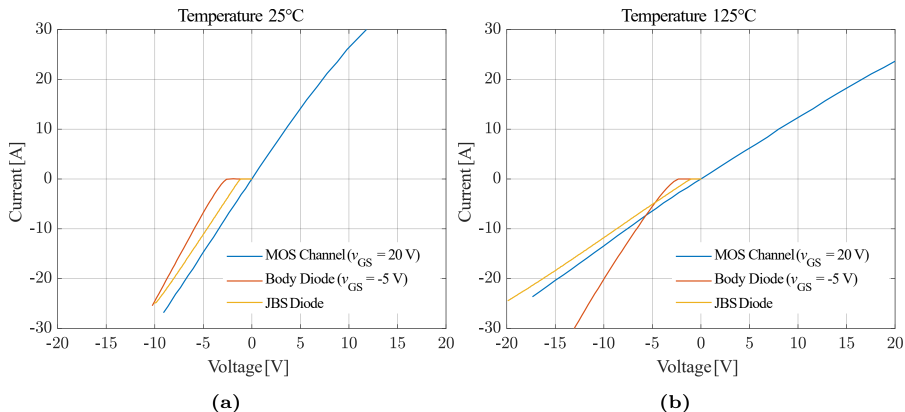


Fig. 2.3: Measured I–V characteristics for 10 kV SiC MOSFET and 10 kV SiC JBS diode at (a) 25°C (b) 125°C.

As can be seen from Fig. 2.3, 10 kV SiC MOSFET exhibits symmetric first quadrant and third quadrant I–V characteristics for a positive gate bias of 20 V. Based on the measured I–V characteristics of a 10 kV SiC MOSFET die, on-state resistance which exhibits positive temperature coefficient is identified to be 364 mΩ and 817 mΩ at 25°C and 125°C, respectively. Whereas, the gate-source threshold voltage is identified to be 7.0 V and 5.2 V at drain current of 100 mA from measured transfer characteristics at drain-source voltage of 30 V and temperatures of 25°C and 125°C, respectively.
The forward voltage drop of body diode decreases with temperature and is measured to be 2.6 V and 2.4 V at 100 mA forward current for temperatures of 25°C and 125°C, respectively. In case of the 10 KV SiC JBS diode the forward voltage is within 1.1 V – 1.2 V at forward current of 100 mA, with similar on-resistance as 10 kV SiC MOSFET for temperature range of 25°C – 125°C. It is worth to mention that, for a 10 kV SiC MOSFET in a third quadrant operation with a positive gate bias of 20 V, the body diode turn-on is not identified and current is primarily conducting through a MOSFET channel [61], [62]. This is attributed to the increase in body diode turn-on voltage when

MOSFET channel is on [62]. Such behaviour is reported for SiC MOSFETs in 3.3 kV or higher voltage class, where ratio of drift layer resistance to total on-state resistance for the MOSFET increases [62]. At 125°C temperature, with increased current levels (>7.5 A) the body diode conduction provides lower on-state voltage drop in comparison to the JBS diode. For the intended application of a 10 kV SiC MOSFET in AC-DC or DC-AC converters where a MOSFET is turned on with a positive gate bias during reverse conduction, the current will primarily conduct through the MOSFET channel or will be shared between the MOSFET channel and anti-parallel JBS diode if present. Although, inclusion of anti-parallel SiC JBS diode may provide lower conduction losses by providing a parallel path to the SiC MOSFET channel during reverse conduction, eliminating a SiC JBS diode is beneficial from a cost and power density point of view for the power module. This can be considered if 10 kV SiC MOSFET body diode performs as good as SiC JBS diode in terms of reverse recovery.

Measured input, output and reverse transfer parasitic capacitances for a 10 kV SiC MOSFET with drain-source voltage bias of up to 3 kV utilizing Keysight B1506 curve tracer [63], is shown in Fig. 2.4. Here, the input capacitance (C_{ISS}) is equal to the sum of MOSFET gate-source capacitance (C_{GS}) and drain-source capacitance (C_{DS}). Whereas, the output capacitance (C_{OSS}) is equal to the sum of MOSFET gate-drain capacitance (C_{GD}) and drain-source capacitance (C_{DS}). The reverse transfer capacitance (C_{RSS}) often referred to as a Miller capacitance is equal to the gate-drain capacitance (C_{GD}). The gate-source capacitance (C_{GS}) of a MOSFET, which is almost constant with

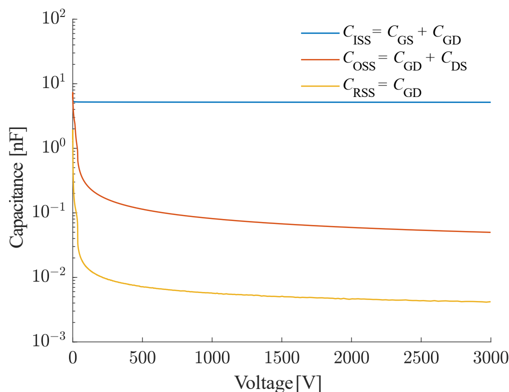


Fig. 2.4: Measured input, output and reverse transfer capacitances with drain-source voltage bias of up to 3 kV for a 10 kV SiC MOSFET.

respect to the applied drain-source voltage bias is measured to be 5.2 nF. The gate-drain capacitance (C_{GD}) and drain-source capacitance (C_{DS}) are highly non-linear, where major drop in capacitance (nF to tens or hundreds of pF)

occurs within the first few hundred volts of the applied drain-source bias voltage as can be seen in Fig. 2.4. The drive power or gate charge requirement for a gate driver along with the switching transition times of a SiC MOSFET are primarily determined by the MOSFET input capacitance. The output capacitance of the MOSFET is of a great importance as this gets charged or discharged during the switching event, which incurs losses. From, this point of view, smaller power device input and output capacitance of SiC MOSFETs compared to their Si counter parts is desirable to achieve faster switching transition time and lower switching energy dissipation [30], [64], [65].

2.4 Summary

In this chapter, the 10 kV half-bridge SiC MOSFET power modules to be utilized in the research work are introduced. The key data from static I–V characterisation at 25°C and 125°C and capacitance measurements for 10 kV SiC power semiconductor devices are presented.

Chapter 3

Galvanically isolated low-isolation capacitance gate driver

3.1 Introduction

In the case of MV half-bridge SiC MOSFET power modules, $\mathrm{d}v/\mathrm{d}t$ at the output terminal of a half-bridge during switching transient can be as high as up to 250 kV/µs [22], [56], [66]. The fast switching transient, introduces displacement current through the isolation barrier of the gate driver power supply as well as signal path that appear as common mode (CM). The magnitude of CM current i_{CM} is related to the $\mathrm{d}v/\mathrm{d}t$ and the value of isolation capacitance C_{iso} as presented in (3.1),

$$i_{\mathrm{CM}} = C_{\mathrm{iso}} \cdot \frac{\mathrm{d}v}{\mathrm{d}t} \tag{3.1}$$

The magnitude of CM current needs to be limited to sufficiently lower value in order to ensure reliable operation of the half-bridge power module, since increased CM noise may negatively impact the gate drive control signal fidelity [67]. This impose a requirement of a high isolation voltage with a very low coupling capacitance, typically less than 5 pF for the gate driver [67]. Commercially available DC-DC power supplies with the isolation voltage rating in the range of 10 kV are unregulated or exhibit high isolation capacitance (10 pF – 20 pF) [68]–[70]. Furthermore, the fast switching transient can lead to a shoot-through due to Miller induced false turn-on of either high side (HS) or low side (LS) device in a half-bridge power module during the turn-on of the complementary device [71], [72]. This can be mitigated by the integration of the active Miller clamp (AMC) circuitry, which limits the complementary device gate-source

voltage (v_{GS}) below its threshold by providing a low impedance path to the high dv/dt induced Miller current [73]. Above mentioned considerations, require a design of the MV isolated, low isolation capacitance gate driver customized for the 10 kV half-bridge SiC MOSFET power modules. Various designs for the MV SiC MOSFET gate driver has been reported in literature, which are summarized in Table 3.1 with details on the DC-DC power supply and gate drive architecture including list of additional functionalities.

Table 3.1: Summary from the literature review of MV SiC MOSFET gate drivers.

DC-DC power supply and gate driver	Additional functionality
[67] DC-DC: Single output voltage, primary side full-bridge and secondary side diode rectifier with a toroidal core transformer with windings enclosed inside Polyvinyl chloride (PVC) tube. Voltage regulation with a regulator on a secondary side. (C_{iso} = 5 pF) Gate driver: Driver IC DEIC 420 from IXYS. Signal isolation using a pulse transformer.	-
[66] DC-DC: Dual output voltage, single active bridge topology with primary side full-bridge and secondary side diode rectifier with a toroidal core transformer. (C_{iso} = 4.3 pF)	-
[74] DC-DC: Primary side frequency controlled LC current source series resonant circuit feeding common AC bus as a primary, that supplies multiple toroidal core current transformer secondaries with single output. Secondary side diode bridge rectifier with hysteresis voltage controller for output voltage stabilization. (C_{iso} = 1.05 pF) Gate driver: Driver IC IXDD614 from IXYS with under voltage lockout (UVLO). Signal isolation using a fiber optic link.	-

Table 3.1 – cont.

DC-DC power supply and gate driver	Additional functionality
[75] DC-DC: Power transmission over fiber optic with laser transmitter and receiver. Voltage regulation using, linear voltage regulator (C_{iso} theoretically infinite) Gate driver: P-channel and N-channel MOSFET totem pole based driver. Signal isolation using a fiber optic link.	AMC and desaturation (DESAT) based over current detection.
[76] DC-DC: Flyback based dual output unregulated power supply with a toroidal core transformer. (C_{iso} = 4.1 pF) Gate driver: Driver IC IXDN614 from IXYS. Singal isolation using a fiber optic link.	-
[77] DC-DC: Single ended push-pull converter with a half-bridge on primary side and diode rectifier on secondary side, with a toroidal core transformer utilizing single turn primary. Voltage regulation using linear regulator on secondary side. (C_{iso} = 3.5 pF) Gate driver: No information on gate driver available. Signal isolation using a fiber optic link.	-
[78] DC-DC: Single active bridge topology utilizing full-bridge on the primary side and diode rectifier on the secondary side with a single output. Power supply utilizes PCB based isolation transformer. Voltage regulation using linear regulator on secondary side. (C_{iso} = 1.6 pF) Gate driver: Driver IC HPCL 316-J from Broadcom with an integrated DESAT detection with a current booster stage, which utilizes a driver IC from IXYS IXDN614YI. Signal isolation using a fiber optic link.	DESAT based short circuit protection, utilizing 8 kV Schottky diode as a DESAT diode.

Table 3.1 – cont.

DC-DC power supply and gate driver	Additional functionality
[79] DC-DC: Series-series compensated load independent resonant converter topology with full bridge on primary side and diode rectifier on the secondary side. Transformer design with ferrite E-cores. Buck-boost converter stage on the secondary side to generate negative voltage. ($C_{\text{iso}} = 2.5$ pF) Gate driver: Driver IC UCC27531-Q1 from Texas Instruments (TI) with a current boost stage. Signal isolation using a fiber optic link.	Current transformer based over current sensing and protection circuit with fast reaction time. (22 ns)
[80] DC-DC: Resonant LCC-S topology with high frequency full-bridge on the primary side and diode rectifier on the secondary side with dual output voltage. Power supply utilizes single PCB integrated transmitter and receiver coil for wireless power transfer. Voltage regulation using regulated DC-DC converter on secondary side. ($C_{\text{iso}} = 2.6$ pF) Gate driver: Driver IC ISO5852S from TI. Signal isolation using a fiber optic link.	-
[81] DC-DC: Commercial single output DC-DC power supply (unregulated) ISO5125I-120 from Power Integrations. ($C_{\text{iso}} = 4$ pF) Gate driver: Driver IC STGAP1AS from STMicroelectronics with external multiple parallel BJT totempole based current booster stage. Signal isolation using a fiber optic link.	PCB embedded Rogowski current sensor for over current protection.
[82] DC-DC: Resonant current source LCCL-LC topology with high frequency half-bridge on the primary side and diode rectifier on the secondary side. Utilizes a single turn primary that supplies multiple secondaries with a toroidal core. Output voltage regulation using linear voltage regulator. ($C_{\text{iso}} = 1.67$ pF)	-

Based on the literature survey presented in Table A.2, it is identified that the most commonly adopted approach for a DC-DC power supply is to use an active half-bridge or full-bridge circuit on primary side with a diode rectifier on

secondary side, where voltage regulation is achieved by utilizing a linear voltage regulator or additional DC-DC regulated power supply on the secondary side. The isolation transformer design include toroidal core, E-core and PCB based solutions. For gate driving stage a totem pole driver IC with a current booster stage to increase the peak source–sink current capability in case drive current requirement is higher than what gate driver IC can support. For this signal isolation stage, fiber optic based solution is adopted.
For the 10 kV half-bridge power module, a custom gate driver is designed which utilizes a Flyback based regulated +20 V/−5 V dual output voltage DC-DC isolated power supply with coupling capacitance less than 3 pF and isolation voltage rating of up to 10 kV with a gate driving stage incorporating AMC functionality. An optional thermistor temperature measurement circuit using 555 IC configured as astable multivibrator is utilized [83]. To achieve high voltage isolation and CM noise immunity for the signal path, a fiber optic based solution is adopted. The schematic of a gate driver architecture is shown in Fig. 3.1.

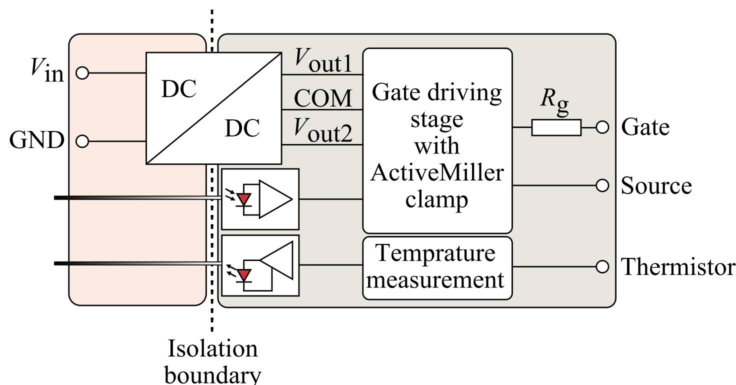


Fig. 3.1: Schematic of the gate driver architecture.

As shown in Fig. 3.2, the gate charge requirement for a 10 kV SiC MOSFET is identified by obtaining the gate current from a measured voltage across the gate resistor in double pulse test (DPT) at the DC-link voltage V_{DC} of 6 kV and switched drain (i_D) or load current (i_L) of 14 A utilizing an external gate resistance R_G of 20 Ω with turn-on ($v_{GS(on)}$) and turn-off ($v_{GS(off)}$) gate drive voltage of +20 V and −5 V, respectively. The test conditions correspond to its intended operating point in terms of DC-link voltage and current levels. The gate charge Q_G is measured to be 255 nC at V_{DC} of 6 kV and i_L of 14 A. The gate drive power requirement for a SiC MOSFET is calculated based on (3.2) and is identified to be 31.9 mW and 63.8 mW for switching frequencies of 5 kHz and 10 kHZ respectively.

$$P_{DRV} = Q_G \cdot (v_{GS(on)} - v_{GS(off)}) \cdot f_{sw} \tag{3.2}$$

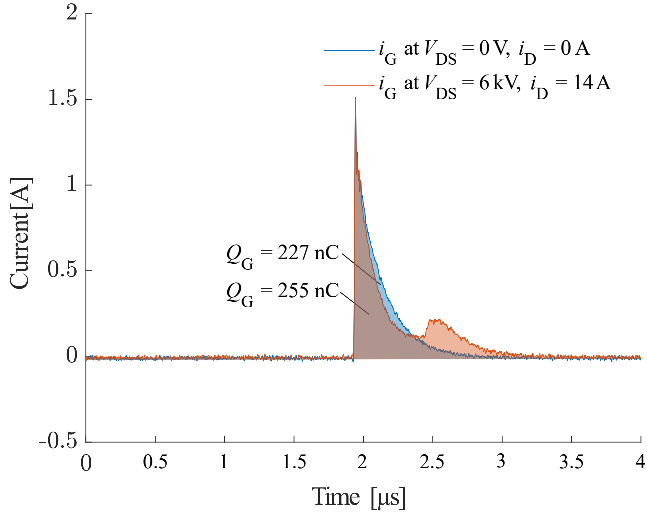


Fig. 3.2: Derived gate charge from obtained gate current by utilizing voltage measured across the external gate resistance in a double pulse test. (Test conditions V_{DC} = 6 kV, i_L = 0 A and 14 A, R_G = 20 Ω)

Whereas for a multi-chip power module, with four dies in parallel per switch position, the gate drive power requirements are 127.6 mW and 252.2 mW for switching frequency of 5 kHz and 10 kHz, respectively. The DC-DC power supply capable of delivering 2 W to 3 W of power, suffice the requirement of total power consumption for the gate driver.

3.2 DC-DC isolated power supply

The design of a DC-DC isolated power supply is based on Flyback topology and utilizes dual secondary winding as shown in Fig. 3.3. The Flyback IC LT 8302 with an integrated controller and 65 V/ 3.6 A switch capable of delivering 18 W is chosen, to obtain lower component count and smaller footprint [84]. The Flyback controller IC operates with a variable frequency range of 12 - 400 kHz in either discontinuous or boundary conduction mode. The boundary or discontinuous conduction mode operation of a Flyback converter in comparison to continuous conduction mode, enables the reduced requirement of magnetizing inductance. In addition to this, Flyback controller IC utilizes the primary winding voltage of Flyback transformer for output voltage regulation. This eliminates an additional coupling capacitance that will be introduced by secondary side voltage sensing and feedback circuit to transfer the sensed secondary side voltage to primary side controller across the isolation barrier. The lower limit of the primary magnetizing inductance is set by the minimum

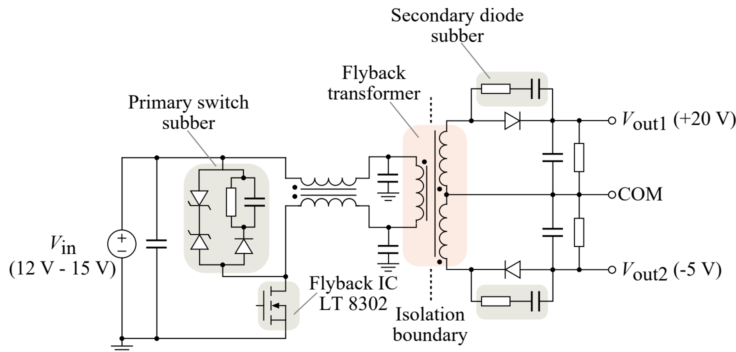


Fig. 3.3: Schematic of a designed Flyback converter, primary switch and secondary snubber circuit.

requirement for the inductance foisted by the Flyback controller IC, which is determined to be 5.17 μH from the datasheet [84]. Whereas, the upper limit is determined by the maximum value of magnetizing inductance below which, Flyback converter operates in the discontinuous conduction mode and is identified to be 931 μH. For a given core geometry and material type, the reduced requirement of magnetizing inductance results in a lesser number of turns and thereby lower coupling capacitance due to smaller surface area of the core occupied by the winding.

The Flyback transformer has a primary and dual secondary windings. The secondary windings connect to the diode rectifier output stage as shown in Fig. 3.3. The output voltages of the Flyback power supply is set to +20 V and −5 V, which corresponds to the turn-on and turn-off gate driving voltage for the 10 kV SiC MOSFET recommended by preliminary datasheet.

3.2.1 Transformer design

The primary requirement of the Flyback transformer is to obtain low isolation capacitance ($\leq$ 5 pF) with isolation voltage rating of up to 10 kV. The Flyback transformer is designed utilizing a Manganese–Zinc (MnZn) medium frequency 3F3 toroidal core TN32/19/13-3F3 from Ferrox Cube, which has a high permeability ($\mu_{\mathrm{i}} = 1800$) with an inductance factor ($A_{\mathrm{L}} = L/N^2$) of 2270 nH.

The minimum and maximum number of turns are identified to be in the range of 2 – 20 based on the minimum and maximum primary magnetizing inductance specified above. With constrains specified by Flyback controller IC the primary to secondary turns ratio ($N_{\mathrm{p}}/N_{\mathrm{s}}$) is chosen to be 0.5, with number of turns for the primary and secondary windings to be $N_{\mathrm{p}} = 5$ and $N_{\mathrm{s}} = 10$, respectively. The secondary winding is split into two with $N_{\mathrm{s1}} = 8$ and $N_{\mathrm{s2}} = 2$, in order to obtain the voltage of +20 V and −5 V with respect to common

point.

To fulfill the MV isolation requirements and achieve low isolation capacitance the windings are placed distantly on the core. In this case, the coupling capacitance between the primary and secondary winding is predominantly due to the capacitive coupling through the core. The coupling capacitance between the winding and the core is determined by winding-core overlap area, distance between the winding and core as well as the permittivity of the core and insulating material in-between. For a toroidal core, high inductance factor is desirable since it lowers the turns requirement for windings to obtain required inductance. Thereby reducing the area of core occupied by windings. A 3D printed spacers from Polylactic Acid (PLA) [85] are spaced between the core and winding, which increases the distance from winding to the core. This results into further reduction of transformer winding to core capacitance and thereby lowering the isolation capacitance between primary and secondary winding. (The relative permittivity of the toroidal core is 10^5 [86], core insulation coating is 4.47 [87] and spacers PLA is 2.7 (1 MHz) [85])

Triple insulated wire [88], with diameter of 0.8 mm and break down voltage rating of 6 kV AC is used for the windings with clearance between the primary and secondary windings of 16 mm. The toroidal core are coated with polyamide and is rated for the DC isolation voltage of 2 kV. Considering breakdown voltage of air of 3 kV/mm and insulation rating of 6 kV AC rms for the tripple insulated wire on either side of winding, clearance of 16 mm is deemed sufficient for its intended operating voltage of 6 kV – 7.2 kV. The picture of a Flyback transformer is shown in Fig. 3.4.

The isolation capacitance between transformer primary and secondary winding

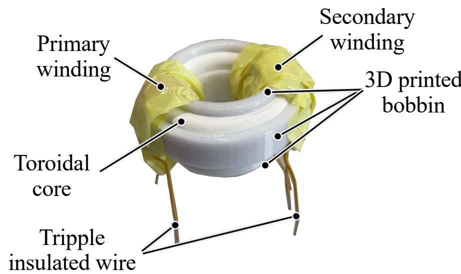


Fig. 3.4: Picture of a Flyback transformer.

is measured to be 1.4 pF (@ 1 MHz) and between the input and output of a gate driver PCB is measured to be 2.9 pF (@ 1 MHz), utilizing a Keysight E4990A impedance analyzer [89]. Measured capacitance as a function of frequency is shown in Fig. 3.5. Some of the key parameters for the Flyback transformer measured utilizing the Keysight E4990A impedance analyzer are listed in Table 3.2. Such arrangement of the primary and secondary windings, results in a poor magnetic coupling for a Flyback transformer, which can be observed from

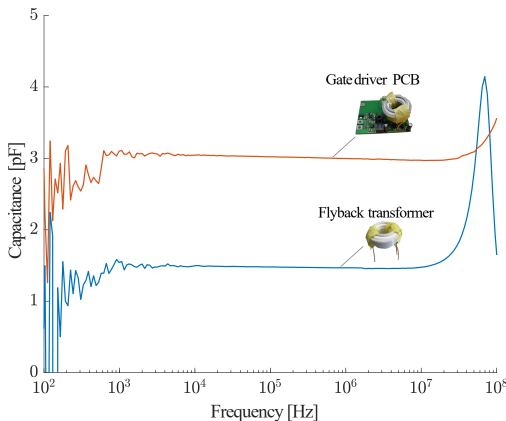


Fig. 3.5: Measured isolation capacitance for the Flyback transformer and gate driver PCB using Keysight 4990A impedance analyser.

Table 3.2: Measured key electrical parameters of the Flyback transformer using a Keysight E4990A impedance analyser.

Parameters	Values
Isolation Capacitance (C_{iso})	1.4 pF
Primary magnetizing inductance (L_{p})	51 µH
Secondary 1 magnetizing inductance (L_{s1})	133 µH
Secondary 2 magnetizing inductance (L_{s2})	8.3 µH
Primary leakage inductance ($L_{\sigma\text{p}}$)	2.66 µH
Secondary 1 leakage inductance ($L_{\sigma\text{s1}}$)	7.07µH
Secondary 2 leakage inductance ($L_{\sigma\text{s2}}$)	0.5 µH

the impedance analyser measurements for primary magnetizing and leakage inductances presented in Table 3.2. The primary and secondary leakage inductance of a Flyback transformer causes voltage overshoot across the primary side switch and secondary side diode rectifier respectively, during their turn off. The voltage overshoot across the primary switch needs to be suppressed within the blanking time of a Flyback controller IC to ensure the correct sensing of Flyback primary winding voltage. In addition to this the voltage spike needs to be limited below the maximum switch voltage rating. This is achieved by utilizing an RCD snubber with RC time constant smaller than the blanking time of the Flyback controller IC and Zener clamp with Zener voltage rating below the break down voltage of an integrated 65 V semiconductor switch as shown in Fig. 3.3.

3.3 Gate driving stage

The schematic of gate driving circuitry is shown in Fig. 3.6. The gate driver IC IXDN614 from IXYS is chosen as the primary gate driving stage, which has a peak source/sink current capability of 14 A and input to output propagation delay in the range of 50 ns – 70 ns [90]. For both turn-on and turn-off a common gate resistance is utilized. To ensure the MV isolation for the signal path and high $\mathrm{d}v/\mathrm{d}t$ noise immunity, the input signal to the gate driver is transmitted optically and is interfaced to the gate driver utilizing a fiber optic link.

To prevent the Miller induced false turn-on a Miller clamp circuit is integrated, which utilizes a comparator, logic gate and N-channel MOSFET with a very low on-state resistance [91]. The Miller clamp is activated after the MOSFET gate-source voltage reaches below 0 V during the turn-off. The Miller clamp provides a low-impedance path to the high $\mathrm{d}v/\mathrm{d}t$ induced Miller current and prevents gate-source voltage to rise above the SiC MOSFET threshold voltage during the complementary MOSFET turn-on in the half-bridge power module. For the power modules with NTC, a 555 timer based temperature monitoring circuit [92] is utilized, which outputs the frequency signal corresponding to the voltage across NTC. The frequency output signal is transmitted optically from the gate driver, which can be used for the baseplate temperature monitoring or protection purpose.

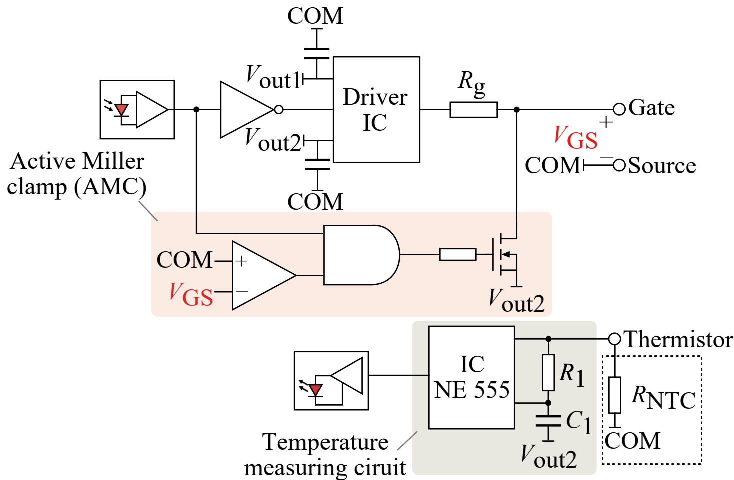


Fig. 3.6: Schematic of the gate driving stage.

3.4 Experimental validation

Picture of a PCB incorporating DC-DC isolated power supply and gate driving stage for a 10 kV half-bridge SiC MOSFET power modules is shown in Fig. 3.7.

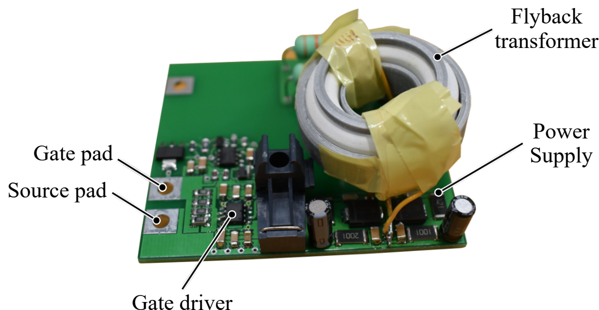


Fig. 3.7: Picture of a PCB incorporating DC-DC isolated power supply and gate driver for a 10 kV half-bridge SiC MOSFET power module. [D]

The Flyback transformer and gate driver PCB are tested under a DC voltage stress by utilizing SRS 20 kV, 0.5 mA high voltage power supply in an experimental test setup as shown in Fig.3.8. A DC voltage of 10 kV is applied for one hour between the primary and secondary windings of a Flyback transformer. In case of a gate driver PCB, DC voltage is applied between the input power terminals and output gate/source terminals. During the test leakage current is measured utilizing a Keithley 6485 Picoammeter that has +/- 10 fA resolution [93]. The leakage current for a Flyback transformer and gate driver PCB is measured to be 1 nA and 7 nA, respectively at DC voltage bias of 10 kV.

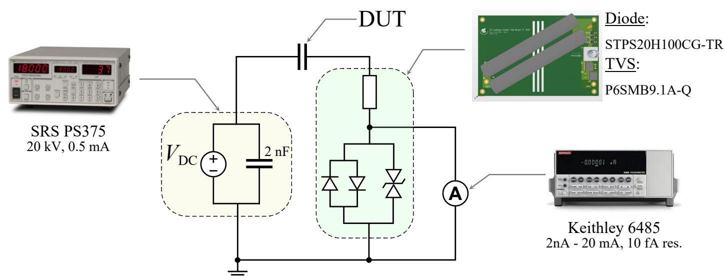


Fig. 3.8: Test setup for characterizing leakage current of device under test at high voltage DC bias.

An experimental test setup utilizing a 10 kV half-bridge power module as shown in the subset of Fig. 3.9, is used to measure the CM current through an isolation barrier of a gate driver PCB under the application of high $\mathrm{d}v/\mathrm{d}t$. Output of a

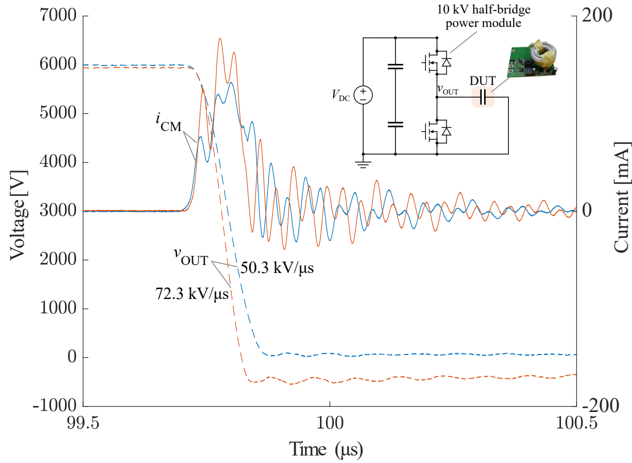


Fig. 3.9: Measured displacement current through isolation barrier of gate driver PCB for test at DC-link voltage of 6 kV in a half-bridge test setup.

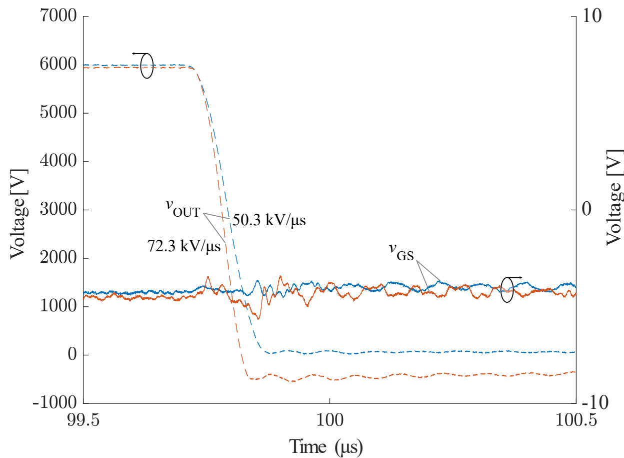


Fig. 3.10: Measured gate-source voltage of the HS SiC MOSFET for test at DC-link voltage of 6 kV in a half-bridge test setup.

half-bridge power module is connected to the gate and source pad of the gate driver PCB, whereas the input of a gate driver PCB is connected to ground. For the test, half-bridge output voltage, capacitive displacement or CM current and gate-source voltage of HS MOSFET is measured using a PPE 20 kV passive voltage probe [94], Pearson 2877 current monitor [95] and an optically isolated HVFO103 differential probe [96], respectively. The half-bridge power module is switched at DC-link voltage of 6 kV and switching frequency of 5 kHz with duty

cycle of 0.5, where dv/dt at the half-bridge output terminal can be changed by changing the external gate resistance of the gate driver. As can be seen in Fig. 3.9, the peak amplitude of capacitive displacement current through a gate driver PCB isolation barrier is measured to be 172 mA and 132 mA for a dv/dt of 72.3 kV/µs and 50.3 kV/µs, respectively. From the measured dv/dt and peak amplitude of displacement currents, the isolation-capacitance calculated using (3.1) range between 2.3 pF – 2.6 pF, which is in good agreement with the measured isolation-capacitance for a gate driver from impedance analyser as presented in Fig. 3.5.
The active Miller clamp function of a gate driver is validated by measuring a gate-source voltage of the HS SiC MOSFET in a same experimental test setup as presented in Fig. 3.9. The measured HS MOSFET gate-source voltage under the similar dv/dt and experimental conditions are presented in Fig. 3.10. The gate-source voltage of HS MOSFET remain clamped at the turn-off gate-source voltage level of -5 V. The high frequency oscillation measure in a gate-source voltage during the dv/dt is small in magnitude and well below the gate-source threshold voltage ($v_{\mathrm{GS(th)}} = 7$ V (25°C), 5.2 V (125°C) obtained for $i_{\mathrm{D}} = 100$ mA) of a 10 kV SiC MOSFET.

3.5 Summary

In this chapter, low isolation capacitance gate driver for a 10 kV SiC MOSFET half-bridge power module is presented. The Flyback based dual output voltage regulated power supply with a toroidal core transformer features a very low coupling capacitance of 1.4 pF (@ 1 MHz). To prevent Miller current induced false turn-on of a SiC MOSFET, an active Miller clamp function is integrated in the gate driving stage. The designed gate driver is subjected to DC voltage bias of 10 kV for an hour long duration, during which DC leakage current is measured to be 7 nA. To evaluate and validate the CM current and active Miller clamp function of the designed gate driver, a half-bridge setup with a 10 kV power module is utilized. The peak capacitive current is measured to be 172 mA at dv/dt of 72.3 kV/µs. The calculated isolation capacitance from measured peak capacitive displacement current and dv/dt, exhibit good agreement with the isolation capacitance measurements from impedance analyser. Under similar experimental conditions, the AMC function of the gate driver is validated by measuring gate-source voltage of the HS MOSFET. The gate-source voltage remains clamped at turn-off gate-source voltage level, preventing a false turn-on of a MOSFET under the high dv/dt switching transient resulting from a complementary device turn-on in a half-bridge power module.

Chapter 4

Dynamic switching characterisation of SiC MOSFET power modules

4.1 Introduction

For MV SiC MOSFET power module packaging, the module parasitic capacitance is found to be a critical design consideration compared to the inductance. This is primarily due to the fact that, in the case of similarly-rated (S_{rated}) MV and LV power modules, the energy stored in parasitic capacitances ($E_{\text{cap}} = \frac{1}{2} \cdot C \cdot V^2$) is significantly higher compared to the energy stored in parasitic inductances ($E_{\text{ind}} = \frac{1}{2} \cdot L \cdot I^2$) for MV power module in comparison to the LV power module considering a typical range of power module parasitics, i.e parasitic inductances and capacitances in the order of nH and pF, respectively as presented in publication [E]. In the case of MV power module packaging, the electrical parasitics of critical design consideration is found to be the capacitance resulting from the presence of electrically insulating ceramic substrate between the two copper layers of DBC as shown in Fig. 4.1 [57], [97]–[100].

These parasitic capacitances when subjected to the high $\mathrm{d}v/\mathrm{d}t$ switching tran-

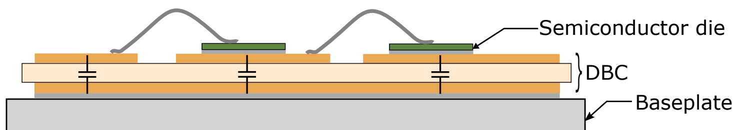


Fig. 4.1: Schematic showing the parasitic capacitance in power module packaging. [B]

sient get charged and discharged during every switching event, which introduce

displacement current. This displacement current forms a CM current path through the power module, heatsink and DC-link/decoupling capacitor, leading to an increased conducted EMI [101]–[105] and switching energy dissipation [106]. The magnitude of $\mathrm{d}v/\mathrm{d}t$, value of module parasitic capacitance and heatsink grounding impedance governs the amplitude of displacement current. In the case of MV SiC MOSFET, the magnitude of $\mathrm{d}v/\mathrm{d}t$ during the switching transient is order of magnitudes higher than their Si counter parts, which can lead to the peak amplitude of displacement currents to approach significant fraction of the SiC MOSFETs rated current. Therefore, in case of the MV power modules accurate prediction and quantification of the module parasitic capacitance is a key in order to design the power modules which can qualify for the EMC standards. Furthermore, analysis on the impact of module parasitic capacitance on SiC MOSFET in terms of switching transient and switching energy dissipation can provide insight on its severity considering intended use of the power module at medium voltage levels with relatively high switching frequencies.

The impact of power module parasitic capacitances on SiC MOSFET switching dynamics is analysed in an experimental case study using custom-packaged 10 kV half-bridge power modules. A well defined approach is proposed, to dissect the switching energy dissipation. Using this approach the impact of module parasitic capacitance is shown with quantitative measurements in terms of CM current and added switching energy dissipation in an experimental case study.

In a different case study, the impact of SiC JBS diode on SiC MOSFET switching transient and switching energy dissipation is analysed, using a proposed switching energy dissection method. The study focuses on evaluating the change in switching energy dissipation for a half-bridge power module with and without an anti-parallel SiC JBS diode in terms of (i) added switching energy dissipation for the power module with an anti-parallel SiC JBS diode due to added output capacitance of a JBS diode in parallel to the MOSFET and (ii) performance of a SiC MOSFET body diode in terms of reverse recovery for the power module without anti-parallel SiC JBS diode.

4.2 Impact of power module parasitic capacitances on the SiC MOSFET switching transients

4.2.1 Device under test

In the experimental case study, two 10 kV half-bridge SiC MOSFET power modules A and B are utilised. These power modules are packaged using a

0.63 mm Aluminium Nitride (AlN) substrate soldered on a 3 mm thick AlSiC baseplate. The DBC is populated with third generation 10 kV SiC MOSFET and SiC JBS diode dies. These two modules have the similar terminal configuration, however they differ in terms of their DBC layout. The distributed parasitic

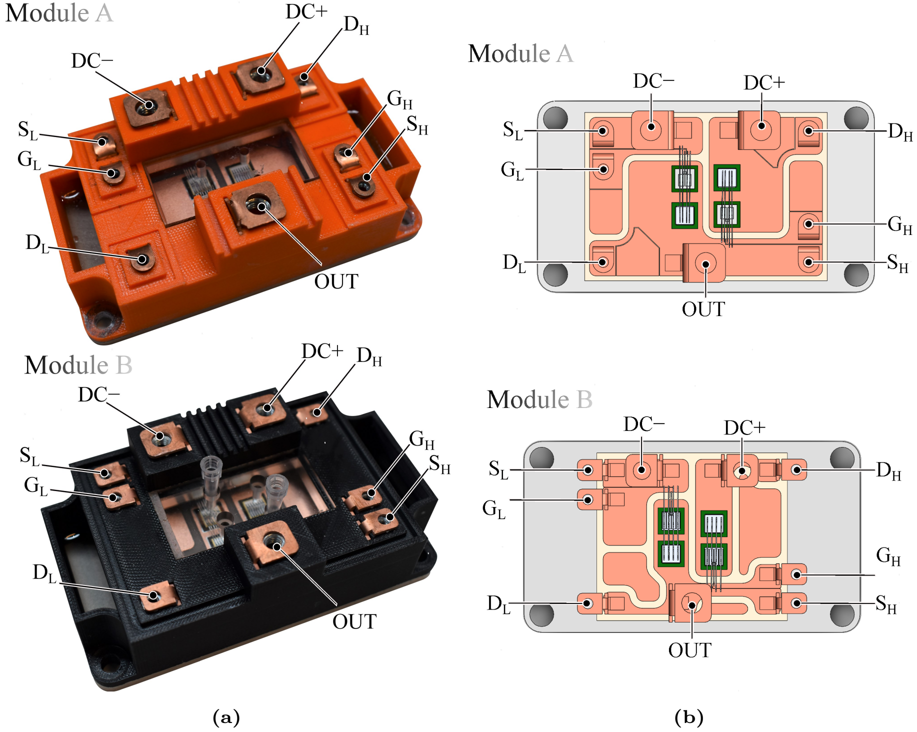


Fig. 4.2: (a) Picture and (b) Solidworks rendering for the 10 kV half-bridge SiC MOSFET power modules A and B with different DBC layouts. [B]

capacitances inside the power module due to the ceramic substrate between the top and bottom copper layers of the DBC substrate are denoted as $C_{\sigma+}$, $C_{\sigma\mathrm{GH}}$, $C_{\sigma\mathrm{OUT}}$, $C_{\sigma\mathrm{GL}}$ and $C_{\sigma-}$. The physical reference of these parasitic capacitances within the power modules is shown in Fig. 4.3. In case of the half bridge power module, parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ experience high $\mathrm{d}v/\mathrm{d}t$ during the switching transients. Therefore, from power module EMI and switching performance point of view the parasitic capacitance $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ have dominant impact and are of crucial importance.

The parasitic capacitances extracted from ANSYS Q3D for power modules A and B are listed in Table 4.1. For parasitic extraction, the permittivity for an individual material inside a power module package is assigned from the manufacturer datasheet.

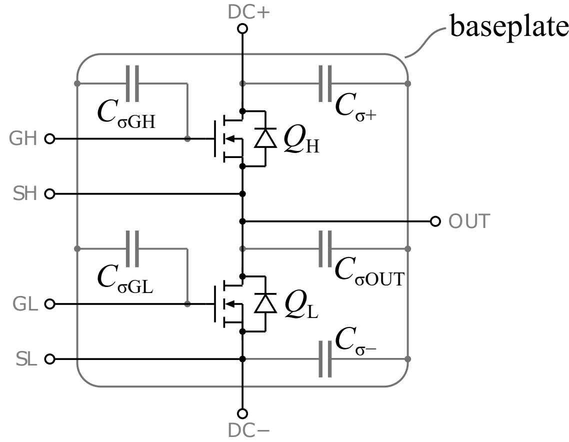


Fig. 4.3: Schematic representation of the distribution of the parasitic capacitances in a half bridge power module. [B]

Table 4.1: Values of parasitic capacitances obtained from ANSYS Q3D for the 10 kV half-bridge SiC MOSFET power modules A and B. (All in [pF]) [B]

Module	$C_{\sigma+}$	$C_{\sigma\mathrm{GH}}$	$C_{\sigma\mathrm{OUT}}$	$C_{\sigma\mathrm{GL}}$	$C_{\sigma-}$
A	108	20.5	159.2	23.5	47.5
B	68.1	12.4	81.4	35.6	32.7

4.2.2 Impedance network between the power module and heatsink

An equivalent impedance network representation between the power module output terminal and heatsink, can enable accurate prediction of displacement currents due to the power module parasitic capacitance for a given voltage excitation [101].

In most power electronics applications a low impedance ground connection is provided between the heatsink and ground to keep heatsink at ground potential due to safety reasons. With such configuration, the module parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ experience the same $\mathrm{d}v/\mathrm{d}t$ appearing at the output terminal of a half bridge. Since, power module parasitic capacitance $C_{\sigma+}$, $C_{\sigma\mathrm{GL}}$ and $C_{\sigma\text{-}}$ are referenced to a fixed voltage potential, they do not experience this $\mathrm{d}v/\mathrm{d}t$. During the turn-on and turn-off switching transients, $\mathrm{d}v/\mathrm{d}t$ appearing at the output terminal will introduce displacement currents that charge or discharge the parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$.

An equivalent impedance network between the half-bridge output terminal and ground, which can be utilized for predicting the ground current is shown in Fig. 4.4. In Fig. 4.4 Z_1 is the equivalent impedance between the power module

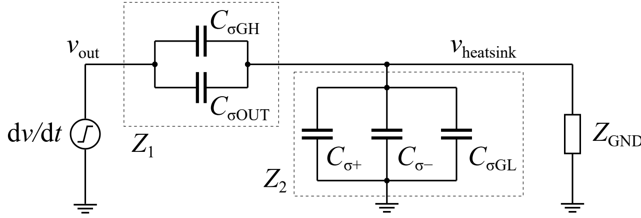


Fig. 4.4: Schematic of an equivalent impedance network between the half-bridge output terminal and ground. [B]

output terminal and heatsink, which is modelled as the parallel combination of module parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$. Whereas, the impedance between a heatsink and ground is modeled as the parallel combination of impedance Z_2 and Z_{GND}. The impedance Z_2 is an equivalent impedance between the power module DC as well as low side gate-source terminals and heatsink, which is modeled as the parallel combination of module parasitic capacitances $C_{\sigma+}$, $C_{\sigma\mathrm{GL}}$ and $C_{\sigma\text{-}}$ The magnitude of the displacement currents due to parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ due to the $\mathrm{d}v/\mathrm{d}t$ appearing at the half-bridge output terminal can be determined as $i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} \approx C_{\sigma\mathrm{OUT}} + C_{\sigma\mathrm{GH}} \cdot \mathrm{d}(v_{\mathrm{OUT}} - v_{\mathrm{heatsink}})/\mathrm{d}t$.

4.2.3 Experimental test bench

In order to evaluate the dynamic switching performance of 10 kV SiC MOSFET half-bridge power modules, it is required to characterise them in an inductive switching test setup such as double pulse test (DPT). The power modules are tested in a double pulse test setup, whose schematic and picture are shown in Fig. 4.5. In the test setup, a power module is connected to the two paralleled 50 μF, 5 kV rated DC-link polypropylene film capacitors through a low inductance busbar connection. The high voltage DC power supply (XR 6000-1.0/415/+HS+LXI, XR 10000-0.2/415/+HS+LXI) is used to charge the DC-link capacitors at desired voltage levels. An air core inductor with inductance value of 47 mH is utilized as a load inductor. To minimize the influence of the load inductor parasitic capacitance on SiC MOSFET switching dynamics and losses, an air core inductor with a relatively low value of equivalent parallel parasitic capacitance ($C_{\mathrm{L}} \approx 12$ pF) is utilized. For the SiC MOSFET power module, a custom made low isolation-capacitance (≤ 3 pF) MV gate drivers are utilised. For the gate driver external gate resistance is chosen to be of 20 Ω. The power module is placed on a temperature controlled heatsink, which is connected to a DC- terminal of the DC-link busbar using a low impedance ground connection. The module currents $i_{\mathrm{DC+}}$, $i_{\mathrm{DC-}}$, i_{OUT} and i_{GND} are recorded at the DC+, DC−, output and heatsink grounding connections, respectively. These current

(a)

(b)

Fig. 4.5: (a) Schematic and (b) picture of the double pulse test bench. [B]

measurements are recorded using the 70 MHz – 200 MHz high bandwidth Pearson 2878 and 2877 current monitors [95], [107]. The connection from the DC+ and DC− terminals of the power module to the DC−link busbar is provided using short wires on which the Pearson current monitors are inserted. Each of this short wire connection introduces approximately 50 nH of the additional inductance to the main power loop. The output voltage at the half-bridge terminal is measured utilizing 100 MHz PPE 20 kV passive probe [94]. Whereas, an optically isolated HVFO103 differential probe [96] is utilized to measure the LS MOSFET gate-source voltage.

4.2.4 Analysis of SiC MOSFET turn-on and turn-off switching transients

The impact of power module parasitic capacitances on SiC MOSFET turn-on and turn-off switching transient is analysed in this section using the double pulse test circuit shown in Fig. 4.5 and the measured turn-on and turn-off switching waveforms for a single-chip 10 kV half-bridge power module in a double pulse experimental test setup at temperature of 25°C.

Turn-on switching transient

Measured turn-on switching waveforms for the half-bridge power module at DC-link voltage of 6 kV and load current level of 14 A is presented in Fig. 4.6. The turn-on switching dynamics corresponding to the time interval $t_0 - t_4$ in Fig. 4.6 is analysed and discussed as follows:

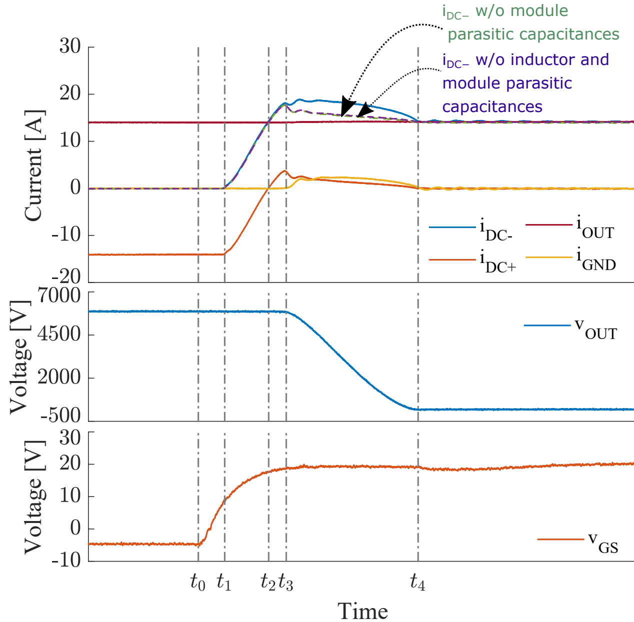


Fig. 4.6: Measured turn-on switching waveforms for a 10 kV half-bridge power module in an experimental double pulse test setup. (V_{DC} = 6 kV and i_L = 14 A) [B]

- $t_0 - t_1$: Turn-on gate command is applied to the LS MOSFET Q_L at time t_0. Upon receiving the turn-on command, the gate-source voltage (v_{GS}) starts to increase from the turn-off gate bias level and reaches the gate-source threshold voltage level ($v_{GS(th)}$) at time t_1. At this time instant LS MOSFET starts conducting.

- $t_1 - t_2$: The load current commutation from the HS MOSFET (body diode) and JBS diode begins as LS MOSFET starts conducting the load current. At time t_2, the commutation of the load current from the HS diode to the LS MOSFET is completed. At this time instant gate-source voltage of the LS MOSFET reaches the Miller voltage level.

- $t_2 - t_4$: The time interval $t_2 - t_4$ is commonly termed as Miller region. During this time interval, the HS diode goes through reverse recovery and stops conducting the current. And, the voltage at the half-bridge output terminal changes from the DC-link voltage level to the MOSFET on-state voltage level. During the half-bridge output voltage transition, the combined HS MOSFET and JBS diode output capacitance gets charged through the LS MOSFET, which incurs switching energy dissipation within LS MOSFET.

  In addition to this, the module parasitic capacitance $C_{\sigma\mathrm{OUT}}$, $C_{\sigma\mathrm{GH}}$ discharges and inductor parasitic capacitance C_L charges with the displacement currents $i_{\sigma\mathrm{OUT}}$, $i_{\sigma\mathrm{GH}}$ and i_{C_L} respectively due to the negative rate of change of voltage ($\mathrm{d}v/\mathrm{d}t$) at the half bridge output terminal. The increased magnitude of the module current $i_{\mathrm{DC-}}$ and different waveform trajectory in comparison to current $i_{\mathrm{DC+}}$ during the time interval $t_2 - t_4$, is associated with the displacement currents due to module parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$, as shown in Fig. 4.6. The impact of displacement current due to the inductor parasitic capacitance is insignificant owing to its very small value of parasitic capacitance. The displacement currents $i_{\sigma\mathrm{OUT}}$, $i_{\sigma\mathrm{GH}}$ and i_{C_L} during the half-bridge output voltage change conduct through the LS MOSFET channel, which incur losses that add on to the overall switching energy dissipation.

  Within this time interval, LS MOSFET also conducts the current due to discharging of its own and anti-parallel JBS diode output capacitances. However, this current can not be measured at the DC- terminal of the half bridge power module and therefore the energy dissipation in LS MOSFET due to discharging of its own and JBS diode output capacitance can not be measured, since these current path is constricted within the LS MOSFET and the combined MOSFET and JBS diode output capacitance itself [108].

  It is important to mention that the gate-source voltage does not remain flat corresponding to the load current level i_L during the Miller region or time interval $t_2 - t_4$. Due to increased channel current through LS MOSFET at the beginning of time interval $t_2 - t_4$, will lead to increase in gate-source voltage that corresponds to the channel current. The increase in gate-source voltage will result in an increased time interval $t_2 - t_4$ and thus lower $\mathrm{d}v/\mathrm{d}t$. This is due to decrease in the MOSFET gate-source

and turn-on gate drive voltage potential difference, that results in lower gate current magnitude that charges the MOSFET Miller or gate-drain capacitance.

Turn-off switching transient

Measured turn-off switching waveforms for the half-bridge power module at DC-link voltage of 6 kV and load current level of 14 A is presented in Fig. 4.7. The turn-off switching dynamics corresponding to the time interval $t_5 - t_7$ in Fig. 4.7 is analysed and discussed as follows:

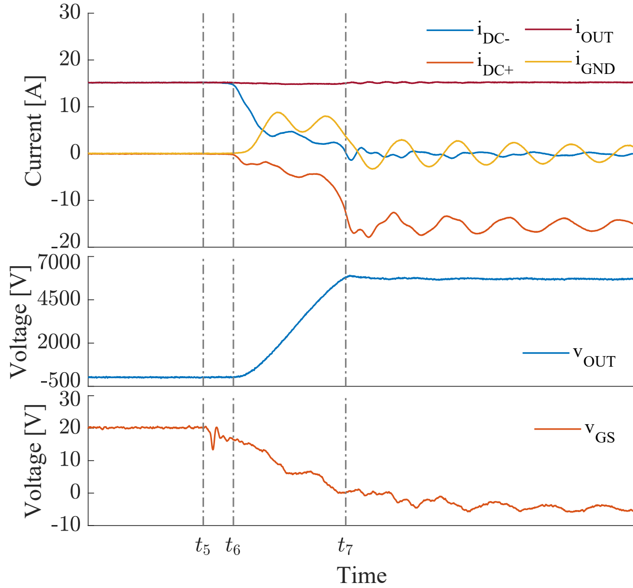


Fig. 4.7: Measured turn-off switching waveforms for a 10 kV half-bridge power module in an experimental double pulse test setup. (V_{DC} = 6 kV and i_L = 14 A) [B]

- $t_5 - t_6$: Turn-off gate command is applied to the LS MOSFET at time t_5. Upon, receiving the turn-off command, the gate-source voltage (v_{GS}) starts to decrease from the tun-on gate voltage level and reaches the Miller level at time t_6.

- $t_6 - t_7$: The time interval $t_6 - t_7$ correspond to the Miller region in case of the turn-off switching transient. During this time interval, the voltage at the half-bridge output terminal changes from the MOSFET on-state voltage level to the DC-link voltage level. The current through LS MOSFET decreases from the load current level and stops conducting the current, when gate-source voltage is lower than the threshold voltage. In the presented case, this occurs before time t_7, and the current measured

at the DC- terminal of the half bridge power module is due to the charging of the the combined output capacitances of the LS MOSFET and JBS diode [108].

The current i_{OUT}, measured at the output terminal of a half-bridge module during time interval $t_6 - t_7$ constitutes the charging and discharging currents of the combined output capacitances of the HS and LS MOSFETs and JBS didoes, respectively. In addition to this, i_{OUT} also constitutes the displacement currents charging the module parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$, as well as the displacement current discharging the inductor parasitic capacitance C_{L}.

Contrary to the turn-on, during the turn-off switching transient, discharging current due to the power module parasitic capacitances does not conduct through the LS MOSFET channel and therefore does not produce Joule heating.

4.2.5 Discussion on an indirect measurement method utilized to obtain the power module parasitic capacitance related displacement current

An indirect measurement methodology is proposed to obtain the module parasitic capacitance related displacement current, since this current can not be measured directly. The power module capacitance related displacement current for, both turn-on and turn-on switching transients is obtained utilizing the accessible half-bridge power module current measurements $i_{\mathrm{DC+}}$, $i_{\mathrm{DC\text{-}}}$ and i_{OUT}. The proposed indirect measurement methodology is validated by the experimental results obtained in a double pulse test setup.

For the double pulse test circuit schematic presented in Fig. 4.5a with the perfectly grounded heatsink, it is reasonable to consider that no displacement currents flow through capacitance $C_{\sigma+}$, $C_{\sigma\mathrm{GL}}$ and $C_{\sigma-}$, as almost no $\mathrm{d}v/\mathrm{d}t$ appear across these capacitances during the switching transients. Although in practice, the voltage drop due to stray inductance in the ground path can result in a high frequency voltage oscillations at heatsink node, although its influence on the voltage change across module parasitic capacitance $C_{\sigma+}$, $C_{\sigma\mathrm{GL}}$ and $C_{\sigma-}$ is negligible in comparison to the voltage change across capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$. With this consideration ground current can be considered to be equal to the total sum of displacement currents $i_{\sigma\mathrm{OUT}}$ and $i_{\sigma\mathrm{GH}}$. Also, the half-bridge power module currents $i_{\mathrm{DC+}}$ and $i_{\mathrm{DC-}}$ can be considered almost equal to the, currents at the HS MOSFET source terminal and LS MOSFET drain terminals, respectively. For a presented case study, the passive voltage probe utilized to measure a half-bridge output voltage and HS gate driver, also introduce capacitive couplings that are external to the power module. The displacement currents introduced due to external capacitive couplings is denoted as $i_{\mathrm{C_{AUX}}}$,

which conducts through the LS MOSFET due to the negative $\mathrm{d}v_{\mathrm{OUT}}/\mathrm{d}t$ during the turn-on switching transient.

Applying Kirchhoff's current law (KCL) at the half-bridge output terminal, module current $i_{\mathrm{DC-}}$ can be identified as,

$$i_{\mathrm{DC-}} = i_{\mathrm{DC+}} + i_{\mathrm{OUT}} + i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} + i_{\mathrm{C_{AUX}}} \tag{4.1}$$

The equation above can be solved for module parasitic capacitance related displacement currents during the turn-on switching transient.

$$i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} = i_{\mathrm{DC-}} - i_{\mathrm{DC+}} - i_{\mathrm{OUT}} - i_{\mathrm{C_{AUX}}} \tag{4.2}$$

and

$$i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} = (C_{\sigma\mathrm{OUT}} + C_{\sigma\mathrm{GH}}) \cdot \frac{\mathrm{d}}{\mathrm{d}(t_4 - t_3)} v_{\mathrm{OUT}} \tag{4.3}$$

The coupling capacitances of HS gate driver and high voltage passive probe are less than 3 pF, which are significantly lower compared to the module parasitic capacitances. As a result, the displacement current $i_{C_{\mathrm{AUX}}}$ is relatively smaller compared to the power module parasitic capacitance induced displacement currents $i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}$. With this consideration, (4.2) can be simplified as,

$$i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} \approx i_{\mathrm{DC-}} - i_{\mathrm{DC+}} - i_{\mathrm{OUT}} \tag{4.4}$$

The displacement current $i_{C_{\mathrm{L}}}$ due to inductor parasitic capacitance during the turn-on switching transient can be obtained as,

$$\begin{aligned} i_{\mathrm{C_L}} &= i_{\mathrm{OUT}} - i_{\mathrm{L}} \\ &\left[i_{\mathrm{L}} = i_{\mathrm{OUT(t_2)}}, v_{\mathrm{OUT}} = V_{\mathrm{DS(LS)}}\right] \\ &= C_{\mathrm{L}} \cdot \frac{\mathrm{d}}{\mathrm{d}(t_4 - t_3)} (V_{\mathrm{DC+}} - v_{\mathrm{OUT}}) \end{aligned} \tag{4.5}$$

Utilizing similar approach as presented for the turn-on switching transient, the displacement currents due to the power module and inductor parasitic capacitances in case of turn-off switching transient can be obtained as (4.6) and (4.7), respectively.

$$\begin{aligned} i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} &= i_{\mathrm{DC+}} - i_{\mathrm{DC-}} + i_{\mathrm{OUT}} - i_{\mathrm{C_{AUX}}} \\ &= (C_{\sigma\mathrm{OUT}} + C_{\sigma\mathrm{GH}}) \cdot \tfrac{\mathrm{d}}{\mathrm{d}(t_7 - t_6)} v_{\mathrm{OUT}} \end{aligned} \tag{4.6}$$

and

$$\begin{aligned} i_{\mathrm{C_L}} &= i_{\mathrm{OUT}} - i_{\mathrm{L}} \\ &\left[i_{\mathrm{L}} = i_{\mathrm{OUT(t_6)}}, v_{\mathrm{OUT}} = V_{\mathrm{DS(LS)}})\right] \\ &= C_{\mathrm{L}} \cdot \frac{\mathrm{d}}{\mathrm{d}(t_7 - t_6)} (V_{\mathrm{DC+}} - v_{\mathrm{OUT}}) \end{aligned} \tag{4.7}$$

Experimental and simulation based validation

Fig 4.8 presents the comparison of a measured ground current i_{GND} with a simulated ground current ($i_{\mathrm{GND(sim)}}$) and the indirectly obtained module parasitic capacitance related displacement currents ($i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}$) in case of turn-on and turn-off switching transients for power modules A and B at DC-link voltage of 6 kV and load current of 14 A.

The simulated ground current $i_{\mathrm{GND(sim)}}$ is obtained from LTspice simulation by utilizing an equivalent impedance network between the half bridge output terminal to ground as presented in Fig. 4.4. For the simulation, measured half-bridge output voltage is utilized as the voltage excitation. As can be seen in Fig. 4.8, the measured and simulated ground currents exhibit similar amplitude and frequency response, for both turn-on and turn-off switching transients. However, slight difference in terms of the amplitude of $i_{\sigma\mathrm{OUT}}+i_{\sigma\mathrm{GH}}$ is assigned to the displacement currents due to capacitive couplings introduced by the HS gate driver and high voltage passive probe. Measured peak amplitude of the ground currents during turn-on switching transient in case of power modules A and B are 2.4 A and 1.8 A for the turn on $\mathrm{d}v/\mathrm{d}t$ of 11.2 kV/µs and 15.6 kV/µs, respectively. Whereas, in the case of turn-off switching transient the peak amplitude of ground currents for power modules A and module B are 8 A and 5 A for the turn-off $\mathrm{d}v/\mathrm{d}t$ of 30.7 kV/µs and 39.3 kV/µs, respectively. Under

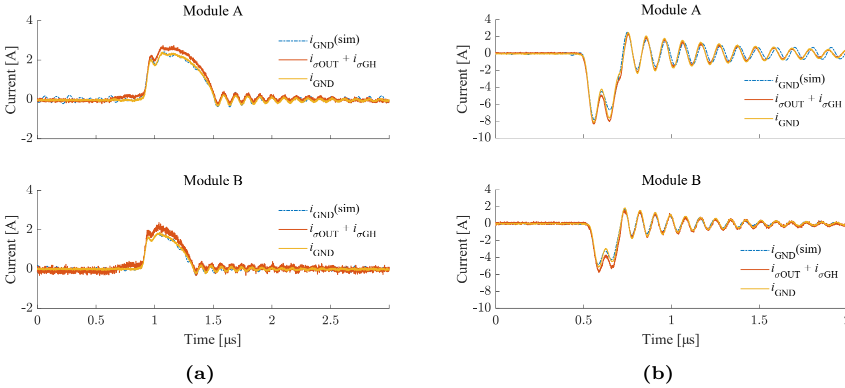


Fig. 4.8: Experimentally measured/extracted and simulated ground currents during (a) turn-on (b) turn-off switching transient for power modules A and B in the case where heatsink is shorted to ground. (Test conditions V_{DC} = 6 kV, i_{L} = 14 A) [B]

similar test conditions (i.e temperature, DC-link voltage, load current level, gate resistance and gate driving voltage) the turn-on and turn-off $\mathrm{d}v/\mathrm{d}t$ are higher for module B in comparison to module A, which is due to the impact of module parasitic capacitance $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ as will be discussed in Section 4.2.6. The peak amplitude of measured ground current is lower for module B in

comparison to module A even at higher turn-on and turn-off dv/dt switching transient, which correspond to the reduced power module parasitic capacitance for module B in comparison to module A.

4.2.6 Analysis of power module parasitic capacitance impact on the turn-on and turn-off switching energy dissipation

The impact of power module parasitic capacitance on the turn-on switching energy dissipation is analysed by splitting the measured turn-on energy dissipation into five segments, which are denoted as E_{on1}, E_{on2}, $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$, $E_{\sigma\mathrm{L}}$ and $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$. Contribution from each of these switching energy segments to the total turn-on switching energy dissipation is graphically illustrated in Fig. 4.9 and is discussed in detail.

Switching energy dissipation during the turn-on transient time interval $t_1 - t_2$

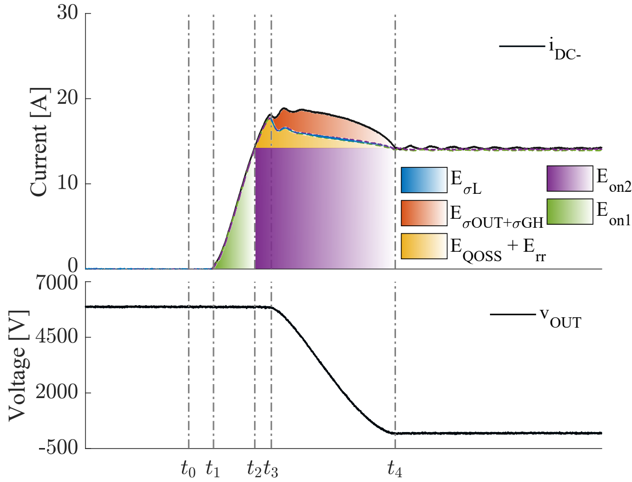


Fig. 4.9: Illustration of split in turn-on switching energy dissipation. (Test conditions V_{DC} = 6 kV, i_{L} = 14 A)) [B]

is termed as E_{on1} and is derived from (4.8).

$$E_{\mathrm{on1}} = \int_{t1}^{t2} i_{\mathrm{DC-}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{4.8}$$

The switching energy dissipation due to constant load current magnitude i_{L} ($i_{\mathrm{L}} = i_{\mathrm{OUT(t2)}}$) during the time interval $t_2 - t_4$ is termed as E_{on2} and is derived

from (4.9).

$$E_{\mathrm{on2}} = \int_{t2}^{t4} i_{\mathrm{L}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \quad \left[i_{\mathrm{L}} = i_{\mathrm{OUT(t_2)}}\right] \tag{4.9}$$

Switching energy dissipation due to the Joule heating from the charging of HS MOSFET and JBS diode output capacitance as well as the diode reverse recovery charge combined, is termed as $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ and is derived from (4.10).

$$E_{\mathrm{QOSS}} + E_{\mathrm{rr}} = \int_{t2}^{t4} i_{\mathrm{DC+}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{4.10}$$

Utilizing the power module and inductor parasitic capacitance induced displacement currents $i_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ and $i_{\mathrm{C_L}}$ based on (4.2) and (4.5) respectively, the switching energy dissipation in LS MOSFET due to discharging and charging of the power module and inductor parasitic capacitance can be obtained from (4.11) and (4.12),

$$E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}} = \int_{t3}^{t4} (i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}) \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{4.11}$$

$$E_{\sigma\mathrm{L}} = \int_{t3}^{t4} i_{\mathrm{C_L}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{4.12}$$

The total turn-on switching energy dissipation E_{on} is given as,

$$\begin{aligned} E_{\mathrm{on}} &= E_{\mathrm{on1}} + E_{\mathrm{on2}} + E_{\mathrm{QOSS}} + E_{\mathrm{rr}} + E_{\sigma\mathrm{L}} + E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}} \\ &= \int_{t1}^{t4} i_{\mathrm{DC-}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \end{aligned} \tag{4.13}$$

Turn-on switching energy dissipation

The turn-on switching energy dissipation and its split as well as the turn-on $\mathrm{d}v/\mathrm{d}t$, measured at DC-link voltage (V_{DC}) of 6 kV and load current (i_{L}) of 0 A – 14 A for power modules A and B is shown in Fig. 4.10. It can be identified from Fig. 4.10, that the turn-on $\mathrm{d}v/\mathrm{d}t$ decreases with the increase in load current magnitude. With increase in load current magnitude, the gate-source Miller plateau voltage shift towards higher value. This reduces the magnitude of gate current charging the reverse transfer capacitance C_{GD}, resulting in an increased voltage fall time interval ($t_3 - t_4$) and thus lowering the turn-on $\mathrm{d}v/\mathrm{d}t$. Under identical experimental condition and for the similar load current levels, the turn-on $\mathrm{d}v/\mathrm{d}t$ for module A is lower than module B. The lower turn-on $\mathrm{d}v/\mathrm{d}t$ for module A, is due to an increase in gate-source voltage plateau during

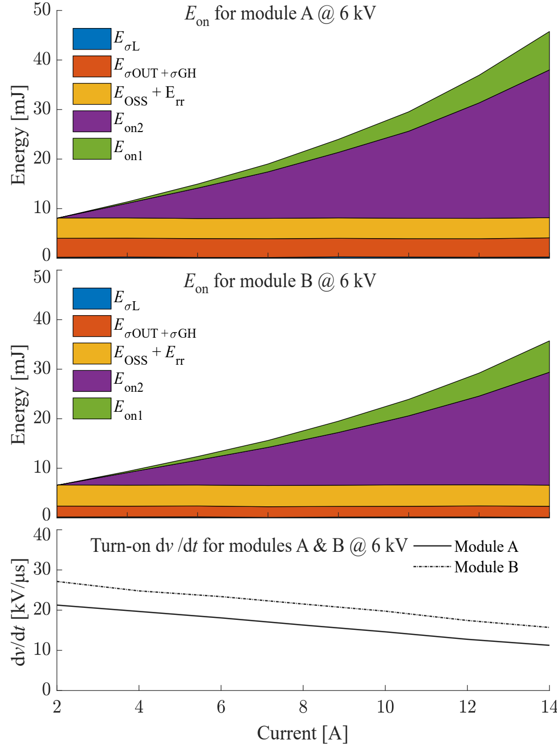


Fig. 4.10: Comparison of the turn-on switching energy dissipation E_{on} and dv/dt for modules A and B at DC-link voltage of 6 kV and load currents of 0 A – 14 A. [B]

the Miller region because of the higher value of module parasitic capacitance resulting in an increased magnitude of the displacement current through LS MOSFET channel. The turn-on dv/dt for module A is approximately 28 % lower compared to module B for 6 kV, 14 A test.

It can be observed from Fig. 4.10 that switching energy dissipation E_{on1} and E_{on2} increase with the load current. This is due to both increase in the load current magnitude and time intervals $t_1 - t_2$ as well as $t_3 - t_4$, because of the shift in gate-source Miller plateau voltage level to higher value as the load current increases.

The switching energy dissipation E_{on1} for the module A is slightly higher than the module B, which is resulting from the positive shift in plateau voltage resulting into the increase in the time interval $t_1 - t_2$.

An indirect impact of the module parasitic capacitance can be clearly observed, when comparing the switching energy dissipation E_{on2} for power

modules A and B. The increased time interval $t_3 - t_4$ for module A in comparison to module B results in the higher magnitude of E_{on2} for module A. The E_{on2} for module A is 29.8 mJ, which is approximately 7 mJ higher in comparison to module B for 6 kV, 14 A test.

The switching energy dissipation $E_{\sigma\text{OUT}+\sigma\text{GH}}$, $E_{\sigma\text{L}}$ and E_{QCOSS} occur during the time interval $t_2 - t_4$, due to Joule heating incurred from the charging or discharging of the power module, inductor and combined HS MOSFET as well as JBS diode output parasitic capacitances. Since these switching energy dissipation occur due to losses from the charging and discharging of the parasitic capacitance, the decrease in turn-on $\mathrm{d}v/\mathrm{d}t$ or increase of time interval $t_2 - t_4$ does not impact these losses and are therefore are not dependant on the load current.

The measured switching energy dissipation $E_{\text{QOSS}} + E_{\text{rr}}$ obtained from (4.10) for power modules A and B, is in the range of 4 mJ – 4.2 mJ, which is almost constant at the DC-link voltage of 6 kV for load current of up to 14 A. To further strengthen the analysis, measured $E_{\text{QOSS}} + E_{\text{rr}}$ from the DPT is compared with $E_{\text{OSS(Static)}}$ which is obtained from the static capacitance measurements of the third generation 10 kV SiC MOSFET and JBS diode dies using the Keysight B1506 curve tracer [63]. The capacitance measurements in curve tracer is limited up to 3 kV DC-bias due to its maximum output voltage limit. For the voltages above 3 kV the capacitance is extrapolated by curve fitting as shown in Fig 4.11a. The combined MOSFET and JBS diode output capacitance as well as reverse recovery related charge is measured from the DPT based on (4.14), and compared with the $Q_{\text{OSS(static)}}$ that is obtained from static curve tracer capacitance measurements. From, the comparison shown in 4.11b, it can be observed that the $Q_{\text{OSS}} + Q_{\text{rr}}$ obtained from DPT measurements for lower (2 A) and higher (14 A) end of the load current values are in good agreement with the $Q_{\text{OSS(Static)}}$, indicating negligible charge due to diode reverse recovery.

$$Q_{\text{OSS}} + Q_{\text{rr}} = \int_{t2}^{t4} i_{\text{DC}+} \cdot \mathrm{d}t \tag{4.14}$$

The switching energy dissipation E_{QOSS} is due to the Joule heating resulting in LS MOSFET due to charging of the HS MOSFET and JBS diode output capacitance. This charging current conducting though the LS MOSFET with voltage potential $V_{\text{OUT}} = V_{\text{DC}+} - V_{\text{Q}_\text{H}}$, results in the energy dissipation which can be analytically obtained as $Q_{\text{OSS}} \cdot V_{\text{DC}} - E_{\text{OSS}}$ from solving for $\int i_{\text{DC}+} \cdot (V_{\text{DC}+} - V_{\text{Q}_\text{H}}) \cdot \mathrm{d}t$. Meaning that the measured switching energy dissipation $E_{\text{QOSS}} + E_{\text{rr}}$, needs to compared with the $Q_{\text{OSS(Static)}} \cdot V_{\text{DC}} - E_{\text{OSS(Static)}}$ and not $E_{\text{OSS(Static)}}$. As can be seen in Fig:4.11c, the measured $E_{\text{QOSS}} + E_{\text{rr}}$ at the DC-link voltage of 6 kV at high as well as low end of load current range, is in good agreement with $Q_{\text{OSS(Static)}} \cdot V_{\text{DC}} - E_{\text{OSS(Static)}}$ calculated from the curve tracer capacitance measurement data, indicating almost negligible contribution of E_{rr} due to the diode reverse recovery.

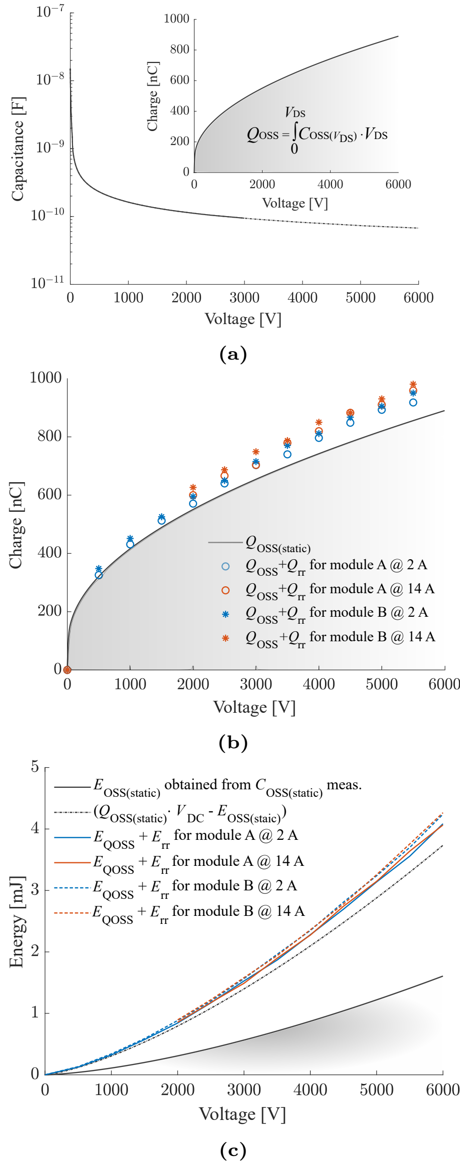


Fig. 4.11: (a) Output capacitance ($C_{\mathrm{OSS(Static)}}$) measurement for the 10 kV SiC MOSFETs and JBS diode obtained form B1506 curve tracer, (b) comparison of the output capacitance charge ($Q_{\mathrm{OSS(Static)}}$) with output capacitance as well as reverse recovery related charge obtained form the double pulse test setup (c) comparison of the stored energy on the output capacitance charge ($E_{\mathrm{OSS(Static)}}$) with switching energy dissipation $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ for power modules A and B. [B]

The impact of module parasitic capacitance can identified when comparing the $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ for power modules A and B. $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ for module A is approximately 3.8 mJ for the DC-link voltage of 6 kV, which is higher than that of the 2.2 mJ for module B. This accounts for approximately 8.3 % and 6.1 % of the total turn-on switching energy dissipation for module A and B respectively. The ratio of $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ to the total turn-on energy will increase with lower value of gate resistance, due to the lower magnitude of E_{on2} resulting from the reduced voltage fall time but the switching energy dissipation $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ will remain unchanged.

The measured switching energy dissipation $E_{\sigma\mathrm{L}}$ for power modules A and B are identical, and is in the range of 0.1 – 0.3 mJ for the DC-link voltage of 6 kV and load current of up to 14 A.

The total turn-on switching energy dissipation E_{on} for module A and B at DC-link voltage of 6 kV and load current of 14 A is 45.7 mJ and 35.7 mJ, respectively. The 22 % increase in E_{on} for module A is mainly due to the increase in E_{on2} and $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ as an direct and indirect impact of the power module parasitic capacitances.

It is worth mentioning that, actual switching energy dissipation E^{*}_{on}, is higher than the measured switching energy dissipation E_{on}, by value of E_{OSS} [108]. This is due to the fact that the discharging current of LS MOSFET and JBS diode can not be measured at power module DC- terminal since the current path is confined within the power semiconductor devices itself. Thus, actual switching energy dissipation can be obtained by adding up the stored energy E_{OSS} on device output capacitance to the measured turn-on switching energy dissipation as presented in (4.15).

$$E^{*}_{\mathrm{on}} = E_{\mathrm{on}} + E_{\mathrm{OSS(Static)}} \tag{4.15}$$

Turn-off switching energy dissipation

The turn-off switching energy dissipation as well as the turn-off $\mathrm{d}v/\mathrm{d}t$, measured at DC-link voltage of 6 kV and load current of 0 A – 14 A for power modules A and B is shown in in Fig. 4.12. Contrary to the turn-on, for turn-off switching transient $\mathrm{d}v/\mathrm{d}t$ increases as the load current increases. During turn-off switching transient, it is the load current magnitude which predominantly determines the charging and discharging rate of the combined LS and HS MOSFET as well as JBS diode output capacitance [108]. Therefore, in case of turn-off switching transient the load current has more influence on the turn-off $\mathrm{d}v/\mathrm{d}t$ or the voltage rise time interval $t_6 - t_7$ in comparison to the gate resistance. This can be identified with the linear dependence of measured turn-off $\mathrm{d}v/\mathrm{d}t$ on the load current magnitude. During turn-off switching transient, the module parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ act as a snubber, as they are in parallel to the LS MOSFET. This results into the lower turn-off $\mathrm{d}v/\mathrm{d}t$ for power module with higher parasitic capacitance. However, the displacement current charging

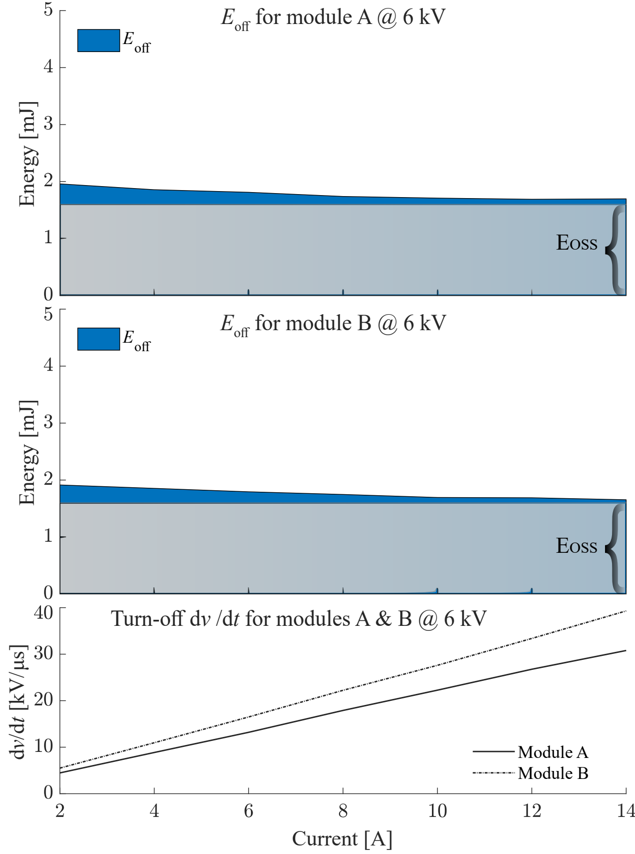


Fig. 4.12: Comparison of the turn-off switching energy dissipation E_{off} and $v/\mathrm{d}t$ for modules A and B at DC-link voltage of 6 kV and load currents of 2 A – 14 A. [B]

module parasitic capacitance does not conduct through the MOSFET and therefore does not produce Joule heating in the LS MOSFET channel. The turn-off $\mathrm{d}v/\mathrm{d}t$ for power modules A and B is measured to be 30.7 kV/µs and 39.3 kV/µs, respectively for tests at 6 kV, 14 A. The turn-off switching energy dissipation is derived from (4.16).

$$E_{\mathrm{off}} = \int_{t6}^{t7} i_{\mathrm{DC-}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{4.16}$$

The E_{off} for both power modules A and B is within 1.6 mJ – 1.9 mJ for the DC-link voltage of 6 kV and load currents of up to 14 A, which is significantly lower compared to the E_{on}. During turn-off switching transient, measured current at the power module DC− terminal is predominantly the charging current of the combined LS MOSFET and JBS diode output capacitance, which

does not produce a Joule heating. Part of the drain current which conducts through the MOSFET channel produces the Joule heating. Thus the actual turn-off switching energy dissipation is derived from,

$$E^{*}_{\text{off}} = E_{\text{off}} - E_{\text{OSS(Static)}} \tag{4.17}$$

From comparing the measured E_{off} to $E_{\text{OSS(Static)}}$, it can be identified that the major part of turn-off switching energy dissipation is the combined stored energy on LS MOSFET and diode output capacitance.

4.3 Assessment on the impact of SiC JBS diode on SiC MOSFET switching transient

In the presented case study, two half-bridge power modules with and without anti-parallel SiC JBS diode are utilized. For the two half-bridge power modules, DBC layouts are identical, which allows to make a case study on the impact of SiC JBS diode on SiC MOSFET switching transient. Thereby the contribution of module parasitic capacitance in terms of difference in SiC MOSFET switching transient for two power modules can be discarded due to their identical DBC layouts. In case of power module with SiC JBS diode, the impact of JBS diode in terms of added switching energy dissipation due to the added junction capacitance in parallel to SiC MOSFET is analysed. In addition to this, the reverse recovery performance of the body diode is investigated for the power module without anti-parallel SiC JBS diode.

4.3.1 Device under test

Picture of the two variants of 10 kV half-bridge power modules, one with and another without JBS diode are shown in Fig. 4.13a. Their 3D-CAD top view showing the DBC layouts are presented in Fig. 4.13b. The 10 kV SiC devices are soldered on a 0.63 mm identical layout AlN DBC [57] attached to a 3 mm AlSiC baseplate [57]. The power module parasitic capacitances extracted from ANSYS Q3D are similar to the one presented in Table 4.1 for Module A. In the presented case study power modules with and without anti-parallel SiC JBS diode is referred here as module X and Y.

4.3.2 Analysis of turn-on and turn-off switching energy dissipation for power module with and without SiC JBS diode

The two power modules are tested in a double pulse test setup presented in Section 4.2.3 utilizing similar measurement techniques and probes. The

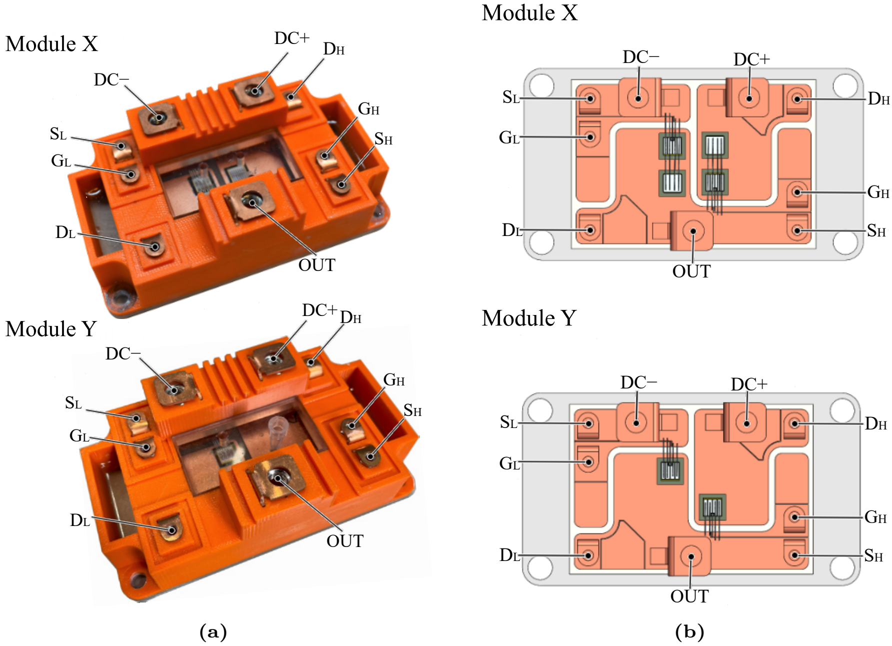


Fig. 4.13: (a) Picture and (b) Solidworks rendering for the 10 kV half-bridge SiC MOSFET power modules with (termed as X) and without (termed as Y) anti-parallel SiC JBS diode. [C]

experiments are performed at DC-link voltage of 6 kV, load current levels of up to 14 A with temperature range of 25°C – 100°C. The turn-on and turn-off switching waveforms for two power modules for 6 kV, 14 A test at 25°C are presented in Publication [C].

Turn-on switching energy dissipation

The comparison of two power modules X and Y, in terms of their turn-on switching energy dissipation and $\mathrm{d}v/\mathrm{d}t$ at DC-link voltage of 6 kV, load currents of up to 14 A for temperatures of 25°C and 100°C is presented in Fig. 4.14 and Fig. 4.15, respectively. As can be seen in Fig.4.14 and 4.15, for a similar load current level the turn-on $\mathrm{d}v/\mathrm{d}t$ for tests at 100°C is higher than 25°C, which is due to decrease in MOSFET gate-source threshold and Miller voltage with increase in temperature. However, lower turn-on $\mathrm{d}v/\mathrm{d}t$ for module X in comparison to module Y at similar load current levels and temperature is identified due to the positive shift in the gate-source plateau voltage for module X when compared to module Y. The positive shift in plateau voltage is identified as an effect of increased MOSFET channel current due to the added SiC JBS diode junction capacitance in parallel to SiC MOSFET and partly due to the

variance within the die parameters. The turn-on $\mathrm{d}v/\mathrm{d}t$ at 6 kV, 14 A for module Y is measured to be 26 kV/µs and 39.2 kV/µs at 25°C and 100°C respectively, which is approximately 120 % and 57 % higher in comparison to module X at 25°C and 100°C, respectively.

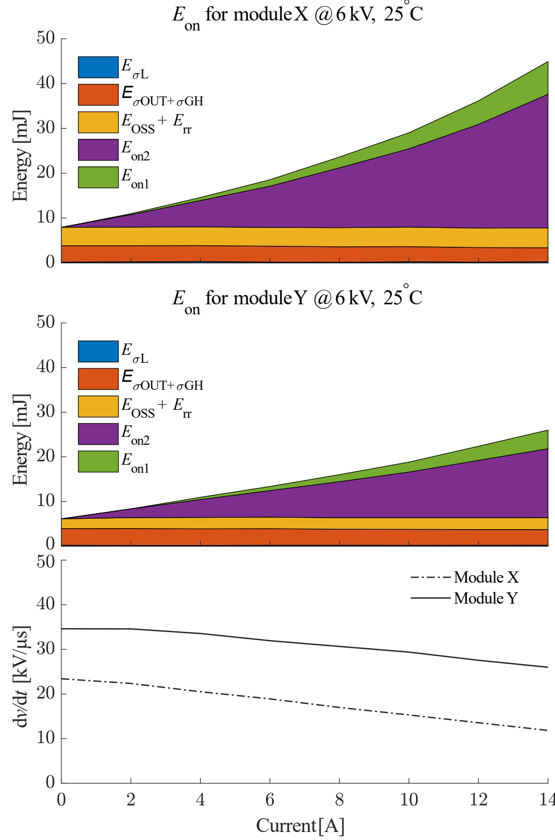


Fig. 4.14: Comparison of the turn-on switching energy dissipation E_{on} and $\mathrm{d}v/\mathrm{d}t$ for modules X and Y at the DC-link voltage of 6 kV, load currents of 0 A – 14 A and temperature of 25°C. [C]

Switching energy dissipation E_{on1} at 6 kV, 14 A, for module X is 7.3 mJ and 4.1 mJ, whereas for module Y it is 4.1 mJ and 2.8 mJ, at 25°C and 100°C respectively. The higher E_{on1} for module X in comparison to module Y under similar experimental condition, is due the reduced $\mathrm{d}i/\mathrm{d}t$ for module X. The decrease in $\mathrm{d}i/\mathrm{d}t$ for module X in comparison to module Y, is attributed to the die parameter variance (MOSFET gate-source threshold voltage and Miller voltage level) and difference in the reverse recovery characteristics for the module with SiC JBS diode. The decrease in E_{on1} for two modules with increase in temperature, is due to the reduced MOSFET gate-source threshold and Miller

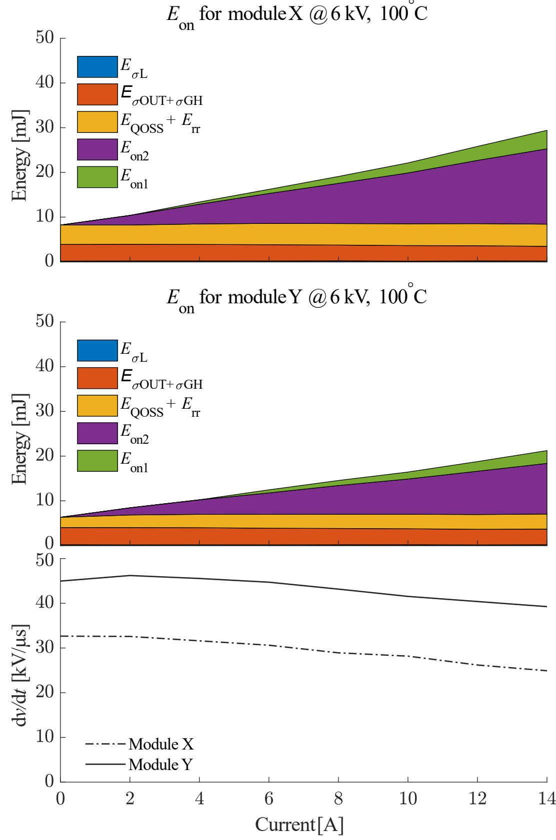


Fig. 4.15: Comparison of the turn-on switching energy dissipation E_{on} and $\mathrm{d}v/\mathrm{d}t$ for modules X and Y at DC-link voltage of 6 kV, load currents of 0 A – 14 A and temperature of 100°C. [C]

voltage level.

When comparing switching energy dissipation E_{on2} for modules X and Y, it can be seen that for similar experimental condition E_{on2} for module X is higher than module Y. The increase in E_{on2} for module X is primarily due to the reduced $\mathrm{d}v/\mathrm{d}t$ because of increased Miller voltage level, which is resulting from the increased MOSFET channel current due to added parallel junction capacitance of the body diode, and in part due to variance in die parameters. Decrease in E_{on2} with increase in temperature for both modules, is due to the decrease in Miller voltage level with increasing temperature. The E_{on2} at 6 kV, 14 A, for module X is 29.8 mJ and 16.8 mJ, whereas for module Y it is 15.4 mJ (48 % lower compared to module X) and 11.3 mJ (16 % lower compared to module X) at 25°C and 100°C, respectively.

Switching energy dissipation $E_{\text{QOSS}} + E_{\text{rr}}$ that is contributed due to discharg-

ing of HS power device output capacitance and diode reveres recovery charge through LS MOSFET channel increases slightly with increase in load current level and temperature for both power modules X and Y. The $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ at 6 kV and load current range of 2 A – 14 A is measured to be in the range of 4.1 mJ – 4.9 mJ and 4.3 mJ – 4.9 mJ for module X, whereas for module Y it is measured to be 2.1 mJ – 2.6 mJ and 2.2 mJ – 3.3 mJ at 25°C and 100°C, respectively. The increase in $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ for module X in comparison to module Y is due to the added junction capacitance of SiC JBS diode. Both modules X and Y show excellent performance in terms of reverse recovery with respect to increasing load current levels and temperatures. To extend the analysis further, $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ is compared with the derived energy $(Q_{(\mathrm{OSS(static)})} \cdot V_{\mathrm{DC}})$ - $E_{\mathrm{OSS(static)}}$ as shown in Fig. 4.16b. The charge $Q_{\mathrm{OSS(static)}}$ and energy $E_{\mathrm{OSS(static)}}$ are obtained from the output capacitance measurement of 10 kV SiC MOSFET and JBS diode dies utilizing Keysight B1506 curve tracer as shown in Fig. 4.16a. Due to the output voltage limitation of the curve tracer of 3 kV, the capacitance measurements above 3 kV are extrapolated by curve fitting. For the DC bias of 6 kV the output capacitance stored energy E_{OSS} and derived energy $(Q_{(\mathrm{OSS(static)})} \cdot V_{\mathrm{DC}})$ - $E_{\mathrm{OSS(static)}}$ for MOSFET is 0.8 mJ and 1.8 mJ, whereas for MOSFET and JBS diode combined it is identified to be 1.6 mJ and 3.7 mJ, respectively.

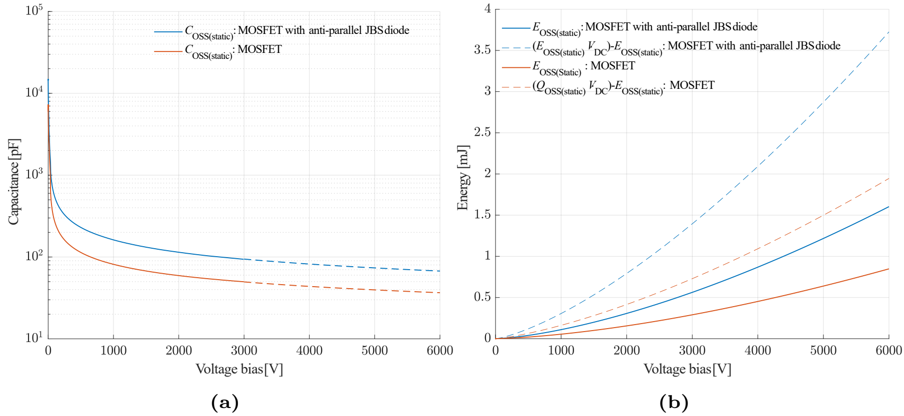


Fig. 4.16: (a) Output capacitance ($C_{\mathrm{OSS(static)}}$) measurements obtained utilizing the Keysignt B1506 curve tracer and (b) derived output capacitance stored energy $E_{\mathrm{OSS(static)}}$ and $(Q_{\mathrm{OSS(static)}} \cdot V_{\mathrm{DC}}) - E_{\mathrm{OSS(static)}}$ for the generation 3 10 kV SiC MOSFET and the 10 kV SiC MOSFET with anti-parallel 10 kV SiC JBS diode. [C]

The switching energy dissipation $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ for module X and Y at 6 kV with load current range of 0 A – 14 A is compared with the derived energy $(Q_{(\mathrm{OSS(static)})} \cdot V_{\mathrm{DC}})$ - $E_{\mathrm{OSS(static)}}$ as shown in Fig. 4.17. From the comparison presented in Fig. 4.17, it can be identified that the major portion of $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ account for energy dissipation due to discharging of output capacitance stored

energy, whereas small portion of $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ can be identified due to the reverse recovery.

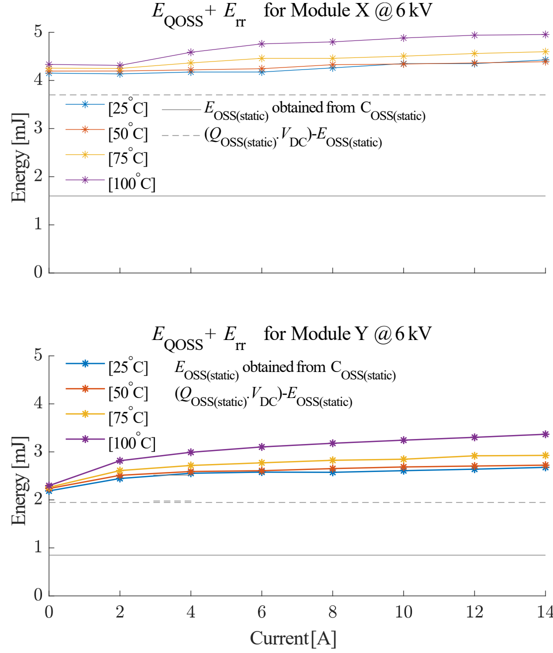


Fig. 4.17: comparison of the stored energy on the output capacitance ($E_{\mathrm{OSS(static)}}$) and with switching energy dissipation $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ for power modules X and Y at the DC-link voltage of 6 kV, load currents of 0 A – 14 A and temperature range of 25°C–100°C. [C]

The switching energy dissipation $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ due to discharging of power module parasitic capacitance through LS MOSFET channel, is measured to be in the range of 3.1 mJ – 3.7 mJ for module X and 3.4 mJ – 3.8 mJ for module Y at 6 kV, 0 A – 14 A tests at 25°C and 100 °C. For similar experimental conditions, switching energy dissipation $E_{\sigma\mathrm{L}}$ due to charging of load inductor parasitic capacitance through LS MOSFET channel, is measured to be in the range of 0.1 mJ – 0.2 mJ for module X and 0.1 mJ – 0.3 mJ for module Y. Since, switching energy dissipation $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ and $E_{\sigma\mathrm{L}}$ are related to capacitive charging or discharging they are almost independent of load current and temperature.

Turn-off switching energy dissipation

The comparison of two power modules X and Y, in terms of their turn-off switching energy dissipation and $\mathrm{d}v/\mathrm{d}t$ for DC-link voltage of 6 kV, load currents of up to 14 A for temperatures of 25°C and 100°C is presented in Fig. 4.18 and Fig, 4.19, respectively. For a similar load current level the turn-off $\mathrm{d}v/\mathrm{d}t$ for tests at 100 °C is only slightly higher compared to the tests performed at

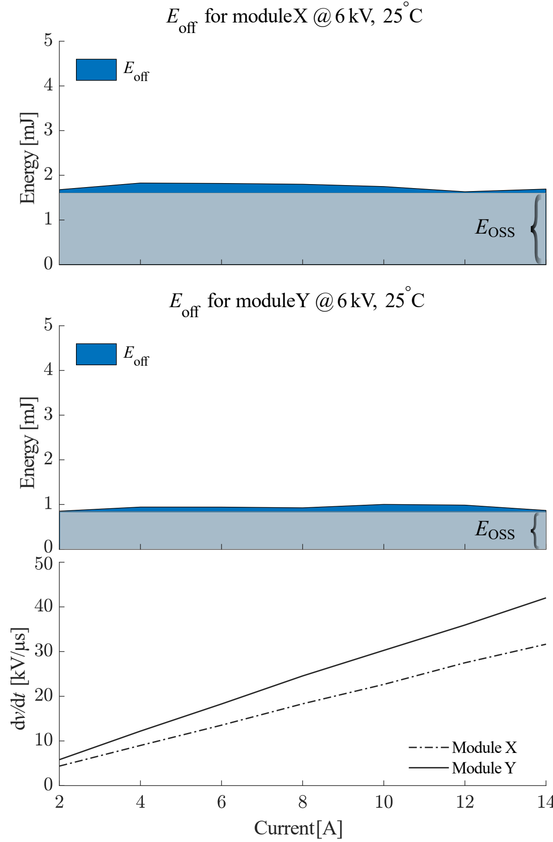


Fig. 4.18: Comparison of the turn-off switching energy dissipation E_{off} and $\mathrm{d}v/\mathrm{d}t$ for modules X and Y at the DC-link voltage of 6 kV, load currents of 0 A – 14 A and temperature of 25°C. [C]

25°C, indicating insignificant impact of decrease in threshold and Miller voltage level on the turn-off $\mathrm{d}v/\mathrm{d}t$ with increase in temperature. The turn-off $\mathrm{d}v/\mathrm{d}t$ at 6 kV, 14 A for modules Y is measured to be 42 kV/µs and 40.8 kV/µs at 25°C and 100°C respectively, which is 33 % higher in comparison to module X for similar test condition at 25°C and 100°C. The lower turn-off $\mathrm{d}v/\mathrm{d}t$ for module X in comparison to module Y is due to the added JBS diode junction capacitance in parallel to the SiC MOSFET that acts as a snubber. As can be seen in Fig. 4.14 and 4.15, the measured turn-off switching energy dissipation is in the range of 1.6 mJ – 1.9 mJ for module X, whereas for module Y it is in the range of 0.8 mJ – 1 mJ at 6 kV, 2 A – 14 A tests at 25°C and 100°C. The measured E_{off} for module X and Y is only slightly higher than the output capacitance stored energy E_{OSS}, which for a 10 kV SiC MOSFET is 0.8 mJ and for MOSFET and JBS diode combined it is 1.6 mJ at voltage bias of 6 kV.

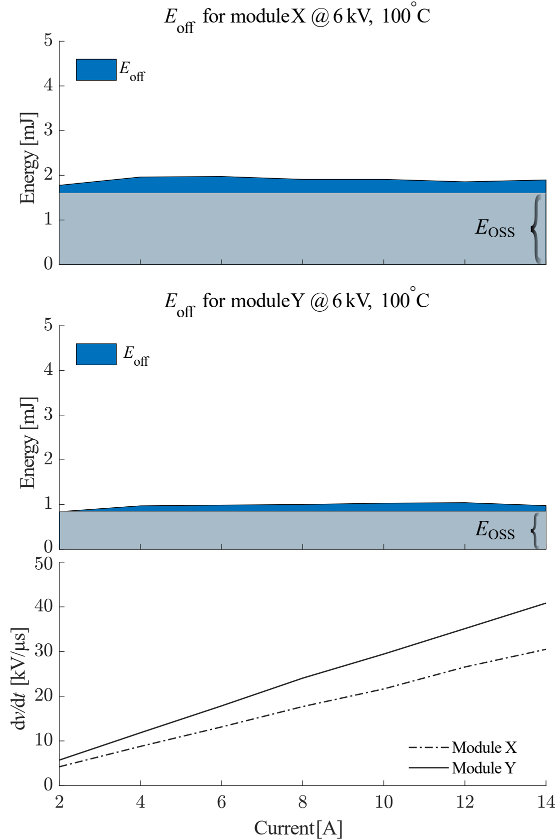


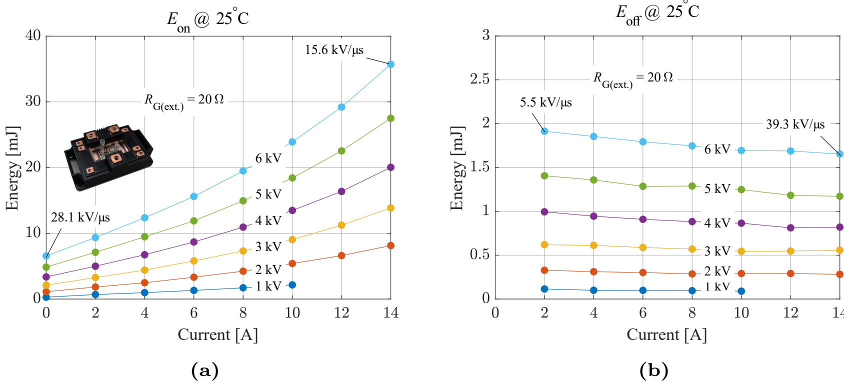
Fig. 4.19: Comparison of the turn-off switching energy dissipation E_{off} and $\mathrm{d}v/\mathrm{d}t$ for modules X and Y at DC-link voltage of 6 kV, load currents of 0 A – 14 A and temperature of 100°C. [C]

This indicates that major portion of the measured turn-off switching energy dissipation, is stored energy on the LS device output capacitance. The inclusion of SiC JBS diode reduces the turn-off $\mathrm{d}v/\mathrm{d}t$, however its impact on the actual turn-off switching energy dissipation is insignificant compared to its impact on the turn-on switching energy dissipation.

With excellent reverse recovery performance of the SiC MOSFET body diode the power module without SiC JBS diode exhibit superior performance in terms of over all switching energy dissipation in comparison to the power module with anti-parallel SiC JBS diode. Eliminating the SiC JBS diode from a power module is attractive consideration in the case, where benefits in terms of power module cost and power density outweigh the gains in terms of lower conduction losses.

4.4 Impact of power module design change in terms of reduced module capacitance and elimination of SiC JBS diode

The outcome of the power module parasitic capacitance and SiC JBS diode impact on SiC MOSFET switching transient and energy dissipation, are utilized in the design of multi-chip power module. In case of a single-chip power module the module parasitic capacitance $C_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$, is 98.3 pF in comparison to 64.5 pF for a multi-chip power module, which is approximately 45 % higher. Furthermore, in case of a multi-chip power module the displacement current due to module parasitic capacitance is distributed among four MOSFET dies in parallel, that aids in lessening the impact of module parasitic capacitance on the switching transient and switching energy dissipation.



(a) (b)

Fig. 4.20: (a) Turn-on and (b) turn-off switching energy dissipation of single-chip 10 kV half-bridge SiC MOSFET power module. [D]

The single-chip and multi-chip power modules are tested in a double pulse test setup similar to one described in section 4.2.3. One of the difference in the double pulse test for the multi-chip power module is that the LS MOSFET or module current $i_{\mathrm{DC}-}$, is measured using a 25 mΩ co-axial shunt resistor. The turn-on and turn-off switching energy dissipation for DC-link voltage of up to 6 kV and load currents of up to 14 A for 10 kV single-chip and 56 A for multi-chip power modules at 25°C is presented in Fig. 4.20 and Fig. 4.21, respectively. In case of single-chip module the external gate resistance is 20 Ω, whereas for multi-chip module with four dies in parallel the external gate resistance is 8.25 Ω. The multi-chip module also includes 1 Ω of auxiliary source resistance in series for each parallel connected MOSFETs. The time to charge gate-source capacitance to Miller voltage level for given load current is proportional to gate-source capacitance, turn-on and off gate drive voltage as

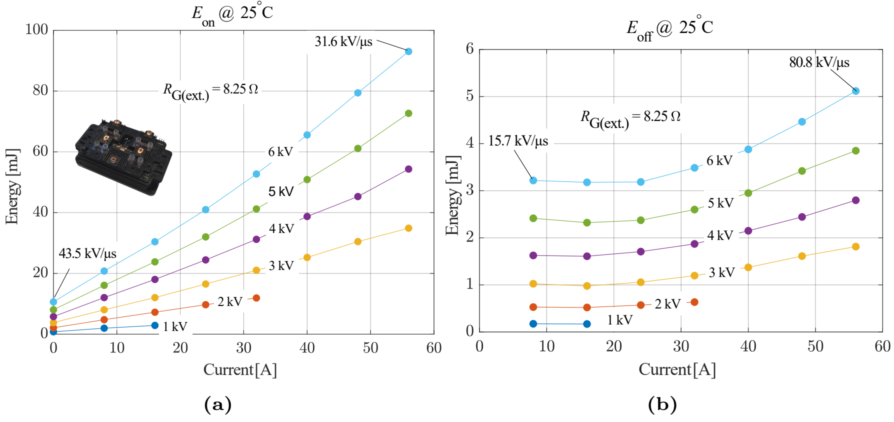


Fig. 4.21: (a) Turn-on and (b) turn-off switching energy dissipation of single-chip 10 kV half-bridge SiC MOSFET power module.

well as gate resistance.

This means in an ideal case with identical die characteristics, in order to obtain similar charging time to reach Miller voltage level for a given load current in case of multi-chip power module with four MOSFET dies in parallel the gate resistance needs to be four times lower because of increase in equivalent gate-source capacitance by factor of four. For the presented case, the gate-resistance for multi-chip power module is 8.5 Ω, which for a single die is " equivalent" to 34 Ω. Combine with reduced parasitic capacitance and elimination of SiC JBS diode, multi-chip power module exhibit faster switching transient and superior switching performance even with 70 % higher equivalent external gate resistance. The turn-on and turn-off switching energy dissipation and dv/dt for a single-chip module at DC-link voltage of 6 kV and load current of 14 A is compared with the multi-chip power module for load currents of 56 A, which is equivalent to 14 A per die. For a single-chip power module turn-on dv/dt and switching energy dissipation is measured to be 15.6 kV/µs and 35.7 mJ, respectively at 6 kV, 14 A test. Whereas in case of multi-chip power module turn-on dv/dt and switching energy dissipation is measured to be 31.6 kV/µs and 93 mJ respectively at 6 kV, 56 A test, which per die is approximately 33 % lower in comparison to single-chip power module. The turn-off dv/dt and switching energy dissipation for single-chip power module is measured to be 31.6 kV/µs and 1.6 mJ, respectively at 6 kV, 14 A test. Whereas, in case of multi-chip power module turn-off dv/dt and switching energy dissipation is measured to be 80.8 kV/µs and 5.1 mJ respectively at 6 kV, 56 A test. The turn-off switching energy dissipation for both modules is only slightly higher than their respective output capacitance stored energy.

4.5 Summary

The chapter presented an in-depth analysis of the module parasitic capacitance impact on the SiC MOSFET switching transient. An indirect measurement method proposed in this chapter allows to obtain the displacement current due to module parasitic capacitance during SiC MOSFET switching transient by utilizing accessible current measurements for the half-bridge power module. Furthermore, the heatsink impedance network is utilized in an LTspice simulation framework to predict the power module parasitic capacitance induced displacement currents. The good agreement between the measurement and simulation validate the accuracy of the modelled impedance network and extracted module parasitic capacitances in the presented analysis.

Based on a detailed investigation on the module parasitic capacitance induced displacement current paths in a half bridge power module during turn-on and turn-off switching transients, switching energy dissection methodology is proposed. Utilizing proposed switching energy dissection, detailed quantitative analysis and comparison of module parasitic capacitance impact on the switching transient and switching energy dissipation is presented based on the experimental study utilizing 10 kV half-bridge power modules that are custom packaged with a different DBC layouts. The findings from the experimental study reveal that the impact of module parasitic capacitance on the turn-on switching energy dissipation is two-fold and is preeminent in comparison to turn-off switching energy dissipation. In case of MV SiC MOSFET power modules with its fast switching characteristics, the impact of module parasitic capacitance on the SiC MOSFET is significant, which can not be neglected. Not taking into consideration, the module parasitic capacitance impact can result in errors in assigning switching energy dissipation and behavioural based modeling of the power modules that is often utilized to simulate power module switching dynamics and losses.

The proposed switching energy dissection method is extended to another study, in which the impact of the SiC JBS diode on SiC MOSFET switching transient is analysed with experimental study on two 10 kV half-bridge power modules with and without SiC JBS diode packaged with an identical DBC layouts. With an excellent reverse recovery of the SiC body diode, from a switching performance point of view eliminating anti-parallel SiC JBS diode in a half-bridge power module can lower over-all switching energy dissipation. Eliminating the SiC JBS diode from a power module is an attractive consideration in the case, where benefits in terms of power module cost and power density outweigh the gains in terms of lower conduction losses.

Chapter 5

10 kV SiC MOSFET enabled medium voltage power stack

5.1 Introduction

This chapter presents the design and demonstration of MV power stack rated for 50 kVA and 4.16 kV line-line voltage utilizing 10 kV half-bridge SIC MOSFET power modules in a two-level voltage source converter topology. The terminology medium voltage power stack refers to the basic power electronic building block for a high power MV converter, which can be paralleled to achieve increased power rating for the converter. Designed MV power stack is realized in a commercial 500 kVA, 690 V line-line voltage rated IGBT based power stack frame. The 50 kVA power stack presented in this research work is the first

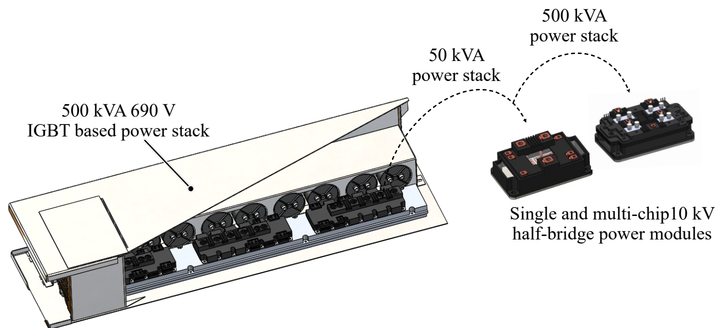


Fig. 5.1: 3D CAD model of a commercial low voltage IGBT based power stack. The power stack frame and cooling assemblies are utilized to retrofit SiC power modules.

demonstrator prototype with final target of realizing 500 kVA rated MV power stack in the similar footprint utilizing the multi-chip 10 kV half-bridge SiC MOSFET power modules. Experimental validation of a designed MV power stack is demonstrated in a DC-fed three phase back to back test setup at the DC-link voltage of 6 kV, load current of 7 A and switching frequency of 5 kHZ.

5.2 Topology and system specification

The proposed MV power stack utilizes a simple two-level VSC topology as shown in Fig.5.2, whose design specifications are summarized in Table 5.1.

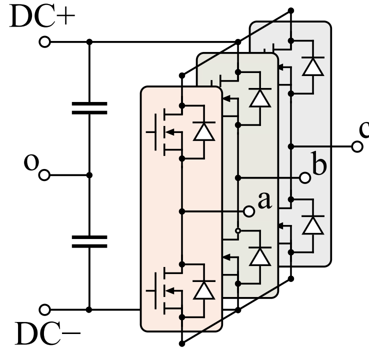


Fig. 5.2: Schematic of a two-level topology for three phase MV power stack.

Table 5.1: Specifications of the designed MV power stack. [D]

Parameter	Value
Rated Power (S)	50 kVA
DC-link voltage (V_{DC})	6 kV – 7.2 kV
Line-line AC rms voltage ($V_{\mathrm{LL(rms)}}$)	4.16 kV
Phase rms current ($i_{\mathrm{ph(rms)}}$)	7 A
Switching frequency (f_{sw})	5 kHz – 10 kHz

The minimum DC-link voltage rating of 5.9 kV – 6.8 kV for MV power stack is determined based on (5.1), considering the rated rms line-line voltage of 4.16 kV with sine wave pulse width modulation (SVPWM) or space vector modulation (SVM) [109]. In (5.1), m_{a} is the modulation index, where maximum value of m_{a} is 1 and 1.15 for SPWM and SVM, respectively. For a specified DC-link voltage ratings in Table 5.1, the voltage utilization factor for 10 kV power modules is 60% – 72%.

$$v_{\mathrm{LL(rms)}} = \sqrt{\frac{3}{8}} \cdot m_{\mathrm{a}} \cdot V_{\mathrm{DC}} \tag{5.1}$$

5.3 MV power stack assembly

Designed MV power stack assembly includes, 10 kV half-bridge SiC MOSFET power modules, low-isolation capacitance gate drivers, DC-link capacitors with busbar assembly and a direct liquid cooled thermal management system as shown in Fig. 5.3. Since, 10 kV half-bridge SiC MOSFET power modules and the low isolation capacitance gate driver have been discussed in previous Chapters 2 and 3 of the thesis, it is not discussed here and a brief discussion on the design and dimensioning of a DC-link and thermal management is presented.

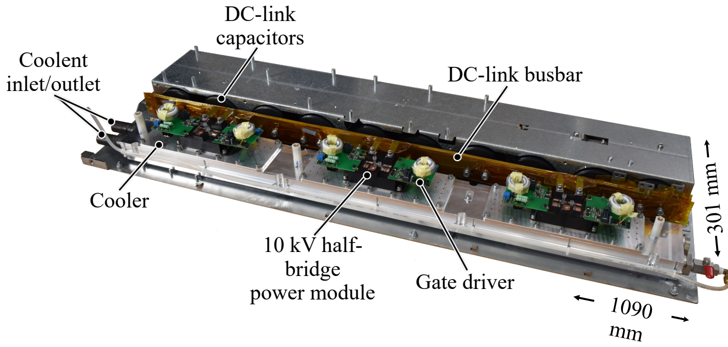


Fig. 5.3: Picture of a designed three phase 50 kVA, 4.16 kV rated MV power stack. [D]

5.3.1 DC-link and busbar design

The DC-link capacity of a designed MV power stack is determined for the rated power of 500 kVA instead of 50 kVA. The DC-link rms ripple current is obtained based on (5.2) [110], as shown in Fig. 5.4. For a pulse width modulated (PWM) converter, the worst case current stress on the DC-link capacitors occur under unity power factor (PF) with modulation index (m_{a}) of approximately 0.6. For 500 kVA, 4.16 kV rated MV power stack, the worst case current stress is calculated to be 49 A using (5.2).

$$\begin{aligned} i_{\mathrm{C_{DC(pu)}}} &= \frac{i_{\mathrm{C_{DC(rms)}}}}{i_{\mathrm{base}}} = \frac{i_{\mathrm{C_{DC(rms)}}}}{i_{\mathrm{ph(rms)}}} \\ &= \sqrt{\left[2 \cdot m_{\mathrm{a}} \cdot \left\{\frac{\sqrt{3}}{4 \cdot \pi} + \cos^2(\phi)\left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} \cdot m_{\mathrm{a}}\right)\right\}\right]} \end{aligned} \tag{5.2}$$

Minimum requirement for the DC-link capacitance in case of a MV power stack is obtained by calculating the maximum Ampere second of capacitor current during a switching period (Asec $= i_{\mathrm{c}} \cdot \mathrm{d}t$) for allowable capacitor voltage ripple

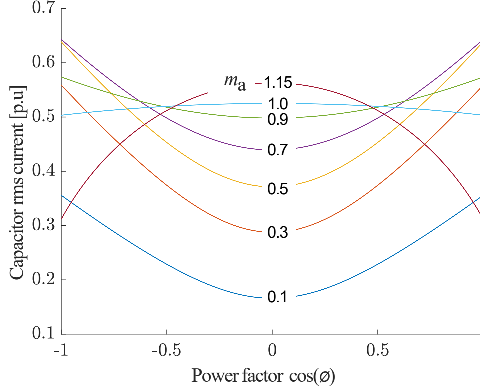


Fig. 5.4: Capacitor rms current in p.u as a function of modulation index and power factor for PWM converter.

[111]. Based on (5.3) and (5.4), it can be identified that maximum Asec for a PWM converter at zero and unity PF appears around modulation index of 1.15 and 0.66, respectively. [111].

$$Asec = \frac{1}{4} \cdot \sqrt{\frac{3}{2}} \cdot i_{\text{ph(rms)}} \cdot \frac{1}{f_{\text{sw}}} \cdot m_{\text{a}} \tag{5.3}$$

$$\text{Asec} = \frac{\sqrt{6}}{2} \cdot i_{\text{ph(rms)}} \cdot \frac{1}{f_{\text{sw}}} \cdot m_{\text{a}} \cdot \cos(\phi) \cdot \left[\frac{\sqrt{3}}{2} - \frac{3}{4} \cdot m_{\text{a}} \cdot \sin(\frac{\pi}{3}) \right] \tag{5.4}$$

With maximum Asec values corresponding to zero and unity PF obtained from (5.3) and (5.4), minimum requirement for the DC-link capacitance considering maximum voltage ripple of 10 % is calculated base on (5.5) and is presented in Fig. 5.5, for its intended operating switching frequency range of 5 kHZ – 10 kHz.

$$C_{\text{DC(min)}} = \frac{\text{Asec}_{\text{max}}}{\%\text{ripple} \cdot V_{\text{DC}}} \tag{5.5}$$

Based on the calculated minimum requirement of DC-link capacitance with voltage ripple criteria of 10 % and maximum capacitor current stress, a DC-link film capacitor rated for 3.6 kV, 40 µF (Electronicon E50.N14-403NTO) [112] is found suitable for a DC-link capacitaor bank of MV power stack. As shown in Fig.5.6, DC-link rated for 100 µF, 7.2 kV is designed with the series parallel combination of ten 3.6 kV, 40 µF DC-link capacitors.

Three layers of stacked busbar, each cutout from a 1.2 mm steel sheet is used to provide electrical connection between the DC-link capacitors and power modules. A simple approach is adopted to provide insulation between the two adjacent busbar layers, where each of this busbar is covered with four layers of 50 µm Kapton tape, which can provide voltage withstand capability of

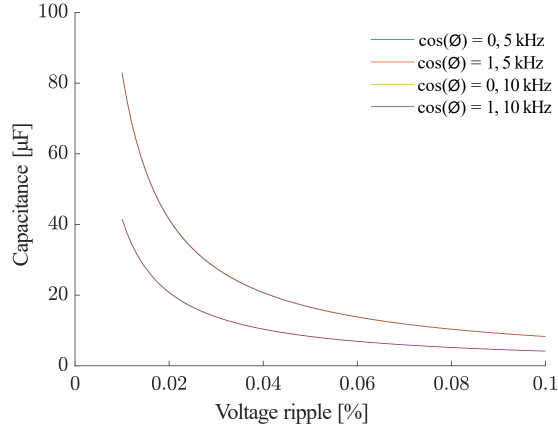


Fig. 5.5: Minimum DC-link capacitance requirement as a function of capacitor voltage ripple at unity and zero power factor for a switching frequencies of 5 kHz and 10 kHz.

approximately 48 kV [113]. This approach is deemed to be suitable considering low scale of economy for manufacturing laminated busbar for the designed MV power stack prototype together with its planned experimental validation in the laboratory environment. The 3D-CAD model and image of the DC-link assembly is shown in Fig. 5.6.

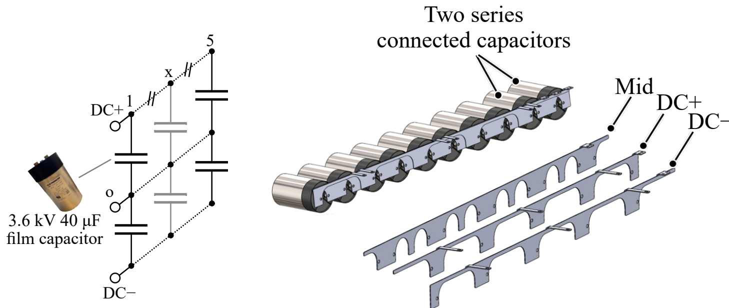


Fig. 5.6: Schematic of a DC-link capacitor bank and 3D-CAD model of DC-link capacitor-busbar assembly. [D]

To investigate voltage overshoot due to busbar stray inductance, the parasitic parameters for busbar assembly are extracted from ANSYS Q3D. An equivalent circuit corresponding to the solved AC inductance-resistance matrix (at solution frequency of 10 MHz) from ANSYS Q3D is exported in an LTspice simulation setup as shown in Fig. 5.7. In the simulation study, current source with constant $\mathrm{d}i/\mathrm{d}t$ of 1 kA/μs is applied across the power module connection terminals to simulate the voltage overshoot due to busbar stray inductance. From presented simulation study, it is identified that the maximum voltage overshoot is within

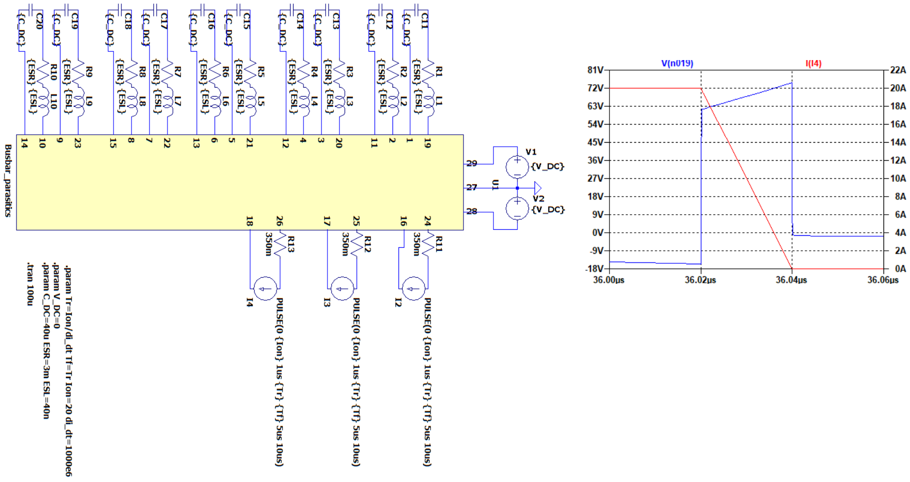


Fig. 5.7: LTspice simulation setup utilizing extracted equivalent circuit of busbar parasitics.

120 V for di/dt of 1 kA/µs, which is higher than the maximum di/dt identified from the experimental measurements of switching waveforms for a single-chip 10 kV SiC power module. The extremely low inductance design for the busbar is not a requirement, considering large margin between the operating DC-link voltage of 6 kV – 7.2 kV and maximum drain source voltage rating of 10 kV for the power module, combined with relatively lower di/dt.

5.3.2 Thermal management

The thermal management system for a MV power stack is designed utilizing the direct liquid cooling solution from Danfoss [114]. The direct liquid cooling system eliminates the conventionally used thin layer of the thermal interface material (TIM) between the power module baseplate and the cooler, which accounts for the 30 % – 50 % of the total thermal resistance.. This improves the thermal performance significantly [114]. The heat transfer coefficient (htc) for a water cooling system can range from 50 – 10000 W/m^{2}K [115]. However, direct liquid cooling system can attain relatively high values of htc compared to indirect liquid cooling system. The htc attainable with the direct liquid cooling is reported to be in the range of 12,500 W/m^{2}K with the liquid coolant flow rate of 10 l/min [116].

The 3D-CAD exploded view of a direct liquid cooling assembly utilized in the MV power stack is shown in Fig. 5.8. The liquid cooling assembly consist of a cooler, plastic turbulator and O-ring. The plastic turbulator has multiple cells in the X-Y directions which guides the liquid coolant and creates turbulant flow along the surface of the power module baseplate. The thermal management

system is designed for a liquid flow rate of up to 20 l/min and pressure of 3 bars, respectively.

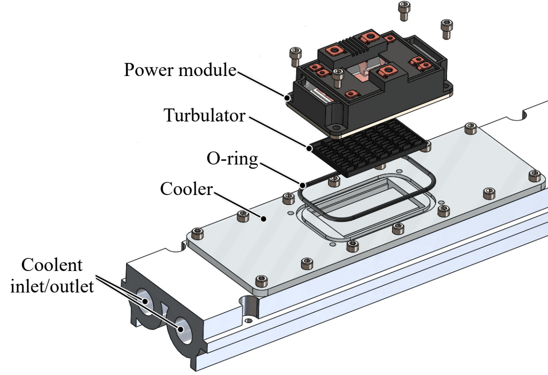


Fig. 5.8: 3D-CAD exploded view of thermal management system for a designed MV power stack. [D]

Extraction of heat transfer coefficient and thermal impedance

This section presents a method utilized to extract heat transfer coefficient (htc) for the utilized direct liquid cooling system in MV power stack. The htc for the power module is extracted by validating experimentally measured thermal response to the simulated thermal response in COMSOL Multiphysics finite element method based (FEM) simulation software. Based on the extracted htc, thermal characteristics for the 10 kV SiC MOSFET power module is simulated in COMSOL.

In an experimental test, the half-bridge power module is mounted on a cooler utilizing cooling assembly shown in Fig. 5.8. Power loss is injected into the MOSFET dies with positive bias of +20 V applied to the HS as well as LS SiC MOSFETs and connecting a DC source with a current control mode to the DC+ and DC- terminals of a half-bridge power module. Power dissipation within the HS and LS MOSFET is obtained by measured output current of a DC power supply and voltages at the half-bridge DC+ and output terminals. The die surface temperature is measured by using a fiber optic temperature sensor OTG F-10 [117], which is inserted through a pipette that provides access to the top surface of a die. Together with die temperatures, coolant flow rate and inlet/outlet temperatures are monitored during the experimental test.

The simulation in COMSOL is setup by importing a 3D-CAD model of the power module as shown in Fig. 5.9 with a zoomed view showing meshing for the geometry. The mesh refinements for a geometry is performed until no change in thermal response is observed for increasing meshing size. The SiC MOSFETs

and JBS diodes dies within a half-bridge module are labeled with numbers 1 – 4 as can be seen in Fig. 5.9. The cross sectional view of a power module showing different interface layers is presented in Fig. 5.10. The key material type, its physical properties utilized in COMSOL simulation and thickness of different interface layers for 10 kV power modules are listed in Fig. 5.2.

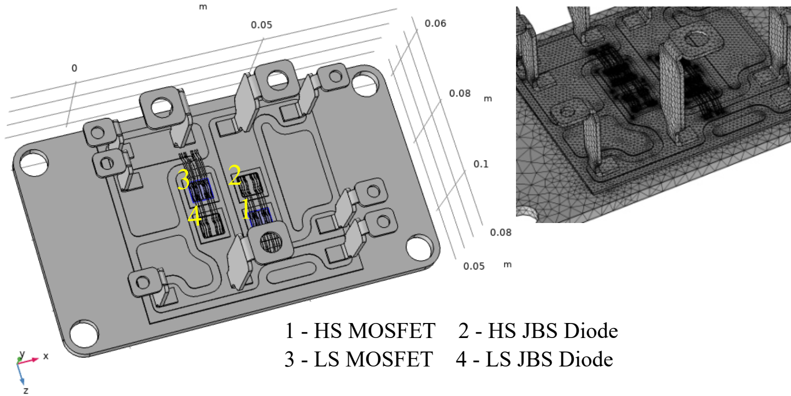


Fig. 5.9: Image of a thermal simulation setup in COMSOL for a 10 kV half-bridge module with a zoomed view of meshing.

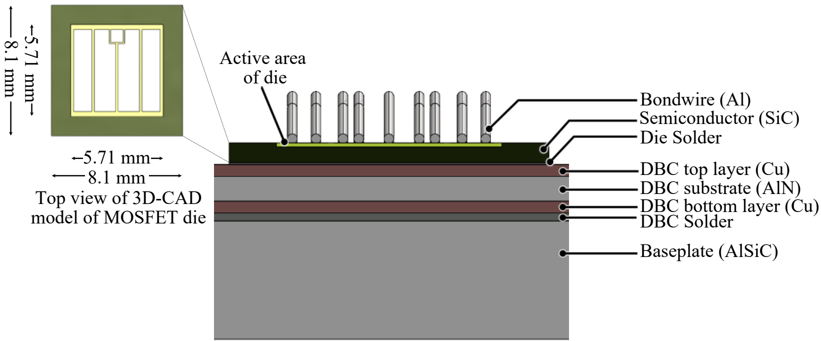


Fig. 5.10: Cross-sectional view from a 3D-CAD model of a 10 kV half-bridge power module.

In the thermal simulation, a heat source with power loss equivalent to the one measured in experimental test is assigned within the volumetric active area (highlighted in yellow in Fig.5.10) of SiC MOSFET dies, whose thickness is assigned to be 100 µm thick [119]. The surface area of the baseplate that is in direct contact with the liquid turbulator is assigned with a boundary condition defined by (5.6). In (5.6), q is heat flux, h is heat transfer coefficient and ΔT (T - T_{amb}) is the temperature difference between the surface and ambient, where

Table 5.2: Thickness and properties of material for different interface layers within power module. [30], [118]
Aluminium (Al), Aluminium Nitride (AlN), AlSiC (Aluminum Silicon Carbide), Copper (CU), Silicon Carbide (SiC)

Power module layer/interface	Material	Layer thickness [mm]	Thermal conductivity $\left[\frac{W}{m \cdot K}\right]$	Heat capacity $\left[\frac{J}{kg \cdot K}\right]$	Density $\left[\frac{kg}{m^3}\right]$
Bondwire	Al	-	238	900	2700
Die	4H-SiC	0.5	370	677	3200
Die solder	96.5Sn-3Ag-0.5Cu	0.05	50	150	9000
DBC top - layer	Cu	0.3	400	385	8960
DBC ceramic	AlN	0.63	170	745	3260
DBC bottom - layer	Cu	0.3	400	385	8960
DBC solder	96.5Sn–3Ag-0.5Cu	0.2	50	150	9000
Baseplate	AlSiC	3	190	741	3010

htc determines heat transfer rate between the solid surface and liquid area.

$$
\begin{aligned}
q &= h \cdot (T - T_{\text{amb}}) \\
h &= \frac{q}{T - T_{\text{amb}}}
\end{aligned}
\tag{5.6}
$$

The value of htc for a given liquid flow rate is identified from a steady-state heat transfer simulation study, by adopting a value of htc for which experimental and simulated device temperature match in steady state. For experimental measurements, at liquid flow rate of 15 l/min, coolant temperature of 13.1°C and power dissipation of 58.1 W and 63.3 W for the HS and LS MOSFET respectively, htc is extracted to be 8700 from simulation. With htc of 8700, the simulated transient thermal response for die temperature is compared with the experimental measurements in Fig. 5.11. As can be seen in Fig.5.11, measured and simulated average surface temperatures for the HS and LS MOSFET dies are in good agreement. The difference in the the HS and LS MOSFET temperatures in Fig. 5.11, is due to the difference in power dissipation within HS and LS MOSFETs. For experimental test, in steady state die temperature increases slightly due to increase in coolant temperature which can not be controlled precisely to a steady value. By utilizing similar approach, htc for different coolant flow rates ranging from 5 l/min – 20 l/min for the liquid cooling system are extracted and listed in Table 5.3.

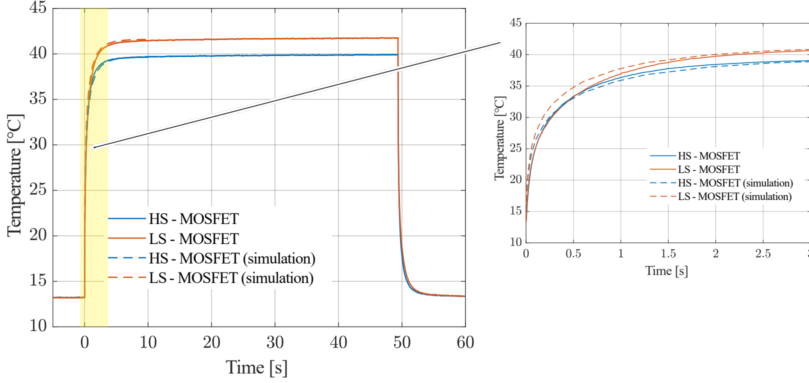


Fig. 5.11: Measured and simulated temperatures for MOSFET dies in a 10 kV-half bridge module with coolant flow rate of 15 l/min in a direct liquid cooled thermal management system.

Table 5.3: Extracted heat transfer coefficient at different flow rates for a 10 kV-half bridge module with a direct liquid cooled thermal management system.

Flow rate $\left[\frac{1}{m}\right]$	htc $\left[\frac{W}{m^2 \cdot K}\right]$
5	4000
10	6800
15	8700
20	14300

Thermal impedance Z_i and coupling terms $\Psi_{i,j}$ for the dies within a half-bridge power module can be simulated for a given flow rate with known value of htc based on (5.7) and (5.8) [120].

$$Z_{i(t)} = \frac{T_{i(t)} - T_{\text{amb}}}{P_{i(t)}} \tag{5.7}$$

In (5.7), $Z_{i(t)}$, $T_{i(t)}$, $P_{i(t)}$ are thermal impedance, temperature and power dissipation of power semiconductor device i, respectively.

$$\Psi_{i,j(t)} = \frac{T_{i(t)} - T_{\text{amb}}}{P_{j(t)}} \tag{5.8}$$

In (5.8), $\Psi_{i,j}$ is cross coupling thermal characteristic parameter and T_i is temperature of power semiconductor device i, P_j is power dissipation in power semiconductor device j, and T_{amb} is the ambient temperature.

Fig. 5.12 presents, the simulated thermal response with thermal impedance and thermal coupling characteristics for dies 1 (HS MOSFET) and 2 (HS diode)

corresponding to Fig. 5.9 for htc of 8700. For, dies 3 (LS MOSFET) and 4 (LS diode) thermal response is expected to be similar as for dies 1 and 2, respectively. Simulated thermal impedance for MOSFET and diode die in half-bridge module

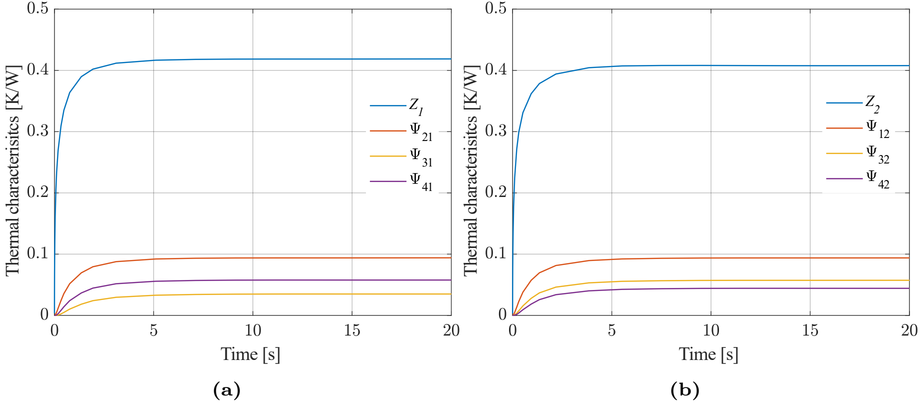


Fig. 5.12: Simulated thermal response for (a) SiC MOSFET and (b) JBS diode dies in 10 kV half-bridge module with a direct liquid cooled thermal management system at coolant flow rate of 15 l/min.

with htc of 8700 is identified to be 0.42 K/W and 0.41 K/W. The thermal response for both dies is almost identical with slightly lower impedance for diode die due to slightly larger active area.

5.4 Experimental setup and results

The experimental validation of designed power stack is performed in a DC-fed three phase back to back test setup as shown in Fig. 5.13. In this test setup, power is cycled between the two power stacks with one of the power stack acting as a source and another as a load. The output voltage and PF angle of an individual power stack can be controlled, with this approach power stack operation can be validated at operating points similar to its intended field application. In a DC-fed three phase back to back test setup, power drawn from a DC source is equivalent to the total losses in a back to back test setup, which primarily accounts for the semiconductor switching and conduction losses as well as losses within magnetic components. In the experimental test setup, half-bridge phase leg outputs of the two power stacks are connected with a 60 mH of load inductor. The DC-link for two power stacks is supplied by two 6 kV, 6 kW (Magna-Power XR-6000-1.0-/380+HS+LXI) positive and negative output polarity power supplies connected in series configuration. The two power stacks are operated in an open-loop configuration, where the fundamental frequency, voltage magnitude and phase angle difference between the phase leg

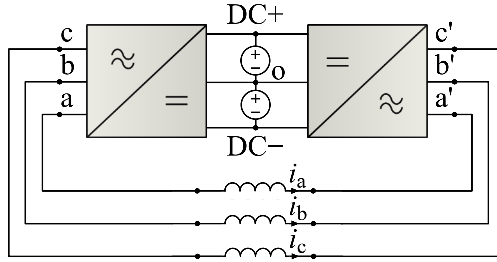


Fig. 5.13: Schematic of a DC-fed three phase back-to-back regenerative test setup.

output voltages of each power stack can obtained analytically to attain desired load current level during the test.

The test is performed at DC-link voltage of 6 kV (± 3 kV) with switching

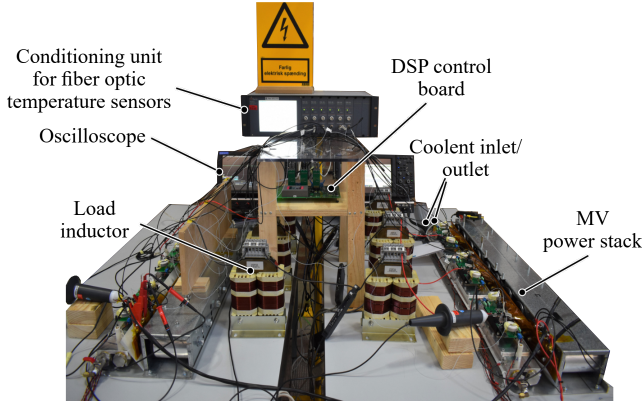
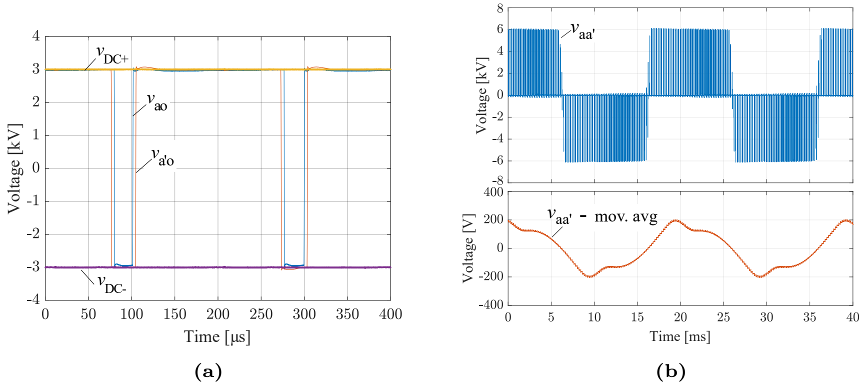


Fig. 5.14: Picture of a DC-fed three phase back-to-back regenerative test setup. [D]

frequency of 5 kHz. The fundamental frequency of the output AC voltage, modulation index and phase angle difference is selected to be 50 Hz, 0.8 and 5 deg respectively to obtain the output rms phase current magnitude of approximately 7 A. The measured DC-link voltage and half bridge output voltages for the phase–a of two power stacks with respect to mid-point of the DC-link is shown in Fig. 5.15a (Measurements performed utilizing PPE 20 kV 100 MHz passive probes). The half-bridge output voltage switches between positive (+3 kV) and negative (-3 kV) DC-link voltage, exhibiting clean switching without significant ringing and voltage overshoot. Voltage across the two series connected load inductors ($v_{aa'} = v_{ao}$-$v_{a'o}$) is obtained from a half-bridge output voltage measurements and is shown in Fig. 5.15b, together with the moving average.

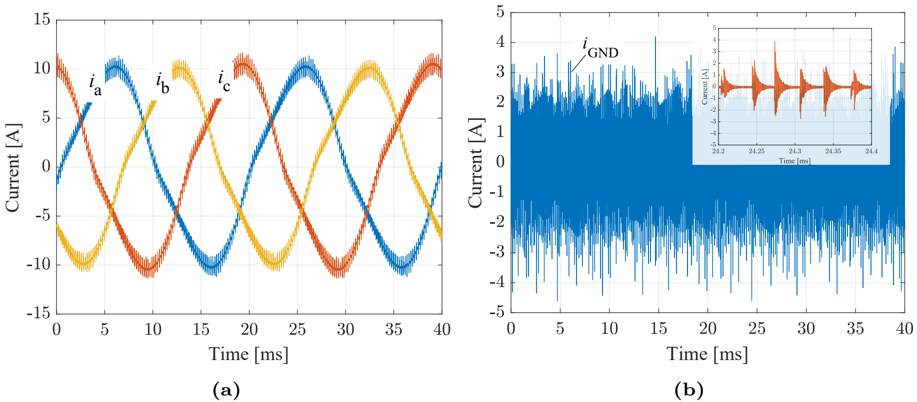
The measured phase current for the individual phases is shown in Fig.5.16a (Measurements performed utilizing Lecroy CP030 50 Mhz current probes). As can be seen the phase current attains the peak amplitude and rms value of



(a) **(b)**

Fig. 5.15: (a) Measured half bridge output voltages (b) load inductor voltage and its moving average for phase–a in a three phase bac-to-back test at DC-link voltage of 6 kV, load current of 7 A and switching frequency of 5 kHz. [D]

approximately 10 A and 7 A, respectively. Since, the test is performed in the open loop configuration the voltage error resulting due to the dead time effect which is current polarity dependent is not compensated. This causes the distortion in voltage waveform which results in the slight distortion in the phase currents. Due to the medium voltage DC-link and lower magnitude of the phase currents the required average voltage across the load inductor at the fundamental frequency of 50 Hz is significantly lower such that the voltage error due to the deadtime reaches magnitudes of the significant fraction of the average voltage across the inductor.



(a) **(b)**

Fig. 5.16: Measured (a) three phase load currents and (b) heatsink ground current in a three phase back-to-back test at DC-link voltage of 6 kV, load current of 7 A and switching frequency of 5 kHz. [D]

The cooler on which the half-bridge power modules are mounted is grounded due to safety reasons. The current measured at the cooler grounding connections, resulting from the charging and discharging of power module parasitic capacitances are shown in Fig.5.16b. The peak amplitude of measured ground current is 4 A, with current oscillations frequency in the range of 1.1 Mhz. To limit the peak amplitude of the ground current an impedance can be inserted between the cooler and the ground connection, however this is avoided as this would result in the voltage potential at the cooler during the switching transient due to the voltage drop across grounding impedance.

During the test, under steady state operation, MOSFET die temperatures within half-bridge power modules for one of the power stacks are measured using OTG F-10 fiber optic temperature sensors [117]. The MOSFET die temperatures are identified to be 45°C with liquid coolant temperature of approximately 20.5°C. Under steady state operating condition, the power output of DC supplies which is equivalent to the total power losses in a three phase back-to-back test setup is read out to be 384 W. The core and copper losses for the load inductor are considerably small, due to significantly low ripple current and resistance of a load inductor. In that case, major portion of the power losses are due to the semiconductor switching and conduction losses within the power stack. With total power losses of 384 W (including semiconductor and switching losses for two power stacks, core and copper losses for inductor) obtained from the DC power supply read out, the losses are identified to be less than 1 % of 35.6 kVA of circulated power. This suggest efficiency > 99 % under presented experimental loading conditions for the designed power stack, which is close to its intended operating point in terms of current and voltage levels.

5.5 Summary

In this chapter, a design and demonstration of a 50 kVA, 4.16 kV rated two-level MV power is presented. The power stack sub-assemblies include custom-packaged 10 kV half-bridge SiC MOSFET power modules, gate drivers, DC-link capacitors with busbar and liquid cooled thermal management system. Design of a MV DC-link capacitor and busbar is presented in detail. Furthermore, busbar parasitic extraction is performed to investigate the impact of stray inductance in terms of voltage overshoot. For, a liquid cooled thermal management system heat transfer coefficient is extracted based on the experimental thermal characterisation and FEM based thermal simulation study. With extracted htc, thermal impedance for a 10 kV power module with utilized direct liquid cooling system is simulated. The thermal impedance can be further utilized in electro-thermal simulation study to investigate power loss and temperature estimation for designed power stack under different loading conditions. The designed power stack is tested in a three phase back-to-back DC-fed regenerative

test setup, with power stack operating at DC-link voltage of 6 kV, load current of 7 A and switching frequency of 5 kHz. The key experimental electrical measurements from power stack testing in a back-to-back test setup are presented, validating operation of a designed power stack close to its intended operating condition. The total power losses for a back-to-back test setup for the presented experimental test condition is identified to be 384 W at a circulated power of 35.6 kVA.

Chapter 6

Conclusion: Summary and future work

6.1 Summary and main contributions

The PhD thesis objectives formulated based on the hypotheses presented in Section 1.3.1 of Chapter 1 are,

- To design and experimentally validate low coupling capacitance and MV isolated gate driver with a high common mode noise immunity for 10 kV SiC MOSFET half bridge power module.
- To analyse the impact of power module parasitic capacitances on SiC MOSFET switching transients and switching energy dissipation.
- To design a kVA rated MV power stack utilizing 10 kV half-bridge SiC MOSFET power modules and demonstrate experimental validation of power stack close to its rated operating condition, with feasible efficiency estimation based on measured power loss data.

In relation to the PhD thesis objectives listed above, the main research contributions of this work in the field of high power medium voltage power conversion applications utilizing MV SiC MOSFETs are summarized as follows.

- **Design and experimental validation of a gate driver with low coupling capacitance and high CM noise immunity**
  A gate driver for a 10 kV SiC MOSFET is presented exhibiting coupling capacitance of less than 3 pF. The gate driver PCB incorporates a low isolation capacitance DC-DC Flyback based power supply and gate driving stage with AMC functionality. The experimental validation of gate driver is performed at a DC-link voltage of 6 kV utilizing a 10 kV half-bridge power

module. The experimentally measured CM current under the application of high dv/dt for the designed gate driver exhibit good agreement with isolation capacitance measurements obtained using impedance analyser. Furthermore DC voltage withstand capability and AMC functionality of the gate driver is validated under high dv/dt (up to 80 kV/µs) switching transient. Experimental tests on the gate driver validate its design in terms of high CM noise immunity and false turn-on mitigation, necessary to ensure reliable operation of 10 kV SiC MOSFET with high dv/dt switching transient.

- **Comprehensive analysis of power module parasitic capacitance on SiC MOSFET switching transient in MV fast switching applications**
  An in-depth analysis of the power module parasitic capacitance induced displacement current paths during SiC MOSFET turn-on and turn-off switching transient is presented using 10 kV half-bridge SiC MOSFET power modules. An indirect measurement method to obtain power module parasitic capacitance induced displacement current is presented with experimental validation. A good agreement between the measured and simulated power module induced displacement current validate the accuracy of the extracted parasitic capacitance from FEM based simulation tools.
  Based on the experimental , it is found that in case of MV SiC MOSFET the peak amplitude of the power module parasitic capacitance induced displacement current during the switching transient can reach magnitudes that is significant fraction of SiC MOSFETs rated current, resulting in an increased conducted EMI. Furthermore, the displacement current conducts through SiC MOSFET during switching transient, resulting in an increase in over-all switching energy dissipation. Thus, a special design consideration in terms of parasitic capacitance for MV SiC MOSFET power module is emphasized and is applied to a custom packaged multi-chip 10 kV power module design, which exhibit faster switching speed and lower switching energy dissipation in comparison to the previous design of 10 kV single-chip custom packaged power modules.

- **Proposed switching energy dissection to analyse the impact of power module parasitic capacitance on SiC MOSFET in terms of added switching energy dissipation**
  By dissecting the switching energy dissipation using proposed method, a quantitative analysis and comparison in terms of the module parasitic capacitance on over-all switching energy dissipation is presented in an experimental case study utilizing custom-packaged 10 kV half-bridge power modules with different DBC layouts. From the experimental study, It is identified that the impact of power module parasitic capacitance

in terms of added switching energy dissipation is more pronounced for turn-on in comparison to turn-off switching energy dissipation. Impact of module parasitic capacitance on over-all switching energy dissipation can be significant in case of MV SiC MOSFET power modules and failing to account for this can lead to inaccuracy in estimation and assignments of switching energy dissipation in practical applications.
Proposed switching energy dissipation applied to another case study,

 – The switching energy dissection method is applied to another case study, where switching performance of single-chip 10 kV SiC MOSFET power modules with and wihout JBS diode is assessed at DC-link voltage of 6 kV, load current of up to 14 A and temperature range of 25°C and 100°C. With excellent reverse recovery performance of body diode for tested experimental condition, the power module without anti-parallel SiC JBS diode exhibit lower switching energy dissipation compared to power module with diode.

- **Design, development and demonstration of kVA rated two-level VSC topology based MV power stack**
  A 50 kVA, 4.16 kVA rated MV power stack based on simple two-level VSC topology is designed using custom-packaged 10 kV single-chip half-bridge power modules. The power stack sub-assembly comprises of a low-isolation capacitance gate driver, DC-link capacitors, busbar and liquid cooled thermal management system. The heat transfer co-efficient and thermal impedance for a 10 kV power module with a direct liquid cooling system is extracted using FEM based simulation and experimental thermal characterisation. Which can further be utilized in an electro-thermal simulation study. The designed power stack is tested at DC-link voltage of 6 kV, load current of 7 A with switching frequency of 5 kHz in a three phase back-to-back test setup. With total circulated power of 37.5 kVA, total losses for the back-to-back system are identified to be 384 W, which indicate efficiency higher than 99% for designed MV power stack under tested operating conditions.

6.2 Future work

This section presents brief overview on the planned future work and several other aspects of research pertaining to medium voltage SiC devices and its application that has not been covered in this thesis due to the project limitations.

- In this research work, experimental validation of 50 kVA power stack close to its intended operating condition is demonstrated with a power loss data based on the DC power supply read out in a three phase back-to-back

test setup. This work needs to be extended to obtain power vs efficiency curves for designed MV power stack under different loading and operating conditions. The calorimetric power loss measurements can be performed by utilizing power stack inlet/outlet liquid coolant temperatures and flow rate. Furthermore, electro-thermal simulation for the power stack can be developed and validated by experimental measurements.

- Scaling up of a power level for MV power stack, with planned 500 kVA demonstrator based on 10 kV multi-chip SiC MOSFET power modules. As shown in the 3D-CAD model of 500 kVA power stack assembly (Fig. 6.1), two multi-chip power modules are to be utilized in hard-parallel configuration per each phase. The impact of gate driver PCB and busbar layout design challenges with hard-paralleling of SiC MOSFET power modules in terms of their dynamic and static current sharing performance needs to be analysed.

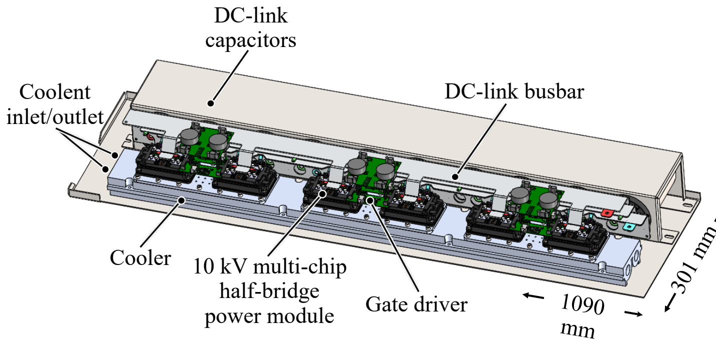


Fig. 6.1: 3D-CAD model of proposed 500 kVA MV power stack assembly.

- The impact of capacitive couplings on current/voltage sensing and feedback circuitry under high dv/dt switching transient needs to investigated, to implement necessary mitigation strategies in order to obtain reliable protection circuit and closed loop control for a power electronic converter. With successful implementation of a 500 kVA power stack, bench marking of MV SiC based solution against conventional LV Si and MV Si based solution can provide interesting insight in terms of attainable power density and system level efficiency benefits by applying MV SiC devices with a simple two-level topology in high power conversion applications.

- Investigation on developing a CM model at converter level and performing EMI/EMC tests for SiC based MV power stacks can provide insight into noise emission levels.

- The high dv/dt, switching transient in case of SiC MOSFETs can change the partial discharge behaviours within power modules, gate drivers and

passive components such as filter inductors. The PD behaviours and detection strategies under PWM voltage excitation with high $\mathrm{d}v/\mathrm{d}t$ switching transients needs to be investigated, considering its qualification for field applications.

- Detail study on the insulation coordination for power modules, gate drivers, passive components and power stacks. FEM based electric field simulation study can be performed to investigate electric field stress and weak links in the design for power stack, its sub-assemblies and passive components.

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Part II

Appended papers

Paper A

Gate driver with high common mode rejection and self turn-on mitigation for a 10 kV SiC MOSFET enabled MV converter

Dipen Narendra Dalal, Nicklas Christensen, Asger Bjørn Jørgensen, Simon Dyhr Sønderskov, Szymon Beczkowski, Christian Uhrenfeldt, Stig Munk-Nielsen

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The layout has been revised.

Gate driver with high common mode rejection and self turn-on mitigation for a 10 kV SiC MOSFET enabled MV converter

Dipen Narendra Dalal, Nicklas Christensen, Asger Bjørn Jørgensen, Simon Dyhr Sønderskov, Szymon Beczkowski, Christian Uhrenfeldt, Stig Munk-Nielsen

Abstract

This paper investigates gate driver design challenges encountered due to the fast switching transients in medium voltage half bridge silicon carbide MOSFET power modules. The paper presents, design of a reduced isolation capacitance regulated DC-DC power supply and a gate driver with an active Miller clamp circuit for a 10 kV half bridge SiC MOSFET power module. Designed power supply and the gate driver circuit are verified in a double pulse test setup and a continuous switching operation using the 10 kV half bridge silicon carbide MOSFET power module. An in-depth experimental verification and detailed test results are presented to validate the gate driver functionality. The designed gate driver circuit shows satisfactory performance with increased common mode noise immunity and protection against the Miller current induced unwanted turn on.

A.1 Introduction

Medium voltage (MV) silicon carbide (SiC) MOSFETs are emerging as promising devices due to their capability of blocking higher voltages and switching at higher frequencies with increased thermal conductivity compared to their Silicon (Si) counterparts [1]. With latest technological improvements these devices are reaching the level of maturity to be considered for medium voltage and high power conversion applications e.g., solid state transformer [2]. Considering high $\mathrm{d}v/\mathrm{d}t$ switching transients, intrinsic device parasitics together with parasitic capacitance external to the device are crucial and require careful optimization to utilize SiC MOSFETs at their full potential [3], [4]. In a half bridge power module, the mid-point experiences high $\mathrm{d}v/\mathrm{d}t$ during switching transients. The isolation barriers inside the power modules and interfacing circuitry which experiences the $\mathrm{d}v/\mathrm{d}t$, introduces the common mode (CM) currents due to capacitive coupling. One of the dominant paths for this CM current is through an isolation barrier of the DC-DC power supply of high side (HS) gate driver circuit as graphically illustrated in Fig. A.1. For reliable operation, and in order to maintain the gate driver control signal fidelity, this CM current needs

to be attenuated. The magnitude of the CM current is directly affected by the $\mathrm{d}v/\mathrm{d}t$ and isolation capacitance (C_{iso}) based on A.1.

$$i_{\mathrm{cm}} = C_{\mathrm{iso}} \cdot \frac{\mathrm{d}v}{\mathrm{d}t} \tag{A.1}$$

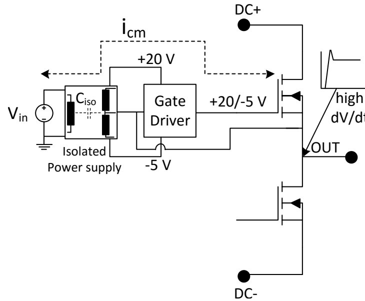


Fig. A.1: Schematic representation of common mode current path for the high side gate driver power supply

Fast switching transients in the MV SiC MOSFETs can result in $\mathrm{d}v/\mathrm{d}t$ as high as 30 kV/µs, which imposes the requirement for a very low isolation capacitance (< 5 pF) in the gate driver circuitry [5]. Readily available galvanically isolated power supplies and driver integrated circuits (ICs) with target application for 6.5 kV IGBTs limits its application for SiC devices with voltage rating of 10 kV and higher. Furthermore, commercially available regulated isolated power supplies with insulation voltage rating of 10 kV or above has an isolation capacitance in the range of 10–20 pF [6]. Recent publications have demonstrated a gate driver power supply for 10 kV SiC MOSFETs/15 kV SiC IGBTs. These are unregulated, which requires an additional stage to achieve voltage regulation [7],[8]. In addition to the CM current, the high $\mathrm{d}v/\mathrm{d}t$ switching transients can induce undesirable turn on in a half bridge power module due to the Miller effect, when the complementary switch is turning on [9]. Taking these above mentioned considerations into account, this paper presents the design of a regulated power supply with an isolation capacitance of 2.6 pF and a gate driver circuit that incorporates an active Miller clamp functionality for stably driving a 10 kV SiC MOSFET.

DC-DC isolated power supply

This section presents the design of a regulated DC-DC isolated power supply. Design considerations for the high insulation voltage and low isolation capacitance transformer are also discussed with measured key parameters.

Power supply topology

The designed power supply utilises a Flyback topology with dual secondary windings as shown in Fig. A.2. In order to achieve compact size, a Flyback controller IC (LT8302) with an integrated switch is chosen. The IC operates in boundary conduction mode (BCM) or discontinuous conduction mode (DCM) with a variable switching frequency (12 to 400 kHz) and regulates the output voltage by sensing transformer primary winding voltage. Voltage regulation based on primary side sensing eliminates the need of a feedback circuitry from secondary side i.e optocoupler, which would contribute as an additional isolation capacitance. Furthermore, a BCM or DCM in comparison to the continuous conduction mode (CCM) of operation facilitates a reduced requirement of the primary magnetizing inductance. Lower and upper boundary for primary magnetizing inductance of 5.17 µH $\leq L_\mathrm{p} \leq$ 931 µH is identified based on: the inductance value for which Flyback operates in boundary conduction mode and minimum inductance requirement imposed by the Flyback controller. Small

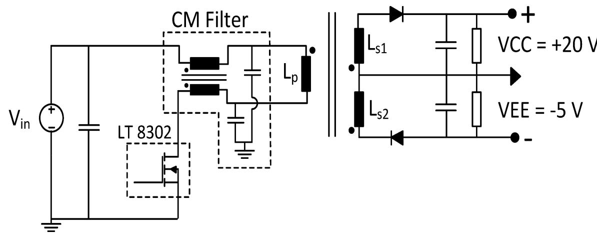
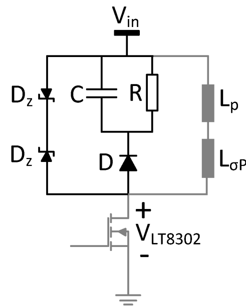
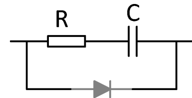


Fig. A.2: Schematic of a designed Flyback converter

Primary switch snubber



Secondary diode snubber



(a) (b)

Fig. A.3: Schematic of (a) primary switch and (b) secondary snubber circuit

magnetizing inductance is desirable because, for a given geometry and magnetic property of a core material, smaller magnetizing inductance yields: fewer number of windings, smaller leakage inductance and lower coupling capacitance. The

requirement for the Flyback output voltages of +20 V and −5 V in reference to secondary mid-point is determined based on the recommended turn on/off driving voltages for a 10 kV SiC MOSFET. A high frequency common mode choke with Y capacitors are placed between the primary winding and control IC to provide a high impedance path for the common mode currents and redirecting it to ground, respectively.

A.1.1 Transformer design

A major requirement for the Flyback transformer is to achieve a low coupling capacitance between the primary and secondary windings. This coupling capacitance is dependent on the distance between the primary to secondary windings and the area occupied by the transformer windings on the core. A significant and potentially dominant contribution of capacitive coupling is present between the primary and secondary windings through the transformer core. Graphical representation of the transformer design is presented in Fig. A.4 and the electrical parameters for the designed transformer are summarised in Table A.1. A MnZn toroidal core (TN32/19/13) utilising medium frequency and

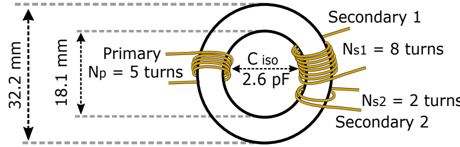


Fig. A.4: Graphical representation of the designed transformer

Table A.1: Measured electrical parameters of the Flyback transformer using a keysight E4990A impedance analyser.

Parameters	Values
Isolation Capacitance (C_{iso})	2.6 pF
Primary magnetizing inductance (L_{p})	52.7 µH
Secondary 1 magnetizing inductance (L_{s1})	134 µH
Secondary 2 magnetizing inductance (L_{s2})	8.6 µH
Primary leakage inductance ($L_{\sigma\mathrm{p}}$)	3.5 µH
Secondary 1 leakage inductance ($L_{\sigma\mathrm{s1}}$)	4.5 µH
Secondary 2 leakage inductance ($L_{\sigma\mathrm{s2}}$)	0.3 µH

high permeability magnetic material (3F3) is chosen for the transformer. A high inductance factor $A_{\mathrm{L}} = L/N^2$ of 2270 nH for the chosen core facilitates with the lower number of windings to achieve the required inductance and thereby reducing the area occupied by the winding on the transformer core. The number of turns for primary and secondary windings are determined based on the design constraints imposed by the Flyback controller IC, the desired inductance value and the primary to secondary winding voltage ratio. The

primary and secondary windings are spaced distantly on the core to increase the physical distance between them, which helps to provide low isolation capacitance but results in an increased leakage inductance of the transformer due to poor magnetic coupling. The core has an insulation coating rated for 2 kV DC. To achieve a higher insulation voltage withstand capability a triple insulated wire is utilised for transformer windings. A layer of insulation tape is placed between the winding and transformer core, lowering the isolation capacitance further by reducing the coupling through the transformer core. Isolation capacitance for the designed transformer is measured to be 2.6 pF using a Keysight E4990A impedance analyser.

A.1.2 Design consideration for primary switch snubber and secondary snubber

Transformer leakage inductance introduces voltage spikes across the primary switch and secondary diodes during turn off. To protect the Flyback switch from over voltages and suppress the voltage spikes within allowable limits, an RCD snubber with a Zener clamp and an RC snubber is designed for the switch and diode, respectively [10]. Resistance and capacitance value for RCD snubber is chosen such that the RC time constant is smaller than the blanking time of the Flyback controller IC, within which the excess energy form the leakage inductance should be dissipated in order to sense the primary winding voltage correctly. For Zener clamp, the Zener diode is chosen such that the Zener voltage is below the breakdown voltage of the Flyback switch.

A.2 Design of a gate driving stage with active Miller clamp functionality

A functional schematic of the gate driving circuitry is presented in Fig. A.5. A high-speed gate driver IC from IXYS (IXDN614) with peak source/sink current capability of 14 A and a low propagation delay is chosen as a primary driving stage. The output of the driver IC is connected to the gate pad with gate resistance R_g. To isolate the control circuit from the high voltage and remove coupling, the gate signals are transferred optically using an optic fiber link. Preliminary tests showed possibility of unwanted turn on of the SiC MOSFETs due to the Miller effect under high dv/dt switching transients. To mitigate this an active Miller clamp circuit is designed and incorporated into the gate drive [11]. Feedback for the Miller clamp circuit is provided by utilizing the gate-source voltage and the input gate signal. A comparator circuit compares the gate-source voltage with a reference voltage and outputs logic high, when the sensed voltage reaches below the reference voltage. An additional logic gate is utilized so that the clamp is activated only when the turn off gate command

Fig. A.5: Schematic of the gate driving stage with active miller clamp circuit

is received and gate-source voltage is below the reference voltage. Reference voltage for the clamp is chosen to be lower than the SiC MOSFETs threshold voltage, meaning that the device turn on/off characteristics are not affected by the Miller clamp and the clamp is only activated after the MOSFET is turned off. To provide a low impedance path for the Miller current, an N - channel MOSFET with low on-state resistance of 50 mΩ is used as a clamping switch. A capacitor with significantly higher capacitance value compared to the device gate-drain capacitance (C_{gd}), is placed between the source of the N - channel MOSFET and ground plane to prevent rise in clamp voltage due to the flow of Miller current. An image of the gate driver and its specification are presented in Fig. A.6 and Table A.2, respectively.

Fig. A.6: Image of a designed gate driver circuit

Table A.2: Gate driver specification

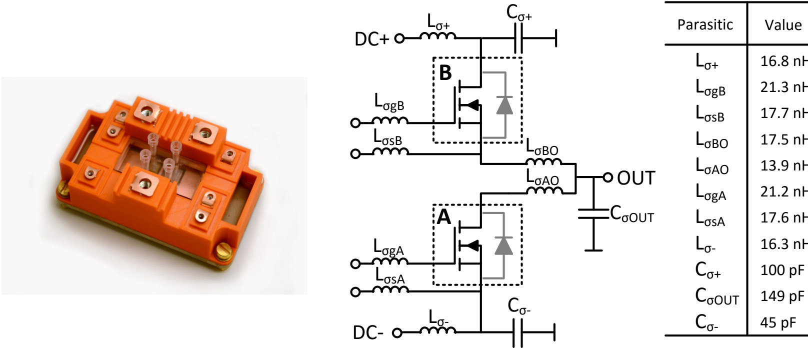
Parameters	Values
Nominal input voltage (v_{in})	12 V
Turn-on gate drive voltage ($v_{gs(on)}$)	+19 V
Clamp voltage (v_{clamp})	−4.5 V
Flyback under voltage lockout	7.5 V
Gate resistance (R_g)	17 Ω / 25 Ω

For a 10 kV SiC MOSFET, a threshold voltage of 2.6 V at the drain current of 1 mA, and internal gate resistance $R_{g(int)}$ of approximately 3 Ω are identified from a static characterisation. This threshold voltage for the SiC MOSFETs may drift due to temperature dependance and application of gate bias stress [12].

Also, the sensed gate-source voltage (v_{gs}) and actual voltage across the device parasitic gate-source capacitance (v_{Cgs}) in reference to Fig. A.5 are different due to the internal gate resistance of the device and parasitic inductance in the gate-source loop. An analytical approach considering the SiC MOSFET parasitics as described in [3], [13], [14], was used to study the fluctuation of gate voltage due to Miller current. Taking into account the above mentioned considerations, a reference voltage of 0 V is chosen to avoid an occurrence, where the clamp is turned on before the voltage across the gate-source capacitance C_{gs} reaches below the 2.6 V threshold voltage.

A.3 Device under test

For the test two 10 kV/10 A SiC MOSFET half bridge power modules with and without external JBS diodes are utilised. One such module with external SiC JBS diodes is presented in Fig. A.7 along with the schematic displaying the power module parasitics extracted form ANSYS Q3D [4]. The shown power module is packaged in-house at Aalborg University and populated with two generation 1 10 kV/10 A SiC MOSFET and 10 kV SiC JBS diode dies from Wolfspeed.



Parasitic	Value
$L_{\sigma+}$	16.8 nH
$L_{\sigma gB}$	21.3 nH
$L_{\sigma sB}$	17.7 nH
$L_{\sigma BO}$	17.5 nH
$L_{\sigma AO}$	13.9 nH
$L_{\sigma gA}$	21.2 nH
$L_{\sigma sA}$	17.6 nH
$L_{\sigma-}$	16.3 nH
$C_{\sigma+}$	100 pF
$C_{\sigma OUT}$	149 pF
$C_{\sigma-}$	45 pF

Fig. A.7: Picture of 10 kV/10 A halfbridge power module populated with generation 1 10 kV SiC MOSFETs and SiC JBS diodes from Wolfspeed and schematic showing power module parasitic with table of values.

Test bench design and experimental results

The designed gate driver circuit and isolated power supply are tested in a double pulse test setup to evaluate CM noise immunity and the Miller effect induced turn on possibility. As presented in Fig. A.8 (a), a high side (HS) MOSFET and a low side (LS) diode for freewheeling is utilised in the double pulse test.

The CM current for the high side gate driver power supply and gate-source voltage of the low side MOSFET are monitored during the test. To validate the gate driver functionality in continuous switching operation, a test setup as presented in Fig. A.8 (b) is used, where the half bridge is switched in an open loop control with a switching frequency of 10 kHz. The power module

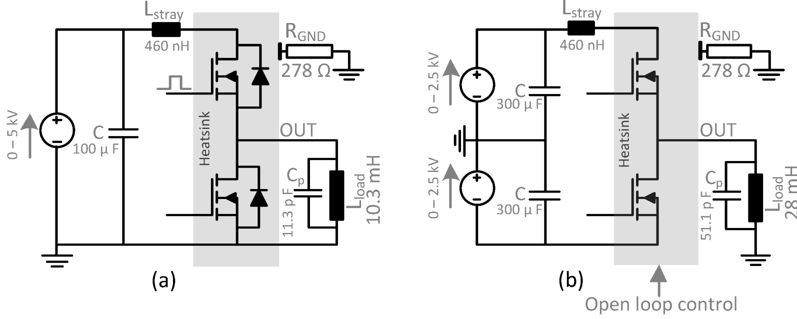


Fig. A.8: Simplified schematic of the (a) double pulse and (b) half bridge test setup used to validate gate drive performance

is attached to a low stray inductance, stacked aluminium bus-bar with low ESR/ESL capacitors. The ceramic substrate layer in the power module DBC forms a parasitc cpacitance between the copper plane on the top of a DBC and the mounting baseplate. The parasitic capacitance $C_{\sigma(\mathrm{OUT})}$ is a source of EMI that introduces CM current during the high dv/dt switching transitions [15], [16]. For improved EMI performance and owing to safety concerns, the heatsink on which the power module is mounted is grounded using a 278 Ω power resistor based on the analysis described in [3].

Double pulse test

The half bridge output voltage (v_{OUT}) and gate-source voltage for the low side switch ($v_{\mathrm{gs(LS)}}$) during the first turn off and the second turn on pulse in a double pulse test at 5 kV DC-link voltage (v_{DC}) are shown in Fig. A.9. The gate-source voltage during the switching transition is approximately −4.5 V with small oscillations, which is well below the threshold voltage of 2.6 V for a 10 kV SiC MOSFET. The CM current measurement on the input side of the gate driver without any common mode filter on the primary side power supply at a v_{DC} of 4 kV is presented in Fig. A.10. The maximum peak amplitude and mean value of the CM current is approximately 172 mA and 58 mA, respectively for the turn on dv/dt of 16.5 kV/μs, suggesting an isolation capacitance of 3.5 pF being present.

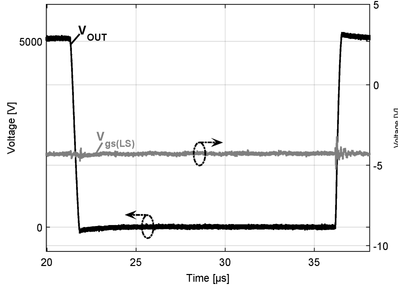


Fig. A.9: Measured half bridge output voltage and gate-source voltage of the low side switch in a double pulse test. Test condition: V_{DC} = 5 kV, Drain current i_{d} = 5 A

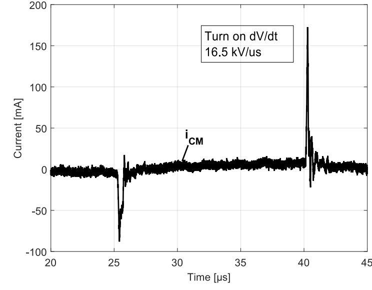


Fig. A.10: Measured common mode current in a double pulse test. Test condition: V_{DC} = 4 kV, Drain current i_{d} = 5 A

A.3.1 Continuous switching operation

In the first case, the half bridge is switched with a duty cycle of 0.5. Under, this condition the the load current magnitude is high enough so that the MOSFET output capacitance (C_{OSS}) charges/discharges within the 2 µs deadtime. This implies that the MOSFET turns on with almost zero voltage across it and achieves soft turn on. Fig. A.11 and Fig. A.12 show the gate current and gate-source voltage for the low side MOSFET, and output voltage of the half bridge module during the turn on and turn off switching transitions. As seen in Fig. A.11, due to the zero voltage turn on, the Miller plateau is not present in the gate-source voltage and the transition is smooth during the MOSFET turn on. With a gate drive voltage of +19/-4.5 V and a gate resistance of 25 Ω, the peak gate current is limited to approximately 1 A. Looking at the turn off switching transition in Fig. A.12, when the turn off command is applied, the gate current (i_{g}) increases from zero to the peak value resulting in a high frequency oscillation in the gate voltage due to voltage drop ($L_{\mathrm{g}} \cdot \frac{\mathrm{d}i_{\mathrm{g}}}{\mathrm{d}t}$) across the parasitic inductance in the gate-source switching loop. The half bridge output voltage starts rising once a gate-source voltage reaches the Miller level. A small delay after the gate-source voltage crosses zero Volts, a steep change in the gate-source and gate current is identified due to the turn on of the Miller clamp. Measured gate-source voltage and the gate current validates the fundamental functionality of the gate driver and DC-DC power supply to operate under continuous switching operation. The measurements presented clearly indicates the satisfactory performance in terms of gate driving voltage and power requirements.

The test was performed at 5 kV bus voltage. The inductor current and half bridge output voltage, together with the drain current of the high side and low side MOSFETs are presented in Fig. A.13. Under this condition,

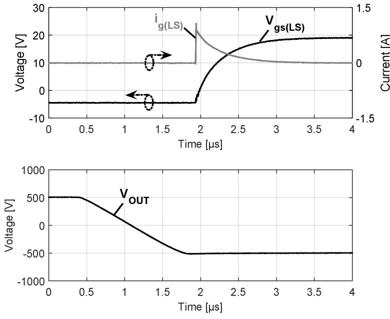


Fig. A.11: Measured low side MOSFET gate current, gate voltage and half bridge output voltage during turn on transition.

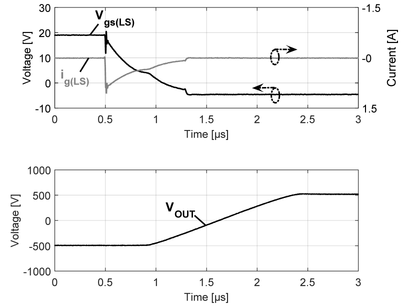


Fig. A.12: Measured low side MOSFET gate current, gate voltage and half bridge output voltage during turn off transition.

the maximum dv/dt during the switching transition is 5.4 kV/µs. During the switching transition, a finite magnitude and opposite polarity of the drain current is identified in the HS MOSFET as well as the LS MOSFET, which is due to the displacement current charging/discharging the MOSFET output capacitance.

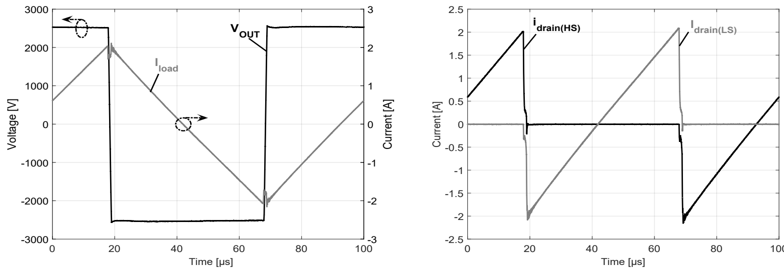


Fig. A.13: Measured half bridge output voltage, inductor current, high side and low side MOSFET drain currents

A.3.2 MOSFET first quadrant operation: turn on/off switching transition

To verify the performance under hard commutation, an open loop sine wave pulse width modulation with a modulation index of 0.02 is performed. Fig. A.14 shows the drain currents, half bridge output voltage and gate-source voltage during the turn on and turn off switching transitions at a V_{DC} of 4.6 kV. This instant corresponds to the negative cycle of the load current during which the drain current for the low side MOSFET is positive (i.e first quadrant operation).

It should be noted that the considerably large difference in the drain current magnitude at the beginning and at the end of the switching period is due to the higher DC link voltage (4.6 kV) and the relatively long switching period (50 ± 0.02 μs), producing the load inductor (31 mH) ripple current of 2.6 A. As

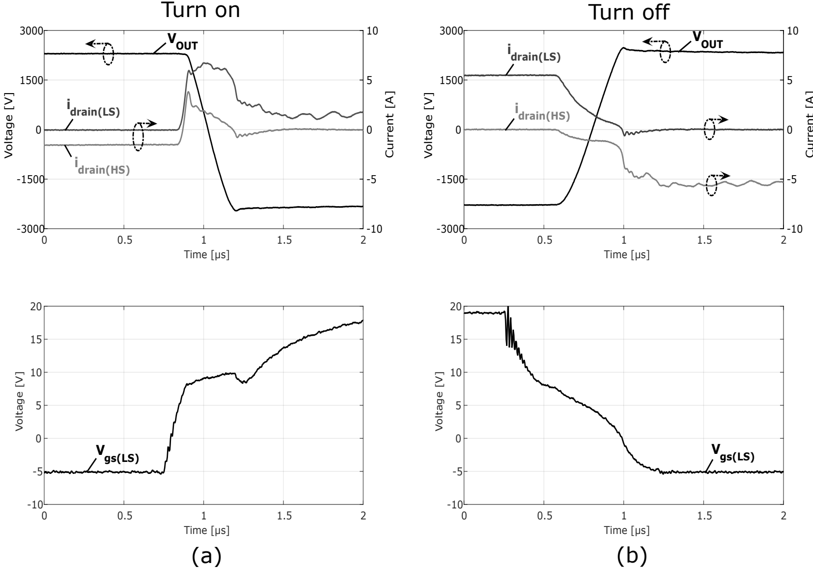


Fig. A.14: Measured half bridge output voltage, MOSFET drain currents and low side MOSFET gate-source voltage during (a) turn on and (b) turn off transition.

seen in Fig. A.14 (a), once the turn on command is received the gate voltage starts to rise. The drain current in the low side switch starts to increase as the gate-source voltage crosses the MOSFET threshold voltage of approximately 2.6 V. The gate-source voltage reaches the Miller level, when the LS MOSFET drain current equals the load current. At this point, the load current is fully commutated from the high side MOSFET body diode to low side MOSFET followed by the reverse recovery process. A non-flat Miller plateau in the gate-source voltage is due to the modest amount of transconductance of a SiC MOSFET in the saturation region [17]. The half bridge output voltage completes its transition during the Miller plateau after which the LS MOSFET is fully turned on and enters into an ohmic region.

The turn off process shown in Fig. A.14 (b), is similar to the one described in a previous section. The experimental verification performed, confirms a smooth and typical turn on switching transition under the hard commutation in continuous switching operation.

MOSFET third quadrant operation: turn on/off switching transition

Fig. A.15 shows the drain currents, half bridge output voltage and gate-source voltage during the turn on and turn off switching transition at a V_{DC} of 4.6 kV. This instant corresponds to the positive cycle of the load current during which

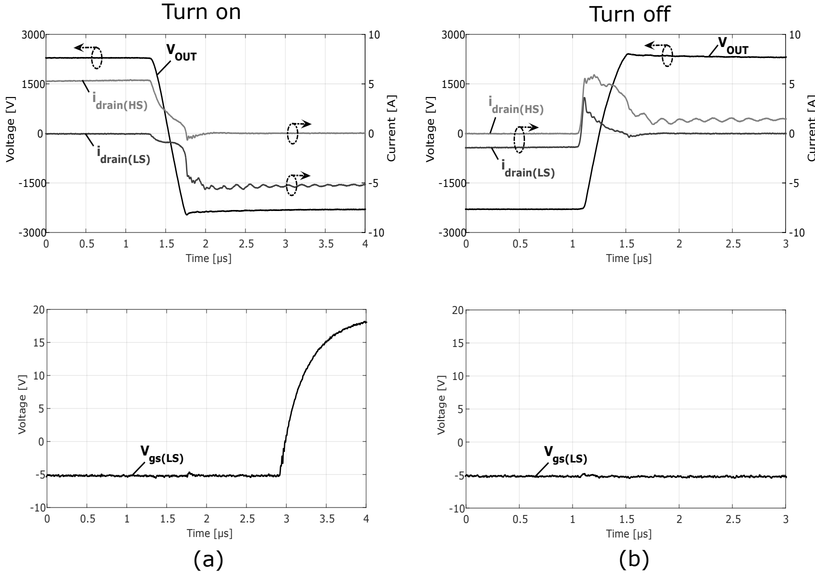


Fig. A.15: Measured half bridge output voltage, MOSFET drain currents and LS MOSFET gate-source voltage during (a) turn on and (b) turn off transition.

the drain current for the low side MOSFET is negative (i.e third quadrant operation). As shown in Fig. A.15 (a), the LS MOSFET achieves zero voltage turn on in third quadrant as the drain-source voltage completes its transition during the deadtime and the LS body diode is conducting during the deadtime. The LS MOSFET turns on after this point and operates in the third quadrant.

The $\mathrm{d}v/\mathrm{d}t$ is high during the hard commutation when, the HS MOSFET turns on and the LS side MOSFET body diode reverse recovers and it is one of the adverse conditions for the Miller clamp in the LS gate driver. This condition is presented in Fig. A.15 (b). The LS MOSFET is off after the gate-source voltage has changed from the positive to the negative drive voltage and LS body diode is conducting during the dead time. The moment at which the HS MOSFET is turned on is identified from the HS drain current and change in the half bridge output voltage. During this $\mathrm{d}v/\mathrm{d}t$ transition, the LS gate-source voltage remains unaffected. The experimental verification performed, confirms the Miller clamp functionality during the hard turn on switching transition of complementary MOSFET in continuous switching operation.

A.4 Conclusion

The paper discusses key challenges in designing the gate driver circuit for fast switching MV SiC MOSFET half bridge power modules. The design of an isolated DC-DC regulated power supply and key design considerations for a low coupling capacitance isolation transformer is presented. A prototype for a gate driver circuit with a very low isolation capacitance and the Miller clamp functionality is developed. The gate driver circuit was exposed to $\mathrm{d}v/\mathrm{d}t$ of up to 20 kV/µs in the double pulse test setup. Further verification was performed in continuous switching operation with switching frequency of 10 kHz. An in depth analysis of the half bridge switching waveforms during the turn on and turn off transition are presented considering different modes of MOSFET operation. The experimental results show that, the design satisfies the gate drive requirements for a 10 kV half bridge SiC MOSFET power module with increased CM noise immunity and protection against the Miller current induced unwanted turn on under the high $\mathrm{d}v/\mathrm{dt}$ switching transients.

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Paper B

Impact of Power Module Parasitic Capacitances on Medium Voltage SiC MOSFETs Switching Transients

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The layout has been revised.

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Abstract

Increased switching speeds of WBG semiconductors result in a significant magnitude of the displacement currents through power module parasitic capacitances which are inherent in packaging design. This is of increasing concern particularly in case of newly emerging medium voltage SiC MOSFETs since the magnitude of the displacement currents can be several order higher due to the fast switching transients and increased voltage magnitudes of the SiC MOSFETs compared to their Si counter parts. The severity intensifies when the magnitude of the displacement current become comparable to a significant fraction of SiC MOSFETs rated current, leading to the worsened impact on the converter EMI as well as performance in terms of switching losses. The key objective of the paper is to provide a detail insight into the impact of the module parasitic capacitances on the SiC MOSFET switching dynamics and losses. To realize this, a well defined approach to dissect the switching energy dissipation is proposed, based on which the detail analysis and quantitative measurements of the module parasitic capacitance impact in terms of added switching energy losses and common mode currents is investigated using a custom packaged 10 kV half bridge SiC MOSFET power modules. The theoretical analysis and experimental results obtained from dynamic as well as static characterization reveals that the impact of the module parasitic capacitance on the switching energy dissipation is two-fold and substantially adverse such that it can not be overlooked considering its intended application in the high power medium voltage power electronic converters.

B.1 Introduction

The medium voltage (MV) Silicon Carbide (SiC) MOSFETs are evolving as a mature technology due to continuous refinements and technological advancement in the SiC device fabrication technology over the past few years. In particular, the modern MV SiC MOSFETs technology in 6.5 kV or higher voltage class has gained increased interest in the medium voltage and high power conversion applications such as solid state transformers, renewable, traction, MV motor

drives and grid support [1]–[2]. Recently, these devices have been demonstrated in a multi-chip half-bridge power module packages that are specially tailored to be utilized in such applications [3]–[4]. In a typical power module, the parasitic capacitances are inevitably present due to the capacitive coupling between the top copper traces on direct bonded copper (DBC) and mounting baseplate as shown in Fig. B.1. Some of these parasitic capacitances get charged or discharged during every switching transient which introduces displacement currents and give rise to the switching losses as well as electromagnetic interference (EMI) issues. The magnitude of these displacement currents is governed by

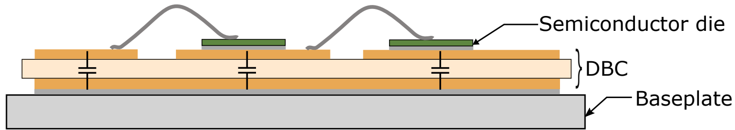


Fig. B.1: Schematic showing the parasitic capacitances in a power module.

the dv/dt appearing across the capacitance, the values of module parasitic capacitances and the heatsink grounding impedance [5]. The dv/dt in the wide band gap (WBG) devices are significantly higher compared to the Si devices which increases the magnitude of the displacement currents to an extent, where accurate quantification and prediction capability of the module parasitic capacitances is key in order to design modules that qualify for the electromagnetic compatibility (EMC) standards [2], [6]–[7]. Apart from its impact on worsening the electromagnetic interference (EMI) performance, the displacement currents due to module parasitic capacitances result in the diminished switching performance in terms of losses. Therefore it is desired to minimize the module parasitic capacitances, however the area occupied by the semiconductor dies, lower stray inductance requirements, thermal performance and cost are the key factors that limits the power module designer in regards to which extent the coupling capacitances can be reduced.

An EMI investigation performed on SiC based power electronics converter for a range of applications in [6], [8]–[9], identified module parasitic capacitances as one of the dominant contributors to the conducted EMI. For example, the simulation based parametric study performed by [10] to investigate the impact of module parasitic capacitance on the switching transients and energy loss for MV SiC MOSFET show that understanding the high dv/dt induced displacement currents due to module packaging is very important to accurately model the device switching behaviour and switching energy dissipation. It can be hard to distinguish the impacts of module parasitic capaciatnce, since these capacitances in turn affects the switching dynamics which changes the switching energy dissipation. In addition to this the parasitic capacitance also adds losses on its own as will be discussed in this paper. Thus it is difficult without a detailed analysis to quantify the different mechanisms impact on the switching losses.

In [11], authors point out the importance of the module parasitic capacitances on the switching losses and investigate the impact for a discrete 10 kV SiC MOSFET package by adding an arbitrary value of an external capacitor in parallel to the MOSFET which essentially acts like a snubber. Even though it mimics the module parasitic capacitance it does not provide a fair comparison in terms of an actual power module layout. Furthermore, authors do not provide the dissection of the switching energy dissipation which is crucial to understand the impact of module parasitic capacitances in relation to the overall switching losses. In this paper, authors provide a complete dissection of the switching energy dissipation to understand the impact of module parasitic capacitance on the overall switching losses. This is done by analysing the switching transients and quantitative comparison of the module parasitic capacitance related losses for the custom made 10 kV SiC MOSFET half bridge power modules in two different layouts.

This paper is organized as follows. In Section II, the details of the case study, i.e custom made 10 kV half bridge SiC MOSFET power modules as well as its key parasitic parameters are presented, while the experimental test bench and measurement methodology utilized to investigate the impact of module parasitic capacitances on the SiC MOSFET switching transients is introduced in Section III. In Section IV, the high $\mathrm{d}v/\mathrm{d}t$ and module parasitic capacitance induced displacement current paths during the MOSFET turn-on as well as turn-off switching transient is analyzed based on the theoretical analysis and experimental results. Since these displacement currents can not be measured directly, an indirect methodology to obtain the displacement currents from the accessible half bridge module current measurements is proposed and validated experimentally in Section V. In Section VI and VII, a complete dissection of the switching energy dissipation is presented based on which the impact of module parasitic capacitance on the turn-on and turn-off switching energy dissipation is discussed in detail.

B.2 Device under test - 10 kV half bridge SiC MOSFET power module

In the present case study, two versions of the custom made 10 kV single die half-bridge SiC MOSFET power modules (referred here as A and B) with different DBC layouts are utilized, the difference being the reduced capacitance DBC layout for module B under restraint of keeping the terminal configurations similar. The picture and top view of the DBC layout for the two power modules is presented in Fig. B.2.

The half-bridge power modules are populated with third generation 10 kV SiC MOSFETs and anti-parallel SiC junction barrier Shcottky (JBS) diodes [12], [13] which are soldered on a 0.63 mm AlN DBC with a 5 mm[1]AlSiC baseplate.

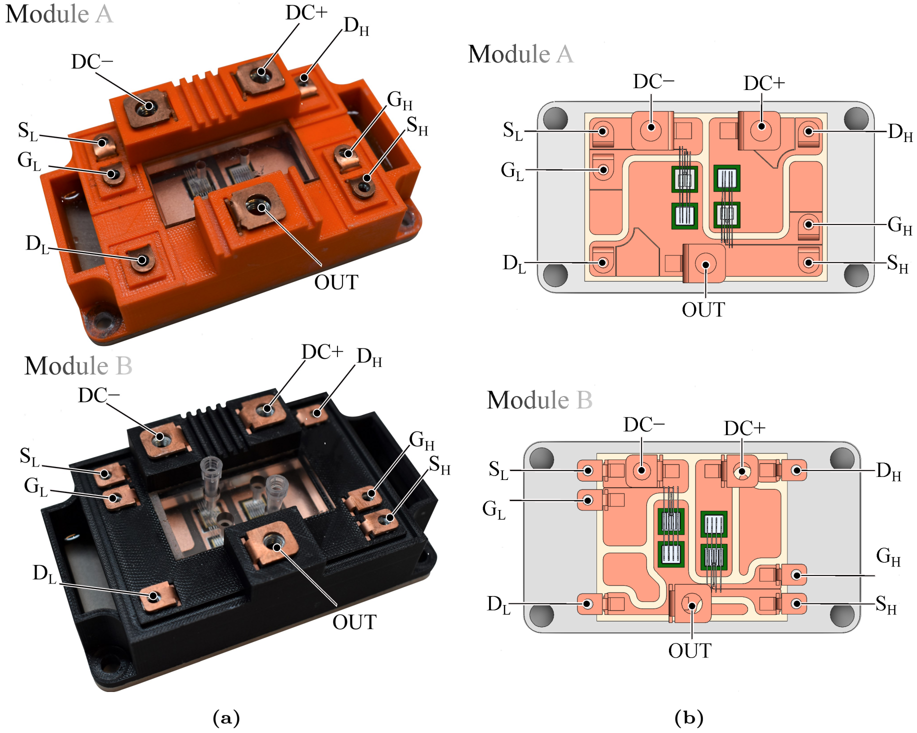


Fig. B.2: (a) Picture and (b) Solidworks rendering for the 10 kV half-bridge SiC MOSFET power modules A and B with different DBC layouts.

The module parasitic capacitances in a half bridge power module resulting from Cu-AlN-Cu layers of the DBC is presented in Fig. B.3, where $C_{\sigma+}$ is the distributed parasitic capacitance from the DC+ plane to the baseplate, $C_{\sigma\mathrm{GH}}$ is from the high-side (HS) gate plane to the baseplate, $C_{\sigma\mathrm{OUT}}$ is from the output plane to the baseplate, $C_{\sigma\mathrm{GL}}$ is from the low-side (LS) gate plane to the baseplate and $C_{\sigma-}$ is from the DC– plane to the baseplate. (See Fig. B.2b for the physical reference.) Although, both modules A and B have unused copper areas on the DBC, which are not etched due to manufacturing reasons. In the design process it was ensured that the EMI performance was still good and the unused copper area on the DBC meets the necessary isolation requirements. The parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ are crucial since these capacitances experience high $\mathrm{d}v/\mathrm{d}t$ during the switching transients and have dominant impact on the EMI and switching performance. In [14], [15], [16] various approaches are proposed for reducing the module parasitic capacitances by means of introducing

[1]In this publication, the power module AlSiC baseplate thickness has been mistakenly reported as 5 mm instead of 3 mm. In spite of this error, the text has not been revised and the appended publication is maintained in the original form of published version.

an additional copper layer within a DBC that acts as a shield, by increasing the thickness of the DBC ceramic substrate or using a flip-chip technology for the low side power semiconductor devices. Whereas in [8], portion of a bottom copper layer of the DBC is replaced by introducing a low permittivity material (air), thereby reducing the module parasitic capacitances and consequently attenuating the CM EMI. For the case at hand, the design of power module B was revised with simple measures to obtain reduced coupling capacitances compared to A by reducing the copper area connected to the output as well as high side gate plane without significantly penalizing the stray inductances and serves as a good showcase here [7]. This facilitates in a comparison simple enough to demonstrate the impact of the module parasitic capacitances on switching transients and switching losses. The parasitic capacitances for two

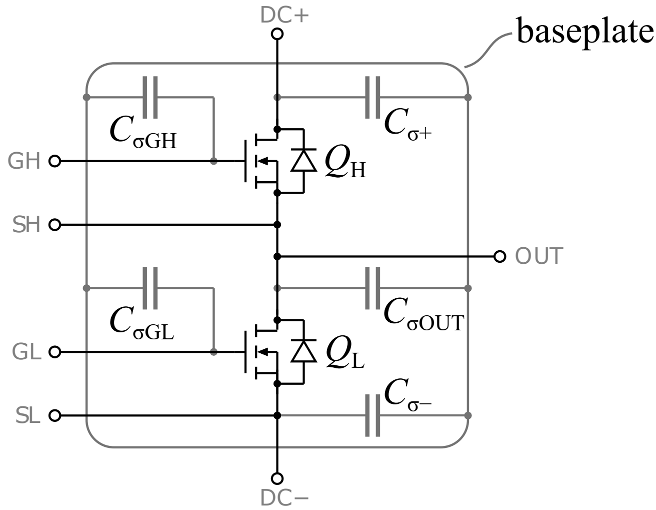


Fig. B.3: Schematic representation of the distribution of the parasitic capacitances in a half bridge power module.

power modules were obtained from the ANSYS Q3D [17] are presented in Table B.1. For the capacitance extraction in the ANSYS simulations, the permittivity for the packaging materials are taken from material datasheet supplied by the manufacturer.

Table B.1: Values of parasitic capacitances obtained from ANSYS Q3D for the 10 kV half-bridge SiC MOSFET power modules A and B. (All in [pF])

Module	$C_{\sigma+}$	$C_{\sigma\mathrm{GH}}$	$C_{\sigma\mathrm{OUT}}$	$C_{\sigma\mathrm{GL}}$	$C_{\sigma-}$
A	108	20.5	159.2	23.5	47.5
B	68.1	12.4	81.4	35.6	32.7

B.2.1 Equivalent impedance network between power module and the heatsink

Apart from the power module layout and the dv/dt, the displacement currents are also affected by the heatsink grounding impedance [18]. Thus in order to be able to analyze the displacement currents due to module parasitic capacitances, an equivalent impedance network between the power module and the heatsink connection is needed, which in turn enables the prediction of the displacement currents based on the voltage measurements as will be presented later.

Since slowing down the switching speed is adverse to the desired fast switching characteristics and lower switching losses of the SiC MOSFETs, only heatsink grounding is left as an available design choice. In a power electronic converter the power module is mounted on the heatsink which is mostly kept at ground potential owing to the safety reasons but some applications may allow to keep heatsink floating or connected through an impedance network although this is exceptional [6]. Considering the case where heatsink is shorted to ground, during the switching transients the module parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ experience the same dv/dt as appearing at the output terminal of the half-bridge, whereas the module capacitances $C_{\sigma+}$, $C_{\sigma\mathrm{GL}}$ and $C_{\sigma-}$ do not experience this dv/dt since these are referenced to a fixed DC+ or DC– potential. Due to the dv/dt appearing at the output terminal of the half-bridge the capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ get charged or discharged by the displacement currents during the turn-on and turn-off switching transient respectively. The differential voltage between the high side gate and source terminal is comparatively small such that the impedance between the output terminal of the half-bridge and heatsink can be modelled as parallel combination of capacitance $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$, which is denoted as Z_1 in Fig. B.4. The impedance between the heatsink and the ground node can be modelled as a parallel combination of the module capacitance $C_{\sigma+}$, $C_{\sigma-}$, $C_{\sigma\mathrm{GL}}$ denoted as Z_2 and grounding impedance Z_{gnd}. The resulting equivalent impedance network between the half-bridge output terminal to ground is presented in Fig. B.4 [5].

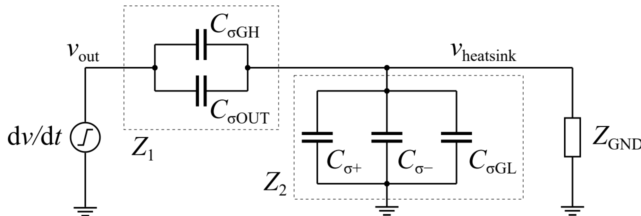


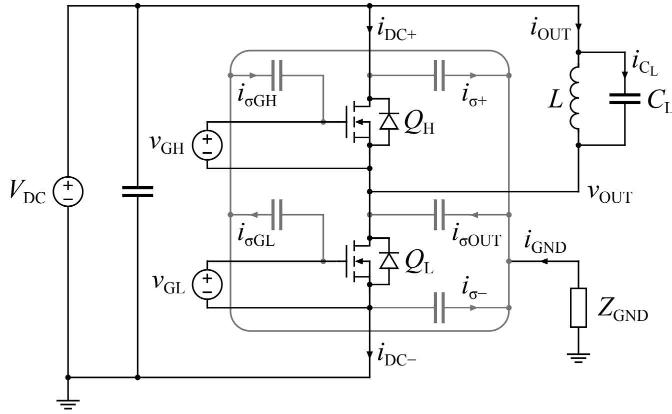
Fig. B.4: Schematic of the equivalent impedance network between the half-bridge output terminal and ground.

The magnitude of the displacement currents during the turn-on and turn-off

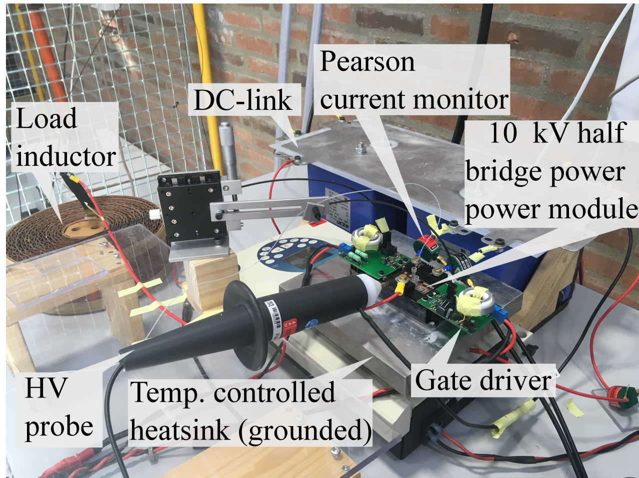
switching transient due to the module parasitic capacitance $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ can be determined as $i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} \approx (C_{\sigma\mathrm{OUT}} + C_{\sigma\mathrm{GH}}) \cdot \mathrm{d}(v_{\mathrm{OUT}} - v_{\mathrm{heatsink}})/\mathrm{d}t$. This method thus allows direct prediction of the $i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}$ for the known values of module parasitic capacitances. The displacement currents $i_{\sigma\mathrm{OUT}}+i_{\sigma\mathrm{GH}}$ conduct through the ground loop resulting in an increased amount of conducted EMI and switching energy dissipation.

B.3 Experimental test bench

The experiments are performed by mounting the half-bridge power modules A and B in a double pulse test setup. The schematic and image of the experimental setup are presented in Fig. B.5a and B.5b respectively. The power module is connected to DC power supply (XR 6000-1.0/415/+HS+LXI) through a low stray inductance busbar with two parallel connected 5 kV, 50 μF polypropylene capacitors. A 47 mH air core inductor is used as a load, whose parasitic capacitance (C_{L}) is measured to be approximately 12 pF. The air coil inductor with very low equivalent parasitic capacitance compared to the module parasitic capacitances is utilised to lessen its influence on the switching dynamics and losses. A low isolation capacitance ($\approx$ 4.8 pF) gate driver with active Miller-clamp functionality is utilized to drive the SiC MOSFETs [19]. The heatsink on which the power module is mounted is connected to the DC- potential of the busbar through copper wire providing low inductance connection and shorter ground current loop to avoid propagating the displacement currents through other ground nodes. For consistency all the module current measurements $i_{\mathrm{DC+}}$, $i_{\mathrm{DC-}}$, i_{OUT} as well as i_{gnd} are recorded using high bandwidth 200 MHz Pearson 2877 current monitors [20].To measure currents $i_{\mathrm{DC+}}$ and $i_{\mathrm{DC-}}$ with Pearson current monitor a short wire is inserted between the module DC+, DC− terminals and the busbar as can be seen in Fig.B.5b, where each of these connections introduces approximately 50 nH of stray inductance in the power loop. The voltage at the output terminal of the power module is measured utilizing Lecroy PPE 20 kV 100 MHz high voltage passive probe [21]. Both power modules A and B are tested in the same experimental setup under identical test conditions. To understand the impact of the module parasitic capacitances induced displacement currents on the SiC MOSFET switching performance, the MOSFET turn-on and turn-off switching transients are analyzed separately in Section IV in the double pulse test circuit.



(a)



(b)

Fig. B.5: (a) Schematic and (b) picture of the double pulse test bench.

B.4 Understanding Impact of power module parasitic capacitance on MOSFET turn-on and turn-off switching transients based on experimental results

B.4.1 Analysis for the turn-on switching transient

An impact of power module parasitic capacitance on the MOSFET turn-on switching transient is analyzed utilizing the double pulse test circuit and turn-on switching waveforms presented in Fig. B.5a and B.6 respectively. As shown in

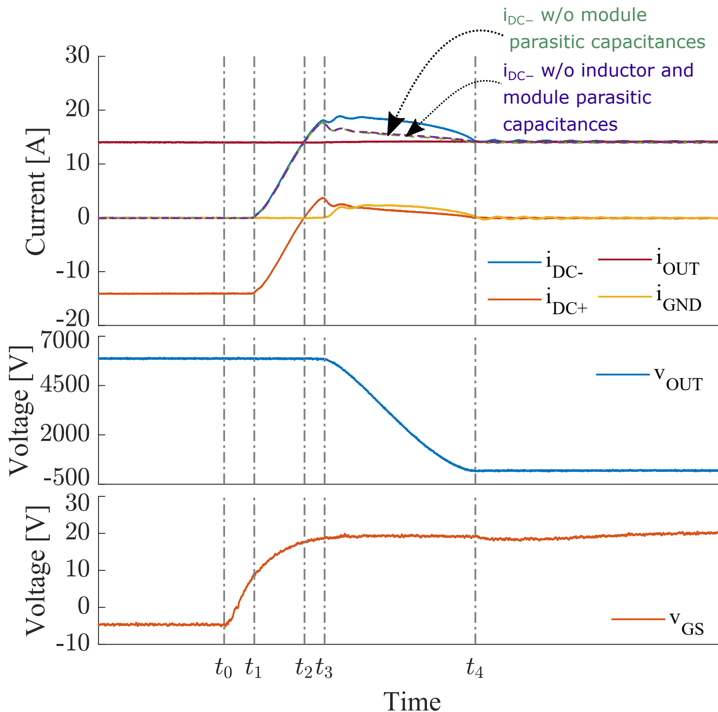


Fig. B.6: Experimental switching waveforms for the turn-on switching transient. (V_{DC} = 6 kV and i_{L} = 14 A)

Fig. B.6, at time t_0 the turn-on gate command is applied to the low side (LS) MOSFET Q_{L}. From time t_0 the gate-source voltage v_{GS} start to rise from the turn-off gate bias level and reaches the MOSFET threshold voltage level $v_{\mathrm{GS(th)}}$ at time t_1. At this time t_1 the LS MOSFET starts conducting. During the time interval t_1–t_2 the current through LS MOSFET increases and reaches the load current level i_{L} at time t_2. At this time instant the load current is completely

commutated from the high side (HS) diode to the low side (LS) MOSFET. The time instant t_1 and t_2 corresponds to the threshold and Miller level respectively for the LS MOSFET gate-source voltage. The time interval t_2–t_4 also termed as Miller region, is where the diode current goes to its peak reverse recovery and reaches zero current level. A voltage change at the output terminal of the half-bridge power module occurs within the time interval t_3–t_4. In this time interval, the LS MOSFET carries the load current plus an additional current due to charging of the combined HS MOSFET and external JBS diode output capacitance. In addition to this, the negative rate of change of voltage ($\mathrm{d}v/\mathrm{d}t$) appearing across the output terminal of the half-bridge in the time interval t_3–t_4 causes the parasitic capacitance $C_{\sigma\mathrm{OUT}}$, $C_{\sigma\mathrm{GH}}$ to discharge and C_{L} to charge with the displacement currents $i_{\sigma\mathrm{OUT}}, i_{\sigma\mathrm{GH}}$ and $i_{\mathrm{C_L}}$ respectively which is conducted through the LS MOSFET. These displacement currents $i_{\sigma\mathrm{OUT}}, i_{\sigma\mathrm{GH}}$, $i_{\mathrm{C_L}}$ produce a Joule heating in the LS MOSFET which adds to the turn-on switching losses. The measured ground current (i_{GND}) in Fig. B.6, is solely due to the discharging of the module parasitic capacitance $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$. The magnitude of the displacement current $i_{\mathrm{C_L}}$, is significantly small due to the very low parasitic capacitance of the load inductor and therefore its impact on the load current i_{OUT} is not clearly visible. The increased magnitude of the module current $i_{\mathrm{DC+}}$ during time interval t_3–t_4 due to the module parasitic capacitance related displacement currents is clearly identified from the module current measurements presented in Fig. B.6.

From t_2–t_4 the current through the LS MOSFET consists of the (i) load current, (ii) displacement currents due to charging and discharging of the HS as well as LS MOSFET and diode combined output capacitance, (iii) HS diode reverse recovery current and (iv) displacement currents due to discharging and charging of the module as well as load inductor parasitic capacitances respectively.

Although the displacement current due to discharging of the LS MOSFET and diode output capacitances is conducted through the LS MOSFET channel it can can not be measured at the DC– terminal of the half-bridge since this discharging current path is confined within the LS MOSFET and JBS diode output capacitance itself. [22].

It should be noted that the gate-source voltage during the Miller region does not remain clamped corresponding to the load current level i_L but increases due to the additional displacement currents that flow through the LS MOSFET channel. The increase in the gate-source voltage will result in a decrease in the gate-drain current charging the Miller capacitance C_{GD} hence resulting in a lower $\mathrm{d}v/\mathrm{d}t$ at the output terminal of the half-bridge. Thus the turn-on $\mathrm{d}v_{\mathrm{OUT}}/\mathrm{d}t$ decreases with increasing value of module parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$.

B.4.2 Analysis for the turn-off switching transient

The impact of power module parasitic capacitance on the MOSFET turn-off switching transient is analyzed utilizing the double pulse test circuit and the corresponding switching wave-forms as presented in Fig. B.5a and B.7 respectively.

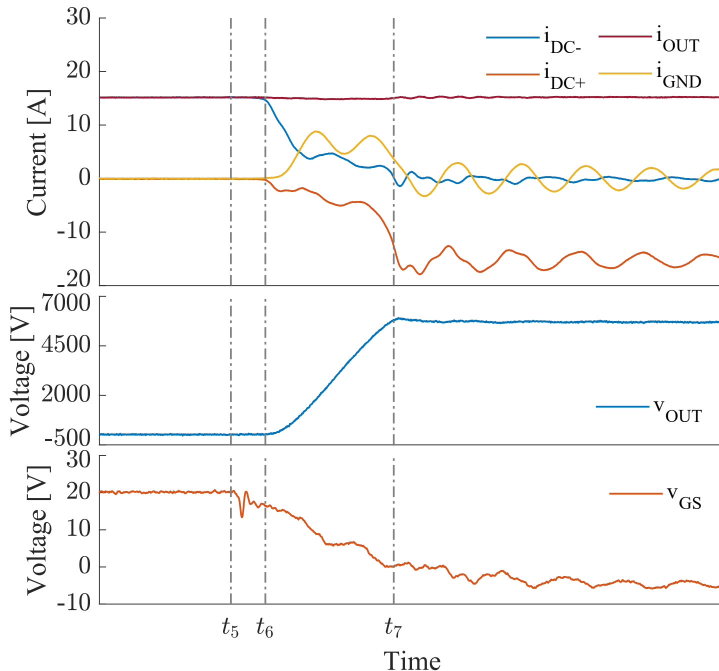


Fig. B.7: Experimental switching waveforms for the turn-off switching transient. (V_{DC} = 6 kV and i_{L} = 14 A)

At time t_5, the gate-source voltage starts to decrease from the turn-on gate voltage level. And at time t_6, the LS MOSFET enters into the saturation region from the linear region. The time instant t_6 is where the LS MOSFET gate-source voltage reaches the Miller-level. During the Miller plateau which occurs within time interval t_6–t_7, voltage at the output terminal of the half-bridge starts to increase. In time interval t_6–t_7, the current through LS MOSFET starts to decrease and MOSFET turns off when gate-source voltage is below the threshold voltage. This happens before time t_7 and the current measured at the DC- terminal even after the gate-source voltage of the LS MOSFET reaches below threshold voltage is due to the charging of the combined LS MOSFET and JBS diode output capacitance as beyond that point no current conducts through the MOSFET channel.

During t_6–t_7, the load inductor current comprises of the displacement cur-

rents that are charging and discharging the combined output capacitances of LS and HS MOSFET as well as JBS diode capacitance, displacement currents charging the module parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ that conducts through heatsink ground path. In contrast to the turn-on during the turn-off switching transient displacement currents charge the parasitic capacitances through the paths that does not conduct through MOSFET channel hence does not produce a joule heating.

B.5 Indirect methodology utilized to obtain module parasitic capacitance related displacement currents

The displacement current through the module parasitic capacitances can not be measured directly and therefore an indirect approach for obtaining the displacement current is required. In this section the methodology, which utilizes accessible half bridge current measurements $i_{\mathrm{DC+}}$, $i_{\mathrm{DC-}}$ and i_{OUT} to accurately obtain the module parasitic capacitance related displacement currents for both the turn-on and turn-off switching transition is introduced with supporting experimental validation.

At first, the turn-on switching transient is analysed considering the double pulse test circuit presented in Fig. B.5a. In this test circuit when heatsink is shorted to ground it is justifiable to consider that no displacement currents flow through capacitances $C_{\sigma+}$, $C_{\sigma\mathrm{GL}}$ and $C_{\sigma-}$ because these capacitances does not experience $\mathrm{d}v/\mathrm{d}t$ and ground current i_{GND} can be considered to be the total sum of the displacement currents through $C_{\sigma\mathrm{GH}}$ and $C_{\sigma\mathrm{OUT}}$ as presented in (B.1). In practice the stray inductance in the heatsink grounding path can produce a high frequency displacement currents through $C_{\sigma+}$, $C_{\sigma\mathrm{GL}}$ and $C_{\sigma-}$ due to voltage oscillation at heatsink node. However, for the grounded heatsink the voltage drop across the stray inductance due to the ground current is negligible in comparison to the voltage change across capacitance $C_{\sigma\mathrm{GH}}$ and $C_{\sigma\mathrm{OUT}}$.

$$i_{\mathrm{GND}} \approx i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} \tag{B.1}$$

Considering a fact that for the half-bridge power module accessible points for power loop current measurements are terminals DC+, OUT and DC-, magnitude of the displacement currents through inductor and module parasitic capacitance needs to be obtained indirectly utilizing three current measurements $i_{\mathrm{DC+}}$, $i_{\mathrm{DC-}}$ and i_{OUT} as presented in (B.2) and (B.4).

$$\begin{aligned} i_{\mathrm{C_L}} &= i_{\mathrm{OUT}} - i_{\mathrm{L}} \\ &\left[i_{\mathrm{L}} = i_{\mathrm{OUT(t_2)}}, v_{\mathrm{OUT}} = V_{\mathrm{DS(LS)}}\right] \\ &= C_{\mathrm{L}} \cdot \frac{\mathrm{d}}{\mathrm{d}(t_4 - t_3)}(V_{\mathrm{DC+}} - v_{\mathrm{OUT}}) \end{aligned} \tag{B.2}$$

Since almost no displacement currents flow through the module parasitic capacitance $C_{\sigma+}$, $C_{\sigma \mathrm{GL}}$ and $C_{\sigma-}$ the currents $i_{\mathrm{DC+}}$ and $i_{\mathrm{DC-}}$ can be considered almost equal to the current at the source terminal of the HS MOSFET and current at the drain terminal of the LS MOSFET respectively. For the analyzed test case, circuits external to the power module such as high side gate driver power supply and passive voltage probe utilized to measure the voltage at the power module output terminal also introduce capacitive couplings to ground, which results in displacement currents $i_{\mathrm{C_{AUX}}}$ that is conducted through the LS MOSFET during the turn-on $\mathrm{d}v_{\mathrm{OUT}}/\mathrm{d}t$. Considering this notion and applying Kirchhoff's current law (KCL) at the output terminal of the half-bridge $i_{\mathrm{DC-}}$ can be given as (B.3).

$$i_{\mathrm{DC-}} = i_{\mathrm{DC+}} + i_{\mathrm{OUT}} + i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} + i_{\mathrm{C_{AUX}}} \tag{B.3}$$

The displacement currents due to module parasitic capacitances can be approximated as,

$$i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} = i_{\mathrm{DC-}} - i_{\mathrm{DC+}} - i_{\mathrm{OUT}} - i_{\mathrm{C_{AUX}}} \tag{B.4}$$

and

$$i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} = (C_{\sigma\mathrm{OUT}} + C_{\sigma\mathrm{GH}}) \cdot \frac{\mathrm{d}}{\mathrm{d}(t_4 - t_3)} v_{\mathrm{OUT}} \tag{B.5}$$

Taking into account that the coupling capacitances due to the probe (≈ 3 pF) and gate driver power supply (4.8 pF) are significantly small compared to the module parasitic capacitances, the magnitudes of the displacement currents $i_{\mathrm{C_{AUX}}}$ are relatively smaller compared to the $i_{\mathrm{C_{\sigma OUT}}} + i_{\mathrm{C_{\sigma GH}}}$. Based on this consideration (B.4) can be further simplified into (B.6),

$$i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} \approx i_{\mathrm{DC-}} - i_{\mathrm{DC+}} - i_{\mathrm{OUT}} \tag{B.6}$$

The displacement currents due to inductor and module parasitic capacitances for the turn-off switching transient can be obtained using (B.7) and (B.8) similar to the explanation presented for the turn-on switching transient.

$$\begin{aligned} i_{\mathrm{C_L}} &= i_{\mathrm{OUT}} - i_{\mathrm{L}} \\ &\left[i_{\mathrm{L}} = i_{\mathrm{OUT(t_6)}}, v_{\mathrm{OUT}} = V_{\mathrm{DS(LS)}} \right] \\ &= C_{\mathrm{L}} \cdot \frac{\mathrm{d}}{\mathrm{d}(t_7 - t_6)} (V_{\mathrm{DC+}} - v_{\mathrm{OUT}}) \end{aligned} \tag{B.7}$$

and

$$\begin{aligned} i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} = &\quad i_{\mathrm{DC+}} - i_{\mathrm{DC-}} + i_{\mathrm{OUT}} - i_{\mathrm{C_{AUX}}} \\ = &\quad (C_{\sigma\mathrm{OUT}} + C_{\sigma\mathrm{GH}}) \cdot \tfrac{\mathrm{d}}{\mathrm{d}(t_7 - t_6)} v_{\mathrm{OUT}} \end{aligned} \tag{B.8}$$

Fig. B.8 and Fig. B.9, shows the comparison for the ground current measurements during turn-on and turn-off transients for the power modules A and

B respectively for a double pulse test at DC-link voltage of 6 kV and load current of 14 A. In Fig. B.8 and Fig. B.9, $i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}$ is the current obtained utilizing the three module current measurements $i_{\mathrm{DC+}}$, $i_{\mathrm{DC-}}$ and i_{OUT} based on (B.6). The current i_{GND} is the measured current through the wire that is shorting a heatsink to the ground and $i_{\mathrm{GND(sim)}}$ is the simulated ground current obtained by implementing the power module output terminal to heatsink impedance network (as per Fig. B.4) in LT Spice simulation. An image of

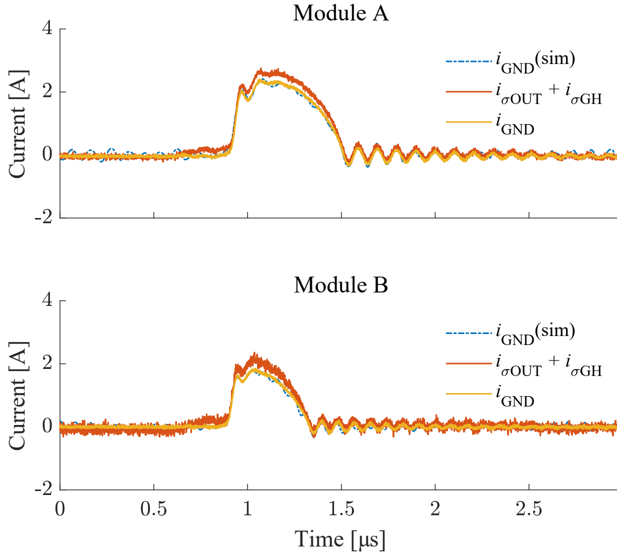


Fig. B.8: Experimentally measured/extracted and simulated ground currents during turn-on switching transient for power modules A and B in the case where heatsink is shorted to ground. (Test conditions $V_{\mathrm{DC}} = 6$ kV, $i_{\mathrm{L}} = 14$ A)

the LT Spice simulation implementation is shown in Fig. B.10, where input to the simulation is measured half-bridge output voltage. The values of module parasitic capacitances used are extracted from the ANSYS Q3D (see Table B.1). The parameters R_{GND}, L_{GND} and C_{GND} for the grounding impedance Z_{GND} in this case are obtained form the impedance analyzer as 5 Ω, 700 nH and ≈ 0 pF.

For both power modules, measured and simulated ground current show good agreement in terms of their amplitude and frequency response in case of turn-on as well as turn-off switching transients. However, the amplitude of the measured current i_{GND} differ slightly from the $i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}$. This difference is attributed to the common mode (CM) currents resulting from the capacitive couplings introduced by the circuits external to the power module such as the high side gate driver power supply (≈ 4.8 pF) and voltage probe (≈ 3 pF). As can be seen in Fig. B.8, in case of the turn-on switching transient the peak

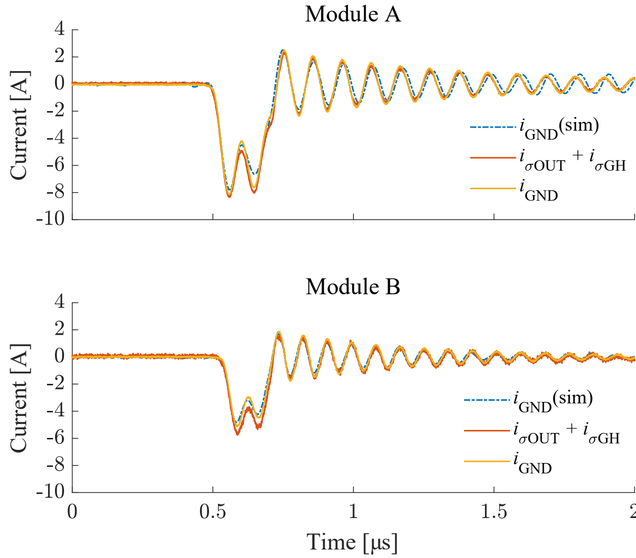


Fig. B.9: Experimentally measured/extracted and simulated ground currents during turn-off switching transient for power modules A and B in the case where heatsink is shorted to ground. (Test conditions V_{DC} = 6 kV, i_{L} = 14 A)

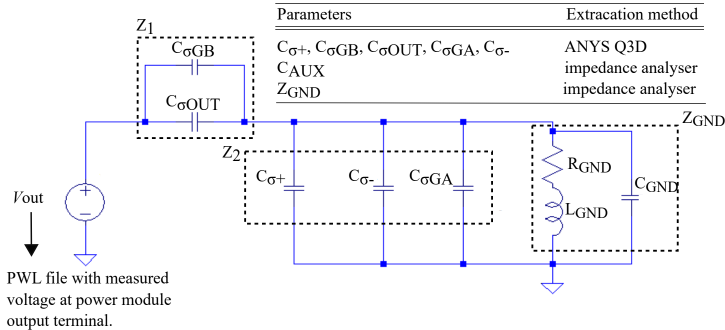


Fig. B.10: Image of the LT spice simulation implementation.

amplitude of the ground current i_{gnd} for module A is 2.4 A at the turn-on $\mathrm{d}v/\mathrm{d}t$ of 11.2 kV/μs in comparison to the 1.8 A for module B at the turn-on $\mathrm{d}v/\mathrm{d}t$ of 15.6 kV/μs. Similarly for the turn-off switching transient the absolute peak amplitude of the ground current for module A is 8 A at turn-off $\mathrm{d}v/\mathrm{d}t$ of 30.7 kV/μs in comparison to 5 A at turn-off $\mathrm{d}v/\mathrm{d}t$ of 39.3 kV/μs for module B.

The lower peak amplitude of the ground currents in module B in comparison to the module A even with high $\mathrm{d}v/\mathrm{d}t$, correlates with the reduced module parasitic capacitance for module B in comparison to module A. For the same

DC-link voltage, load current level and gate resistance the turn-on and turn-off $\mathrm{d}v/\mathrm{d}t$ is higher for the module B in comparison to module A. This is due to the influence of module parasitic capacitance $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ on the voltage rise and fall times as will be discussed in Section VI and VII.

To further corroborate, the charge $Q_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ for the module parasitic capacitances is calculated from double pulse test results using (B.9) and is then compared with the theoretically computed charge as in (B.10) utilizing the values of module parasitic capacitance $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ presented in Table. B.1.

$$Q_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}} = \int_x^y (i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}) \cdot \mathrm{d}t \tag{B.9}$$

(for turn on transient x = t_3 and y = t_4 and for turn-off transient x = t_6 and y = t_7.)

For the module parasitic capacitance, the stored charge increases linearly with the increase in DC-link voltage such that.

$$Q_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}(\text{Calculated} \quad \text{ANSYS}) = (C_{\sigma\mathrm{OUT}} + C_{\sigma\mathrm{GH}}) \cdot V_{\mathrm{DC}} \tag{B.10}$$

In addition to this charge Q_{GND} is also calculated by integrating the measured ground current i_{GND}. Fig. B.11 shows, the charge $Q_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$, Q_{GND} obtained using double pulse test results for DC-link voltage of up to 6 kV with load currents of 2 A and 14 A. The charge Q_{GND} show an excellent agreement with the theoretically computed charge. However, the charge $Q_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ show a values slightly higher compared to Q_{GND} (160 nC - 230 nC at 6 kV). This is attributed to the capacitive charge contributed by the circuits external to the power module such as the probe and gate driver power supply capacitance as discussed in previous Section. From the known value of the probe and gate driver parasitic capacitance of 3 pF and 4.8 pF respectively, the total charge due to the probe and gate driver capacitance is calculated to be 46.8 nC at DC-link voltage of 6 kV. With this charge added to the analytically obtained module parasitic capacitance charge measurement ($Q_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ - Calculated ANSYS), the maximum difference of 11.9 % and 16.9 % corresponding to the charge of 103 nC and 134 nC is left unaccounted for the modules A and B respectively. It is worth mentioning that this measurement discrepancy only gives approximately 10 pF to 15 pF of observable difference. This can in-fact be due to the undetected circuit stray capacitances, fine details of the current integration time window used to calculate the charge combined with the fine accuracy any measurements will have.

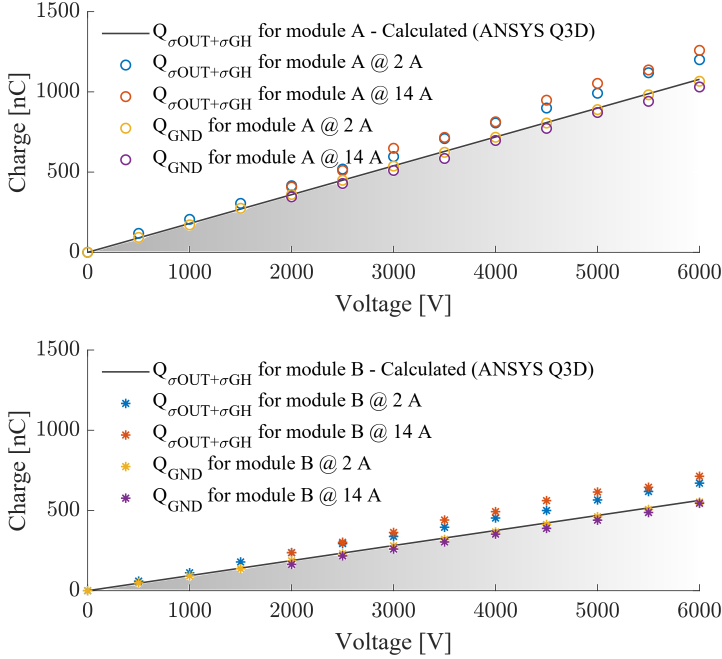


Fig. B.11: Comparison of the experimentally obtained and analytically calculated charge for the power module parasitic capacitance $C_{\sigma\mathrm{OUT}}$, $C_{\sigma\mathrm{GH}}$.

B.6 Analysis of impact of module parasitic capacitance impact on turn-on switching energy dissipation

To analyze the impact of the module parasitic capacitance on the overall turn-on switching losses, the turn-on switching energy dissipation E_{on} for the LS MOSFET is split into five segments. Each of these switching energy contribution is denoted as E_{on1}, E_{on2}, $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$, $E_{\sigma\mathrm{L}}$, $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ and is assigned as following. Segment E_{on1} is the switching energy dissipation during the turn-on switching transient time interval t_1–t_2 and is given by,

$$E_{\mathrm{on1}} = \int_{t1}^{t2} i_{\mathrm{DC}-} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{B.11}$$

Whereas, E_{on2} is the switching energy dissipation during time interval t_2–t_4 due to the constant load current magnitude i_{L} ($i_{\mathrm{L}} = i_{\mathrm{OUT}(t_2)}$) and is obtained

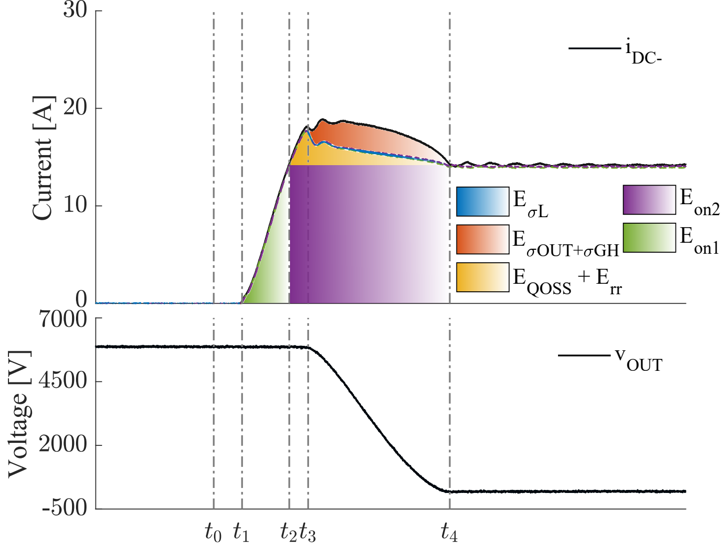


Fig. B.12: Illustration of split in turn-on switching energy dissipation. (Test conditions V_{DC} = 6 kV, i_{L} = 14 A))

from,

$$E_{\mathrm{on2}} = \int_{t2}^{t4} i_{\mathrm{L}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t$$
$$\left[i_{\mathrm{L}} = i_{\mathrm{OUT(t_2)}}\right] \tag{B.12}$$

The switching energy dissipation E_{QOSS} and E_{rr} due to the joule heating resulting from a charging of the HS MOSFET and diode output capacitances as well as diode reverse recovery charge is obtained from,

$$E_{\mathrm{QOSS}} + E_{\mathrm{rr}} = \int_{t2}^{t4} i_{\mathrm{DC+}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{B.13}$$

Switching energy dissipation due to the displacement currents charging the power module and inductor parasitic capacitance can be obtained, using the current magnitudes ($i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}$) and $i_{\mathrm{C_L}}$. (from (B.2) and (B.4)

$$E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}} = \int_{t3}^{t4} (i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}) \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{B.14}$$

$$E_{\sigma\mathrm{L}} = \int_{t3}^{t4} i_{\mathrm{C_L}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{B.15}$$

The total energy dissipation E_{on} that is measured utilizing the module currents and voltage measurements is expressed as,

$$
\begin{aligned}
E_{\text{on}} &= E_{\text{on1}} + E_{\text{on2}} + E_{\text{QOSS}} + E_{\text{rr}} + E_{\sigma\text{L}} + E_{\sigma\text{OUT}+\sigma\text{GH}} \\
&= \int_{t1}^{t4} i_{\text{DC}-} \cdot v_{\text{OUT}} \cdot \text{d}t
\end{aligned} \tag{B.16}
$$

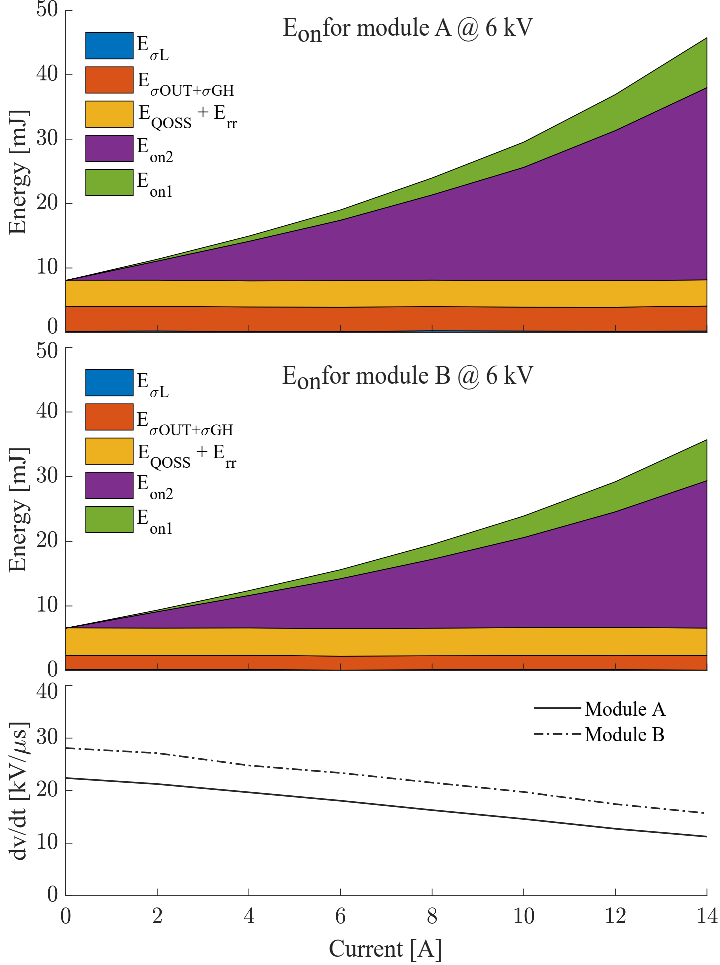


Fig. B.13: Comparison of the turn-on switching energy dissipation E_{on} and $\text{d}v/\text{d}t$ for modules A and B at DC-link voltage of 6 kV and load currents of 0 A – 14 A.

To draw a comparison between the two layouts and understand the impact of the module parasitic capacitance on the turn-on switching performance, the split of turn-on switching energy dissipation as illustrated in Fig. B.12 is

calculated using (B.11)-(B.16) from the double pulse test results obtained using the experimental test bench.

Fig. B.13 shows the split of turn-on switching energy dissipation for the DC-link voltage of 6 kV and load currents of 0 A – 14 A along with the turn-on $\mathrm{d}v/\mathrm{d}t$ comparison for modules A and B. As can be seen in Fig B.13, with increase in load current the tun-on $\mathrm{d}v/\mathrm{d}t$ decreases. This is because, the voltage magnitude at which the gate-source voltage reaches the plateau shifts towards the higher value with increasing magnitude of the load current. As the Miller plateau voltage shifts towards higher value, the voltage difference between the gate drive output voltage and gate-source voltage decreases. This results in the increased voltage fall time interval (t_3–t_4) due to lower magnitude of the gate current charging the reverse transfer capacitance C_{GD} and thus reducing the turn-on $\mathrm{d}v/\mathrm{d}t$.

Furthermore, for the same magnitude of the load current and similar experimental conditions the turn-on $\mathrm{d}v/\mathrm{d}t$, for the module A is lower than that of the module B, because module A in comparison to module B results in a higher plateau voltage during the Miller region as a result of the increased magnitude of the displacement current caused by the higher value of the module parasitic capacitance $C_{\sigma\mathrm{OUT}}$ an $C_{\sigma\mathrm{GH}}$. Meaning the voltage fall time t_3–t_4 corresponding to the turn-on switching transient increases for module A in comparison to module B, resulting in a lower turn-on $\mathrm{d}v/\mathrm{d}t$ for module A. At the DC-link voltage of 6 kV and load current of up to 14 A, the turn-on $\mathrm{d}v/\mathrm{d}t$ for the module A is identified to be approximately 28 % lower compared to module B.

From the turn-on switching energy separation presented in Fig.B.13, the dependency of the E_{on1} and E_{on2} on the load current is noticeable. Both, E_{on1} and E_{on2} increase with the load current. As discussed E_{on1} is the switching energy dissipation corresponding to the time interval t_1–t_2, where t_1 and t_2 relates to the time at which the gate-source voltage reaches the threshold and plateau voltage respectively. The increase in the E_{on1} for module A is attributed to the increase in time interval t_1–t_2 due to positive shift in the plateau voltage as discussed.

An indirect impact of the module parasitic capacitances on the turn-on switching performance can be clearly observed when comparing switching energy dissipation E_{on2} for both modules A and B. The higher magnitude of E_{on2} for module A in comparison to the module B is because of the lower turn-on $\mathrm{d}v/\mathrm{d}t$ or increased voltage fall time interval $t_3 - t_4$ for module A as explained in previous text. An increase in the voltage fall time interval will lead to increase in E_{on2}, since it is identified as the switching energy dissipation due to the constant load current magnitude over time interval t_2–t_4. For the DC-link voltage of 6 kV and drain current of 14 A, the E_{on2} for module A is 29.8 mJ which is approximately 7 mJ higher compared to module B. For a given DC-link voltage the E_{on2} increases with the load current, both because of the increase in load current magnitude as well as time interval t_3–t_4.

As can be noticed, that the capacitive losses $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$, $E_{\sigma\mathrm{L}}$ and E_{QCOSS} which occurs during time interval t_2–t_4 are load current independent. This is because the capacitive losses are not dependent on the time duration t_2–t_4, the change in the time interval will only result in the change in current magnitude with which the module and inductor parasitic capacitances are being charged or discharged, however the losses remain constant for a given DC-link voltage since the stored charge on the capacitor only changes with DC-link voltage.

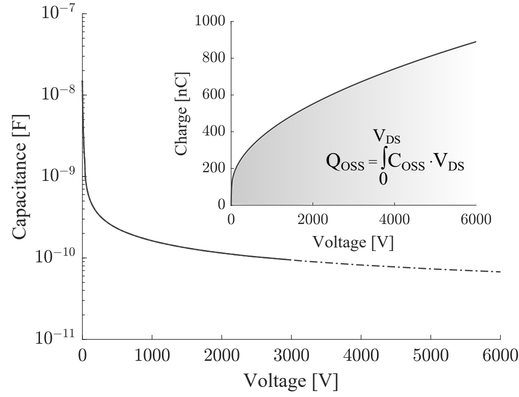
For both modules A and B the measured switching energy $E_{\mathrm{QCOSS}} + E_{\mathrm{rr}}$ based on (B.13), is almost constant and is within the range of 4 mJ to 4.2 mJ for the DC-link voltage of 6 kV and load currents of upto 14 A. To further strengthen the analysis and understanding for $E_{\mathrm{QCOSS}}+E_{\mathrm{rr}}$, a detail comparison is drawn between the double pulse experimental results and static measurements for 10 kV SiC MOSFET and JBS diode obtained using the curve tracer.

Fig. B.14a shows the output capacitance measurements as a function of voltage bias for a third generation 10 kV SiC MOSFET with an anti-parallel SiC JBS diode obtained utilizing the B1506 curve tracer. Due to the maximum output voltage limitation of 3 kV for the curve tracer, the capacitance for the voltage range of 3 kV – 5 kV is extrapolated using curve fitting. The charge $Q_{\mathrm{OSS(Static)}}$ is calculated from the curve tracer capacitance measurement data (see inset of Fig. B.14a) and its comparison with the output capacitance and reverse recovery charge measurements obtained from the double pulse test based on (B.17) is presented in Fig. B.14b for the DC-link voltage of up to 6 kV with the load currents of 2 A and 14 A.

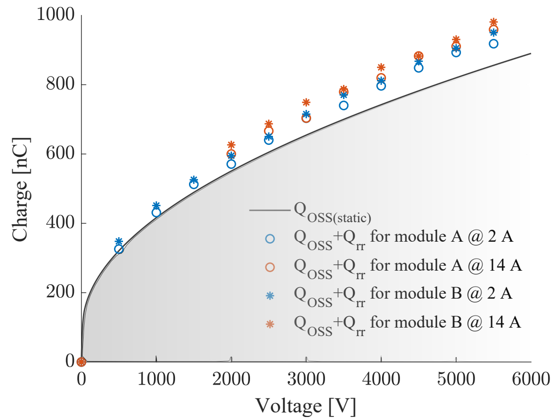
$$Q_{\mathrm{OSS}} + Q_{\mathrm{rr}} = \int_{t2}^{t4} i_{\mathrm{DC+}} \cdot \mathrm{d}t \tag{B.17}$$

The combined output capacitance and reverse recovery charge obtained from the double pulse test almost coincide with the static output capacitance charge measurements for both the higher (14 A) and lower (2 A) extreme of load currents, indicating almost no charge is present due to the diode reveres recovery. The charge $Q_{\mathrm{OSS(Static)}}$ increases with square root profile because of the non-linear behaviour of the MOSFET and JBS diode output capacitance as a function of bias voltage across it.

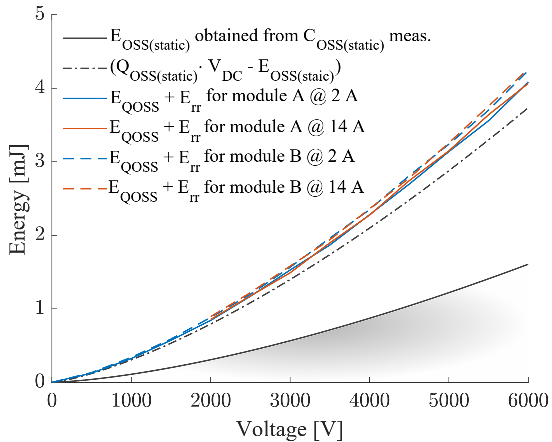
The measured $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ results for the DC-link voltage range of upto 6 kV and load currents of 2 A and 14 A are presented in Fig B.14c. The switching energy dissipation E_{QOSS}, which is due to the charging current of the complementary or in this case HS device output capacitance passing through the voltage potential of the LS MOSFET ($V_{\mathrm{OUT}} = V_{\mathrm{DC+}}$ - $V_{\mathrm{Q_H}}$). As a result the analytical prediction of the losses is $\int i_{\mathrm{OSS_H}} \cdot (V_{\mathrm{DC+}} - V_{\mathrm{Q_H}})$, which when simplified turns out to be $Q_{\mathrm{OSS}} \cdot \mathrm{V_{DC}} - E_{\mathrm{OSS}}$. Some may erroneously believe this energy to be E_{OSS} but note that this is note solely the energy stored in the output capacitance given by E_{OSS}. Therefore the switching energy dissipation $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ needs to be compared with $Q_{\mathrm{OSS(Static)}} \cdot \mathrm{V_{DC}} - E_{\mathrm{OSS(Static)}}$ and



(a)



(b)



(c)

Fig. B.14: (a) Output capacitance ($C_{\mathrm{OSS(Static)}}$) measurement for the 10 kV SiC MOSFETs and JBS diode obtained form B1506 curve tracer, (b) comparison of the output capacitance charge ($Q_{\mathrm{OSS(Static)}}$) with output capacitance as well as reverse recovery related charge obtained form the double pulse test setup (c) comparison of the stored energy on the output capacitance charge ($E_{\mathrm{OSS(Static)}}$) with switching energy dissipation $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ for power modules A and B.

not $E_{\mathrm{OSS(Static)}}$. It is interesting to see that the measured $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ almost coincide with the $Q_{\mathrm{OSS(Static)}} \cdot \mathrm{V_{DC}} - E_{\mathrm{OSS(Static)}}$ curve calculated from the static measurement leaving almost no room for the reverse recovery losses. This is in agreement with the dynamic charge measurements presented in Fig. B.14b justifying negligible contribution of the diode reverse recovery to the total turn-on switching energy dissipation for the full range of the load currents. This is expected due to the excellent reverse recovery performance of the SiC JBS diode [23].

In Fig. B.13, the clear difference is identified in the switching energy dissipation $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ for modules A and B. Switching energy dissipation $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ is approximately 3.8 mJ for module A in comparison to the 2.2 mJ for module B at the DC-link voltage of 6 kV. This accounts for about 8.3 % and 6.1 % of the measured total turn-on switching energy dissipation for modules A and B respectively. It should be noted that for a given DC-link voltage the percentage of $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ to the total turn-on energy dissipation will increase with reduced gate resistance, since with lower gate resistance the overall turn-on switching energy dissipation will reduce due to decrease in E_{on1} and E_{on2} as the voltage fall time shrinks but the capacitive losses $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ do not change. The switching energy dissipation $E_{\sigma\mathrm{L}}$ obtained using (B.15) is identical for modules A and B as expected and is measured to be in the range of 0.1 − 0.3 mJ for the DC-link voltage of 6 kV and load currents of upto 14 A. Relatively small magnitude of the $E_{\sigma\mathrm{L}}$ is due to the very low parasitic capacitance (≈ 12 pF) of the air core inductor.

From the total turn-on energy dissipation for the power module A and B presented in Fig. B.13, it can be seen that the difference in E_{on} for modules A and B is predominantly due to the variation in E_{on2} and $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ that result from the indirect and direct effect of module parasitic capacitances respectively. For the DC-link voltage of 6 kV and load current of 14 A the total turn-on switching energy dissipation for module A is 45.7 mJ which is about 22 % higher compared to 35.7 mJ for module B.

It is worth to note that the actual energy dissipation E^*_{on} for the turn-on switching transient is higher than the measured E_{on}. This is because the energy dissipation E_{OSS} as a result of the displacement current due to discharging of LS MOSFET and diode capacitance can not be measured at the DC– terminal of the power module since the current path is confined within the semiconductor itself. The common approach to this remedy is to add E_{OSS} obtained from the device datasheet or static measurement to the measured turn-on switching energy dissipation [22], expressed as (B.18).

$$E^*_{\mathrm{on}} = E_{\mathrm{on}} + E_{\mathrm{OSS(static)}} \tag{B.18}$$

B.7 Analysis of module parasitic capacitance impact on turn-off switching energy dissipation

The impact of module parasitic capacitance on the turn-off switching energy dissipation is discussed in this Section. Fig. B.15, shows the turn-off switching energy dissipation for the DC-link voltage of 6 kV and load currents of 2 A – 14 A along with the turn-off $\mathrm{d}v/\mathrm{d}t$ comparison for modules A and B. In contrast to the turn-on, for the turn-off switching transient the turn-off $\mathrm{d}v/\mathrm{d}t$ increases with the increase in load current. During the turn-off switching transient it is the load current magnitude that determines the charging and discharging rate of the combined LS and HS output capacitance of the MOSFET and JBS diode. Therefore it is the load current magnitude that predominantly determines the voltage rise time t_6–t_7 and the gate resistance has very little or no influence. Because of this the turn-off $\mathrm{d}v/\mathrm{d}t$ in Fig. B.15 show almost a linear dependence on the load current magnitude. It is important to notice that during the turn-off switching transient displacement currents due to the module parasitic capacitance does not conduct through the MOSFET channel hence does not result in Joule heating, however it decreases the turn-off $\mathrm{d}v/\mathrm{d}t$ at the half-bridge output terminal since module parasitic capacitance $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ appear in parallel to the LS MOSFET that acts as a snubber. This is the reason that the turn-off $\mathrm{d}v/\mathrm{d}t$ for module A is lower than that of the module B. For the case at hand, at the DC-link voltage of 6 kV and load current of 14 A the turn-off $\mathrm{d}v/\mathrm{d}t$ for module A and module B is identified to be 30.7 kV/μs and 39.3 kV/μs respectively. The turn-off switching energy dissipation for both power modules A and B is obtained using (B.19). The E_{off} for both power modules is approximately similar ranging within 1.6 mJ – 1.9 mJ for the DC-link voltage of 6 kV and load current range of 2 A – 14 A.

$$E_{\mathrm{off}} = \int_{t6}^{t7} i_{\mathrm{DC-}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{B.19}$$

The turn-off switching energy dissipation for the 10 kV SiC MOSFET is significantly small compared to the turn-on switching energy dissipation. Furthermore, the impact of module parasitic capacitance on the turn-on switching transient is more profound since during the turn-off switching transient displacement currents due to module or circuit parasitic does not produce a Joule heating because these currents does not commutate through the MOSFET. An important thing to notice here is that, most of the current measured at DC– terminal during the turn-off transient is due to the charging of the combined output capacitance of the LS MOSFET and JBS diode which does not produce a Joule heating. The portion of the drain current that flows through the MOSFET channel only contributes to the switching losses. Therefore, the actual switching energy

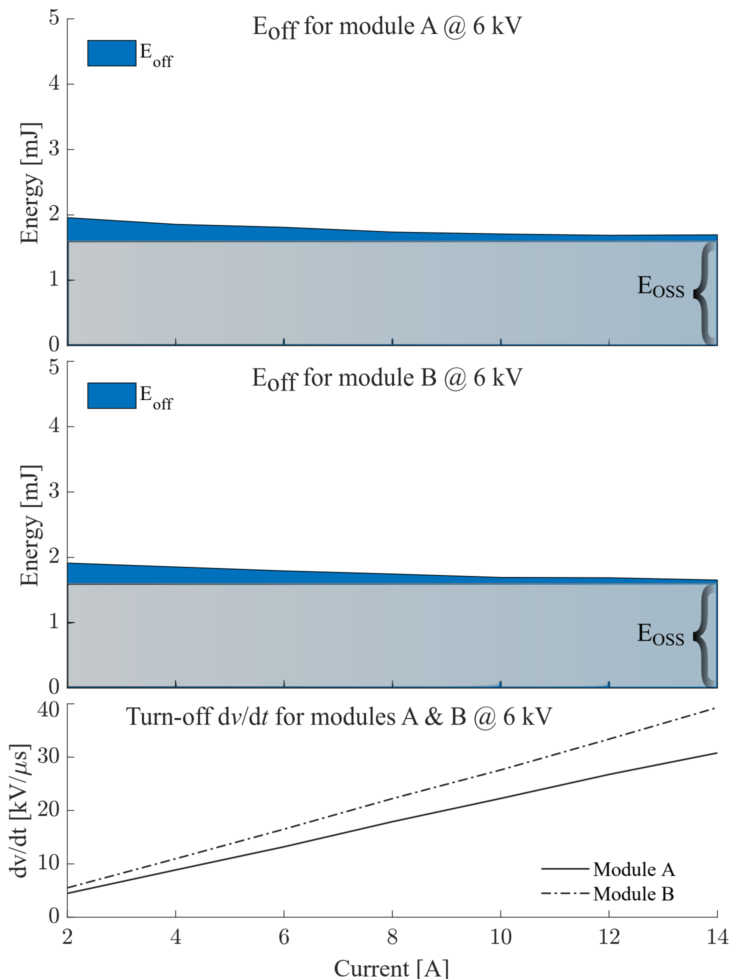


Fig. B.15: Comparison of the turn-off switching energy dissipation E_{off} and $v/\mathrm{d}t$ for modules A and B at DC-link voltage of 6 kV and load currents of 2 A – 14 A.

dissipation E^*_{off} during the turn-off transient can be obtained as presented in (B.20) [22].

$$E^*_{\text{off}} = E_{\text{off}} - E_{\text{OSS(Static)}} \tag{B.20}$$

The comparison of the $E_{\text{OSS(Static)}}$ which is obtained from the curve-tracer capacitance measurements to the measured E_{off} presented in Fig. B.15, reveal that the most of the portion of the measured turn-off switching energy dissipation contribute to the charging of the LS combined MOSFET and JBS diode output capacitance which is capacitive stored energy. This is also the reason that the turn-off losses for both modules almost are not influenced by the turn-off $\mathrm{d}v/\mathrm{d}t$

and are same for both modules A and B regardless of the turn-off dv/dt.

B.8 Conclusion

This paper provides an in-depth understanding about the impact of power module parasitic capacitances on the SiC MOSFET switching transients in respect to losses and analyzes it quantitatively. An indirect method to obtain the displacement currents due to module parasitic capacitances during the MOSFET turn-on and turn-off switching transients utilizing the accessible power module current measurements is proposed and validated experimentally. Moreover, a simple approach of utilizing the heatsink impedance network to predict the power module parasitic capacitace induced displacement currents was also presented which confirm the high accuracy of the modelled impedance network and extracted parasitic parameters used for the analysis. The experimental results presented in this paper show that the power module parasitic capacitances results in significant magnitudes of the displacement currents, which can lead to increased conducted EMI potentially resulting in difficulties with meeting EMC standards in practical applications. The key contribution of the paper lays in analysing the power module parasitic capacitance induced displacement current paths for the turn-on as well as tun-off switching transients and specifically revealing the impact of the module parasitic capacitances on the switching performance by dissecting the switching energy dissipation with great accuracy. This is showcased based on the experimental results obtained using the custom packaged 10 kV half bridge SiC MOSFET power modules with different DBC layouts. It is shown that the impact of module parasitic capacitance on the turn-on switching energy dissipation is two-fold and is more pronounced in comparison to the turn-off switching energy dissipation. A comparison of the the module parasitic capacitance related switching energy dissipation to the overall switching energy dissipation presented for the DC-link voltage of 6 kV and load current upto 14 A show the significance of the module parasitic capacitance on the switching performance. Failing to account for the module parasitic capacitances in design can lead to incorrect assignments as well as considerable error in estimating switching energy dissipation. Thus the module parasitic capacitance should no longer be neglected for a SiC MOSFET enabled power electronic converter foreseen to be utilized in medium voltage fast switching applications.

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Paper C

Switching Performance Assessment of 10 kV Half-Bridge SiC MOSFET Power Modules With and Without Anti-Parallel SiC JBS Diode

Dipen Narendra Dalal, Jannick Kjær Jørgensen, Hongbo Zhao, Szymon Bęczkowski, Michael Møller Bech, Christian Uhrenfeldt and Stig Munk-Nielsen

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The layout has been revised.

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Dipen Narendra Dalal, Jannick Kjær Jørgensen, Hongbo Zhao, Szymon Bęczkowski, Michael Møller Bech, Christian Uhrenfeldt and Stig Munk-Nielsen

Abstract

The impact of a SiC JBS diode on a SiC MOSFET switching transient is analysed utilizing the custom made medium voltage half-bridge SiC MOSFET power modules populated by, third generation 10 kV SiC MOSFETs with and without anti-parallel 10 kV SiC JBS diodes on an identical layout DBCs. The two power modules are tested in a double pulse test setup at 60% of their rated drain-source voltage of 6 kV and load currents of up to 14 A for a temperature range of 25°C – 100°C. The quantitative comparison and analysis on the impact of SiC JBS diode in terms of SiC MOSFET turn-on and turn-off switching energy dissipation is presented. With excellent reverse recovery performance of a 10 kV SiC MOSFET body diode over the tested load current and temperature range, the power module without an external 10 kV SiC JBS diode exhibit lower turn-on as well as turn-off switching energy dissipation. The impact on the turn-on switching energy is significant and two-fold as analysed from the proposed dissection of the switching energy dissipation. An increase in the turn-on switching energy dissipation for the module with SiC JBS diode is due to the increased energy dissipation in a SiC MOSFET as a result of the added stored capacitive charge on the SiC JBS diode junction capacitance and increase in the turn-on and turn-off switching times because of the reduced turn-on and turn-off $\mathrm{d}v/\mathrm{d}t$. From the power module switching performance point of view, power module without SiC JBS diode exhibit superior performance in comparison to power module with SiC JBS diode.

C.1 Introduction

The medium voltage third generation 10 kV Silicon Carbide (SiC) Metal Oxide Field Effect Transistor (MOSFET) with an on-state resistance of 350 mΩ was introduced by Wolfspeed in 2015 [1]. Since then various demonstrations and designs of the medium voltage (MV) power modules populated with 10 kV SiC MOSFET with or without junction barrier Schottky (JBS) diode dies have been reported by industry as well as academia [2]–[5].

For a 10 kV SiC MOSFET, at 25°C third quadrant operation with positive gate bias (v_{GS} ≥15 V) exhibit lower on-state voltage drop, whereas at 125°C

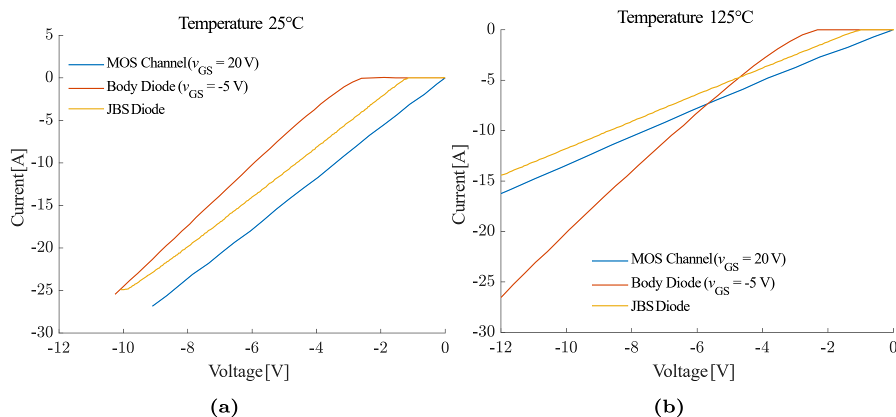


Fig. C.1: Static third quadrant IV characteristics for a 10 kV SiC MOSFET and forward IV characteristics for a 10 kV SiC JBS diode at temperatures of (a) 25°C and (b) 125 °C.

third quadrant operation with negative gate bias (v_{GS} ≤0 V) provides lower on-state voltage drop at increased current levels [6]. This can be observed from the IV characteristics obtained utilizing Tektronix B371A curve tracer, presented in Fig. C.1 for a 10 kV SiC MOSFET and JBS diode at 25°C and 125°C. Third quadrant IV characteristics with a positive gate bias for a 10 kV SiC MOSFET is almost symmetric to the first quadrant with no turn-on of the body diode observed up to drain-source voltage of 12 V, when MOSFET channel is on. Findings in [6] explain that for SiC MOSFETs in 3.3 kV or higher voltage class, where drift layer resistance constitutes larger portion of a MOSFET on-state resistance, the body diode turn-on voltage is higher than the P-N junction built in potential, when the MOSFET channel is turned on in a third quadrant operation. In power electronics AC-DC or DC-AC converters, in case of 10 kV SiC MOSFET if operated in a third quadrant with a positive gate bias during reverse conduction, the current will be conducted through the MOSFET channel or shared between the MOSFET channel and an external anti-parallel JBS diode, if present. This may lead to a lower conduction losses in third quadrant during the reverse conduction, as 10 kV SiC JBS diode exhibit parallel conduction path with almost similar on-state resistance as of 10 kV SiC MOSFET with a forward voltage of 1 V – 1.2 V. Except for the deadtime, where the current will be shared between body diode and JBS diode. Furthermore, at higher temperatures (125°C) the 10 kV SiC MOSFET body diode exhibit a lower on resistance than the 10 kV SiC JBS diode [7]. With above mentioned considerations, even though it may lower the reverse conduction losses in third quadrant operation, elimination of the SiC JBS diode is an attractive solution from the cost reduction and high power density point of view for the 10 kV power modules in the case where acceptable performance in terms of a reverse

recovery can be achieved with the SiC MOSFET body diode. This requires that, an assessment from a switching performance point of view be made for the 10 kV SiC modules with and without anti-parallel SiC JBS diode.

In [8], extensive characterization of the 10 kV, 100 A half-bridge SiC MOSFET power module without an anti-parallel SiC JBS diode is presented. Characterization in terms of switching energy dissipation for the third generation SiC MOSFET with anti-parallel JBS diode in a half-bridge configuration is reported in [2]. In [9], the reverse recovery performance of the SiC MOSFET body diode and anti-parallel JBS diode is investigated individually with comparing the peak reverse recovery current in the double pulse or clamped inductive switching test, which is different from a half-bridge configuration. This paper aims at analysing the impact of a SiC JBS diode on a SiC MOSFET switching characteristics and its impact on the switching energy dissipation, where the total switching energy is dissected to assess the output junction capacitance and reverse recovery related losses for the modules with and without anti-parallel SiC JBS diode. The analysis presented assesses need of an external anti-parallel JBS diode for 10 kV SiC half-bridge power modules from a switching performance point of view. The impact of a SiC JBS diode on a SiC MOSFET switching performance is investigated in [10], however the analysis is limited to the drain-source voltage of 3 kV which is 30% of a 10 kV SiC MOSFETs rated voltage. The stored charge or the energy on the output capacitance of a SiC MOSFET and JBS diode is significantly different at voltage bias of 6 kV compared to 3 kV as the energy stored on the capacitor increases with voltage squared. Furthermore, [10] concludes that, the impact of an external SiC JBS diode on the turn-on switching transient and energy dissipation is insignificant, which is contrary to the fact that the energy dissipation due to the Joule heating in the SiC MOSFET during the turn-on switching transient as a result of charging of the complementary device output capacitance is considerably higher for the power module with anti-parallel SiC JBS diode due to increased combined output capacitance as presented in this paper. In addition to this, the inclusion of an anti-parallel JBS diode results in an increase in voltage rise and fall times due to the reduced turn-on as well as turn-off $\mathrm{d}v/\mathrm{d}t$ and thereby increased switching energy dissipation in SiC MOSFET.

This paper presents, comparative evaluation on the impact of a SiC JBS diode on the switching transient as well as switching energy dissipation by dissecting the total switching energy dissipation into different segments as proposed in [11]. To eliminate the impact of the power module parasitic capacitance on a SiC MOSFET switching transient and energy dissipation [11], power modules with identical DBC layouts are utilized. The paper is organized as follows, first the device under tests - 10 kV half-bridge SiC MOSFET power modules with and without JBS diode are introduced in Section II. In section III, the double pulse experimental test setup is described in detail. In section IV, the impact of a SiC JBS diode on SiC MOSFET switching transient is discussed

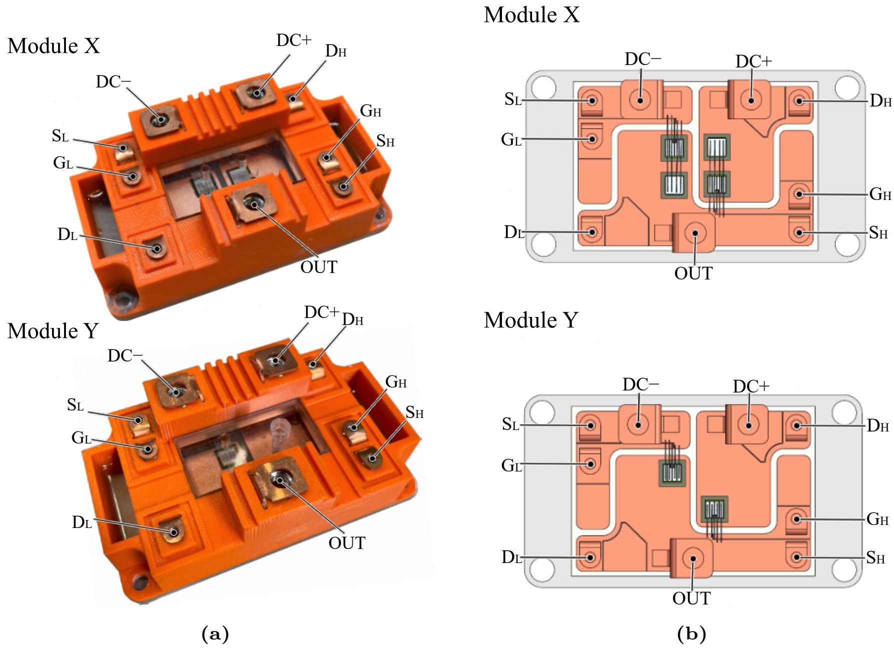


Fig. C.2: (a) Picture and (b) Solidworks rendering for the 10 kV half-bridge SiC MOSFET power modules with (termed as X) and without (termed as Y) anti-parallel SiC JBS diode.

in detail based on the experimental waveforms obtained from the double pulse test bench. With the proposed switching energy dissection, the two-fold impact of an external SiC JBS diode in terms of added switching energy dissipation in a SiC MOSFET is analysed and quantitative comparison is drawn in section V for the two power modules with conclusion presented in section VI.

C.2 Device under test - 10 kV half-bridge SiC MOSFET power module

The image of custom made single die 10 kV half-bridge SiC MOSFET power modules with and without anti-parallel SiC JBS diode referred here as modules X and Y are shown in Fig. C.2a. The power modules are populated with third generation 10 kV SiC MOSFET and JBS diode dies [1], on the 0.63 mm Aluminium Nitride (AlN) DBC soldered on a 3 mm AlSiC baseplate [4]. The DBC layout is identical for both power modules as can be seen from the top view of the 3D CAD model shown in Fig. C.2b. The AlN ceramic substrate between two copper layers on the either side of a DBC introduces capacitive couplings between the top copper layer of the DBC and the baseplate. The power module

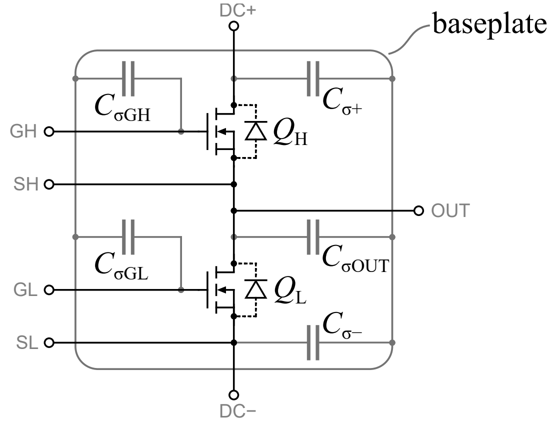


Fig. C.3: Schematic representation of the distribution of the parasitic capacitances in a half bridge power module. [11]

parasitic capacitance for the half-bridge power module is extracted from the ANSYS Q3D [12] with the permittivity of the materials specified in the datasheet supplied by the manufacturer are presented in Table C.1.

Table C.1: Values of parasitic capacitances obtained from ANSYS Q3D for the 10 kV half-bridge SiC MOSFET power module. (All in [pF])

$C_{\sigma +}$	$C_{\sigma \mathrm{GH}}$	$C_{\sigma \mathrm{OUT}}$	$C_{\sigma \mathrm{GL}}$	$C_{\sigma -}$
108	20.5	159.2	23.5	47.5

As presented in Fig.C.3, $C_{\sigma +}$ and $C_{\sigma -}$ are the distributed capacitance between the DBC copper planes DC+, DC- and the baseplate. Similarly, $C_{\sigma \mathrm{GH}}$, $C_{\sigma \mathrm{GL}}$ and $C_{\sigma \mathrm{OUT}}$ are the distributed parasitic capacitaces between the DBC and baseplate due to the capacitive couplings from the high side gate, low side gate and output DBC copper planes, respectively. Depending on an impedance network between the heatsink on which power module is mounted, some of these parasitic capacitances get charged and discharged during the switching transient [13], resulting in a common mode (CM) current. In the case where heatsink is shorted to ground, the parasitic capacitances $C_{\sigma \mathrm{OUT}}$ and $C_{\sigma \mathrm{GH}}$ experience the $\mathrm{d}v/\mathrm{d}t$ during a switching transient, which introduces the displacement currents. The impact of module parasitic capacitance in terms of change in switching dynamics and added switching energy dissipation of the SiC MOSFET is significant and can not be neglected in case of the MV power modules utilizing SiC devices [11]. In the present case study, power modules with an identical DBC layout are utilized. With this approach and considering that both of the power modules in terms of their switching transients are investigated under the identical test conditions, the difference in the SiC MOSFET switching

characteristics and switching energy dissipation between the two power modules can be predominantly assigned to the SiC JBS diode and in part due to the die parameter variance.

C.3 Experimental test setup

The two variants of 10 kV half bridge power modules with and without SiC JBS diode are mounted on a temperature controlled heat plate. The DC-link is set up by utilizing two 50 μF, 5 kV rated polypropylene capacitors connected in parallel with a low inductance busbar connection. The heatplate is grounded by connecting a short wire to the DC- connection of the busbar. High voltage 10 kV power supply (XR 10000-0.2/415/+HS+LXI) from Magna Power is used to supply the DC-link. A 47 mH air core inductor with very low ($\approx$ 12 pF) parallel parasitic capacitance is utilized as the load inductor. The low side (LS) SiC MOSFET is utilized as the DUT. A low coupling capacitance ($\leq$ 2.6 pF) isolated gate driver with gate turn-on and turn-off gate voltage of +20V/-5V and external gate resistance of 20 Ω is used to drive the SiC MOSFETs [14]. The schematic and image of the test setup is shown in Fig. C.4. The electrical connection between the power module and DC-link busbar is provided by utilizing a short-wire for insertion of Pearson current monitors. High bandwidth (BW) Pearson current monitors 2878 (BW = 70 MHz) [15] and 2877 (BW = 200 MHz) [16] with usable rise time of 2 ns and 4 ns are utilized to measure the currents $i_{\mathrm{DC+}}$, $i_{\mathrm{DC-}}$, i_{OUT} and i_{GND} at the half-bridge module DC+, DC-, Output terminals and heat plate ground connection, respectively. The half-bridge output voltage and the LS MOSFET gate-source voltage are measured using a high voltage PPE 20 kV passive probe [17] (BW = 100 MHz, probe input resistance = 100 MΩ, input capacitance = $\leq$ 3 pF) and an optically isolated differential probe HVFO103 [17] (BW = 150 MHz), respectively. The measurements are performed with a LeCroy WaveRunner 8058HD 500 MHz oscilloscope [18]. The two power modules are tested in a double pulse test setup at a DC-link voltage of 6 kV, load currents of up to 14 A for 25°C – 100°C.

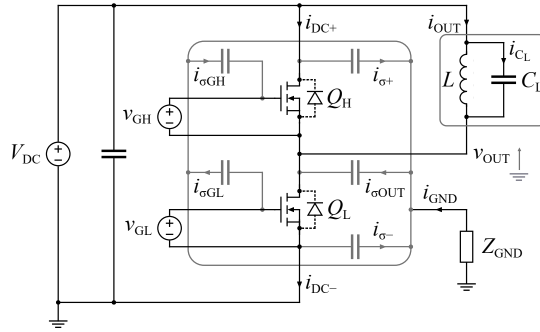
C.4 Impact of the anti-parallel SiC JBS diode on the SiC MOSFET switching transient

The impact of an anti-parallel SiC JBS diode on SiC MOSFET turn-on and turn-off switching transient is analysed utilizing the experimental results obtained from a double pulse test for the two power modules at the DC-link voltage of 6 kV, load current of 14 A and temperature of 25°C.

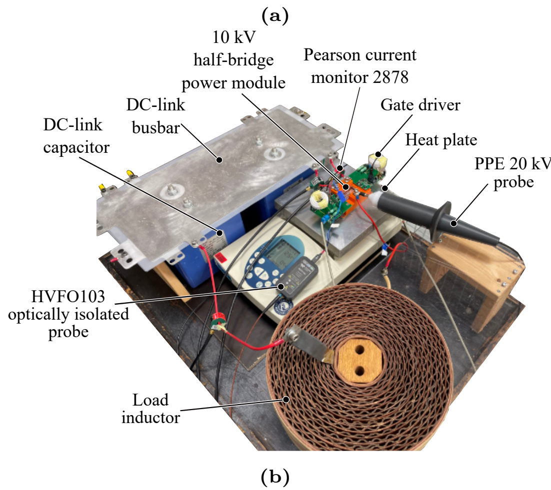
C.4.1 Analysis of the turn-on switching transient

For comparison, the turn-on switching transient for power modules with (X) and without (Y) SiC JBS diode at a DC-link voltage of 6 kV and load current of 14 A at 25°C is shown in Fig. C.5. The experimental waveforms and their time instants in Fig. C.5, for modules X and Y are differentiated using dashed and solid line, respectively. The comparative analysis of a turn-on switching transient for both half-bridge power modules is presented for the time interval t_0–t_4.

- t_0–t_1: For both power modules, turn-on gate command is applied at time t_0. The gate-voltage starts to increase from negative gate-bias at time t_0 and reaches the gate-source threshold voltage at time t_1, where LS MOSFET channel starts conducting the current. The small difference in time interval t_0–t_1, for two power modules can be due to the slight



(a)



(b)

Fig. C.4: (a) Schematic and (b) picture of the double pulse test bench.

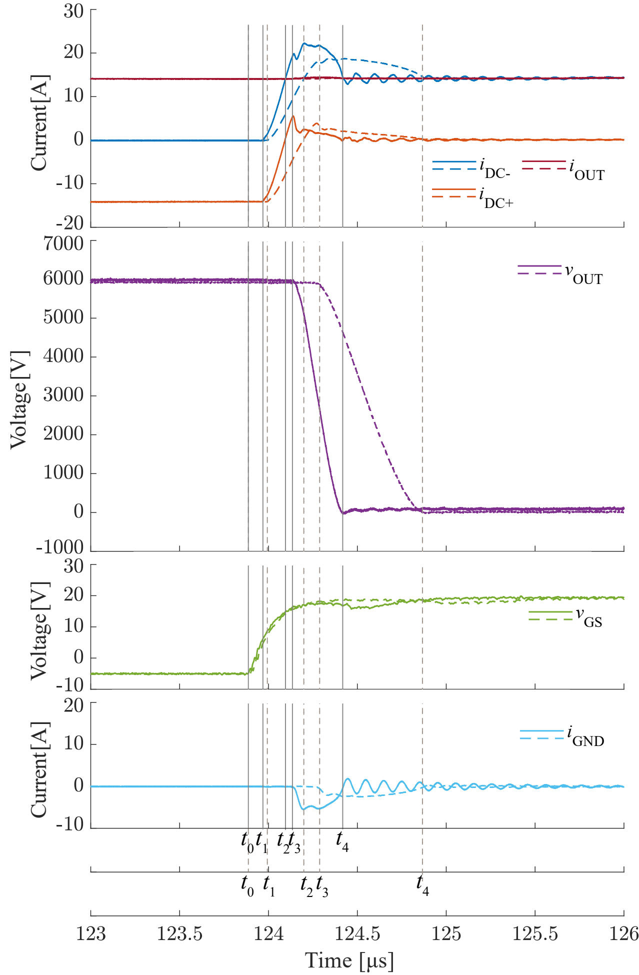


Fig. C.5: Experimental switching waveforms for the turn-on switching transient. – solid line for module without JBS diode (Y) and dashed line for module with JBS diode (X) (V_{DC} = 6 kV and i_{L} = 14 A at 25°C)

mismatch in the MOSFET gate-source threshold voltage.

- t_1–t_2: During this time interval the load current commutates from the high side (HS) diode to the low side (LS) MOSFET. At time instant t_2, the current through the LS MOSFET reaches load current level and the gate-source voltage corresponding to the time instant t_2 is termed as Miller level. The increased duration for the time interval t_1–t_2, for the power modules with JBS diode is identified due to the device parameter variance and difference in the reverse recovery characteristics of the bipolar

intrinsic SiC PiN diode and unipolar SiC JBS diode, which results in a lower $\mathrm{d}i/\mathrm{d}t$ in case of the power module with the JBS diode compared to the power module without JBS diode.

- $t_2 - t_4$: The time interval t_2–t_4 termed as Miller region. At time instant t_2, the load current is completely commutated from the HS diode to the LS MOSFET. However, due to the diode reverse recovery, the current through the LS MOSFET increases beyond the load current level and reaches the peak value at time instant t_3 and reaches back to the load current level at time instant t_4. The voltage change at the output terminal of the half-bridge module occurs during the time interval t_3–t_4. During time interval t_3–t_4, in addition to the load current LS MOSFET conducts the current due to the charging and discharging of the power device, load inductor and power module parasitic capacitances.

  For power module Y, the output capacitance of the MOSFET and for power module X the combined output capacitance of the HS MOSFET and JBS diode gets charged though the LS MOSFET and produces Joule heating. Also, the inductor parasitic capacitance C_{L} as well as the power module parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$, gets charged and discharged through a LS MOSFET with the displacement currents $i_{\mathrm{C_L}}$, $i_{\sigma\mathrm{OUT}}$ and $i_{\sigma\mathrm{GH}}$ respectively, which also produces a Joule heating that adds up to the turn-on switching energy dissipation. As can be seen from comparing LS MOSFET current (half-bridge current $i_{\mathrm{DC\text{-}}}$) to the diode reverse recovery current (half-bridge current $i_{\mathrm{DC+}}$) waveform trajectory during the time interval t_3–t_4, the increased current magnitude for the LS MOSFET is predominantly due to the discharging of the power module parasitic capacitance, whereas the impact of the load inductor parasitic capacitance is significantly small owing to its small magnitude. In the present case study, where the heatsink is shorted to the ground the magnitude and frequency response of the power module parasitic capacitance $i_{\sigma\mathrm{OUT}}$ and $i_{\sigma\mathrm{GH}}$ is almost equal to the measured i_{GND} shown in Fig. C.6 and experimentally validated in [11]. The HS gate driver and the passive probe utilized to measure the half-bridge output voltage also introduces the capacitive coupling and thus displacement currents during the voltage change at half-bridge output terminal. However, the magnitude of the gate driver isolation capacitance ($\leq$3.6 pF) and probe capacitance ($\approx$ 3 pF) is significantly small compared to the power module parasitic capacitance. With this consideration the power module parasitic capacitance related displacement current during the turn-on switching transient can be obtained as shown in [19] as,

$$i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} = i_{\mathrm{DC-}} - i_{\mathrm{DC+}} - i_{\mathrm{OUT}} \tag{C.1}$$

and

$$i_{\sigma\text{OUT}} + i_{\sigma\text{GH}} = (C_{\sigma\text{OUT}} + C_{\sigma\text{GH}}) \cdot \frac{\mathrm{d}}{\mathrm{d}(t_4 - t_3)} v_{\text{OUT}} \tag{C.2}$$

Inductor parasitic capacitance related displacement current can be obtained as,

$$\begin{aligned} i_{\mathrm{C_L}} &= i_{\text{OUT}} - i_{\text{L}} \\ &\left[i_{\text{L}} = i_{\text{OUT(t_2)}}, v_{\text{OUT}} = V_{\text{DS(LS)}}\right] \\ &= C_{\text{L}} \cdot \frac{\mathrm{d}}{\mathrm{d}(t_4 - t_3)} (V_{\text{DC+}} - v_{\text{OUT}}) \end{aligned} \tag{C.3}$$

The increased peak magnitude of the ground current for the module without JBS diode in comparison to the module with JBS diode is due to the increased $\mathrm{d}v/\mathrm{d}t$.

In addition to this, for the power modules Y, the current due to the discharging of the LS MOSFET output capacitance and for power module X the current due to discharging of the combined LS MOSFET and diode capacitance conducts through the LS MOSFET resulting in a Joule heating. However, since this current path is confined within the LS MOSFET it can not be measured at the DC- terminal of the half-bridge power module [19]. The added capacitance due to an external JBS diode would result in an increased current through the LS MOSFET for the power module X due to the added diode junction capacitance in parallel (which can not be measured at DC- terminal since current path is confined within the MOSFET). The increased channel current together with a slight variance in the die parameter results in an increased gate-source voltage during the time interval t_3–t_4 for the module X, thus reducing the voltage difference between the turn-on gate bias voltage and gate source voltage leading to a reduced magnitude of the gate current charging the MOSFET gate-drain capacitance, thus lowering the turn-on $\mathrm{d}v/\mathrm{d}t$.

C.4.2 Analysis of the turn-off switching transient

For comparison, the turn-off switching transient for power modules with (X) and without (Y) SiC JBS diode at the DC-link voltage of 6 kV and load current of 14 A at 25°C is shown in Fig. C.6. The experimental waveforms and their time instants in Fig. C.6, for modules X and Y are differentiated using solid and dashed line respectively. The comparative analysis of the turn-off switching transient for both half-bridge power modules is presented for the time interval t_5–t_7.

- t_5–t_6: For both power modules, the turn-off gate command is applied at time instant t_5. From time t_5, the LS MOSFET gate-source voltage starts

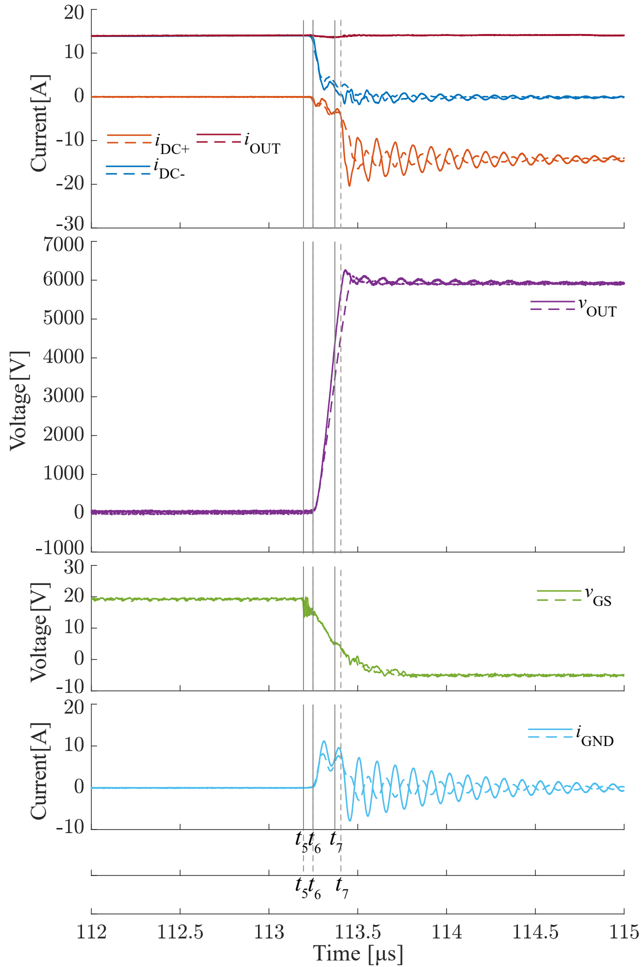


Fig. C.6: Experimental switching waveforms for the turn-off switching transient. – solid line for module without JBS diode (Y) and dashed line for module with JBS diode (X) ($V_{\mathrm{DC}} = 6$ kV and $i_{\mathrm{L}} = 14$ A at 25°C)

to decrease from the turn-on gate bias to the Miller level corresponding to the load current magnitude at time instant t_6. As can be seen from Fig. C.6, no observable difference is identified in time duration t_5–t_6, for the modules with and without SiC JBS diode.

- t_6–t_7: At time instant t_6, the LS MOSFET enters into the saturation region and the voltage at the output terminal of the half-bridge starts to increase and the current through the LS MOSFET starts to decrease. The current measured at the DC- terminal of the half-bridge module also consist the charging current of the LS power device output capacitances

and therefore the measured current after the LS MOSFET gate-source voltage has reached below its threshold voltage is solely due to the charging of the LS power device output capacitance and does not result in Joule heating.

During time interval t_6–t_7, the load current splits in (i) to charge LS MOSFET output capacitance in the case of module X and the combined LS MOSFET and JBS diode output capacitance in the case of module Y, (ii) to discharge the HS MOSFET output capacitance for the module X and the combined LS MOSFET and diode output capacitance for module Y. In addition to this, the load inductor and power module parasitic capacitances also get discharged and charged by the load current. For power module X, the interval time interval t_6–t_7 increases and thus the turn-off $\mathrm{d}v/\mathrm{d}t$ decreases, due to the additional parasitic capacitance introduced by the SiC JBS diode in parallel to the LS MOSFET that acts as a snubber.

C.5 Comparison of the switching energy dissipation for the module with and without anti-parallel SiC JBS diode

The comparative analysis for the turn-on and turn-off switching energy dissipation for power modules with (X) and without JBS diode (Y) is analysed utilizing the current and voltage measurements from the double pulse test setup.

C.5.1 Analysis of the turn-on switching energy dissipation

To analyse the impact of the SiC JBS diode on the SiC MOSFET on the overall turn-on switching energy dissipation, a dissection of switching energy is proposed as documented in [11]. The total turn-on switching energy dissipation is split into five different segments namely E_{on1}, E_{on2}, $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$, $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ and $E_{\sigma\mathrm{L}}$. Each of these individual segments is graphically illustrated in Fig. C.7 and defined as follows. The segment E_{on1} is defined as a switching energy dissipation within time interval t_1–t_2 as,

$$E_{\mathrm{on1}} = \int_{t1}^{t2} i_{\mathrm{DC-}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{C.4}$$

Whereas, the segment E_{on2} is defined as a switching energy dissipation due to constant load current magnitude i_{L} ($i_{\mathrm{L}} = i_{\mathrm{OUT}(t_2)}$) within the time interval

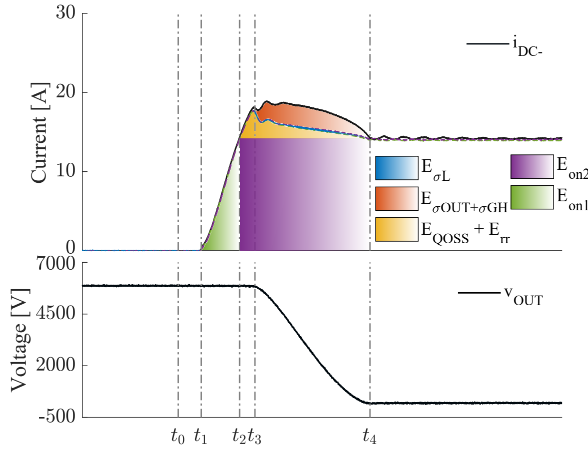


Fig. C.7: Illustration of split in turn-on switching energy dissipation. (Test conditions V_{DC} = 6 kV, i_{L} = 14 A))

t_2–t_4 as,

$$E_{\mathrm{on2}} = \int_{t2}^{t4} i_{\mathrm{L}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \quad \left[i_{\mathrm{L}} = i_{\mathrm{OUT}(t_2)}\right] \tag{C.5}$$

The segment E_{QOSS} and E_{rr} defined as a switching energy dissipation due to the Joule heating resulting from charging of the HS power device output capacitance and the reverse recovery charge within the time interval t_2–t_4 as,

$$E_{\mathrm{QOSS}} + E_{\mathrm{rr}} = \int_{t2}^{t4} i_{\mathrm{DC+}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{C.6}$$

The segments $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ and $E_{\sigma\mathrm{L}}$, which are defined as the switching energy dissipation due to the discharging and charging of the power module and inductor parasitic capacitance due to displacement currents during time interval t_3–t_4 as,

$$E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}} = \int_{t3}^{t4} (i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}) \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{C.7}$$

$$E_{\sigma\mathrm{L}} = \int_{t3}^{t4} i_{\mathrm{C_L}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{C.8}$$

In the equations above the currents $(i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}})$ and $i_{\mathrm{C_L}}$ from (C.3) and (C.1) respectively.

The turn-on switching energy dissipation E_{on} is the total sum of five segment as defined as,

$$\begin{aligned} E_{\text{on}} &= E_{\text{on1}} + E_{\text{on2}} + E_{\text{QOSS}} + E_{\text{rr}} + E_{\sigma\text{L}} + E_{\sigma\text{OUT}+\sigma\text{GH}} \\ &= \int_{t1}^{t4} i_{\text{DC}-} \cdot v_{\text{OUT}} \cdot \text{d}t \end{aligned} \tag{C.9}$$

The comparison of a turn-on switching energy dissipation and switching energy dissection, together with a turn-on $\text{d}v/\text{d}t$ for power modules X and Y at the DC-link voltage of 6 kV, load currents of up to 14 A at temperatures of 25°C and 100°C is shown in Fig. C.8 and Fig. C.9, respectively. As can be seen from Fig. C.8 and C.9, the turn-on $\text{d}v/\text{d}t$ decreases with the increase in the load current magnitude. This is because the voltage magnitude at which the gate-source voltage reaches the Miller level increases with increasing load current magnitude. For the similar experimental conditions, the turn-on $\text{d}v/\text{d}t$ for the power module X is lower than that of the power module Y. This is attributed to the positive shift in the gate-source plateau voltage for module X in comparison to module Y due to the added parallel capacitance from the external SiC JBS diode and in part due to the die parameter variance. Whereas, the turn-on $\text{d}v/\text{d}t$ for the power modules X and Y at 100 °C increases in comparison to 25°C which is attributed to the decrease in the gate-source threshold voltage and the Miller level [20]. The turn-on $\text{d}v/\text{d}t$ for module X at the DC-link voltage of 6 kV and load current of 14 A at 25°C and 100°C, is 11.8 kV/µs and 24.9 kV/µs respectively, which is 54.4% and 36.5% lower compared to module Y.

As can be seen from C.8 and C.9, the switching energy dissipation E_{on1} and E_{on2} increase with the increase in the load current magnitude.

E_{on1}, which is defined as the switching energy dissipation occurring within time interval t_1–t_2 is slightly higher for module X in comparison to module Y. This is due to the reduced $\text{d}i/\text{d}t$ resulting in an increased time interval t_1–t_2 for module X in comparison to module Y. The reduced $\text{d}i/\text{d}t$ for module X is attributed to the die parameter variance and the difference in the diode recovery characteristics for the module with and without diode. The E_{on1} at the DC-link voltage of 6 kV and load current of 14 A at 25°C for modules X and Y is 7.3 mJ and 4.1 mJ, respectively. Where as at 100°C, due to decrease in the gate-source threshold and Miller voltage the E_{on1} for module X and Y is identified to be reduced to 4.1 mJ and 2.8 mJ respectively.

The indirect impact of the external SiC JBS diode can be identified when comparing switching energy dissipation E_{on2} for the power modules X and Y. The increase in E_{on2} for the module X can be identified due to the increase in the gate-source voltage magnitude for module X in comparison to module Y during the Miller region (can be seen in Fig. C.5) attributed to the added parallel junction capacitance and in part due to the die parameter variance, which results in the reduced turn-on $\text{d}v/\text{d}t$. The E_{on2} at the DC-link voltage of

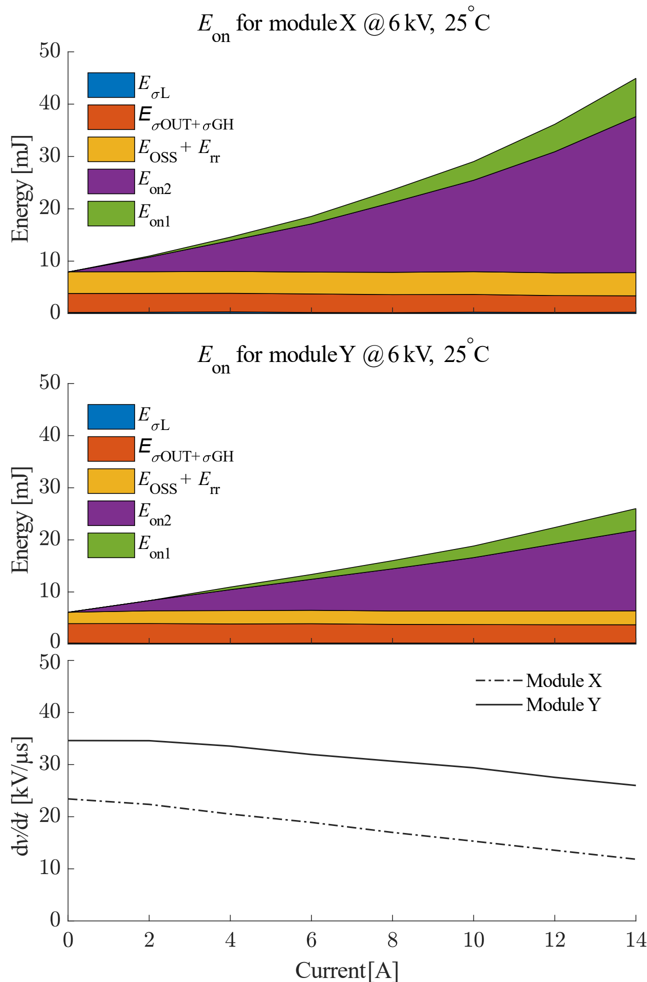


Fig. C.8: Comparison of the turn-on switching energy dissipation E_{on} and $\mathrm{d}v/\mathrm{d}t$ for modules X and Y at the DC-link voltage of 6 kV, load currents of 0 A – 14 A and temperature of 25°C.

6 kV and load current of 14 A at 25°C for module X and Y is 29.8 mJ and 15.4 mJ, which is almost 48% increase in comparison to module Y. With increase in temperature at 100°C, the E_{on2} for module X and Y is identified to be 16.8 mJ and 11.3 mJ, respectively for the similar DC-link voltage and load current level. The decrease in E_{on2} at alleviated temperature can be associated with the reduced turn-on $\mathrm{d}v/\mathrm{d}t$ due to decrease in the gate-source plateau voltage.

The switching energy dissipation $E_{\text{OSS}} + E_{\text{rr}}$, due to the Joule heating resulting from the charging of HS power device output capacitance and the diode reverse recovery charge show very small increase with the increase in the

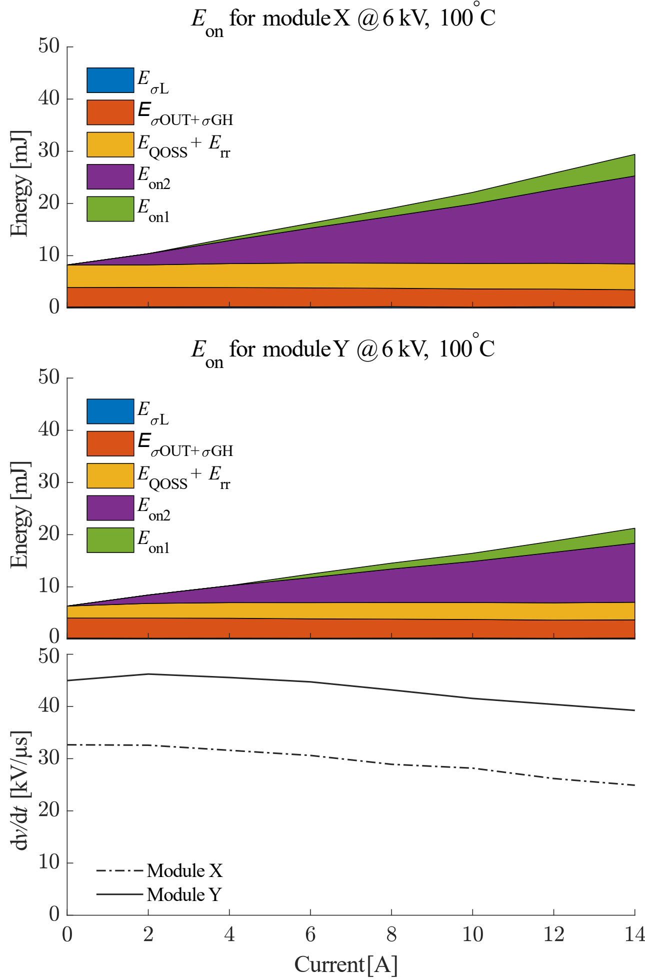


Fig. C.9: Comparison of the turn-on switching energy dissipation E_{on} and dv/dt for modules X and Y at DC-link voltage of 6 kV, load currents of 0 A – 14 A and temperature of 100°C.

load current and temperature for both modules X and Y. The $E_{QOSS} + E_{rr}$ for module X is in the range of 4.1 mJ – 4.4 mJ and 4.3 mJ – 4.9 mJ at 25°C and 100°C respectively, for the DC-link voltage of 6 kV and load current range of 2 A – 14 A. For module Y the $E_{QOSS} + E_{rr}$ is in the range of 2.1 mJ – 2.6 mJ and 2.2 mJ – 3.3 mJ at 25°C and 100°C respectively, for the similar voltage and current levels. When comparing the modules X and Y, it can be observed that the, $E_{QOSS} + E_{rr}$ for module X is higher than the the module Y due to added parallel capacitance of the external SiC JBS diode. It can be identified that the modules with and without SiC JBS diode, both exhibit excellent reverse

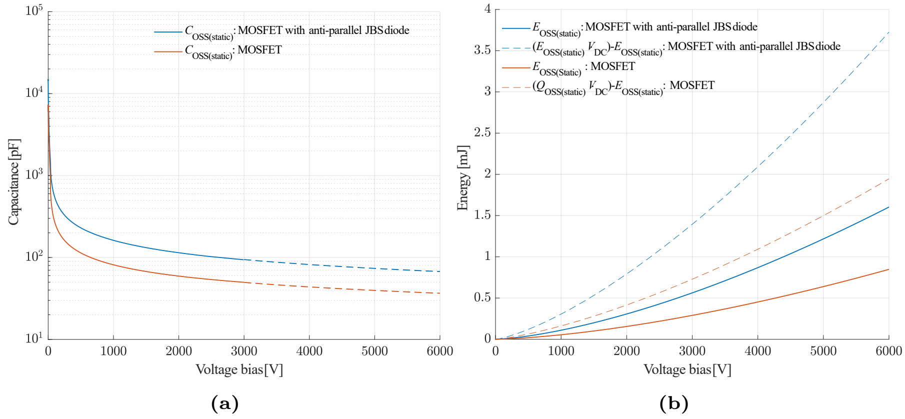


Fig. C.10: (a) Output capacitance ($C_{\mathrm{OSS(static)}}$) measurements obtained utilizing the Keysight B1506 curve tracer and (b) derived output capacitance stored energy $E_{\mathrm{OSS(static)}}$ and $(Q_{\mathrm{OSS(static)}} \cdot V_{\mathrm{DC}}) - E_{\mathrm{OSS(static)}}$ for the generation 3 10 kV SiC MOSFET and the 10 kV SiC MOSFET with anti-parallel 10 kV SiC JBS diode.

recovery performance in terms of their dependency with the load currents and temperature.

To further strengthen the analysis the switching energy dissipation $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ is compared with the stored energy on the device output capacitances based on the static capacitance measurement obtained utilizing the curve tracer. The output capacitance for the generation 3 10 kV SiC MOSFET and the combined output capacitance for the 10 kV SiC MOSFET with anti-parallel 10 kV SiC JBS diode obtained utilizing the Keysight B1506 curve tracer at room temperature (22°C) are shown in Fig. C.10a. Due to the maximum output voltage limitation of 3 kV for the curve tracer, the capacitance for the voltage bias of 3 kV – 6 kV is extrapolated utilizing the curve fitting as shown in Fig. C.10a with dashed line. The stored energy on output capacitance E_{OSS} and derived energy curve $(Q_{\mathrm{OSS(static)}} \cdot V_{\mathrm{DC}}) - E_{\mathrm{OSS(static)}}$ from the curve tracer capacitance measurements is shown in Fig. C.10b. The curve $(Q_{\mathrm{OSS(static)}} \cdot V_{\mathrm{DC}}) - E_{\mathrm{OSS(static)}}$ corresponds to the energy dissipation in the SiC MOSFET due to the charging of the complementary device output capacitance. Therefore, the switching energy dissipation $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ obtained from the double pulse test needs to compared with the derived energy curve $(Q_{\mathrm{OSS(static)}} \cdot V_{\mathrm{DC}}) - E_{\mathrm{OSS(static)}}$ and not the ouput capacitance stored energy $E_{\mathrm{OSS(static)}}$. The stored energy on the power device output capacitance $E_{\mathrm{OSS(static)}}$ and energy $(Q_{\mathrm{OSS(static)}} \cdot V_{\mathrm{DC}}) - E_{\mathrm{OSS(static)}}$ at the DC bias of 6 kV is 1.6 mJ and 3.7 mJ for the MOSFET with anti-parallel JBS diode, whereas in case of the MOSFET it is identified to be 0.8 mJ and 1.9 mJ, respectively.

The measured switching energy dissipation $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ at the DC-link voltage of 6 kV, load currents of up to 14 A and temperature range of 25°C–

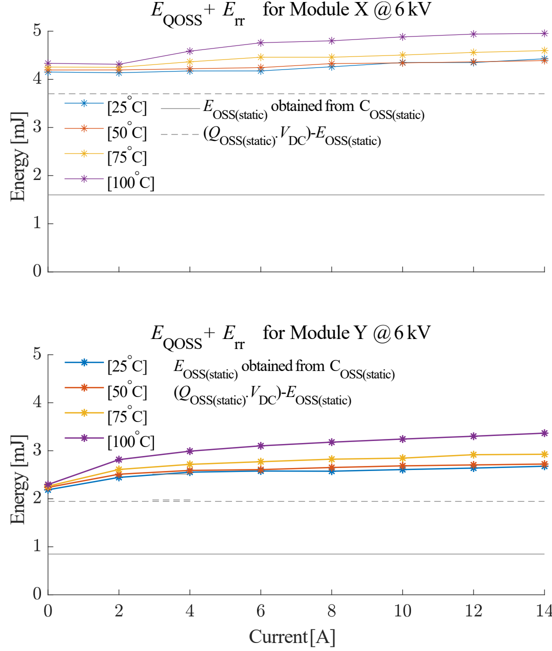


Fig. C.11: comparison of the stored energy on the output capacitance ($E_{\mathrm{OSS(static)}}$) and with switching energy dissipation $E_{\mathrm{QOSS}}+E_{\mathrm{rr}}$ for power modules X and Y at the DC-link voltage of 6 kV, load currents of 0 A – 14 A and temperature range of 25°C–100°C.

100°C for modules X and Y is compared with the derived energy $(Q_{\mathrm{OSS(static)}} \cdot V_{\mathrm{DC}}) - E_{\mathrm{OSS(static)}}$ in Fig.C.10b. It can be identified that major portion of a measured switching energy dissipation $E_{\mathrm{QOSS}}+E_{\mathrm{rr}}$ is contributed by the stored energy on an output capacitance, whereas contribution from the diode reverse recovery is negligible in both cases. Furthermore, $E_{\mathrm{QOSS}}+E_{\mathrm{rr}}$ show only slight increment with the increase in current magnitude and temperature indicating excellent performance in terms of reverse recovery for the modules with and without SiC JBS diode.

The switching energy dissipation in the LS MOSFET due to the discharging and charging of the power module and inductor parasitic capacitance, $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ and $E_{\sigma\mathrm{L}}$ (shown in Fig. C.8 and Fig.C.9) are independent of the load current, turn-on dv/dt and temperature as these switching energy dissipation is due to Joule heating resulting in the MOSFET channel due to the charging or discharging of the parasitic capacitance $C_{\sigma\mathrm{OUT}}+C_{\sigma\mathrm{GH}}$ or $C_{\sigma\mathrm{L}}$. The change in tun-on dv/dt with the load current only change the magnitude of the current with which the capacitance gets charged or discharged whereas the temperature has almost no impact on the magnitude of the capacitance. The $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ for module X is measured to be in the range of 3.1 mJ – 3.7 mJ, whereas for module Y it is measured to be in the range of 3.4 mJ – 3.8 mJ

for the DC-link voltage of 6 kV, load currents of up to 14 A and temperature range of 25°C–100°C.

The $E_{\sigma\text{L}}$ for module X is measured to be in the range of 0.1 mJ – 0.2 mJ, whereas for module Y it is measured to be in the range of 0.1 mJ – 0.3 mJ for the DC-link voltage of 6 kV, load currents of up to 14 A and temperature range of 25°C – 100°C. The switching energy dissipation $E_{\sigma\text{OUT}+\sigma\text{GH}}$ and $E_{\sigma\text{L}}$ is almost identical for both power modules X and Y due to the similar power module DBC layout and same load inductor utilized for the test.

It is worth mentioning that, discharging of the LS device output capacitance through the MOSFET channel also incur switching energy dissipation equal to $E_{\text{OSS(static)}}$, however this can not be measured as discussed in [19]. Therefore, the actual turn-on switching energy dissipation E^{*}_{on} in the LS SiC MOSFET is higher than the measured switching energy dissipation E_{on} by the value of $E_{\text{OSS(static)}}$ and can be expressed as,

$$E^{*}_{\text{on}} = E_{\text{on}} + E_{\text{OSS(static)}} \tag{C.10}$$

C.5.2 Analysis of the turn-off switching energy dissipation

The comparison of a turn-off switching energy dissipation together with the turn-off $\mathrm{d}v/\mathrm{d}t$ for the power modules X and Y at the DC-link voltage of 6 kV, load currents of up to 14 A at temperatures of 25°C and 100°C is shown in Fig. C.12 and Fig. C.13, respectively.

Opposite to the turn-on in the case of turn-off switching transient, the $\mathrm{d}v/\mathrm{d}t$ increases with the increase in the load current magnitude. For turn-off switching transient the load current magnitude has dominant influence on the $\mathrm{d}v/\mathrm{d}t$, than that of the gate resistance itself [19]. For the similar experimental condition, the turn-off $\mathrm{d}v/\mathrm{d}t$ for module X is lower than that of module Y. This is due to the added capacitance due to the external JBS diode that acts as snubber resulting in an increased time interval t_6–t_7. The turn-off $\mathrm{d}v/\mathrm{d}t$ for both modules X and Y show only minor increment with increase temperature. The turn-off $\mathrm{d}v/\mathrm{d}t$ for module X at the DC-link voltage of 6 kV and load current of 14 A at 25°C and 100°C, is 30.5 kV/µs and 31.6 kV/µs respectively, whereas for module Y it is identified to be 40.8 kV/µs and 42 kV/µs respectively. The E_{off} for module X is measured to be in the range of 1.6 mJ – 1.9 mJ, whereas for module Y it is measured to be in the range of 0.8 mJ – 1 mJ for the DC-link voltage of 6 kV, load currents of up to 14 A and temperature range of 25°C – 100°C.

$$E_{\text{off}} = \int_{t6}^{t7} i_{\text{DC}-} \cdot v_{\text{OUT}} \cdot \mathrm{d}t \tag{C.11}$$

The switching energy dissipation E_{off} is slightly higher than the measured E_{OSS} from the curve tracer capacitance measurements. This suggest in case of both

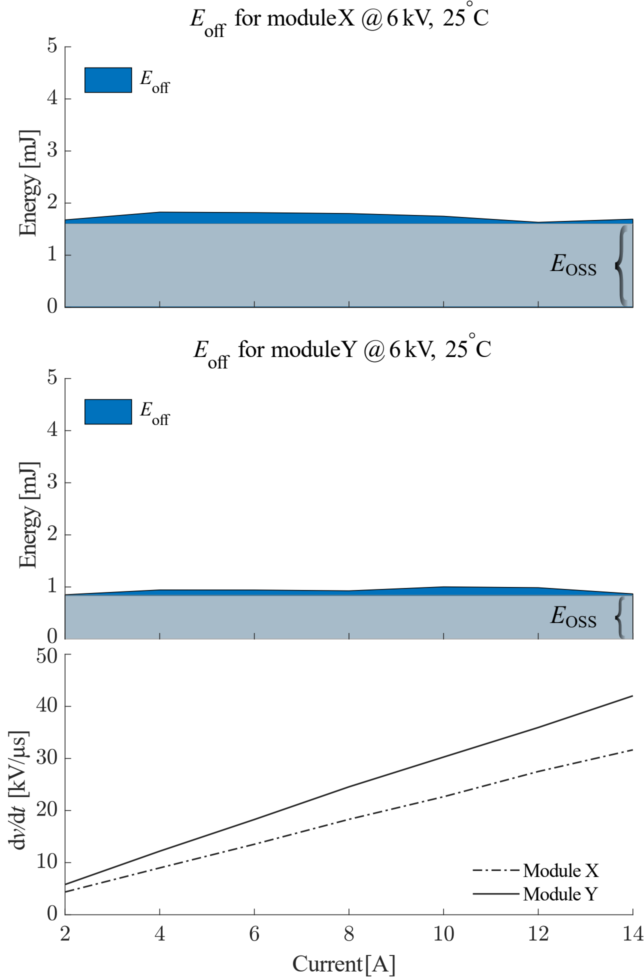


Fig. C.12: Comparison of the turn-off switching energy dissipation E_{off} and $\mathrm{d}v/\mathrm{d}t$ for modules X and Y at the DC-link voltage of 6 kV, load currents of 0 A – 14 A and temperature of 25°C.

power modules X and Y most of switching energy measured during the turn-off switching transient is stored energy on the LS device output capacitance.

Thus, in the case of turn-off switching transient actual switching energy dissipation E^*_{off} is lower than the measured switching energy dissipation by the value of $E_{\text{OSS(static)}}$ and can be expressed as,

$$E^*_{\text{off}} = E_{\text{off}} - E_{\text{OSS(Static)}} \tag{C.12}$$

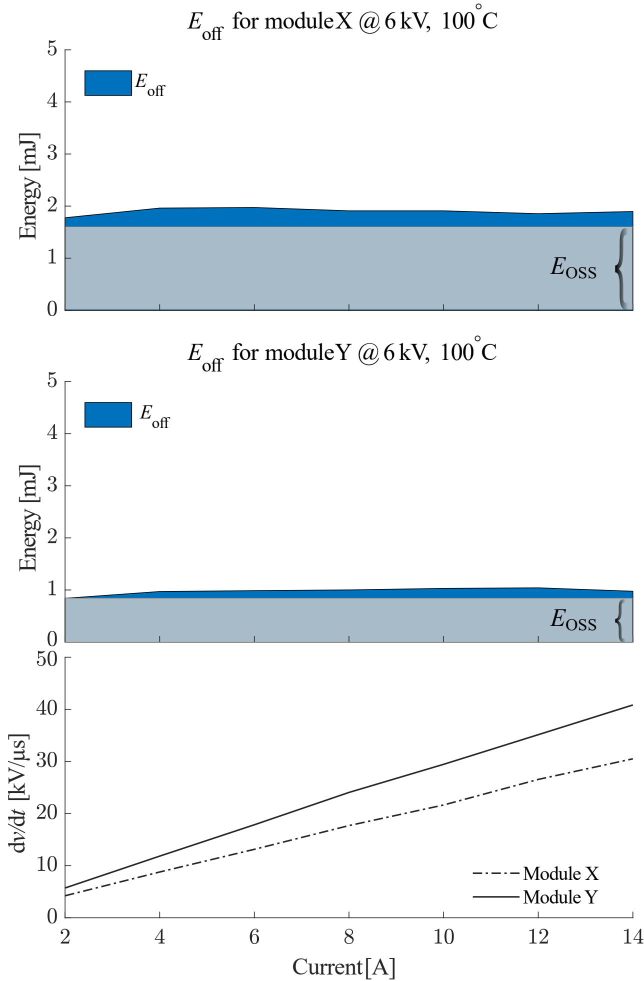


Fig. C.13: Comparison of the turn-off switching energy dissipation E_{off} and $\mathrm{d}v/\mathrm{d}t$ for modules X and Y at DC-link voltage of 6 kV, load currents of 0 A – 14 A and temperature of 100°C.

C.6 Conclusion

The impact of the external anti-parallel SiC JBS diode on the SiC MOSFET switching transient is analysed utilizing two 10 kV half bridge SiC MOSFET power modules with and without SiC JBS diode. With switching energy dissection, a quantitative analyses on the switching energy dissipation for the modules with and without SiC JBS diode is analysed. The difference in a turn-on switching energy dissipation for the module without SiC JBS diode is due to the increased switching time interval and additional capacitive losses

incurred due to the added junction capacitance of the SiC JBS diode. With excellent reverse recovery performance for the 10 kV SiC MOSFET body diode for tested load current range of up to 14 A and temperature of 25°C and 100°C at DC-link voltage of 6 kV, the power module without an anti-parallel SiC JBS diode exhibit superior performance in terms of turn-on switching energy dissipation. In the case of turn-off, the inclusion of an anti-parallel SiC JBS diode results in an increased switching time interval. However, its impact on the actual turn-off switching energy dissipation is negligible in comparison to turn-on switching energy dissipation.

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Paper D

Demonstration of a 10 kV SiC MOSFET based Medium Voltage Power Stack

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The layout has been revised.

Demonstration of a 10 kV SiC MOSFET based Medium Voltage Power Stack

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Abstract

This paper presents a 10 kV SiC MOSFET based power stack, featuring medium voltage power conversion with a simple two-level voltage source converter topology. The design of the medium voltage (MV) power stack is realized in a commercial IGBT based three phase power stack frame. The power stack assembly comprises of the custom packaged single-chip half bridge 10 kV SiC MOSFET power modules, gate driver units with a very low isolation capacitance, DC-link capacitors, busbar and a liquid cooled heatsink. The designed power stacks are tested in a DC-fed three phase back-to-back setup with the total circulated power of 42 kVA, DC-link voltage of 6 kV, rms load current of 7 A and 5 kHz switching frequency. Under this operating conditions, an efficiency $> 99\%$ is deduced for the designed MV power stack.

D.1 Introduction

Silicon Carbide (SiC) semiconductor devices in 10 kV –15 kV voltage class offers unprecedented blocking voltage capability and superior switching characteristics compared to their Silicon (Si) counterparts [1]. These properties of the SiC power devices have resulted in an increased interest for their adoption in the medium voltage (MV) power electronics applications, since they enable simplification of the power converter topology, increased efficiency and operation at higher switching frequencies [2], [3]. In addition to this, the inherent benefits resulting from a superior material characteristics of SiC over Si opens up new possibilities for power densities and efficiency improvements in medium voltage high power conversion applications [4]. The lower switching losses due to the faster switching speeds of the MV SiC MOSFET enables the converter switching frequencies in the range of few tens of kHz to MHz for the DC-link voltages of 3 kV up to 10 kV in various hard switched or soft switched applications such as solid state transformers [3], [5], grid support [2], induction heating [6].

This paper demonstrates a 50 kVA MV power stack design based on the custom packaged single-chip half bridge 10 kV SiC MOSFET power modules, with a two-level voltage source converter (VSC) topology. The power stack is designed with the same frame of a commercial 500 kVA, 1.7 kV IGBT based

690 V three phase power stack. The rated power of up to 500 kVA is aimed to achieve in the same power stack footprint utilizing multi-chip 10 kV SiC MOSFET power modules as opposed to what is deployed here for the 50 kVA demonstration. The key specifications of the 50 kVA and proposed 500 kVA scalable MV power stack are presented in Table D.1.

Table D.1: Specifications of the medium voltage power stack.

Parameter	Value
Rated Power	50 kVA–500 kVA
DC-link voltage	6 kV–7.2 kV
Line-line AC voltage (rms)	4.16 kV
AC current (rms)	7 A–70 A
Switching frequency	5 kHz–10 kHz

The key components and sub-assembly of the power stack including the half bridge power module with reduced parasitic capacitance, low isolation capacitance gate driver, DC-link and busbar layout as well as thermal designs are presented in Section II. In Section III, the static characterisation related to the on-state resistance of the 10 kV SiC MOSFET and switching energy dissipation for the custom packaged half bridge SiC MOSFET power modules are presented to provide an insight into the semiconductor conduction and switching performance. The designed power stack are tested in a DC-fed three phase back-to-back test setup. The experimental results for the converter operation with the DC-link voltage of 6 kV, rms load current of 7 A at 5 kHz switching frequency are presented with a brief discussion on the designed power stack efficiency.

D.2 Medium voltage power stack

This section presents the key components and sub-assembly of the MV power stack.

D.2.1 Half bridge 10 kV SiC MOSFET power module

The power stack design is based on the custom packaged single-chip half bridge 10 kV SiC MOSFET power module [7], as shown in Fig. D.1. This half bridge power module is populated with the 3rd generation 350 mΩ, 10 kV SiC MOSFET (CPM3-10000-0350) and JBS diode dies from Wolfspeed [4], which are soldered on a 0.63 mm Aluminium Nitiride (AlN) Direct Bonded Copper (DBC) with a 5 mm[1] AlSiC baseplate. The power module is housed in a 3D printed plastic housing encapsulated in a Silicon gel. A plastic holder is placed inside the module which provides an access to the surface of the die. With

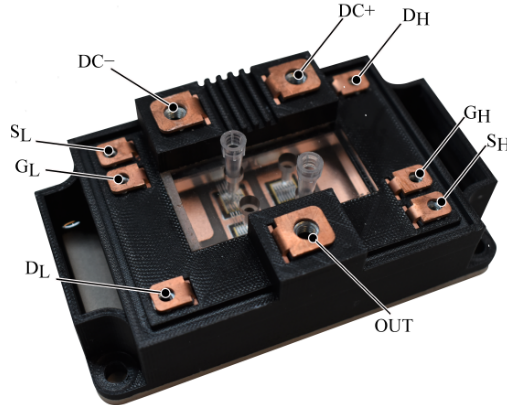

Fig. D.1: Picture of the single-chip half bridge 10 kV SiC MOSFET power module.

this arrangement the local surface temperature of the die can be monitored using a fiber optic temperature sensors. With the SiC MOSFETs the $\mathrm{d}v/\mathrm{d}t$ during the switching transitions can reach the magnitudes of extremely high values [2], therefore in case of the MV converter enabled by the SiC MOSFETs it is increasingly important to minimize the parasitic capacitances to limit the capacitive currents during the switching transitions. The power module is designed with a reduced capacitive couplings between the top copper layer of the DBC connected to the half bridge output as well as high side gate plane and baseplate [7]. This is required to limit the capacitive currents during the switching transitions, which results in an increased switching energy dissipation and conducted Electromagnetic Interference (EMI) [8], [9]. In contrast to the low voltage SiC or Gallium Nitrie (GaN) semiconductor devices, where the switching performance is sensitive to parasitic inductances in terms of over voltage and ringing, for MV power modules the lower parasitic capacitance design is necessary.

D.2.2 Isolated power supply and gate driver

To drive the high side SiC MOSFET in the half bridge SiC MOSFET power module, a gate driver power supply with an appropriate galvanic isolation is required. Furthermore, the high $\mathrm{d}v/\mathrm{d}t$ switching transitions of the SiC MOSFET leads to the common mode current through the isolation capacitance of the high side gate driver power supply. From this point of view, an isolated DC-DC power supply with a low isolation capacitance and high $\mathrm{d}v/\mathrm{d}t$ ruggedness is

[1] In this publication, the power module AlSiC baseplate thickness has been mistakenly reported as 5 mm instead of 3 mm. In spite of this error, the text has not been revised and the appended publication is maintained in the original form of published version.

necessary for the reliable operation of the gate driver circuit [10]. A custom made DC-DC power supply with a very low isolation capacitance and isolation voltage rating of up to 10 kV was designed [11]. The picture of the PCB which includes both the the DC-DC isolated power supply and the gate driver circuit for the 10 kV half bridge SiC MOSFET power module is shown in Fig. D.2.

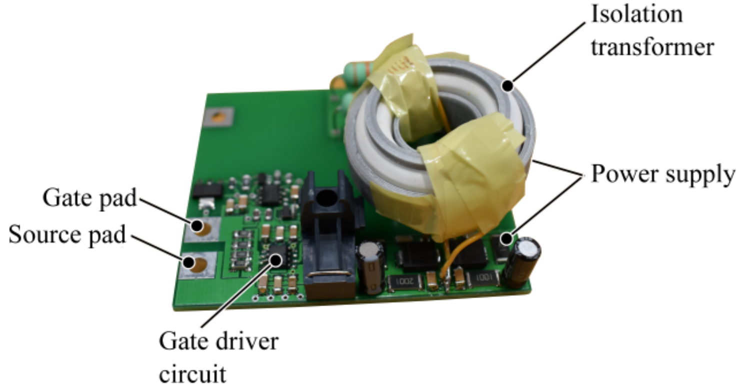

Fig. D.2: Picture of an isolated DC-DC power supply and gate driver PCB.

A Flyback topology with a primary side sensing is chosen to avoid the additional coupling capacitance resulting from the feedback signals over the isolation barriers. For, the isolation transformer a high permeability 3F3 Ferrite core is used. For the windings, the triple insulated wire with insulation voltage of 15 kV is utilised to achieve the desired isolation level. The maximum isolation capacitance for the gate driver is measured to be 2.6 pF [12]. The power supply outputs +20 V and -5 V, which is the recommended turn-on and turn-off gate driver voltage respectively for the 10 kV SiC MOSFET.

The output stage of the gate driver is designed with a driver IC IXDN614 with peak sink/source current capability of 14 A. In order to prevent the Miller induced false turn-on, an Active Miller clamp functionality is incorporated in the gate driver stage. In order to provide the isolation and achieve increased $\mathrm{d}v/\mathrm{d}t$ at the control interface, the gate signals to the driver from the DSP control card are transferred via an optic fiber link.

D.2.3 DC-link and busbar design

The DC-link capacitance for the power stack is designed considering the maximum converter power rating of 500 kVA. For a PWM (Pulse Width Modulated) converter, the worst case current stress on the DC-link capacitor appears for the converter operation with modulation range of approximately 0.6 and unity load

power factor [13]. With the output line-line converter rms voltage of 4.16 kV and rated power of 500 kVA, the worst case DC-link current stress is calculated analytically ($i_{C_{DC},rms} = 45$ A) based on [13]. The minimum DC-link capacitance requirement established based on the maximum ripple voltage of 10% [14], is plotted in Fig. D.3 for the converter switching frequency of 5 kHz and 10 kHz.

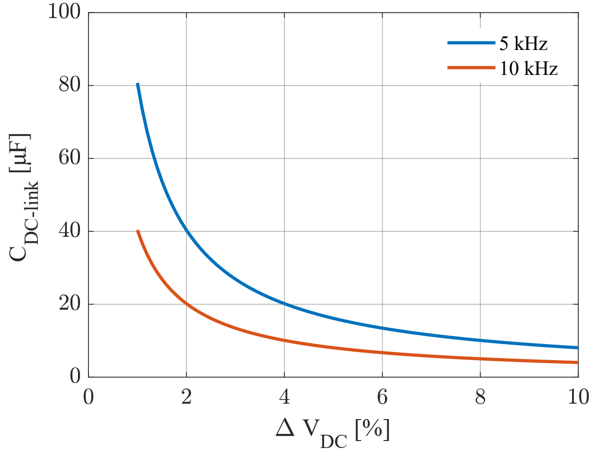

Fig. D.3: DC-link capacitance requirement as a function of voltage ripple for switching frequency of 5 kHz and 10 kHz. (Obtained for the worst case capacitor ripple current)

Taking into account the maximum ripple voltage criteria of 10 %, calculated worst case current stress and the available product range of the DC-link capacitors for MV applications, a 3.6 kV, 40 µF film capacitor (Electronicon E50.N14-403NTO [15]) is chosen for the designed DC-link, ensuring that it fulfills the maximum DC-link voltage ripple criteria of 10 % and the maximum rms current rating of the capacitor is well within the analytically obtained worst case DC-link current stress. Total DC-link capacitance of 100 µF with rated voltage of 7.2 kV is obtained using series/parallel combination of total ten 40 µF, 3.6 kV capacitors as shown in Fig. D.4. The electrical connection from the DC-link capacitance to the SiC MOSFET power module is provided using, a three layer stacked busbar, which is cutout from the 1.2 mm steel sheet as shown in Fig. D.4. (The choice of the steel for the busbar is to do with the required mechanical strength for the given bending radius at the power module connection terminals for the busbar.) Considering the low scale of economy in case of a laminated busbar for the designed prototype together with its intended operation in the laboratory environment, a simple approach is used to provide adequate isolation between each layer of the stacked busbar. Where, each layer of the sacked busbar is isolated with four layers of 50 µm Kapton tape providing isolation voltage withstand capability of approx. 48 kV [16]. The 3D CAD

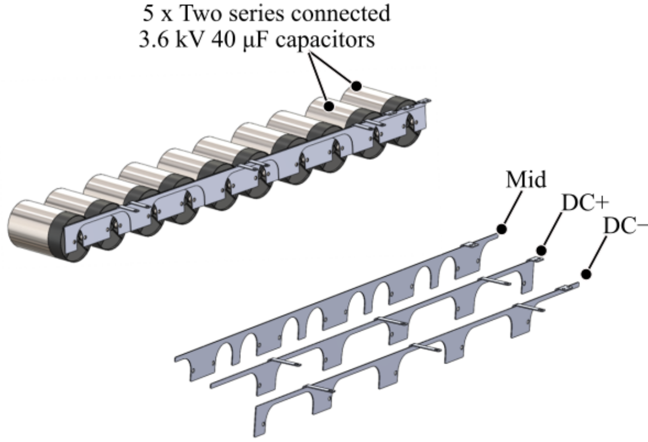

Fig. D.4: 3D-CAD model of the DC-link capacitors and busbar assembly.

model of the designed busbar and the picture of the assembly is presented in Fig. D.4. With the rated blocking voltage capability of 10 kV for the SiC MOSFET and relatively low $\mathrm{d}i/\mathrm{d}t$, an extremely low inductive busbar design is of little to no importance since the inductance has minor influence on the switching performance in terms of the over voltages and ringing.

D.2.4 Thermal management

The significantly higher heat transfer coefficients for the liquid cooling in comparison to the air cooling provides a superior thermal performance, which enables a high power density and compact solution for a power electronics converter. Considering this fact, a direct liquid cooling solution (ShowerPower concept from Danfoss [17]) is opted for the designed power stack as shown in Fig. D.5. In contrast to the indirect liquid cooling, the direct liquid cooling eliminates the thermal interface material (TIM) between the power module baseplate and cooler since in the case of direct liquid cooling the coolant is in direct contact with the baseplate. The TIM accounts for approximately 30%–50% of the total thermal resistance, so elimination of the TIM in the direct liquid cooling significantly improves the thermal performance [17].

The liquid cooling assembly shown in Fig.D.5 features a plastic turbulator, O-ring for sealing purpose and a custom-made adapter which is mounted on the cooler. The coolant reaches the turbulator through the grooves on the sides via the openings provided on the cooler. The turbulator which consists of multiple cells in X and Y directions, guides the coolant along the power module baseplate. The coolant flow rate and pressure for the shown liquid cooling systems are in the range of 20 litres/minute and 3 bars respectively.

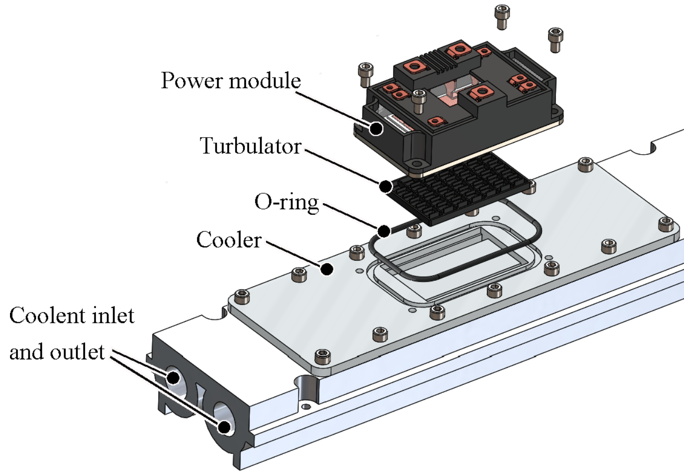

Fig. D.5: 3D CAD model of the half bridge 10 kV SiC MOSFET power module and cooler assembly.

D.2.5 Power stack assembly

The picture of the designed liquid cooled MV three phase power stack is shown in the Fig. D.6. The power stack assembly consist of one single chip half bridge 10 kV SiC MOSFET power modules per phase, DC-link capacitors with busbars, gate drivers and a cooler.

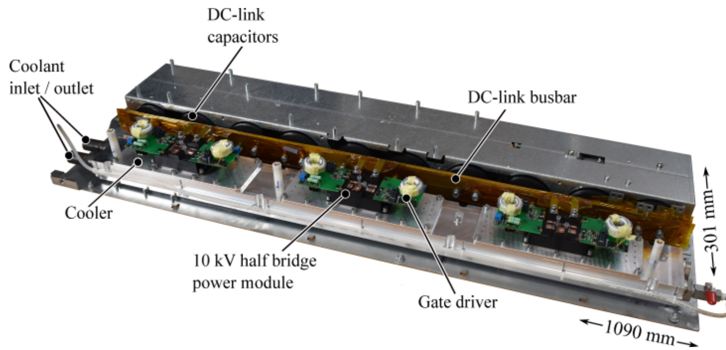

Fig. D.6: Picture of the 10 kV SiC MOSFET based liquid cooled medium voltage power stack.

D.3 Experimental results

In this section, the static and dynamic characterisation results are presented to provide an insight into the MOSFET on-state resistance and switching energy dissipation for the 10 kV SiC MOSFET die and half bridge power modules respectively. In addition to this the key experimental results for the converter operation in a three phase back-to-back setup are presented with a brief discussion.

D.3.1 On-sate and switching characteristics of the half bridge 10 kV SiC MOSFET power module

Fig. D.7a, shows the MOSFET on-state resistance $R_{\mathrm{DS(on)}}$ as a function of temperature for the two dies. These two dies represent the the upper and lower extreme of the on-state resistance from the sample of total 78 dies based on the spread in their VI characteristics at 25°C. The on-state resistance as function of temperature for these two dies is presented in Fig.D.7a, which is obtained by evaluating the slope of the MOSFET VI characteristics in ohmic region corresponding to the gate-source voltage of 20 V. The on-state resistance ranges within 340 mΩ - 380 mΩ at 25°C, which increases by approximately 120% to 795 mΩ - 840 mΩ at 125°C.

In the case when, the SiC MOSFET is operated in a third quadrant with a gate bias of 10 V–20 V, the intrinsic body diode conduction is predominantly through the MOSFET channel [18], since the channel resistance acts as a shunt in parallel with the body diode suppressing bipolar current injection through the diode [19], [20]. Therefore, the VI characteristics in the third quadrant follows the same slope as in the first quadrant for the gate bias of 10 V–20 V. In case, when the 10 kV anti-parallel JBS diode is used the current is predominantly shared between the MOSFET channel and the anti-parallel JBS diode. The forward VI characteristics of the 10 kV JBS diode is shown in Fig. D.7b, where it can be seen that the forward voltage of the diode is in the range of 1 V–1.2 V for the temperature range of 25 °C–125 $°C$. In this temperature range, the slope of the JBS diode forward VI characteristics is found to be close to that of the on-state resistance of the 10 kV SiC MOSFET. During the third quadrant operation of the SiC MOSFET with a gate bias of 20 V and an anti-parallel 10 kV SiC JBS diode, the diode will start to share the current as soon the drain-source voltage of the MOSFET is above (-1 V)–(-1.2 V). Even in this case, the MOSFET channel shares the largest portion of the current.

The turn-on and turn-off switching energy dissipation (E_{on} and E_{off}) for the 10 kV half bridge SiC MOSFET power modules are obtained from its dynamic characterisation in a double pulse test setup with a baseplate temperature of 25°C. The E_{on} and E_{off} for the external gate resistance of 20 Ω is plotted in Fig. D.7c and D.7d respectively as a a function of load current and DC-link

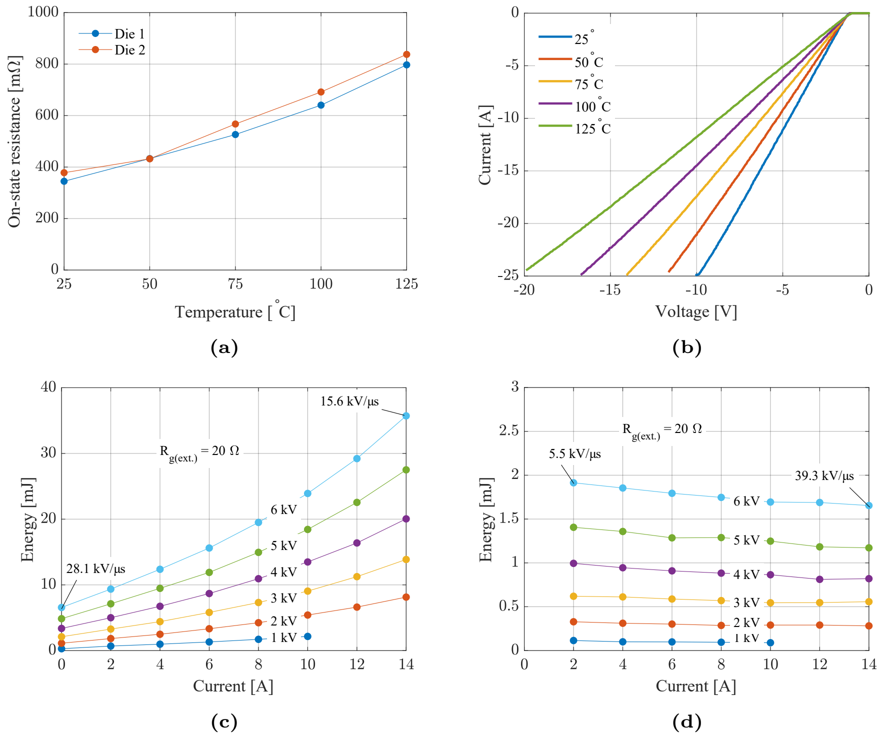

Fig. D.7: (a) On-state resistance vs temperature of the 10 kV SiC MOSFET, (b) forward IV characteristics of 10 kV JBS diode, (c) turn-on and (d) turn-off switching energy dissipation for the 10 kV half bridge SiC MOSFET power module.

voltages of 1 kV–6 kV. For a given load current, the turn-on switching energy dissipation increases, whereas the turn-off switching energy dissipation remains almost constant or changes slightly with increase in the load current magnitude. The turn-on and turn-off switching energy dissipation for the load current of 14 A and DC-link voltage of 6 kV is measured to be 35.7 mJ and 1.6 mJ respectively. The turn-on $\mathrm{d}v/\mathrm{d}t$ increases whereas the turn-off $\mathrm{d}v/\mathrm{d}t$ decreases with increasing value of the load current magnitude [18]. The maximum turn-on and turn-off $\mathrm{d}v/\mathrm{d}t$ is identified to be 28.1 kV/μs and 39.3 kV/μs for the load current magnitude of 0 A and 14 A respectively.

For the same DC-link voltage and the load current magnitude, the the turn-on switching speed of the SiC MOSFET increases resulting in a slightly lower turn-on switching energy dissipation at alleviated temperatures [18]. The increase in switching speed is due to the combined effect of the temperature dependent shift in the gate threshold and trans-conductance parameter, which lowers gate-source Miller plateau voltage with increasing temperature. Whereas, the temperature has almost no or negligible effect on the turn-off switching energy dissipation [18]. Considering that the coolant temperature of the power stack is maintained at 23°C for the nominal operating conditions, the turn-on and turn-off switching energy dissipation shown in Fig. D.7 measured at 25°C with gate resistance of $R_\mathrm{g} = 20\ \Omega$ can be regarded as the worst case scenario for the switching energy dissipation.

D.3.2 Experimental setup and test results

The designed power stack is tested in the DC fed three phase back-to-back setup with an inductive load of 160 mH per phase. The schematic and the picture of the laboratory test setup is shown in Fig. D.8a and D.8b respectively. In this test setup, the power cycles between the two converters where one of the converter can be regarded as a source and another as a load. The DC source supplies the losses contributed by semiconductors and magnetics. With such arrangement, the power modules can be exposed to the current and voltage stresses as experienced in a realistic three phase converter operation.

In the experimental test, the two back-to-back converters are controlled in the open loop, where the voltage magnitude or phase difference of the fundamental output voltage at the each phase of the two converters are adjusted appropriately to obtain the desired load current magnitude. The test results presented here on-wards are related to the converter operation at the DC-link voltage of 6 kV and switching frequency of 5 kHz. The modulation index (M) and the phase shift are set to 0.8 and 10 deg. respectively, which results in the rms load current $i_\mathrm{ph,rms}$ of approximately 7 A. Fig. D.8c, shows the DC-link voltage and the zoomed view of the output voltages at phase-a for the two converters with respect to the mid-point of a DC-link. The phase output voltages v_ao and $v_\mathrm{a'o}$, show clean switching transitions without any significant overshoot or ringing.

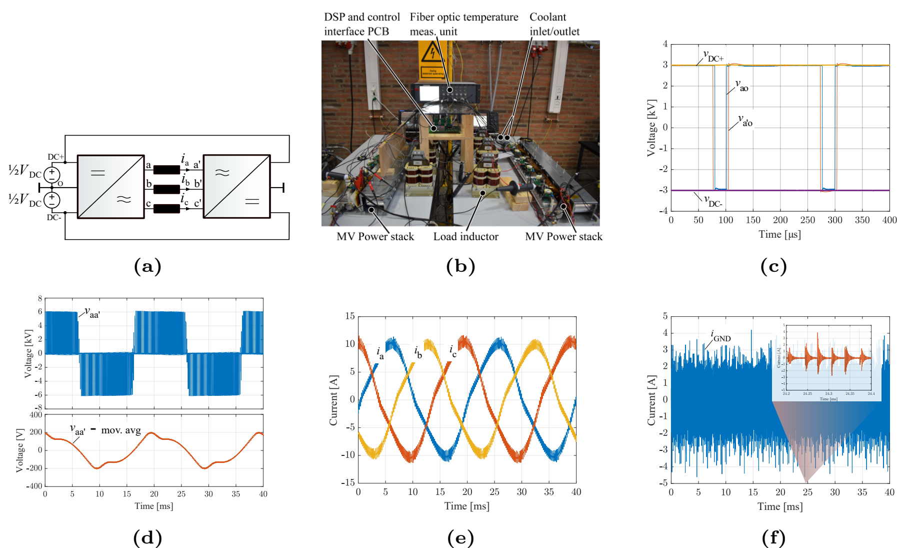

Fig. D.8: (a) Schematic and (b) image of the thee phase back-to-back test setup, (c) measured phase-a half bridge output voltages, (d) Phase-a load inductor voltage and its moving average, (e) measured three phase load currents and (f) heatsink ground current.

The voltage across the load inductor $v_{aa'}$ for the phase-a is obtained from the measured phase output voltages ($v_{aa'} = v_{ao}$ - $v_{a'o}$) and its moving average is plotted in Fig. D.8d. The measured three phase load currents are plotted in Fig D.8e. Since, the converter is operated in an open loop without dead-time error compensation, the voltage error (due to the inverter non-linearities - i.e: deadtime, device parasitics..) resulting during the deadtime which is current polarity dependent, causes the distortion around the zero crossing of the load currents. To obtain the desired rms load current of 7 A with fundamental frequency of 50 Hz, the required average voltage across the 160 mH[2]inductor is significantly low compared to the DC-link voltage of 6 kV. Due to this the voltage error during the deadtime is comparable to the average voltage across the inductor, resulting in a more pronounced distortion effect around the zero crossing of the three phase load currents.

The capacitive currents due to the charging and discharging of the power module parasitic capacitances conducts through the heatsink which needs to be grounded due to the safety requirements. The measured currents at the grounding connection point of the heatsink is presented in Fig. D.8f, which shows the peak amplitude of 4 A with high frequency oscillations in the range of 1.1 MHz. Depending on the application and the heatsink grounding

[2]In this publication, the load inductor value has been mistakenly reported as 160 mH instead of 60 mH. In spite of this error the text has not been revised and the appended publication is maintained in the original form of published version.

requirements, there is also a possibility of redirecting the heatsink ground current to the DC-link by providing a low impedance connection. In order to suppress the heatsink ground current the impedance can be inserted between the heatsink and ground, however this would result in the voltage potential on the heatsink during the converter operation. The magnitude and the voltage potential on the heatsink is determined by the nature of the inserted impedance network [21].

For the converter operation in the back-to-back test setup, the surface temperature of die is measured using a fiber optic temperature sensor (OTG F-10 from OpSense [22]) in order to monitor the expected junction temperature during the nominal operating conditions. With the coolant temperature of 20.5°C, the mean temperature of the MOSFET die under the converter steady state operating condition is measured to be 45° C. At this operating point, the total power losses for the back-to-back test setup is deduced to be 384 W from the DC power supply readout. Based on the on-state resistance measurement of the 10 kV SiC MOSFET die and switching energy dissipation for the half bridge power module presented in Section II as well as the DC-resistance of the inductor obtained from the impedance analyser measurement, it can be inferred that the major part of the total power losses is accounted due to the semiconductor switching and conduction and a small part of it is due to the copper losses in the inductor. It should be noted that in the presented test configuration the core losses are almost negligible for the inductor due to significantly lower load current ripple. Considering that the power losses are distributed equally in the two power stacks under test, the power loss for the individual power stack (i.e conduction and switching losses in the three half bridge power modules) including the load inductor is deduced to be less than 1% of the total circulated power of 42 kVA[3], resulting in an efficiency $> 99\%$ for the designed power stack.

D.4 Conclusion

This paper demonstrates the medium voltage liquid cooled power stack enabled by custom packaged single-chip half bridge 10 kV SiC MOSFET power modules. The power stack sub-assembly including the half bridge power modules, gate driver, DC-link busbar and heatsink is discussed briefly including the key design considerations imposed by the medium voltages and extremely fast switching speeds of SiC MOSFETs. The designed power stacks are tested in a DC fed three phase back-to-back setup with an inductive load at DC-link voltage of 6 kV and switching frequency of 5 kHz. Under this operating conditions with

[3]In this publication, the total circulated power has been mistakenly reported as 42 kVA instead of 35.6 kVA. In spite of this error, the text has not been revised and the appended publication is maintained in the original form of published version.

a total circulated power of 42 kVA, an efficiency $> 99\%$ is deduced for the designed MV power stack.

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Paper E

Multi-chip Medium Voltage SiC MOSFET Power Module with Focus on Low Parasitic Capacitance.

Jannick Kjær Jørgensen, Dipen Narendra Dalal, Szymon Bęczkowski, Stig Munk-Nielsen and Christian Uhrenfeldt

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The layout has been revised.

Multi-chip Medium Voltage SiC MOSFET Power Module with Focus on Low Parasitic Capacitance

Jannick Kjær Jørgensen, Dipen Narendra Dalal, Szymon Bęczkowski, Stig Munk-Nielsen and Christian Uhrenfeldt

Abstract

Advances in high breakdown voltage SiC MOSFETs is enabling the use of simpler topologies, such as a half-bridge in medium voltage applications. In order to increase the power output it is necessary to parallel multiple MOSFETs, which can be done in power modules. At high voltage operating conditions parasitic capacitances of the power module become increasingly important to consider, due to increased switching losses and increased risk to cause EMI. A 10 kV, 80 A half-bridge design is presented using four MOSFETs in parallel, with a design focus on minimal parasitic capacitances.

E.1 Introduction

The introduction of 10 kV SiC MOSFETs is enabling the possibility for simpler topologies in medium voltage (MV) applications, however due to their low current rating it is necessary to use multiple dies in parallel to increase the power output as is done in [1]–[3]. When paralleling multiple MOSFETs it is important to consider the risk of current imbalance, mainly caused by gate loop impedance mismatch, common source impedance mismatch, and die variation as explained in [4]. Traditionally the design focus for conventional power modules has been minimizing parasitic inductances, due to the high current rating relative to the voltage rating. The parasitic capacitances of a power module has received little attention although they impact switching losses and increase the risk to cause electromagnetic interference (EMI), which is of increasing concern at higher voltage ratings enabled by SiC transistors. In this paper a custom made 10 kV, 80 A power module will be presented with minimal parasitic capacitances that impact switching losses and reduces the risk to cause EMI, along with experimental results of a double pulse test, indicating a fast switching speed at a relatively high external gate-resistance. The maximum $\mathrm{d}v/\mathrm{d}t$ found was 74 kV/µs for turn-off at 6 kV, 56 A and 41.4 kV/µs for turn-on at 6 kV, 8 A.

E.2 Medium Voltage Design Considerations

When designing power modules the focus has historically been to minimize parasitic inductances of the power loop and gate loops, however in MV power module this design focus is shifted. This can be seen from the perspective of energy stored in the parasitics of a power module. As unwanted perturbations of a system require and scale with energy it can used as an indicator for the proper design focus. The stored energy in parasitic inductance and capacitance are found by:

$$E_{\text{Cap}} = \frac{1}{2} \cdot C_{\text{para}} \cdot V^2 \quad \& \quad E_{\text{Ind}} = \frac{1}{2} \cdot L_{\text{para}} \cdot I^2, \tag{E.1}$$

The ratio between energy stored in parasitic capacitance and inductance is then:

$$\frac{E_{\text{Capacitive}}}{E_{\text{Inductive}}} = \frac{C_{\text{para}} \cdot V^2}{L_{\text{para}} \cdot I^2} = S_{\text{parasitic}} \left(\frac{V}{I}\right)^2 \tag{E.2}$$

with $S_{parasitic}$ being the ratio between the parasitic capacitance and the parasitic inductance. This relationship can be used as an indicator on which type of parasitics may be most important to focus on. **Equation** (E.2) can be examined for multiple voltage to current ratings as is done in **Figure E.1** for a low voltage (LV) power module rating of 1700 V, 1200 A and MV power module rating of 10 kV, 80 A.

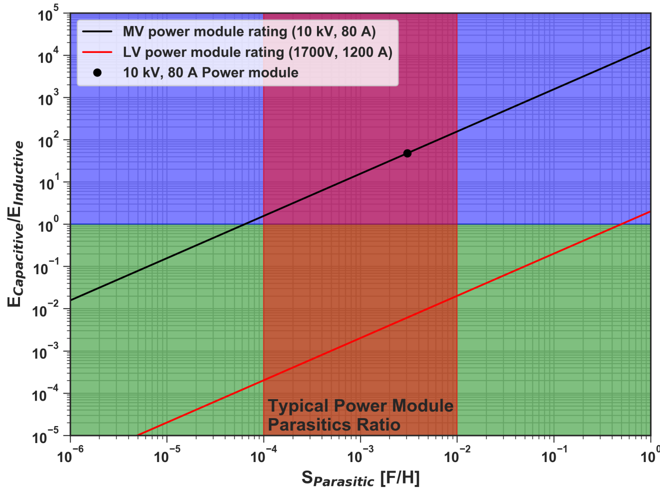

Fig. E.1: Stored energy ratio of parasitics as a function of $S_{parasitic}$ for a medium (black) and low (red) voltage rating. The black dot indicates location for the power module presented in this paper. Blue and green regions indicate higher stored energy in parasitic capacitance or inductance, respectively. Red region indicates typical parasitic ratios for power modules.

The parasitics used for $S_{\text{parasitic}}$ should be critical for the power module and related to the voltage and current ratings, such as any inductance that carries parts of power loop current, or capacitances that are charged or discharged every switching event, due to coupling to a changing voltage potential. The designer of a power module may also have a general idea of the typical ratio of the application which can also be used as an estimate early in the design process. The parasitic inductance is typically on the order of nH, and the parasitic capacitance on the order of pF for power modules giving $S_{\text{parasitic}} \approx 10^{-3}$.

Using an example of a LV power module rating of 1700 V, 1200 A it can be seen that energy stored in parasitic inductance is dominant across the entire typical $S_{\text{parasitic}}$ range. It it therefore appropriate for the LV power module design focus to be minimizing parasitic inductances. For the MV power module rating, however, this design focus is no longer correct. As is seen in **Figure E.1** the energy stored in parasitic capacitance is dominant even if the parasitic ratio is one order of magnitude lower than the typical. In the figure there is also a black dot showing the energy ratio for the specific MV power module presented later, which shows that the energy stored in parasitic capacitance is still dominating. It must be emphasized that this argument can not stand alone as the only design focus, as certain critical parasitics are still important to consider. As the power module presented in this paper is a multi-chip design it is critical to ensure current balance between the parallel MOSFETs, which is related to the mismatch of gate-loop parasitic inductance and mismatch of common source parasitic inductances as explained in [4].

E.3 Design of 10 kV, 80 A SiC MOSFET Power Module

The power module is a multi-chip half-bridge design with eight 10 kV MOSFETs, as shown in **Figure E.2**. Four MOSFETs are in parallel for each DC-link connection. The body diode of the MOSFET is good enough to use as reported in [5]-[6], therefore no 10 kV JBS diodes are used, as they impact the parasitic capacitance of the power module both by increasing the physical copper area needed inside the power module and their junction capacitance, which increases switching losses. In a half-bridge design the parasitic capacitance from the output to the baseplate ($C_{\sigma\text{OUT}}$) and the parasitic capacitance from the gate high side to the ground ($C_{\sigma\text{GH}}$) are key to consider as both are charged and discharged during turn-off and turn-on, increasing switching losses and risk to cause EMI as explained in [7]. The layout, shown in **Figure E.3**, has been designed to minimize these capacitances. The power module consists of two 1 mm Aluminum Nitride direct bonded copper substrates (DBCs) soldered on a AlSiC baseplate. The layout of the DBCs are mirrored, with each DBC handling two 10 kV 350 mΩ MOSFETs from Wolfspeed in parallel. As the half-bridge

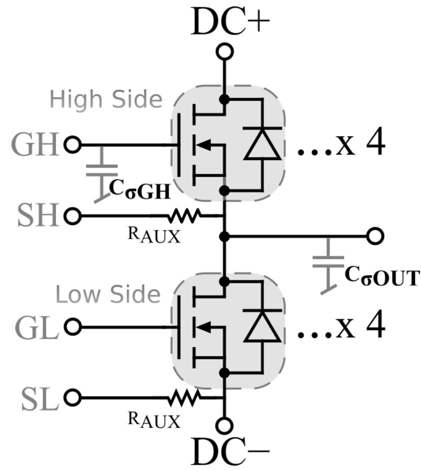

Fig. E.2: Half-bridge topology with 4 MOSFETS in parallel for both high side and low side DC-link connections, highlighting the parasitic capacitances $C_{\sigma\text{OUT}}$ and $C_{\sigma\text{GH}}$ and series resistors used in the auxiliary source connection. σ denotes the baseplate.

consists of a high side and low side this amounts to 4 MOSFETs soldered to each DBC. The clearance between copper areas with differing voltage potential is 2.5 mm and all copper area corners are rounded to a radius of 2.5 mm to minimize the strength of electric fields inside the power module. In the middle of each DBC there is an additional small DBC soldered on top, to reduce parasitic capacitance from the output plane to the baseplate, which the output terminal feet are welded on. Some of the output copper area is still on the bottom DBC as the low side MOSFETs placed on the output copper area require a low thermal impedance to the baseplate for efficient heat transfer.

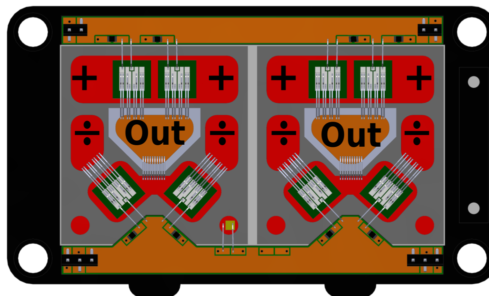

Fig. E.3: DBC-Layout of the power module. Red areas are copper on the bottom DBCs. Symbols indicate copper terminal feet placement. The outer black area is the ABS support structure for the PCBs.

The gate-tracks are made using 4-layer PCBs which are placed 2.5 mm above

the baseplate on a 3D printed ABS support that surrounds the bottom DBCs. The PCBs have the benefit of providing low effective parasitic inductance in the gate-loop, mitigating current imbalance in the power loop. The gate loop consists of a gate connection and auxiliary source connection to the MOSFETs. Some coupling between the power loop and the gate loop is still present through the auxiliary source connections between individual MOSFETs, however 1 Ω series resistors are placed at each auxiliary source connection to minimize the coupling between the gate loop and power loop as explained in [8]. The external connections are handled by copper terminals with two for each DC-link connection and one for the output. For the gate driver connection surface mounted header pins are used on the gate track PCBs. The copper terminal feet placement are shown in **Figure E.3** with symbols and the designs of the terminals are shown in **Figure E.4** on a manufactured power module.

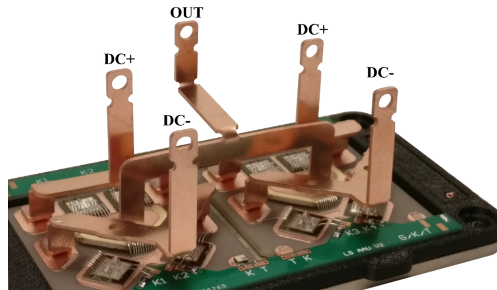

Fig. E.4: Picture of power module prior to potting, showing the symmetrical copper terminal design.

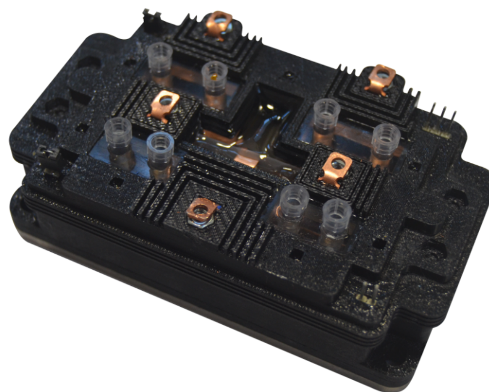

Fig. E.5: Picture of finished power module showing external connections.

The terminals were designed so that each parallel die should have close to identical impedance power loops. The power module was potted in a silicone

gel with a dielectric strength of at least 23 kV/mm. The housing was made by 3D printing ABS. The complete module is shown in **Figure E.5** filling an area of 104 x 59 mm^2. The clearance in air is more than 22 mm between each different terminal connection.

E.4 Parasitics and Simulation

The design of the power module was optimized based on parasitic extraction in ANSYS Q3D. An equivalent circuit with the key parasitics is shown in **Figure E.6** and their values are reported in **Table E.1**. The parasitic capacitances to the baseplate extracted for the table are the high side plane capacitance ($C_{\sigma \mathrm{DC+}}$), the high side gate capacitance ($C_{\sigma \mathrm{GH}}$), the output plane capacitance ($C_{\sigma \mathrm{OUT}}$), the low side gate capacitance ($C_{\sigma \mathrm{GL}}$), and the low side plane capacitance ($C_{\sigma \mathrm{DC-}}$). As mentioned the most important ones to discuss are $C_{\sigma \mathrm{OUT}}$ and $C_{\sigma \mathrm{GH}}$. The loss related to these parasitic capacitances are twofold. Firstly the loss associated with charging them will be $\frac{1}{2} \cdot (8.5 + 56)$ pF $\cdot V^2$, which e.g. for 6000 V will be 1.2 mJ and is dissipated in the MOSFET. Secondly the current from these capacitances will run through the MOSFET channels increasing the Miller plateau voltage, in turn lowering the dv/dt of the switching event as explained in [7].

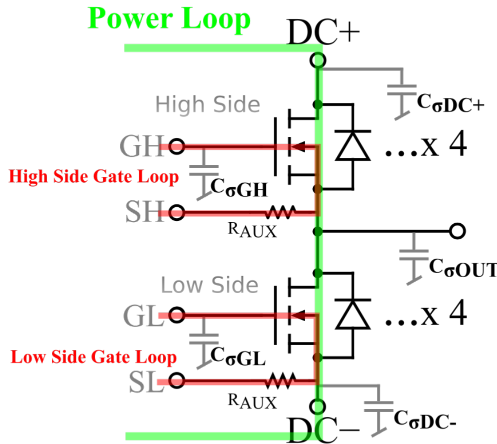

Fig. E.6: Finished power module showing external connections.

The parasitic inductances extracted are the power loop from the DC+ terminals to the DC- terminals, the gate loop through the closest MOSFET die, and the gate loop through the furthest MOSFET die relative to the gate pin. From simulations, the gate loop asymmetry does not give significant gate signal phase difference between the MOSFETs, assuming identical MOSFET characteristics for all dies.

Parasitic Capacitances to baseplate	
$C_{\sigma DC+}$	62.3 [pF]
$C_{\sigma GH}$	8.5 [pF]
$C_{\sigma OUT}$	56 [pF]
$C_{\sigma GL}$	11.3 [pF]
$C_{\sigma DC-}$	30.4 [pF]
Parasitic Loop Inductances	
Powerloop	21.15 [nH]
$\text{Gateloop}_{\text{close}}$	29 [nH]
$\text{Gateloop}_{\text{far}}$	31 [nH]

Table E.1: Key parasitics extracted from ANSYS Q3D.

E.5 Double Pulse Setup

In order to obtain switching losses for the power module a double pulse setup is made as shown in **Figure E.7**. The low side of the power module is used as the device under test, while the high side is used for freewheeling. A 47 mH air-core inductor with a parasitic capacitance of 12 pF is used as the load inductor and the DC-link consists of two 5 kV 50 µF capacitors parallel connected. The current through the low side MOSFETs is measured using a 25 mΩ current shunt resistor, while the voltage across the low side MOSFETs is measured using a PPE 20 kV high voltage probe from Lecroy. The DC-power supply is a XR10000-0.20/240SPNEG+LXI from Magna Power which is negatively grounded. The power module is fastened to a metal plate, which is connected to the ground of the DC-link via a wire. A 2878 Pearson current monitor is attached to this wire connection in order to monitor the ground current during switching events. A HVFO103 differential probe from Lecroy is used to measure the gate-source signal of the low side gate driver. The gate driver used is custom-built and utilizes a transformer with 1.2 pF isolation capacitance to avoid false turn-on, which is described in [9]-[10]. The external gate-resistance is 8.25 Ω. The high side gate is kept low with a -5 V drive voltage, while the low side gate is switched with 20 V and -5 V corresponding to the positive and negative drive voltage of the SiC MOSFET, respectively.

E.6 Experimental Results and discussion

The low side was tested from 1 kV to 6 kV in steps of 1 kV from 8 A to 56 A in steps of 8 A. The power module was not tested to higher voltages due to the voltage rating of the DC-link capacitors used for the double pulse tests, which were already only rated for 5 kV. The second turn-on event and first turn-off event for 6 kV, 8 A is shown in **Figure E.8**. The second turn-on event

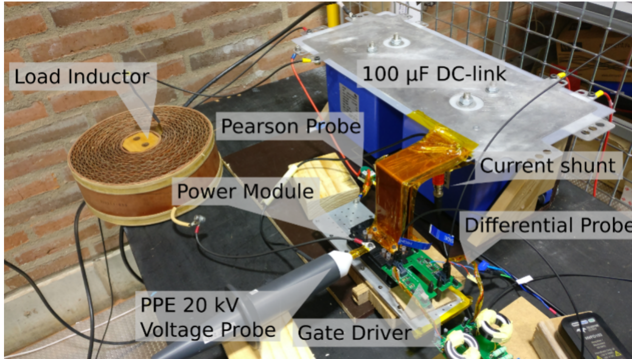

Fig. E.7: Picture of the double pulse setup.

took approximately 310 ns with a dv/dt from 90% to 10% output voltage of 41.4 kV/µs. The peak current was 27.3 A, related to the charging of the drain-source capacitances of the high side MOSFETs, together with the discharging of $C_{\sigma GHS}$ and $C_{\sigma OUT}$. The current ripple after the event is mainly caused by the parasitic capacitances to the grounded baseplate. The first turn-off event took approximately 500 ns with a dv/dt of 15.15 kV/µs.

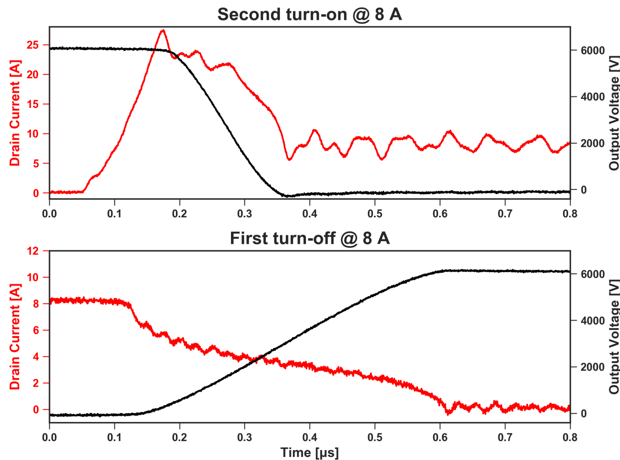

Fig. E.8: 2nd turn-on and 1st turn-off events for the double pulse test at 6000V, 8 A.

In **Figure E.9** the second turn-on and first turn-off events are shown for 6 kV, 56 A. Here the second turn-on is the slowest event at 499 ns and a dv/dt of 29.9 kV/µs. The first turn-off is the fastest event of all tests occurring in 118 ns with a dv/dt of 74 kV/µs. The ringings after the first turn-off event have a negative peak current of 14 A.

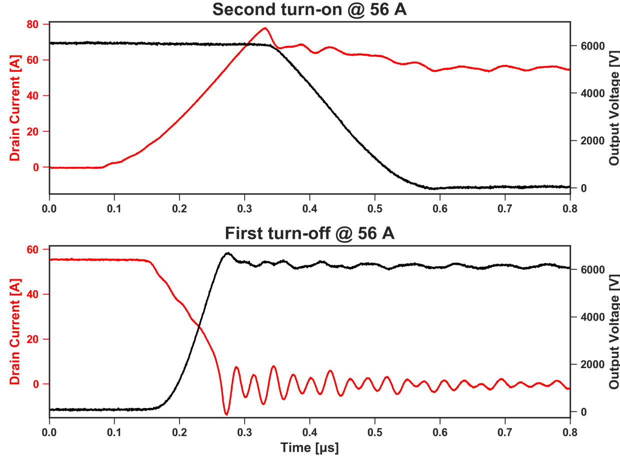

Fig. E.9: 2nd turn-on and 1st turn-off events for the double pulse test at 6000V, 56 A.

The gate-source voltage for the low side and the ground current through the baseplate was also measured in the double pulse tests and are shown in **Figure E.10** and **Figure E.11**. The ground current oscillation is around 16 MHz, however this will change with the wire type and length used for grounding the baseplate. The peak amplitude is determined by the capacitance to the baseplate and the $\mathrm{d}v/\mathrm{d}t$ of the switching event. For 6 kV, 8 A the peak ground current is 4 A for second turn-on and 1 A for first turn-off. The largest ground current peak is 50% of the total load current, however there is little impact on the gate-source voltage. For 6 kV, 56 A the peak ground current is 3.7 A for second turn-on and 6.5 A for first turn-off. The largest ground current peak is only 10% of the total load current and has little impact on the gate-source voltage. In order to compare the power module switching speed with other similar 10 kV power modules based on the same MOSFETs it is proper to account for varying die count and gate resistance. This is done by analyzing an equivalent circuit for a single-chip gate loop and a multi-chip gate loop shown in **Figure E.12**. The multi-chip gate loop may have auxiliary series resistances on the source side, however this can be included in the total external gate-resistance in calculations for this equivalent circuit. The circuit is valid for a turn-on event and holds until the Miller plateau is reached. At the beginning of the turn-on event the gate is at V_{low}. The gate driver will then charge the gate-source capacitance to the Miller plateau from the low signal which is described by

$$V_{\mathrm{Miller}} - V_{\mathrm{low}} = (V_{\mathrm{high}} - V_{\mathrm{low}}) \cdot \left(1 - e^{\frac{-t}{R_g C_{\mathrm{gs}}}}\right), \tag{E.3}$$

with V_{high} and V_{low} being the high and low driving voltage supplied from the gate driver, respectively. The time to charge the capacitor to the Miller plateau

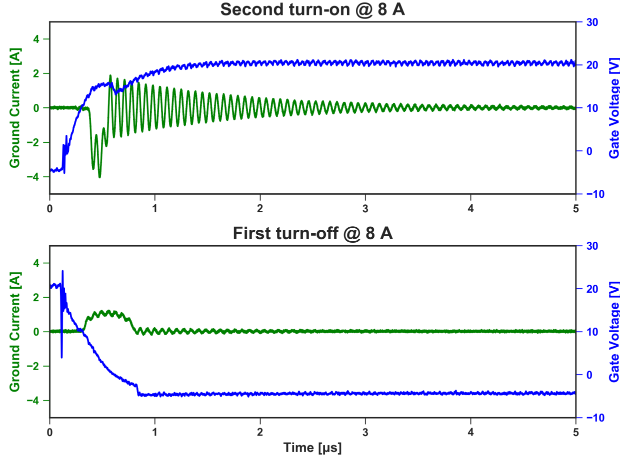

Fig. E.10: 2nd turn-on and 1st turn-off events for the double pulse test at 6 kV, 8 A.

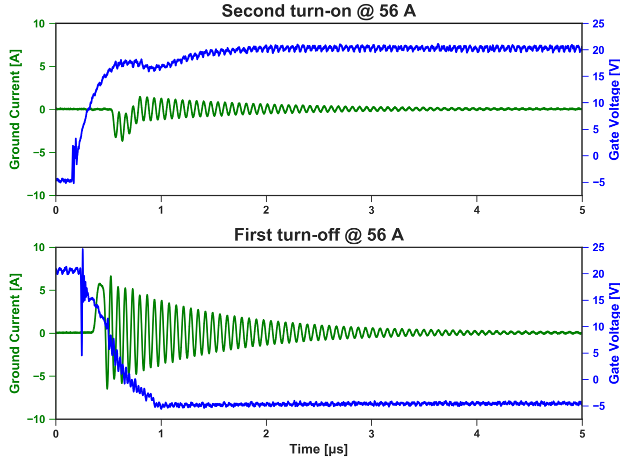

Fig. E.11: 2nd turn-on and 1st turn-off events for the double pulse test at 6 kV, 56 A.

is then

$$t = -\ln\left(1 - \frac{V_{\text{Miller}} - V_{\text{low}}}{V_{\text{high}} - V_{\text{low}}}\right) \cdot R_g C_{\text{gs}}. \tag{E.4}$$

As the time to charge the gate-source capacitor to a given Miller plateau is directly proportional to the gate-source capacitor and the gate resistance it is understood that to achieve the same charging speed to the Miller plateau for a power module with 4 of the same MOSFETs in parallel the gate-source capacitance of the gate-loop is 4 times higher. Thus in order to compensate for this an "equivalent" resistance for the same charging speed to the same Miller

plateau would be 4 times lower. Thus, the gate resistance and the number of dies can be compensated for when comparing different power modules using the same dies. The 10 kV, 80 A power module was double pulse tested using a 8.25 Ω external gate resistance and 1 Ω auxiliary source series resistances for each MOSFET, meaning a total external gate loop resistance of 8.5 Ω. A

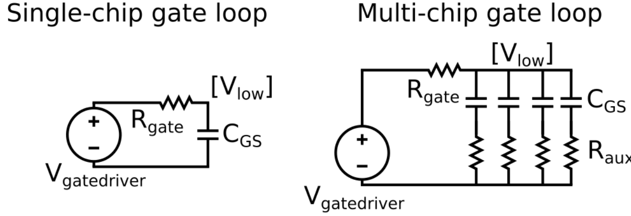

Fig. E.12: Equivalent circuits for the charging of the gate-source capacitance of the MOSFETs in single-chip and multi-chip gate loops. Bracket voltages indicate initial conditions for the nearby node.

comparison can then be made with a single-chip 10 kV, 20 A power module using the same MOSFETs as described in [7]. The single-chip power module was double pulse tested using a 20 Ω gate resistance. Equivalently, that test would correspond to using a 5 Ω total external gate resistance on the multi-chip power module, indicating that for the same Miller plateau or current running through the individual MOSFET channel the single-chip power module should be switching faster. The second turn-on $\mathrm{d}v/\mathrm{d}t$ found in [7] is approximately 28 kV/µs for 2 A and 16 kV/µs for 14 A. These load currents correspond to the pr. die load current of the multi-chip power module for the 8 A and 56 A tests and thus if only the load current was going through the MOSFET channels the Miller plateau and charging time should be the same, assuming no die variation. However, as reported the $\mathrm{d}v/\mathrm{d}t$ for the multi-chip power module is double even for a equivalent total external gate resistance that is larger by more than 50%. The reason behind this is found in the parasitic capacitance to the baseplate and the anti-parallel JBS diode placed in the single-chip power module. The JBS diode junction capacitance will contribute to a higher Miller plateau the same way as the output capacitance of the MOSFETs by increasing the current going through the MOSFET during turn-on. The parasitic capacitance to the baseplate of the single-chip power module is 93.8 pF which is approximately 45% larger than the multi-chip power module parasitic capacitance. Additionally as there are four MOSFETs in parallel each channel will only take 1/4 of the current originating from these capacitances during switching events further lowering the impact. Capacitance to the baseplate per die in the multi-chip power module is 16.13 pF, almost 6 times smaller than the same capacitance in the single-chip power module. The total switching losses are the total energy dissipated during first turn-off and second turn-on in the MOSFETs of the low side, and can be

seen in **Figure E.13**. For 6 kV, 56 A the switching losses amount to 96.7 mJ. The losses would be smaller if using a smaller external gate-resistance, however this will lead to even higher $\mathrm{d}v/\mathrm{d}t$, which may cause EMI issues for systems connected to the power module. Comparing with the single-chip power module the losses in the multi-chip power module are approximately 33% lower for 6 kV, 14 A load current per MOSFET, leading to more efficient switching.

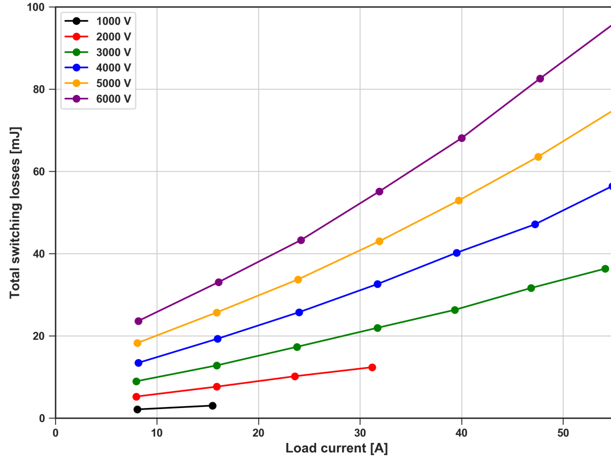

Fig. E.13: Switching losses as a function of load current.

E.7 Conclusion

A 10 kV, 80 A multi-chip power module based on the half-bridge topology with four 10 kV, 20 A MOSFETs in parallel has been presented together with an argument for changing the design focus towards minimizing parasitic capacitances when designing for medium voltage power modules due to the stored energy ratio of the parasitic capacitances and inductances in this voltage and current rating. The power module has been investigated using double pulse tests from 1 kV to 6 kV and 8 A to 56 A. A comparison with a single-chip 10 kV power module is made, showing greater switching speeds and lower switching losses for the multi-chip power module due to the emphasis on minimizing parasitic capacitances and not including JBS diodes in anti-parallel with the MOSFETs.

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