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An On-line Calibration Method for TSEP-based Junction Temperature Estimation

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Yingzhou Peng, *Member, IEEE*, Qian Wang, *Member, IEEE*, Haoran Wang, *Member, IEEE*, Huai Wang, *Senior Member, IEEE*

Abstract—**Temperature Sensitive Electrical Parameters (TSEP) provide an indirect and non-invasive method for on-line junction temperature estimation of power semiconductor devices. It is known that the fundamental of TSEP-based methods is to calibrate the relationship between TSEP and junction temperature in advance. However, the calibration methods in the literature need to open the module, require pre-testing, or record the operating data of a converter in the entire power rating range, which are inconvenient in field applications. This paper proposes an on-line and non-invasive calibration method by measuring the data at three operating states that are already existed in the regular converter operation. It is achieved by measuring the accessible heatsink/case temperature and TSEP during converter regular operation. The concept, implementation, and error analysis of the proposed method are presented in this paper. Experimental verification is given to prove the effectiveness, accuracy, and convenience of the proposed method.**

Index terms— Power semiconductor, junction temperature, condition monitoring, power converter.

I. INTRODUCTION

The junction temperature of power semiconductors T_j is a critical parameter for the lifetime prediction, condition monitoring, and optimal operation of power electronic systems. [1, 2]. Extensive efforts have been made to junction temperature estimation in the last two decades.

One of the primary ways is to estimate the T_j indirectly by measuring TSEPs, such as the on-state voltage [3–5], change rate of collector-emitter voltage [6], base-collector voltage drop [7], switching time [8, 9], gate peak current [10, 11], pre/threshold voltage [12], miller plateau in gate voltage [13], and Kelvin power emitter voltage [14, 15], etc. If the relationship between T_j and TSEPs is calibrated in advance as shown in Fig.1, finding the relationship curve between T_j and TSEPs, T_j can, thereafter, be estimated easily by measuring TSEPs in real-time. Therefore, for all TSEP-based methods, the specific calibration is a critical and fundamental step. Depending on the implementation features, the existing calibration methods can be classified into three categories as shown in Fig.2.

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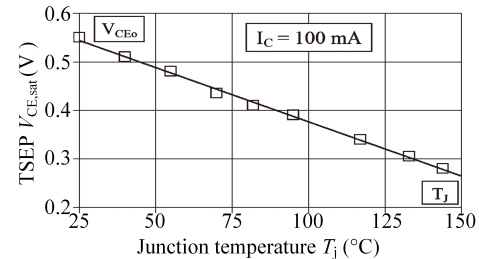

Fig. 1. Calibration between TSEP and junction temperature [16].

1) Invasive calibration during lab testing: The first group of methods is off-line calibration. It measures the T_j directly by thermal camera or optical fiber for an open-module, and the TSEP [10, 17] to realize calibration. The direct measurement enables high accuracy. However, it is an invasive method.

2) Non-invasive calibration with pre-testing: The second group of methods is performed before the running period of power converter and does not need to open the power module. They can be further divided into two subgroups: 1) the power module that is not assembled into a power converter yet is placed in a thermostat or on a heat plate to achieve different temperature-levels [9, 11, 18]. Then, the device under test (DUT) is controlled to operate at low-power mode by conducting low-current (e.g., 100 mA) or high-current with short-period (e.g., 100 μs), so that the T_j can be assumed to equal to the case/heatsink temperature. Consequently. the calibration can be finished by fitting the obtained multiple points of T_j and TSEP; 2) when the power converter is assembled and ready to operate, it's control is modified intentionally to operate converter at low-power mode. To exclude the heat plate, the different temperature-levels can be realized by intentionally changing the cooling conditions [19]. Another one presented in [20] realizes the calibration by managing the power converter to operate under a specific mission profile that includes wide power rating range (e.g., 0.1-0.9 pu), and sufficient heatsink temperature variation (e.g., 5-10 °C) by changing the coolant flow or fan speed. In conclusion, the calibration methods discussed in this group can achieve the estimation error of T_j by less than 10 °C compared to direct measurement or simulation result. However, they need to add or modify controls, and conduct pre-testing before converter is ready to operate. For field applications, there are two concerns. Firstly, there are parameter variances in a population of components of interest, due to tolerance and
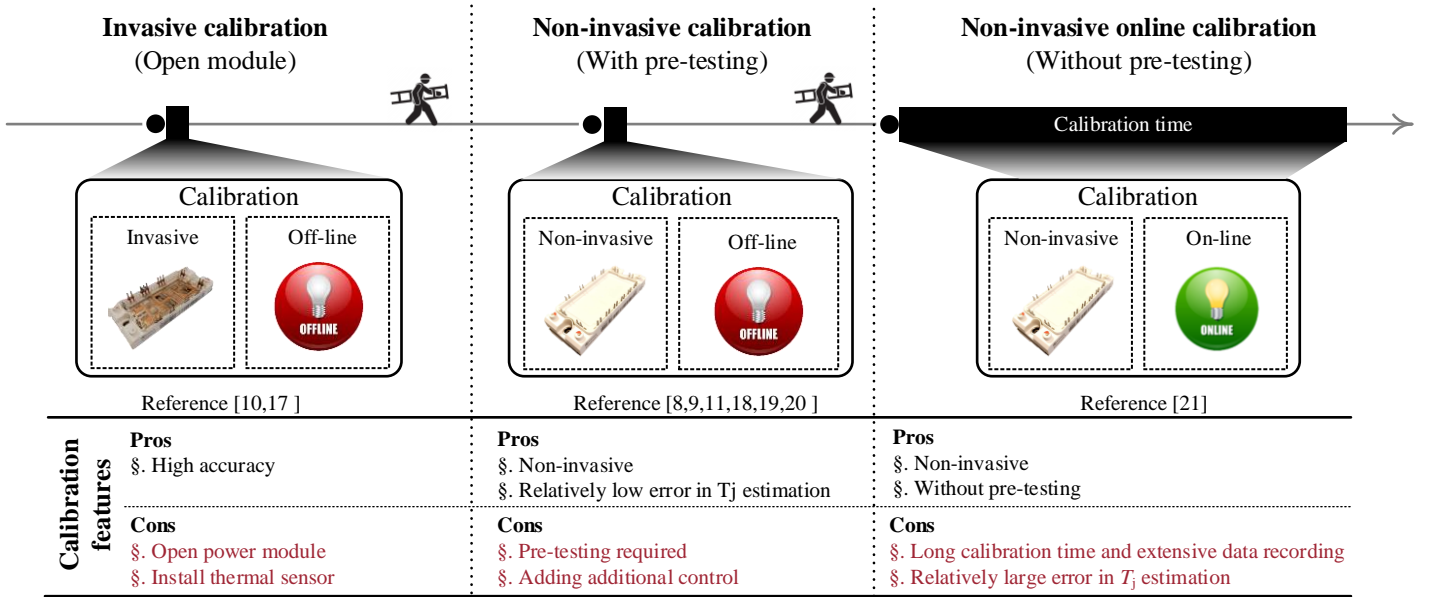
Fig. 2. Implementation comparison of the existing calibration methods.

other sources of uncertainties. Nevertheless, due to the time-consuming process, offline calibrations are usually preformed for a limited number of samples and cannot fully exclude the impact of parameter variances. Secondly, degradation of components will alter the relationship, such as the on-state voltage and junction temperature. It would be a challenge in updating this relationship by offline calibration after components are installed in products.

3) Non-invasive on-line calibration during normal operation: From industry perspective, it would be more acceptable if the calibration is conducted on-line and without adding or modifying original controls of converter. Also, on-line calibration is more practical and effective considering the calibration is required for each power device and once the degradation occurs. The on-line implementation is defined in this paper that the calibration methods utilize the natural operational statuses of converter only and do not add or modify the original control. Based on our best knowledge, there is only one paper that discloses a non-invasive on-line calibration method [21]. It builds a look-up table by logging the on-state voltage of IGBT at the selected sensing current, fundamental current I_{rms}, and the liquid temperature of cooling system T_{l} at the whole power range (e.g., 0.1 to 1.0 p.u.) of converter and with enough heatsink temperature variation (e.g., 10 °C). Then, this look-up table is used to calculate the temperature difference between T_{j} and T_{l}. Since this look-up table is discrete, this method requires long-time measurement and huge data set to cover every potential operational power condition of converter as much as possible. Otherwise, it cannot predict the T_{j} when the converter operates at the power conditions that are not covered by the look-up table. Although it can use the neighboring data to approximately represent the uncovered conditions, which can cause approximate errors. In [21], three-months operation

data-logging is used to finish calibration. Then, the estimated result can sense the change of junction temperature but with a maximum error by 20 °C compared to the simulated result. Overall, this method is non-invasive and can be realized on-line. Its drawbacks are long calibration time and relatively larger error in estimating junction temperature.

Overall, those existing calibration methods have been developed from off-line to on-line. For the one without pre-testing is, however, still facing the challenge that long-time and extensive data measurement are required to cover every potential operation conditions of converter.

This paper proposes an on-line calibration method for TSEPs-based T_{j} estimation by taking advantage of the nature operation of converter. It is realized by measuring a reference temperature (e.g, heatsink temperature T_{h}) and TSEP during the start-up, and two thermal steady-states of a power converter only. By comparing with the existing methods presented in Fig.2, the proposed method shows that: 1) it is an on-line method by leveraging the natural operation statuses of power converter and without conducting pre-testing; 2) it does not need to add or modify controls in the original controller since the required operational statuses of converter are existed naturally; 3) it requires three pairs of TSEP and heatsink temperature only, and can be conducted in a much shorter time compared to the method in [21]; 4) it can achieves comparable accuracy of T_{j} estimation with the methods illustrated in the second group above. Moreover, the proposed method can be performed throughout the service life of power devices in a system to distinguish the impact of degradation. Finally, it should be noted that the mentioned reference temperature can also be the case temperature T_{c}, the NTC temperature T_{NTC} of the power device module, or even the ambient temperature T_{a}, which can be easily achieved.
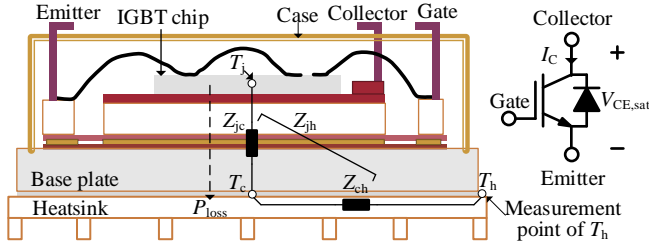
Fig. 3. Structure of IGBT module and its symbol.

The rest of this paper is outlined as follows: the principle and implementation are discussed in Section II. The error analysis and experimental verification are given in Section III, followed by the conclusions.

II. CONCEPT AND IMPLEMENTATION OF THE PROPOSED METHOD

To illustrate the methodology of the proposed calibration method, the on-state voltage is taken as a TSEP example in this paper, since it is a typical and the most widely reported TSEP. For some other TSEPs that are measurable during the start-up and normal operation of converter, and have liner relationship with junction temperature, the calibration can also be realized through the proposed method, such as threshold voltage, switching time, and gate miller plateau voltage.

By taking IGBT as an example, its T_j has a linear relationship with the on-state voltage $V_{CE,sat}$ at a given collector current I_C [2], which can be expressed as:

$$T_j = aV_{CE,sat}(I_C) + b \qquad (1)$$

To estimate T_j in real time through (1), the coefficients a and b have to be obtained in advance. Thus, this paper focuses on the parameterization of a and b by using the information which can be easily measured during the converter operation.

A. Calculation of a

The junction temperature of an IGBT chip is a function of the power loss, thermal resistance, and a reference temperature (e.g., heatsink temperature) at the thermal-steady state [22]. By assuming there are m IGBT chips inside a module, the T_j of the 1st chip can be given by:

$$T_j = \begin{bmatrix} R_{jh,11} & R_{jh,21} & ... & R_{jh,m1} \end{bmatrix} \times \begin{bmatrix} P_{loss,1} \\ P_{loss,2} \\ ... \\ P_{loss,m} \end{bmatrix} + T_h \qquad (2)$$

where $R_{jh,11}$ is the self thermal resistance of the 1st chip from junction to heatsink. $R_{jh,21}$-$R_{jh,m1}$ are the coupled thermal resistance between the 1st chip and other chips. $P_{loss,1}$-$P_{loss,m}$ are the averaged power losses generated by the 1st to mth chips over one fundamental period, respectively.

For an operating power converter, if its fundamental current I_{rms} is fixed and the heatsink temperature T_h is increased from

T_{h1} to T_{h2} by 5-10 °C (in practice, the change of T_h can be realized by one of the possible ways: 1) by fan speed change in forced-air cooling; 2) by coolant speed control in liquid cooling; 3) ambient temperature change), the parameters a and b in (1) can keep in constant at these two temperature-levels. Also, the thermal resistance R_{jh} is assumed as constant at a given degradation level. Then, (1) and (2) can be re-written at these two temperature-levels as:

$$\begin{cases} T_j(T_{h1}) = aV_{CE,sat}(I_C, T_{h1}) + b \\ T_j(T_{h2}) = aV_{CE,sat}(I_C, T_{h2}) + b \end{cases} \qquad (3)$$

$$\begin{cases} T_j(T_{h1}) = \sum_{i=1}^{m}(P_{loss,i}(T_{h1})R_{jh,i1}) + T_{h1} \\ T_j(T_{h2}) = \sum_{i=1}^{m}(P_{loss,i}(T_{h2})R_{jh,i1}) + T_{h2} \end{cases} \qquad (4)$$

Subtracting one equation from another one in (3) and (4), respectively,

$$T_j(T_{h2}) - T_j(T_{h1}) = a(V_{CE,sat}(I_C, T_{h2}) - V_{CE,sat}(I_C, T_{h1})) \qquad (5)$$

$$T_j(T_{h2}) - T_j(T_{h1}) = \sum_{i=1}^{m}((P_{loss,i}(T_{h2}) - P_{loss,i}(T_{h1}))R_{jh,i1}) \\ + T_{h2} - T_{h1} \qquad (6)$$

Then, dividing (5) and (6) by $\Delta V_{CE,sat}(I_C)$ (i.e., $V_{CE,sat}(I_C, T_{h2}) - V_{CE,sat}(I_C, T_{h1})$),

$$\begin{cases} \dfrac{\Delta T_j}{\Delta V_{CE,sat}(I_C)} = a \\ \dfrac{\Delta T_j}{\Delta V_{CE,sat}(I_C)} = \dfrac{\sum_{i=1}^{m}(\Delta P_{loss,i}R_{jh,i1})}{\Delta V_{CE,sat}(I_C)} + \dfrac{\Delta T_h}{\Delta V_{CE,sat}(I_C)} \end{cases} \qquad (7)$$

where ΔT_j is $T_j(T_{h2}) - T_j(T_{h1})$, ΔT_h is T_{h2}-T_{h1}, and $\sum_{i=1}^{m}\Delta P_{loss,i}$ is $\sum_{i=1}^{m}P_{loss,i}(T_{h2}) - \sum_{i=1}^{m}P_{loss,i}(T_{h1})$.

If I_{rms} is unchanged and T_h is increased by ΔT_h, the increase of power losses ΔP_{loss} is only due to the change of T_h, which could be a relatively low value. Moreover, the thermal resistance R_{jh} is usually less than 1 and is unchanged if the solder layer is not degraded. As a results, $\sum_{i=1}^{m}(\Delta P_{loss,i}R_{jh,i1})$ is far less than ΔT_h in (7) [21], a can be given as:

$$a = \frac{\Delta T_j}{\Delta V_{CE,sat}(I_C)} \approx \frac{\Delta T_h}{\Delta V_{CE,sat}(I_C)} \qquad (8)$$

In this paper, (8) is verified with a case study later (Section III, Part C). It should be noted that it does not require frequent calibration, e.g., once per month or year could be sufficient. Therefore, it expects to introduce negligible disturbance in converter operation to have 5-10 °C change of T_h during the calibration process even by intentionally change the cooling.

Overall, if the $V_{CE,sat}$ at a given I_C, and the T_h are measured at two heatsink temperature levels, a can be calculated by:

$$a = \frac{T_{h2} - T_{h1}}{V_{CE,sat}(I_C, T_{h2}) - V_{CE,sat}(I_C, T_{h1})} \qquad (9)$$
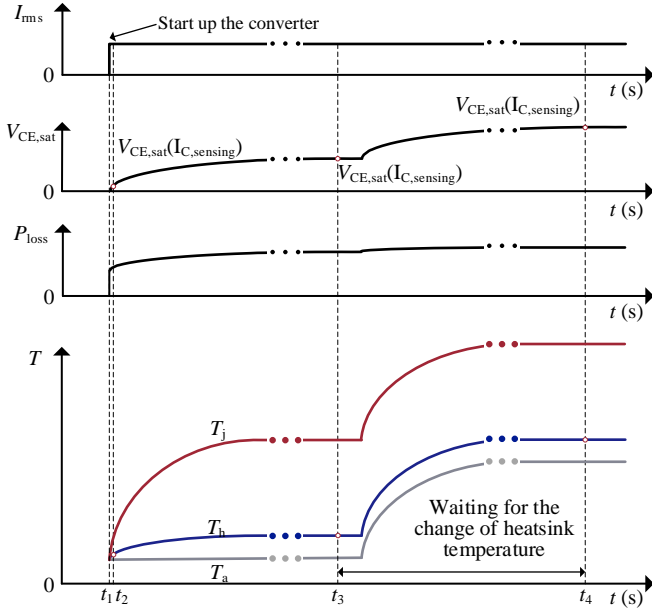
Fig. 4. Time sequence of implementing the proposed method.

TABLE I
SPECIFICATIONS OF THE SINGLE-PHASE INVERTER IN THE CASE STUDY

Parameters	Value	Parameters	Value
V_{dc}	400 V	R	10 Ω
$I_{L,pk}$	20 A	L	2 mH
f_{sw}	10 kHz	Dead time	2 μs
$I_{C,sensing}$	(5-5.1) A	Module	F4-50R12KS4

C. Implementation process

To clarify the implementation process of the proposed method, the time sequence is depicted in Fig.4, including three stages:

1) Stage 1 [t_1-t_2]: During the start up, the $V_{CE,sat}$ is recorded when I_C reaches the given sensing current $I_{C,sensing}$ at the first time, and the corresponding T_h as well. The time duration of this stage is less than a quarter fundamental period (e.g., 5 ms). The data obtained in Stage 1 are used for calculating the value of b once a is obtained in the Stage 3 discussed later.

2) Stage 2 [t_2-t_3]: Thereafter, the converter arrives at thermal steady-state at t_3. Then, the corresponding $V_{CE,sat}$ at the given sensing current, and T_h are recorded again. This stage duration depends on the thermal response of the applied power module and the specific installation, which may last for up to several minutes. The thermal steady-state is determined when the T_h is not increased and keeps the variation at a certain range.

3) Stage 3 [t_3-t_4]: Finally, the another thermal steady-state at the same I_{rms} can be obtained by waiting for the change of ambient temperature for 5-10 °C. Then, the corresponding $V_{CE,sat}$ at the given sensing current, and T_h are recorded again. This stage may last for one day in field applications. The data recorded in stage 2 and 3 are used to calculate a through (9). There is a requirement that the I_{rms} of inverter must be same only at t_3 and t_4.

B. Calculation of b

Once a is obtained, b can be calculated by substituting one pair of T_j and $V_{CE,sat}$ into (1). At the beginning of the start-up of converter, T_j can be assumed to equal to T_h since they have negligible difference, which can be explained by the following analyses.

Based on Foster thermal network [23], at the start-up transient, the thermal resistance in (2) is replaced with the transient thermal impedance. Then, the T_j with response to the P_{loss} is:

$$T_j = \begin{bmatrix} R_{jh,11}(1 - e^{-t/\tau_{11}}) \\ R_{jh,21}(1 - e^{-t/\tau_{21}}) \\ ... \\ R_{jh,m1}(1 - e^{-t/\tau_{m1}}) \end{bmatrix}^T \times \begin{bmatrix} P_{loss,1} \\ P_{loss,2} \\ ... \\ P_{loss,m} \end{bmatrix} + T_h \qquad (10)$$

where τ_{11} are the self time constant of the chip to be tested at the ith order. τ_{21}-τ_{m1} are the coupled time constants between the tested chip and other chips at the ith order. During the start-up of a power converter, t is a low value (e.g., 20 ms), which means the first term on the right side of (6) can be low enough to lead to a negligible difference between the T_j and T_h, compared to T_h. Therefore, b can be calculated by substituting one pair of T_h and $V_{CE,sat}$ measured at the early stage of the start-up into (1). It should be noted that measuring $V_{CE,sat}$ as earlier as possible during the start-up could limit the error since a lower $R_{jh,m1}(1-e^{-t/\tau_{m1}})$ can be obtained. It should be noted that since the first term on the right side of (6) is neglected, the thermal network does not affect the accuracy of the proposed method no matter it is first-order or nth-order.

III. APPLICATION OF THE PROPOSED METHOD FOR THE IGBT IN A SINGLE-PHASE INVERTER

To verify the feasibility of the proposed method, a single-phase inverter setup is built by using the IGBT module F4-50R12KS4, as shown in Fig.5(a), along with its hardware realization in Fig.5(b). A heatsink temperature point is selected as the reference temperature in this case study as shown in Fig.5(b). It should be noted that for the converter with four to six power modules that are placed onto a same heatsink, the changes of their heatsink temperature may be different and cannot be represented with the heatsink temperature at one point. To address this potential issue, the reference temperature of each module should be selected and measured individually. Based on the theoretical analysis above, it is seen that the feasibility of the proposed method is component-dependent and application-dependent. It has two requirements: 1) the selected TSEP has linear relationship with the junction temperature of semiconductor switch component and is measurable during

start-up of converter; 2) the application should have a start-up event and at least two different heatsink temperature-levels when power converter is in normal operation. And two assumptions: 1) at the early stage of start-up transient of power converter, the junction temperature of power device is assumed to equal to a reference temperature (e.g., T_h, T_c, or T_{NTC}); 2) if the fundamental current I_{rms} is constant, the change of the selected reference voltage caused by the change of ambient temperature is assumed to equal to the change of junction temperature. It can be seen that the mentioned requirements and assumptions are mainly related to specific application, instead of topology and control. Hence, upon the component and application aspect conditions are met, the method expect to be feasible.

The device under test (DUT) in this case study is T1 and its on-state voltage $V_{CE,sat}$ is measured on-line through a circuit that is capable of extracting the low on-state voltage (e.g., up to few Volts) from the high DC-link voltage (e.g., up to kV-level) with the resolution in mV-level, which is detailed in [24, 25]. The specifications are shown in Table I. V_{dc} is the DC-link voltage; $I_{L,pk}$ is the peak value of inductor current; f_{sw} is the switching frequency; $I_{C,sensing}$ is the collector-emitter current of IGBT while measuring $V_{CE,sat}$ in this paper; L and R are the filter inductor and load, respectively. The module is mounted on a forced-air heatsink and T_h is measured by a K type thermocouple with 0.1 °C resolution. For the comparative study, the plastic case of the IGBT module is removed as shown in Fig.6(a). An optical fiber temperature sensor (OTG-F type from OPsens) is used to measure the T_j of DUT directly as shown in Fig.6(b). Its response time and resolution are 5 ms and 0.05 °C, respectively.

It is reported that the temperature distribution on the surface of the chip is uneven and usually the temperature at the center is higher than that at the edge [22]. To investigate it, two testing points are selected to measure the T_j while the inverter is in operation as shown in Fig.6(c). When the T_h is 40 °C, the temperature at the center point and edge point are 51 °C and 49 °C, respectively. This temperature difference should be considered during the accuracy analysis of the proposed method. In the rest of this paper, the measurement point of T_j with the optic sensor is at the center of chip surface.

A. Experimental calibration procedure

Firstly, It should be noted that I_C is unaccessible in practical applications and the measured current may not keep at a certain value at every measurement with the 10 kHz sampling frequency. However, the I_C of T1, for example, is same with the inductor current I_L when T1 is in conduction state. Thus, instant I_L is used and measured to replace I_C in this paper. Secondly, measuring $V_{CE,sat}$ at a fixed current may be impractical. Thus, a small range is selected for the case study in this paper and the selection principle of sensing current is discussed in Section III, Part D. The implementation of the proposed method is given in Fig.7, which can be programmed as an auto self-calibration process as listed below:
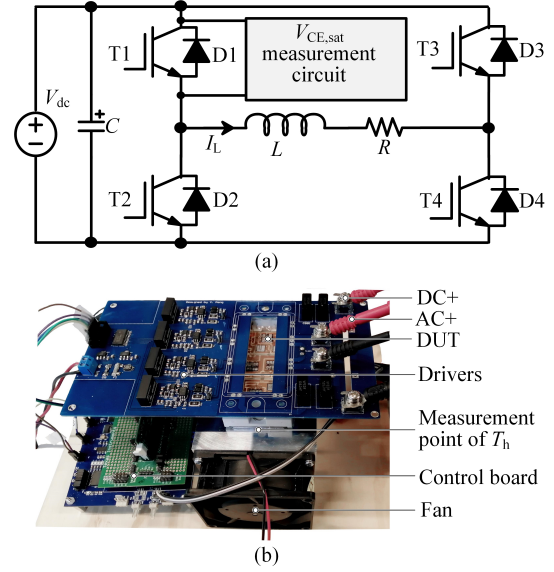

Fig. 5. Experimental setup: (1) topology; (2) hardware (the $V_{CE,sat}$ measurement circuit is connected to the collector and emitter of the DUT).
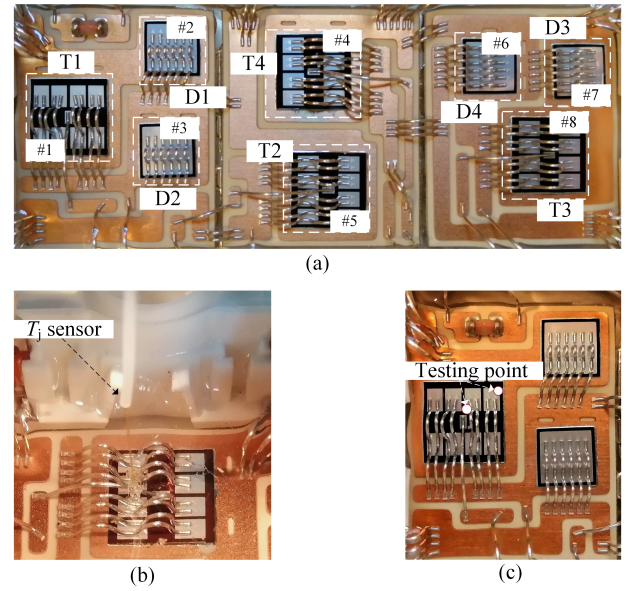

Fig. 6. Layout of the applied IGBT module: (a) marked number of chips; (b) implementation of the optical fiber temperature sensor; (c) junction temperature measuring point.

1) Step 1: Once the start-up of inverter occurs as shown in Fig.8(a), the T_j is recored by the applied optic fiber temperature sensor as shown in Fig.8(b), indicating that T_j is increased from T_h (40.5 °C) to 52 °C after the start-up for 7 s. Also, in this case study, the time duration from the start-up to the thermal steady-state is less than 100 s. Based on the zoom-in figure of Fig.8(b), if $V_{CE,sat}$ is measured at the first fundamental period (20 ms), assuming T_h is equal to T_j causes the error by 0.8 °C only. In this case study, the $V_{CE,sat}$ when I_L is within (5, 5.1) A is measured at every fundamental period

from the start-up of inverter as shown in Fig.9 and only the first point is used. Besides, it is worth noticing that the start-up is performed for six times at the same condition to verify the repeatability of the proposed method. The values of $V_{\mathrm{CE,sat}}$ of the six measurements are plotted in the zoom-in figure of Fig.9. To investigate the fluctuation caused by these measurements, both the highest one (1.742 V) and lowest one (1.738 V) are used to calculate b later;

2) Step 2: After the inverter reaches the thermal steady-state, T_{h} and $V_{\mathrm{CE,sat}}$ are measured when I_{L} is within (5, 5.1) A as T_{h1} and $V_{\mathrm{CE,sat}}(I_{\mathrm{C}}, T_{\mathrm{h1}})$, respectively. It is worth mentioning that the thermal steady-state in this case study is determined when the variation of T_{h} is less than $\pm 0.3°\mathrm{C}$ based on experimental testing.

3) Step 3: Then, the fan speed of cooling is reduced and T_{h} reaches the second thermal steady-state. The T_{h} and $V_{\mathrm{CE,sat}}$ are measured again as T_{h2} and $V_{\mathrm{CE,sat}}(I_{\mathrm{C}}, T_{\mathrm{h2}})$, respectively. The experimental results of Step 2 and Step 3 are shown in Fig.10, indicating that T_{h} and T_{j} are increased by 21 °C and 21.5 °C, respectively. As a result, T_{jh} is increased from 10.2 °C to 10.7 °C, implying a negligible dT_{jh}. The change of T_{h} is about 21 °C in this case study, which is enough due to the high linearity between temperature and TSEP, and has also been verified in [19–21]

4) Step 4: By substituting the measured T_{h1}, T_{h2} and $V_{\mathrm{CE,sat}}(I_{\mathrm{C}}, T_{\mathrm{h1}})$, $V_{\mathrm{CE,sat}}(I_{\mathrm{C}}, T_{\mathrm{h2}})$ into (5), a is obtained as shown in Fig.11 (411.8 °C/V). The negligible difference between $dT_{\mathrm{h}}/dV_{\mathrm{CE,sat}}$ and $dT_{\mathrm{j}}/dV_{\mathrm{CE,sat}}$ verifies that it is reasonable to neglect the term $d\sum_{i=1}^{m}(P_{\mathrm{loss,i}}Z_{\mathrm{jh,i1}})/dT_{\mathrm{h}}$ in (3).

5) Step 5: Based on the calculated a, measured T_{h} at the step 1, and (1), two of the measured $V_{\mathrm{CE,sat}}$ in Fig.9 (1.738 V and 1.742 V) are used to calculate b, which are -675.2 (b_1) and -676.9 (b_2), respectively.

Finally, through the proposed method, the relationship between T_{j} and the $V_{\mathrm{CE,sat}}$ under a given $I_{\mathrm{C,sensing}}$ are calibrated as:

$$T_{\mathrm{j}} = 411.8 \times V_{\mathrm{CE,sat}}(I_{\mathrm{C,sensing}}) - 675.2 \qquad (11)$$

and

$$T_{\mathrm{j}} = 411.8 \times V_{\mathrm{CE,sat}}(I_{\mathrm{C,sensing}}) - 676.9 \qquad (12)$$

B. On-line estimation of T_j with the proposed calibration

Once a and b are calibrated as (11) and (12) in this case study, the T_{j} of the DUT can be estimated. For the comparison purpose, T_{j} is also measured directly by the optical fiber thermal sensor. The operating condition is changed by turning on and off the fan of the forced-air cooling manually. Meanwhile, $V_{\mathrm{CE,sat}}$ of DUT is measured when I_{L} is within 5 A and 5.1 A, and transformed into T_{j} through (11) and (12), respectively, as shown in Fig.12. It can be seen that most of the errors between the results from the optical fiber temperature sensor and the proposed method with a and b_1 are within absolute 2 °C, and with a and b_2 are within absolute 4 °C, which is mainly caused by: 1) assuming T_{j} is equal to T_{h} while calculating b; 2) the measurement of I_{L} is within a small range, leading to
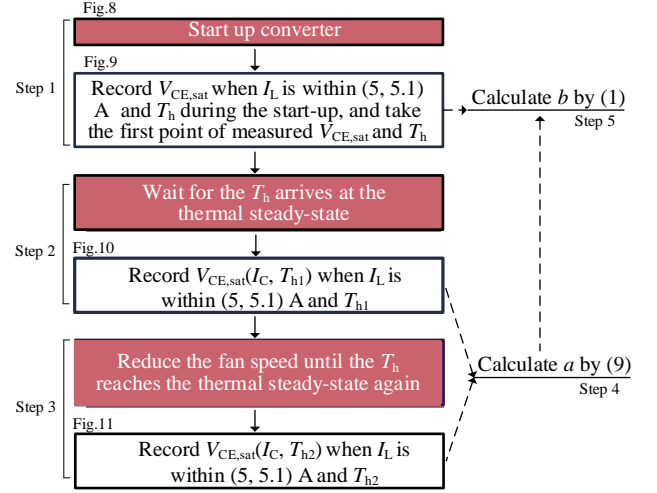

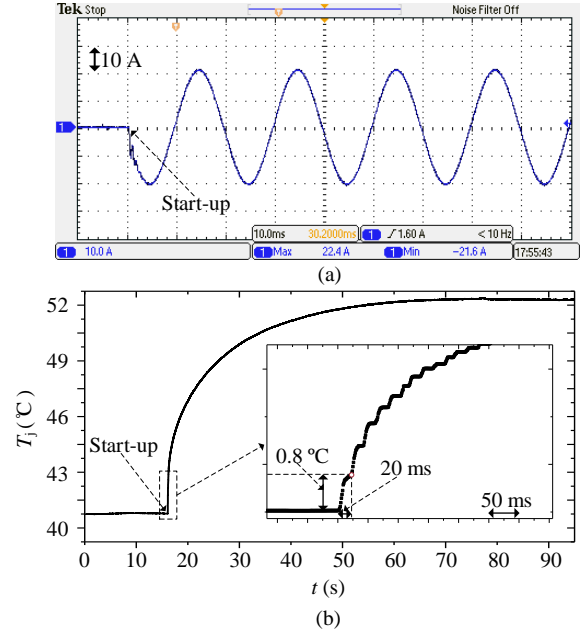Fig. 7. Implementation process of the proposed method.

Fig. 8. Start-up of the inverter: (a) Inductor current of converter I_{L}; (b) Measured T_{j} with 1 kHz sampling frequency.
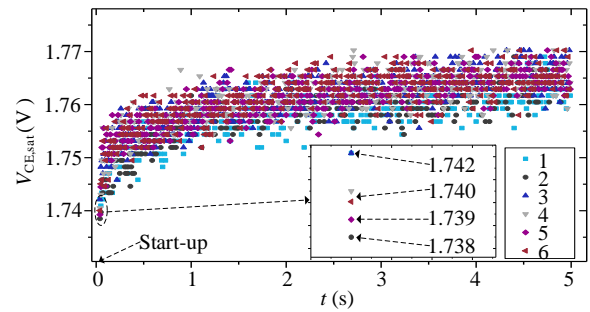

Fig. 9. Measured $V_{\mathrm{CE,sat}}$ when I_{L} is within (5, 5.05) A after the start-up for six times.
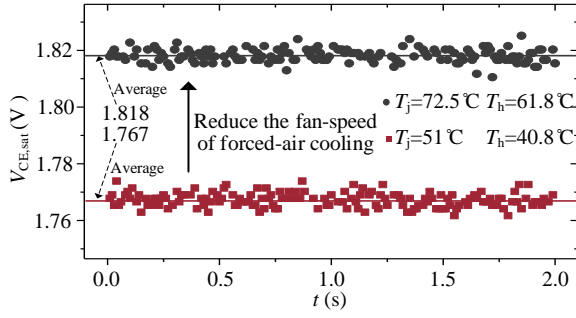
Fig. 10. Synchronous measurement of T_j and T_h before and after the change of the fan speed.
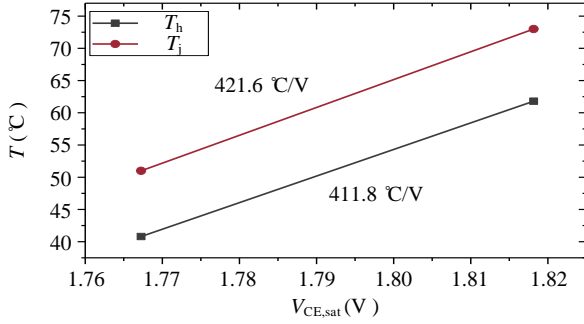

Fig. 11. Comparison between $dT_j/dV_{CE,sat}$ and $dT_h/dV_{CE,sat}$.

the fluctuation of $V_{CE,sat}$ within a small range as well; 3) the direct measurement of T_j refers to the point with the highest temperature on the chip surface. While the T_j estimated by the TSEP based method refers to the average temperature of the chip surface. Therefore, it is reasonable that the temperature estimated by the proposed method is lower than that of the direct measurement. Moreover, it can be seen that the absolute error is increased with increasing temperature, which is due to the positive temperature dependence of the first term on the right side of (3). Thus, neglecting it while calculating a can increase the error at higher temperature. Overall, the proposed method enables an on-line calibration with a satisfactory accuracy level in junction temperature estimation.

C. Accuracy analysis

The accuracy of the proposed calibration method is mainly affected by the assumptions made while calculating a and b. To analyze it quantitatively, the thermal impedances of the applied IGBT module are measured experimentally through the method presented in [26]. Fig.13 depicts the self thermal impedance $_{jh,11}$ of the chip to be tested (T1) and the coupled thermal impedances between T1 and other chips in the applied IGBT module, and their steady-state values are listed in Table II. Also, based on the datasheet of the IGBT module and the specifications in Table I, the average power losses of one IGBT and one diode over one fundamental period are calculated as 16.5 W and 8.6 W, respectively, in this case study. Meanwhile, the change rate of $V_{CE,sat}$ with response to temperature can
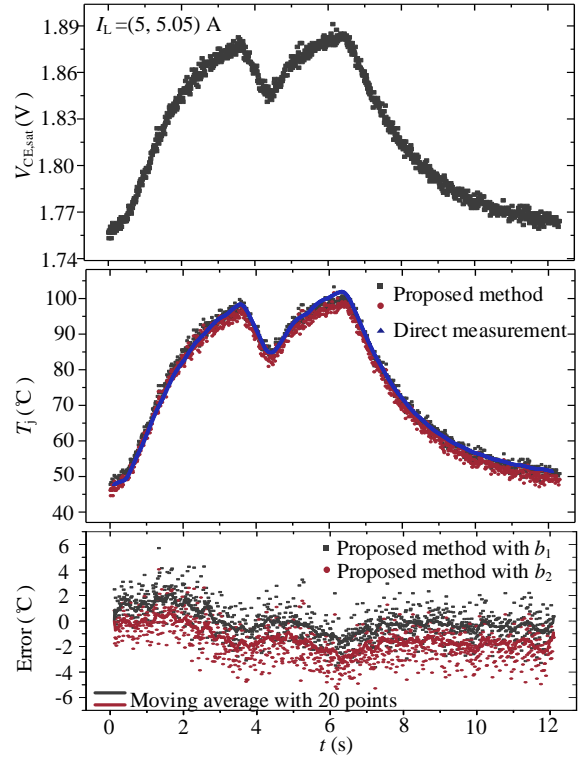

Fig. 12. Measured $V_{CE,sat}$ when I_L is within (5, 5.05) A (top), estimated T_j with proposed method and measured T_j with optic fiber temperature sensor (middle), and the corresponding error (the data with the proposed method minus the data with the direct measurement) (bottom).
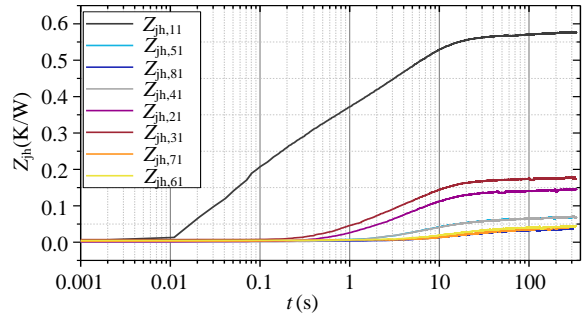

Fig. 13. Measured self and coupled thermal impedances of the applied IGBT module (F4-50R12KS4). $Z_{jh,11}$: self thermal impedance of T1; $Z_{jh,(2-8)1}$: coupled thermal impedance between T1 and other seven chips.

be obtained through the datasheet information as well. Then, with the information above, (7) can be graphically plotted when $I_{C,sensing}$ is 5 A and $I_{L,pk}$ is 20 A, as shown in Fig.14. It implies that dT_h is 99.5 % of dT_j, while dT_{jh} is only 0.5% of dT_j. Therefore, for this applied IGBT module, the error is 0.5% theoretically while calculating a.

In addition, the thermal resistances and time constants are obtained by fitting the measured thermal impedance in Fig.13. To simplify the analysis, it is assumed that the instant power losses of IGBT and diode are represented by the average power losses and independent from the temperature during the start-up. Then, combining with (10), the response of T_j over the

R_{th}	Value (K/W)	R_{th}	Value (K/W)
$R_{\mathrm{jh},11}$	0.578	$R_{\mathrm{jh},51}$	0.069
$R_{\mathrm{jh},21}$	0.146	$R_{\mathrm{jh},61}$	0.044
$R_{\mathrm{jh},31}$	0.175	$R_{\mathrm{jh},71}$	0.043
$R_{\mathrm{jh},41}$	0.07	$R_{\mathrm{jh},81}$	0.038
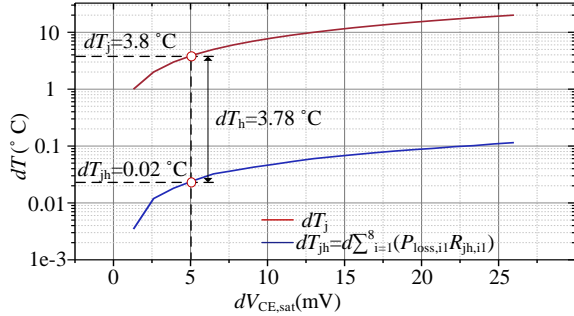
Fig. 14. Variation of dT_{j}, dT_{h}, and dT_{jh} with respect to $dV_{\mathrm{CE,sat}}$ at I_C=5 A and the average P_{loss} at $I_{L,pk}$=20 A, based on the datasheet of the applied IGBT module (F4-50R12KS4), Table I, and (7).
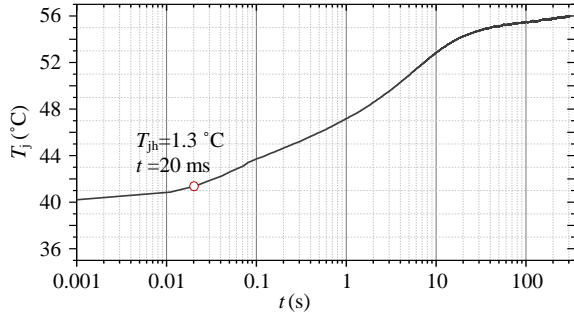

Fig. 15. T_{j} of the applied IGBT module (F4-50R12KS4) with response to the 14 W average P_{loss} in this case study when T_{h} is 40 °C.

start-up is depicted in Fig.15, indicating that T_{j} is increased by 1.3 °C during the first fundamental period (20 ms). Hence, theoretically, for the applied IGBT module, the caused error while calculating b is 1.3, accounting for 0.2% of the measured b before (i.e., 675.2).

D. Practical considerations

There are some practical considerations should be noted: 1) the measurement of I_{L} is set to a small range instead of a certain value based on the sampling frequency and resolution of current sensor; 2) due to the measurement range of I_{L} and the measurement noises, the measured $V_{\mathrm{CE,sat}}$ may fluctuate in a small range as well. Thus, the average of the measured $V_{\mathrm{CE,sat}}$ in steady-state is used to calculate a as shown in Fig.10; 3) the bad data of $V_{\mathrm{CE,sat}}$ may existed due to measurement noise in field applications. To exclude it, the measured $V_{\mathrm{CE,sat}}$ can be limited to a reasonable range, or compared with its neighboring data, which is not covered in this paper; 4) the selection of sensing current level is based on the trade-off between the

measurement error, sampling frequency, and achievable value of current during start-up: the higher sensing current has lower change rate that requires lower sampling frequency. However, the measurement error is increased while calculating b due to increased power losses. Therefore, the optional sensing current is in a range and differs from case to case. In this paper, the sensing current is selected as (5,5.1) A, which is determined by:a) it causes relatively low error; b) it has relatively low change rate; c) it is available during start-up; and 5) the fundamental current I_{rms} is expected to be constant at the required two thermal-steady states and the entire calibration time is two times of the thermal response time of the installed module, which is about 200 s based on the experimental testing results (Fig.8(b)) in this case study. In field applications, the constant I_{rms} at two points of time can be obtained by recording I_{rms} during one day for example. Then, two same or similar points of I_{rms} can be selected among the recorded data. Moreover, the change of heatsink temperature T_{h} can be realized by waiting for the change of ambient temperature for 5-10 °C within one day for example. Also, considering the high-linearity between $V_{\mathrm{CE,sat}}$ and T_{j}, 5-10 °C change should be enough [19, 21]. The required time intervals to perform one calibration is relatively longer in practical applications, e.g., every one day or week. For majority of applications, it would be a reasonable assumption that there are at least one start-up condition and two normal operation conditions with an ambient temperature difference of 5-10 °C.

The limitation of the proposed method is that it is applicable to those applications that have start-up event during regular operation. Moreover, the calibrated result through the proposed method can only estimate the T_{j} at the sensing current over the fundamental period, which is, however, sufficient for practical condition monitoring since it can also sense the change of T_{j} between different fundamental periods and capable of realizing protection and health monitoring for power devices. For example, without the whole picture of T_{j} over one fundamental period, the junction temperature increase due to the degradation of power devices can still be indicated by the TSEPs measured at the sensing current only.

IV. CONCLUSIONS

This paper presented an on-line and non-invasive calibration method for the temperature sensitive electrical parameter (TSEP) based junction temperature estimation of power semiconductors. It overcomes the limitation of conventional methods that require control modification and pre-testing, or long-time and extensive data recording. Meanwhile, the proposed method can achieve comparable accuracy with the highest accuracy achieved by conventional non-invasive off-line calibration methods. The experimental validation is conducted with a single-phase inverter and the results show that: 1) the calibration between junction temperature T_{j} and on-state voltage $V_{\mathrm{CE,sat}}$ is achieved by measuring the heatsink temperature and the $V_{\mathrm{CE,sat}}$ when the inductor current is within (5, 5.1) A for an operating converter; 2) Through the proposed

calibration method, the error of TSEP-based T_j estimation with respect to a direct measurement is limited to 2-4 °C in this case study; 3) the calibration can be finished within 200 s by measuring $V_{CE,sat}$ and T_j at three operation conditions of inverter in this case study. While, in practice, the proposed calibration can still be finished within one day in many cases by waiting for the change of ambient temperature for 5-10 °C. Additionally, considering the impact of the degradation of power devices on the relationship between $V_{CE,sat}$ and T_j, the proposed calibration can be conducted periodically or once the degradation is detected, e.g, once per month or year could be sufficient considering the long design lifetime of power semiconductor devices.

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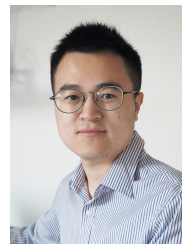
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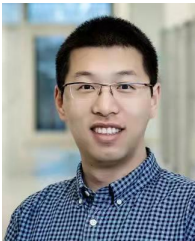
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