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Peng, Yingzhou; Chu, Kaiqi; Mu, Shuji; Cao, Hu; Wang, Huai

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A Parasitic Effect Compensation Method for IGBT On-state Voltage Measurement in Traction Inverter Application

Yingzhou Peng, *Member, IEEE*, Kaiqi Chu, Shujia Mu, Hu Cao, Huai Wang, *Senior Member, IEEE*

***Abstract*—This letter proposes a novel compensation method to eliminate the impact of parasitic inductances on the measurement accuracy of on-state voltage of power semiconductor devices in operating converters. It is an on-line and non-invasive method by measuring the output current of inverter and on-state voltage of power device only. The impact of parasitic inductances and its compensation are verified experimentally through a traction inverter system.**

***Index terms*—** Power semiconductor, compensation, parasitic inductance, on-state voltage.

I. Introduction

The on-state voltages are closely relative to the health condition and junction temperature of power semiconductor devices [1, 2]. Therefore, their accurate measurement is essential to the realization of predictive maintenance and reliability improvement [1]. Tremendous efforts have been devoted to realizing the online measurement of on-state voltage, consisting of component-level solutions [3–5] and converter-level solutions [6, 7].

Nevertheless, based on our best knowledge, the impact of the parasitic inductances in direct copper bond (DCB) layer and terminals of power semiconductor devices is rarely considered in the literature, and effective compensation method is also not well researched, which can heavily impair the measurement accuracy of on-state voltage in an operating converter. Although higher measurement accuracy of on-state voltage (e.g., $\pm$10 mV and $\pm$5 mV) is reported in [5] and [7], they are obtained through static DC input voltage testing, which does not induce voltage drop in the parasitic inductances. In addition, the direct-current (DC) power cycling testing presented in [8] is also independent on the parasitic inductances. However, in real power converter applications, the alternative current (AC) flowing through the DCB and terminals can induce additional voltage and has to be considered. Particularly in motor drive applications, the slope of current is variable due to different operational modes. In addition, for high-power applications, the parasitic inductances of power module might be too large to be neglected. In [3], the deviation of on-state voltage due to parasitic inductances could be more than 150 mV in a wind turbine power converter and a method is proposed to reduce the impact of parasitic inductances by integrating the measured on-state voltage over one switching-cycle. However, it can only obtain the average of on-state voltage during a switching cycle, instead of the instantaneous on-state voltage, which faces two challenges: (1) during one switching cycle, the change of current could be more than hundreds of amperes, leading to the loss of on-state voltage when power device operates in high-current status; (2) for traction inverter applications, there could be very few switching cycles over one fundamental period, which means very limited on-state voltage information can be obtained over one fundamental period.

In this letter, the impact of parasitic inductances on the measurement of on-state voltage in an operating power electronic converter is investigated and modeled by analyzing its sources and dependencies. Then, a novel compensation strategy is proposed to eliminate the impact of parasitic inductances at any instantaneous current-levels. It utilizes the measured on-

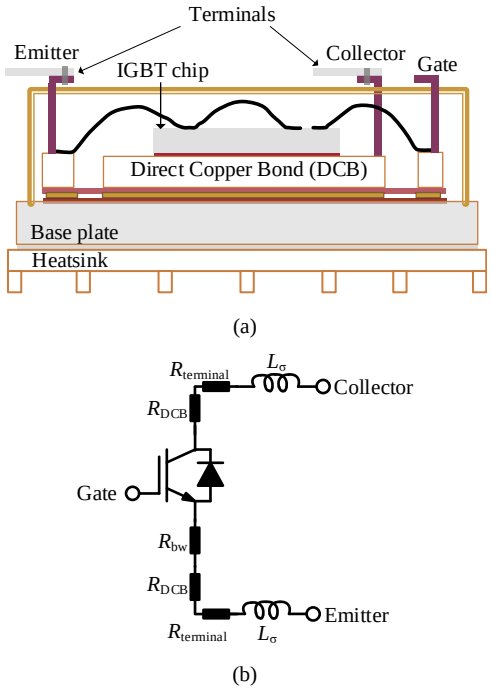

Fig. 1. An example of IGBT module: (a) cross-section; (b) equivalent circuit.

Y. Peng and H. Wang are with the Department of Energy Technology, Aalborg University, Aalborg, Denmark (email: ype@et.aau.dk, hwa@et.aau.dk). K. Chu, S. Mu, and H. Cao are with the CRRC Qingdao Sifang Co., Ltd (*Corresponding author*: Kaiqi Chu).

state voltage and phase-current in an operating converter to calculate the parasitic inductances in real-time. As a result, the voltage drop generated in the parasitic inductances can then be compensated without impairing the normal operation of converter. The experimental verification is also conducted through a traction inverter system with high-voltage and high-current.

II. Investigation and Compensation on Parasitic Inductances

In this letter, the analysis and demonstration of the proposed method are conducted based on an IGBT module. It is also applicable to other power devices, such as MOSFET. Fig.1(a) gives an example of a typical wire-bonded IGBT module. The terminals that are made of aluminum alloy provide electrical connection with outside and are soldered on the surface of DCB as like the bond wires inside the power module. Therefore, the physical parasitic elements of those electrical-conduction materials are spatially distributed inside the power module. Fig.1(b) illustrates the equivalent circuit of one IGBT with parasitic resistances and inductances.

Parasitic resistances R_{DCB} and R_{bw} are contributed by the tracks on DCB and aluminum bond wires inside the power module, respectively. R_{terminal} represents the parasitic resistance of the terminals. L_σ is the parasitic inductances from collector to emitter. In an operating power converter, the inductive and resistive parasitic elements can lead to the deviation of measured total on-state voltage from the on-state voltage of IGBT chip $V_{\mathrm{CE,sat,chip}}$, which can be expressed by:

$$\begin{cases} V_{\mathrm{CE,sat}} = V_{\mathrm{CE,sat,chip}} + i_{\mathrm{c}} R_{\mathrm{tot}} + 2L_\sigma \dfrac{di_{\mathrm{c}}}{dt} \\ R_{\mathrm{tot}} = 2R_{\mathrm{DCB}} + R_{\mathrm{bw}} + 2R_{\mathrm{terminal}} \end{cases} \tag{1}$$

R_{DCB} and R_{bw} are thermally connected to chip and the voltage drops on them will follow chip temperature linearly for a given current-level [3]. As a result, the sensitivity to temperature change of $V_{\mathrm{CE,sat}}$ is amplified. Moreover, R_{DCB} and R_{bw} have link to the degradation of DCB and bond-wire, respectively. Overall, the existence of R_{DCB} and R_{bw} can be seen as a benefit for the health condition assessment of power module. The value of R_{terminal} is usually in $\mu\Omega$-level and has negligible impact on $V_{\mathrm{CE,sat}}$ even at different temperatures [3]. It is reported that parasitic inductance usually has a distinct temperature-dependency when frequency is larger than 1 GHz for example [9], which is much higher than that in most power electronic applications. Also, for most cases, the terminal temperature is relatively stable due to its extremely low parasitic resistance and relatively stable temperature inside inverter. Overall, the temperature impact on parasitic inductance can be neglected.

Fig.2 illustrates the topology of a three-phase inverter for motor drive application. According to the modulation strategy

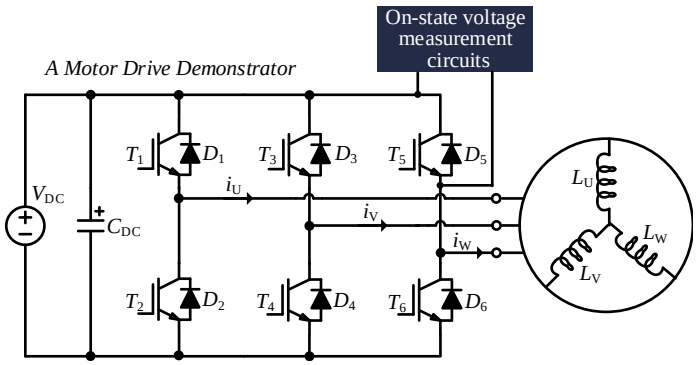

Fig. 2. An example of motor drive system with on-state voltage measurement circuit.

(e.g., SPWM or SVPWM), the operation statues of the inverter can be roughly given by:

$$\begin{cases} L_{\mathrm{x1}} \dfrac{di_{\mathrm{x1}}}{dt} - L_{\mathrm{x2}} \dfrac{di_{\mathrm{x2}}}{dt} = V_{\mathrm{DC}} \\ L_{\mathrm{x1}} \dfrac{di_{\mathrm{x1}}}{dt} - L_{\mathrm{x2}} \dfrac{di_{\mathrm{x2}}}{dt} = 0 \\ L_{\mathrm{x1}} \dfrac{di_{\mathrm{x1}}}{dt} - L_{\mathrm{x2}} \dfrac{di_{\mathrm{x2}}}{dt} = -V_{\mathrm{DC}} \end{cases} \tag{2}$$

where x1 and x2 could be any two of U, V, and W, implying that L_{x1} and L_{x2} are any two of the three equivalent inductances in the motor L_{U}, L_{V}, and L_{W}. i_{x1} and i_{x2} are any two of the three AC currents i_{U}, i_{V}, and i_{W}. V_{DC} is the DC-link voltage. It should be noted that i_{U}, i_{V}, and i_{W} can be seen as the collector current i_{c} of the power switch that is in conduction-mode.

Based on (2), over one fundamental period, the derivative of current di_{c}/dt is not constant and can be either positive or negative, and changes with variable DC-link voltage. It implies that the measured $V_{\mathrm{CE,sat}}$ has a variable error, which leads to an unacceptable deviation on the evaluation of junction temperature and health condition of device under test (DUT). Especially, the desired switching cycles of DUT in a three-phase inverter are generated by means of pulse width modulation (PWM) method. For example, in an inverter with space-vector pulse width (SVPWM) modulation scheme, there are seven switching vectors during one switching cycle [3], resulting in several changes in di_{c}/dt and voltage drops of parasitic inductance.

Therefore, compared to parasitic resistances, the impact of parasitic inductances is more complex due to the variable derivative of current (di_{c}/dt) in response to time when the DUT is in conduction-mode, which can affect the accuracy of $V_{\mathrm{CE,sat}}$ and has to be compensated.

For example, when DUT is in conduction-mode, two collector current points with same value but different slopes are selected and indicated as I_{c1} and I_{c2} during one switching cycle. Meanwhile, their corresponding on-state voltages are $V_{\mathrm{CE,sat1}}$ and $V_{\mathrm{CE,sat2}}$, respectively. Based on the measured current data before and after I_{c1} and I_{c2}, and data sampling frequency, the current slopes at I_{c1} and I_{c2} can be calculated as

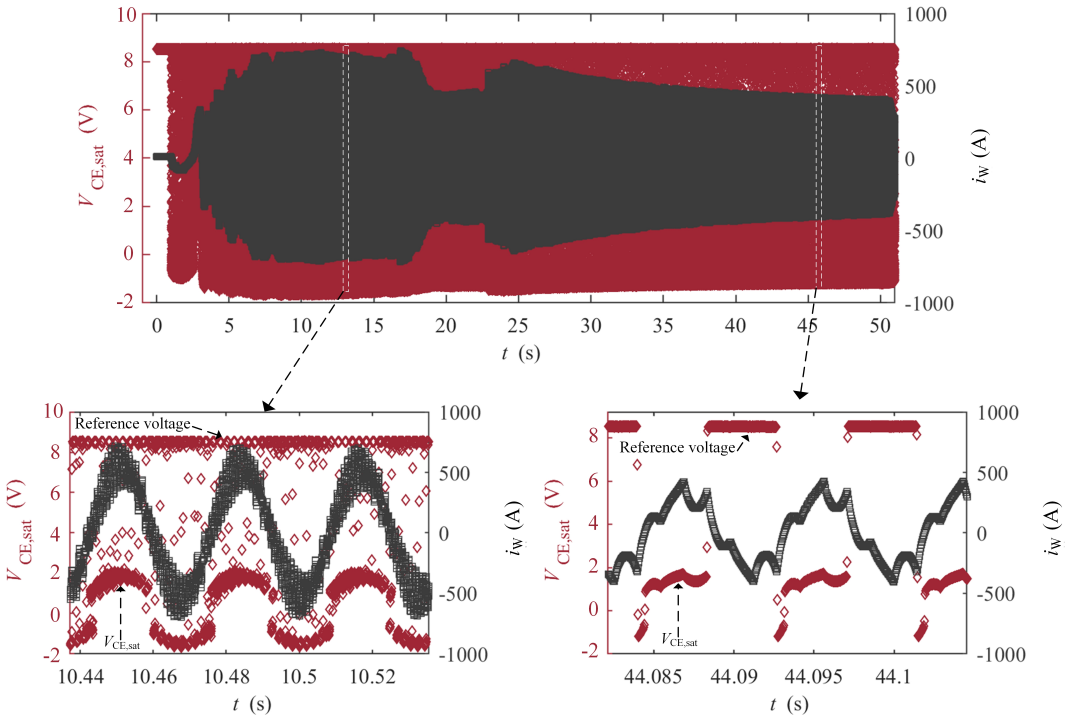

Fig. 3. Measured on-state voltage of T_5 and phase current i_W while motor drive is in operating (note: when the DUT is in off-state, the voltage across collector to emitter is the DC-link voltage that is blocked and clamped into a reference voltage by the measurement circuit).

dI_{c1}/dt and dI_{c2}/dt, respectively. Then, the following equations can be obtained:

$$V_{\mathrm{CE,sat1}} = V_{\mathrm{CE,sat,chip1}} + I_{c1}R_{\mathrm{tot}} + L_{\sigma,\mathrm{tot}}\frac{dI_{c1}}{dt} \quad (3)$$

$$V_{\mathrm{CE,sat2}} = V_{\mathrm{CE,sat,chip2}} + I_{c2}R_{\mathrm{tot}} + L_{\sigma,\mathrm{tot}}\frac{dI_{c2}}{dt} \quad (4)$$

where $L_{\sigma,\mathrm{tot}}$ indicates the total parasitic inductance from the collector to emitter of IGBT.

If I_{c1} is assumed to be same with I_{c2}, resulting in that $V_{\mathrm{CE,sat,chip1}} + I_{c1}R_{\mathrm{tot}}$ is same with $V_{\mathrm{CE,sat,chip2}} + I_{c2}R_{\mathrm{tot}}$. Then, subtract (4) from (3):

$$L_{\sigma,\mathrm{tot}} = \frac{V_{\mathrm{CE,sat1}} - V_{\mathrm{CE,sat2}}}{dI_{c1}/dt - dI_{c2}/dt} \quad (5)$$

Since $V_{\mathrm{CE,sat}}$ and dI_c/dt are measurable, the parasitic inductance $L_{\sigma,tot}$ can then be calculated in real-time. Consequently, the inductive term in (1) can be compensated in real-time.

It should be noted that ensuring I_{c1} is same with I_{c2} could be a challenge in practice. Therefore, the introduced error due to different I_c should be analyzed. For the module with high power rating (e.g., 3300 V/1500 A), R_{tot} could be far less than 1 mΩ. While R_{tot} is usually couple of mΩ for the module with low power rating (e.g., 1200 V/50 A). Thus, the former one has more wider tolerance in current difference than the latter module, which corresponds to practical applications since high-current sensor has low resolution than low-current sensor. Actually, the change rate of on-state voltage in response to current $dV_{\mathrm{CE,sat}}/dI_c$ can be obtained from the datasheet of applied IGBT module. Then, the error due to different I_c can be estimated in advance. It is acceptable if this error is less than the absolute value of $V_{\mathrm{CE,sat1}} - V_{\mathrm{CE,sat2}}$ by 10%, which will be verified experimentally in next section.

III. Experimental Verification with a Case Study of Motor Drive

The proposed method is verified through a motor drive system with 1800 V DC-link voltage, variable fundamental and switching frequency f_{sw}. The IGBT in the up-bridge of phase-W (i.e., T_5 in Fig.2) is taken as the DUT. (the implementation for other power devices can be derived similarly) and an on-line on-state voltage measurement circuit is used as shown in Fig.2. The applied measurement circuit, originally introduced in [7], is capable of either extracting the on-state voltages of multiply power devices by connecting to the middle-point of each phase-leg, or extracting the on-state voltage of one power device by connecting to the collector-emitter of DUT.

During testing, the motor is set to operate at three different conditions: speed-up, uniform-speed, and speed-down. The measured output phase current i_{W} and on-state voltage of T_5 over 50 s are presented in Fig.3. The resolution of applied Analog-Digital Converter (ADC) is 12-bits and data sampling frequency f_{sm} is 25 kHz. In order to get enough details of current and on-state voltage over one switching-cycle and improve the estimation accuracy of $L_{\sigma,\mathrm{tot}}$, f_{sm} should be 20-30 times of f_{sw} according to the experimental results in later this section. The white dash-rectangle parts in the up-figure of Fig.3 are zoomed-in, implying that $V_{\mathrm{CE,sat}}$ and i_{W} are

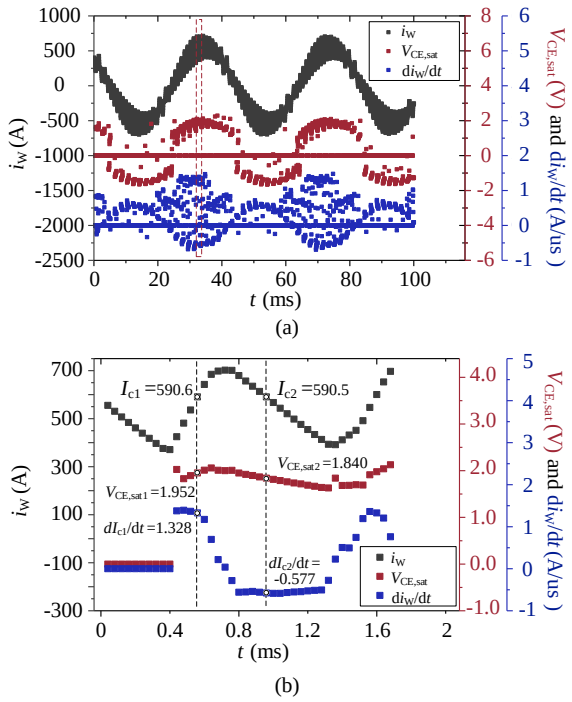

Fig. 4. Experimental waveforms: (a) over two fundamental period; (b) over one switching cycle (note: before about 0.4 ms, the DUT is in off-state and the di_{W}/dt and $V_{\mathrm{CE,sat}}$ are set to zero).

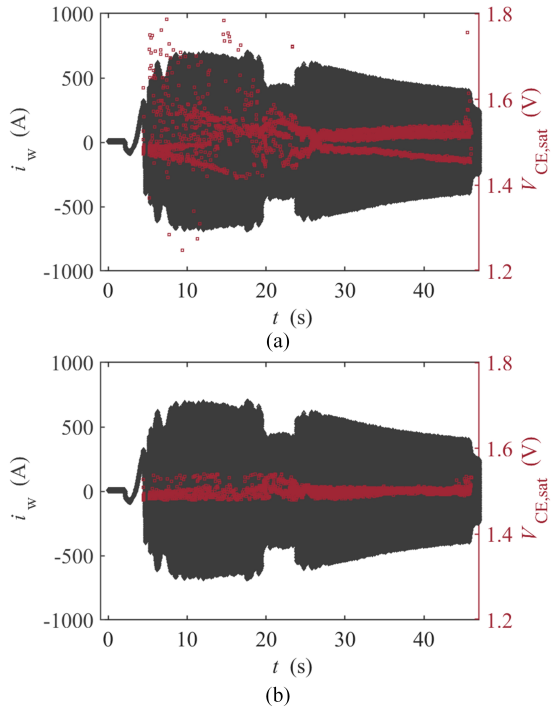

Fig. 5. Extracted on-state voltage when i_{W} is within (300 - 305) A: (a) before compensation; (b) after compensation.

measurable and synchronous, and have variable fundamental and switching frequency at different operation conditions. In practice, considering the phase current sensors are already existed for control or protection purpose in most applications, an additional on-state voltage measurement circuit is required only in terms of hardware. However, f_{sm} has to be increased, which can be realized by modifying the existing control unit or using an additional data acquisition system with enough f_{sm} as a condition monitoring unit.

The slope of i_{W} is simply calculated by using three neighboring points in i_{W} as:

$$di_{\mathrm{W,k}}/dt = \frac{i_{\mathrm{W,k+1}} - i_{\mathrm{W,k-1}}}{2T_{\mathrm{sample}}} \tag{6}$$

where T_{sample} is the sampling period.

The calculated di_{W}/dt is shown in Fig.4. $V_{\mathrm{CE,sat}}$ is the measured on-state voltage of DUT. The red rectangle in Fig.4(a) is zoomed-in to show the detail of one switching-cycle as presented in Fig.4(b). The data at upward-track and downward-track, but similar current-level are marked. It can be seen that the on-state voltage at upward-track is higher than the value at downward-track by about 112 mV at this current-level due to the different current slopes and the existence of parasitic inductance. With the marked data in Fig.4(b) and (5), the parasitic inductance can be calculated as:

$$L_{\sigma,\mathrm{tot}} = \frac{1.952 - 1.840}{(1.328 - (-0.577)) \times 10^{-6}} \approx 59nH \tag{7}$$

To verify the repeatability of (7), another five switching cycles are selected randomly to calculate $L_{\sigma,\mathrm{tot}}$, showing 53 nH, 56 nH, 69 nH, 62 nH, and 62 nH. This fluctuation is due to the measurement error and can be reduced by calculating the average of these $L_{\sigma,\mathrm{tot}}$, which is about 60 nH.

Then, the impact of parasitic inductance can be compensated by substituting this 60 nH into (3) and (4). Five current pairs with similar value are taken from the upward-track and downward-track, and the corresponding on-state voltages are recorded as $V_{\mathrm{CE,sat1}}$ and $V_{\mathrm{CE,sat2}}$, respectively, as listed in Table I. The $dV_{\mathrm{CE,sat}}/dI_{\mathrm{c}}$ of the applied IGBT module is about 1.3 mV/A according to its datasheet. Considering the $L_{\sigma,\mathrm{tot}}$ caused difference in $V_{\mathrm{CE,sat}}$ could be 112 mV in this case study, the difference of selected current pairs should be less than 8-9 A. Before compensation, the measured $V_{\mathrm{CE,sat}}$ at upward-track is higher than the value at downward-track by 5.6 % to 6.1 % even at similar selected current-level. However, after compensation, their difference is reduced down to only 0.1 % of the value at upward-track, which proves the effectiveness of the proposed method. Moreover, this deviation is increased from 0.1 % to 0.5 % when the current difference is changed from 0 A to 7 A.

In addition, the on-state voltage when current i_{W} is within a narrow range (e.g., (300 - 305) A in this case study) is extracted over experimental testing. Then, the proposed compensation strategy is applied to eliminate the impact of parasitic inductances. Fig.5 gives the results before and after compensation. It implies that the obtained on-state voltage after compensation has a much narrower variation and better continuity than the data before compensation.

Overall, with enough data sampling frequency, the proposed

TABLE I
COMPARISON OF MEASURED ON-STATE VOLTAGE BEFORE AND AFTER COMPENSATION (UNIT: V)

i_{w} (A)	Up/Down	481/476	536/543	590/590	642/635
Before Compen--sation	$V_{\mathrm{CE,sat1}}$	1.828	1.894	1.952	2.010
	$V_{\mathrm{CE,sat2}}$	1.716	1.788	1.840	1.898
	Percentage	6.1%	5.6%	5.7%	5.6%
After Compen--sation	$V_{\mathrm{CE,sat1}}$	1.744	1.812	1.872	1.940
	$V_{\mathrm{CE,sat2}}$	1.750	1.822	1.874	1.930
	Percentage	0.3%	0.4%	0.1%	0.5%

Note: Up/Down indicate the upward-track and downward-track of current over one switching-cycle, respectively.

method can be implemented in an operating converter by five steps: 1) extract the data over 5-10 switching cycles at the beginning; 2) confirm the current data is in upward-track or downward-track by calculating the change rate of each current data through (6); 3) find the similar currents in upward-track and downward-track, respectively, and corresponding on-state voltages; 4) calculate $L_{\sigma,\mathrm{tot}}$ and its average; 5) compensate $V_{\mathrm{CE,sat}}$ through the calculated average of $L_{\sigma,\mathrm{tot}}$ and measured current.

IV. CONCLUSIONS

In this letter, the parasitic elements in the on-state voltage of power semiconductor devices are modeled to explore the impact of inductive parasitic elements. Then, a novel compensation strategy is proposed to reduce the deviation of on-state voltage caused by parasitic inductances. It uses the phase current of inverter and on-state voltage of power semiconductor device only, and can be realized in real time. The experimental verification is conducted through a traction inverter case study. The results imply that the deviation of the on-state voltages measured at similar current-level but with different current slopes could be up to 6.1 % in this case study, which is unacceptable considering the change of on-state voltage due to device degradation is 5 % to 20 %, and its temperature sensitivity is less than 5 mV/°C for most cases. While, after compensation, this deviation is reduced up to 0.5 % under the selected current-levels in this case study.

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