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Published in:
2021 IEEE Energy Conversion Congress and Exposition (ECCE)

DOI (link to publication from Publisher):
10.1109/ECCE47101.2021.9595130

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

Discontinuous Modulation for Improved Thermal Balance of Three-Level 1500-V Photovoltaic Inverters under Low-Voltage Ride-Through

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***Abstract*—This paper investigates the thermal behavior of a 90-kW/1500-V, three-level, neutral-point-clamped (3L-NPC), single-stage PV inverter during low-voltage ride-through (LVRT) operation. To improve thermal performance during LVRT operation, a modified discontinuous pulse-width modulation (DPWM) scheme is proposed in this paper. As a major outcome, we concluded that, with the proposed scheme, the thermal stress is distributed more equally among the power devices compared to that with the conventional strategy. Simulation and experimental results are presented to assess the effectiveness of the proposed DPWM.**

***Index Terms*—Photovoltaic (PV) inverters, low voltage ride through, modulation, power loss, thermal stress.**

I. Introduction

1500-V photovoltaic (PV) systems are increasingly employed in utility-scale power plants to achieve lower installation costs [1]–[4]. Notably, the single-stage approach based on three-level neutral point clamped (3L-NPC) inverters, as shown in Fig. 1, is promising for 1500-V PV applications [5]. However, for utility-scale 1500-V PV applications, the grid requirements generally mandate reactive power support to the grid, which may impose high loading stress on the PV inverters [6]. In fact, with the conventional continuous pulse-width modulation (PWM) strategies [7], [8], the outer devices (e.g., T1, D1), the inner devices (e.g., T2, D2), and clamping diodes (e.g., D5) of the NPC inverter are not equally utilized and have considerably different loading. This is more critical during low-voltage ride-through (LVRT) conditions, where the inverter output voltage is low, while the injected reactive current is high. When a severe grid voltage sag occurs (e.g., over 50% sag depth), two things happen: 1) the inverter needs to provide 100% rated reactive current [9], and 2) the DC-link voltage gets close to the open-circuit voltage of the PV string [10], which means that the inverter needs to operate at extreme conditions but with very low modulation indices at the same time. Consequently, the inner switches and clamping diodes will carry much higher root-mean-square (RMS) currents than the outer devices, resulting in a considerably unequal power loss and thermal distribution, which directly affects the reliability performance of the NPC inverter. Nevertheless, the thermal stress analysis of a single-stage 3L-NPC PV inverter during LVRT events has not been thoroughly studied yet, especially for 1500-V applications.

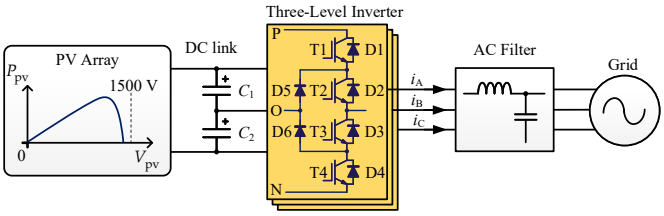

Fig. 1. Simplified configuration of a single-stage 1500-V PV system based on a three-level NPC inverter: P_{pv} – PV power, V_{pv} – PV voltage, i_{ABC} – phase current, C_1, C_2 – DC-link capacitor.

Many efforts have been made on both continuous PWM (CPWM) and discontinuous PWM (DPWM) to relieve the most stressed devices. In [11], several new CPWM strategies have been proposed for 3L-NPC wind power converters. These CPWM schemes adopt special vector sequences with reduced zero voltage outputs or decreased commutations. A three-level DPWM achieving an overall minimized switching loss was proposed in [12], where maximum or middle phase current is clamped to the positive, neutral or negative point of the DC link according to the modulation index and power factor angle. In [13], the impact of different DPWM schemes on the thermal stress distribution of the T-type NPC inverter was investigated. However, the investigated strategies are conventional DPWM schemes optimized for maximum switching loss reduction rather than for thermal redistribution under specific power-factor angles. In addition, the model predictive control (MPC) is also suited for thermal redistribution. The authors of [14] proposed a control algorithm based on the finite set MPC to redistribute the power losses among the switches and diodes within the 3L-NPC converters without increasing computational efforts and additional hardware for measurement. However, the switching frequency under this control algorithm is not constant due to the lack of a modulator.

Considering the above, this paper fills a gap of knowledge

TABLE I
PV INVERTER SPECIFICATIONS.

Nominal power P_{nom}	90 kW
Grid line-to-line RMS voltage V_{LL}	600 V
Grid frequency f_g	50 Hz
Switching frequency f_{sw}	10 kHz
Modulation method	Sinusoidal pulse-width modulation (SPWM) [17]
Power module producer and part number	Semikron Skiip 39MLI12T4V1 [18]
Power module rating	1200 V /150 A

around the operation of 1500-V single-stage 3L-NPC PV inverters under LVRT operation. It starts with analyzing the power loss and thermal distribution among the power devices, i.e., diodes and IGBTs. This analysis is carried out on a 90-kW/1500-V PV inverter adopting 1200-V/150-A NPC power modules under a sinusoidal PWM (SPWM) strategy. The results indicate that the clamping diodes suffer from much higher thermal stresses than the other power devices within the inverter during severe grid voltage sags. It is then pointed out in Section II that, in such cases, the power losses on the clamping diodes are dominated by conduction losses. Accordingly, a modified DPWM scheme from the method in [12] is proposed, where the clamping state is selected in a way to redistribute the thermal stress among power devices. The principle of the modified DPWM is presented in Section III, followed by an assessment of its ability to distribute the thermal loading among the power devices in Section IV. After that, the experimental validation of the proposed DPWM is presented in Section V. Finally, Section VI gives the conclusions.

II. THERMAL STRESS ANALYSIS OF PV INVERTER DURING LVRT

A 90-kW/1500-V single-stage 3L-NPC PV inverter is considered in this paper, as shown in Fig. 1. The key parameters are given in Table I. A detailed thermal stress analysis has been carried out in PLECS [15], where the inverter undergoes LVRT operation. Taking the LVRT requirements in Denmark as an example, the PV system is required to provide maximum voltage support by delivering a certain amount of reactive current when a voltage sag occurs as shown in Fig. 2 (i.e., yellow area) [16]. Considering a severe case, a grid voltage sag is set to be below 0.5 p.u., and the single-stage PV inverter needs to provide 100% reactive current with its maximum DC-link voltage, i.e., the open-circuit voltage of the PV array, which is close to 1500 V.

Under certain inverter operating conditions, the conduction losses and switching losses of each power device in the 3L-NPC inverter can be modeled based on the current and voltage information with a power loss model [19]. After that, the junction temperature can be obtained by applying the power losses to the thermal model [20], as shown in Fig. 3. A series

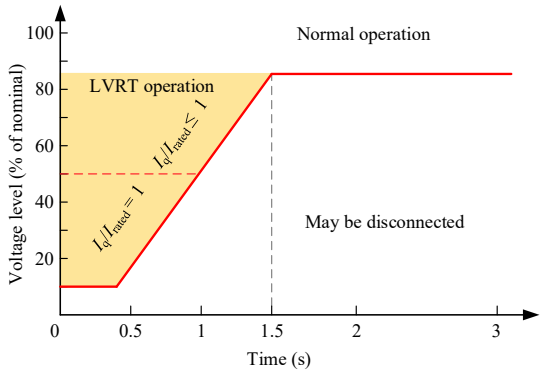

Fig. 2. LVRT requirements for PV system above 11 kW in Denmark, where I_q and I_{rated} represent the reactive current and rated current, respectively [16].

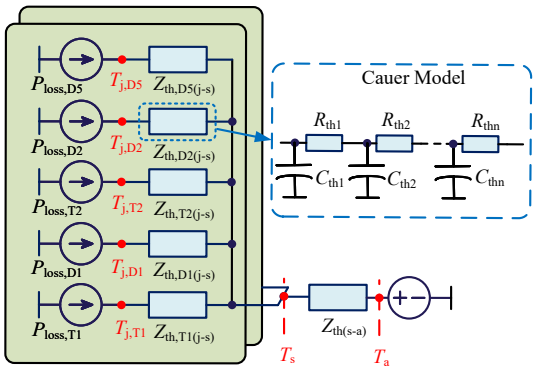

Fig. 3. Thermal model of the NPC inverter, where T_j, T_s, and T_a represent the junction, heatsink and ambient temperature, respectively.

combination of the junction-to-heatsink thermal impedance $Z_{th(j-s)}$ and heatsink-to-ambient thermal impedance $Z_{th(s-a)}$ is used, as the selected power module is based on the baseplate-less technology. The Cauer model has been chosen as the thermal model of each IGBT and diode, and the RC parameters of it have been obtained by fitting the thermal impedance curve from the module datasheet [21]. In this case study, the heatsink temperature is set to be at a fixed temperature of 60 °C, having considered its large thermal capacitance and the short duration of grid voltage sags (several milliseconds to a few seconds as shown in Fig. 2). More details regarding the electro-thermal simulation of the 3L-NPC PV inverter have been presented in [7] and [22].

The power devices' junction temperatures in the NPC inverter under two different grid voltage sags are shown in Fig. 4, where the PV inverter is operated with 100% rated reactive current and 1300-V DC-link voltage. To consider the worst-case scenario, the operation time under the reduced grid voltage has been set to be long enough to obtain the maximum thermal stresses (i.e., time to saturate the thermal capacitance $C_{th(j-s)}$. It can be observed in Fig. 4 that the clamping diodes suffer from much higher thermal stresses than other power devices, especially when a more severe voltage sag occurs. With a further power loss analysis as shown in Fig. 5, it can be noted that the high thermal stress of the clamping diodes is

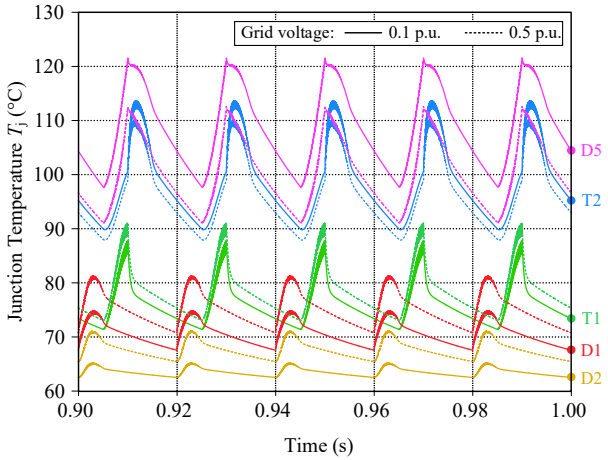

Fig. 4. Junction temperature of the power devices within the NPC inverter during two different LVRT operation conditions, i.e., 0.1 p.u. and 0.5 p.u. grid voltage.

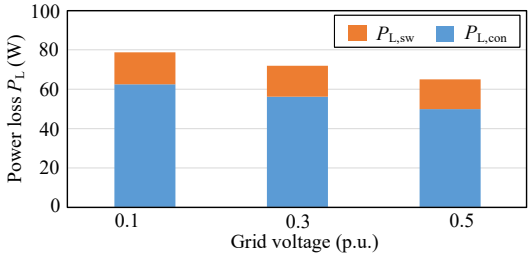

Fig. 5. Power losses of D5 under three levels of voltage sags during LVRT operation: $P_{L,sw}$ – switching loss, $P_{L,con}$ – conduction loss.

mainly caused by their conduction losses, which implies that the modulation schemes could be optimized toward reducing the RMS current carried by the clamping diodes.

III. Proposed Modified DPWM

Referring to Fig. 1, each leg of the three-level inverter has three available switching states, i.e., "P" (T1, T2: ON, others: OFF), "O" (T2, T3: ON, others: OFF), and "N" (T3, T4: ON, others: OFF), which forms a vector space with 27 space vectors, as shown in Fig. 6 [23]. Generally, the three-level DPWM strategies can clamp each phase X (X = A, B, C) to the positive (X+), neutral (X0), or negative (X-) point of the DC link for a certain fraction of the fundamental period [12], [24]. Considering small modulation indices ($\leq$ 0.5), all the available clamping states (X+, X0, X-) for different subsectors are labeled in Fig. 6. For instance, when V_{ref} is located in the subsector shown in Fig. 6, there are five available clamping states, i.e., A+, A0, B0, C0, and C-. A detailed description regarding the implementation of the three-level DPWM can be found in [12] and [24].

Typically, for DPWM strategies, different clamping states are selected according to the positions of current peaks to reduce switching losses as much as possible. As shown in Fig. 6, when the modulation index is lower than 0.5, each type of the clamping state can be selected to achieve maximum switching

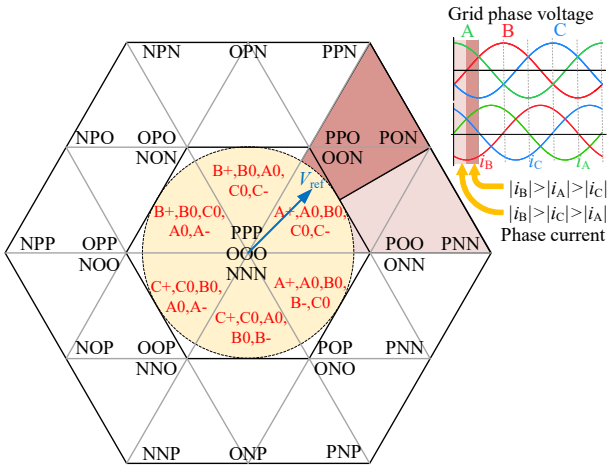

Fig. 6. Vector space and available clamping states when the modulation index is lower than 0.5.

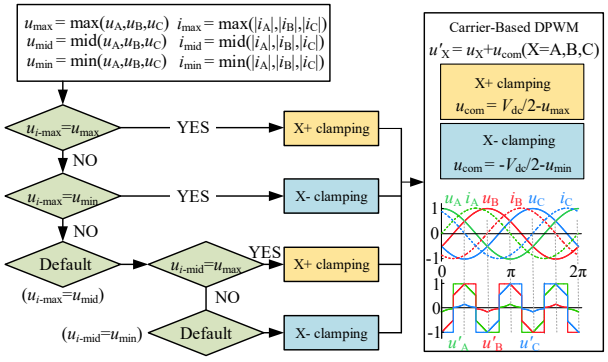

Fig. 7. Flow chart of the proposed DPWM for thermal balance in the 3L-NPC under LVRT operation.

loss reduction [12]. It is worth noting that, considering a 100% reactive power feeding during LVRT (assuming the current lags grid voltage by 90°), as shown in Fig. 5, in most of cases only "X0" will be selected for current peaks, as the phase difference between the grid voltage and the inverter output is, in practice, very small. However, as pointed out in the previous section, the clamping diodes suffer from severe thermal stress during LVRT operation. Therefore, in such a case, the "X0" clamping state should not be used to avoid further aggravating the clamping diodes' overloading.

In this paper, the selection strategy of the clamping state is thus modified to achieve an improved thermal distribution. The proposed strategy is summarized in Fig. 7. In Fig. 7, $u_{i\text{-}max}$ and $u_{i\text{-}mid}$ denote the phase voltage corresponding to the maximum current i_{max} and middle current i_{mid}, respectively; u'_X, u_{com}, u_X, and i_X are the modulation voltage, injected common-mode voltage, original reference phase voltage, and phase current, respectively. Fig. 7 also shows the modulation waves when the current lags the voltage by 90°, where it can be seen that no "X0" is selected when applying the proposed strategy. Correspondingly, when it is not possible to align "X+" or "X-" to current peaks, the middle current is considered for "X+" and "X-" selection. It can be expected that adopting the

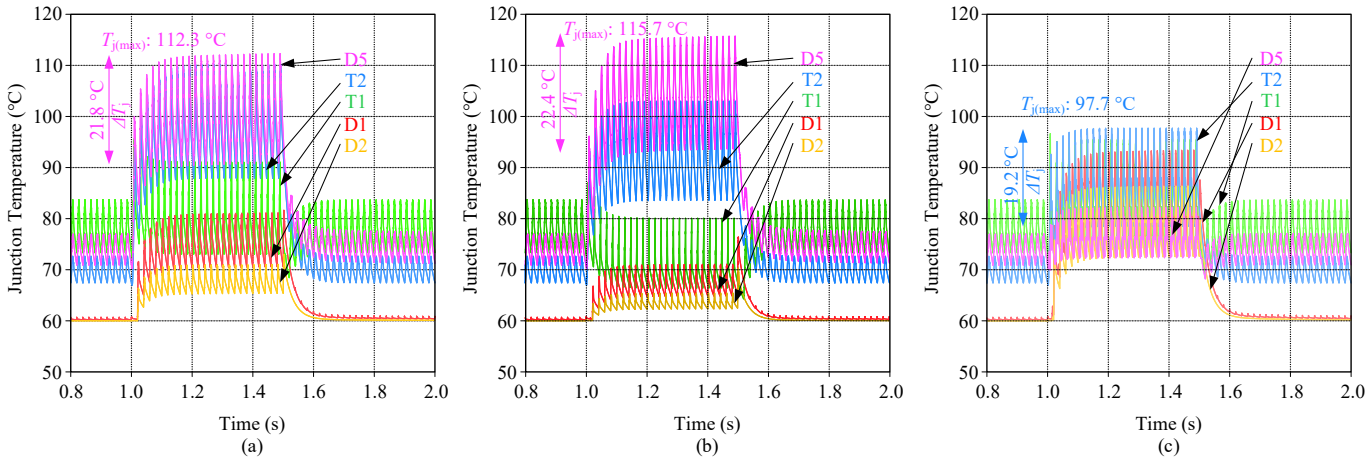

Fig. 8. Junction temperature dynamics, where a 0.5-p.u. voltage sag occurs at t = 1.0 s and lasts for 0.5 s: (a) SPWM during LVRT, (b) SLDPWM during LVRT, and (c) proposed DPWM during LVRT.

proposed DPWM strategy during LVRT operation will reduce the utilization of clamping diodes and redistribute the power loss and thermal stress among the power devices.

IV. Analysis of Power Loss and Thermal Redistribution

To evaluate the effectiveness of the proposed DPWM on power loss and thermal stress redistribution, the dynamic of the device temperature has been simulated, where the PV inverter experiences a 500-ms 0.5-p.u. voltage sag from normal operation. During normal operation before and after the voltage sag, the PV inverter is assumed to work with the conventional SPWM and inject around 50% rated active power to the grid at 1100-V DC-link voltage under the maximum power point tracking (MPPT), which is a moderate operating condition in practice. When the LVRT operation occurs, the modulation strategy will be transferred to the proposed DPWM or other PWM schemes for comparison, and 100% rated reactive current is produced with a 1300-V DC-link voltage.

The proposed DPWM is compared with two other modulation schemes: 1) the conventional SPWM which is regarded as normal modulation for the case study, and 2) the DPWM strategy in [12] aiming for switching loss reduction (called SLDPWM for convenience). Fig. 8 shows the junction temperature dynamics of the PV inverter under different PWM schemes. It can be observed in Fig. 8(a) that using the normal modulation during LVRT operation results in a much higher thermal stress (both in terms of maximum junction temperature $T_{j(max)}$ and cycle amplitude of junction temperature ΔT_j) in the clamping diode D5 compared to the other devices. If the SLDPWM is applied, as shown in Fig. 8(b), the thermal stress of IGBT T1 will be reduced to a large extent compared to that in the normal modulation in Fig. 8(a). However, the thermal stress of the clamping diode D5 is even higher compared to that in Fig. 8(a). This happens because the "X0" clamping state is given priority for small modulation indices when applying the SLDPWM. When the proposed DPWM is applied during the LVRT operation, as shown in Fig. 8(c), the thermal stress of D5 is considerably reduced (only slightly higher than that during the normal operation). The cost of this stress reduction is that both the thermal stresses of D1 and D2 are increased to a certain extent. Consequently, T2 becomes the "most stressed" device, but its thermal stress is still much lower than that of D5 with normal modulation.

Seen from the perspective of power losses, as shown in Fig. 9, both the total power losses under the proposed DPWM and the SLDPWM are reduced remarkably compared with that under normal modulation. When comparing the power losses between the SLDPWM and the proposed one, the proposed DPWM redistributes the loss from D5 to D1 and D2, i.e., the most stressed devices to the less stressed ones, which achieves an improved power loss and thermal stress distribution. It should be pointed out that the modulation performance should be also evaluated with other considerations like the power/current quality and the control ability of the neutral-point voltage, which will be the future work.

V. Experimental Validation

Based on the PV inverter specifications of Table I, an experimental platform, as shown in Fig. 10, is constructed to verify the feasibility of the proposed DPWM. The platform is based on DSP TMS320F28377D controller, where a 1500-V DC power supply IT6080C-1500-40 is used to provide the DC-link voltage, and an LC filter (2.4 mH, 10 μF) as well as a 10-kVA isolation transformer are connected between the inverter and 400-V (line voltage) AC grid. Also, as shown in Fig. 10, an optic fiber sensor is installed on top of one IGBT module (with openings to reach the IGBT/diode chips) to measure the junction temperature. Correspondingly, a signal conditioner from CoreSens is selected as the monitoring system, which converts the optical signal into a voltage signal with a programmable scale and offset. The DC-link voltage is set to 1300 V when injecting reactive current to the 400-V

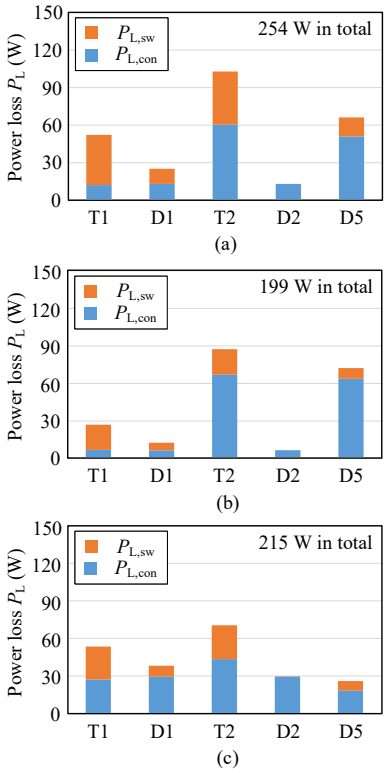

Fig. 9. Power loss distribution during the 0.5 p.u. voltage sag: (a) SPWM during LVRT, (b) SLDPWM during LVRT, and (c) proposed DPWM during LVRT ($P_{L,sw}$ – switching loss, $P_{L,con}$ – conduction loss).

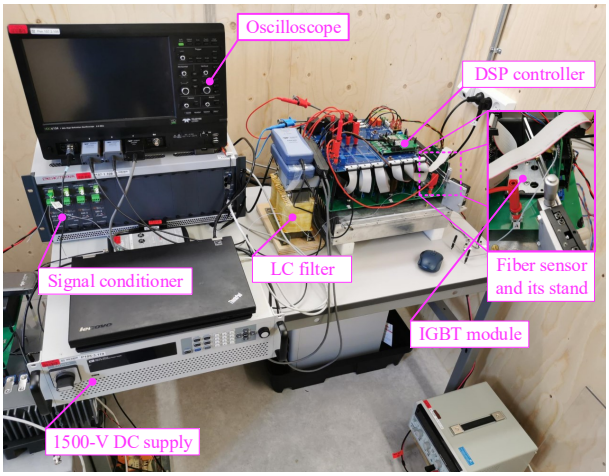

Fig. 10. Experimental prototype of the 3L-NPC 1500-V PV inverter.

grid, which is similar to the operating conditions of the PV inverter during severe LVRT events.

Fig. 11 shows the steady-state phase voltage u_A (inverter output to the neutral point of the DC-link), phase current i_A, and line voltage v_{AB} between the LC filter and the transformer. It can be seen from Fig. 11 that the phase voltage only clamps to the positive or negative point of the DC-link when using the proposed DPWM. This is different from the previous DPWM strategies, where the objective is to reduce the overall

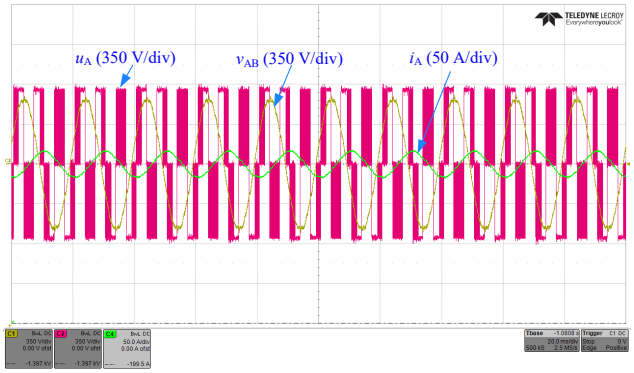

Fig. 11. Steady-state phase voltage u_A, phase current i_A, and line voltage v_{AB} of the experimental platform when injecting reactive currents to the grid with a 1300-V DC link voltage.

switching losses and the best clamping state in such a case will be "X0" as discussed in [12]. For the proposed DPWM, the lower current (i.e., the middle current defined in Section III) is considered for "X+" and "X-" selection.

Applying different modulation strategies, Fig. 12 presents the junction temperature variation of the clamping diode D5 when the peak value of the reactive current increases linearly from 0 A to 15 A with a 1 A/second slope. In Fig. 12(a), with the SPWM strategy and after 20 s operation, the junction temperature increases almost linearly from 24 °C to 37 °C. In contrast, the highest mean junction temperature is 30 °C in Fig. 12(b), where the modulation strategy is changed from the SPWM to the proposed DPWM when the peak current is higher than 10 A. It can be noted in Fig. 12(b) that, after switching to the proposed DPWM, the junction temperature has been declining for several seconds even the current is still increasing. After a one-second operation with the proposed DPWM, a 2-°C temperature drop has been achieved compared to that with the SPWM strategy. Although the above results can not quantitatively analyze the inverter thermal performance under LVRT operation, it suggests that the proposed DPWM can reduce the thermal stress of the most stressed devices during LVRT operation.

In the future, experimental tests under LVRT events will be performed to further assess the effectiveness of the proposed DPWM in distributing the thermal stresses among the switches and diodes of the 3L-NPC PV inverters.

VI. Conclusion

In this paper, the thermal stress of the 1500-V single-stage 3L-NPC PV inverter was investigated considering LVRT operation. The high DC-link voltage, high output current while low output voltage during LVRT operation make the clamping diodes suffer from much higher thermal stress than the other power devices, and this is mainly attributed to the high conduction losses of the clamping diodes. A modified DPWM has been proposed hereby to relieve the thermal stresses on the clamping diodes. The concept of the proposed DPWM is that the phase legs are only clamped to the positive or negative point of the DC link when they are corresponding

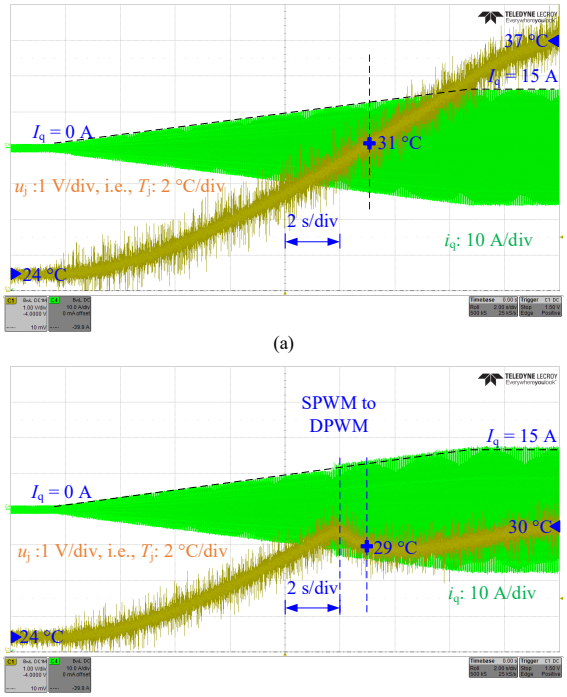

Fig. 12. Junction temperature $T_{j,D5}$ variations when the peak value of reactive current i_q increasing linearly from 0 A to 15 A with a 1 A/second slope: (a) SPWM only, (b) SPWM to DPWM when the current is higher than 10 A.

to the maximum or middle phase current. By doing so, the clamping diode will not carry the maximum current during LVRT operation, where more equal thermal distribution can be achieved. It is worth mentioning that when applying the proposed DPWM instead of the conventional CPWM during LVRT events, the 3L-NPC inverter may achieve a higher reactive current rating due to an improved thermal stress balance. In the future, experimental tests under LVRT events will be performed to further assess the effectiveness of the proposed DPWM in distributing the thermal stresses among the switches and diodes of the 3L-NPC PV inverters.

ACKNOWLEDGMENT

The authors would like to thank the College of New Energy at China University of Petroleum (East China) for providing technical support in developing the experimental prototype.

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