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Derivation, Design and Simulation of the Zeta converter

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Abstract—The purpose of this paper is to guide electrical engineering students from analysing basic DC-DC converter topologies to more advanced topologies. Textbooks and free online papers include the derivation of second order DC-DC topologies such as buck, boost and buck-boost, while fourth order such as the Zeta converter are not as readily available as open knowledge online. This paper provides a detailed derivation of the Zeta converter topology in continuous conduction mode (CCM), it presents an example of component sizing and verifies the design by simulation in LTspice.

I. INTRODUCTION

ELECTRICAL engineering students are typically introduced to the topic of switch mode power supplies through the analysis of basic second order DC-DC converter topologies such as the buck, boost and buck-boost converters. Derivation of these topologies are derived in detail available as online open-access sources [1]. However, generally for the fourth order DC-DC converter types Ćuk, Zeta and Single-Ended Primary-Inductor Converter (SEPIC) the detailed derivation of their operation is not as freely available. Fourth order DC-DC converters are mentioned in the most popular textbooks by Muhammad Rashid [2], Robert W. Erickson & Dragan Maksimovic [3] and Ned Mohan et al. [4], however they are not open access and derivations are not presented in detail either. Most of free online sources describing these fourth order DC-DC converter topologies most often focus on more advanced topics, such as state space control [5], comparison of total harmonic distortion [6] or design guidelines are given without much description on how to derive them [7]–[9].

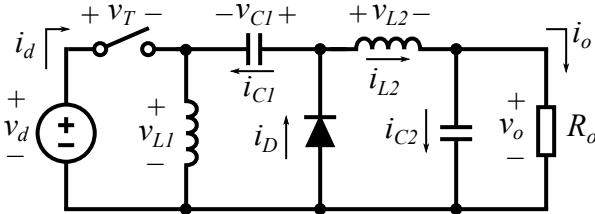


Fig. 1: Diagram of the Zeta converter.

This paper provides a detailed derivation of the Zeta converter, shown in Fig. 1, when operated in CCM. A design example is given and it is verified by simulation.

II. DERIVATION OF THE ZETA CONVERTER

In the following section instantaneous values of voltages and currents are denoted with lower case letters v and i , respectively, while capital letters V and I are used for average voltage and currents. The switch is turned on at $t = 0$ until $t = DT_s$ where T_s is the switching period and D is the duty cycle. The voltage and current waveforms of inductor L_1 are shown in Fig. 2.

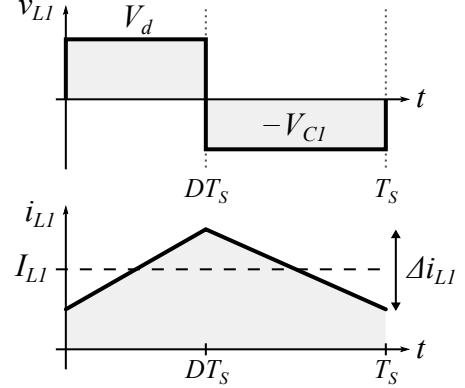


Fig. 2: Voltage and current waveforms of inductor L_1 .

For the converter operating in steady state and CCM, it is assumed that the current through the inductor begins and ends at the same value after an entire switching period. This is also known as the volt-second balance, meaning that the average of applied voltage on the inductor is equal to zero during a switching period, as given by

$$\frac{1}{T_s} \int_0^{T_s} v_{L1} dt = 0$$

Splitting the total switching period, T_s , into two segments at which the switch is turned on and off

$$\frac{1}{T_s} \left(\int_0^{DT_s} v_{L1} dt + \int_{DT_s}^{T_s} v_{L1} dt \right) = 0$$

During the time from $t = 0$ to $t = DT_s$ the voltage is $v_{L1} = V_d$, while from $t = DT_s$ to $t = T_s$ it is $v_{L1} = -V_{C1}$. Thus, the integral equals

$$\begin{aligned} \frac{1}{T_s} (V_d \cdot DT_s - V_{C1}(1-D)T_s) &= 0 \\ V_d \cdot D - V_{C1}(1-D) &= 0 \end{aligned}$$

Rearranging to get an expression for V_{C1} equals

$$V_{C1} = V_d \cdot \frac{D}{1-D} \quad (1)$$

Similarly, the voltage and current waveforms of inductor L_2 are shown in Fig. 3.

The volt-second balance of L_2 is calculated as

$$\begin{aligned} \frac{1}{T_s} \int_0^{T_s} v_{L2} dt &= 0 \\ D(V_{C1} + V_d - V_o) - V_o(1-D) &= 0 \\ D \cdot V_{C1} + D \cdot V_d - D \cdot V_o - V_o + D \cdot V_o &= 0 \end{aligned}$$

By collecting terms this equals

$$V_o = D \cdot V_{C1} + D \cdot V_d$$

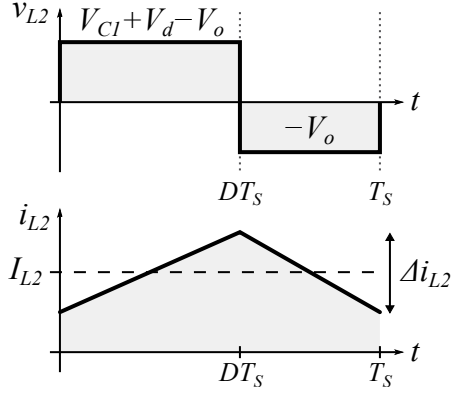


Fig. 3: Voltage and current waveforms of inductor L_2 .

Again, this is rearranged for V_{C1} to equal

$$V_{C1} = \frac{V_o}{D} - V_d \quad (2)$$

By combining (1) and (2)

$$V_d \cdot \frac{D}{1-D} = \frac{V_o}{D} - V_d$$

This expression is then solved for the conversion ratio, $M = \frac{V_o}{V_d}$

$$\begin{aligned} \frac{V_o}{D} &= V_d \cdot \frac{D}{1-D} + V_d \\ \frac{V_o}{V_d} &= \frac{D^2}{1-D} + D \\ \frac{V_o}{V_d} &= \frac{D^2 + D(1-D)}{1-D} \end{aligned}$$

And by combining all terms

$$M = \frac{V_o}{V_d} = \frac{D}{1-D} \quad (3)$$

Alternatively, it may be solved for the duty cycle, D

$$D = \frac{V_o}{V_d + V_o} \quad (4)$$

Thus for D in the range of 0 to 1, the Zeta converter is capable of both stepping the voltage up and down. If compared with the buck-boost or Čuk converter, the voltage output is non-inverting, meaning that it has the same polarity as the input voltage, where the buck-boost and Čuk converters are inverting.

Now (3) is rearranged to

$$V_d = V_o \frac{1-D}{D} \quad (5)$$

When inserting (5) to (1) we obtain an expression for the average voltage across the capacitor C_1

$$V_{C1} = V_d \frac{D}{1-D} = V_o \frac{1-D}{D} \frac{D}{1-D}$$

By cancelling terms we obtain

$$V_{C1} = V_o$$

This information could also have been obtained by assessing the diagram in Fig. 1. When the converter is operating in steady state, the volt-second balance means that the average voltage

across the inductors are zero. Thus, by applying Kirchoffs voltage law to the loop of L_1 , C_1 , L_2 and output V_o , then the average voltage across the capacitor must be equal to the output V_o .

Similarly, simply from assessing Fig. 1 and using the steady state assumption that the output capacitor C_o is large enough to maintain a stable voltage, we may also conclude that

$$V_{C2} = V_o$$

As we are now reading information from the diagram, we can also conclude that in steady state the average current in the capacitors are zero, thus if we apply Kirchoffs current law, we obtain

$$I_{L1} = I_d \quad (6)$$

and

$$I_{L2} = I_o \quad (7)$$

For an ideal lossless DC-DC converter, all power, P , is transferred from the input to the output.

$$P = V_d \cdot I_d = V_o \cdot I_o$$

Thus, if we use (5), we obtain that

$$I_d = \frac{D}{1-D} I_o \quad (8)$$

However, we are not only concerned with the average values of the inductor current in L_1 and L_2 . It is just as important to choose a large enough inductance, to ensure that the inductor current ripple is adequately low. From Fig. 2 we may see that the inductor current ripple, Δi_{L1} , can be expressed as.

$$\Delta i_{L1} = \frac{V_d D T_s}{L_1}$$

By inserting (5) and using that $f_s = 1/T_s$, where f_s is the switching frequency, we obtain that

$$\Delta i_{L1} = \frac{V_o(1-D)}{L_1 f_s} \quad (9)$$

From this equation we can see that to keep a low inductor current ripple, we may choose a large inductance or high switching frequency. The expression for inductor current ripple is also used to ensure that the converter operates in CCM. For the Zeta converter to always operate in CCM, it is required that the current is always above zero. The limit is when the inductor current just reaches zero at the very end of the switching period, $t = T_s$, as shown in Fig. 4.

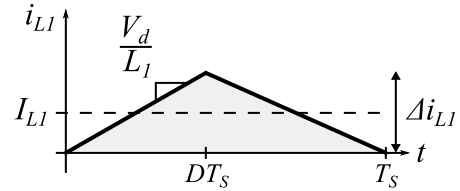


Fig. 4: Inductor L_1 current at its CCM limit.

At the CCM limit, from geometrical considerations, we may read that the DC-value of the inductor current is $I_{L1} = \frac{\Delta i_{L1}}{2}$. Thus, to ensure CCM we need that

$$I_{L1} \geq \frac{\Delta i_{L1}}{2} \quad (10)$$

Inserting both (6), (8) and (9) to (10) we obtain

$$\frac{D}{1-D} I_o \geq \frac{V_o(1-D)}{2L_1 f_s}$$

This expression is rearranged to isolate L_1

$$L_1 \geq \frac{(1-D)^2 V_o}{2D f_s I_o}$$

Substituting $R_o = V_o/I_o$ we get the following expression for the minimum size of inductance L_1 to ensure that it is operating in CCM.

$$L_1 \geq \frac{(1-D)^2 R_o}{2D f_s} \quad (11)$$

Similarly for sizing of L_2 , we need an expression for the inductor current ripple of L_2 , denoted as Δi_{L2} . Geometrically from Fig. 3, we see that

$$\Delta i_{L2} = \frac{V_o(1-D)T_s}{L_2} \quad (12)$$

The limit to ensure CCM for the current in inductor L_2 is shown Fig. 5.

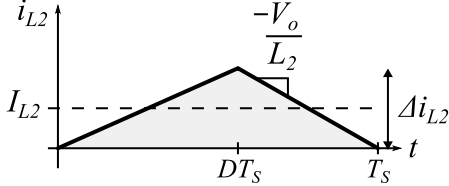


Fig. 5: Inductor L_2 current at its CCM limit.

Geometrically, the following equation must be fulfilled

$$I_{L2} \geq \frac{\Delta i_{L2}}{2} \quad (13)$$

Inserting (7) and (12) to (13) equals

$$I_o \geq \frac{V_o(1-D)T_s}{2L_2}$$

Rearranging the equation to isolate L_2 , once again using that $T_s = 1/f_s$ and $R_o = V_o/I_o$ gives the following equation for the minimum required inductance to ensure CCM operation.

$$L_2 \geq \frac{(1-D)R_o}{2f_s} \quad (14)$$

In addition to the sizing of inductors and maximum allowable current ripple, it is also important to size the capacitors C_1 and C_2 for a maximum allowable voltage ripple, ΔV . To size the capacitors, we will utilize that the capacitance is defined as $C = \frac{dQ}{dV}$, where Q is the electric charge. By rewriting to an average rate of change, we get $\Delta V = \frac{\Delta Q}{C}$. The amount of charge is given as the integral of current $\Delta Q = \int i(t)dt$. Now, for C_1 if we assume negligible current ripple, it is discharged by $I_{L2} = I_o$ during the switch on time, as shown in Fig. 6.

From the following observations we obtain the following equation

$$\Delta V_{C1} = \frac{\int_0^{DT_s} I_o dt}{C_1}$$

which equals

$$\Delta V_{C1} = \frac{I_o DT_s}{C_1}$$

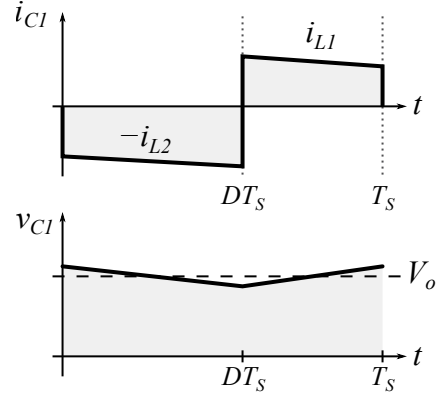


Fig. 6: Current and voltage waveforms of capacitor C_1

By rearranging for the value of C_1 , we get that

$$C_1 = \frac{I_o D}{\Delta V_{C1} f_s}$$

Typically, we will assign a requirement that the ripple of the capacitor voltage may not exceed some predetermined level, i.e. 1 or 5 % of its DC-value. Thus, the equation should be written as

$$C_1 \geq \frac{I_o D}{\Delta V_{C1} f_s} \quad (15)$$

For sizing of C_2 we use geometrical approximations, as shown in Fig. 7. Similarly to the sizing of C_1 , we are interested in the change in charge, which is also the integration of current. The voltage and current waveforms of C_2 are shown in Fig. 7.

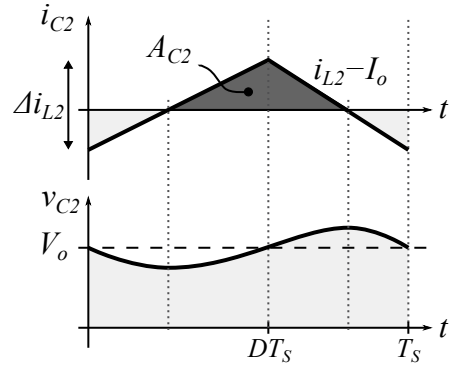


Fig. 7: Current and voltage waveforms of capacitor C_2

Now, the charge which determines the voltage change of C_2 , is shown as the area A_{C2} . Geometrically we obtain that

$$A_{C2} = \frac{1}{2} \frac{T_s}{2} \frac{\Delta i_{L2}}{2}$$

Collecting the terms and using (12) for Δi_{L2} , we get that

$$A_{C2} = \frac{T_s}{8} \cdot \frac{V_o(1-D)T_s}{L_2}$$

However, this only represents the charge. To size the capacitor we utilize $C = \frac{\Delta Q}{\Delta V}$, where $\Delta Q = A_{C2}$. For C_2 this gives

$$C_2 \geq \frac{A_{C2}}{\Delta V_{C2}} = \frac{V_o(1-D)}{8 \cdot L_2 f_s^2 \Delta V_{C2}} \quad (16)$$

This concludes the section, as we now have equations for the sizing of all passive components, L_1 , L_2 , C_1 and C_2 .

III. COMPONENT SIZING

The following section presents a simple Zeta converter design example. The input voltage of the converter is $V_d = 20\text{V}$, while its output must be maintained at $V_o = 60\text{V}$. The load resistance can be in a range of 50 to 100Ω . Since $P = \frac{V_o^2}{R_o}$, we calculate the output power is in the range of 36 to 72W .

As a design engineer, we have chosen that the switching frequency is $f_s = 50\text{kHz}$, and that the maximum voltage ripple of both capacitors should be maximum 1% of the output voltage, thus $\Delta V_{C1} = \Delta V_{C2} = 0.01 \cdot V_o = 0.6\text{V}$. The converter must be operating in CCM.

First we calculate the duty cycle, D using (4)

$$D = \frac{V_o}{V_d + V_o} = \frac{60\text{V}}{20\text{V} + 60\text{V}} = 0.75$$

To size the inductor L_1 we use (11) as shown

$$L_1 \geq \frac{(1-D)^2 R_o}{2Df_s}$$

The worst case condition is when $R_o = 100\Omega$, which is equivalent to a low output current. Inserting numbers we obtain that L_1 must have a minimum value of

$$L_1 \geq \frac{(1-0.75)^2 \cdot 100\Omega}{2 \cdot 0.75 \cdot 50\text{kHz}} = 83.33\mu\text{H}$$

Next is the sizing of inductor L_2 , given by (14)

$$L_2 \geq \frac{(1-D)R_o}{2f_s}$$

Once again, the worst case for this inductor, is when the output current is low i.e. closer to zero, which is the CCM limit. Thus, L_2 should have a minimum size of

$$L_2 \geq \frac{(1-0.75) \cdot 100\Omega}{2 \cdot 50\text{kHz}} = 250\mu\text{H}$$

Now for the sizing of the capacitor C_1 we use (15)

$$C_1 \geq \frac{I_o D}{\Delta V_{C1} f_s}$$

The worst condition for the capacitor voltage ripple is when the output current, I_o , is high. For a fixed output voltage of $V_o = 60\text{V}$, the highest output current occurs when the resistance is $R_o = 50\Omega$. This equals an output current of $I_o = \frac{V_o}{R_o} = \frac{60\text{V}}{50\Omega} = 1.2\text{A}$. Thus, the minimum capacitance of C_1 required, which ensures a voltage ripple of less than 0.6V , is calculated

$$C_1 \geq \frac{1.2\text{A} \cdot 0.75}{0.6\text{V} \cdot 50\text{kHz}} = 30\mu\text{F}$$

Similarly, using (16) for C_2 the minimum required capacitance

$$C_2 \geq \frac{V_o(1-D)}{8 \cdot L_2 f_s^2 \Delta V_{C2}}$$

Inserting values

$$C_2 \geq \frac{60\text{V} \cdot (1-0.75)}{8 \cdot 250\mu\text{H} \cdot (50\text{kHz})^2 \cdot 0.6\text{V}} = 5\mu\text{F}$$

This concludes the section, as all four passive components have been sized for operation in CCM. Note, that this example of a Zeta converter design procedure only had a single varying parameter. If necessary, see [10] for an example of a SEPIC converter with multiple design parameters being in a range.

IV. SIMULATION

In the following section, the circuit simulation software LTspice [11] is used to verify the converter design values calculated in Section III. The LTspice circuit schematic and the required SPICE directives used to specify the models for the switch and diode are shown in Fig. 8 The SPICE directives

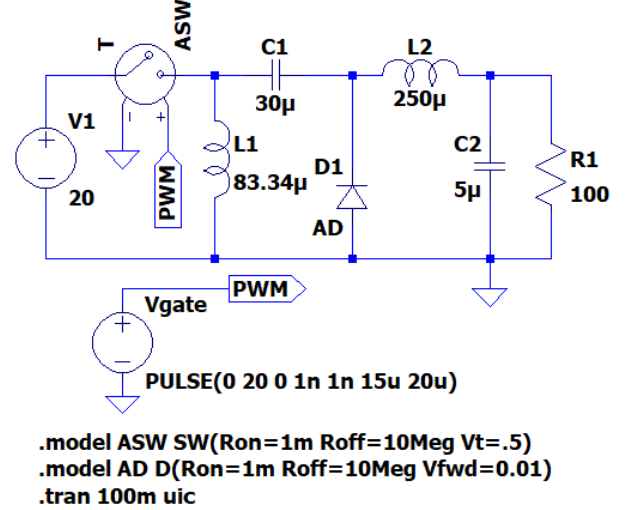


Fig. 8: LTspice schematic of Zeta converter.

from Fig. 8 are also given below for ease of copying:

```
.model ASW SW(Ron=1m Roff=10Meg Vt=.5)
.model AD D(Ron=1m Roff=10Meg Vfwd=0.01)
.tran 100m uic
```

The devices in LTspice cannot be ideal, and thus they do not turn on/off instantly and they are neither perfect conductors or have infinite resistance in their on and off state, respectively. The switch and diode models are given in line 1 and 2. The on-resistance of both devices is defined as $1\text{m}\Omega$ and an off-resistance of $10\text{M}\Omega$. The gate threshold voltage of the switch is set at 0.5V , while the forward voltage of the diode is defined at 0.01V . Line 3 specifies a transient non-linear analysis stopping after 100ms , and that the circuit is solved without calculating initial conditions for any of the inductive or capacitive elements, meaning that all voltages and current start at zero.

The gate signal is defined as a voltage source pulse train, having a time period of $T_s = 1/f_s = 1/50\text{kHz} = 20\mu\text{s}$. For a duty cycle of $D = 0.75$, this means that the turn-on period is $T_{on} = T_s \cdot D = 15\mu\text{s}$. This signal is then supplied to the switch.

The circuit is now ready for simulation. First we want to validate that the converter is operating on the limit of CCM, when the output current is at its lowest limit, equivalent to an output resistance of $R_o = 100\Omega$. Shown in Fig. 9 is the inductor current of both L_1 and L_2 . It is seen that the inductor currents reach zero just at the end of the switching period, as predicted by the design equations (11) and (14). Next, we want to verify that the voltage ripple of capacitors C_1 and C_2 is below the requirement of 0.6V , when the converter is operating at its maximum power output, which occurs at a power output of 72W . Thus, the output load resistance is changed to $R_o = 50\Omega$

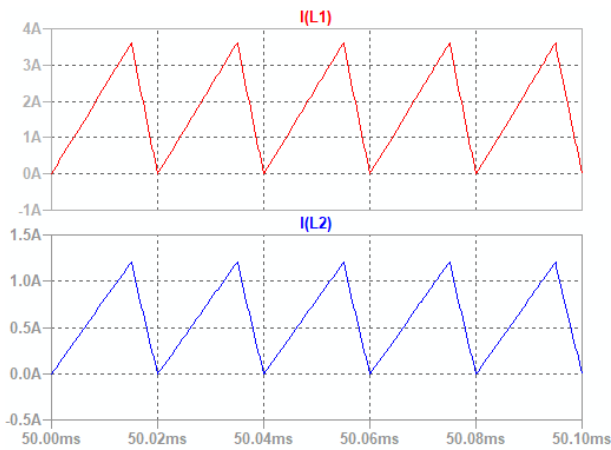


Fig. 9: Simulated $i_{L1}(t)$ and $i_{L2}(t)$ at $R_o = 100\Omega$.

in LTspice, and the simulation is run again. The voltage across the capacitors C_1 and C_2 are shown in Fig. 10. For both of

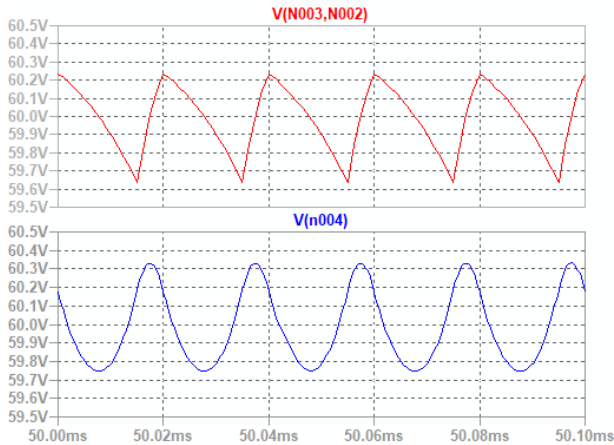


Fig. 10: Simulated $v_{C1}(t)$ and $v_{C2}(t)$ at $R_o = 50\Omega$.

the capacitors it is read that the voltage ripple is at the limit of the specified 0.6 V. Secondly, the approximated triangular waveform shape of $v_{C1}(t)$ and sinusoidal-like shape of $v_{C2}(t)$, which was shown in Fig. 6 and 7, are justified. This verifies the design equations of Section III and concludes this section.

V. CONCLUSION

A thorough derivation of fourth order DC-DC converter topologies is generally lacking in open access literature. This creates a knowledge gap for engineering students in moving from simple DC-DC topologies like buck, boost or buck-boost to Ćuk, SEPIC or Zeta. This paper provides a detailed derivation of the required equations to design a Zeta DC-DC converter topology for operation in CCM. Following the derivation, a simple design example is given for a case with variable load resistance. The converter design is verified by simulation in LTspice. The analytical equations show good compliance with the simulated waveforms.

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