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Article

Electrical Stress on the Medium Voltage Medium Frequency Transformer

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Abstract: This paper proposes an equivalent circuit model to obtain the transient electrical stress quantitatively in medium voltage medium frequency transformers in modern power electronics. To verify this model, transient simulation is performed on a 1.5 kV/1 kHz transformer, revealing voltage overshoot quantitatively between turns and layers of the transformer's HV winding. Effects of rise time of the input pulse voltage, stray capacitance of the winding insulation, and their interactions on the voltage overshot magnitude are presented. With these results, we propose limiting the voltage overshoot and, thereafter, enhancing medium voltage medium frequency transformer's insulation capability, which throws light on the transformer's insulation design. Additionally, guidance on the future studies on aging and endurance lifetime of the medium voltage medium frequency transformer's insulation could be given.

Keywords: MVMF transformer; insulation; pulse voltage; electrical stress

1. Introduction

In several modern power electronic systems, a transformer is one of the most critical devices serving as voltage scaling up/down, electrical isolation, and power transmission. One of the typical topologies of the power electronic system with transformers commonly used in power distribution and transportation fields is shown in Figure 1 [1]. Connected with power electronic switches on both sides, these transformers are working under voltage with magnitude from several to tens of kV, while the frequency is in the range from hundreds of Hz to tens of kHz (depending on the electrical capability of modern IGBT and MOSFET). Because of their working conditions characteristics, these transformers are called medium voltage medium frequency (MVMF) transformers. Compared with a conventional transformer working under 50/60 Hz sinusoidal voltages in an HV power delivery system, an MVMF transformer has quite a different overall layout with a smaller size. Combined with power electronic switches, these transformers also have higher controllability than the conventional ones [2]. So, they are widely used in modern power electronic applications, such as railway traction, DC grids, etc. Recently, MVMF transformers have further reduced size to reach lower costs and higher power densities. However, along with the development of MVMF transformers, challenges exist such as increased hysteresis loss and conductor loss due to higher working frequency. These factors can lead the transformer to overheating. Additionally, another important challenge is related to insulation reliability, since the MVMF transformer may be faced with fast insulation degradation due to electrical overstress [3].

The waveform of the voltage applied to the MVMF transformer is the medium-frequency PWM pulse. It has a much shorter rise time compared with the sinusoidal voltage. So, the electrical stress faced by the transformer's insulation system would be different from that of traditional transformers working under power frequency sinusoidal voltages. Previous research on inverter-fed motors shows that when pulse voltage with short rise time is added to the multi-turn winding, oscillation on the rising edge of the

voltage between turns can be induced. As a result, a transient voltage with a much higher peak value than the static voltage drop between turns is reached [4]. What is more, the voltage distribution among turns is uneven. Usually, the turns closest to the voltage source output terminals would suffer from the highest peak voltage values [5]. Since transformers also have multi-turn windings, when working in MVMF power electronic conditions, the similar phenomenon of interturn overvoltage and uneven voltage distribution may also exist. If so, the probability of partial discharge (PD) occurrence in the interturn insulation of the transformer would be higher [6]. Continuous PD can degrade the insulation material quickly and greatly shorten the time-to-failure of the transformer in MVMF application [7]. When PD is combined with temperature rise due to increased hysteresis loss and conductor loss, the insulation aging rate may be even faster [6]. As MVMF transformers are developing to be smaller in size, which means the insulation distance may also be reduced inevitably, insulation issues caused by unusual electrical stress would probably be more serious. In addition, for transformers with multi-layer windings, not only the interturn insulation, but also the interlayer insulation may suffer from electrical overstress brought from the pulse operating voltage. Therefore, research on the insulation problems of the MVMF transformers is also necessary.
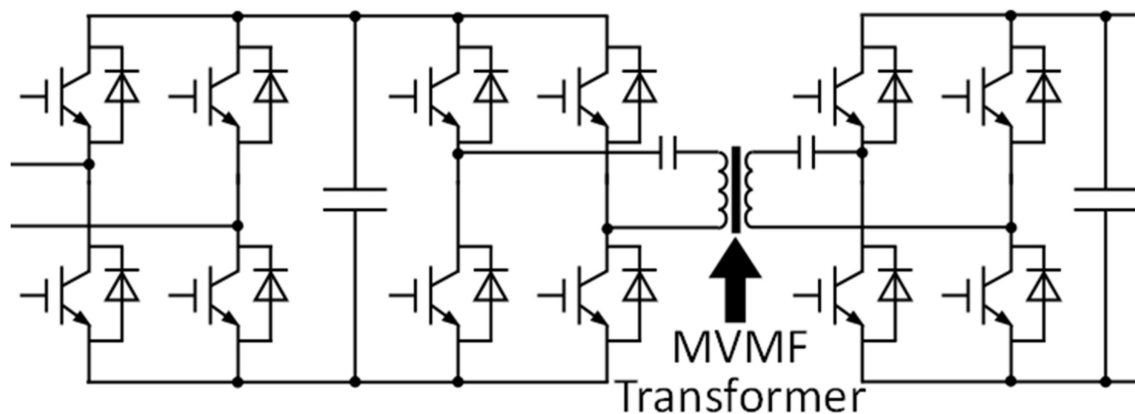

Figure 1. A typical topology with a medium voltage medium frequency transformer.

Some researchers have already investigated the electrical stress on the MVMF transformers and take strategies to deal with it. In [8], the author conducts an FEM electric field simulation and finds that the electrical field concentrates mostly in one side of the turns of HV winding that is facing the LV winding. Zheng in [9], proposes a segmented winding structure to reduce the largest interlayer voltage in an MVMF transformer's winding. Authors in [10] find that adding an angle ring and electrostatic ring within the transformer's structure can reduce the value of peak electric field intensity. For the design of MVMF transformers in [11,12], authors apply extra semi-conductive layers on the surface of the winding insulation. Electric field simulation shows that this method can effectively reduce the electric field intensity in air gaps between winding and core. Although this research can surely be advantageous to the improvement of insulation capabilities of MFMV transformers, they mostly focus on the steady-state electric field/voltage simulation. As mentioned before, the most obvious difference between MVMF and conventional transformers with respect to the insulation problem is the transient overvoltage and uneven voltage distribution that may happen within the MVMF transformer's winding when working under pulse voltage with a short rise time. Steady-state simulation ignores the transient response in the MVMF transformer's winding when exposed to pulse voltage with very short rise time and frequency much higher than the power frequency. Consequently, the maximum electrical field magnitude applied to the winding insulation is underestimated.

Yet, some previous research on the electrical stress of inverter-fed motors provides good suggestions regarding the way of studying the electrical stress of MVMF transformers working under similar electrical condition, since they pay a lot of attention to transient

voltage drop within the winding. In [13], Wan conducts an FEM calculation to obtain stray parameters of a motor prototype's winding and builds an equivalent circuit model of the winding. Based on that, interturn voltage drop simulation under pulse voltage is conducted. Results show that the overshoot of the voltage drop on the first turn is higher than that on other turns, which means voltage distribution within the winding is uneven. In [14], Wen conducts interturn voltage simulation similar to that of Wan's and finds that reducing the capacitance to ground of the turns can decrease the peak interturn voltage value. Krings analyzes inter-coil (consists of several turns) voltage waveform of an HV motor working under PWM voltage [15]. He discovers that the voltage drop between the first two coils is usually the highest and increasing the rise time of pulse voltage makes the voltage between different adjacent coils distribute more evenly. The experiment results on a real prototype are in high accordance with that of simulation. Moghadam conducts experiments on interturn voltage within a single coil of a motor under different electrical parameters [16]. The author finds that besides shorter rise time, the longer pulse width can also bring a stronger interturn voltage drop, leading to a more serious electrical stress on the coil's insulation. Table 1 summarizes the comparison among the reviewed studies and this paper with respect to contributions and inadequacies from the perspective of MVMF transformer.

Table 1. Comparisons between reviewed studies and this paper from the perspective of an MVMF transformer.

Reference Number	Contribution	Inadequacies	Advantage of This Paper
[8–12]	• Reveal the position of the electrical field hot point in the transformer's winding. • Propose a suitable method to reduce the interlayer overvoltage and electric field intensity in the air gap within the winding.	• Transient response from the winding, when exposed to pulse voltage, is not considered. • The maximum electrical stress in the winding insulation is underestimated.	• Sufficiently consider the effect of transient overvoltage in the winding exposed to pulse voltage. The maximum electrical stress in the winding is obtained with enough accuracy.
[13–16]	• Reveal the interturn and inter-coil overvoltage within the winding of inverter-fed motors. • The strongest electrical stress brought from transient overvoltage caused by pulse voltage is adequately considered.	• Not accurate enough to predict the electrical stress of MVMF transformers due to the difference in winding structures between motors and transformers.	• Predict the electrical stress of MVMF transformers with higher accuracy, since this study directly focuses on the MVMF transformer.

Considering that the winding structure of the transformer is not the same as that of the motor, conclusions from the studies on electrical stress of inverter-fed motors cannot be directly used for that of MVMF transformers. Although, in decades before, studies have been conducted focusing on surge distribution in power frequency transformers [17,18], the electrical stress brought from repetitive PWM voltage may not be the same as these single pulses. Besides, the MVMF transformer is different from conventional power transformers with respect to the size and layout of windings and cores, when added with similar pulse voltage, the electrical stress may also show different characteristics. Therefore, investigation on electrical stress suffered by MVMF transformers through transient voltage analysis is necessary.

Aiming at investigating the transient maximum electrical stress of MVMF transformer that is not covered by previous papers and combined with the advanced methods from the studies on inverter-fed motors, this article builds an equivalent circuit model of a transformer' HV winding through software Ansys Q3D and MATLAB. Based on that, a simulation on the electrical stress in the winding is conducted. The results confirm

the existence of interturn and interlayer overvoltage. Mechanism of the occurrence of interturn/layer overvoltage and the factors that can influence it are analyzed. According to the mechanism, measures to improve the insulation capability of an MVMF transformer can be proposed.

2. Transformer Prototype for the Simulation

A transformer prototype proposed in the literature [8,19] is selected as a typical case for the electrical stress study. The reason for choosing this prototype is that this transformer is a typical MVMF transformer, which is inherently different from a power transformer with respect to design and operating voltage. Therefore, this prototype fits with our paper's scope. Besides, its voltage and frequency ratings (1.5 kV and 1 kHz, respectively) are common among the prevailing MVMF transformers. In addition, this transformer is designed to be used in a power electronic transformer system (PET), which will be widely applied in fields such as the distribution system, DC grid, and high-speed railway systems. Therefore, study on this prototype has a certain extent of universality, which can be beneficial for insulation improvement of other MVMF transformers in similar applications. Its basic parameters are depicted in Table 2.

Table 2. Basic parameters of the transformer prototype.

Electrical Parameters	Value
Operation frequency	1 kHz
Rated power	35 kW
Turn ratio	120:32
Rated voltage of HV winding	1500 V
Rated voltage of LV winding	400 V
Design Parameters	**Type**
Core material	Ferrite (with permeability 1900)
Core size (width/height/thick)	27 cm/19 cm/10 cm
Core structure	Core type
Window area	105 cm^2
Primary winding conductor	2 mm $\times$ 5 mm flat copper wire
Secondary winding conductor	0.4 mm $\times$ 110 mm copper foil
Insulation material	Polyimide
Interturn insulation distance	1 mm (primary)/0.3 mm (secondary)
Inter-winding insulation distance	1.5 mm

The transformer's overall 3D outlook and 2D partial cross-section of its winding are shown in Figure 2. Its HV winding is made from flat copper wires with 5 mm in height and 2 mm in width. Its LV winding is made of copper foils. Both of the windings are distributed on each limb of the core evenly, and the HV winding has three layers. Since this paper focuses on the study on electrical stress rather than insulation degradation or breakdown, we simply assume that this transformer prototype is in a very good insulation condition with all the gaps between conductors completely filled with insulation (seen in yellow area in Figure 2). For HV winding, interturn insulation and interlayer insulation distance are 0.6 mm and 1 mm, respectively. While the insulation distance of LV winding is 0.3 mm. The core made by ferrite (with relative permeability 1900) has a core-type structure with dimensions of 27 cm in height, 19 cm in width, and 10 cm in thickness, whereas the window area is 105 cm^2. With today's transformer design and manufacturing technology, usually the electrical field intensity within the LV winding is low [20]. So, the probability of facing serious insulation problems by LV winding is much lower than that of HV winding. Therefore, the study on the electrical stress in this transformer prototype would only focus on the HV winding.
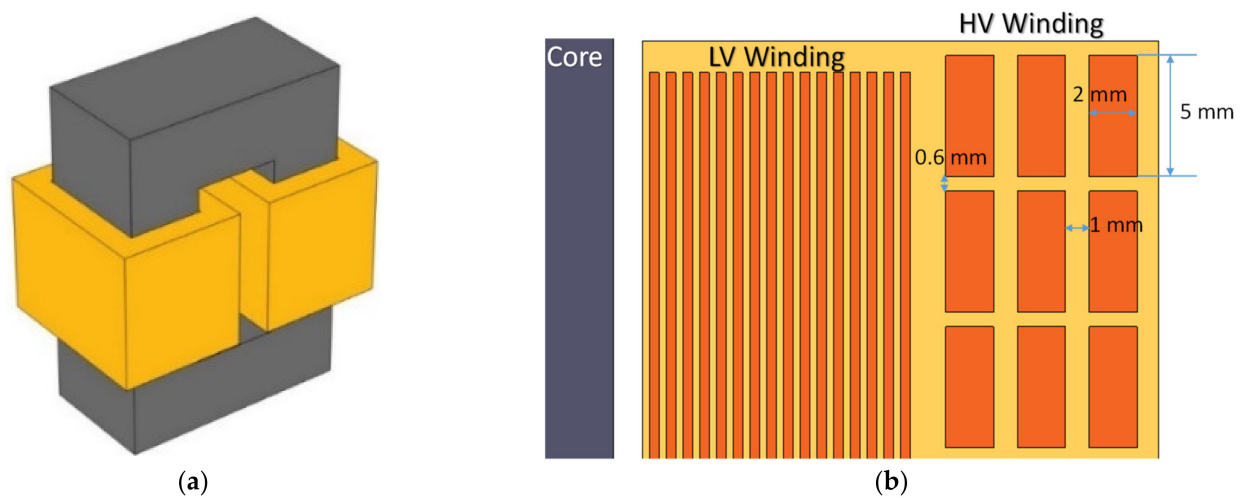
Figure 2. Transformer prototype: (**a**) 3D outlook; (**b**) partial 2D cross-section of the winding.

3. Equivalent Model of HV Winding

To conduct the transient voltage simulation in the HV winding, an equivalent circuit model of the winding should be built [14]. In the building of the circuit model, stray parameters of each turn of the HV winding are considered including resistance, capacitance, and inductance. All of these aforementioned parameters are calculated in FEM-based software, Ansys Q3D. The model used in the FEM calculation is 3D model as depicted in Figure 2. The material of turns is set as copper, while the original insulation material is set as polyimide with relative permittivity of 3.9 (in Section 5, these stray parameters are recalculated with different insulation materials). In the FEM calculation, Dirichlet boundary condition is used as the electromagnetic field boundary condition [14], the potential function is expressed by (1)

$$\varnothing|_r = g(\Gamma_1) = 0 \tag{1}$$

where Γ_1 is the Dirichlet boundary, and $g(\Gamma_1)$ is the ecumenical function of position. The element type is quadrilateral.

3.1. Stray Capacitance

According to the FEM calculation results, capacitances between non-adjacent turns (for example, C_{1-3}) are very small compared with that between adjacent turns (for example, C_{1-2}). In addition, due to the long distance between HV winding and core (longer than 12 mm), turn-to-core capacitances are much smaller than interturn capacitances. Therefore, interturn capacitances between non-adjacent turns and turn-to-core capacitances are ignored. In this three-layer HV winding structure, interlayer capacitances, such as C_{1-40} shown in Figure 3 (numbers in the figure refer to the serial numbers of the turns in the winding), should be taken into consideration because their values are comparable with the interturn capacitances such as C_{1-2}.
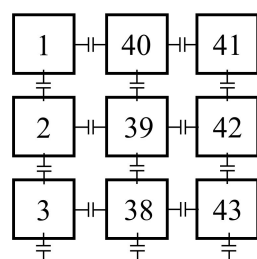

Figure 3. Stray capacitance taken into consideration.

3.2. Inductance and Resistance

In this case study, the voltage waveform for the simulation is square wave pulse voltage with a very short rise time. It is known that this kind of voltage is a combination of a sinusoidal wave voltage with fundamental frequency and a series of odd harmonics [21]. When a higher order of harmonics is added to form the square wave, its waveform is closer to an ideal square wave. That is to say, the rise time is shorter. This formation of the square wave can be expressed through Figure 4, where the peak-to-peak value and frequency of the square wave are in accordance with that listed in Table 2.
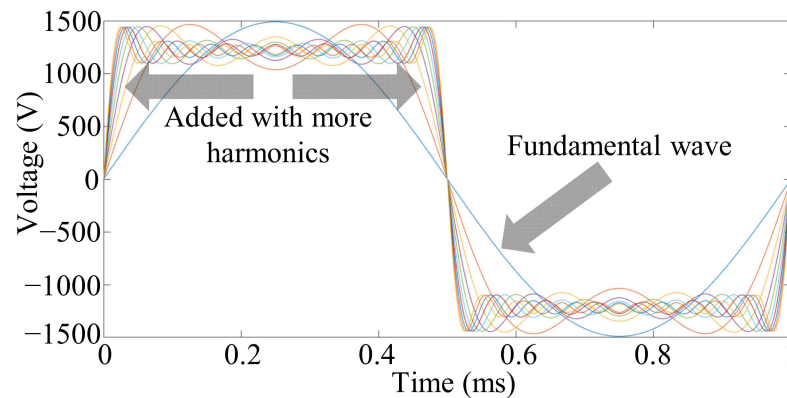

Figure 4. Formation of the square wave.

The equivalent highest frequency f_u of a pulse voltage with a fixed rise time can be calculated approximately by (2) [22]:

$$f_u = \frac{1}{\pi t} \tag{2}$$

where t is the voltage rise time. In PWM-like voltages produced from power electronic switches, it is usually in a range from hundreds of ns to several μs. Inductance can be affected by frequency. Additionally, the resistance will increase due to the skin and proximity effects under higher frequencies. So these two parameters are calculated in the frequency domain with the frequency of the aforementioned high-order harmonics taken into consideration. Because of the effect from the core with high relative permeability, strong mutual inductive coupling exists among the turns even though they are not close to each other. Therefore, a 120×120 mutual inductance matrix obtained from the FEM calculation is used in the building of the equivalent circuit model.

4. Analysis on the Mechanism of Overvoltage

With the FEM calculation by Ansys Q3D discussed in the last section, stray parameters of the winding are obtained. These parameters include resistance and self-inductance of each turn along with mutual (interturn/layer) capacitances and mutual inductances between different turns (expressed as Rx, Lx, Cx-y, and Mx-y, respectively, x and y vary from 1 to 120). Based on that, an equivalent circuit model of the transformer's HV winding is constructed in MATLAB's module Simulink, shown in Figure 5. Value ranges of the stray parameters are listed in Table 3, where R, L, and C in the table refer to RX, LX, and Cx-y in Figure 5, respectively. A voltage source that can generate pulse voltage with adjustable magnitude, frequency, and rise time is connected between the first turn and the last turn of the winding's circuit model. Set the pulse voltage's peak-to-peak value and frequency as 1500 V and 1 kHz, respectively, and the rise time as 100 ns, the first simulation is conducted. During this simulation, the interturn voltage drops within the first six turns are recorded (expressed as V1–2, V2–3, V3–4, V4–5, and V5–6, respectively). Typical waveforms of these interturn voltage drops in a half period are shown in Figure 6. It is clear that strong oscillations exist on the rising edge of the pulse voltage. This oscillation lasts for more

than 30 µs and leads to a peak voltage value above 22 V, which is much higher than the static voltage value (around 4.7 V). To understand why this overvoltage would happen and which factors can bring influence on it, analysis is needed.
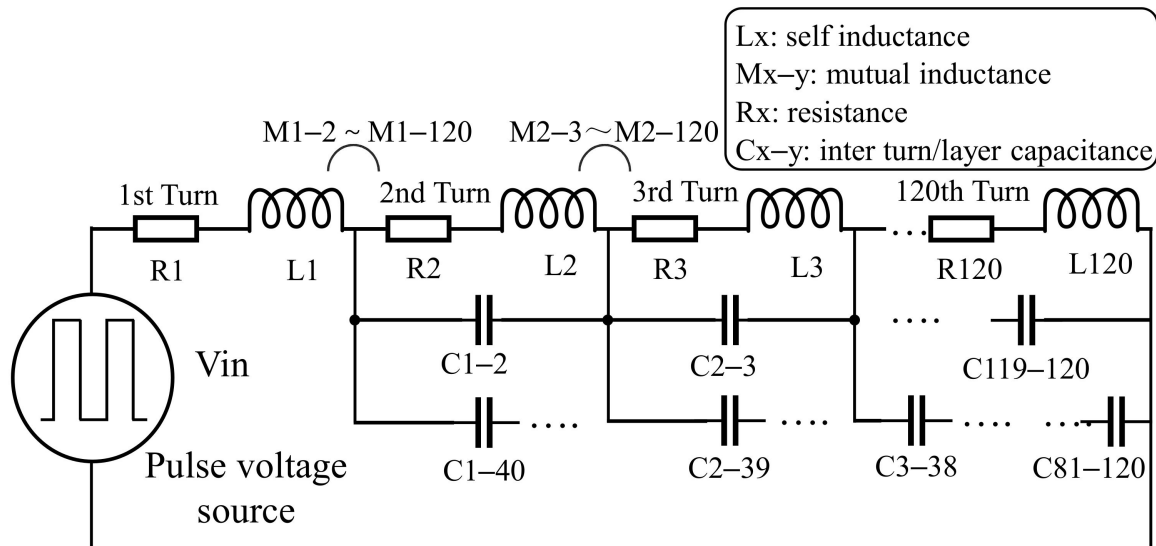

Figure 5. Equivalent circuit model of the transformer's HV winding (values of Lx, Rx, and CX–Y lies in the range of R, L, and C listed in Table 3).

Table 3. Value ranges of the stray parameters of the selected transformer prototype.

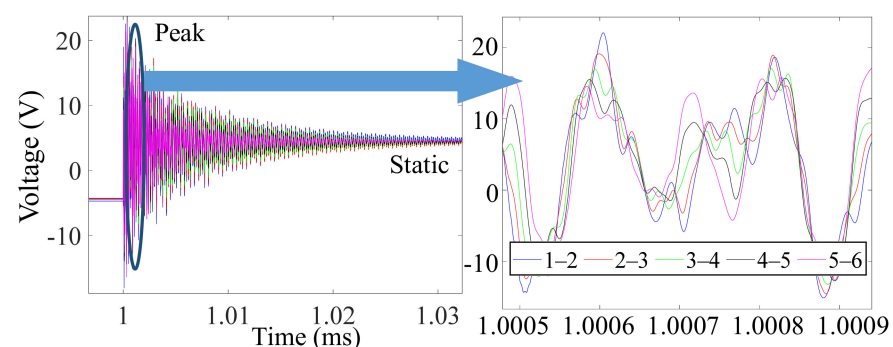| Parameters	Range
Resistor (R)	0.03–0.06 Ω
Inductance (L)	50–70 nH
Capacitance (C)	50–80 pF

Figure 6. Overall (**left**) and partial zoom in (**right**) of the rising edge interturn voltage drop waveform on the rising edge of pulse voltage.

Since the model in Figure 5 is a very complex model with 120 turns and three layers, analyzing the mechanism of occurrence of overvoltage through this complete model would be very complicated. Yet, in this transformer prototype, interturn insulation distance (0.6 mm) is shorter than interlayer insulation distance (1 mm). So, interturn capacitance is larger than the interlayer capacitance and would play a more important role in affecting the transient interturn voltage. Therefore, to reduce the complexity of the overvoltage mechanism analysis, we simplify this model into a single-layer winding with (n + 1) turns, in which the interlayer capacitances are ignored. This simplified circuit model can be seen in Figure 7. R, L, and C values of each turn are regarded as the same, and the mutual inductance is ignored to reduce the complexity of the following calculation on the

output voltage. Then, we conduct Laplace transformation for the impedance in this circuit. Impedance $Z_{i+1,i+2}$ $(0 < I \leq n)$ between adjacent points (point 1 and 2, 2 and 3, . . . N + 1 and N + 2) can be expressed by (3).

$$Z_{12}(s) = R + Ls, \; Z_{i+1, \; i+2}(s) = \frac{R + Ls}{LCs^2 + RCs + 1} \tag{3}$$
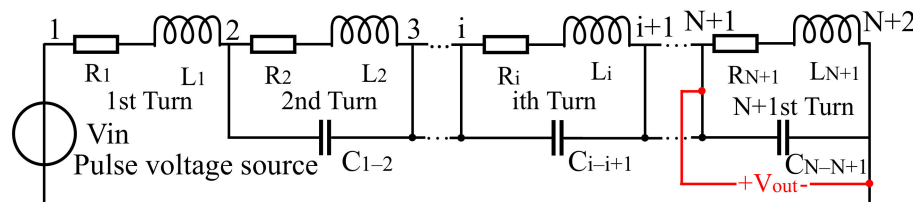

Figure 7. Simplified circuit model.

To find why pulse voltage can generate overvoltage between turns, the relationship between the input pulse voltage V_{in} and interturn output voltage should be expressed. We regard the voltage drop on the $(n + 1)$th turn as the output voltage V_{out}; then, the transfer function between V_{in} and V_{out} is obtained through (4). Through factorization, (4) can be simplified into (5). In this equation, $n + 1$ means the total number of turns.

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{Z_{n+1,n+2}(s)}{Z_{12}(s) + \sum_1^n Z_{i+1,i+2}(s)} = \frac{R + Ls}{L^2Cs^3 + (2RCL)s^2 + (R^2C + (n+1)L)s + (n+1)R} \tag{4}$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{R + Ls}{(R + Ls)(LCs^2 + CRs + n + 1)} = \frac{1}{LC}\left(\frac{1}{s^2 + \frac{R}{L}s + \frac{n+1}{LC}}\right) \tag{5}$$

Then, we can change the circuit model in Figure 7 into an open-loop system shown in Figure 8. Considering that the pulse voltage generated from the practical voltage source is not an ideal step voltage, rise time surely exists. So, the input voltage should be expressed with the combination of a step function and a first-order inertia link $1/(Ts + 1)$ in Function 1 according to the principle of automatic control [23], where T is the time constant, and the rise time equals 2.2 T. Function 2 is a typical two-order system. With these transfer functions in Figure 8, we would be able to analyze the mechanism of the overvoltage and factors that can influence it quantitatively based on the theory of automatic control. Considering the value ranges of R, L, and C obtained from the FEM calculation in Table 3, poles of Function 2 are certainly in the form of $A \pm jB$ (both A, B < 0). So, the waveform of interturn voltage drop is a pulse voltage with damping oscillation on its rising edge as seen in Figure 6, which is similar to that from previous research on the inverter-fed motors [4]. From function 2, natural frequency ω_n and damping ratio ξ can be expressed by (6).

$$\omega_n = \sqrt{\frac{n+1}{LC}}, \; \xi = R\sqrt{\frac{C}{4L(n+1)}} \tag{6}$$
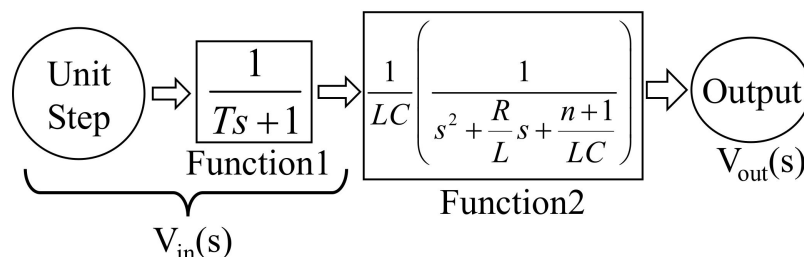

Figure 8. Transfer function of the simplified circuit model.

We can see that increasing the values of R and C can lead to a higher damping ratio, so the oscillation is supposed to be weaker, while increasing the value of L can reduce the damping ratio, giving rise to a stronger oscillation. To prove this deduction, we conducted the simulation with the simplified circuit in Figure 7 to see the changing of the overshoot with the changing of the abovementioned parameters. During the simulation, the value of n in (5) was set to 1 to reduce the simulation time; then, the model in Figure 7 changed into the simplest winding with only two turns. The simulation parameters and the obtained overshoot of the V_{out} are shown in Table 4. Set the transient peak voltage value as V_{peak} and static voltage value as V_{static}; then, overshoot σ is obtained through (7).

$$\sigma = \frac{V_{peak} - V_{static}}{V_{static}} \tag{7}$$

Table 4. Simulation on the simplified circuit model.

Group	L (nH)	R (Ω)	C (pF)	σ (%)
A	50	0.04	50	10.7
B	500	0.04	50	32.84
C	50	0.4	50	8.46
D	50	0.04	500	32.24

Values of the parameters in Group A are in accordance with the value ranges of stray parameters of turns of the transformer model from FEM calculation (listed in Table 3). The other three groups in Table 4 are applied for the comparison of the overshoot under different L, R, and C values. The rise time of the pulse voltage is set to be 20 ns and the peak voltage as 1 V. Comparing the results of group A with groups B and C, we can see that increasing the value of L can lead to a higher overshoot, while a larger R can reduce the overshoot, which is in accordance with the change in damping ratio. However, the comparison between group A and group D shows that larger capacitance gives rise to a larger overshoot even though the damping ratio of Function 2 is higher. This phenomenon is attributed to the decreasing of natural frequency ω_n with an increasing C shown in (6).

The natural frequency ω_n in Function 2 (expressed in (6)) corresponds to the resonant frequency of the circuit. As described in Section 3.2, the pulse voltage has a large content of high-frequency components, of which the highest frequency f_u is calculated approximately in (2). When a circuit is added with pulse voltage, these high frequency components can induce resonance on the output voltage, which is one of the important reasons why the overshoot exists. Considering the values of L and C and rise time t_r in this circumstance, ω_n is much larger (approximately 894 MHz) than f_u (approximately 15.9 MHz). So, if the C is kept constant, reducing the rise time can make the f_u higher and closer to ω_n. Consequently, stronger resonance is induced. Correspondingly, when keeping the rise time unchanged, a higher value of C reduces the ω_n and makes it closer to f_u. Both these two changes can make the overshoot of the output voltage higher. Keeping other parameters the same as that of Group A in Table 4, we repeat the simulation by increasing the capacitance C continuously, and the overshoot with the changing of C can be seen in Figure 9. The curve of the overshoot can be divided into two regions. In region 1, the decreasing of natural frequency ω_n with an increasing C plays the dominant role in the changing of the overshoot, leading to a stronger resonant oscillation. Meanwhile, the damping ratio ζ also keeps increasing, and its effect on suppressing the oscillation becomes stronger. So, when C reaches nearly 80,000 pF, the curve meets a saturation. In region 2, where C is higher than 80,000 pF, the increasing ζ due to increasing C plays the dominant role in changing the overshoot, leading to a weaker oscillation. In the practical situation of a transformer, the interturn capacitance can never be so large as to reach more than 80,000 pF. So, we can draw the conclusion that the interturn voltage overshoot is supposed to increase with the increase in interturn capacitance.
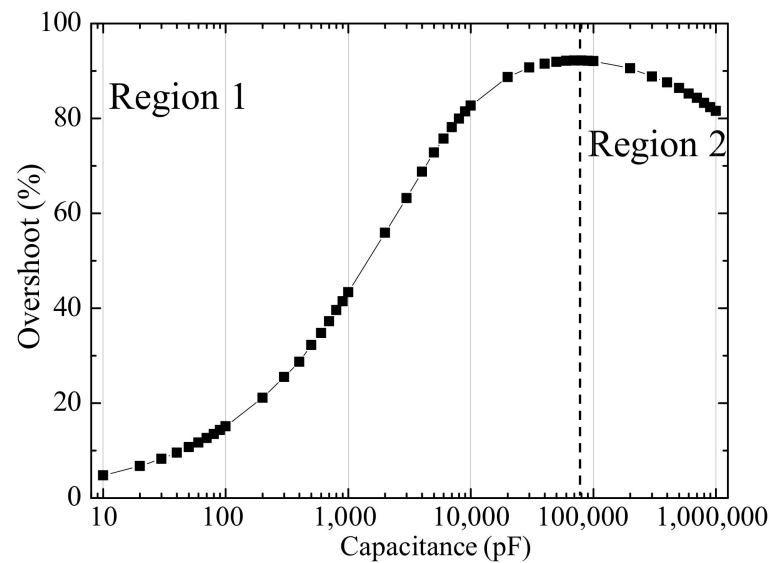
Figure 9. Overshoot with different capacitances.

For different values of *C*, the overshoot of the output voltage in Figure 7 (*n* = 1) under different rise times are shown in Figure 10 (*R* and *L* values are kept as the same as that in Group A of Table 4). We can see, with the decreasing rise time, overshoot increases at first and, then, converges to a stable value. The reason is that for a rise time short enough, the frequency of the high-order harmonics of the pulse voltage can cover the ω_n, which means the strongest resonance is already induced, and further reducing the rise time would not bring much difference. We take the value of the rise time as a critical value with which the overshoot ceases to increase obviously with further reduction in the rise time. We can see that a higher capacitance leads to a larger critical rise time. The reason is that a higher capacitance can reduce the resonant (natural) frequency ω_n expressed in (6). Then, f_u comes closer to ω_n if the rise time does not change, and strong resonance is more easily triggered. Correspondingly, if the rise time reduces (from 100 ns and follows the curve displayed in Figure 10), a relatively longer rise time can already make the frequency of high-order harmonics cover the ω_n to trigger the strongest resonance. This result confirms the explanation for the mechanism of how stray capacitance and rise time influence the overshoot on the voltage drop between different turns.
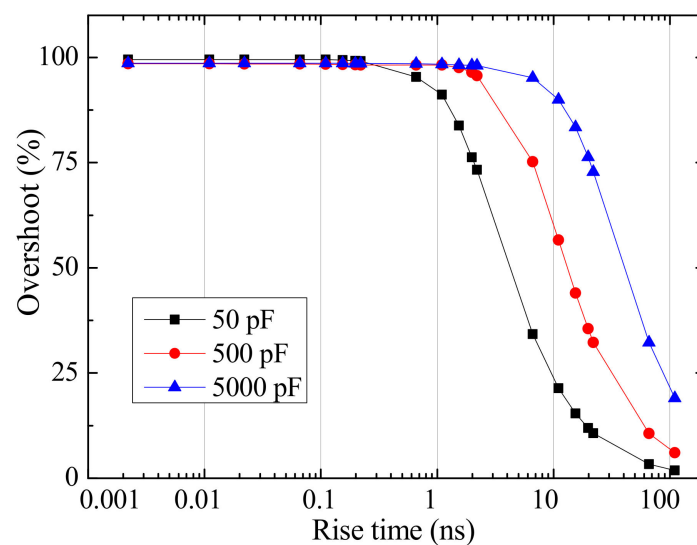

Figure 10. Overshoot under different rise times and capacitances.

The above analysis of the influence of stray capacitance and the pulse voltage rise time on the overvoltage is based on the most simplified one-layer two-turns model. Whether it is suitable for predicting the electrical stress in the complicated three-layer 120-turns model built for the selected practical transformer in Figure 5 needs verification. This will be discussed in the following section.

5. Parameters of the Simulation on the Complete Model

Among the aforementioned parameters in the last section, rise time can be variable in the practical working condition because of the variety of switching capability of semi-conductor switches. For the transformer's design, by keeping the overall dimension and the core of the prototype unchanged, the selection of different insulation materials can bring change to the stray capacitance. Besides, previous research focused on static voltage analysis shows that changing the winding structure can be a method to relieve the electrical stress of the transformer [9]. The influence of this method on the transient electrical stress suffered by transformers working under pulse voltage with short rise time is worth study. Therefore, to confirm the correctness of the analysis on the mechanism of the overvoltage in Section 4 and investigate the impact from the aforementioned factors on the electrical stress, further simulations on the complete circuit model of the selected transformer proto-type (seen in Figure 5) are necessary. This section would describe the parameters for the simulation in detail.

5.1. Rise Time

Power electronic switches are developing to be faster in switching in order to decrease the switching loss. In recent years, some SiC-based switches can even reach a switching time shorter than 100 ns, which would cause more serious electric stress on the insulation of the devices in medium-voltage and medium-frequency applications. To prove the effect of rise time on the electric stress suffered by the transformer's winding, four rise times from 100 ns to 1 μs are selected.

5.2. Insulation Relative Permittivity

Different insulation materials (include polyimide, polyester, Nomex paper, and DMD paper) are used for the insulation of the transformers according to their different working conditions [24]. Besides the difference in electrical strength of these materials, another variable property that can affect the insulation behavior among these materials is the relative permittivity. It is well known that relative permittivity ε_r is proportional to the value of capacitance. Therefore, for the transformer prototype in this case study, larger ε_r leads to larger interturn and interlayer capacitances. This can in turn increase the interturn overvoltage as analyzed in Section 4. To verify the quantitative effect of stray capacitance on the overvoltage and investigate the effect of different insulation materials on the MVMF transformer's electrical stress, simulations on the complete circuit model with different ε_r of insulation should be conducted. Among the materials usually used for transformer's insulation, ε_r of Nomex can be as low as 1.6, ε_r of DMD is usually lower than 3.0, while that of polyimide can be as high as 3.9 [24]. So, three different ε_r values, 3.9, 2.7, and 1.6, are selected to represent these aforementioned materials for the comparative simulation.

5.3. Winding Structure

C-type and Z-type winding structures can be seen in Figure 11 (numbers in the figure refer to the serial numbers of turns); these two structures are usually applied in the design of the transformer with multi-layer windings. According to the research in [9], comparing with the C-type winding, Z-type winding can reduce the largest interlayer voltage drop by 50%, although this winding type is slightly harder to construct. Suppose that in a two-layer winding, every layer of the winding has 2n turns; then, the interlayer voltage drop under different winding structures can be shown in Figure 12. Under C-type winding, the highest interlayer voltage drop is U, while under Z-type winding, the interlayer voltage drop is

constant as U/2. Yet, this conclusion is obtained from static voltage analysis, the influence of changing the winding structure on the transient electric stress brought from pulse-like voltage needs further investigation.
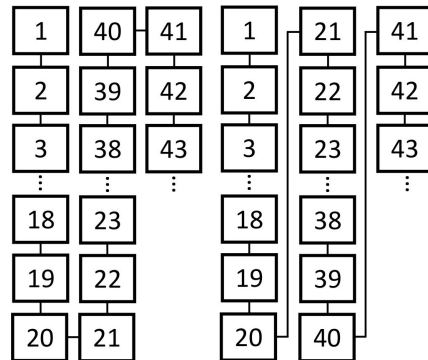

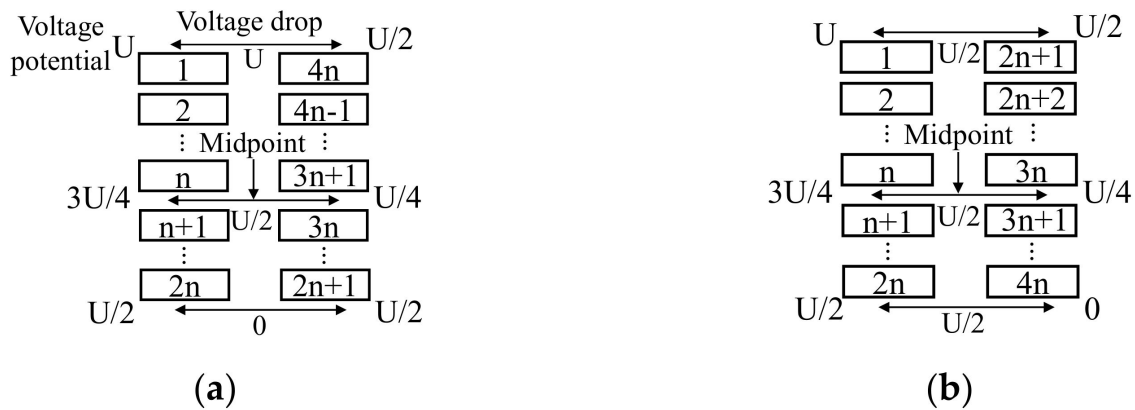**Figure 11.** C-type (**left**) and Z-type (**right**) winding layout.

Figure 12. Interlayer voltage drop: (**a**) C-type winding; (**b**) Z-type winding.

According to the description above, the detailed parameters including rise time t_r, relative insulation permittivity ε_r, and winding structure of the electrical stress simulation on the transformer's equivalent circuit model are shown in Table 5.

Table 5. Detailed parameters of the simulation on the complete model.

Group	t_r (ns)	ε_r	Winding Structure
1	100	3.9	C-type
2	200	3.9	C-type
3	500	3.9	C-type
4	1000	3.9	C-type
5	100	2.7	C-type
6	200	2.7	C-type
7	500	2.7	C-type
8	100	1.6	C-type
9	200	1.6	C-type
10	500	1.6	C-type
11	200	3.9	Z-type

6. Results of Simulation on the Complete Model

6.1. Interturn Voltage

During the simulation, within the first layer of the HV winding, voltage waveforms between the 1st and 2nd turns, 2nd and 3rd turns, 3rd and 4th turns, 4th and 5th turns, and 5th and 6th turns are recorded. Accordingly, interturn voltage drops within the first six turns in the second layer (from 21st to 26th turn) and the third layer (from 41st to 46th turn) are also recorded. All these interturn voltage drops are expressed as $V_{n-(n+1)}$. Take Group 1 in Table 5 as an example, peak voltage values between different adjacent turns during the rising flank of the voltage are shown in Figure 13. It can be seen that the voltage drop in different adjacent turns does not decrease monotonously, this phenomenon is different from that of the voltage drop simulation on motor winding, of which the peak voltage drop V_{peak} between the first two turns is usually the largest [14]. The reason is that the structures of the core and winding of the transformer are different from that of the HV form-winding motor presented in [14]. Especially, for the three-layer winding of the transformer prototype in this case study, interlayer capacitance and mutual inductance exist. Therefore, the inductive and capacitive coupling between turns in this transformer is quite different from that of a motor and more complicated. These factors lead to a different voltage distribution. Yet, the peak values of different interturn voltage drops can still be much higher than the static voltage values, which can also be a threat to the transformer's insulation. To describe the overvoltage, the ratio between peak voltage drop value and the static voltage drop value $R_{ov} = V_{peak}/V_{static}$ is applied. The value of R_{ov} under different rise times and relative permittivity are shown in Figures 14 and 15, respectively. From the results, we can see clearly that overvoltage would increase with the decreasing rise time. While with the lower relative permittivity (leads to lower interturn capacitance), the overvoltage would be lower. These results are in accordance with that of the simulation on the simplified model proposed in Section 4. Detailed similarities between simulation results in this section and Section 4 are listed in Table 6. These results are also similar with the experiments reported in [25], which show that voltage drop across each turn increases when the square wave voltage has a shorter rise time, and the voltage value does not decrease monotonously from the first turn to the last turn. So, the correctness of the overvoltage mechanism analysis in Section 4 and the proposed circuit model in Figure 5 are validated.
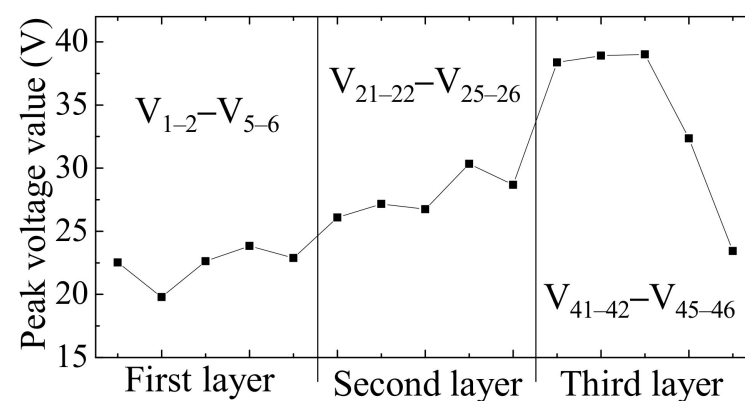

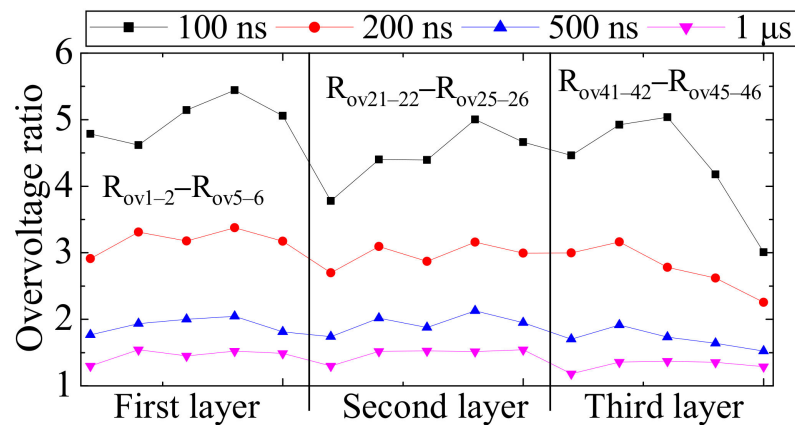**Figure 13.** Overvoltage ratio between adjacent turns in different layers.

Figure 14. Interturn overvoltage ratio between adjacent turns under different rise times ($\varepsilon_r = 3.9$, C-type).
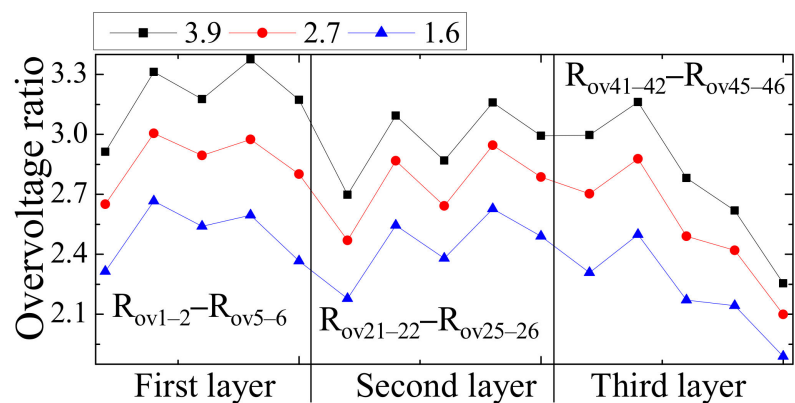

Figure 15. Interturn overvoltage ratio between adjacent turns under different relative permittivity ($t_r = 200$ ns, C-type).

Table 6. Similarities between simulation results in simplified model and complete model.

Simulation Results	Simplified Model	Complete Model
Overshoot on voltage rising edge exists?	Yes	Yes
Peak voltage value with shorter rise time	Higher	Higher
Peak voltage value with larger stray capacitance	Higher	Higher

To investigate the comprehensive effect of relative permittivity and rise time, the interturn overvoltage ratio of the first layer (from 1st to 6th turns) under different rise times and relative permittivity is plotted in Figure 16. The results show that, under shorter rise time, the reduction in ε_r can cause greater decreasing of R_{ov}. Take the interturn voltage between the 1st and 2nd turns as an example, when ε_r changes from 3.9 to 1.6, the R drops by 27.08%, while for the same situation under 500 ns rise time, R_{ov} drops by only 16.07%. Interturn overvoltage ratio under different winding types is shown in Figure 17. Changing the winding structure from C-type to Z-type cannot only reduce the maximum static interlayer voltage drop as seen in Figure 12 but can also reduce the transient interturn overvoltage.
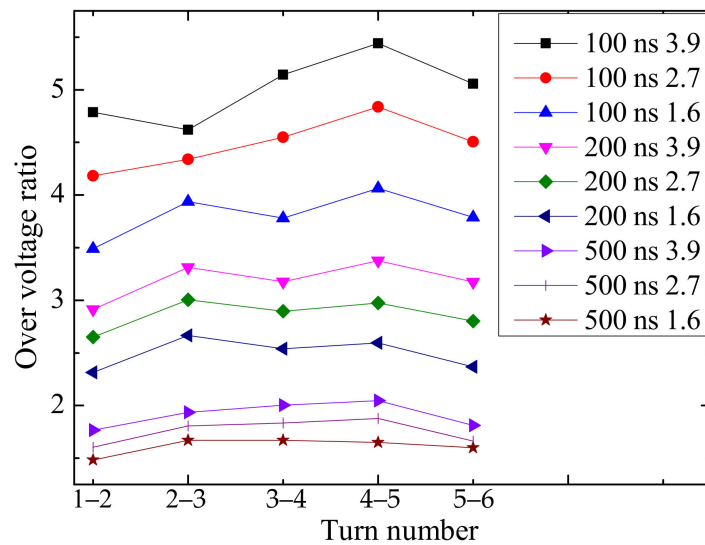
Figure 16. Interturn overvoltage ratio under different rise times and relative permittivity.
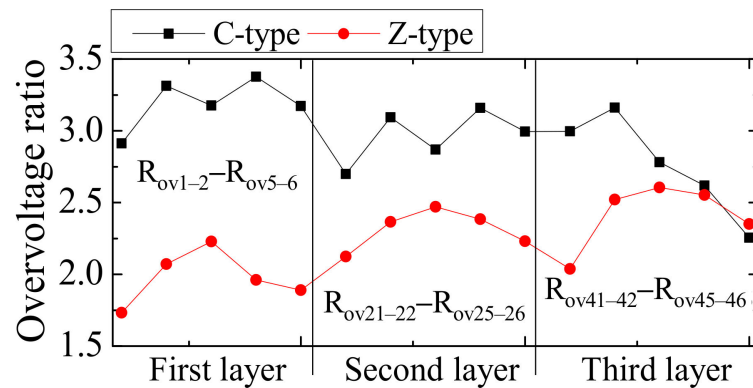

Figure 17. Interturn overvoltage ratio under different winding structures (tr = 200 ns, εr = 3.9).

6.2. Interlayer Voltage

As mentioned in the introduction, for transformers with multilayer windings, inter-layer insulation may also suffer from the electrical stress brought from the fast wave front of power electronic switches, so the simulation on interlayer voltage is also needed. For the measurement of interlayer voltage drop, six test points are applied and seen in Figure 18. V1–V3 are used for detection of the voltage drop between layer 1 and layer 2, V3–V6 are used for that between layer 2 and layer 3. Typical waveforms of the interlayer voltage drops (Group 1 in Table 5) are seen in Figure 19. Unlike the adjacent interturn voltage, of which the static values are almost the same (seen in Figure 6 with time range >1.03 ms), the static voltage drop in different interlayer voltage test points is of a great difference; this is normal for transformer with a multi-layer C-type winding [9]. So, although overvoltage ratio of V2 in Figure 19 maybe higher than that of V1, the transient peak voltage of V1 is still obviously higher than that of V2. Under this circumstance, the overvoltage ratio R_{ov} is not suitable for the comparison of overvoltage in difference test points under different parameters. So, we use the peak voltage value instead, since it displays transient maximum potential difference between adjacent layers, which reflects the interlayer electrical stress. The peak interlayer voltage values under different rise times and relative permittivity are shown in Figures 20 and 21, respectively. The numbers 1–3 and 4–6 refer to the voltage test points V1–V3 (between 1st layer and 2nd layer) and V4–V6 (between 2nd layer and 3rd layer), respectively. Similar to the results from interturn voltage simulation, the interlayer peak voltage is higher under a shorter rise time. When the rise time is 100 ns, the highest peak value in test point V6 can reach more than 450 V, exceeding its static voltage drop by more

than 190 V. In a practical situation, the insulation condition of the transformer is usually not as good as what we assumed in Section 2; small air ducts may be left unintentionally in the insulation between adjacent turns and layers. If that happens, the ionization strength of the air duct may be exceeded. Then, partial discharge (mainly in the form of corona discharge) may be triggered with high probability. Decreasing the relative permittivity can also slightly reduce the peak interlayer voltage.
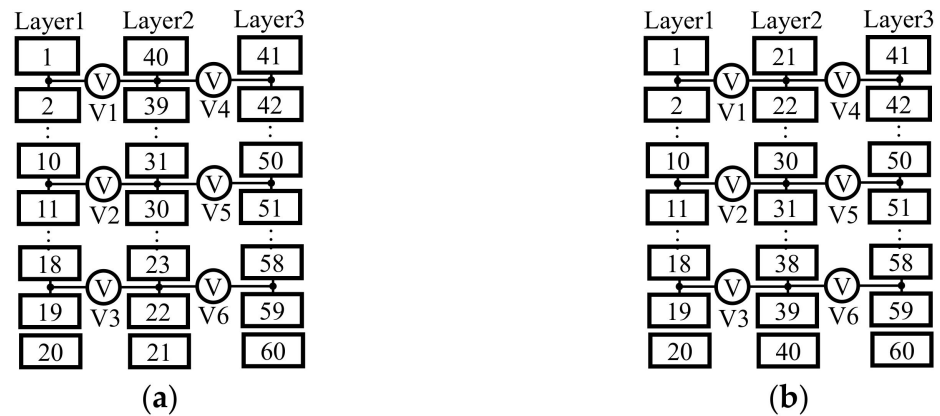

Figure 18. Testing points of the interlayer voltage drop in different winding structures: (**a**) C-type; (**b**) Z-type.
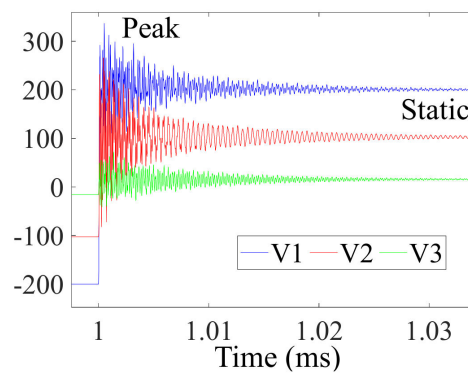

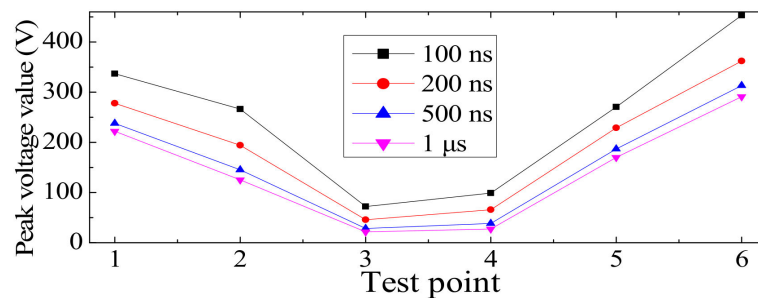**Figure 19.** Typical waveform of layer1-to-layer2 voltage drop (C-type).

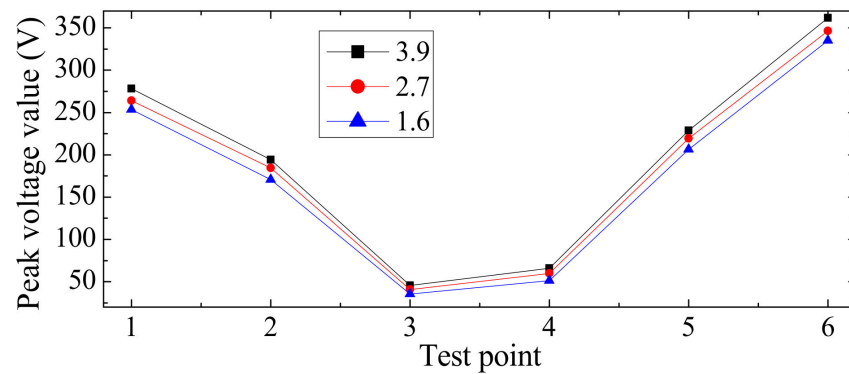**Figure 20.** Peak interlayer voltage under different rise times (εr = 3.9, C-type).

Figure 21. Peak interlayer voltage under different relative permittivity (tr = 200 ns, C-type).

The results of comparative interlayer voltage simulation under different winding structures are shown in Figure 22. In most of the test points, the peak voltage drops in Z-type winding are very different from C-type winding. The reason can be found in Figure 18. For C-type winding, taking the region between Layer 1 and Layer 2 as an example, we can see that in the top area where lies V1, the interlayer voltage drop equals the voltage difference between the 1st turn and the 40th turn. In the downward area, such as the positions of V2 or V3, the turns between the two sides are relatively much closer with respect to electrical connect (V2 between 10th and 31st turns, V3 between 18th and 23rd turns). This is the main reason why the voltage drop value in V1 is much higher than that of V2 and V3. A similar situation can be found in the region between Layer 2 and Layer 3. While in Z-type winding, for different areas in the region between adjacent layers, the distances with respect to electrical connection between turns on the two sides are the same (V1 between 1st and 21st turns, V2 between 10th and 30th turns, V3 between 18th and 38th turns). So, the interlayer voltage values in Z-type winding changes only slightly among different test points. Because of this even distribution of interlayer voltage, the largest peak interlayer voltage value of Z-type winding is only half of C-type winding.
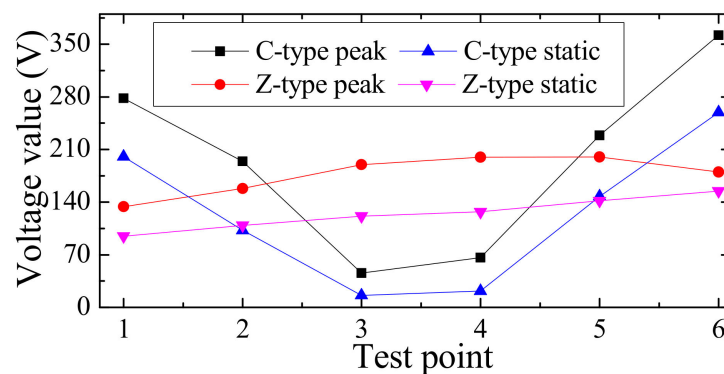

Figure 22. Peak and static interlayer voltage under different winding structures (tr = 200 ns, εr = 3.9).

To display the difference between transient interlayer voltage simulation and static interlayer voltage analysis presented in the previous study [9], we added values of static voltage drop under different winding structures in Figure 22. Although the overall trending of static voltage value vs. time is similar to that of peak voltage value, an obvious difference can be found in test points V2 and V5, which are midpoints between adjacent layers similar to the midpoints displayed in Figure 12. In these two points, static voltage drops under different winding structures are almost the same. However, the results of peak voltage values show that with the existence of voltage overshoot caused by pulse voltage, peak voltage values in V2 and V5 under Z-type winding are lower than that of C-type winding.

It is clear that for transformers working in MVMF applications, using Z-type winding can also effectively relieve its electrical stress. So, in the design of the MVMF transformer, it is suggested to apply this kind of winding structure.

7. Conclusions

Working under PWM voltage with very short rise time, an MVMF transformer may be faced with the problem of overvoltage in the winding, which can be a threat to the transformer's insulation reliability. Therefore, it is necessary to investigate the detailed situation of the electrical stress in the winding of MVMF transformer. This would be beneficial to the study of the MVMF transformer's insulation aging and failure mechanism and finding suitable strategies to reduce the electrical stress. Focusing on the study of electrical stress, the work done by this paper and the conclusions can be summarized as follows:

1. Based on the FEM calculation, an equivalent circuit model of a 1.5 kV, 1 kHz transformer's HV winding is built. Simulations and mechanism analysis verify the correctness of this model and its ability to obtain the transient electrical stress in the winding of MVMF transformer quantitatively.
2. Transient interturn/layer voltage simulation on the model shows the characteristics of transient voltage overshoot in the winding fed by pulse voltage that cannot be observed by steady-state voltage/electric field analysis. The results also indicate that pulse voltage with shorter rise time can induce higher interturn and interlayer overvoltage. Based on that, guidelines about choosing appropriate voltage waveform for aging and endurance lifetime studies on the MVMF transformer insulation can be given. This would help researchers build a life-time model of the insulation with more accuracy.
3. Electrical stress of the MVMF transformer's winding with different design parameters (in this paper, mainly different insulation materials and winding structures) can be obtained through this model. Simulation results show that using insulation material with lower relative permittivity and changing the winding structure from C-type to Z-type can reduce the interturn and interlayer overvoltage. Based on that, we propose limiting the voltage overshoot and, thereafter, enhancing the MVMF transformer's insulation capability in its design phase, which throws light on the MVMF transformer's insulation design.

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Informed Consent Statement: This study did not involve humans.

Data Availability Statement: Data supporting reported results in this paper can be obtained through contacting the 1st and corresponding authors.

Conflicts of Interest: We declare that this research has no conflict of interest.

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