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Rethinking Current Controller Design for PLL-Synchronized VSCs in Weak Grids

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***Abstract*—This article revisits the design of the current controller for grid-connected voltage-source converters (VSCs), considering the dynamic impacts of the phase-locked loop (PLL), weak grids, and of voltage feedforward (VFF) control. First, a single-input single-output transfer-function-based model is proposed to characterize the interactions of control loops. It is analytically found that the proportional gain of the current controller essentially aggravates the instability effect of PLL in weak grids, while the cutoff frequency of the low-pass filter used with the VFF loop has a nonmonotonic relationship with the PLL-induced instability. Then, based on these findings, a guideline for redesigning the current controller of PLL-synchronized VSCs is developed, which enables a codesign of the current controller and VFF controller. Finally, simulation and experimental results confirm the validity of theoretical analyses.**

***Index Terms*—Current controller, phase-locked loop, voltage feedforward control, voltage-source converters, weak grids.**

I. Introduction

THE small-signal synchronization instability may arise when the phase-locked loop (PLL) is adopted to synchronize voltage-source converters (VSCs) with weak grids [1]. Many research works have, thus, been made on the modeling and analysis of the PLL-induced synchronization instability of VSCs [2]–[9]. It is first reported in [2] that the PLL adds a negative resistance at the VSC output, which can destabilize VSC-grid interactions. Further studies are reported in [3] and [4], which reveal that the frequency region of this negative resistance is widened with the increase of PLL bandwidth [3], and the instability is more prone to arise with a lower short-circuit ratio (SCR) of the grid [4]. A quantitative relationship between the proportional gain of PLL and the SCR is plotted based on the eigenvalue analysis [4]. The impacts of reactive power control loops on the synchronization instability of PLL-based VSCs are further discussed in [5]. Yet, the influences of current controller parameters on such PLL-induced instability are overlooked in [2]–[5].

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The impacts of different reference-frame current controllers on the PLL-induced synchronization stability are compared in [6]. It is revealed that the proportional + resonant (PR) current controller in the stationary frame is more robust against the dynamic impact of PLL than the *dq*-frame P + integral (PI) controller, provided that the centre frequency of R controller is not locked with the measured frequency of PLL. However, how different P controller gains affect the synchronization stability is not discussed in [6]. Recently, it is reported in [7] that the increase of P gain of the current controller can reduce the frequency region of negative resistance added by the PLL, and hence, the synchronization stability in weak grids can be enhanced. It is further shown in [8] that the allowed maximum PLL bandwidth to maintain the synchronization stability of VSCs is increased nonlinearly with the increase of P gain of the current controller. Nevertheless, this nonlinear relationship between the PLL and the current controller is merely obtained by numerical analysis with different SCRs of the grid. The interaction between the PLL and the current controller still lacks a clear analytical insight.

Numerous researches on the design of the current controller for PLL-based VSCs can be found in the literature [10]–[14]. Yet, most of them are focused on the current control loop itself [10]–[12], and its dynamic interaction with the *LCL*-filter resonance in the high-frequency range [13]–[15]. Only a few recent works consider the interaction effect of PLL in the design of the current controller [7]–[9]. In addition, the voltage feedforward (VFF) control can also interact with the PLL dynamic in the timescale of current control [9]. The impact of the VFF loop using a low-pass filter (LPF) on the PLL-induced synchronization stability of VSCs is discussed in [5]. Yet, how different cutoff frequencies of LPF affect the synchronization stability still remains an open issue.

This article, therefore, attempts to fill the gap by revisiting the design of the current controller with the consideration of the parametric effects of VFF control and of PLL in weak grids. First, a single-input single-output (SISO) transfer-function-based model is proposed to characterize the interaction between PLL and the current controller. Differing from the conclusions of [7] and [8], the proposed model analytically reveals that the finite P gain of the current controller, in essential, aggravates the instability effect of PLL, i.e., the maximum PLL bandwidth that is allowed in weak grids is reached when the current control loop is idealized with unity closed-loop gain. The use of a linear PI/PR controller with a finite gain reduces the allowed maximum PLL bandwidth, and increasing the P gain of the current controller can only mitigate such bandwidth reduction. Furthermore, based on

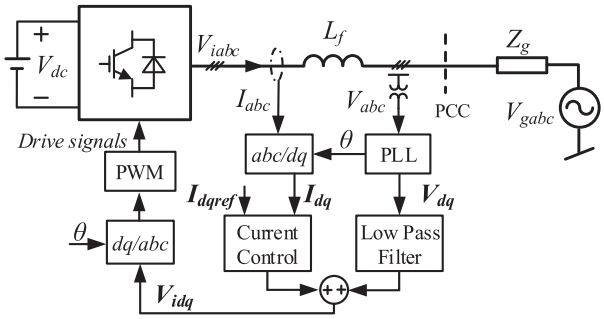

Fig. 1. Simplified one-line diagram of a three-phase grid-connected VSC.

the SISO transfer function model, a nonmonotonic relationship between the cutoff frequency of the LPF used with the VFF control and the synchronization stability is identified.

Then, based on the above findings, a guideline to redesign the current controller is developed for PLL-synchronized VSCs in weak grids. For the P gain of the current controller, a lower limit is identified to prevent the PLL-induced instability, in addition to the upper limit for avoiding high-frequency oscillations [15]. Furthermore, the developed guideline enables a codesign of current control and VFF control, given that the PLL bandwidth is lower than its allowed maximum value under a certain SCR. Finally, the correctness of theoretical analyses is validated through the simulation and experiment results.

II. Small-Signal Modeling of Three-Phase VSCs

A. System Description

Fig. 1 illustrates a simplified one-line diagram of a three-phase grid-connected VSC, where L_f is the filter inductor and Z_g denotes the grid impedance, which is generally inductive [5]. The pure inductor L_g is, thus, used to represent the grid impedance [6] in this article. To emulate the weak grid with a low short-circuit ratio (SCR), the grid inductance is chosen as 13 mH for an SCR of 2.4. I_{abc} and V_{abc} are three-phase inductor currents and three-phase voltages at the Point of Common Coupling (PCC), respectively. V_{iabc} and V_{gabc} represent the converter output voltage and grid voltage. A constant dc-link voltage $V_{\rm dc}$ is assumed. To focus on the impact of the current controller on the synchronization stability, only the current controller, the PLL and VFF control loop are considered. Furthermore, the *dq*-axis current decoupling control is employed, which helps mitigate the cross-coupling impact of the filter. The VSC is synchronized with the grid through PLL, where θ denotes the synchronization phase angle. The current controller is realized with the PI controller in the *dq*-frame. The *dq*-axis voltage is feedforward to the current controller output through a LPF. Table I provides the main circuit and controller parameters used in this article.

B. Small-Signal Modeling of VSC in the DQ-Frame

Fig. 2 depicts the block diagram of the small-signal model of VSC with only the current controller. Since the *dq*-axis current decoupling control is adopted, the cross-coupling impact of the filter can be mitigated [16]. Thus, the admittance model of the *L*-filter plant in the *dq*-frame is written as

$$\mathbf{Y_p} = \begin{bmatrix} sL_f & 0 \\ 0 & sL_f \end{bmatrix}^{-1}. \tag{1}$$

By applying KVL across the filter admittance, the converter output current in the *dq*-frame can be derived as

$$\mathbf{I}_{dq} = \mathbf{Y}_p(\mathbf{V}_{idq} - \mathbf{V}_{dq}) \tag{2}$$

where $\boldsymbol{V}_{dq} = [V_d, V_q]^{\rm T}$ is the PCC voltage in the *dq*-frame and $\boldsymbol{V}_{idq} = [V_{id}, V_{iq}]^{\rm T}$ represents the converter output voltage in the *dq*-frame; $I_{dq} = [I_d, I_q]^{\rm T}$ denotes the *dq*-axis current.

Without the consideration of the VFF control loop, the current controller output is used as the reference voltage for the PWM generation. The converter output voltage can be represented as

$$\mathbf{V}_{idq} = \mathbf{G}_d\mathbf{G}_i(\mathbf{I}_{dqref} - \mathbf{I}_{dq}). \tag{3}$$

$\boldsymbol{G}_i$ is the PI controller, which is given by vvv

$$\mathbf{G_i} = \begin{bmatrix} K_p + K_i/s & 0 \\ 0 & K_p + K_i/s \end{bmatrix} \tag{4}$$

where K_p and K_i mean the proportional gain and integral gain of the PI controller, respectively.

$\boldsymbol{G}_d$ is the time delay of the digital control system, which consists of one sampling period (T_s) of the computation delay

TABLE I
Parameters of Three-Phase VSC

Symbol	Description	Value (p.u.)
ω_1	Grid frequency	50 Hz (1)
f_s	Sampling frequency	10 kHz (200)
V_{d0}	*d*-axis voltage steady values	220 V (1.41)
V_{q0}	*q*-axis voltage steady values	0 V (0)
I_{d0}	*d*-axis current steady values	15 A (0.936)
I_{q0}	*q*-axis current steady values	0 A (0)
f_{sw}	Switching frequency	10 kHz (200)
V_{dc0}	DC-link voltage	730 V (4.7)
L_f	Filtered inductor	3 *m*H (0.097)
L_g	Grid inductor	13 *m*H (0.42)
K_p/K_i	Current inner controller	15.7 Ω / 0 Ω/s
K_{ppll}/K_{ipll}	PI controller of PLL	3.5 rad/s / 957 rad/s^2
α_f	Cutoff frequency of LPF	100 rad/s

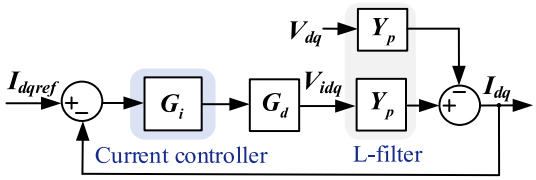

Fig. 2. Block diagram of the small-signal model of VSC with only the current controller.

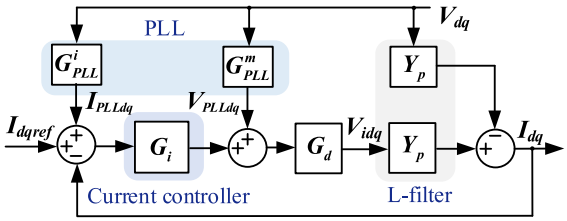

Fig. 3. Block diagram of transfer matrices for the small-signal model of VSC with PLL effects.

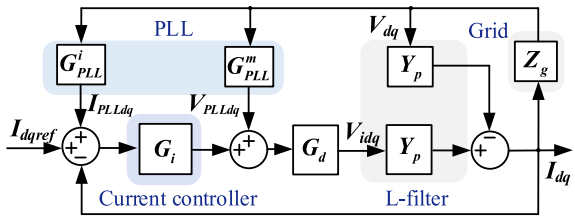

Fig. 4. Block diagram of the small-signal model of VSC connected with the grid.

and half-sampling period ($0.5T_s$) delay of the PWM [17]

$$\mathbf{G}_d = \begin{bmatrix} e^{-1.5T_s s} & 0 \\ 0 & e^{-1.5T_s s} \end{bmatrix}. \tag{5}$$

The closed-loop response of the current control loop can be derived base on (1)–(5), which is given as

$$\begin{aligned} \mathbf{I}_{dq} = {} & [\mathbf{I} + \mathbf{Y}_p \mathbf{G}_d \mathbf{G}_i]^{-1} \mathbf{Y}_p \mathbf{G}_d \mathbf{G}_i \mathbf{I}_{dqref} \\ & - [\mathbf{I} + \mathbf{Y}_p \mathbf{G}_d \mathbf{G}_i]^{-1} \mathbf{Y}_p \mathbf{V}_{dq} \end{aligned} \tag{6}$$

where $\boldsymbol{I}$ is the unitary diagonal matrix.

Fig. 3 illustrates the block diagram of transfer matrixes for the small-signal model of VSC when PLL effects are considered. The SRF-PLL is used in this article to synchronize the VSC with the grid, where the Park-transformation is utilized to detect the PCC voltage phase, and the q-axis voltage is regulated by a PI controller for the phase tracking. The closed-loop transfer function of PLL can be derived as [3]

$$H_{pll} = \frac{K_{ppll} s + K_{ipll}}{s^2 + V_{d0} K_{ppll} s + V_{d0} K_{ipll}} \tag{7}$$

where K_{ppll} and K_{ipll} represent the proportional gain and integral gain of the PI controller in the PLL, respectively.

The effects of PLL on currents and modulated voltages are modeled by two asymmetric transfer matrices, which are given by [6]

$$\mathbf{V}_{\mathrm{PLL}dq} = \begin{bmatrix} V_{\mathrm{PLL}d} \\ V_{\mathrm{PLL}q} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & -V_{iq0} H_{pll} \\ 0 & V_{id0} H_{pll} \end{bmatrix}}_{\mathbf{G}^m_{\mathbf{PLL}}} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \tag{8}$$

$$\mathbf{I}_{\mathrm{PLL}dq} = \begin{bmatrix} I_{\mathrm{PLL}d} \\ I_{\mathrm{PLL}q} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & -I_{q0} H_{pll} \\ 0 & I_{d0} H_{pll} \end{bmatrix}}_{\mathbf{G}^{\mathrm{i}}_{\mathrm{PLL}}} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \tag{9}$$

where V_{idq0} and I_{dq0} are, respectively, the steady-state modulated voltage and VSC current. Due to the PLL effects, (3) is reformulated as

$$\begin{aligned} \mathbf{V}_{idq} &= \mathbf{G}_d[\mathbf{G}_i(\mathbf{I}_{dqref} - \mathbf{I}_{dq} + \mathbf{I}_{\mathrm{PLL}dq}) + \mathbf{V}_{\mathrm{PLL}dq}] \\ &= \mathbf{G}_d[\mathbf{G}_i(\mathbf{I}_{dqref} - \mathbf{I}_{dq} + \mathbf{G}^i_{\mathrm{PLL}} \mathbf{V}_{dq}) + \mathbf{G}^m_{\mathrm{PLL}} \mathbf{V}_{dq}]. \end{aligned} \tag{10}$$

With the consideration of PLL effects, the closed-loop response can be written as

$$\begin{aligned} \mathbf{I}_{dq} = {} & [\mathbf{I} + \mathbf{Y}_p \mathbf{G}_d \mathbf{G}_i]^{-1} \mathbf{Y}_p \mathbf{G}_d \mathbf{G}_i \mathbf{I}_{dqref} \\ & - [\mathbf{I} + \mathbf{Y}_p \mathbf{G}_d \mathbf{G}_i]^{-1} \mathbf{Y}_p (\mathbf{I} - \mathbf{G}_d \mathbf{G}^m_{\mathrm{PLL}} - \mathbf{G}_d \mathbf{G}_i \mathbf{G}^i_{\mathrm{PLL}}) \mathbf{V}_{dq}. \end{aligned} \tag{11}$$

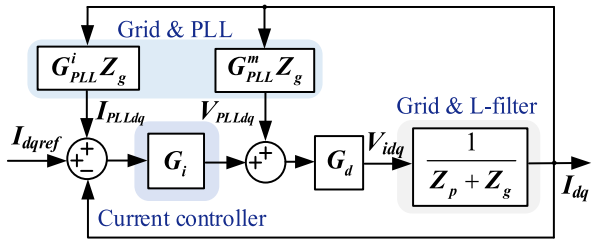

Fig. 5. Equivalent block diagram of VSC connected with the grid.

III. Impact Analysis of Current Controller on Synchronization Stability

A. Equivalent Model of Grid-Connected VSC for Interaction Analysis

To analyze the impact of the current controller on the synchronization dynamics caused by the PLL and weak grid, the small-signal model that incorporates the effect of the grid impedance is developed for VSC [16]. The grid impedance is expressed as

$$\mathbf{Z_g} = \begin{bmatrix} sL_g & -\omega_1 L_g \\ \omega_1 L_g & sL_g \end{bmatrix}. \tag{12}$$

By applying KVL across the grid impedance, the relationship between the grid voltage and PCC voltage can be expressed as

$$\mathbf{V}_{gdq0} + \mathbf{Z_g} \mathbf{I}_{dq0} = \mathbf{V}_{dq0}. \tag{13}$$

By adding the small perturbation to (13) and cancelling the steady-state values, the linearized expression can be obtained. Since the grid voltage V_{gdq0} is stiff, its perturbation term V_{gdq} is equal to zero. Thus, the perturbation term of PCC voltage $\boldsymbol{V}_{dq}$ can be represented by the product of grid impedance and perturbation current $\boldsymbol{I}_{dq}$. Consequently, the equivalent block diagram of the small-signal model of grid-connected VSC is derived by integrating the grid impedance, as shown in Fig. 4.

To analyze the dynamic interaction between the PLL and grid impedance, the transfer matrix of the grid impedance is first embedded into the transfer matrices $\boldsymbol{G}^i{}_{\mathrm{PLL}}$ and $\boldsymbol{G}^m{}_{\mathrm{PLL}}$ that represent the PLL effects. Fig. 5 illustrates the equivalent block diagram of VSC connected with the weak grid.

In order to investigate the impact of the current controller on PLL-induced synchronization stability, the transfer matrix of the current controller is further combined with the transfer matrices of grid impedance and of PLL effects $\boldsymbol{G}^m{}_{\mathrm{PLL}}$. The interaction matrix $\boldsymbol{G}$ is, thus, formulated to analyze the dynamic interaction among the current controller, PLL, and grid impedance, as shown in Fig. 6.

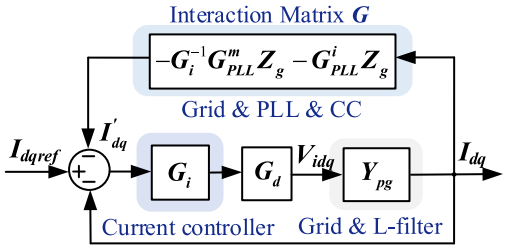

Fig. 6. Equivalent block diagram of the interaction matrix.

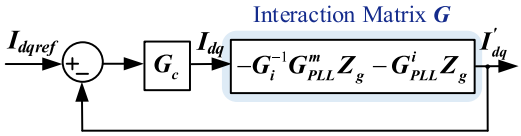

Fig. 7. Simplified block diagram of VSC connected with the grid.

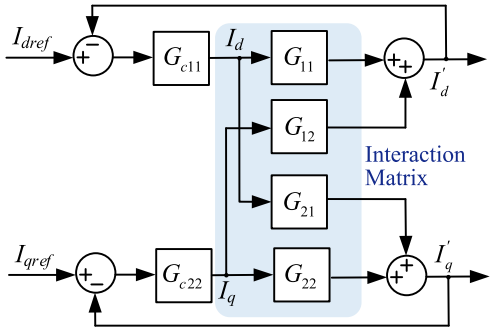

Fig. 8. Equivalent MIMO block diagram of VSC connected with the grid.

To simplify the interaction analysis, the transfer function matrix $\boldsymbol{G}_c$ can be used to represent the closed-loop current controller, as shown in Fig. 7, which is expressed as

$$\mathbf{G}_c = [\mathbf{I} + \mathbf{Y}_{pg}\mathbf{G}_i\mathbf{G}_d]^{-1}\mathbf{Y}_{pg}\mathbf{G}_i\mathbf{G}_d. \tag{14}$$

Since the current controller matrix $\boldsymbol{G}_i$ and time delay matrix $\boldsymbol{G}_d$ are diagonal, the transfer function matrix of the closed-loop current controller is assumed as a diagonal matrix, where the off-diagonal elements are equal to zero.

Fig. 8 gives the detailed multi-input multi-output (MIMO) block diagram of grid-connected VSC used for the interaction analysis, where G_{c11}, G_{c22} and G_{c12}, G_{c21} are the diagonal and off-diagonal entries of the symmetric transfer matrix $\boldsymbol{G}_c$, respectively, and G_{11}, G_{12}, G_{21}, G_{22} represent the elements of the interaction matrix. Since the current reference is constant during operation, the perturbation term on the q-axis is assumed as zero when doing the small-signal modeling on the d-axis. Therefore, based on Fig. 8, two SISO models can be obtained as

$$\frac{I'_d}{I_{dref}} = \frac{G_{c11}G_{11} + G_{c11}G_{c22}\left[G_{11}G_{22} - G_{12}G_{21}\right]}{CE} \tag{15}$$

$$\frac{I'_q}{I_{qref}} = \frac{G_{c22}G_{22} + G_{c11}G_{c2}\left[G_{11}G_{22} - G_{12}G_{21}\right]}{CE} \tag{16}$$

where the denominators of the two transfer functions, namely the characteristic expression are the same, which can be expressed as

$$\begin{aligned} CE &= 1 + G_{c11}G_{11} + G_{c22}G_{22} + \det(\mathbf{G}_c)\cdot\det(\mathbf{G}) \\ &= 1 + G_{c11}G_{11} + G_{c22}G_{22} + \det(\mathbf{G}_c)\cdot\det(\mathbf{G}). \end{aligned} \tag{17}$$

If the transfer function matrix of (14) is not diagonal, the extra terms of $G_{c12}G_{21} + G_{c21}G_{12}$ would be further introduced in (17). However, the analysis method is still applicable. Based on Fig. 6, the interaction matrix $\boldsymbol{G}$ can be written as

$$\boldsymbol{G} = -(\boldsymbol{G}_i^{-1}\boldsymbol{G}_{\mathbf{PLL}}^m + \boldsymbol{G}_{\mathbf{PLL}}^i)\boldsymbol{Z}_g. \tag{18}$$

It is noted that the matrices related to PLL effects have the characteristic that the first column elements of the matrix are equal to 0, as can be found in (8) and (9). Consequently, the first column elements of the combined matrix of ($\boldsymbol{G}_i^{-1}\boldsymbol{G}^m{}_{\mathrm{PLL}}+\boldsymbol{G}^i{}_{\mathrm{PLL}}$) is also equal to 0. Thus, based on the principle of the matrix determinant calculation, the determinant of matrix ($\boldsymbol{G}_i^{-1}\boldsymbol{G}^m{}_{\mathrm{PLL}}+\boldsymbol{G}^i{}_{\mathrm{PLL}}$) is always equal to zero, i.e., *det* ($\boldsymbol{G}_i^{-1}\boldsymbol{G}^m{}_{\mathrm{PLL}}+\boldsymbol{G}^i{}_{\mathrm{PLL}}$) = 0, and the determinant of $\boldsymbol{G}$, i.e., *det*($\boldsymbol{G}$) = –*det* ($\boldsymbol{G}_i^{-1}\boldsymbol{G}^m{}_{\mathrm{PLL}}+\boldsymbol{G}^i{}_{\mathrm{PLL}}$)×*det*($\boldsymbol{Z}_g$) is, thus, equal to zero. Therefore, (17) can be simplified as

$$\begin{aligned} CE &= 1 + G_{c11}G_{11} + G_{c22}G_{22} \\ &= 1 + \underbrace{G_{c11}L_gH_{pll}\left(\omega_1 I_{q0} - sI_{d0} - \frac{sV_{id0}}{G_i}\right)}_{T}. \end{aligned} \tag{19}$$

Since the converter itself will be stable, there will not exist poles in the transfer functions at the numerators of (15) and (16). Thus, based on the analysis of the open-loop transfer function T, the impact of the current controller on the synchronization stability can be revealed. It can be found that the transfer function of the current controller is cascaded with the transfer functions of grid impedance and PLL. Moreover, the transfer functions of the current controller, grid impedance, and PLL appear only once in the open-loop transfer function of the system. Therefore, it is easily understandable how they interact with each other and eventually results in grid synchronization instability.

B. Impacts of Current Controller on the Synchronization Dynamics

To simplify the impact analysis of the current controller, it is assumed that $I_{q0} = 0$ (unit power factor). The open-loop transfer function is further reformulated as

$$\mathrm{T} = -G_{c11}\left[H_{pll}sL_g\underbrace{\left(I_{d0} + \frac{V_{id0}}{G_i}\right)}_{I_{d0}^e}\right] = -G_{c11}(H_{pll}sL_gI_{d0}^e) \tag{20}$$

where I_{d0}^e denotes the equivalently injected d-axis current. The integral gain of the current controller K_i can be designed based on the guideline introduced in [2]. Furthermore, when the VFF control is used, even a smaller integral gain of the current

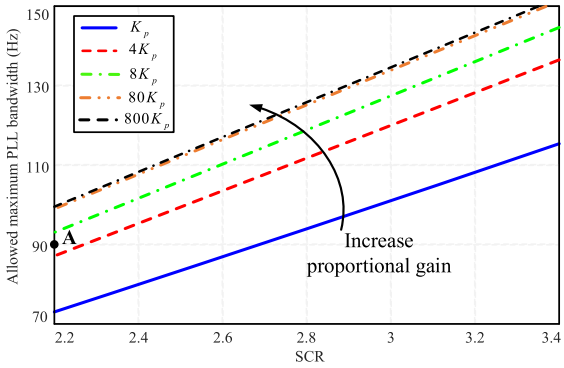

Fig. 9. Allowed maximum PLL bandwidth with different P gains of the current controller.

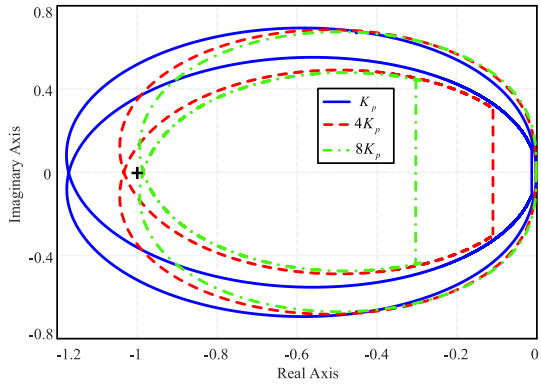

Fig. 10. Nyquist plot of open-loop gain under different P gains of the current controller.

controller is recommended to avoid any adverse interaction with the voltage-feedforward controller [2]. Hence, in this article, the integral gain K_i is chosen as the product of α_c (closed-loop bandwidth of the control system) and the filter resistance, which leads to a sufficiently small value (close to zero). Therefore, the current controller G_i is assumed as the P controller for simplicity, where K means the proportional gain of the current controller. Thus, the injected d-axis current of the VSC can be equivalent as

$$I_{d0}^{e} = I_{d0} + \frac{V_{id0}}{K}. \tag{21}$$

It is noted that the current controller can be considered as a resistor whose terminal voltage is equal to V_{id0}. Based on (21), the current flowing through the resistor is paralleled with the actual d-axis current I_{d0}. When the proportional gain of the current controller changes, i.e., the change of the resistor, the current flowing through the resistor is changed. The equivalently injected current is correspondingly changed, which further affects the synchronization dynamics. Therefore, the impact of the current controller parameter (K) on the synchronization stability can be interpreted as the change of the equivalently injected d-axis current that determines the equivalent SCR of the system. When $K \to +\infty$ the term of V_{id0}/K is close to zero, which means the current controller can be considered as the unit gain and does not affect the synchronization dynamics. In this manner, the maximum PLL bandwidth that is allowed in weak grids is reached. However, when the proportional gain of K decreases, the equivalently injected d-axis current increases, which means the equivalent SCR decreases and the allowed maximum PLL bandwidth is reduced correspondingly. This might result in grid synchronization instability even if the actually injected d-axis current I_{d0} is equal to zero. Therefore, the finite P gain of the current controller essentially aggravates the instability effect of PLL in the weak grid, and the increase of the P gain of the current controller can only mitigate the reduction of allowed maximum PLL bandwidth.

Given the injection of the rated active power into the system, the allowed maximum PLL bandwidth to guarantee the synchronization stability of the system is influenced by the P gain of the current controller. Fig. 9 shows the allowed maximum PLL bandwidth under different SCRs when different P gains of the current controller are adopted. It is proved that the increase of P gain of the current controller increases the allowed maximum PLL bandwidth and the limitation value of such bandwidth is reached when the P gain is approximately infinite, i.e., the current control loop is idealized with the unity closed-loop gain. Thus, it is suggested that the larger proportional gain of the current controller is preferred to utilize the higher bandwidth of PLL and simultaneously guarantee the system stability.

Fig. 10 shows the Nyquist plot of the open-loop gain T under different proportional gains of the current controller, where the bandwidth of PLL is designed as 90 Hz (see point A in Fig. 9). It can be seen that Nyquist curves encircle the critical point (-1, 0) when the proportional gains of the current controller are chosen as K_p and $4K_p$, which implies the unstable systems. When further increasing the proportional gain of the current controller to $8K_p$, the Nyquist curve does not encircle the critical point, and the system is keeping stable.

C. Impacts of VFF Control Loop on the Synchronization Dynamics

VFF control is commonly used to enhance the transient performance of VSC. It may further interact with the synchronization dynamics between the PLL and weak grid, and even cause grid synchronization instability. The transfer function matrix of the LPF $\boldsymbol{H}_f$ used with VFF control can be expressed by

$$\mathbf{H}_f = \begin{bmatrix} \frac{\alpha_f}{s+\alpha_f} & 0 \\ 0 & \frac{\alpha_f}{s+\alpha_f} \end{bmatrix} \tag{22}$$

where α_f means the cutoff frequency of the LPF. $\boldsymbol{G}_{PLL}^{v}$ represents the PLL effects on the transformed PCC voltage that is used for the VFF control. It can be written as

$$\mathbf{G}_{\mathrm{PLL}}^{v} = \begin{bmatrix} 0 & -V_{q0}H_{pll} \\ 0 & V_{d0}H_{pll} \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \tag{23}$$

where V_{dq0} is the steady-state value of PCC voltage in the dq-frame.

Fig. 11 illustrates the equivalent block diagram of the grid-connected VSC. To simplify the analysis, the impact of VFF control on synchronization dynamics can be decomposed into two parts: $\boldsymbol{H}_f\boldsymbol{G}_{PLL}^{v}\boldsymbol{Z}_g$ and $\boldsymbol{H}_f\boldsymbol{Z}_g$, where the PLL effects

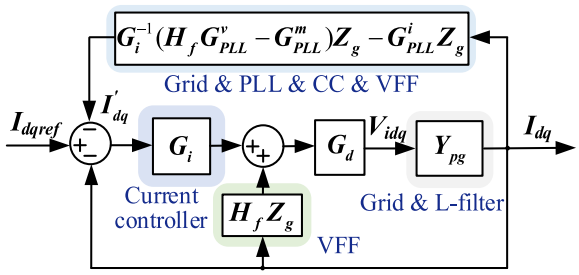

Fig. 11. Equivalent block diagram of grid-connected VSC considering VFF control.

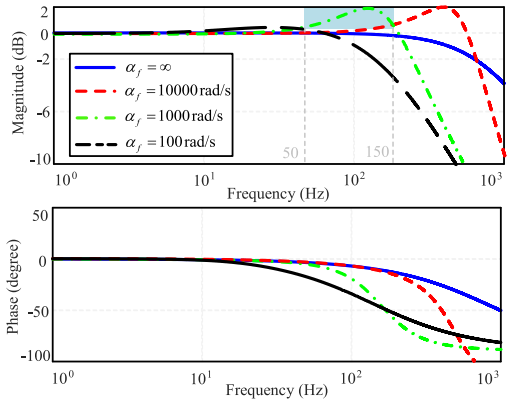

Fig. 12. Bode plot of G_{c11} under different cutoff frequencies of LPF used with VFF.

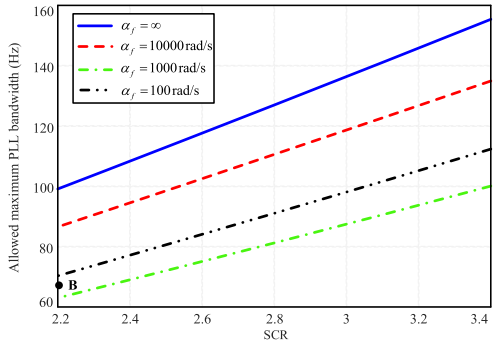

Fig. 13. Allowed maximum PLL bandwidth with different cutoff frequencies of LPF used with VFF.

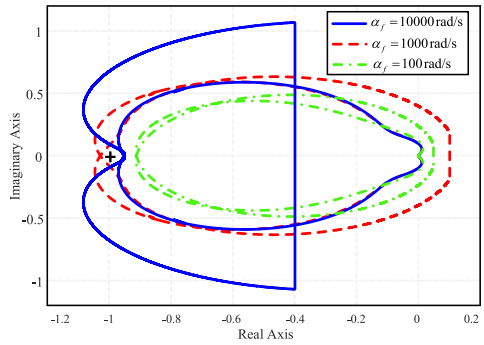

Fig. 14. Nyquist plot of open-loop gain under different cutoff frequencies of LPF used for VFF control.

on the VFF control is integrated with the interaction matrix while the PCC voltage is directly feedforward into the current controller through an LPF. Therefore, the transfer function of $\boldsymbol{G}_c$ and the characteristic expression of (17) can be correspondingly modified, which are expressed as

$$\mathbf{G}_c = [\mathbf{I} + \mathbf{Y}_{pg}\mathbf{G}_i\mathbf{G}_d - \mathbf{Y}_{pg}\mathbf{G}_d\mathbf{H}_f\mathbf{Z}_g]^{-1}\mathbf{Y}_{pg}\mathbf{G}_i\mathbf{G}_d \quad (24)$$

$$CE = 1 + \underbrace{G_{c11}\left(-sL_gH_{pll}\right)\left(I_{d0}^e - \frac{\alpha_f}{s+\alpha_f}\frac{V_{d0}}{K}\right)}_{T}. \quad (25)$$

Fig. 12 shows the Bode plot of G_{c11} under different cutoff frequencies of LPF used for VFF. It can be seen that the current controller integrated with the VFF control loop, i.e., $\boldsymbol{H}_f\boldsymbol{G}_{PLL}^v\boldsymbol{Z}_g$ can be considered as the band-pass amplifier. The corner frequency of the amplifier is located around the synchronization frequency range when the cutoff frequency of LPF is selected at 1000 rad/s, which may amplify the disturbance around the synchronization frequency range and even results in system instability. On the other hand, based on (25), it can be found that the PLL effects on VFF control, i.e., $\boldsymbol{H}_f\boldsymbol{G}_{PLL}^v\boldsymbol{Z}_g$ is to help counteract the negative impacts of the PLL on the modulated voltage, i.e., the equivalently injected d-axis current I^e_{d0} is reduced. Therefore, the larger cutoff frequency of LPF is beneficial for the enhancement of synchronization stability from the aspects of this term.

Fig. 13 depicts the allowed maximum PLL bandwidth under different SCRs when different cutoff frequencies of LPF used for VFF are adopted. It can be seen from the figure that when the cutoff frequency of LPF is equal to 1000 rad/s, the allowed maximum value of PLL bandwidth is the lowest among those cases. The much higher cutoff frequency (>10000 rad/s) of LPF significantly increases the allowed maximum value of PLL bandwidth, while the lower cutoff frequency of LPF also increases the allowed maximum value due to the counteracting effects. However, different cutoff frequencies of LPF in the term of $\boldsymbol{H}_f\boldsymbol{Z}_g$ cause the disturbance amplifying effects at different frequency ranges, which causes the nonmonotonic impact of the cutoff frequency of LPF used with VFF on the synchronization dynamics.

Fig. 14 shows the Nyquist plot of open-loop gain T under different cutoff frequencies of LPF used with VFF, where the bandwidth of PLL is set at 65 Hz (see point B in Fig. 13). It can be seen that the system is unstable when the cutoff frequency of LPF is chosen as 1000 rad/s. However, the system will become stable again, either increasing or decreasing the cutoff frequency of LPF. It further proves that the cutoff frequency of LPF poses a nonmonotonic impact on synchronization stability.

D. Impacts of Reactive Current on the Synchronization Dynamics

When $I_{q0} \neq 0$, the open-loop transfer function can be expressed as

$$T = G_{c11}[-H_{pll}\underbrace{(sL_gI_{d0}^e - \omega_1 L_g I_{q0})}_{\Delta V_{g0}}] \quad (26)$$

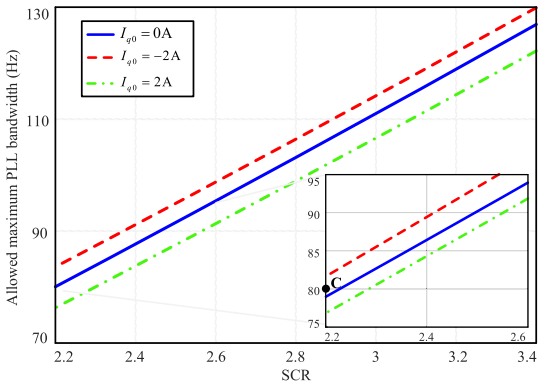

Fig. 15. Allowed maximum PLL bandwidth with different reactive currents injection.

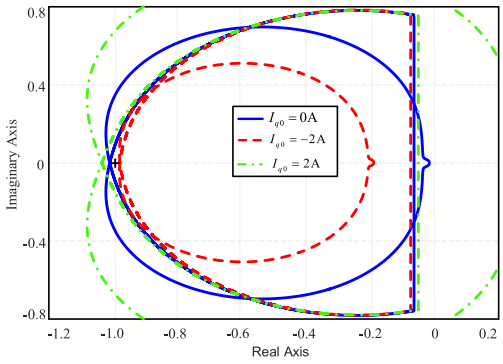

Fig. 16. Nyquist plot of open-loop gain under different reactive currents injection.

where ΔV_{g0} means the voltage dip on the grid impedance. Since the grid voltage is stiff, the PCC voltage is, thus, determined by the voltage dip. When the injected reactive current $I_{q0}<0$, the PCC voltage will be increased, and the SCR would increase correspondingly, which helps to improve the synchronization stability.

Fig. 15 illustrates the allowed maximum PLL bandwidth with different reactive current injections. It can be found that the injection of capacitive reactive current helps to increase the allowed maximum value of the PLL bandwidth, while the injection of inductive reactive current would reduce this value.

Fig. 16 shows the Nyquist plot of open-loop gain under different reactive current injections, where the bandwidth of PLL is designed as 80 Hz (see point C in Fig. 15). When the capacitive reactive current is injected into the system, the Nyquist curve will not encircle the critical point, and the system is stable. Thus, it is further proved that the injection of capacitive reactive current increases the stability margin while the injection of inductive reactive current may destabilize the system.

E. Impact of DC Voltage Controller on the Synchronization Dynamics

There are two possible operating scenarios relevant to the dc-link dynamics. The first scenario is that the dc-link voltage control (DVC) is controlled by a front-end converter (e.g., high-voltage dc system [18]) or an energy storage unit [19] is connected to the dc link. In this case, the dc-link voltage can be assumed as constant, and it, thus, does not influence the synchronization stability [20], [21]

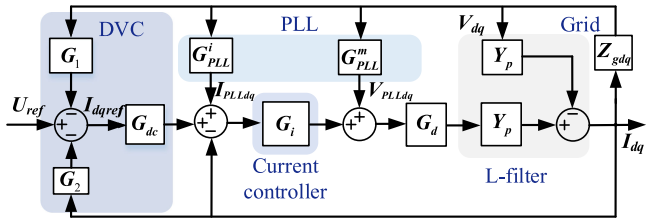

Fig. 17. Block diagram of the small-signal model of VSC connected with the grid when the dc voltage controller is adopted.

The second scenario is that the dc-link voltage is regulated by the VSC. For this scenario, the analysis method proposed in the work is still applicable. The cutoff frequency of the dc-link voltage controller is usually designed to be much slower (one order of magnitude) than that of current control dynamics [2]. Based on which, a detailed discussion on the impacts of dc-link dynamics has been given in the following part. It is found that the dc-link voltage controller has little effect on the synchronization stability. Thus, the previously analyzed results for the impact of the current controller on the synchronization stability will not be affected by the dc voltage controller.

Fig. 17 shows the block diagram of the small-signal model of VSC connected with the grid when the dc voltage controller is considered, where the reactive current reference is directly given as I_{qref}. $\boldsymbol{G}_{\rm dc}$ means the PI controller of dc voltage control. $\boldsymbol{G}_1$ and $\boldsymbol{G}_2$ represent the transfer function matrix related to dc dynamics, which can be expressed as

$$\boldsymbol{G}_1 = \begin{bmatrix} \frac{-I_{d0}}{sU_{\rm dc0}C_{\rm dc}} & \frac{-I_{q0}}{sU_{\rm dc0}C_{\rm dc}} \\ 0 & 0 \end{bmatrix} \tag{27}$$

$$\boldsymbol{G}_2 = \begin{bmatrix} \frac{-(U_{d0}-I_{d0}sL_f)}{sU_{\rm dc0}C_{\rm dc}} & \frac{I_{q0}sL_f}{sU_{\rm dc0}C_{\rm dc}} \\ 0 & 0 \end{bmatrix} \tag{28}$$

where $U_{\rm dc0}$ denotes the steady-state value of the dc voltage, $C_{\rm dc}$ is the capacitor of the dc link. The detailed modeling process of dc voltage control dynamics can be found in [2], which will not be elaborated in this article.

Based on Fig. 17, the equivalent block diagram of the interaction matrix including the DVC is obtained, as shown in Fig. 18. To analyze the impact of DVC on the synchronization dynamics, the interaction matrix $\boldsymbol{G'}$ is also derived, where $\boldsymbol{G}_0$ means the equivalent transfer function matrix related to dc voltage dynamics, which can be written as

$$\mathbf{G}_0 = \mathbf{G}_1\mathbf{Z}_{gdq} + \mathbf{G}_2. \tag{29}$$

According to Fig. 18, the equivalent MIMO diagram can be also obtained, which is similar as Fig. 8. Correspondingly, two SISO models, as shown in (15) and (16), can also be derived. Similarly, the characteristic expression of those SISO models

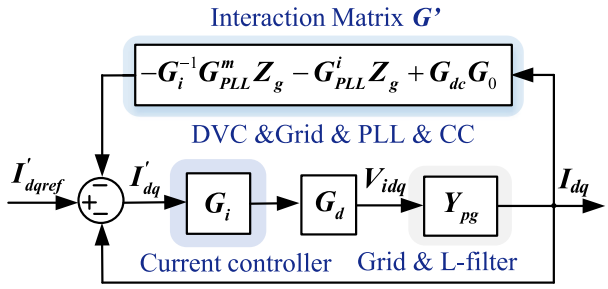

Fig. 18. Equivalent block diagram of the interaction matrix including the dc voltage controller.

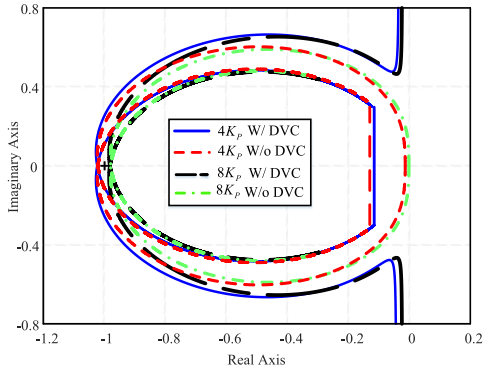

Fig. 19. Nyquist plot of open-loop gain under different P gains of the current controller with/without considering the dc voltage controller.

are the same, which can be rewritten as

$$CE' = 1 + G_{c11}\left[L_g H_{pll}\left(\omega_1 I_{q0} - sI_{d0} - \frac{sU_{d0}}{G_i}\right) + G_{\rm dc}G_{11} + G_{dc}G_{12}H_{pll}L_g\left(-sI_{d0} - \frac{sU_{d0}}{G_i}\right)\right] \tag{30}$$

where

$$G_{11} = \frac{sI_{d0}(L_g - L_f) + U_{d0} + \omega_1 I_{q0}L_g}{sC_{\rm dc}U_{\rm dc0}} \tag{31}$$

$$G_{12} = G_{11} + \frac{I_{d0}L_g\omega_1^2}{s^2 C_{\rm dc}U_{\rm dc0}}.$$

Compared with (19), it is noted that the second term of (30), which is related to the interaction between PLL, grid impedance and current controller, is the same as (19), while the third term of (30) is related to dc dynamics.

Fig. 19 shows the Nyquist plot of open-loop gain of (30) under different P gains of the current controller with/without the dc voltage controller. It can be found that whether the dc voltage controller is considered does not affect the stability margin around the synchronization frequency range, which proves that the dc-link dynamics rarely influence the interaction between PLL, current controller and grid impedance if the cutoff frequency of DVC is designed to be one order magnitude of the current controller. This article mainly focuses on the current controller design considering the synchronization dynamics.

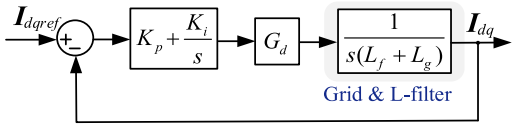

Fig. 20. Block diagram of the current controller considering the grid impedance.

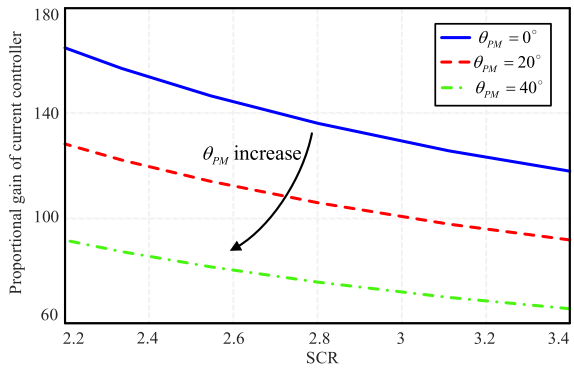

Fig. 21. Proportional gain of the current controller under different SCRs with different phase margins.

For simplicity, the dc voltage controller is not considered in the later section.

IV. Current Controller Design for Synchronization Stability Enhancement

After the investigation on the impacts of the current controller, VFF and reactive current injection on the PLL-induced synchronization stability, the current controller is redesigned to guarantee the synchronization stability of the system.

A. Current Controller Design Based on Time Delay

The conventional current controller is designed based on the time delay and the grid is assumed stiff. Yet, the parameters of the current controller need to be retuned when considering the impact of grid impedance. Fig. 20 illustrates the block diagram of the current controller considering the grid impedance. The proportional gain of the current controller can be calculated based on the time delay and phase margin θ_{PM} [11], which can be expressed as

$$K_p = \frac{\pi - 2\theta_{PM}}{3T_s}(L_f + L_g). \tag{32}$$

Fig. 21 gives the proportional gain of the current controller under different SCRs, where different phase margins are used for the controller design. It can be found that the smaller SCR, i.e., the larger grid impedance yields the higher proportional gain of the current controller. Furthermoe, with the increase of phase margin, the proportional gain of the current controller will be decreased.

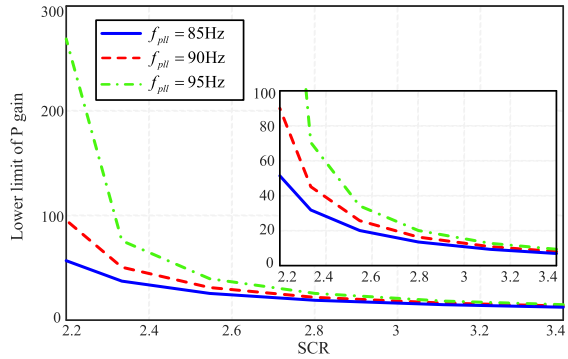

Fig. 22. Lower limit of P gain of the current controller under different SCRs with different PLL bandwidths.

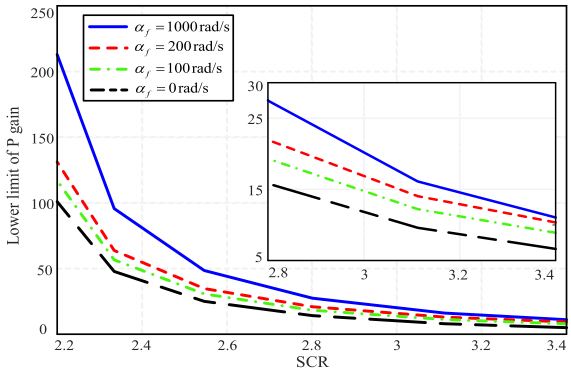

Fig. 23. Lower limit of P gain of the current controller under different SCRs with different cutoff frequencies of LPF for VFF.

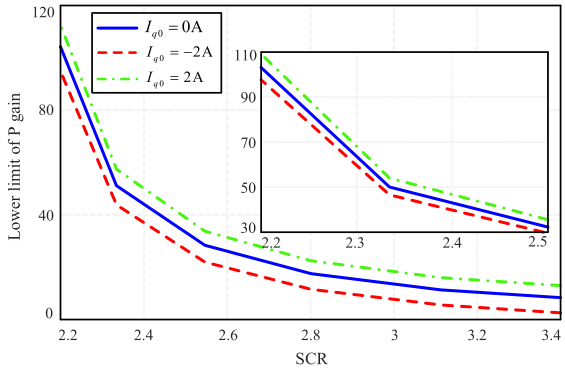

Fig. 24. Lower limit of P gain of the current controller under different SCRs with different injections of reactive current.

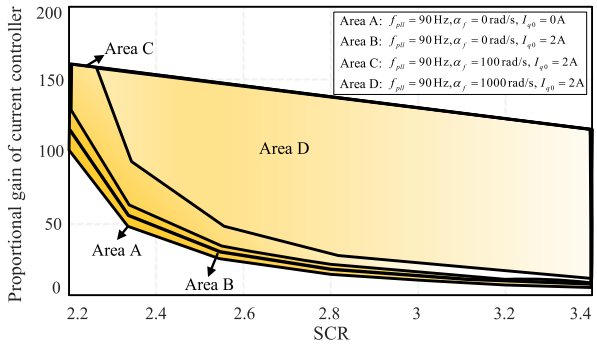

Fig. 25. Boundary of P gain of the current controller under different SCRs with f_{pll}= 90 Hz.

B. Design Guideline of the Current Controller for the Synchronization Stability Enhancement

Based on the previous interaction analysis, the lower limit value of the P gain of the current controller can be yielded to guarantee system stability.

Fig. 22 shows the lower limit of P gain of the current controller under different SCRs, where different bandwidths of PLL are adopted. As the SCR decreases, the lower limit of P gain of the current controller is increased. Furthermore, a larger proportional gain of the current controller is required to guarantee the synchronization stability of the system when a higher bandwidth of PLL is implemented. However, when the PLL bandwidth is larger than the allowed maximum value, the system will become unstable, and no matter how to choose the P gain of the current controller cannot help stabilize the system.

Given the designed PLL bandwidth below the allowed maximum value, Fig. 23 depicts the lower limit of P gain of the current controller under different SCRs when different cutoff frequencies of LPF used with VFF are adopted. It can be found that the higher cutoff frequency of LPF requires a higher P gain of the current controller so that the system is kept stable. Among those cases, the largest value of the P gain of the current controller is reached when the cutoff frequency of LPF is chosen at 1000 rad/s. With the decrease of the cutoff frequency of LPF, the lower limit value of the P gain of the current controller decreases.

Fig. 24 illustrates the lower limit of P gain of the current controller under different SCRs when different reactive currents are injected into the system. It can be seen that the larger P gain of the current controller is required to guarantee synchronization stability when the inductive reactive current is injected into the system and vice versa.

Since the PLL bandwidth, the cutoff frequency of LPF used with VFF and the injection of reactive current influence the synchronization stability, the lower limit value of the P gain of the current controller should be calculated with the consideration of those factors. Based on the upper limit (see Fig. 21) and the lower limit (see Figs. 22–24), the boundary of P gain of the current controller under different SCRs can be formulated, as illustrated in Fig. 25. It can be seen that the boundary of the P gain is shrunk with the consideration of capacitive reactive current injection and a higher cutoff frequency of LPF used with VFF.

The design guideline for the current controller can be summarized as: 1) given an SCR, the allowed maximum PLL bandwidth is reached when the current controller is idealized with unity closed-loop gain, as shown in Fig. 9; 2) given the PLL bandwidth below the maximum value, the P gain of the current controller is calculated with the consideration of the reactive current injection and the impact of VFF control on synchronization dynamics,

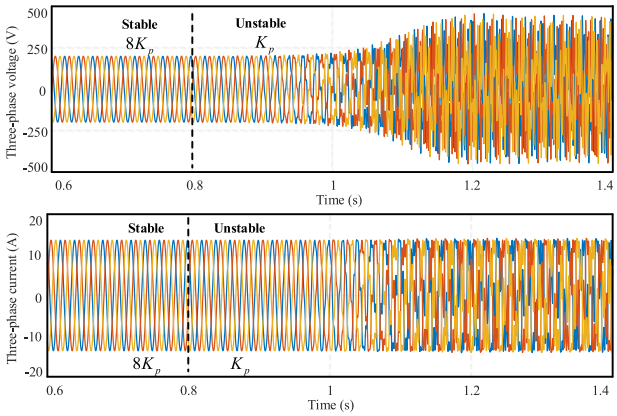

Fig. 26. Simulated results of PCC voltage and current with different P gains of the current controller.

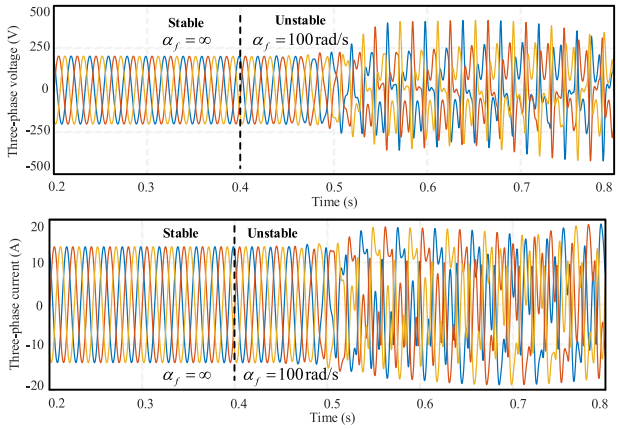

Fig. 27. Simulated results of PCC voltage and current with a high cutoff frequency of LPF used with VFF.

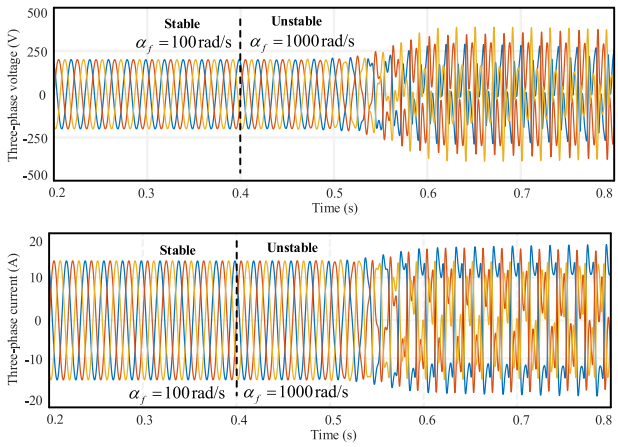

Fig. 28. Simulated results of PCC voltage and current with a low cutoff frequency of LPF used with VFF.

which achieves codesign of the current controller and VFF control, as shown in Fig. 25.

Furthermore, with the VFF control loop, a small integral gain of the current controller can be employed, as the purpose of an integral part is to mitigate the steady-state influence between actual and model inductances and the voltage drop across the filter resistance. It is recommended that the integral gain is selected as the product of the cutoff frequency of the current controller and the filter resistance [2], which should give a sufficiently small gain (approximately zero). Thus, the impact of the integral gain of the current controller on synchronization dynamics has not been discussed in this article.

V. Simulation and Experiment Verification

To verify the accuracy of the theoretical analysis and effectiveness of the controller design guideline, the time-domain simulations, and experiment tests are carried out. The parameters of VSC are presented in Table I.

A. Simulation Validation

Fig. 26 illustrates the simulation results of PCC voltage and current with different proportional gains of the current controller, where the bandwidth of PLL is designed as 90 Hz. When the proportional gain is switched from $8K_p$ to K_p at 0.8 s, the system will become unstable. These results agree with the theoretical analysis of Fig. 10, which proves that the increase of proportional gain of the current controller helps to enhance the synchronization stability of the system.

Fig. 27 shows the simulation results of PCC voltage and current when the high cutoff frequency of LPF used for VFF is adopted. At 0.5 s, the cutoff frequency of LPF is changed from $\alpha_f = \infty$ to $\alpha_f = 100$ rad/s, where the PLL bandwidth is set at 80 Hz (larger than the upper limit, as shown in Fig. 13). The system becomes unstable when a lower cutoff frequency of LPF is adopted, which aligns with the theoretical analysis of Fig. 13.

Fig. 28 gives the simulation results of PCC voltage and current when the low cutoff frequency of LPF used for VFF is used. At 0.5 s, the cutoff frequency of LPF is changed from $\alpha_f = 100$ rad/s to $\alpha_f = 1000$ rad/s, where the bandwidth of PLL is selected as 65 Hz (larger than the upper limit, as shown in Fig. 13). It is noted that the higher cutoff frequency of LPF for VFF may also cause synchronization instability. Compared with Fig. 27, it is summarized that the impact of the cutoff frequency of LPF on synchronization dynamics is nonmonotonic, where the worst case might occur when the cutoff frequency of LPF is close to 1000 rad/s.

Fig. 29 depicts the simulation results of PCC voltage and current when the capacitive reactive current is gradually injected into the system. Fig. 30 illustrates the simulation results of PCC voltage and current when the inductive reactive current is gradually injected into the system. By comparison, it can be found that the injection of the capacitive reactive current is helpful for the enhancement of the synchronization stability, while the injection of the inductive reactive current tends to destabilize the system and reduce the stability margin.

B. Experiment Validation

To further verify the accuracy of the theoretical analysis, the experiments on a laboratory test setup, as shown in Fig. 31, are

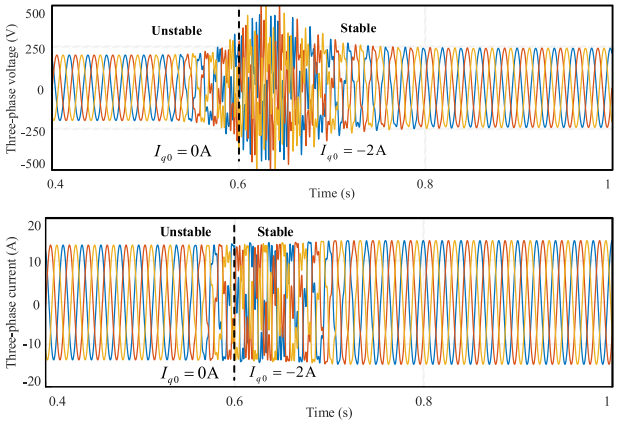

Fig. 29. Simulated results of PCC voltage and current with the injection of capacitive reactive current.

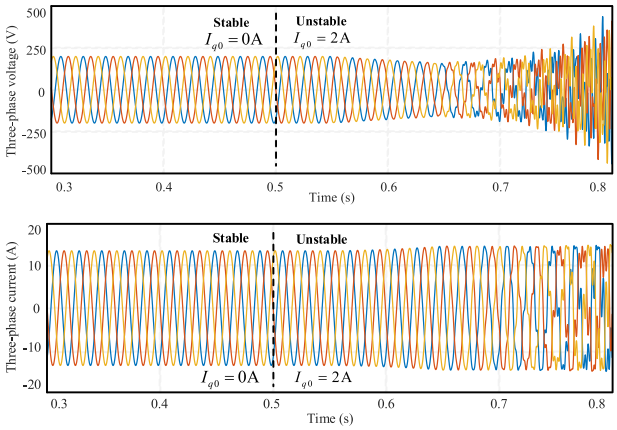

Fig. 30. Simulated results of PCC voltage and current with the injection of inductive reactive current.

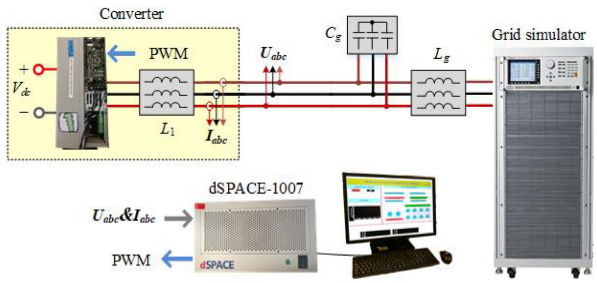

Fig. 31. Experiment setup.

carried out. All the parameters used in the time-domain simulation are tested in experiments. A Danfoss converter is adopted as the grid-connected VSC. The DS1007dSPACE system is used for the control system, where the DS5101 digital waveform output board is employed for generating the switching pules, and the DS2004 A/D board is adopted for the voltage and current measurements. The programmable three-phase voltage source is used to emulate the power grid, and a constant dc voltage supply is used at the dc side.

Fig. 32 shows the experiment results of PCC voltage and current with different proportional gains of the current controller,

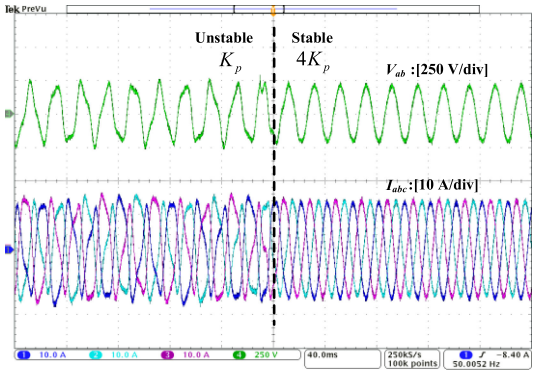

Fig. 32. Experiment results of PCC voltage and current with different proportional gains of the current controller.

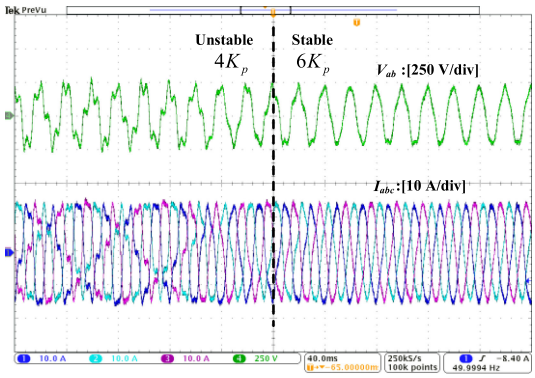

Fig. 33. Experiment results of PCC voltage and current with higher proportional gains of the current controller.

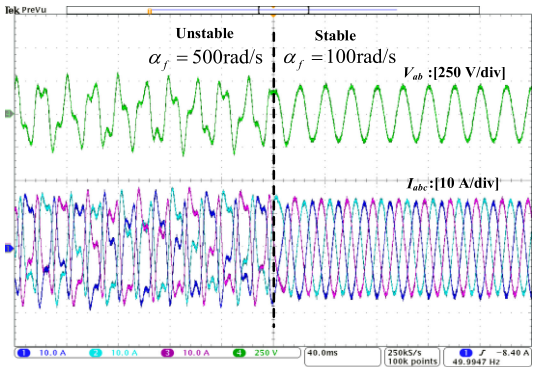

Fig. 34. Experiment results of PCC voltage and current with a lower cutoff frequency of LPF for VFF.

where the bandwidth of PLL is selected as 86 Hz. The proportional gain is first set as K_p and the system is unstable, and then the system becomes stable with the increase of the proportional gain of the current controller to $4K_p$. The bandwidth of PLL is further increased to 90 Hz, and the system becomes unstable again. When the proportional gain of the current controller is increased to $6K_p$, the system is stabilized, as shown in Fig. 33.

Fig. 34 illustrates the experiment results of PCC voltage and current when the cutoff frequency of LPF for VFF control is

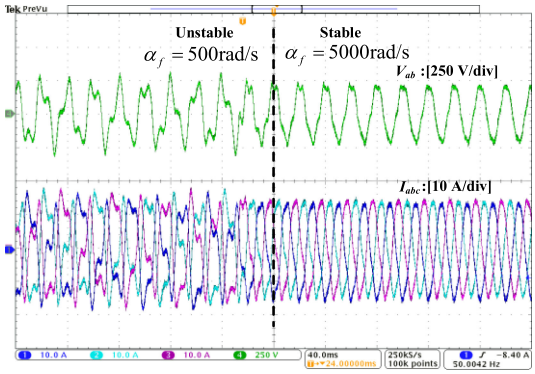

Fig. 35. Experiment results of PCC voltage and current with a higher cutoff frequency of LPF for VFF.

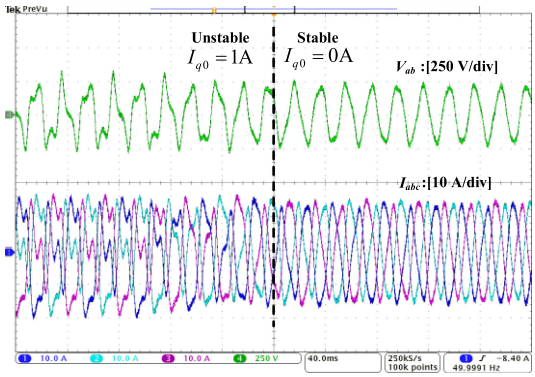

Fig. 36. Experiment results of PCC voltage and current with the injection of inductive reactive current.

changed from 500 rad/s to 100 rad/s, where the bandwidth of PLL is set as 66 Hz. It is noted that the lower cutoff frequency of LPF for VFF is beneficial for the improvement of the synchronization stability.

Fig. 35 illustrates the experiment results of PCC voltage and current when the cutoff frequency of LPF for VFF control is changed from 500 rad/s to 5000 rad/s, where the bandwidth of PLL is set as 66 Hz. Compared with Fig. 34, it can be found that the higher cutoff frequency of LPF for VFF also helps to enhance synchronization stability. Therefore, the impact of the cutoff frequency of LPF used for VFF is nonmonotonic, and there exists the worst case when the cutoff frequency of LPF is located between 500 and 5000 rad/s.

Fig. 36 illustrates the experiment results of PCC voltage and current when the inductive reactive current is injected into the system, where the bandwidth of PLL is set as 86 Hz. The system is unstable when the inductive reactive current is injected into the system, and the system is stable again when there is no reactive current injected into the system.

Fig. 37 depicts the experiment results of PCC voltage and current when the capacitive reactive current is injected into the system, where the bandwidth of PLL is designed as 87 Hz. It is found that the system is unstable when there is no reactive current injected into the system, and the injection of the capacitive reactive current helps to stabilize the system.

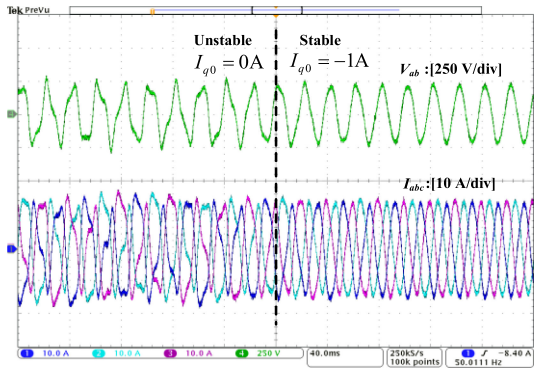

Fig. 37. Experiment results of PCC voltage and current with the injection of capacitive reactive current.

All experimental results match well with simulation results, which further proves the accuracy of the theoretical analysis.

VI. Conclusion

This article has revisited the design of the current controller for VSC with the consideration of the dynamic impacts of PLL, weak grids and VFF control. By integrating the current controller with PLL, grid impedance and VFF control loop, a SISO transfer-function-based model is proposed to characterize the interaction between PLL and the current controller. It is revealed that: 1) finite P gain of the current controller essentially aggravates the instability effect of PLL in weak grids, i.e., the increase of P gain of the current controller can only alleviate such negative effect on the synchronization stability; 2) the injection of capacitive reactive current helps enhance the PLL-induced stability; 3) the cutoff frequency of the LPF used with the VFF control has a nonmonotonic relationship with the synchronization stability.

Then, based on those interaction analysis results, a guideline for the redesign of the current controller is given, which enables a codesign of the current controller and VFF control. Finally, the simulation and experiment results have verified the accuracy of the theoretical analyses.

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